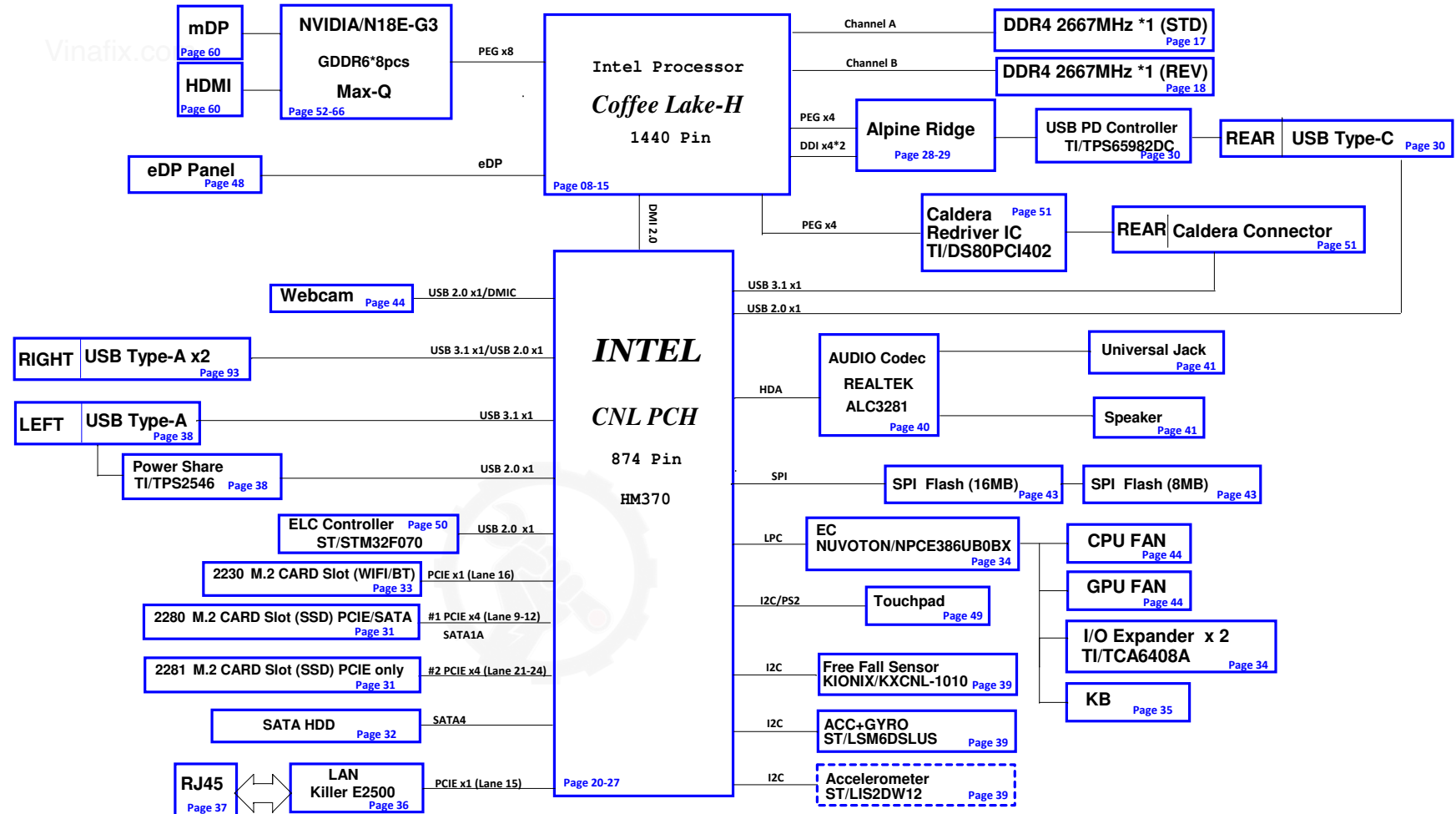


Orion N18E G2/G3-MaxQ (Coffee Lake-H)

Revision_X00

SO-DIMM (support max memory up to 32GB)

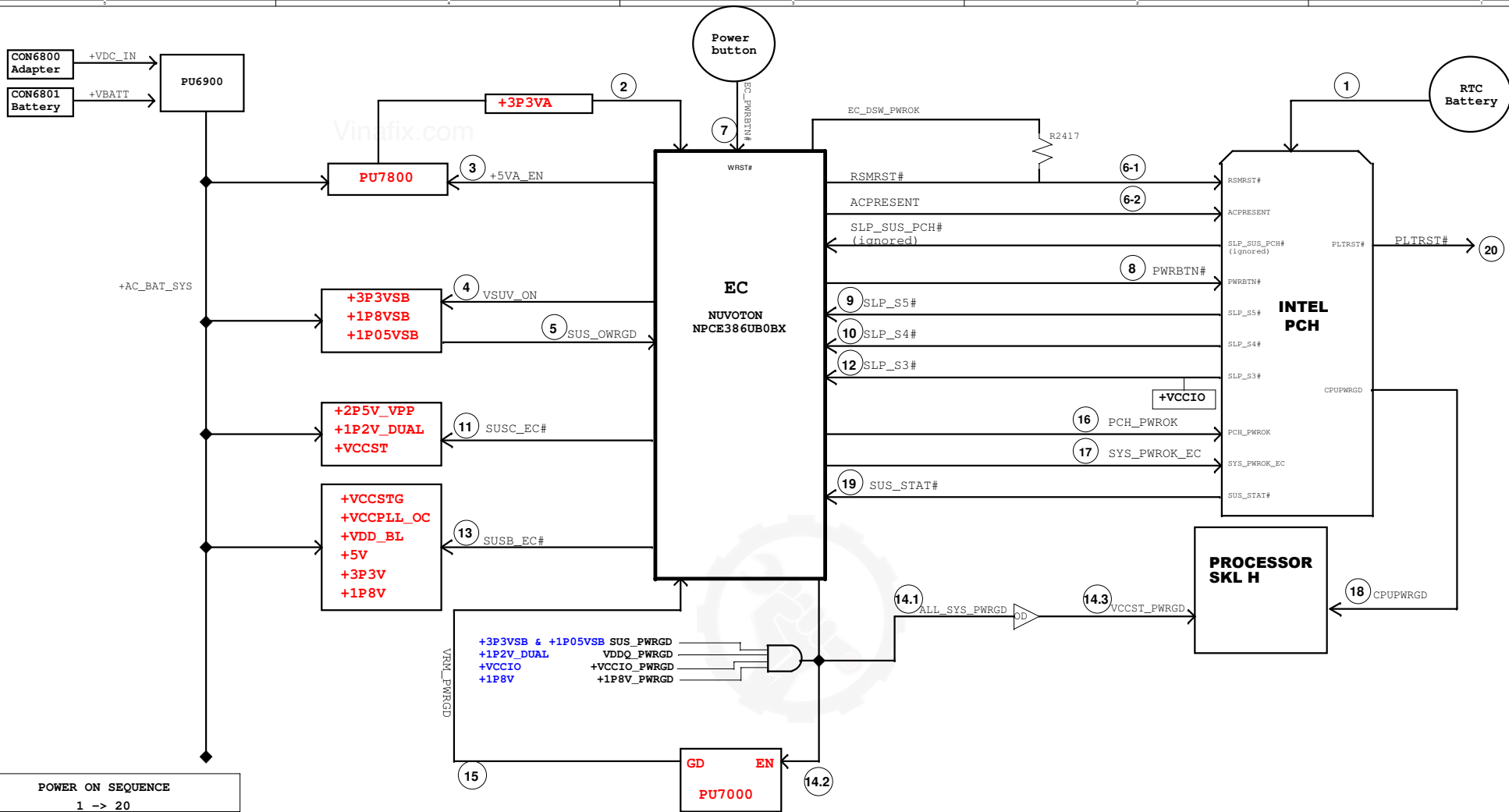


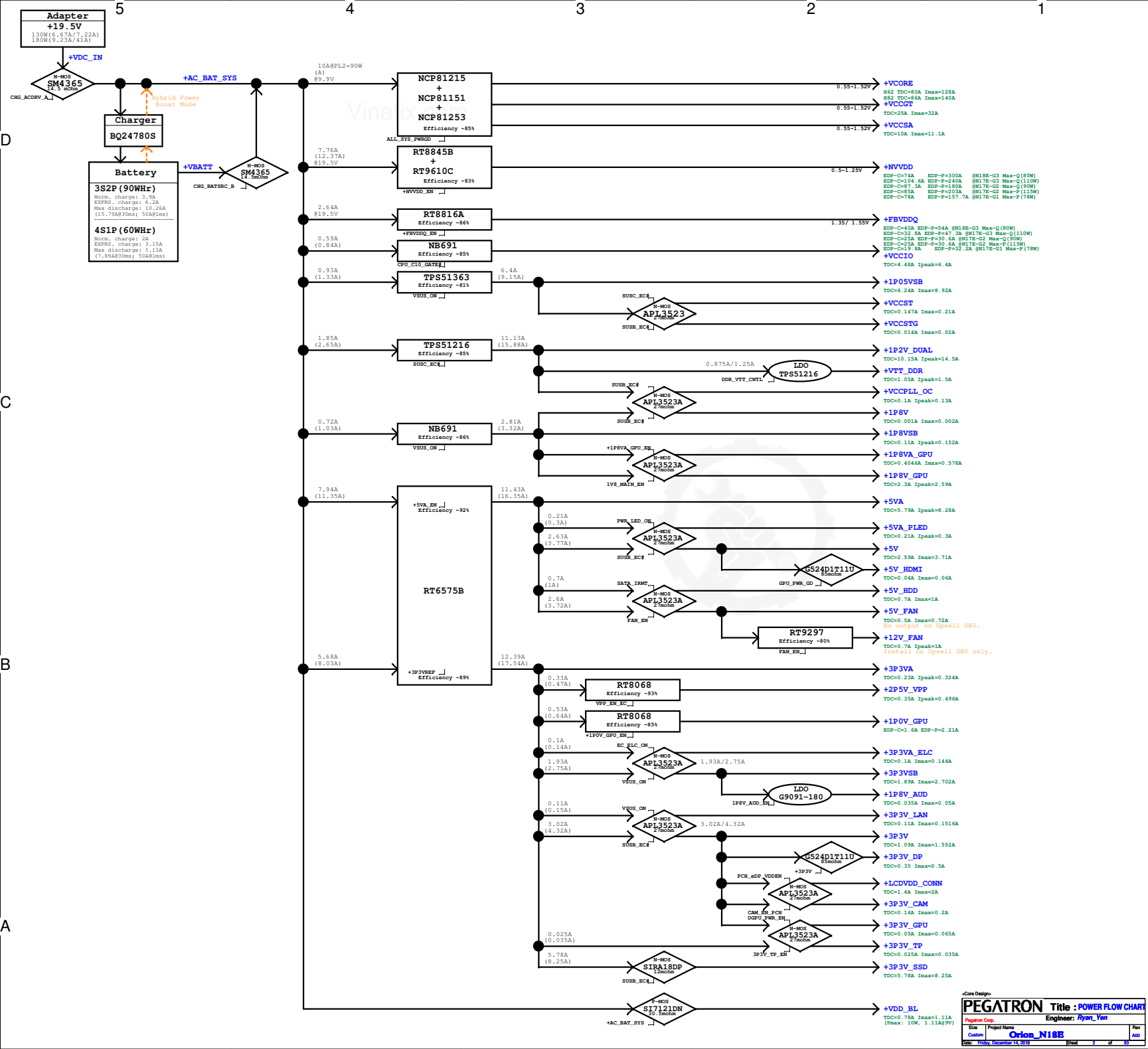
PAGE	TITLE
01	BLOCK DIAGRAM
02	SIGNAL & RESET MAP
03	POWER FLOW CHART
04	CHANGE HISTORY
05	SMBus & I2C Flow
06	GPU Power flow & sequence
07	POWER SEQUENCE
08	CPU DDI/EDP
09	CPU DDR4 CHA
10	CPU DDR4 CHB
11	CPU PCIE/DMI
12	CPU other
13	CPU VSS
14	CPU VCC
15	CPU DECOUPLING
16	ME DISABLE
17	DDR4_SO-DIMM0
18	DDR4_SO-DIMM1
19	DDR4 DECOUPLING
20	PCH DMI PCIE USB SATA
21	PCH SATA/PCIE
22	PCH ESPI/SPI/FAN/HOST
23	PCH AUDIO/CL/I2C/UART
24	PCH SML/I2C/MISC
25	PCH CLOCK
26	PCH VCC/PLL
27	PCH VSS
28	Alpine-Ridge - Controller
29	Alpine-Ridge - Power
30	Alpine-Ridge - PD
31	M.2 2280 SSD #1 & #2
32	SATA HDD
33	M.2 KEY-A 2230 WLAN
34-35	EC_NUVOTON_NPCE386UB0BX
36-37	LAN NIC KILLER & LAN JACK
38	USB CONN and power
39	SENSOR
40	AUDIO CODEC ALC3281
41	AUDIO JACK
42	USB Redriver
43	SM BUS & SPI ROM
44	Other Conn
45-46	PCH/CPU DEBUG TESTPOINT
47	PCB & Label & Screw
48	eDP Conn
49	Touch & Keyboard BL
50	ELC MCU
51	Caldera Redriver & CONN
52	GPU PCIE
53	GPU-Xtal & Straps
54	GPU-BUFFER PARTITION A/B
55	GDDR6 256Mx2Chx16bit _ChA
56	GDDR6 256Mx2Chx16bit _ChB
57	GPU-BUFFER PARTITION C/D
58	GDDR6 256Mx2Chx16bit _ChC
59	GDDR6 256Mx2Chx16bit _ChD
60	HDMI/mDP Conn
61	GPU HDMI/mDP
62	GPU-GPIO
63	GPU-POWER&GND
64	GPU-Decoupling
65	GPU_MIO
66	GPU_IFPAB_DDI

67	GPU_POWER Sequence	88	GPU_POWER_CAP
68	DC_IN	89	GPU POWER DISCHARGE
69	Charger	90	Power Sense
70	VR CONTROLLER	91	+12V_FAN
71-72	Vcore Driver	92	
73	Vccgt Driver	93	CARD-USB CON
74	Vccsa Driver		
75	Vcore & VccGT CAP		
76	+1P05VSB/+2P5VVP		
77	+1P2V_DUAL & +VTDDR		
78	+3VA / +5VA		
79	+VCCIO / +1P8VSB		
80-81	Load switch		
82	NVVDD CONTROLLER		
83-84	NVVDD Driver		
85			
86	+FBVDDQ		
87	+1P0V_GPU/+1P8V_GPU & LDO		

Default component footprint is SMD 0402, Y5V, 5% type. Difference footprint show on schematics.

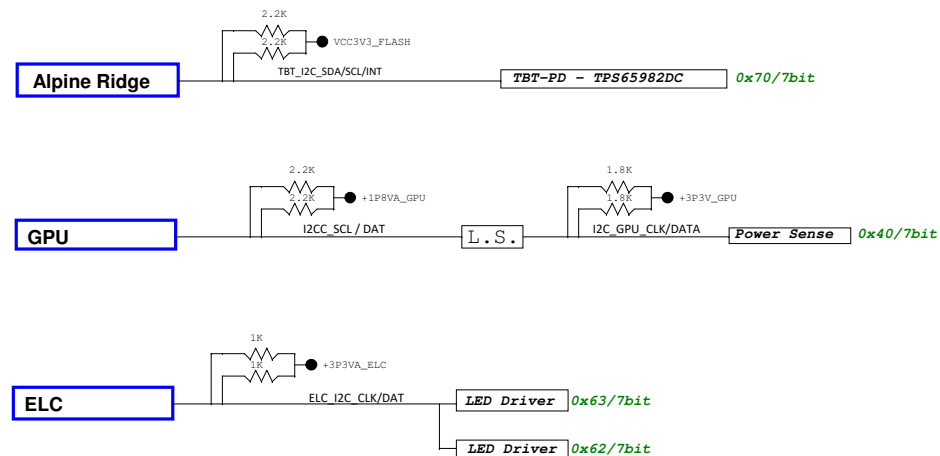
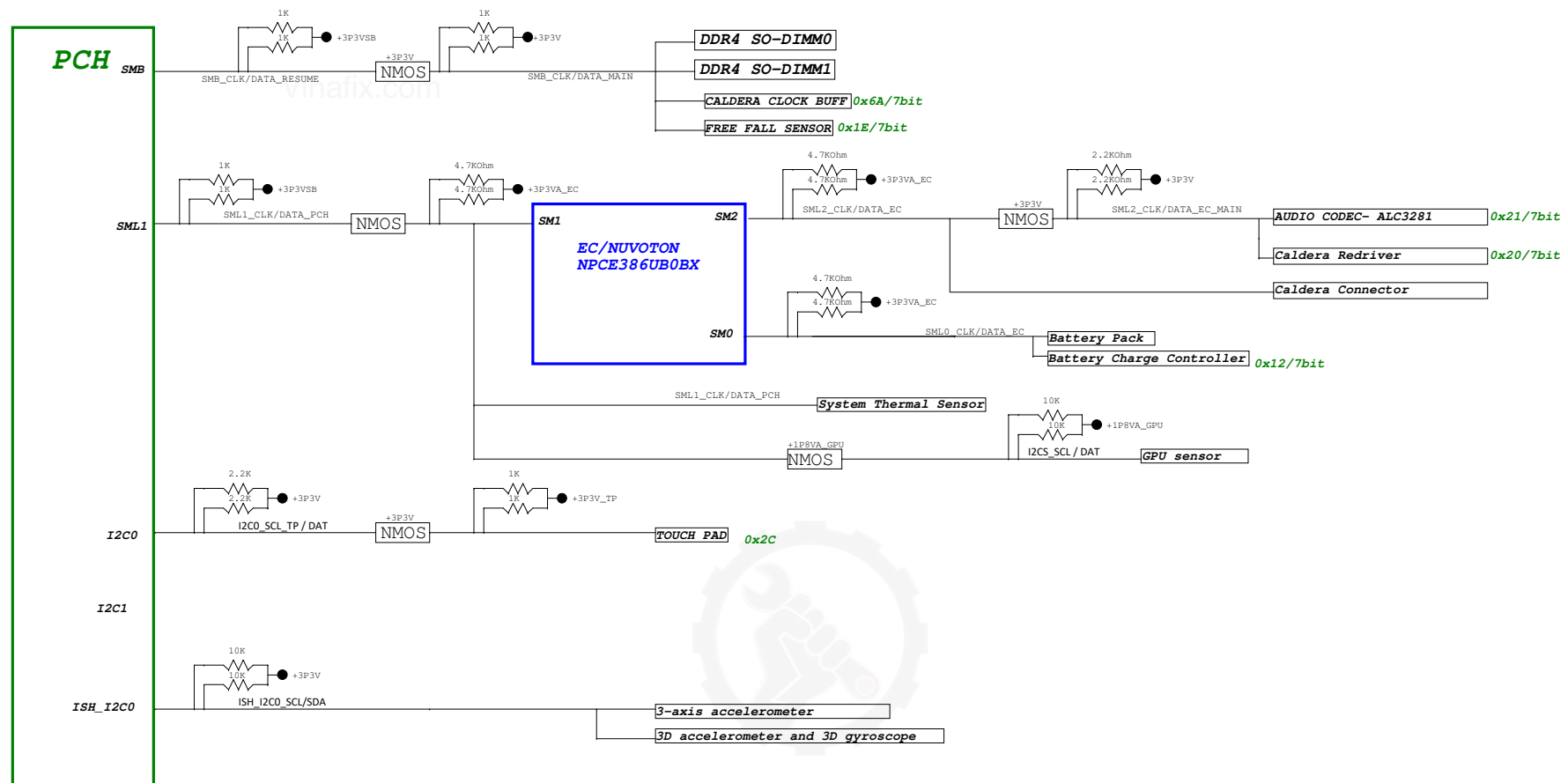
Property: BOM
I = Installed Part.
NI = Not Installed Part.
PROTO = PROTO Phase Only.
VP = Virtual Part.

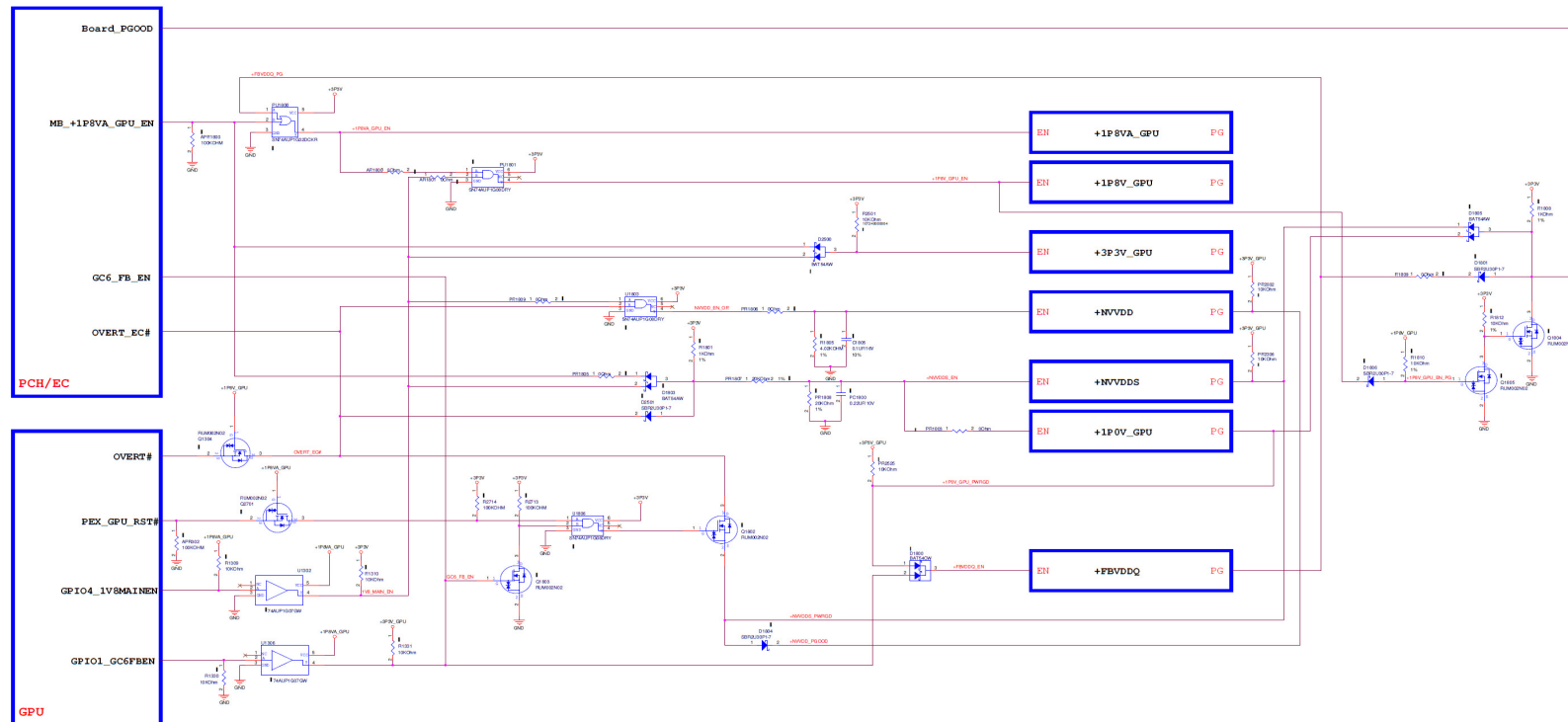
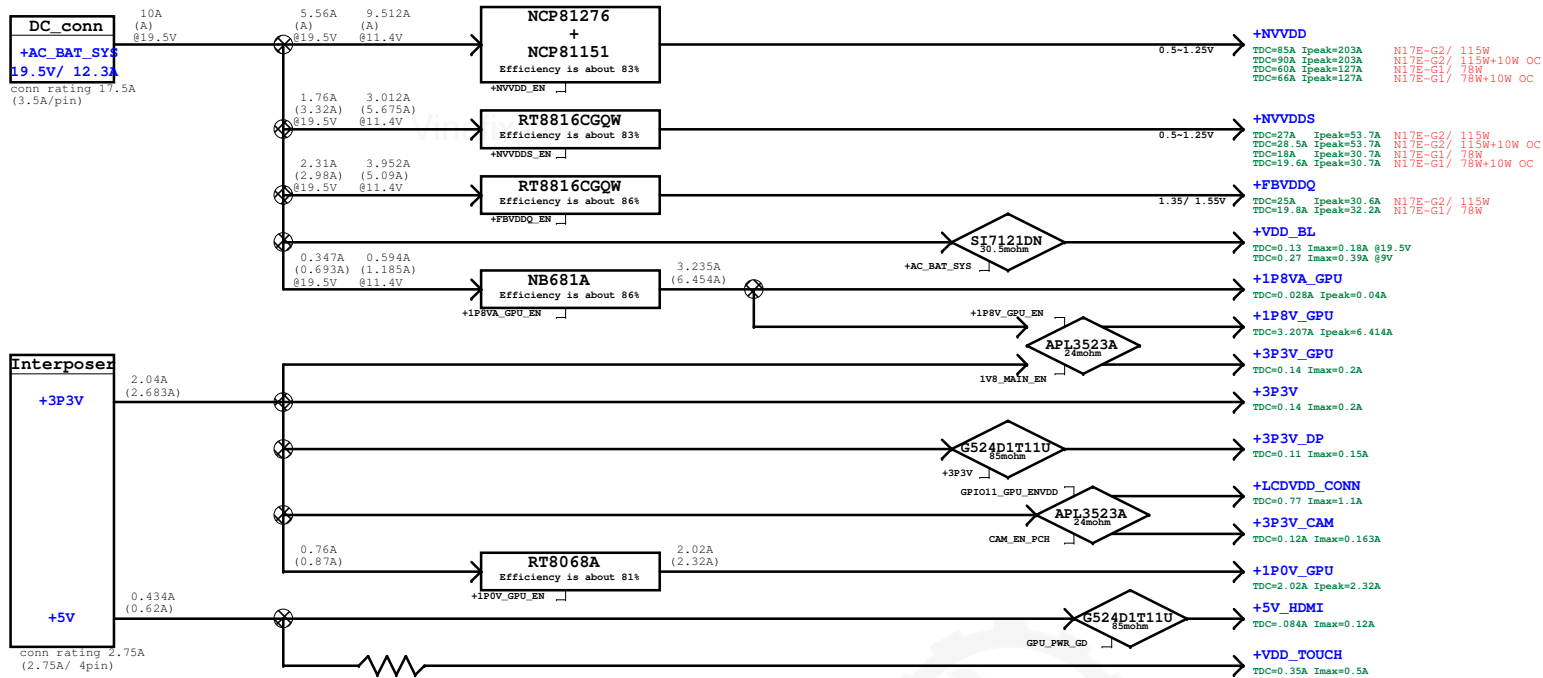




[illegible]

SMBUS & I2C Block Diagram





Vinafix.com



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **POWER SEQUENCE**

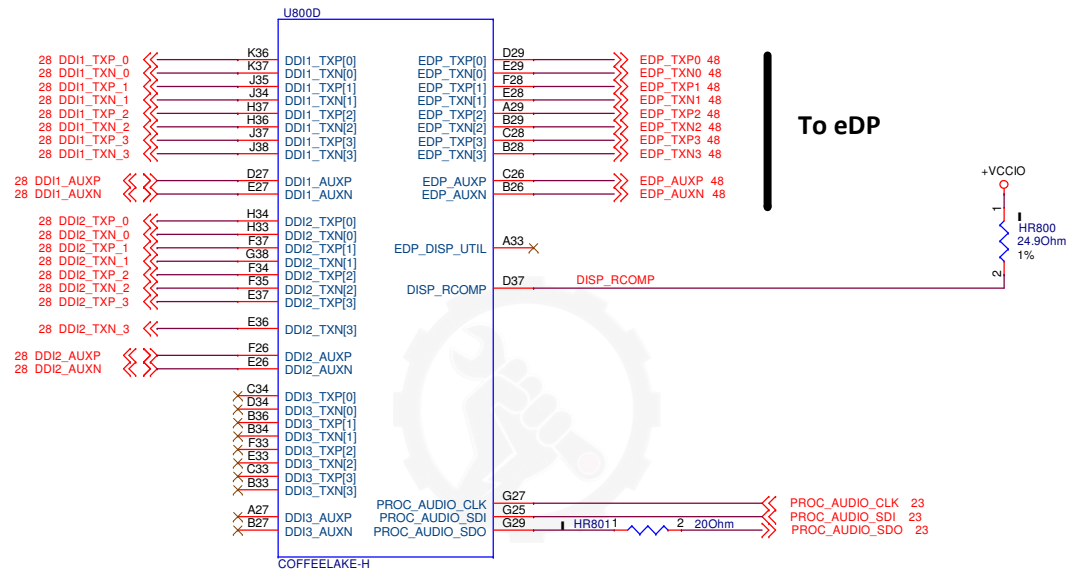
Engineer: **Ryan_Yen**

Size	Project Name	Rev
A2	Orion_N18E	A00

Date: Friday, December 14, 2018 Sheet 7 of 93

To Apline ridge

To eDP



PEGATRON DT-MB RESTRICTED SECRET

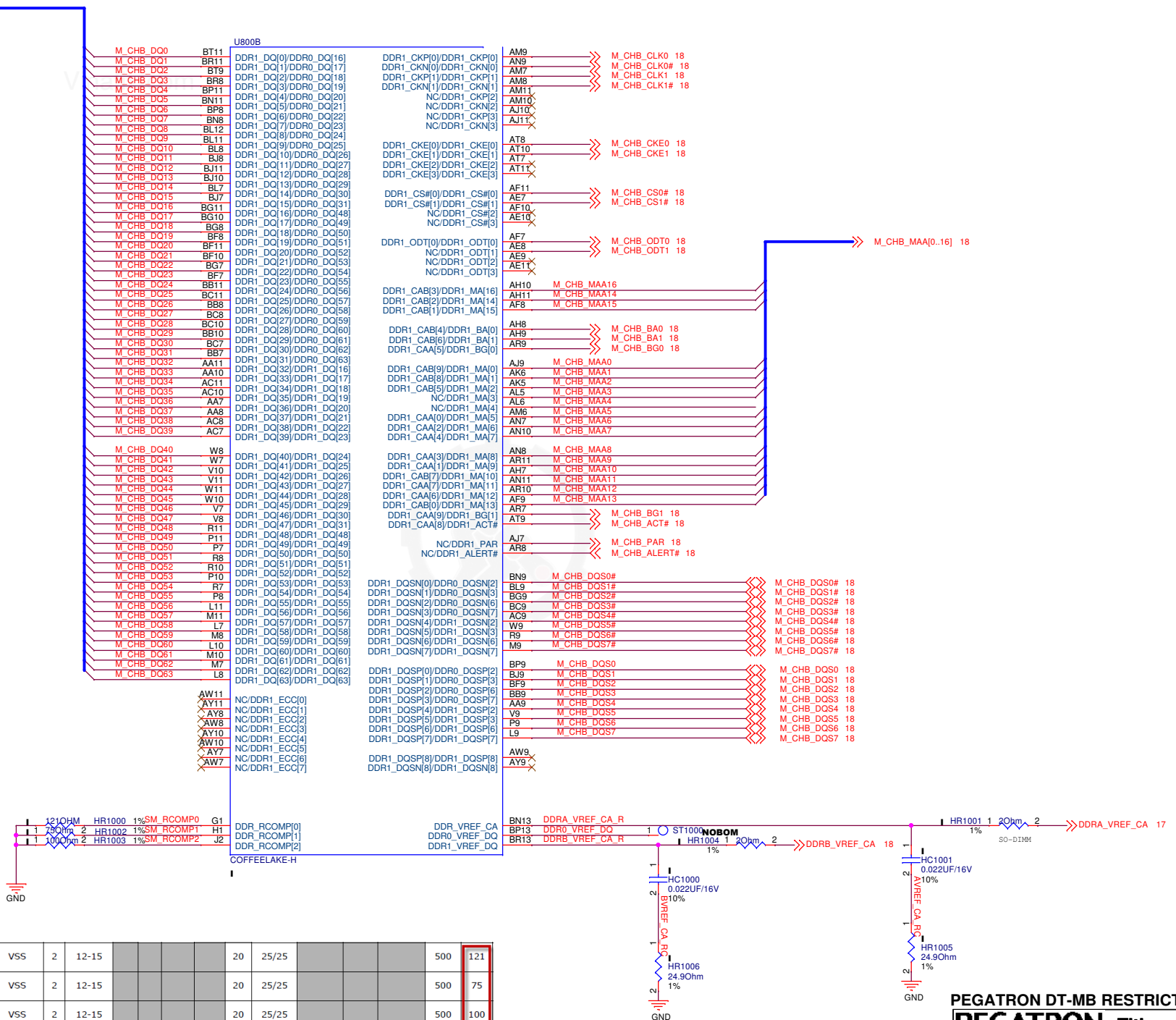
PEGATRON Title : CPU DD/EDP

Pegatron Corp. Engineer: Ryan_Yen

Size A3 Project Name Orion_N18E Rev A00

Date: Friday, December 14, 2018 Sheet 8 of 93

18 M_CHB_DQ[0..63]



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU DDR4 CHB

Pegatron Corp. Engineer: Ryan_Yen

Size A3 Project Name Orion_N18E

Date: Friday, December 14, 2018 Sheet 10 of 93

Caldera x 4

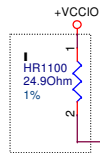
Alpine Ridge x 4

GPU x 8

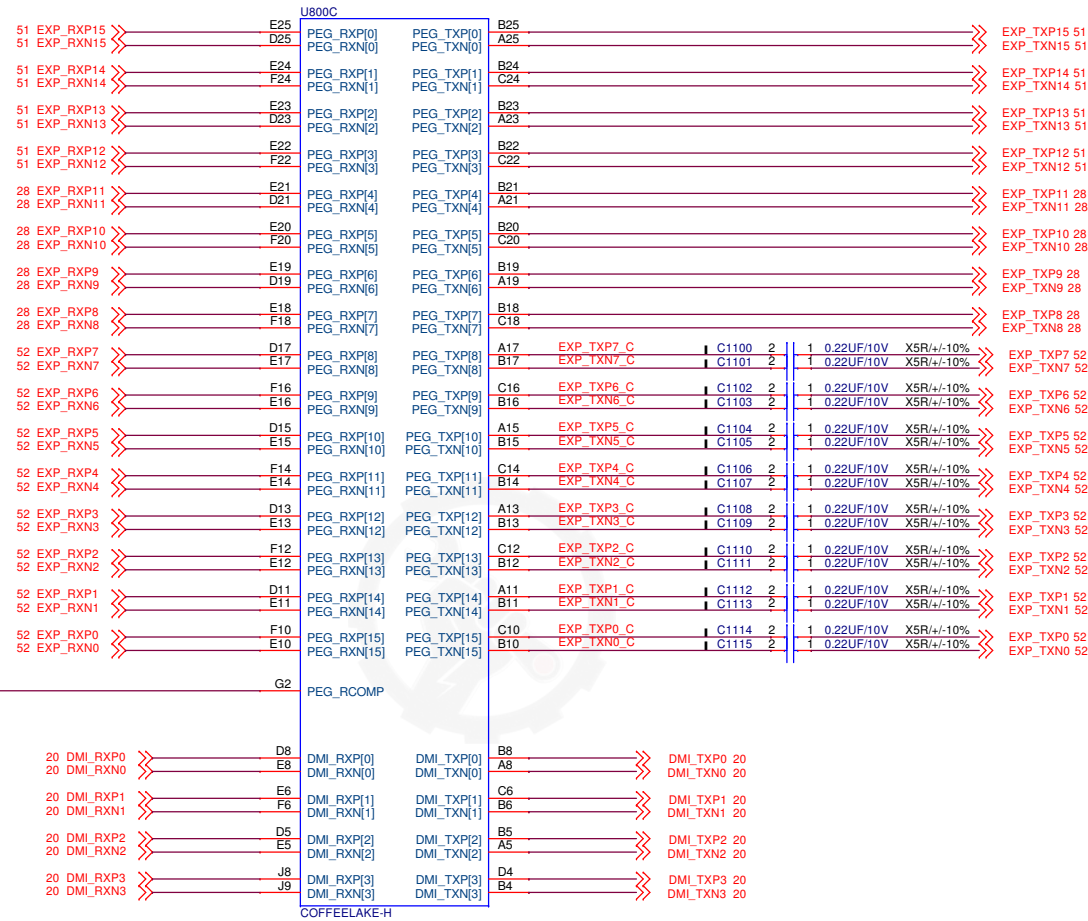
Caldera x 4

Alpine Ridge x 4

GPU x 8

**NOTE:**

W/S=12/15 mil, length<400mil



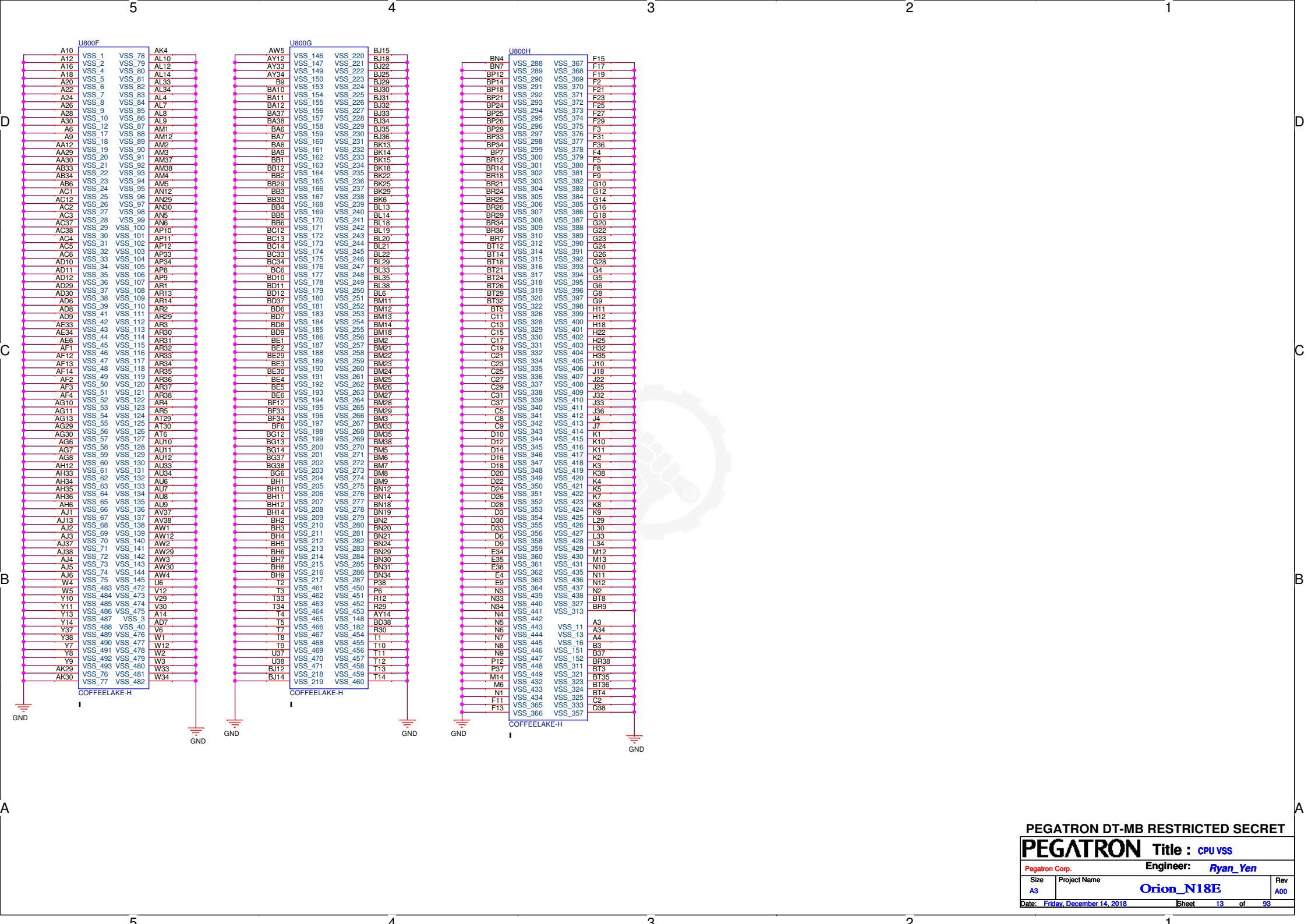
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU PCIE/DMI

Pegatron Corp. Engineer: **Ryan_Yen**

Size A3 Project Name **Orion_N18E** Rev A00

Date: Friday, December 14, 2018 Sheet 11 of 93



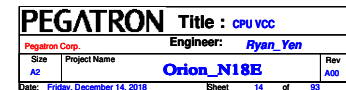
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU VSS

Pegatron Corp. Engineer: Ryan_Yen

Size A3	Project Name Orion_N18E	Rev A00
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Date: Friday, December 14, 2018 Sheet 13 of 93



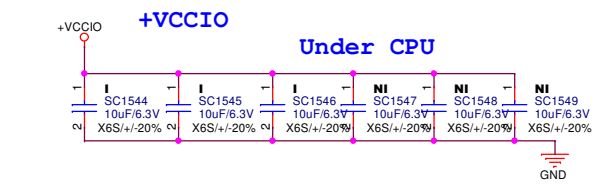
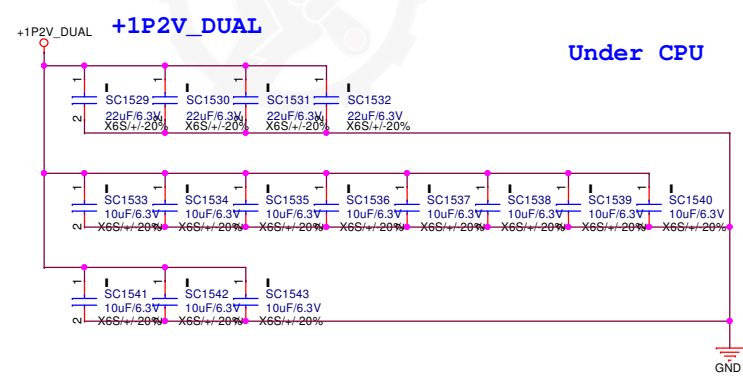
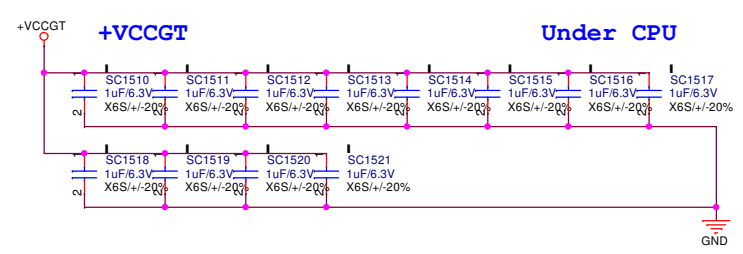
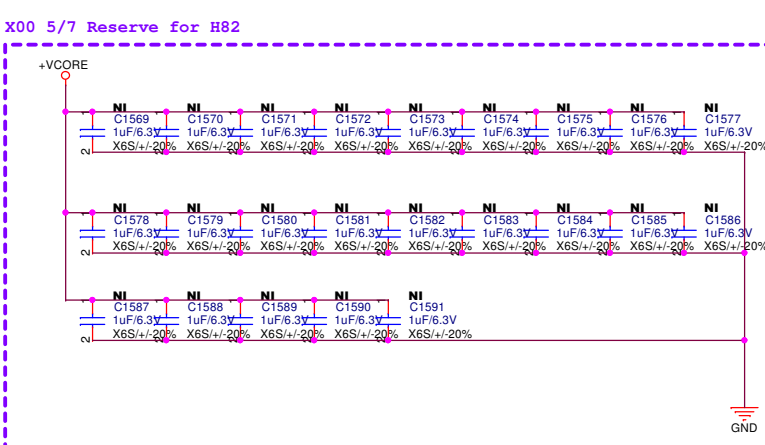
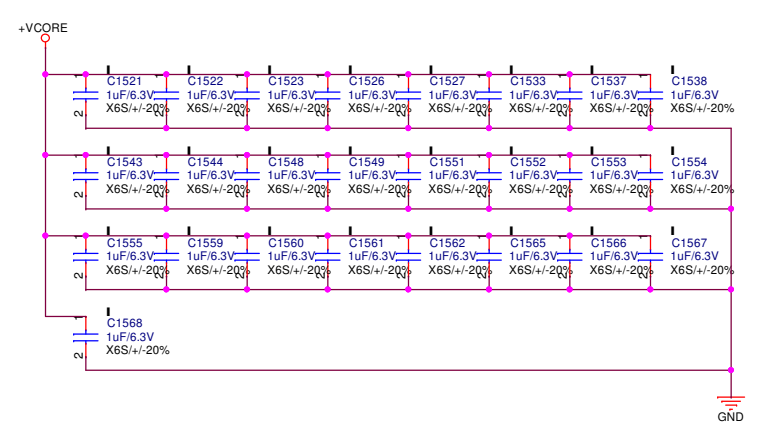
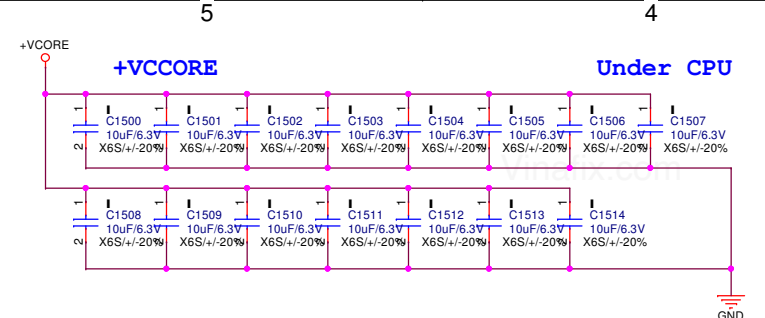
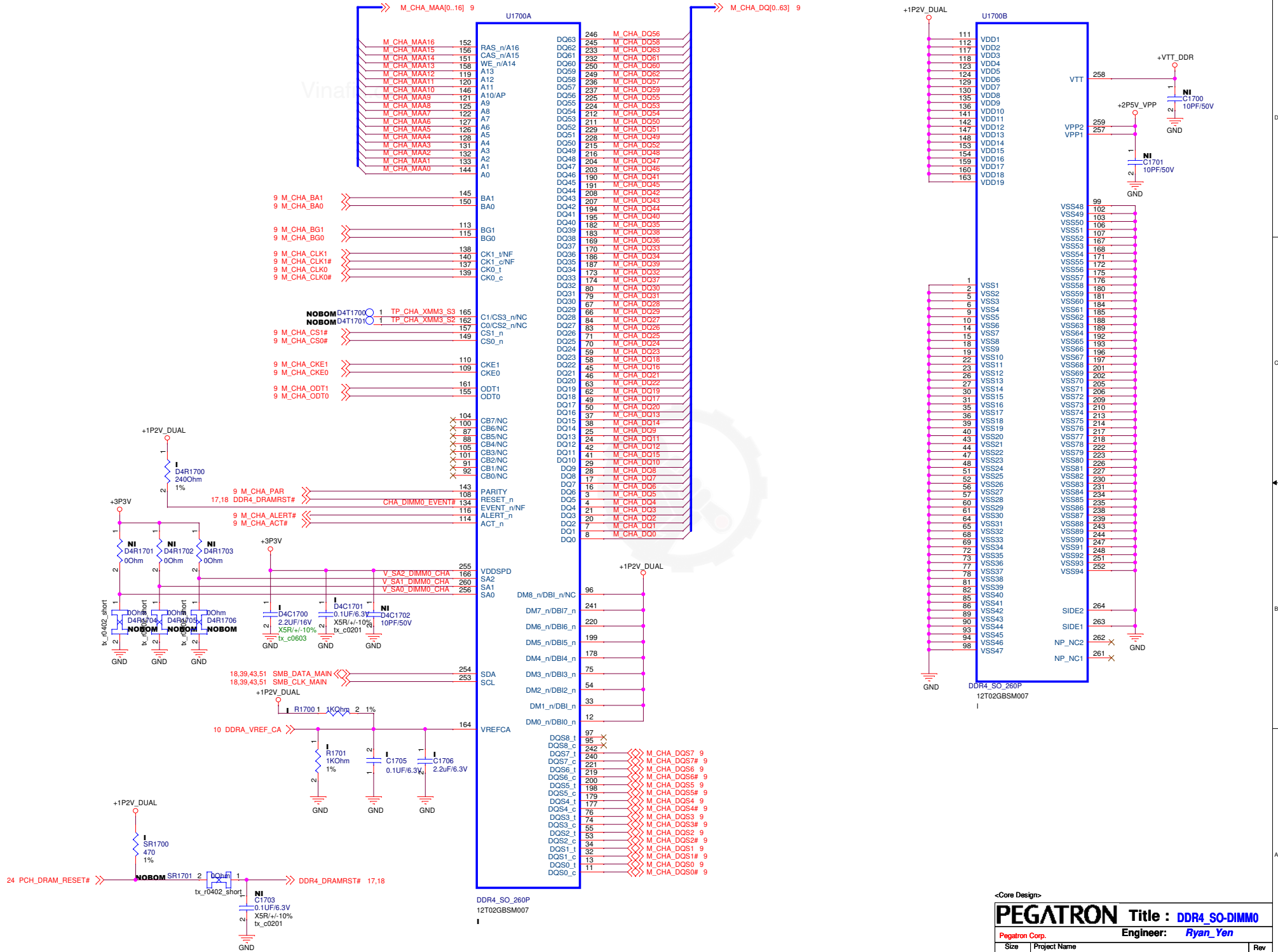
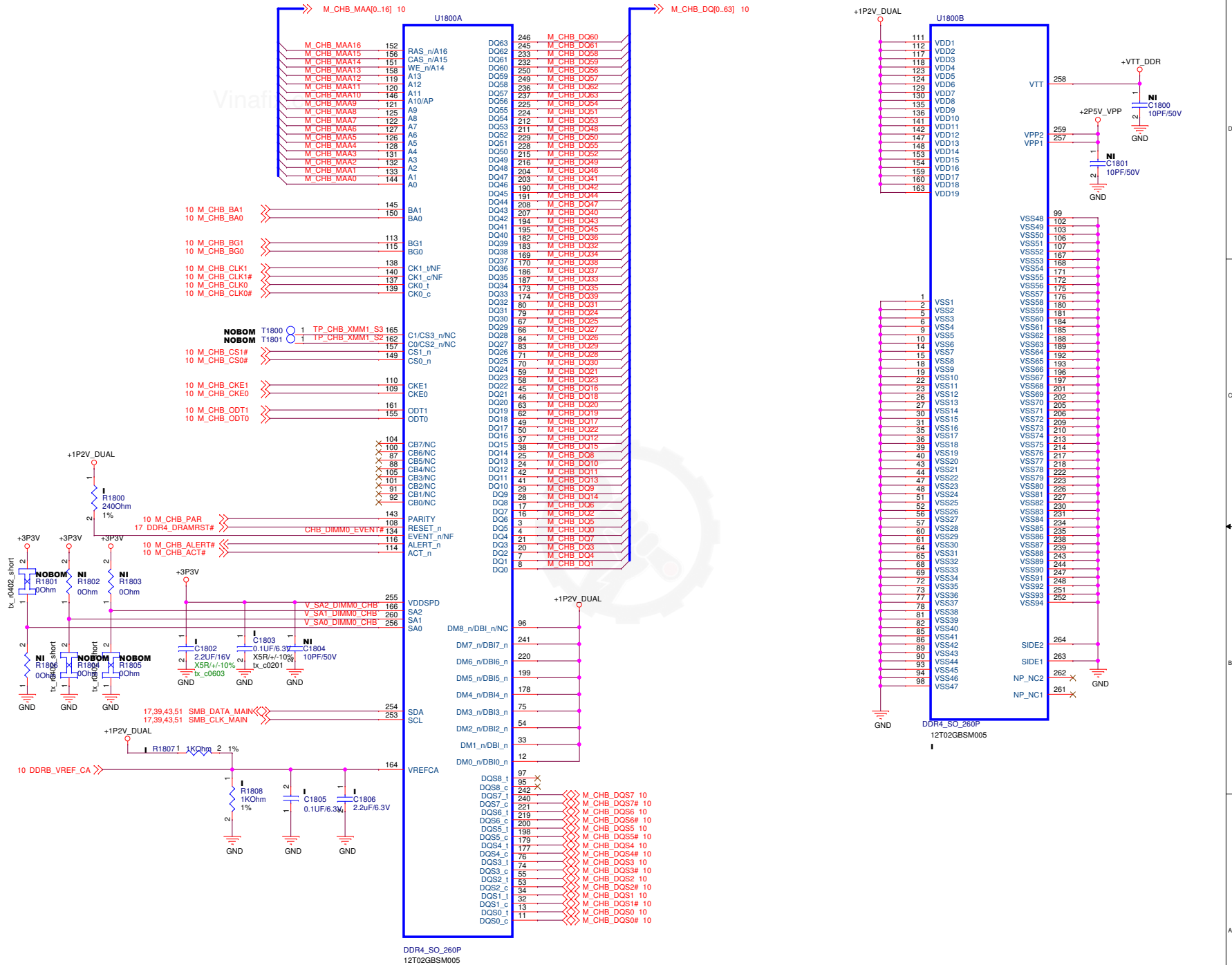


Table 50-3. Decoupling Requirements for CFL H Processor

Domain	Board Edge cap	Backside cap	Notes
Vcc	5x 47uF 0805		
		12x 22uF 0603	
		21x 10uF 0402	
		24x 1uF 0201	
VccGT	3x 47uF 0805 7x 22uF 0603		Place as close to the BGA as possible
		10x 10uF 0402	
		12x 1uF 0201	
VccSA	2x 47uF 0805 2x 22uF 0603		
		7x 10uF 0402	
		1x 1uF 0201	
VDDQ		4x 22uF 0603	
		11x 10uF 0402	
VCCIO		3x 10uF 0402	
		3x 0402 (placeholder)	Additional capacitors might be needed if the connectivity from BGAs to capacitors is not adequate.

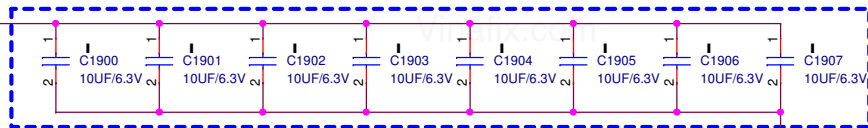




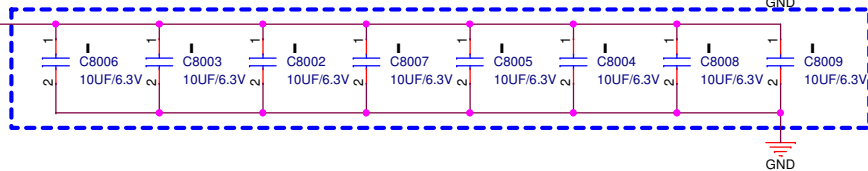
<Core Design>

PEGATRON		Title : <u>DDR4_SO-DIMM1</u>	
Pegatron Corp.		Engineer: <u>Ryan_Yen</u>	
Size <u>Custom</u>	Project Name <u>Orion_N18E</u>		Rev <u>A00</u>
Date: <u>Friday, December 14, 2018</u>		Sheet	<u>18</u> of <u>93</u>

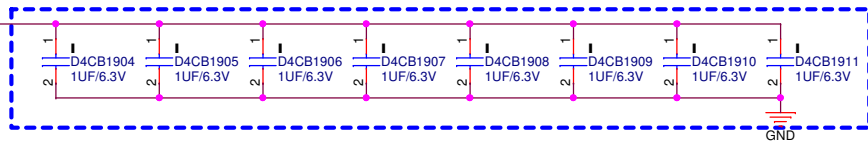
+1P2V_DUAL



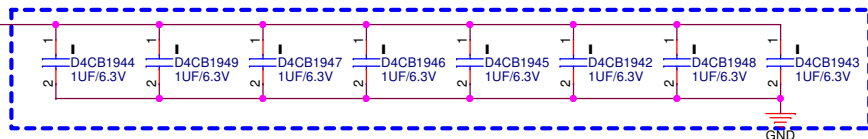
close
CH A SO-DIMM



close
CH B SO-DIMM



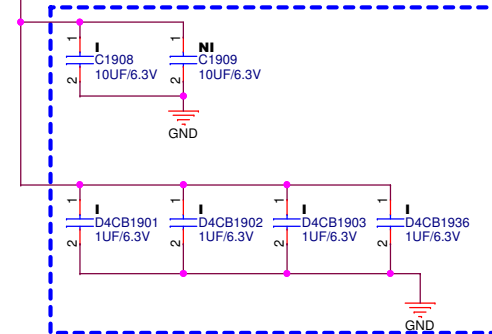
close
CH A SO-DIMM



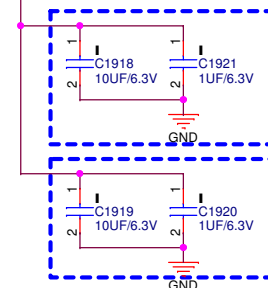
close
CH B SO-DIMM

+VTT_DDR

Near SO-DIMM



+2P5V_VPP



close CH A SO-DIMM

close CH B SO-DIMM

DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x μ F (size)	Note
DDR4 2 Channels SODIMM 1DPC	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10 μ F (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1 μ F (0402)	
		1 placeholder	1x 330 μ F (7343)	
	VTT	Place these caps on the VTT plane close to SODIMM	1x 10 μ F (0603)	
		Placeholder Place these caps on the VTT plane close to SODIMM	1x 10 μ F (0603)	
		Place these caps on the VTT plane close to SODIMM	4x 1 μ F (0402)	
	VPP	DRAM Side	2x 10 μ F (0603)	
		DRAM Side	2x 1 μ F (0402)	
	VDDSPD	Place close to DIMM	1x 0.1 μ F (0402)	
		Place close to DIMM	1x 2.2 μ F (0402)	

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : DDR4 DECOUPLING	
Pegatron Corp.		Engineer: Ryan_Yen	
Size Custom	Project Name Orion_N18E		Rev A00
Date: Friday, December 14, 2018		Sheet	19 of 93

CNL PCH-H Preliminary HSIO Lane Assignments

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
	USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8	
	USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8	
	USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8	
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	USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8	
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	USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8	
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	USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8	
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	USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8	
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	USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8	
	USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8	
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	USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8		PCIe 3.0 x8	
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	USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2		USB 3.1 Gen1 / Gen2 x2																					

SATA SSD4

SATA SSD3

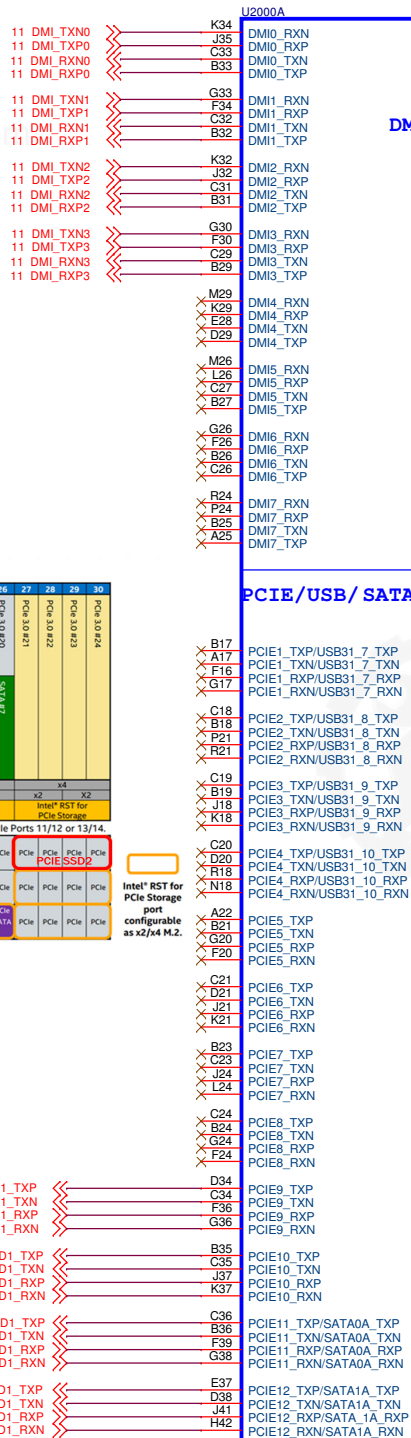
M.2 PCIE X4 #1

31 PCIE9_SSD1_TXP
31 PCIE9_SSD1_TXN
31 PCIE9_SSD1_RXP
31 PCIE9_SSD1_RXN

31 PCIE10_SSD1_TXP
31 PCIE10_SSD1_TXN
31 PCIE10_SSD1_RXP
31 PCIE10_SSD1_RXN

31 PCIE11_SSD1_TXP
31 PCIE11_SSD1_TXN
31 PCIE11_SSD1_RXP
31 PCIE11_SSD1_RXN

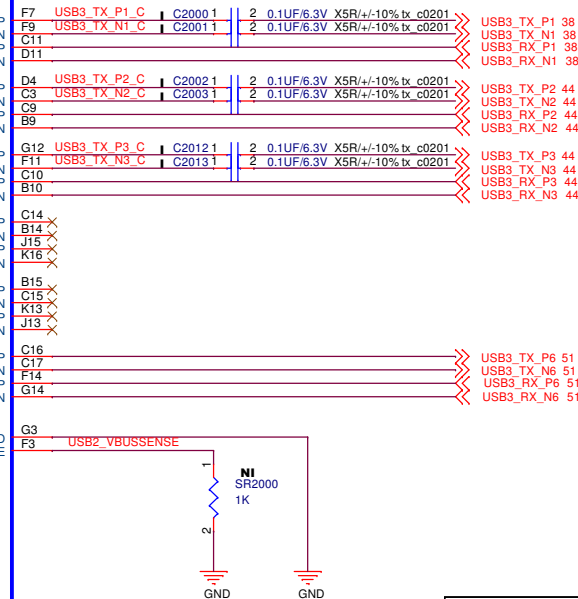
31 PCIE12_SATA1A_SSD1_TXP
31 PCIE12_SATA1A_SSD1_TXN
31 PCIE12_SATA1A_SSD1_RXP
31 PCIE12_SATA1A_SSD1_RXN



PCH-H

USB3.1

USB2_ID
USB2_VBUSSENSE

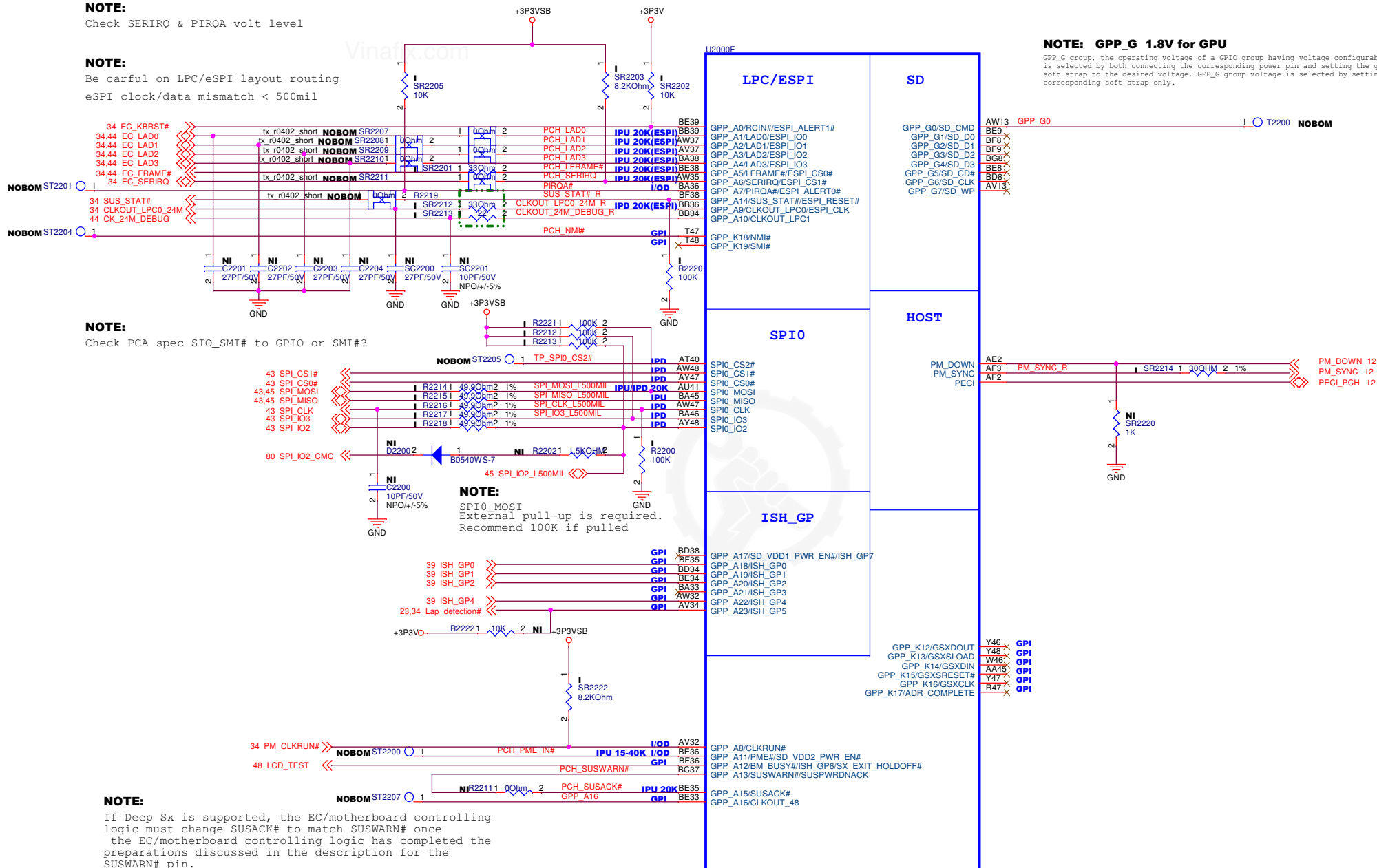


eSPI operates at 1.8V

Check SERIRQ & PIRQA volt level

Be careful on LPC/eSPI layout routing
eSPI clock/data mismatch < 500mil

Check GPP_A0 power well

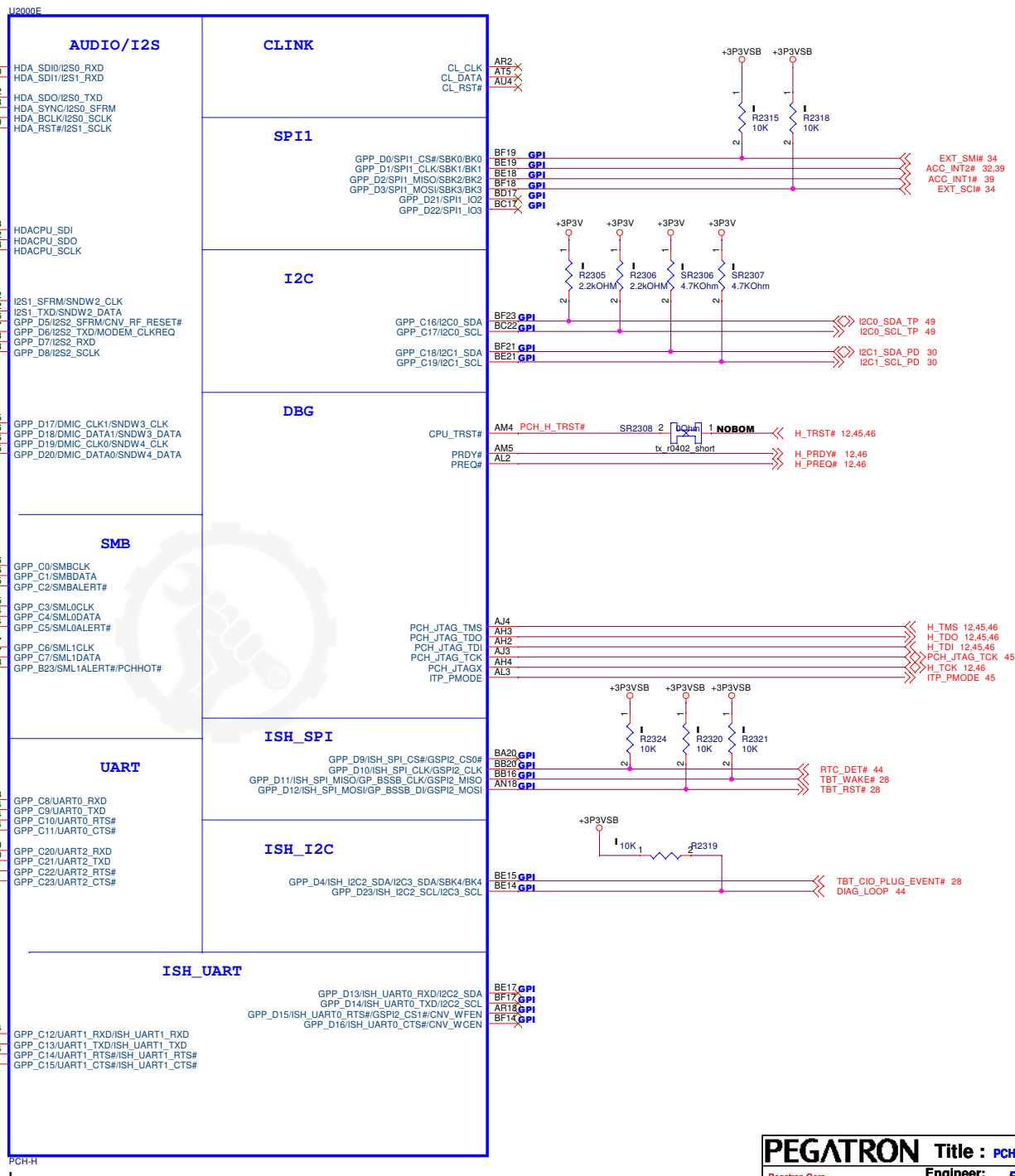
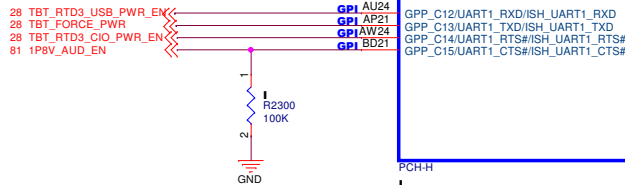


GPP_G group, the operating voltage of a GPIO group having voltage configurability (3.3V or 1.8V) is selected by both connecting the corresponding power pin and setting the group-voltage-selection soft strap to the desired voltage. GPP_G group voltage is selected by setting the corresponding soft strap only.

PEGATRON DT-MB RESTRICTED SECRET

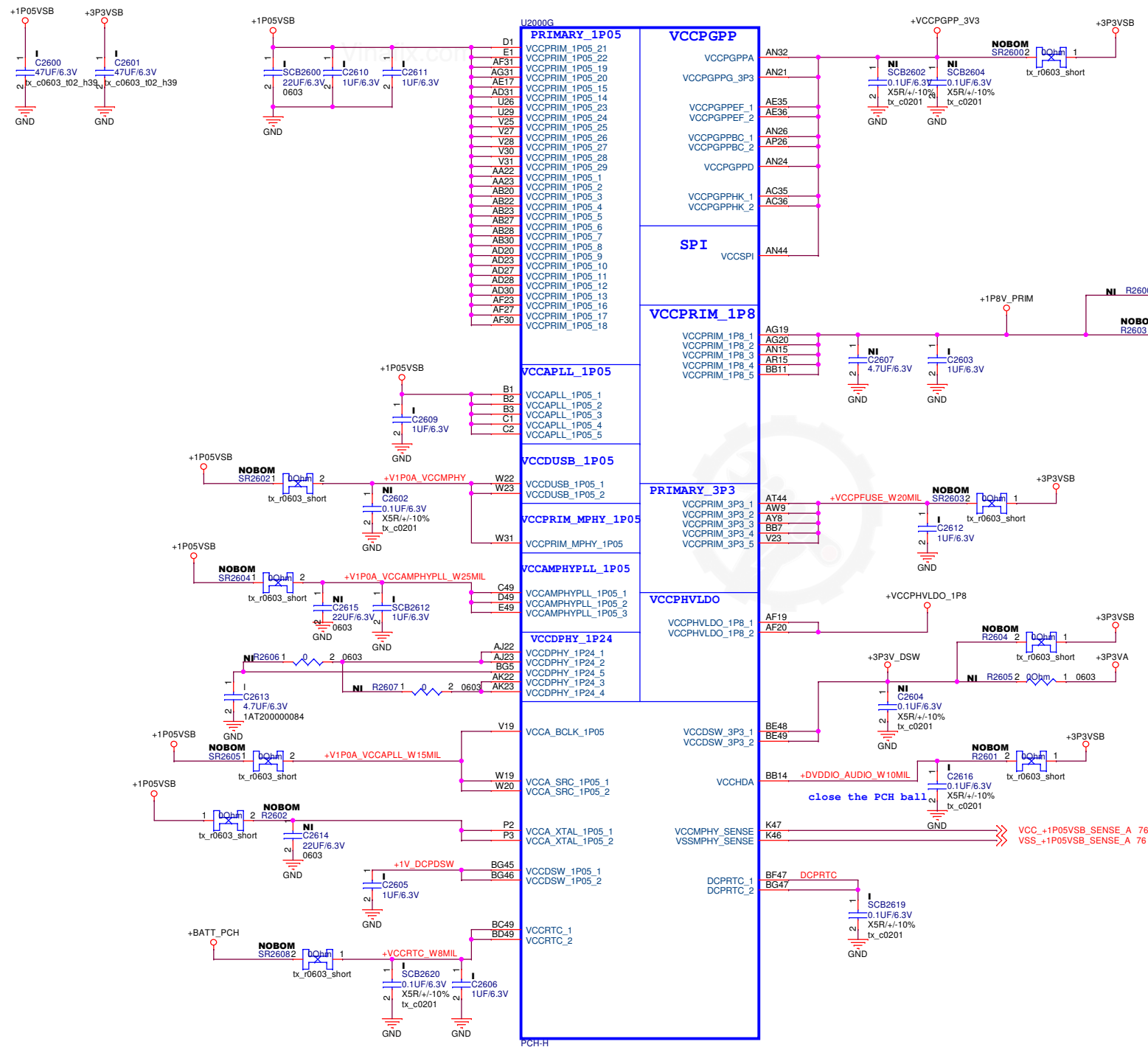
PEGATRON Title : PCH ESPI/SPI/FAN/HOST

Pegatron Corp.		Engineer: <i>Ryan_Yen</i>	
Size Custom	Project Name Orion_N18E	Rev A00	
Date: <u>Friday, December 14, 2018</u>		Sheet <u>22</u> of <u>93</u>	



```
0 = Disable "No Reboot" mode.
1 = Enable "No Reboot" mode
(PCH will disable the TCO Timer system reboot feature).
```

Date: Friday, December 14, 2018 Sheet 24 of 93



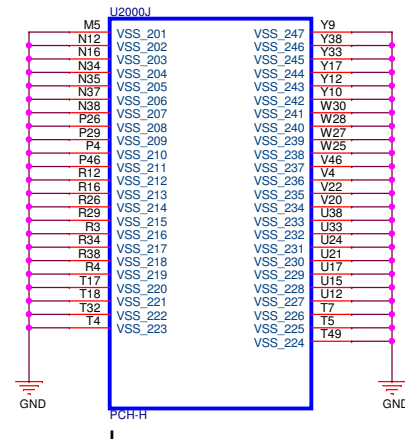
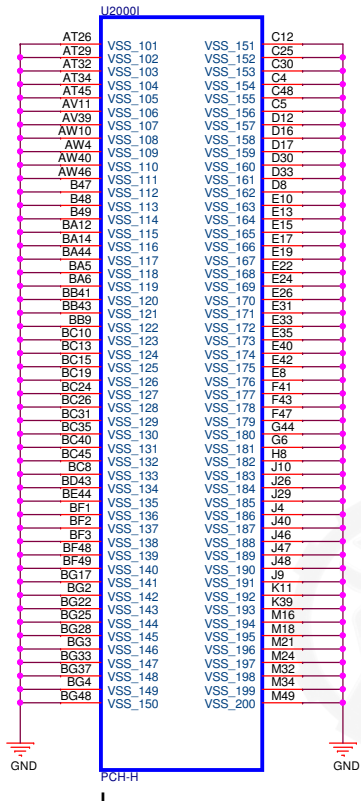
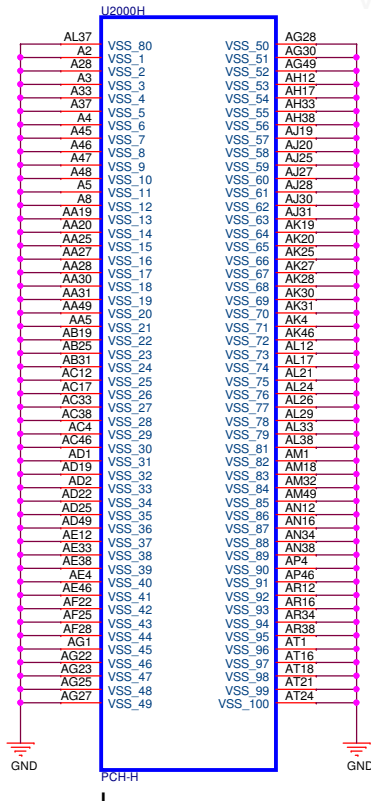
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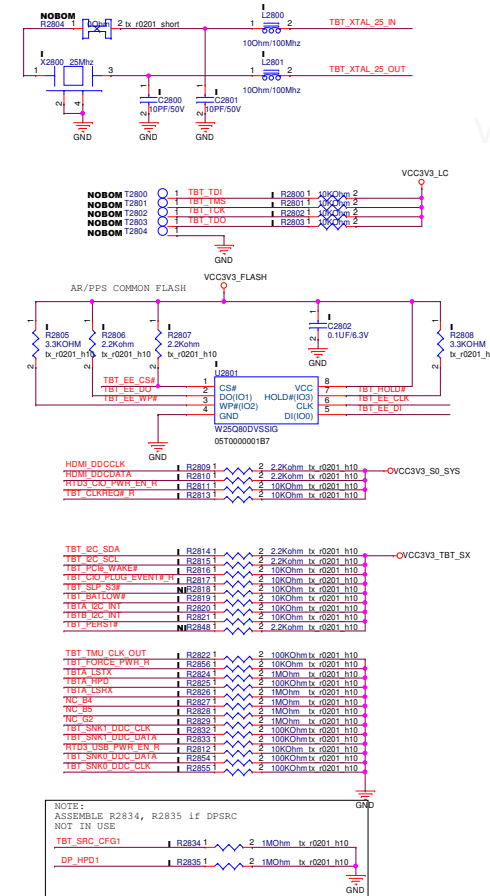
PEGATRON Title : PCH VCC/PLL

Pegatron Corp. Engineer: **Ryan_Yen**

Size A3 Project Name **Orion_N18E** Rev A00

Date: Friday, December 14, 2018 Sheet 26 of 93



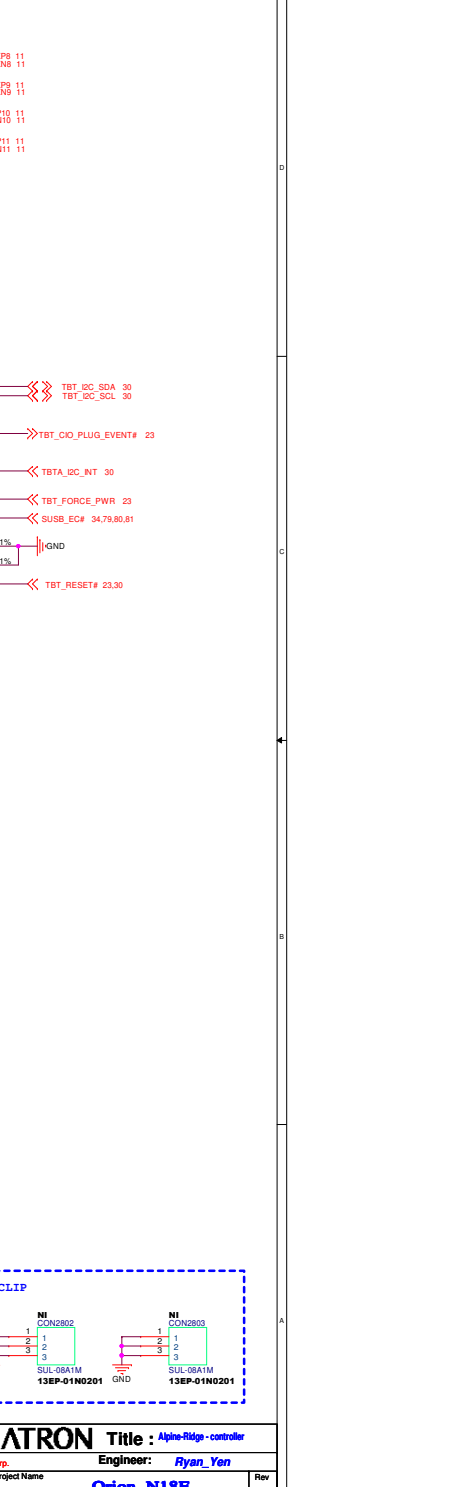
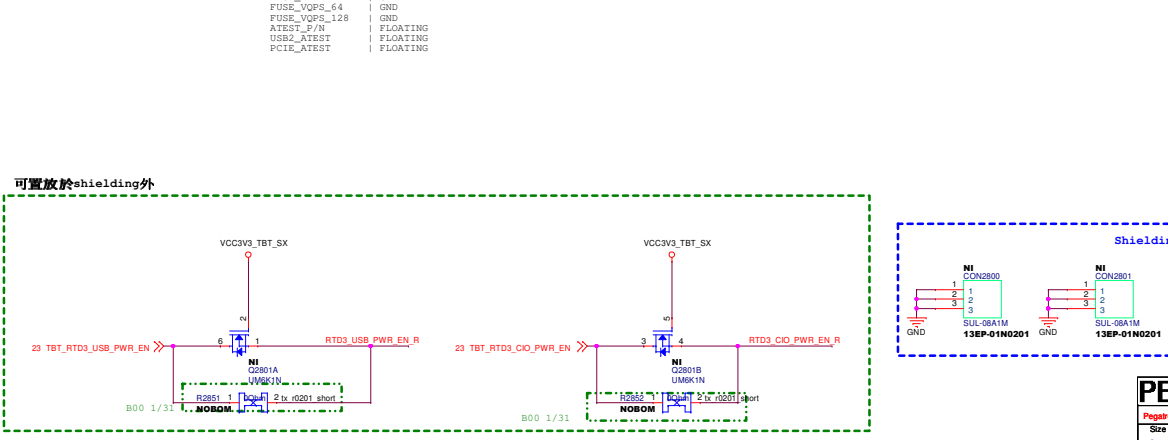
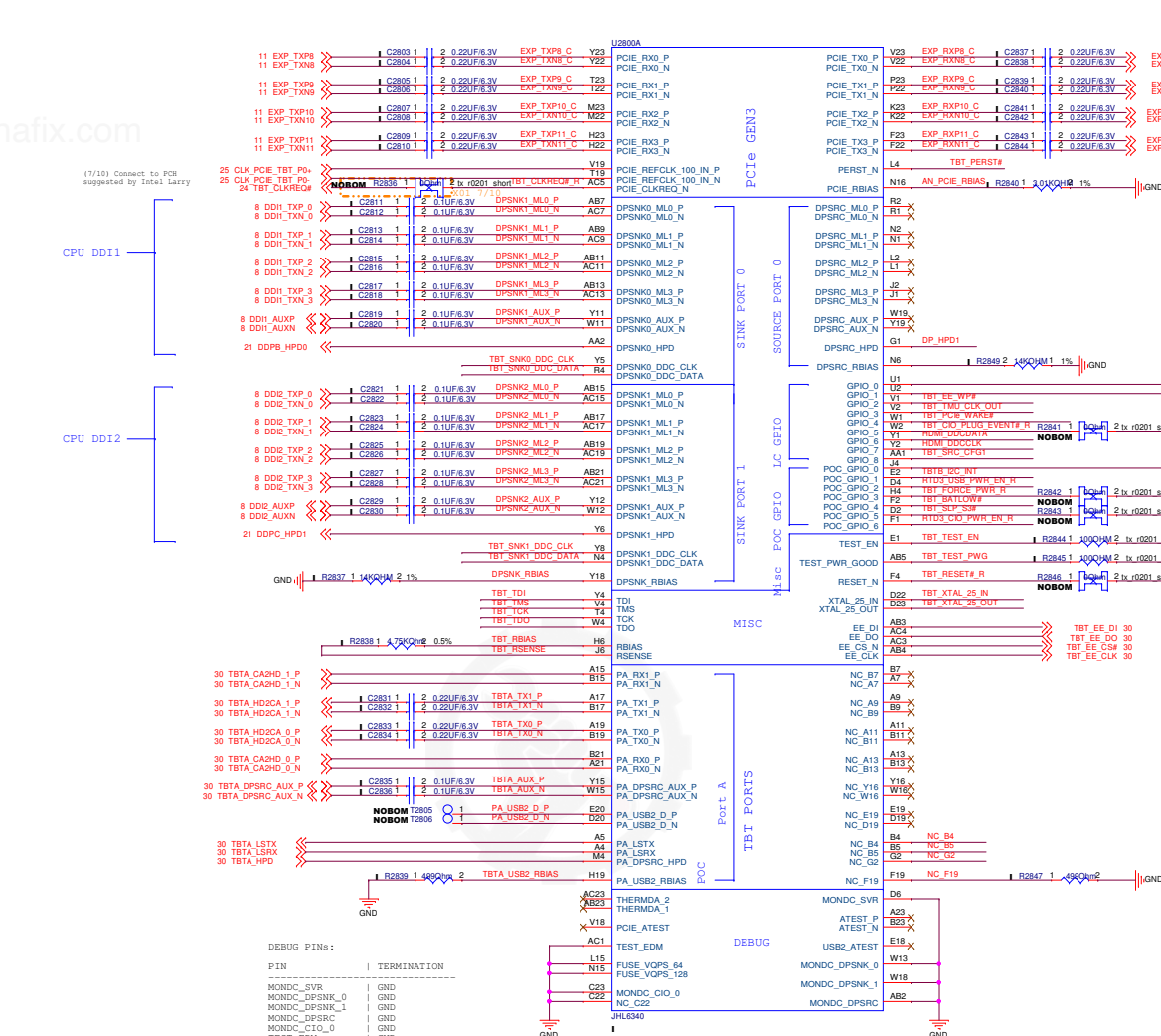
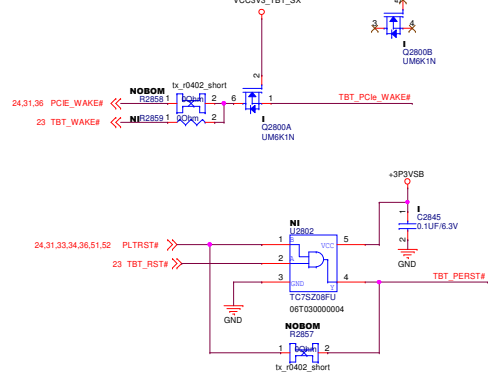


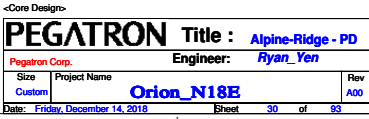
NOTE:
ASSEMBLE R2834, R2835 if DP SRC
NOT IN USE

TBT_SRC_CFG1
DP_HPD1

IF SOME OF GPIOs ARE NOT IN USE FOLLOW TABLE BELOW:

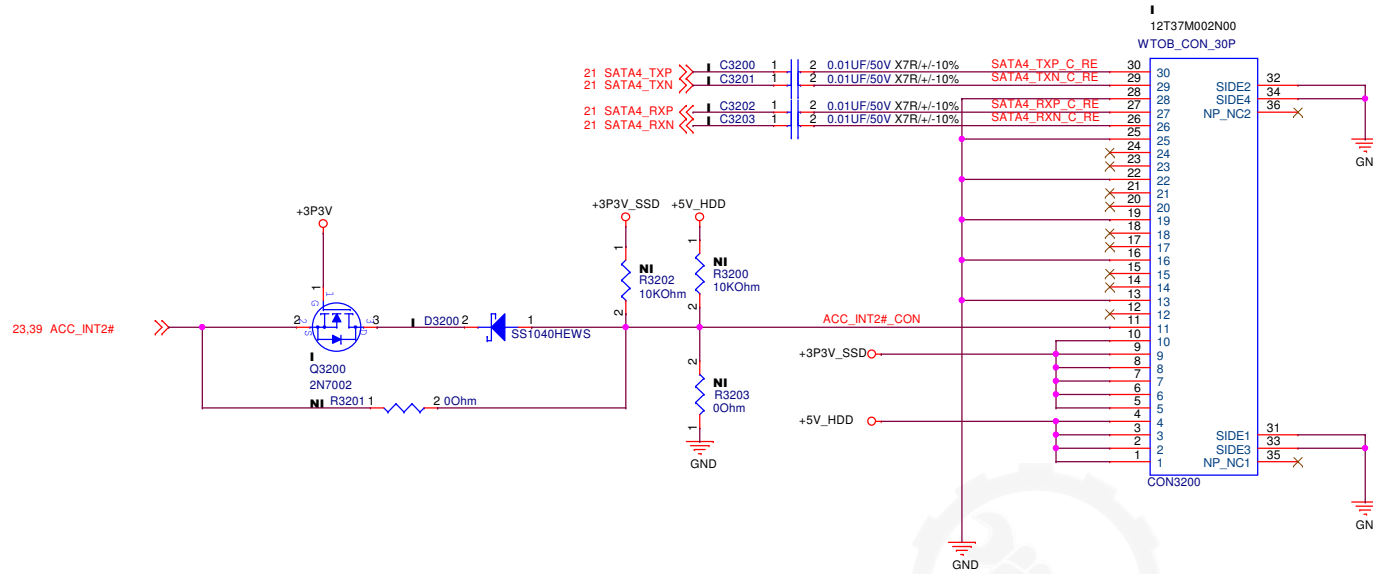
GPIO	TERMINATION	Power Rail
GPIO_0	10K PU	VCC3V3_LC
GPIO_1	10K PU	VCC3V3_LC
GPIO_2	100K PU	VCC3V3_LC
GPIO_3	100K PU	VCC3V3_LC
GPIO_4	10K PU	VCC3V3_LC
GPIO_5	100K PU	VCC3V3_LC
GPIO_6	100K PU	VCC3V3_LC
GPIO_7	100K PU	VCC3V3_LC
GPIO_8	100K PU	VCC3V3_LC
POC_GPIO_0	10K PU	VCC3V3_TBT_SX
POC_GPIO_1	10K PU	VCC3V3_TBT_SX
POC_GPIO_2	100K PU	VCC3V3_TBT_SX
POC_GPIO_3	100K PU	VCC3V3_TBT_SX
POC_GPIO_4	10K PU	VCC3V3_TBT_SX
POC_GPIO_5	100K PU	VCC3V3_TBT_SX
POC_GPIO_6	100K PU	VCC3V3_TBT_SX





The schematic diagram illustrates the electrical connections for the T2144BSM022 board. Key components and connections include:

- Power Supply Sections:** Multiple +3P3V_SSD and +3P3V_SSD sections are shown, each with decoupling capacitors (C3105, C3106, C3107, C3108, C3110, C3111, C3112, C3115, C3116, C3117, C3118) and resistors (R3102, R3104, R3106, R3107, R3108, R3109, R3110, R3111, R3112, R3113, R3114, R3115, R3116, R3117, R3118, R3119, R3120, R3121, R3122, R3123, R3124, R3125, R3126, R3127, R3128, R3129, R3130, R3131, R3132, R3133, R3134, R3135, R3136, R3137, R3138, R3139, R3140, R3141, R3142, R3143, R3144, R3145, R3146, R3147, R3148, R3149, R3150, R3151, R3152, R3153, R3154, R3155, R3156, R3157, R3158, R3159, R3160, R3161, R3162, R3163, R3164, R3165, R3166, R3167, R3168, R3169, R3170, R3171, R3172, R3173, R3174, R3175, R3176, R3177, R3178, R3179, R3180, R3181, R3182, R3183, R3184, R3185, R3186, R3187, R3188, R3189, R3190, R3191, R3192, R3193, R3194, R3195, R3196, R3197, R3198, R3199, R3200, R3201, R3202, R3203, R3204, R3205, R3206, R3207, R3208, R3209, R3210, R3211, R3212, R3213, R3214, R3215, R3216, R3217, R3218, R3219, R3220, R3221, R3222, R3223, R3224, R3225, R3226, R3227, R3228, R3229, R3230, R3231, R3232, R3233, R3234, R3235, R3236, R3237, R3238, R3239, R3240, R3241, R3242, R3243, R3244, R3245, R3246, R3247, R3248, R3249, R3250, R3251, R3252, R3253, R3254, R3255, R3256, R3257, R3258, R3259, R3260, R3261, R3262, R3263, R3264, R3265, R3266, R3267, R3268, R3269, R3270, R3271, R3272, R3273, R3274, R3275, R3276, R3277, R3278, R3279, R3280, R3281, R3282, R3283, R3284, R3285, R3286, R3287, R3288, R3289, R3290, R3291, R3292, R3293, R3294, R3295, R3296, R3297, R3298, R3299, R3300, R3301, R3302, R3303, R3304, R3305, R3306, R3307, R3308, R3309, R3310, R3311, R3312, R3313, R3314, R3315, R3316, R3317, R3318, R3319, R3320, R3321, R3322, R3323, R3324, R3325, R3326, R3327, R3328, R3329, R3330, R3331, R3332, R3333, R3334, R3335, R3336, R3337, R3338, R3339, R3340, R3341, R3342, R3343, R3344, R3345, R3346, R3347, R3348, R3349, R3350, R3351, R3352, R3353, R3354, R3355, R3356, R3357, R3358, R3359, R3360, R3361, R3362, R3363, R3364, R3365, R3366, R3367, R3368, R3369, R3370, R3371, R3372, R3373, R3374, R3375, R3376, R3377, R3378, R3379, R3380, R3381, R3382, R3383, R3384, R3385, R3386, R3387, R3388, R3389, R3390, R3391, R3392, R3393, R3394, R3395, R3396, R3397, R3398, R3399, R3400, R3401, R3402, R3403, R3404, R3405, R3406, R3407, R3408, R3409, R3410, R3411, R3412, R3413, R3414, R3415, R3416, R3417, R3418, R3419, R3420, R3421, R3422, R3423, R3424, R3425, R3426, R3427, R3428, R3429, R3430, R3431, R3432, R3433, R3434, R3435, R3436, R3437, R3438, R3439, R3440, R3441, R3442, R3443, R3444, R3445, R3446, R3447, R3448, R3449, R3450, R3451, R3452, R3453, R3454, R3455, R3456, R3457, R3458, R3459, R3460, R3461, R3462, R3463, R3464, R3465, R3466, R3467, R3468, R3469, R3470, R3471, R3472, R3473, R3474, R3475, R3476, R3477, R3478, R3479, R3480, R3481, R3482, R3483, R3484, R3485, R3486, R3487, R3488, R3489, R3490, R3491, R3492, R3493, R3494, R3495, R3496, R3497, R3498, R3499, R3500, R3501, R3502, R3503, R3504, R3505, R3506, R3507, R3508, R3509, R3510, R3511, R3512, R3513, R3514, R3515, R3516, R3517, R3518, R3519, R3520, R3521, R3522, R3523, R3524, R3525, R3526, R3527, R3528, R3529, R3530, R3531, R3532, R3533, R3534, R3535, R3536, R3537, R3538, R3539, R3540, R3541, R3542, R3543, R3544, R3545, R3546, R3547, R3548, R3549, R3550, R3551, R3552, R3553, R3554, R3555, R3556, R3557, R3558, R3559, R3560, R3561, R3562, R3563, R3564, R3565, R3566, R3567, R3568, R3569, R3570, R3571, R3572, R3573, R3574, R3575, R3576, R3577, R3578, R3579, R3580, R3581, R3582, R3583, R3584, R3585, R3586, R3587, R3588, R3589, R3590, R3591, R3592, R3593, R3594, R3595, R3596, R3597, R3598, R3599, R3600, R3601, R3602, R3603, R3604, R3605, R3606, R3607, R3608, R3609, R3610, R3611, R3612, R3613, R3614, R3615, R3616, R3617, R3618, R3619, R3620, R3621, R3622, R3623, R3624, R3625, R3626, R3627, R3628, R3629, R3630, R3631, R3632, R3633, R3634, R3635, R3636, R3637, R3638, R3639, R3640, R3641, R3642, R3643, R3644, R3645, R3646, R3647, R3648, R3649, R3650, R3651, R3652, R3653, R3654, R3655, R3656, R3657, R3658, R3659, R3660, R3661, R3662, R3663, R3664, R3665, R3666, R3667, R3668, R3669, R3670, R3671, R3672, R3673, R3674, R3675, R3676, R3677, R3678, R3679, R3680, R3681, R3682, R3683, R3684, R3685, R3686, R3687, R3688, R3689, R3690, R3691, R3692, R3693, R3694, R3695, R3696, R3697, R3698, R3699, R3700, R3701, R3702, R3703, R3704, R3705, R3706, R3707, R3708, R3709, R3710, R3711, R3712, R3713, R3714, R3715, R3716, R3717, R3718, R3719, R3720, R3721, R3722, R3723, R3724, R3725, R3726, R3727, R3728, R3729, R3730, R3731, R3732, R3733, R3734, R3735, R3736, R3737, R3738, R3739, R3740, R3741, R3742, R3743, R3744, R3745, R3746, R37

SATA CONN

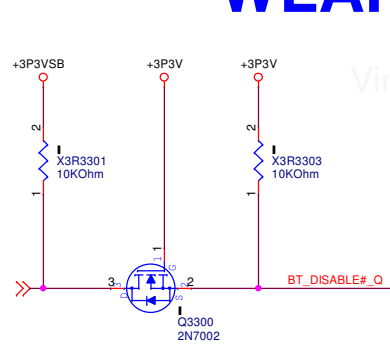
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PEGATRON Title : SATA HDD

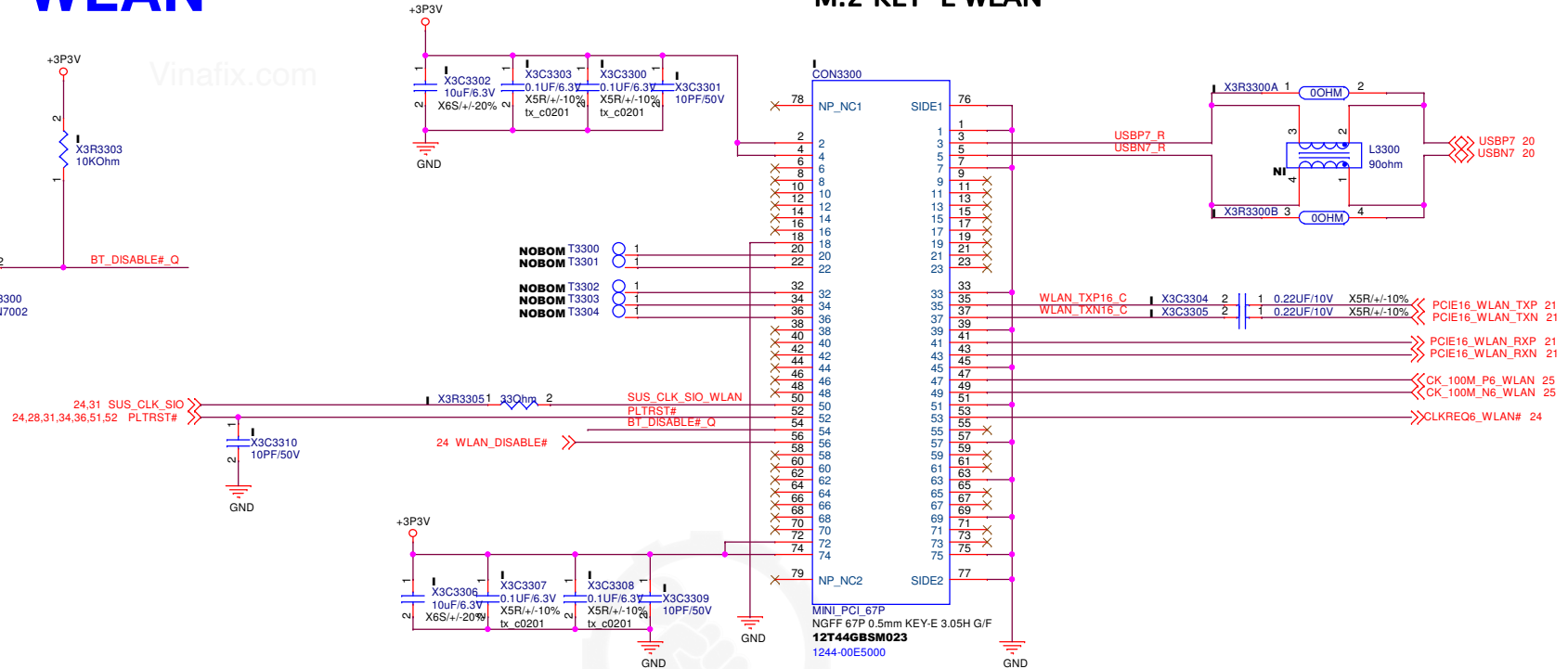
Pegatron Corp.		Engineer: <i>Ryan_Yen</i>	
Size A3	Project Name Orion_N18E	Rev A00	
Date: <i>Friday, December 14, 2018</i>		Sheet	<i>32</i> of <i>93</i>

WLAN

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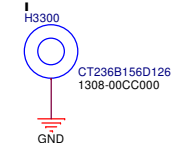
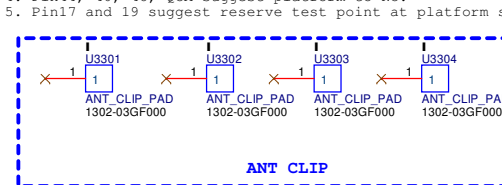
M.2 KEY-E WLAN



59	PERp1	NC	60	I2C_CLK[I]	NC
57	GND	YES	58	I2C_DATA[IO]	NC
55	PCIE_WAKE_L	YES	56	WLAN_DISABLE_L	YES
53	PCIE_CLKREQ_L	YES	54	BT_DISABLE_L	YES
51	GND	YES	52	PCIE_RST_L	YES
49	REFCLKN0	YES	50	SUSCLK(32kHz)	NC(Reverse resister)
47	REFCLKP0	YES	48	LTE_SYNC	YES
45	GND	YES	46	LTE_PRI	YES
43	PETn0	YES	44	LTE_ACTIVE	YES
41	PETp0	YES	42	RSVD	NC
39	GND	YES	40	RSVD	NC
37	PERn0	PCIE_TX_P	38	RSVD	NC
35	PERp0	PCIE_TX_N	36	UART_CTS	YES
33	GND	YES	34	UART_RTS	YES
31	NC	NC	32	UART_RXD	YES
29	NC	NC	30	NC	NC
27	NC	NC	28	NC	NC
25	NC	NC	26	NC	NC
23	NC	NC	24	NC	NC
21	NC	NC	22	UART_TXD	YES
19	DBG_UART_RXD	YES	20	UART_WAKEHOST_L	YES
17	DBG_UART_TXD	YES	18	GND	YES
15	NC	NC	16	LED_BT	YES
13	NC	NC	14	NC	NC
11	NC	NC	12	NC	NC
9	NC	NC	10	NC	NC
7	GND	YES	8	NC	NC
5	USB_D_N	YES	6	LED_WLAN	YES
3	USB_D_P	YES	4	3.3V	YES
1	GND	YES	2	3.3V	YES

Pin #	Name	DUT Connection	Pin #	Name	DUT Connection
75	GND	YES			
73	REFCLKN1	NC	74	3_3V	YES
71	REFCLKP1	NC	72	3_3V	YES
69	GND	YES	70	PEWAKE1	NC
67	PETn1	NC	68	CLKREQ1	NC
65	PETp1	NC	66	PERST1	NC
63	GND	YES	64	RSVD	NC(Reverse resister)
61	PERn1	NC	62	ALERT[0]	NC

- Remark: 1.NC is not connected; YES is connected.
 2. Pin54 is BT_DISABLE_L; Pin56 is WLAN_DISABLE_L.
 3. Pin 20,22,32,34 and 36 are GPIO and have internal pull up(QCA6174A?5), Suggest platform NC those pins.
 4. Pin44, 46, 48, QCA suggest platform to NC.
 5. Pin17 and 19 suggest reserve test point at platform side.



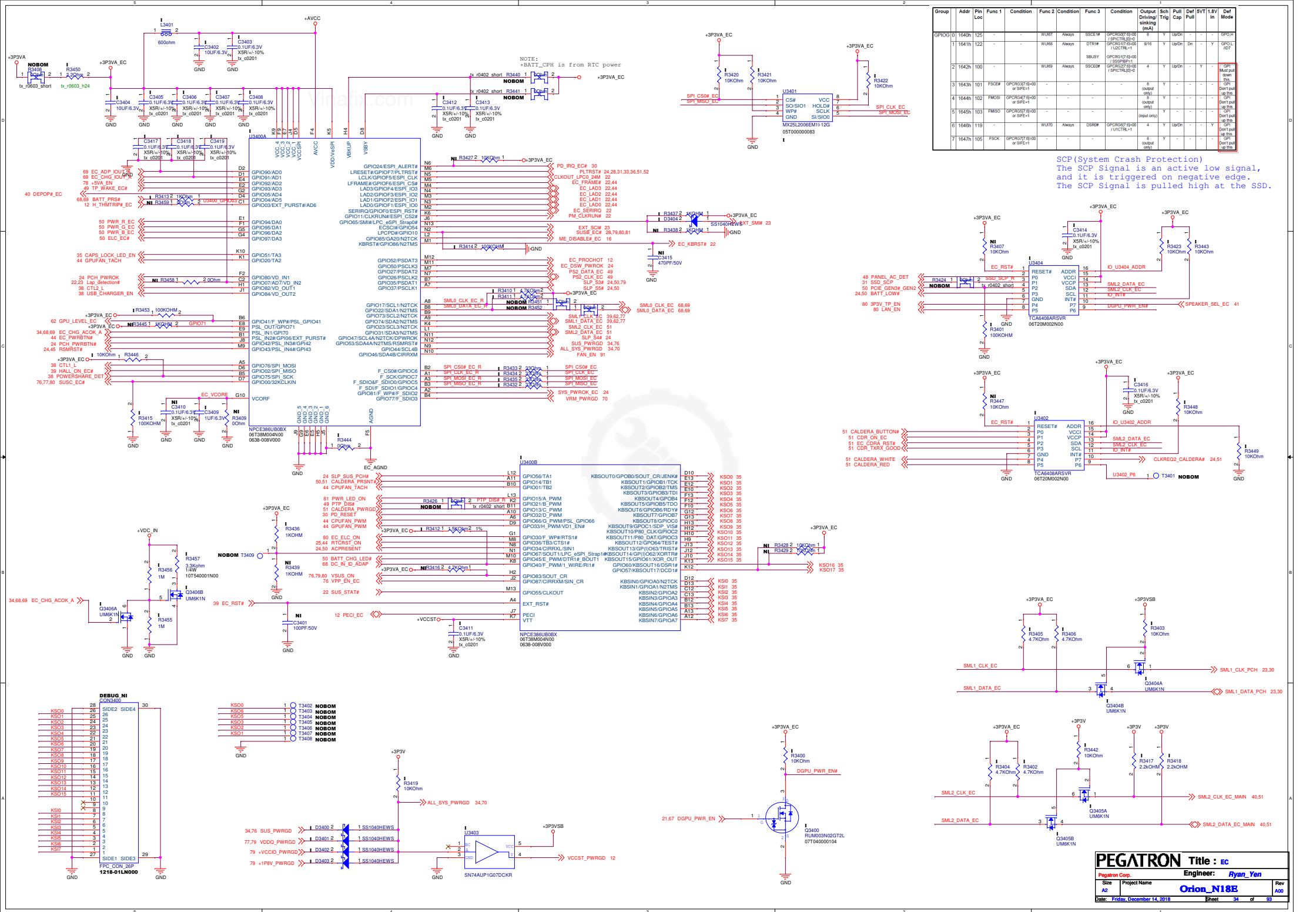
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : M.2 KEY-A 2230 WLAN

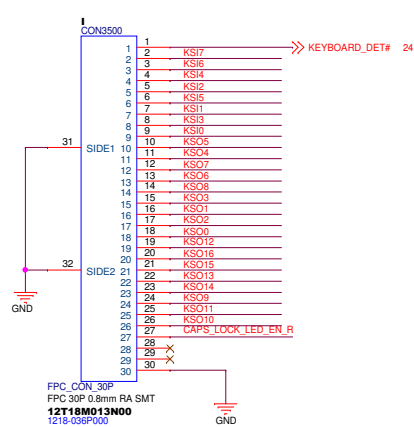
Pegatron Corp. Engineer: Ryan_Yen

Size A3 Project Name Orion_N18E Rev A00

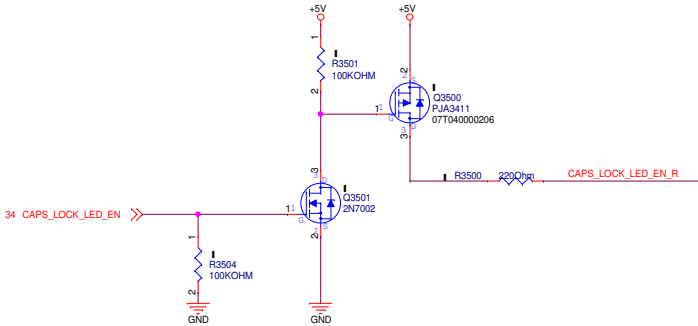
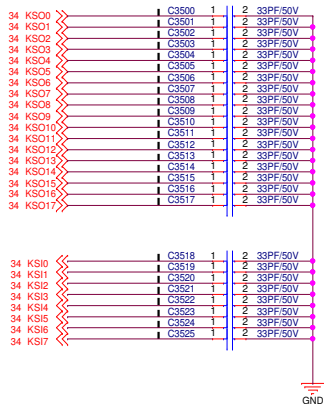
Date: Friday, December 14, 2018 Sheet 33 of 93



KeyBoard connector



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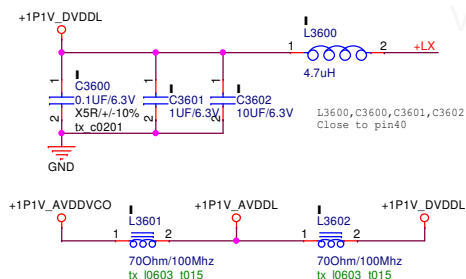
PEGATRON Title : KB & NKRO

Engineer: Ryan_Yen

Size Project Name Rev

Custom Orion_N18E A00

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**If AVDDL/DVDDL comes from internal SWR: mount L3602;
If AVDDL/DVDDL comes from internal LDO: no mount L3602, L3600, C3600, C3601, C3602

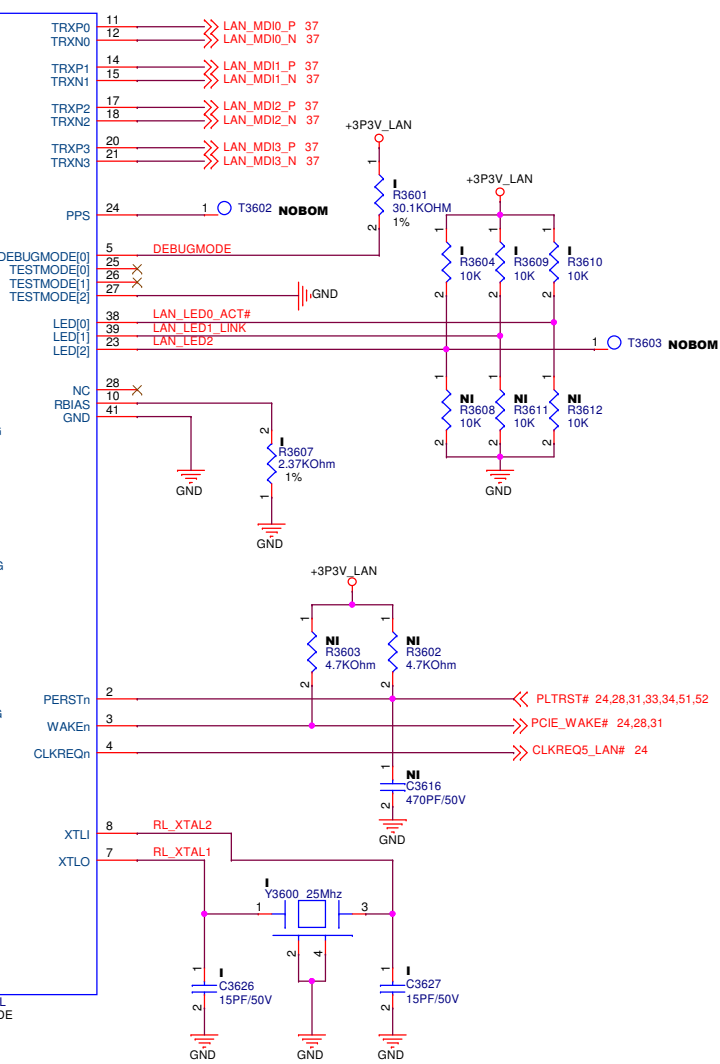
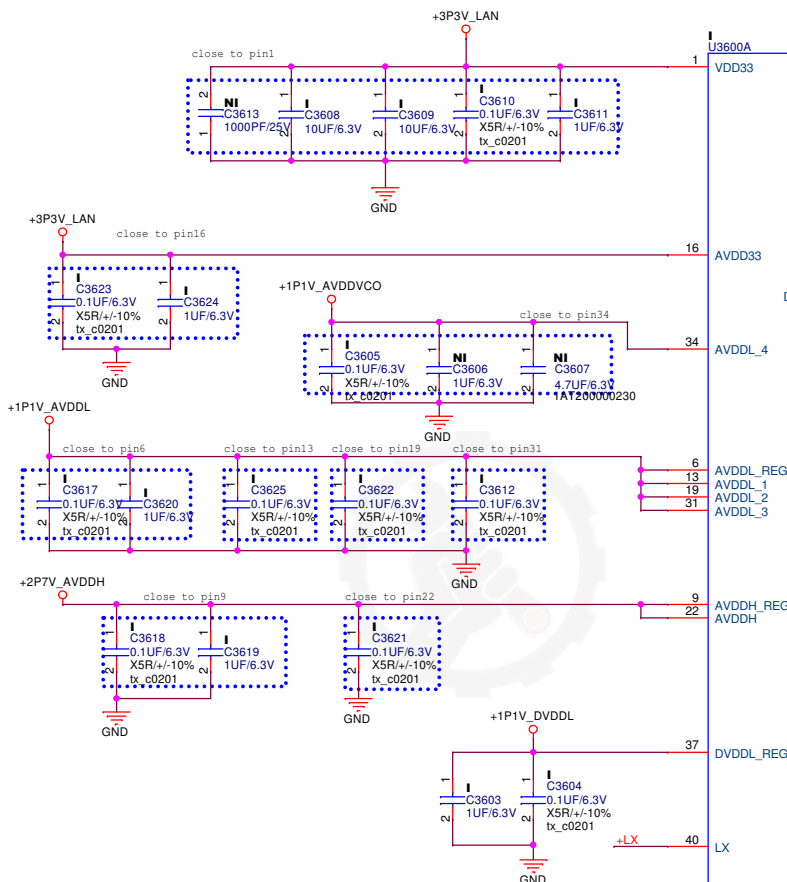
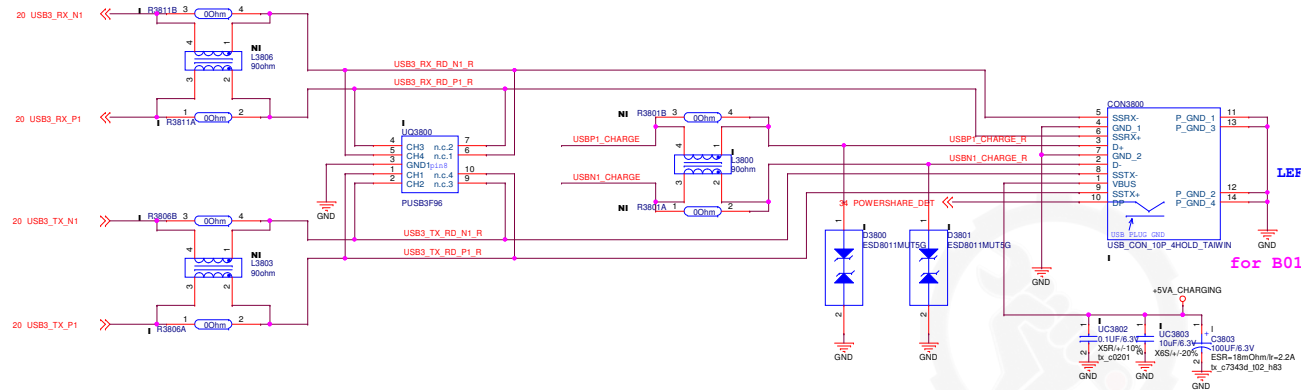


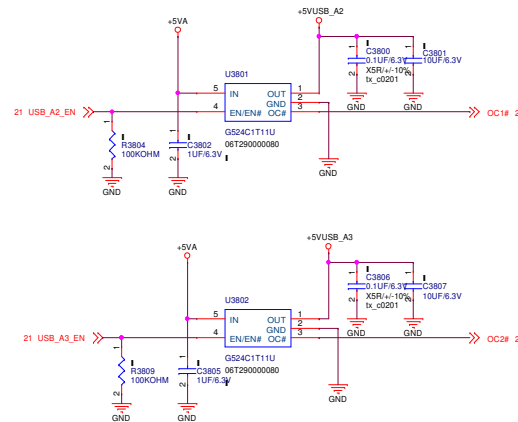
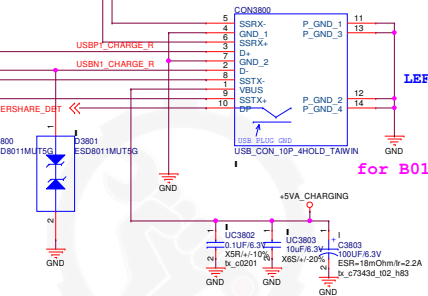
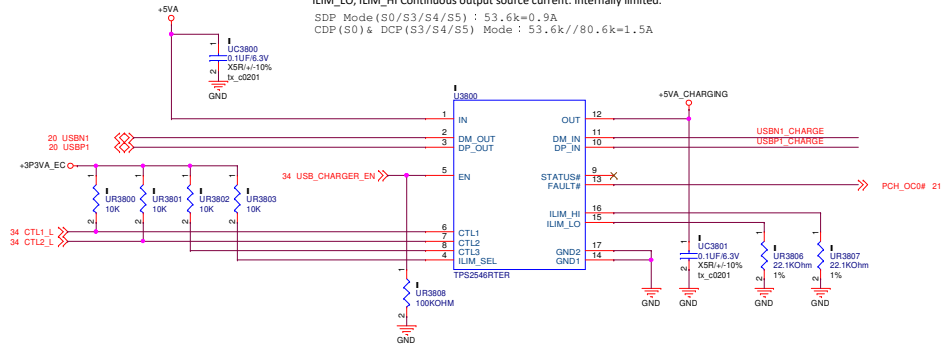
Table 2. Truth Table

CTL1	CTL2	CTL3	ILIM_SEL	MODE	CURRENT LIMIT SETTING	STATUS OUTPUT (Active low)	COMMENT
0	0	0	0	Discharge	NA	OFF	OUT held low
0	0	0	1	Discharge	NA	OFF	
0	0	1	0	DCP_Auto	ILIM_HI	OFF	Data Lines Disconnected
0	0	1	1	DCP_Auto	I _{DS_PV} & ILIM_HI ⁽¹⁾	DCP load present ⁽²⁾	Data Lines Disconnected and Load Detect Function Active
0	1	0	0	SDP1	ILIM_LO	OFF	Data Lines connected
0	1	0	1	SDP1	ILIM_HI	OFF	
0	1	1	0	DCP_Auto	ILIM_HI	OFF	Data Lines Disconnected
0	1	1	1	DCP_Auto	ILIM_HI	DCP load present ⁽³⁾	Data Lines Disconnected and Load Detect Function Active
1	0	0	0	DCP_Shorted	ILIM_LO	OFF	Device Forced to stay in DCP BC1.2 charging mode
1	0	0	1	DCP_Shorted	ILIM_HI	OFF	
1	0	1	0	DCP / Divider1	ILIM_LO	OFF	Device Forced to stay in DCP Divider1 Charging Mode
1	0	1	1	DCP / Divider1	ILIM_HI	OFF	
1	1	0	0	SDP1	ILIM_LO	OFF	
1	1	0	1	SDP1	ILIM_HI	OFF	Data Lines Connected
1	1	1	0	SDP2 ⁽⁴⁾	ILIM_LO	OFF	
1	1	1	1	CDP ⁽⁵⁾	ILIM_HI	CDP load present ⁽⁶⁾	Data Lines Connected and Load Detect Active

- (1) TPS2546 : Current limit (I_{DS}) is automatically switched between I_{DS_PV} and the value set by ILIM_HI according to the Load Detect – Power Wake functionality.
(2) DCP Load present governed by the "Load Detection – Power Wake" limits.
(3) DCP Load present governed by the "Load Detection – Non Power Wake" limits.
(4) No OUT discharge when changing between 1111 and 1110.
(5) DCP Load present governed by the "Load Detection – Non Power Wake" limits and BC1.2 primary detection.



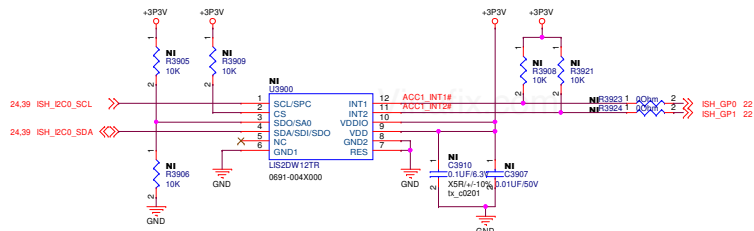
STATUS#, FAULT#, ILIM_LO, ILIM_HI Voltage: 0.3 to 7v.
STATUS#, FAULT# Continuous output sink current: 25mA.
ILIM_LO, ILIM_HI Continuous output source current: Internally limited.
SDP Mode (S0/S3/S4/S5) : 53.6k=0.9A
CDP (S0) & DCP (S3/S4/S5) Mode : 53.6k//80.6k=1.5A



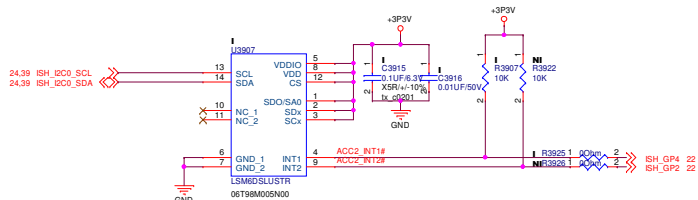
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PEGATRON		Title : USB CONN & POWER	
Pegatron Corp.		Engineer: Ryan_Yen	
Size	Project Name	Rev	
A2	Orion_N18E	A00	
Date: Friday, December 14, 2018		Sheet	38 of 93

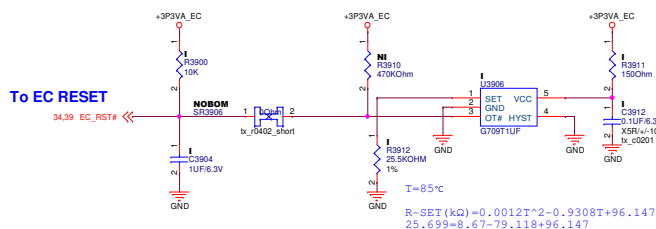
3-axis accelerometer



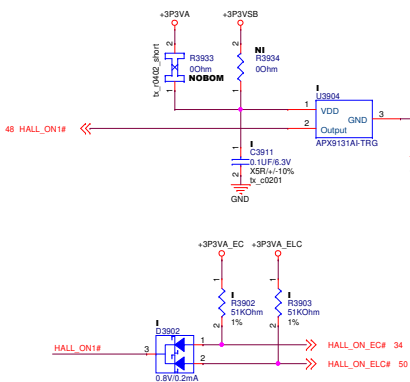
3D accelerometer and 3D gyroscope



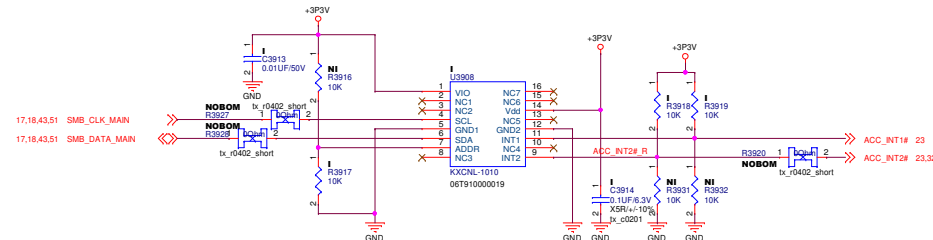
FOR HW thermal protection



HALL SENSOR

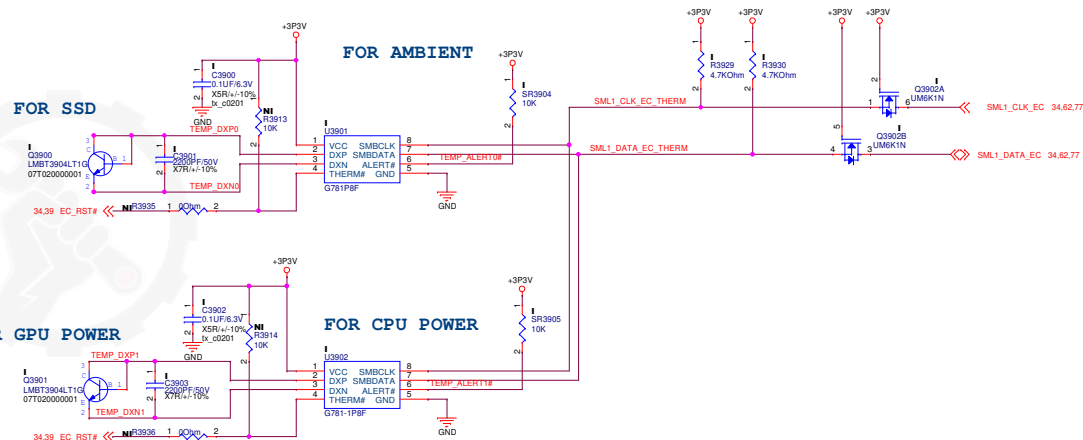


Free fall sensor



ADDR pin status	SAD	SAD + Read	SAD + Write
ADDR = 0	0011110 (1Eh)	00111101 (3Dh)	00111100 (3Ch)
ADDR = 1	0011101 (1Dh)	00111011 (3Bh)	00111010 (3Ah)

FOR SSD

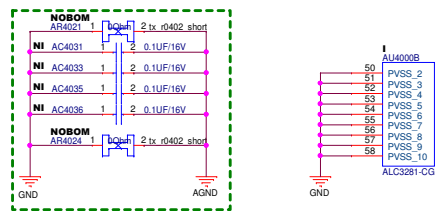
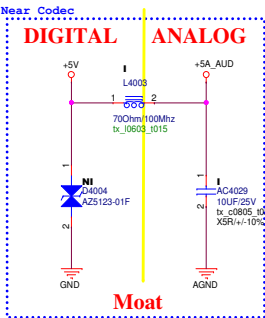
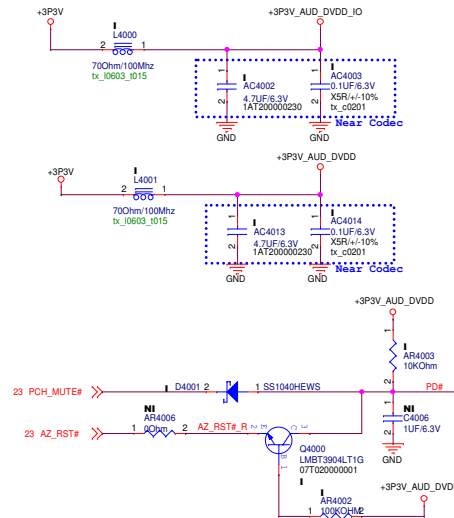


	A6	A5	A4	A3	A2	A1	A0
G781	1	0	0	1	1	0	0
G781-1	1	0	0	1	1	0	1

<Core Design>

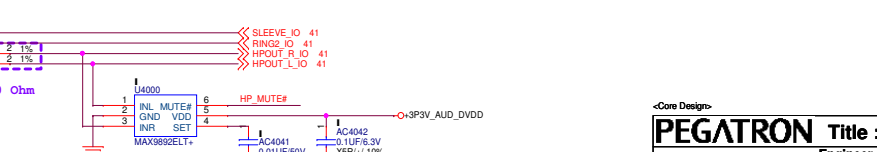
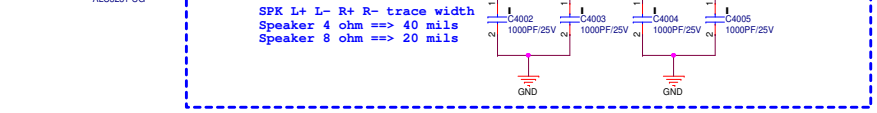
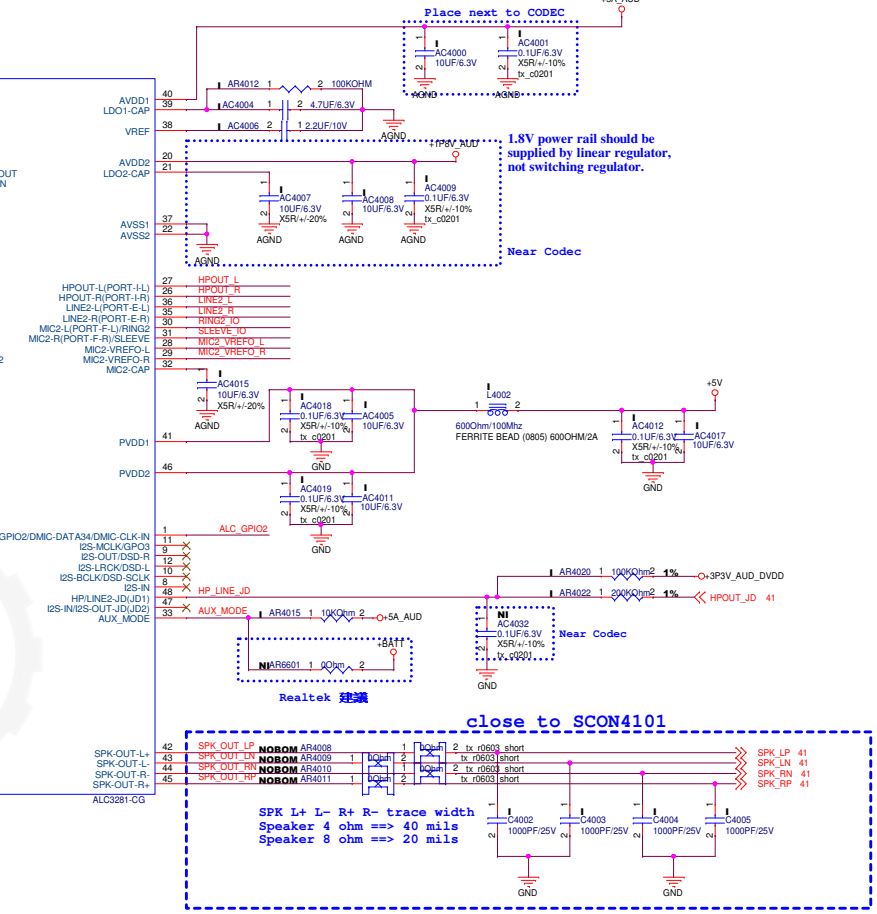
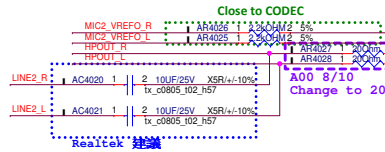
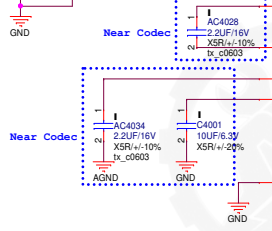
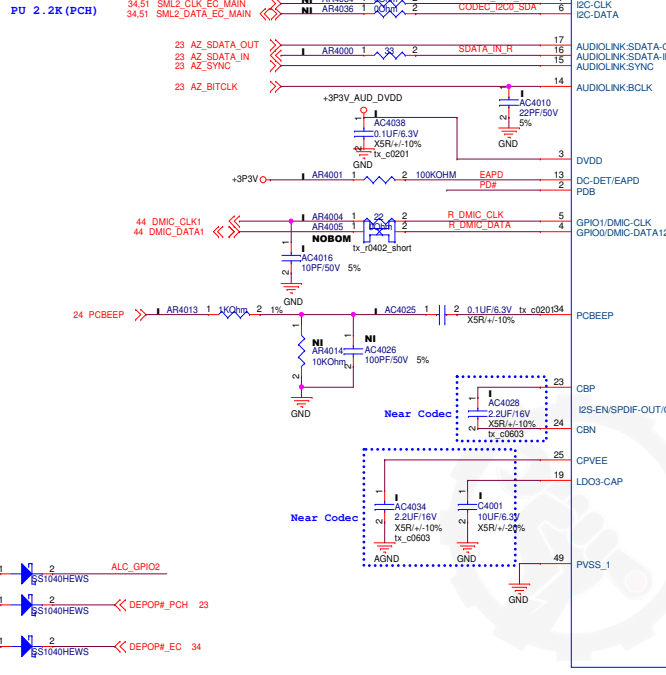
PEGATRON		Title : SENSOR
Size	Project Name	Engineer: Ryan_Yen
A2	Orion_N18E	Rev A00
Umr: Friday, December 14, 2018	Sheet 39	of 93

AUDIO CODEC- ALC3281



AR4021 Place at Codec bottom side.
AR4024 Place near audio connector. Don't short this pad to USB digital ground, and should be far away from any power traces.

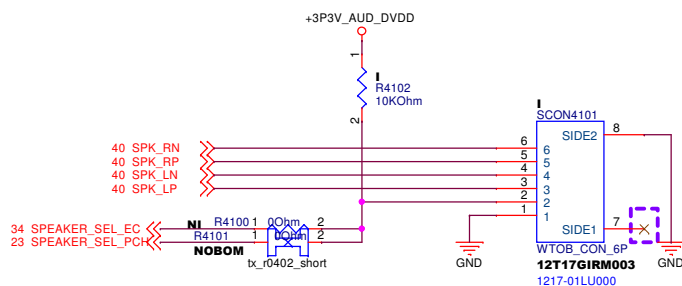
PU 2.2K (PCH)



OMTP/CTIA headset, Headphone, Line-Out, Microphone input, Line input.

This recommended phone-jack has moved #5/#6 Jack detect pin to the last position and lined up with #1 Tip pin. This kind of design will significantly improve the false detect caused by JD triggered timing

PCB trace width of MIC2-R(SLEEVE)/MIC2-L(RING2) are required at least 40 mil for HP crosstalk consideration and, its length should be as short as possible.
L4100/L4103 should choose DC resistance (Rdc) < 30m-ohm to get the best audio performance for HP crosstalk.



	15" FG	15" Zylux	17" FG	17" VECO	BIOS/EE setting
1st source (Pin1 & 2 open)	V		V		Pull High
2nd source (Pin1& 2 short)		V		V	Pull Low

<Core Design>

PEGATRON Title : **AUDIO JACK**

Engineer: Ryan_Yen

Size A3	Project Name Orion_N18E	Rev A00
Date: Friday, December 14, 2018		Sheet 41 of 93

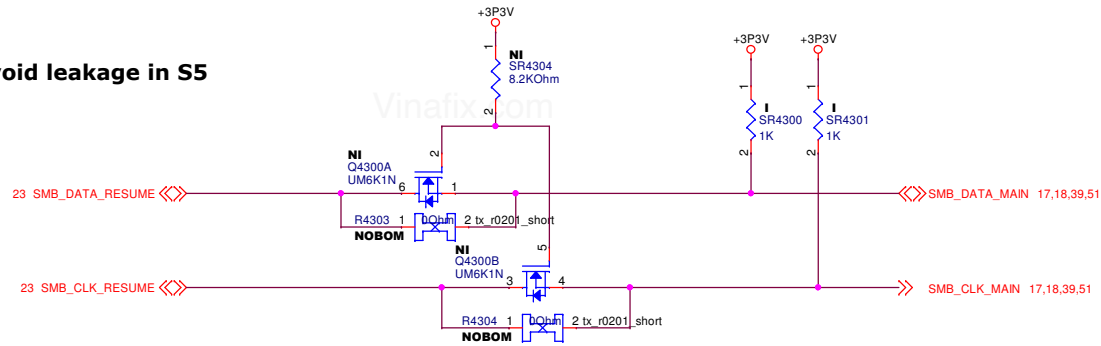
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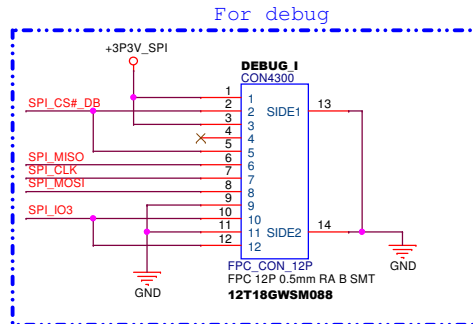
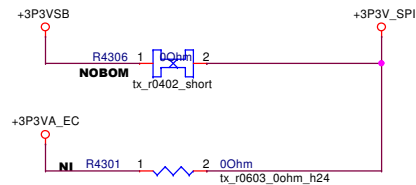
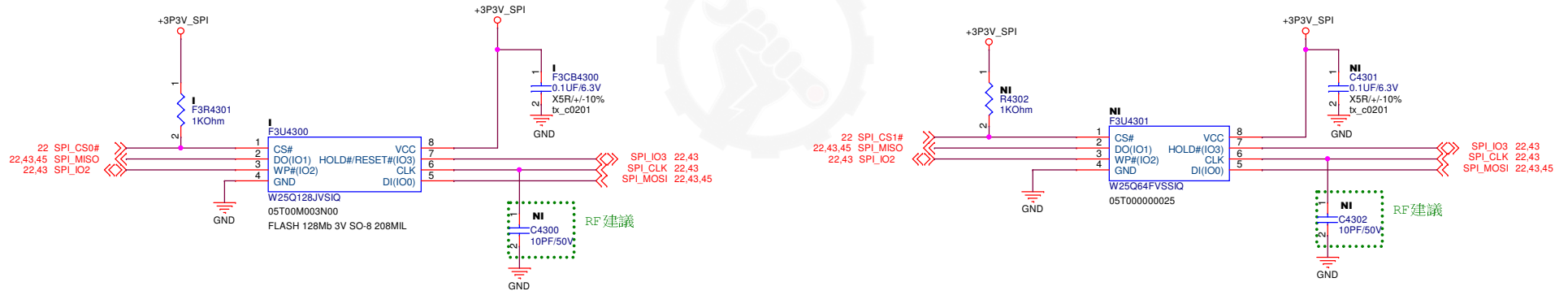
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PEGATRON		Title : USB Redriver	
Pegatron Corp.		Engineer: Ryan_Yen	
Size A3	Project Name Orion_N18E		Rev A00
Date: Friday, December 14, 2018		Sheet 42 of 93	

Avoid leakage in S5



SPI ROM (Quad I/O Supported)



PEGATRON DT-MB RESTRICTED SECRET

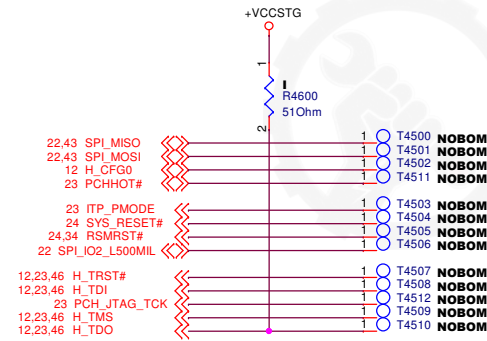
PEGATRON Title : **SM BUS & SPI ROM**

Pegatron Corp. Engineer: **Ryan_Yen**

Size A3 Project Name **Orion_N18E** Rev A00

Date: Friday, December 14, 2018 Sheet 43 of 93

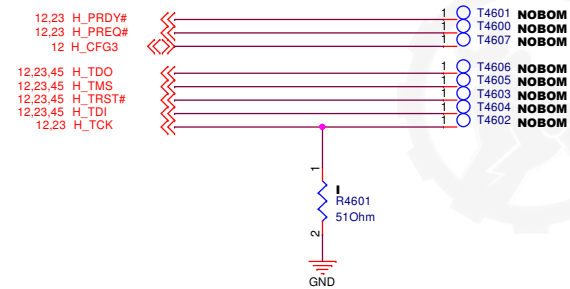
INTEL PCH DEBUG TESTPOINT



<Core Design>

PEGATRON		Title : DEBUG TESTPOINT(PCH)	
Pegatron Corp.		Engineer: Ryan_Yen	
Size A3	Project Name Orion_N18E		Rev A00
Date: Friday, December 14, 2018		Sheet 45 of 93	

INTEL CPU DEBUG TESTPOINT



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **DEBUG TESTPOINT(CPU)**

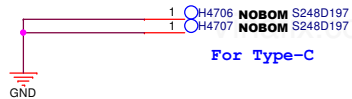
Pegatron Corp. Engineer: **Ryan_Yen**

Size A3	Project Name Orion_N18E	Rev A00
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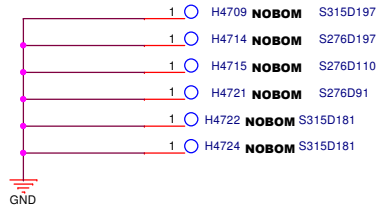
Date: Friday, December 14, 2018 Sheet 46 of 93

NI_TEMP
PCB4700
PCB
PCB_BOARD
CCL = Y

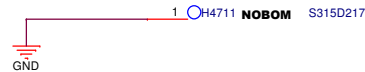
方圓孔 (6.3*6.3, D2.3) 靠近CON3000 (USB TYPE-C) · 2顆



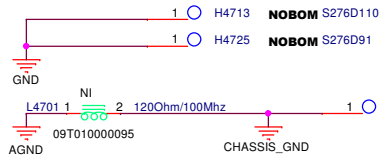
方圓孔 (7*7, D2.3), 1顆
方圓孔 (8*8, D5), 1顆
方圓孔 (7*7, D5), 1顆
方圓孔 (7*7, D2.8), 1顆
方圓孔 (8.8, D4.2), 2顆



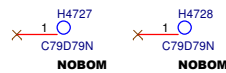
方圓孔 (8*8, D5.5), 1顆



方圓孔 (7*7, D2.8), 4顆

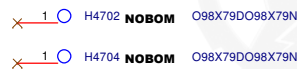


圓孔 2.0mm · 1顆

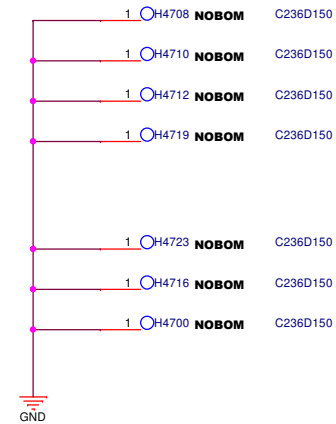


PPID

橢圓孔 2.5mm*2.0mm · 2顆

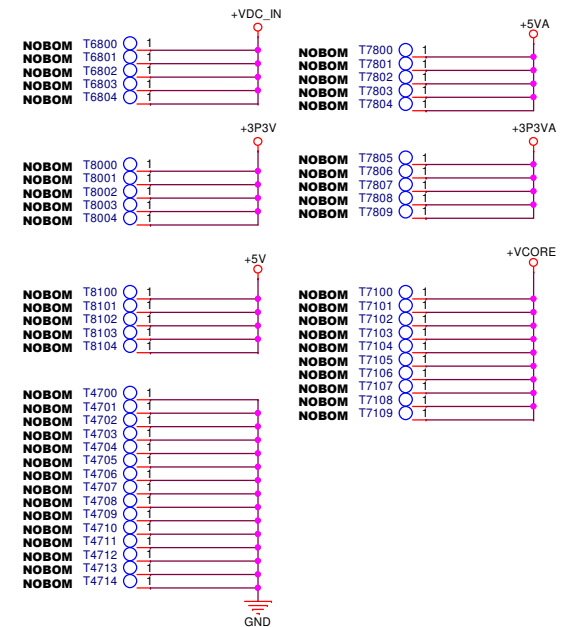


圓孔 (6*6, D3.8), 7顆



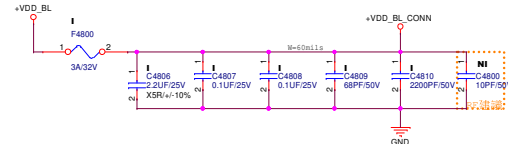
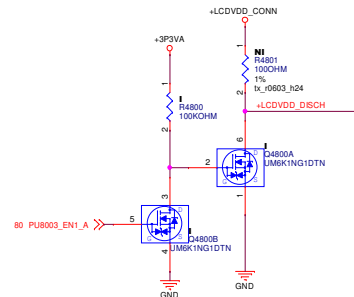
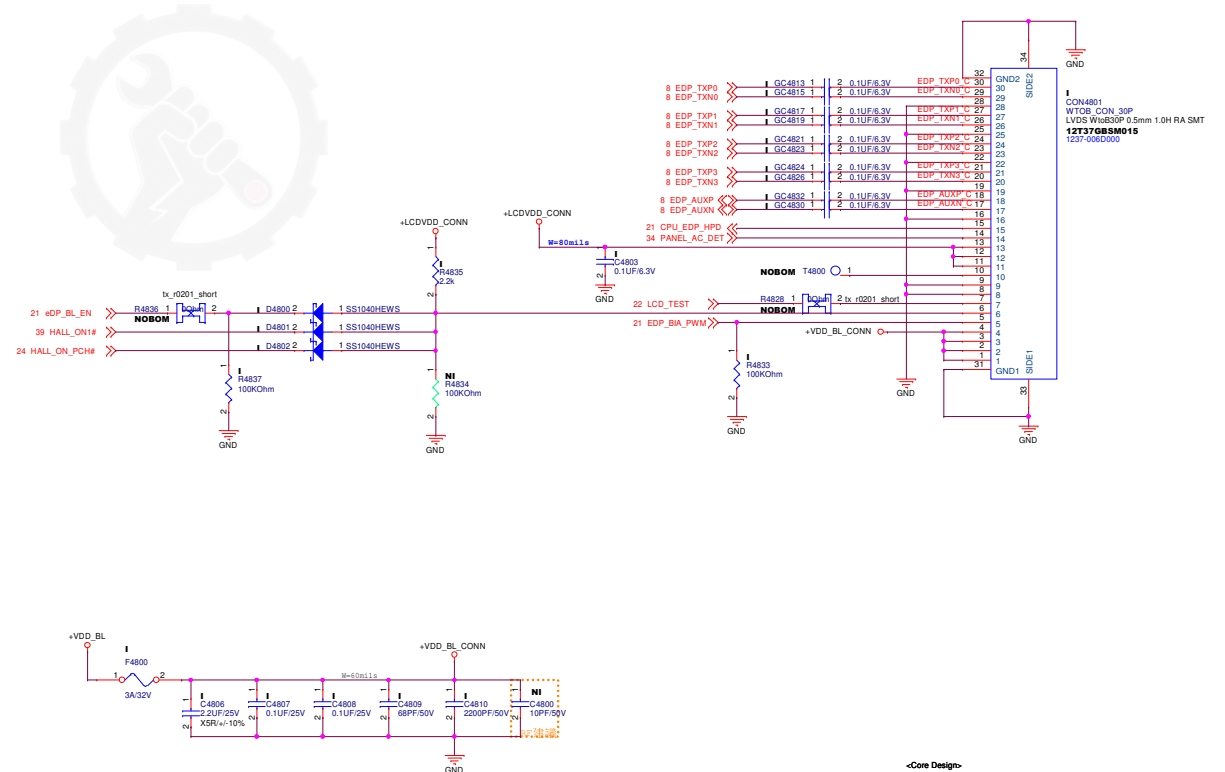
For CPU

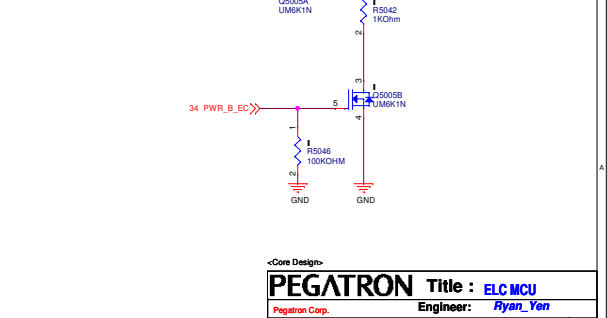
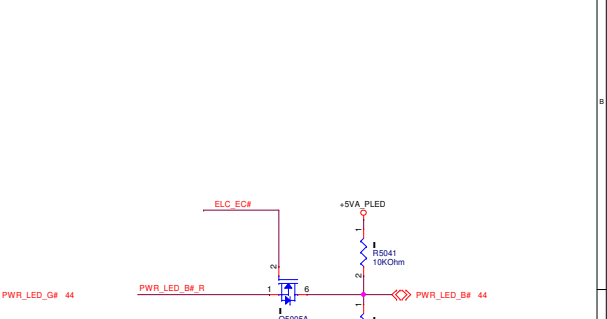
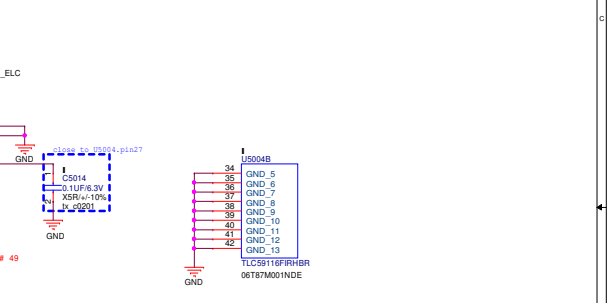
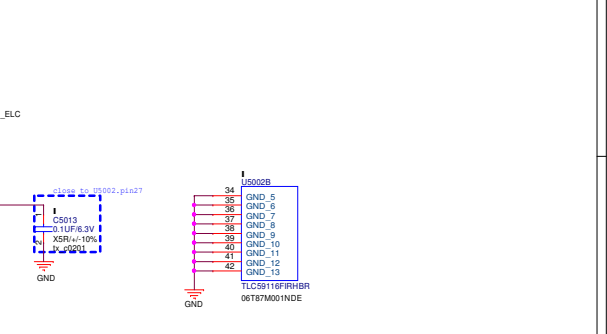
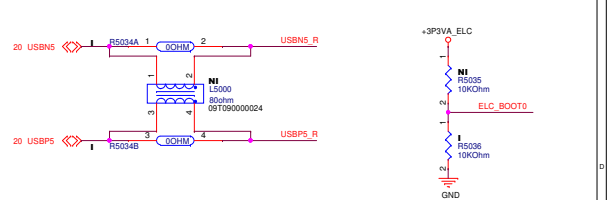
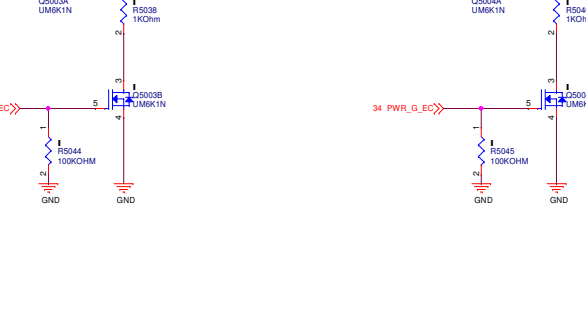
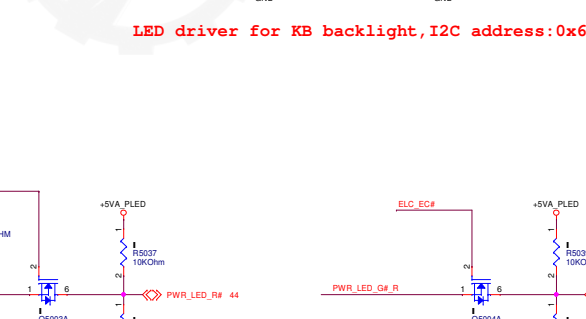
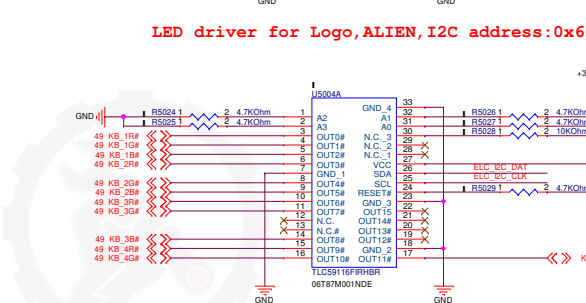
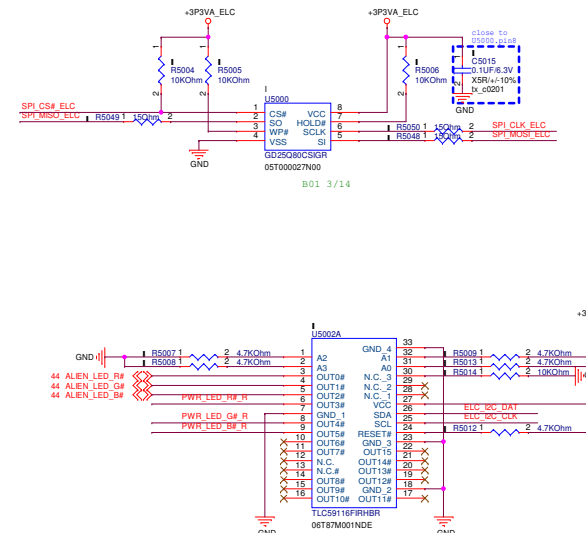
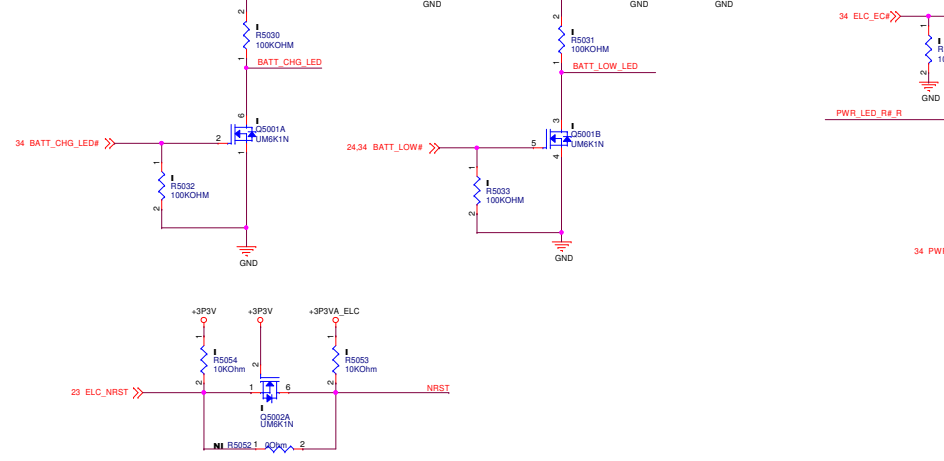
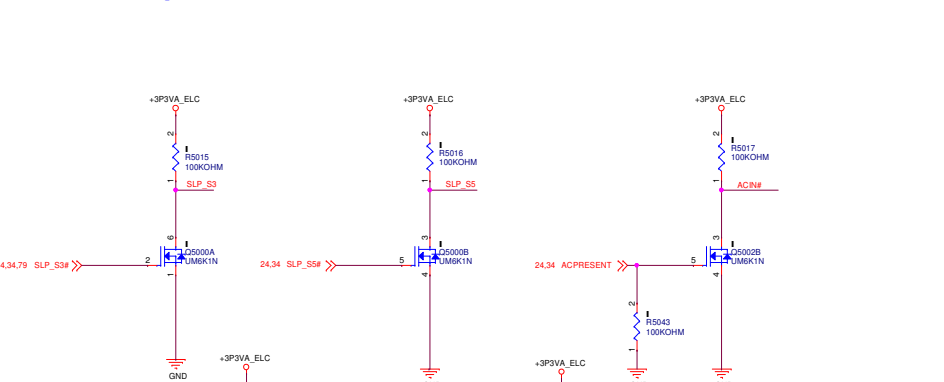
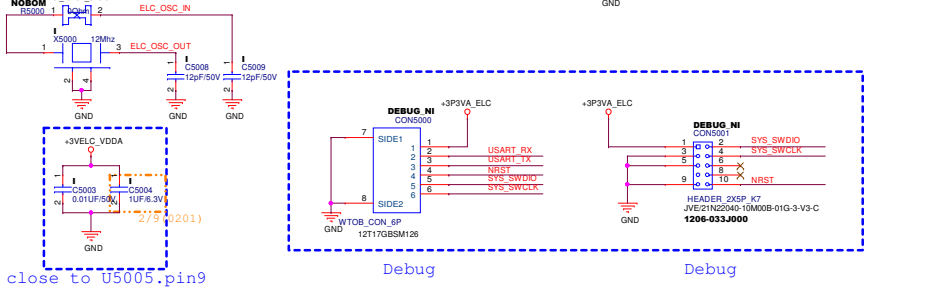
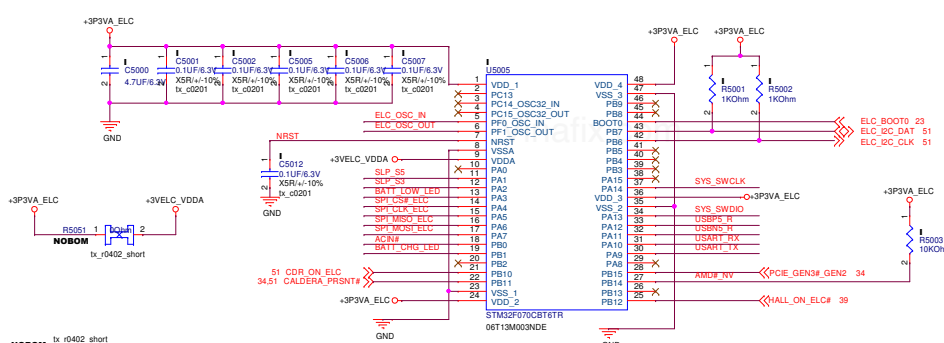
For GPU



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : PCB & Label & Screw	
Pegatron Corp.		Engineer: Ryan_Yen	
Size A3	Project Name Orion_N18E	Date: Friday, December 14, 2018	Rev A00
Sheet 47 of 93			

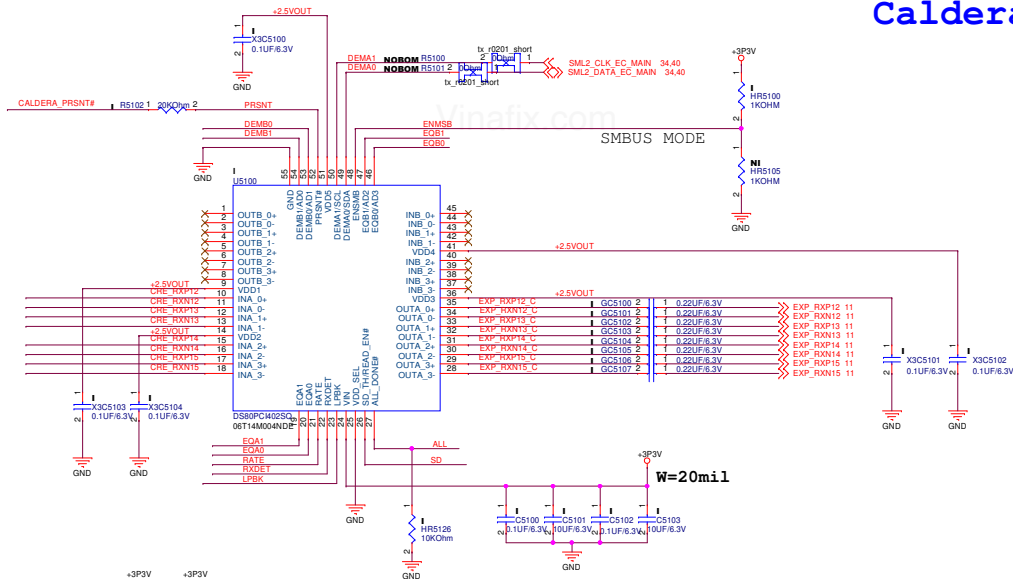




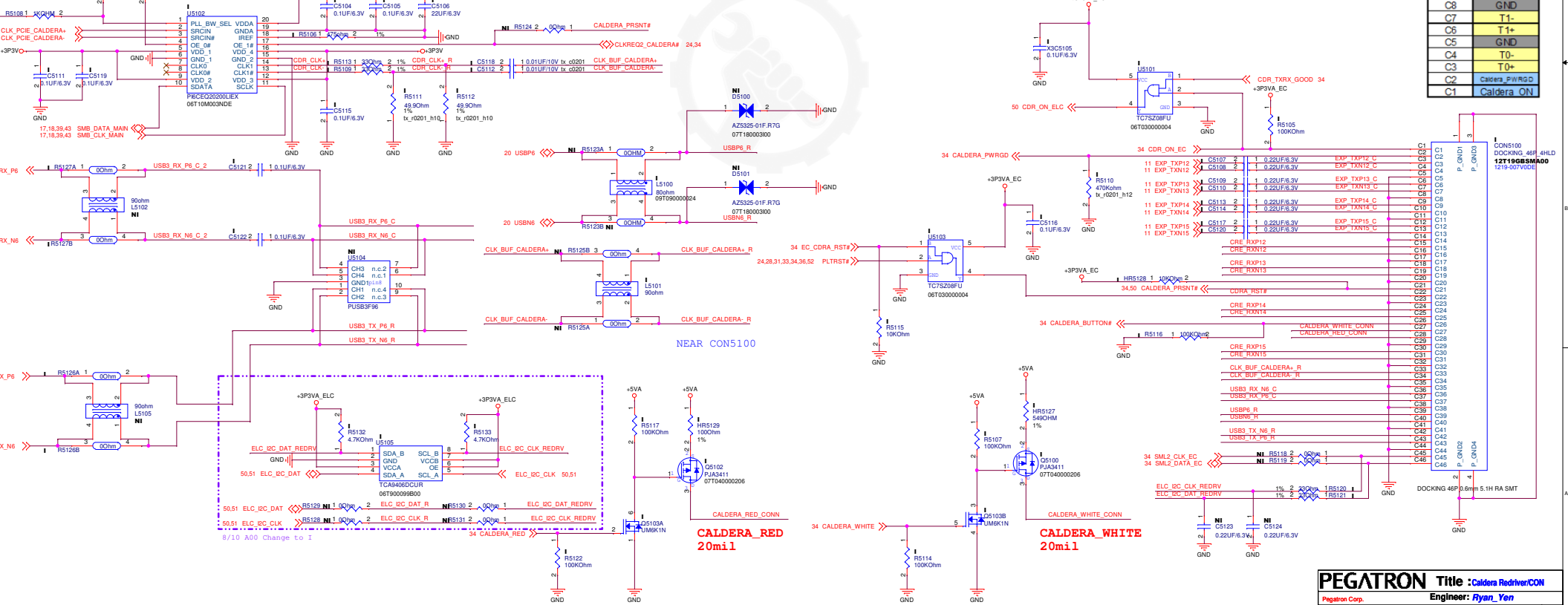
Caldera Redriver

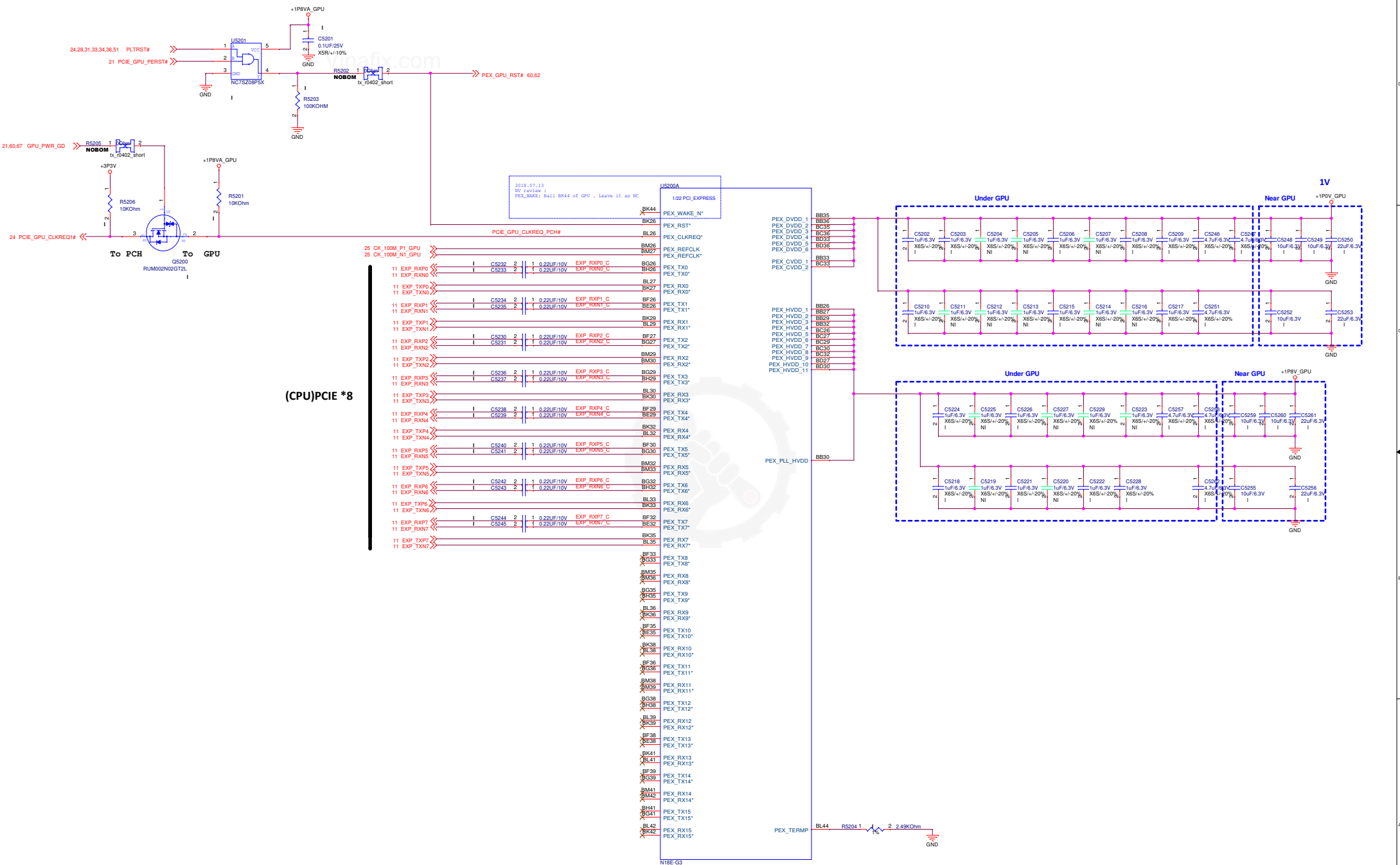
Pin Number	SIO Definition	Usage for Caldera	Comment
37	YLW_LED/GPIO30/S1CT	CALDERA_BUTTON#	User will press this button when they want to initiate an undock event
38	GPIO31/PE/P2_D0L#	CALDERA_PSRNT#	Use for internal cable-detect mechanism
39	GPIO32/BU5Y/P2_D0L#	CALDERA_PWRGD	
53	GRN_LED/GPIO13/STB#	CALDERA_ON	Control the PS_ON# pin to the Caldera ATX PSU
81	GPIO70/TACHPWM4/CIRRX	CALDERA_RED#	
82	GPIO73/TACHPWM5/CIRWB	CALDERA_WHITE#	

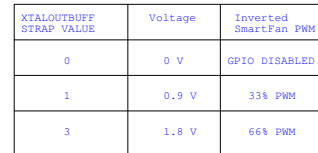
Pin #	Name
C46	I2C_CLK
C45	I2C_DATA
C44	GND
C43	SSRX-
C42	SSRX+
C41	GND
C40	USB D+
C39	USB D-
C38	GND
C37	SSTX-
C36	SSTX+
C35	GND
C34	REFCLK-
C33	REFCLK+
C32	GND
C31	R3-
C30	R3+
C29	GND
C28	LED RED
C27	LED WHITE
C26	BUTTON#
C25	R2-
C24	R2+
C23	GND
C22	PLTRST#
C21	DOCK_DET#
C20	GND
C19	R1-
C18	R1+
C17	GND
C16	R0-
C15	R0+
C14	GND
C13	T3-
C12	T3+
C11	GND
C10	T2-
C9	T2+
C8	GND
C7	T1-
C6	T1+
C5	GND
C4	T0-
C3	T0+
C2	Caldera_PWRGD
C1	Caldera_ON



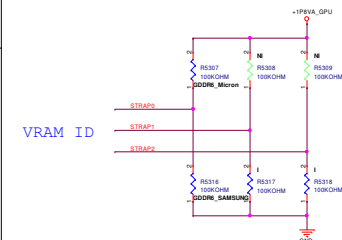
Caldera Connector







Strap Pins <small>see Note</small>			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)

[illegible]

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	L	0	0	0	0
L	L	L	0	0	0	1
L	L	L	0	0	0	0

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

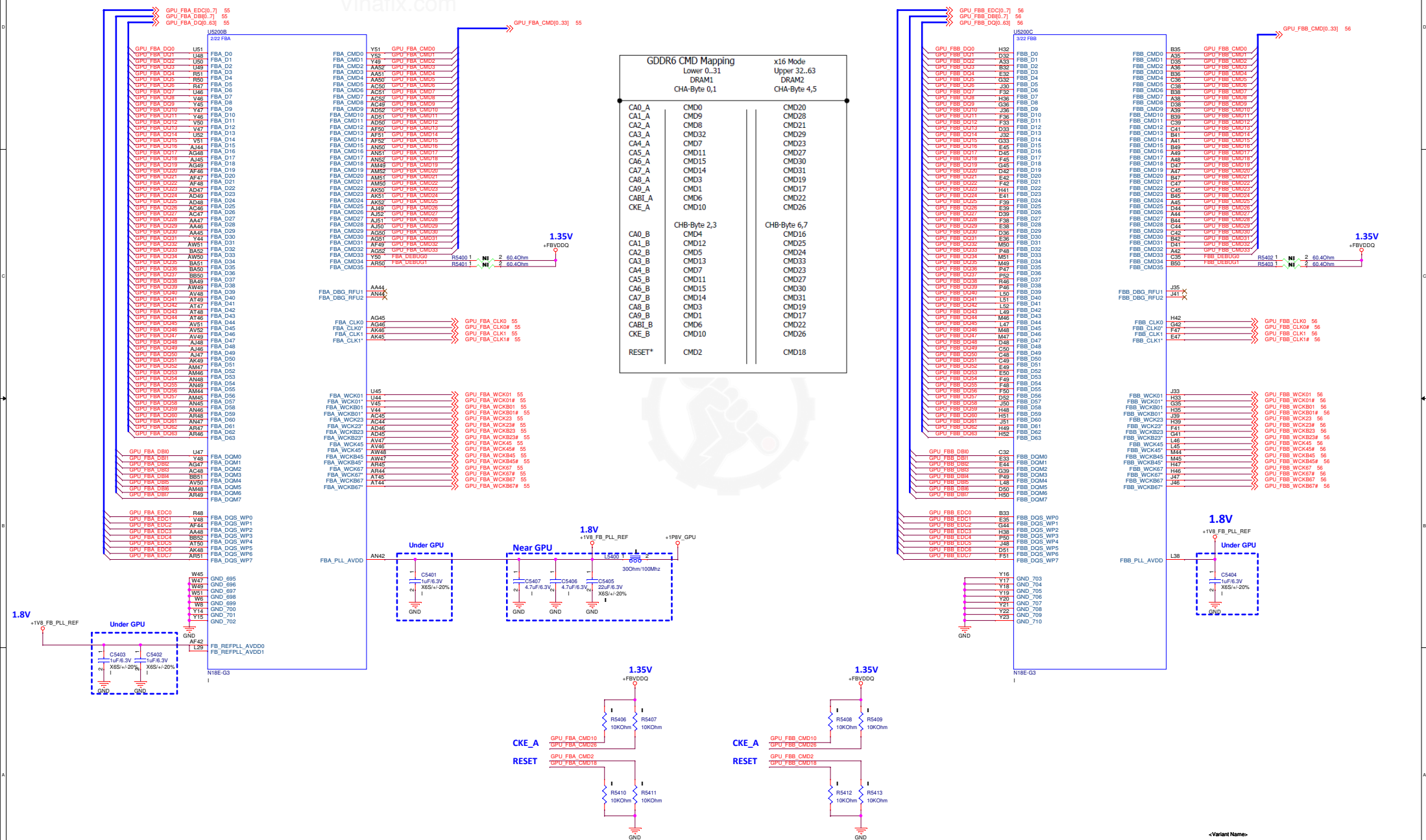
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

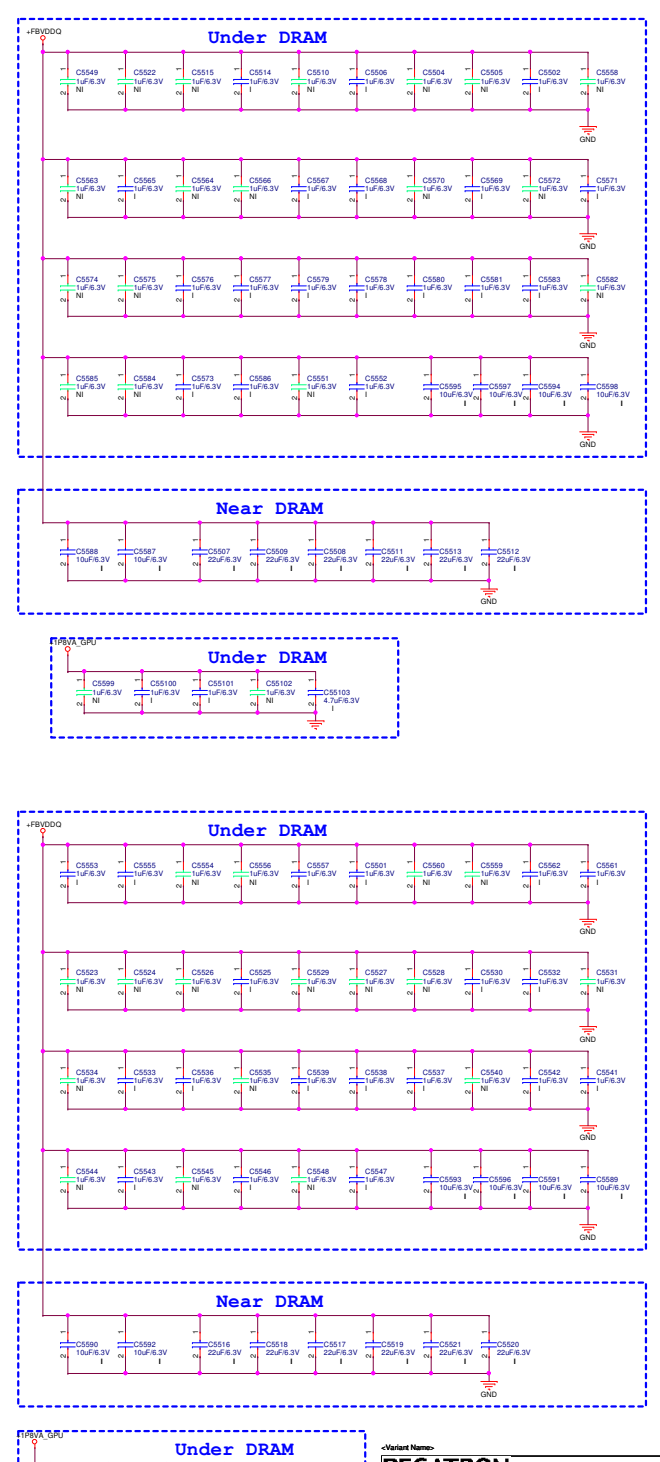
Default

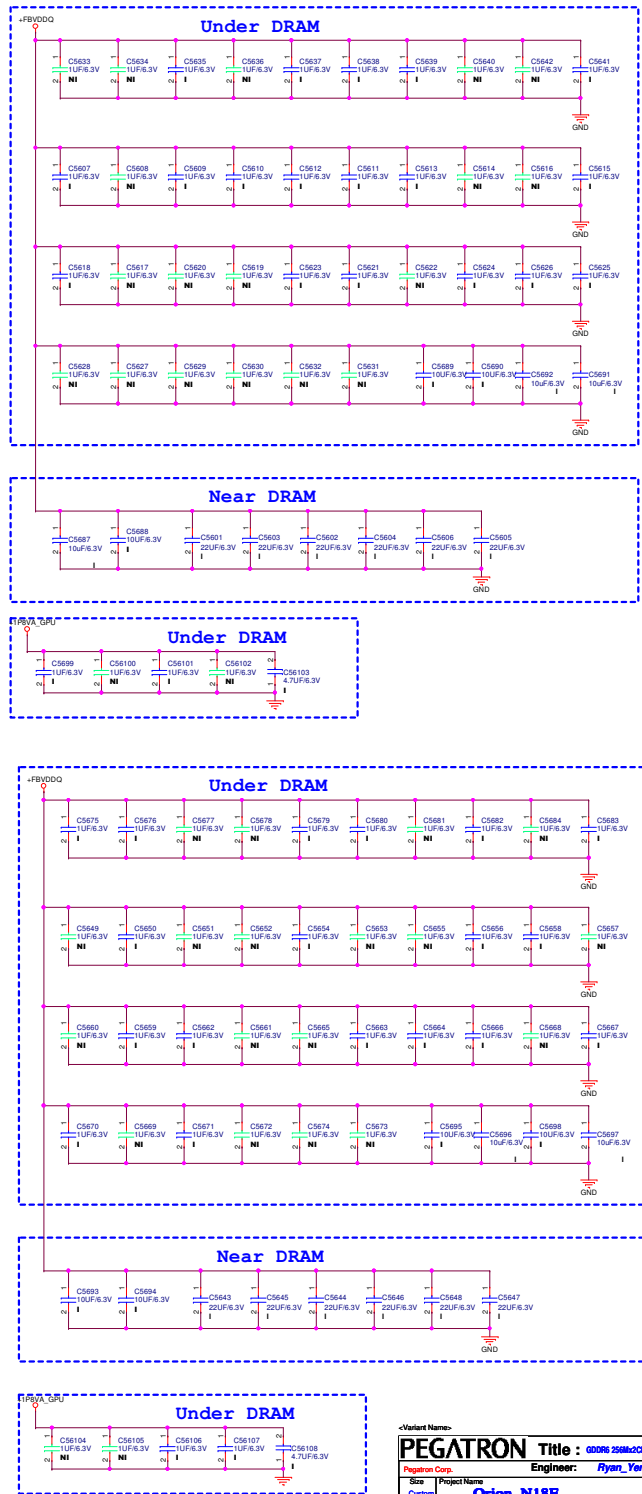
Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx2Chx16	1.35V	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	N/A	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	N/A	Full	Production candidate

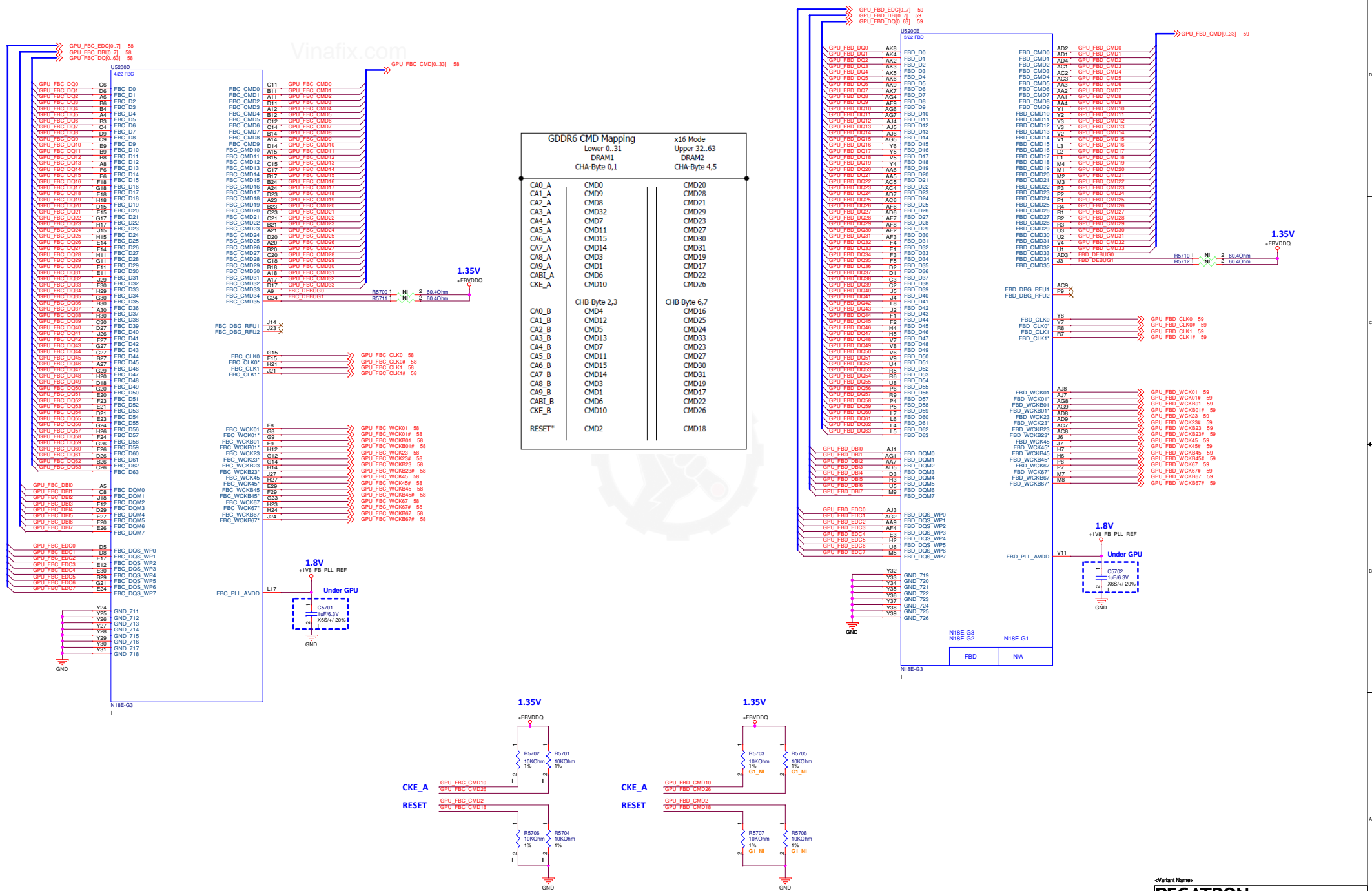
1. For N18E-G3, the maximum allowable memory case temperature is 95 °C.

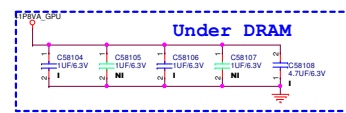
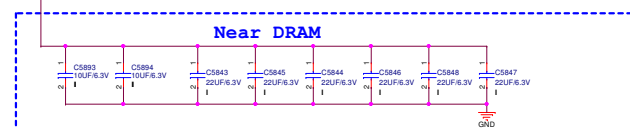
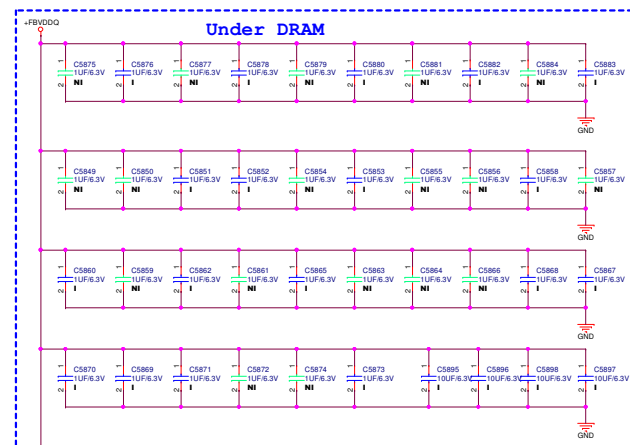
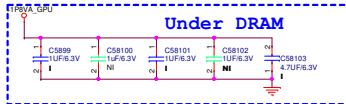
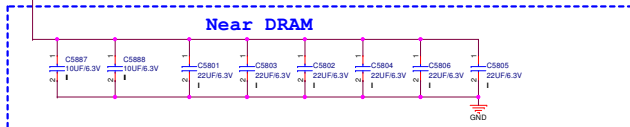
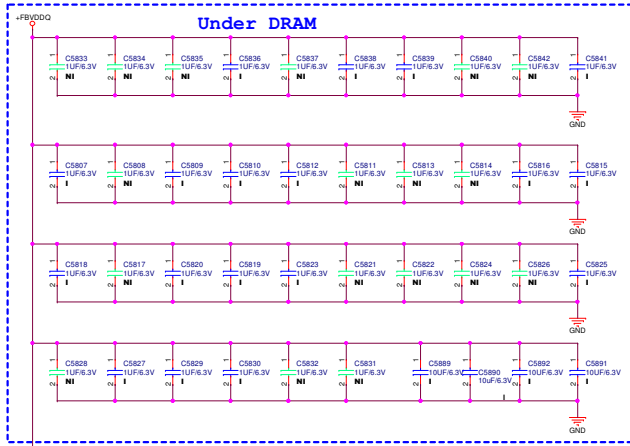
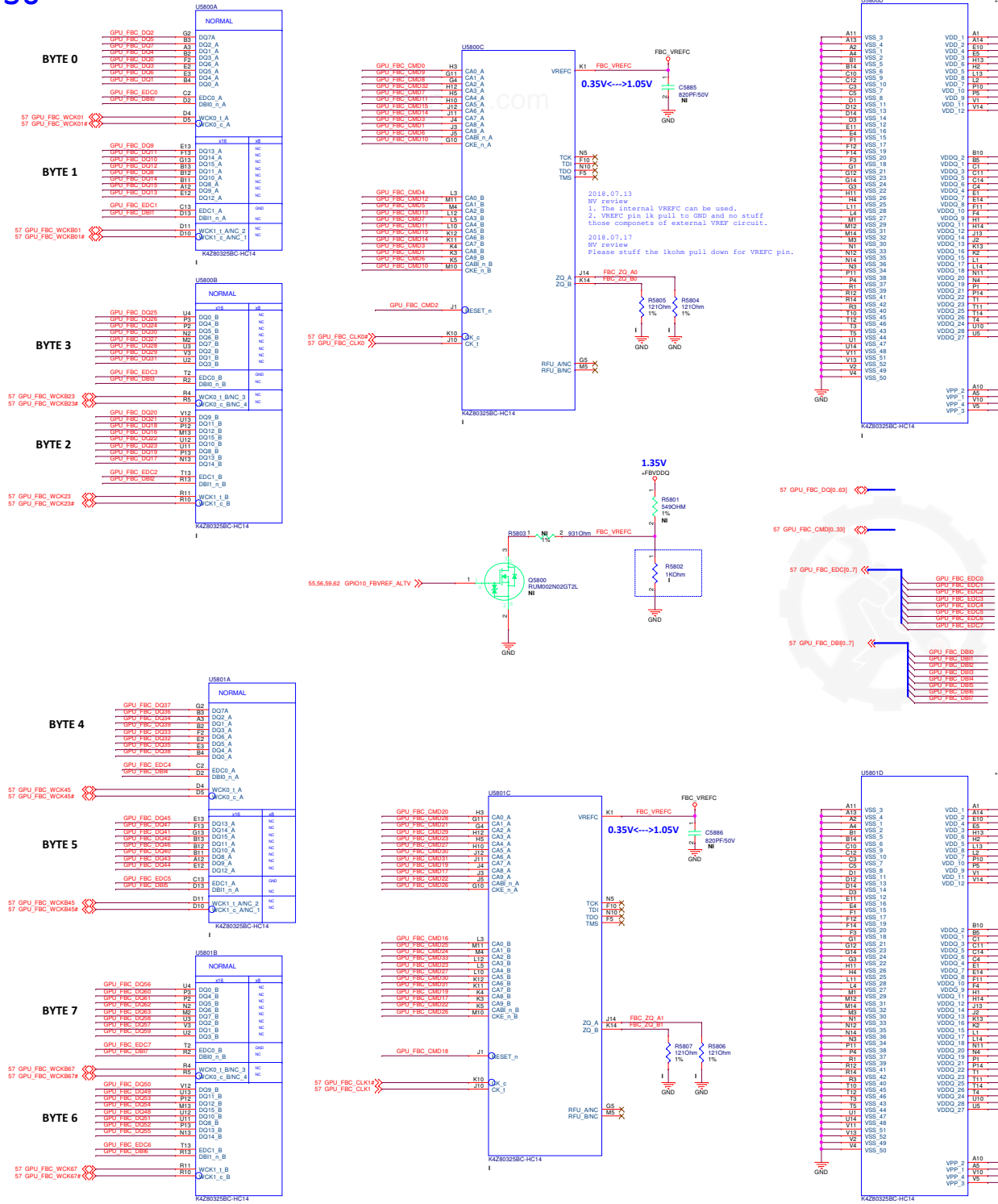
GPU-BUFFER PARTITION A/B

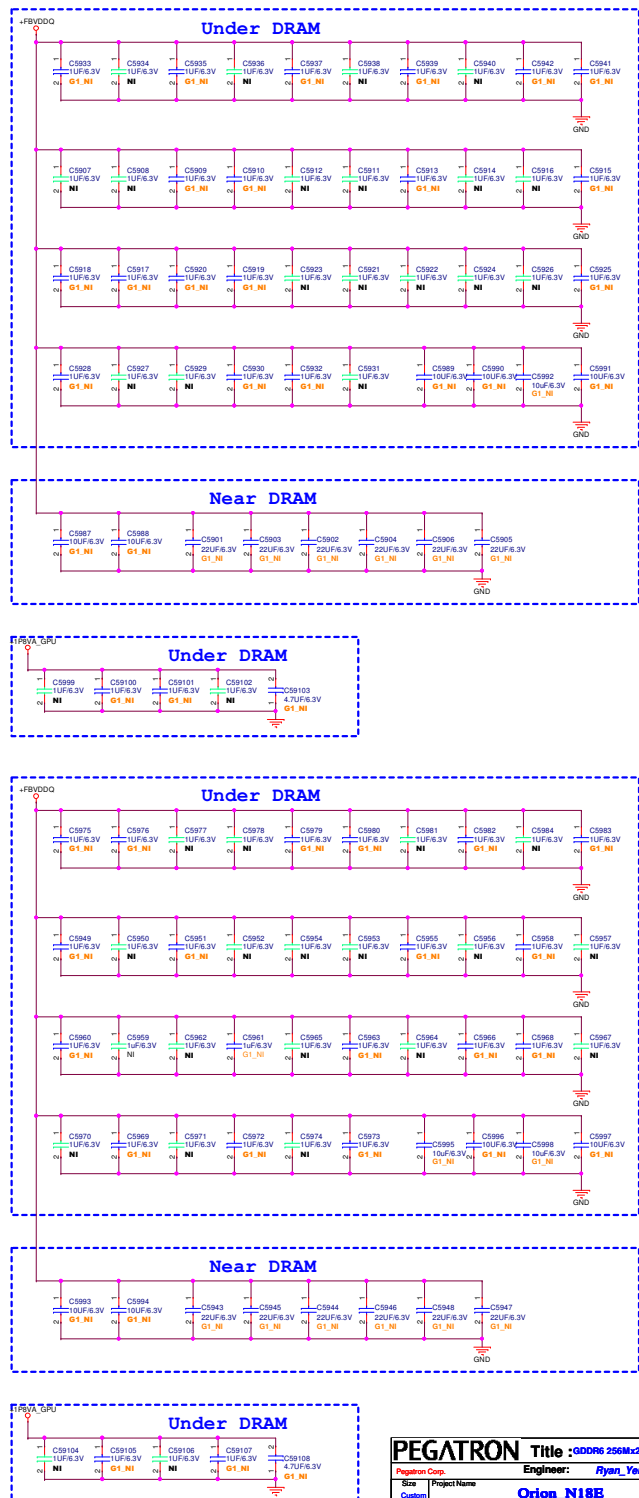








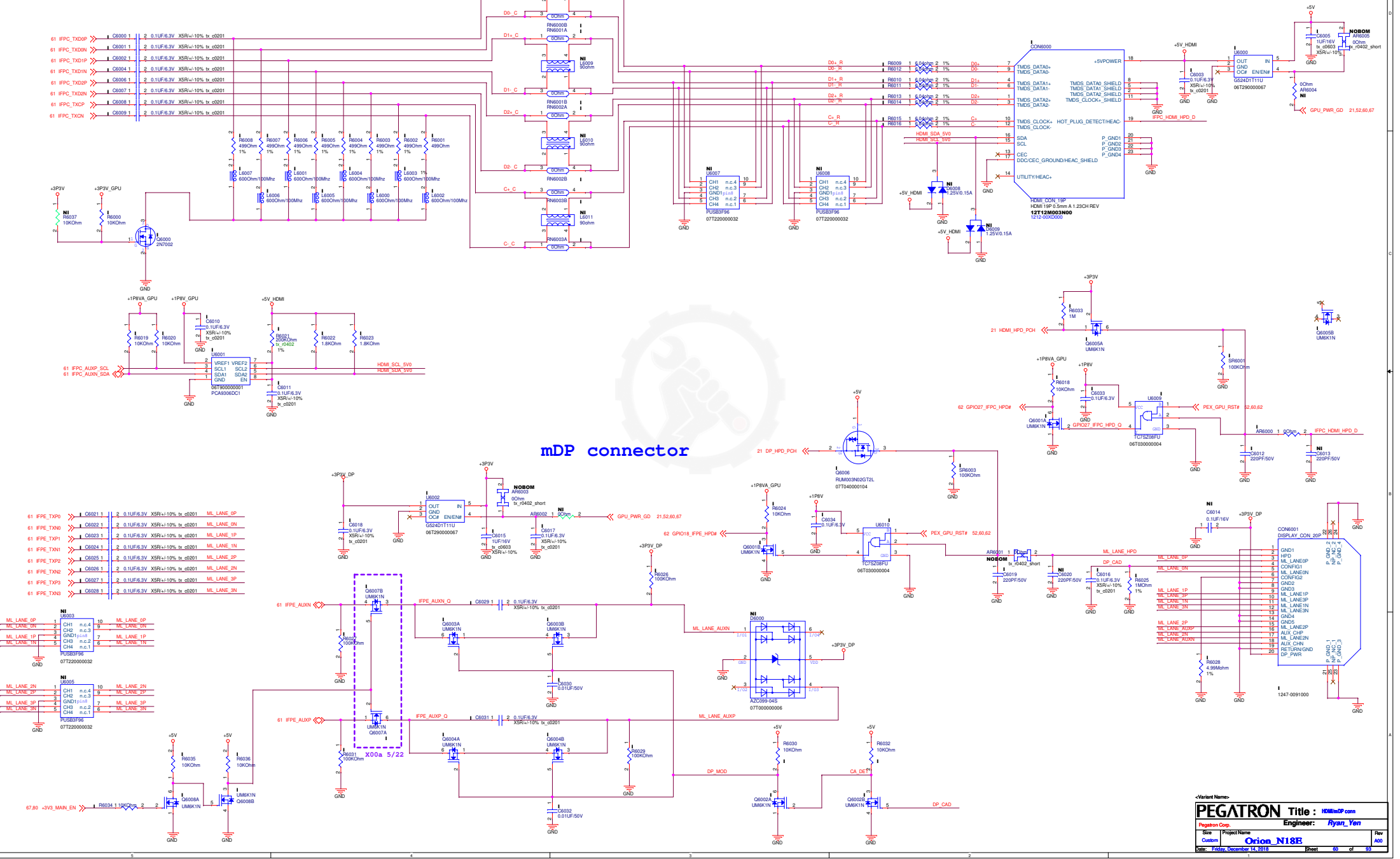


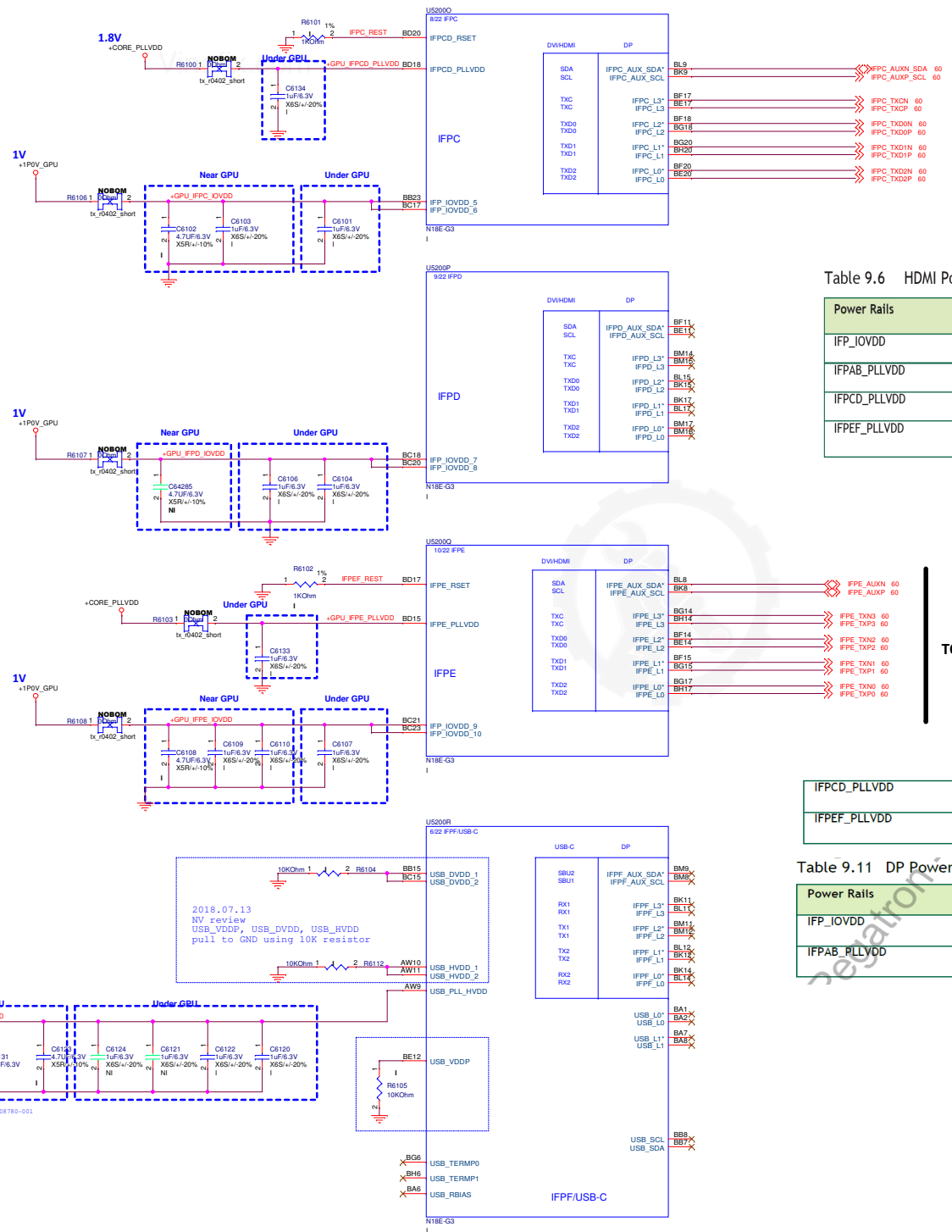


HDMI/MDP conn

HDMI out connector

Vinafix.com





TO HDMI

TO mDP

Table 9.6 HDMI Power Rails

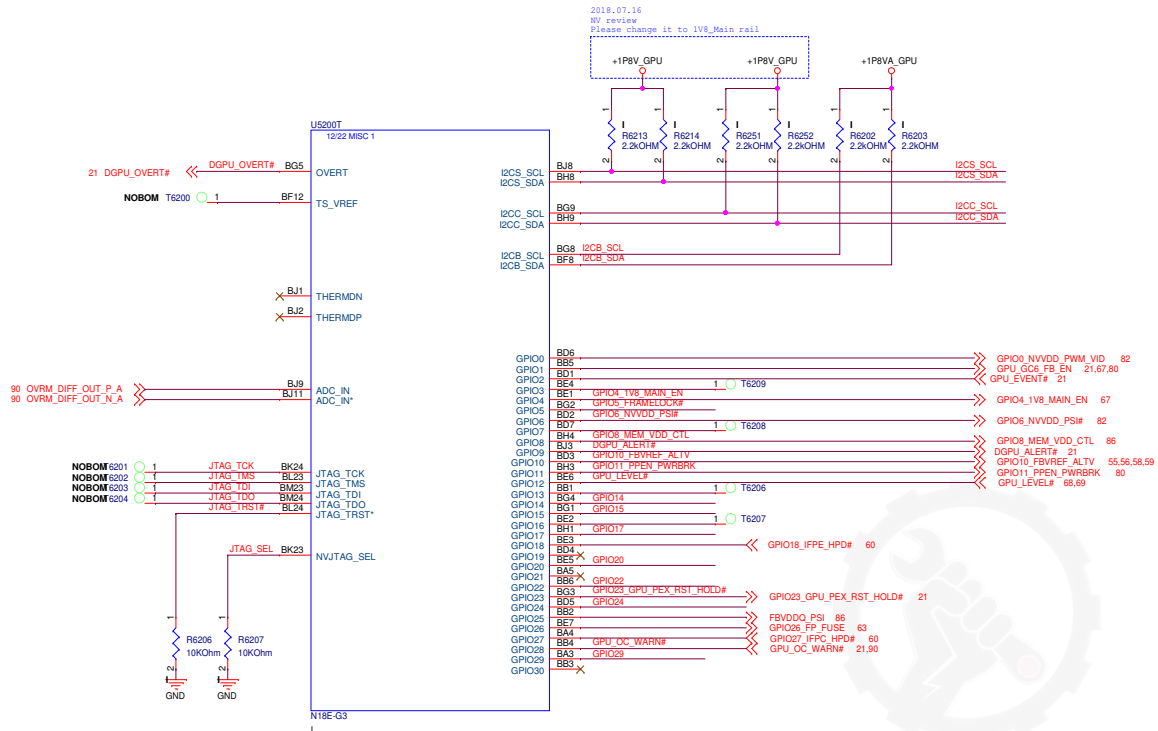
Power Rails	Voltage	Maximum Current Draw
IFPD_IOVDD	1.0 V ± 5%	~87 mA
IFPAB_PLLVDD	1.8 V ± 10%	~98 mA
IFPCD_PLLVDD	1.8 V ± 10%	~98 mA
IFPEF_PLLVDD	1.8 V ± 10%	~98 mA

IFPCD_PLLVDD	1V8 V ± 10%	~102 mA
IFPEF_PLLVDD	1V8 V ± 10%	~102 mA

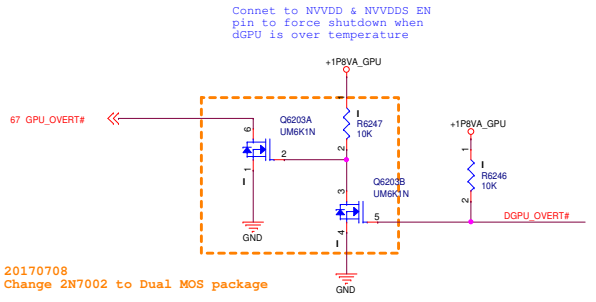
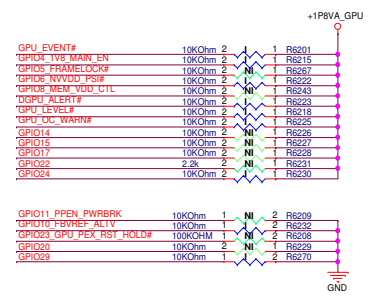
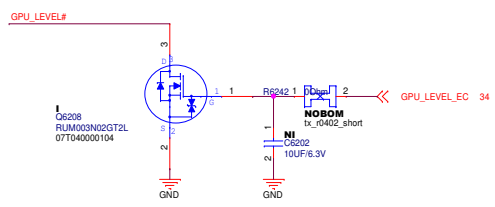
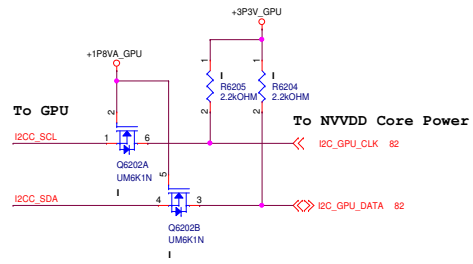
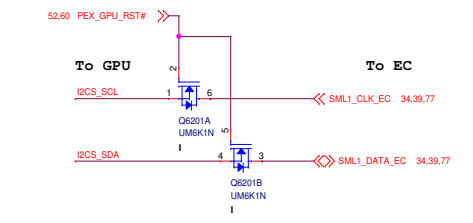
Table 9.11 DP Power Rails

Power Rails	Voltage	Maximum Current Draw
IFPD_IOVDD	1.0 V ± 5%	~118 mA
IFPAB_PLLVDD	1V8 V ± 10%	~102 mA

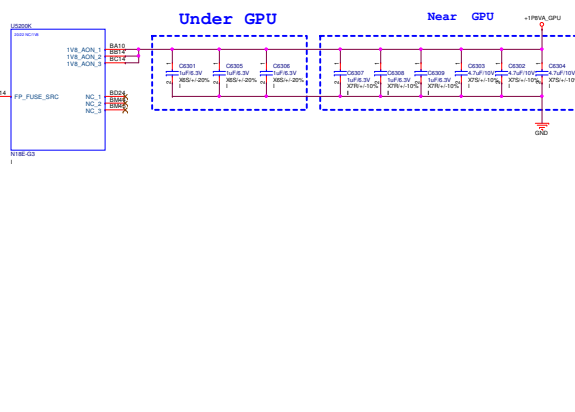
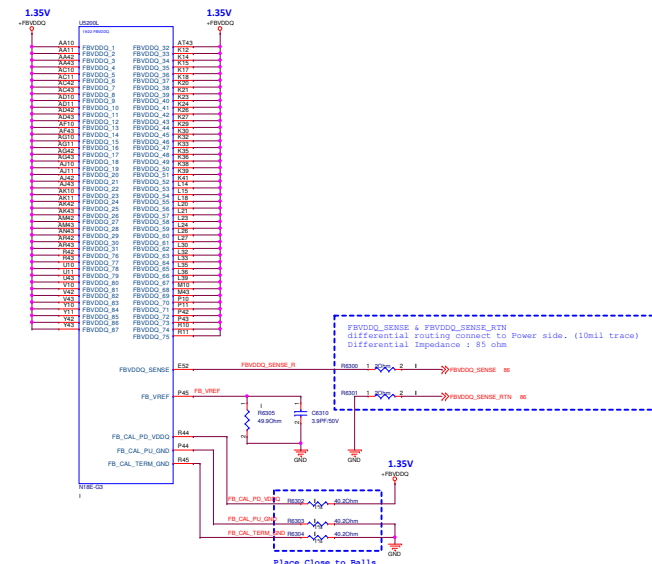
Vinafix.com



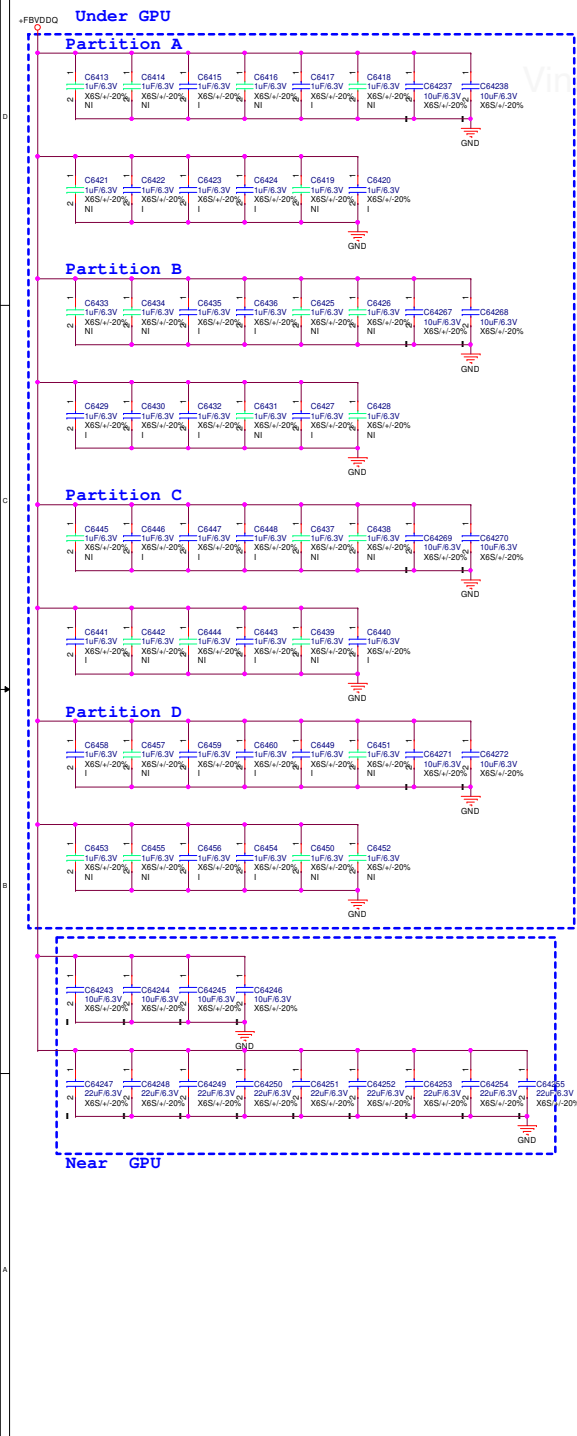
2018.07.05
D0-08780-001 P221
Unused GPIOs may be left floating (NC) on the board design.



20170708
Change 2N7002 to Dual MOS package



+FBVDDQ



+NVVDD



<Variant Name

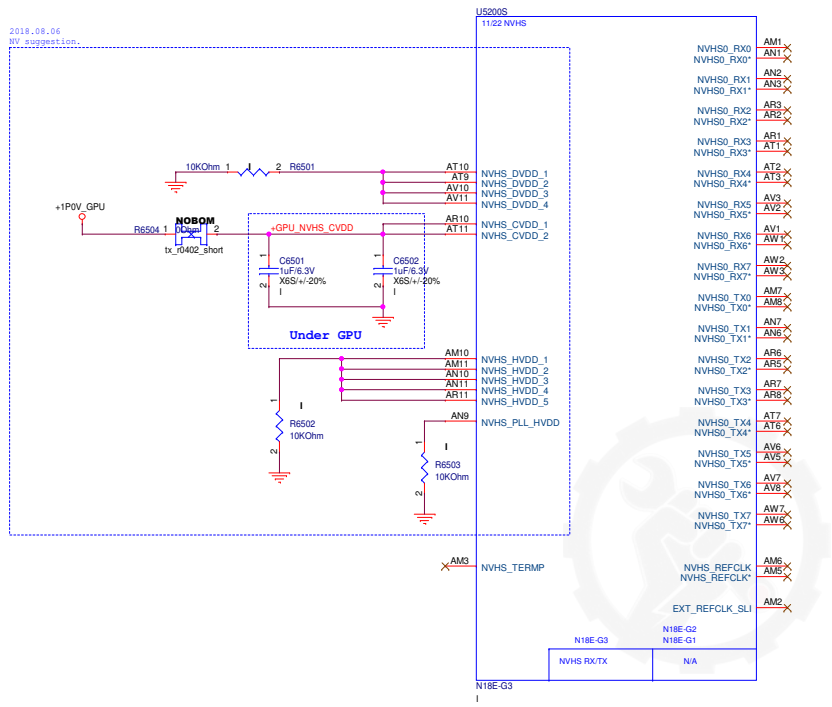
PEGATRON Title : GPU-Decoupling

Engineer: Ryan_Yen

Size	Project Name
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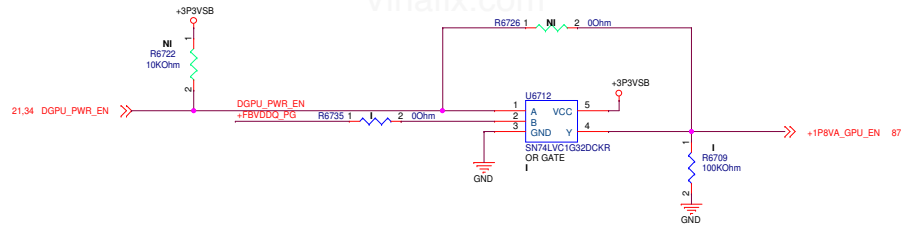
A2	Orion_N18E
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Vinafix.com

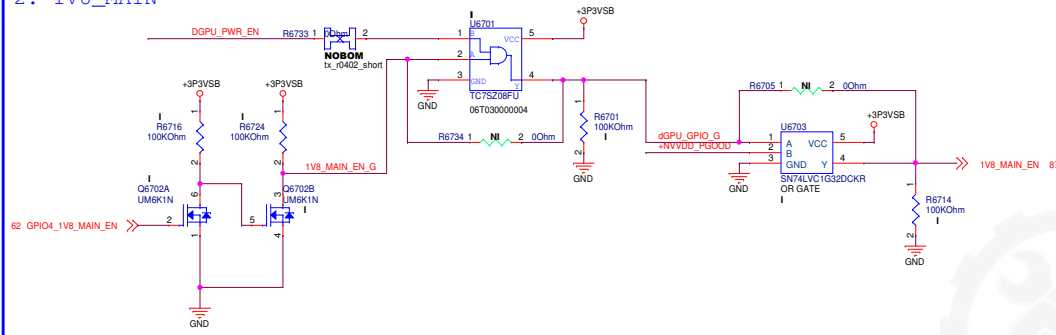


PEGATRON		Title : GPU_IFPAB_DDI	
Pegatron Corp.		Engineer: <i>Ryan_Yen</i>	
Size C	Project Name Orion_N18E	Rev A00	
Date: Friday, December 14, 2018		Sheet	66 of 94

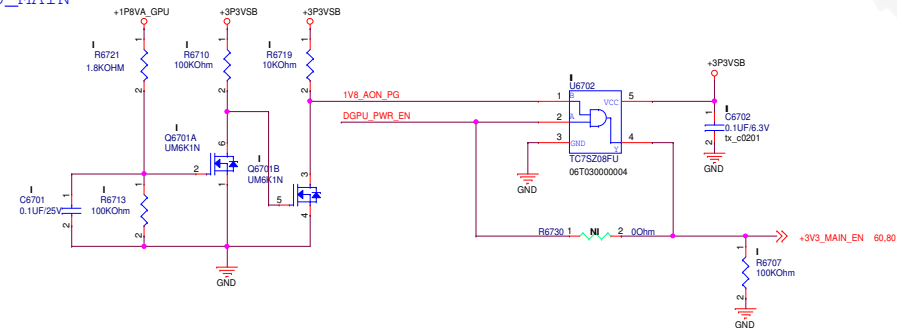
1. 1V8_AON



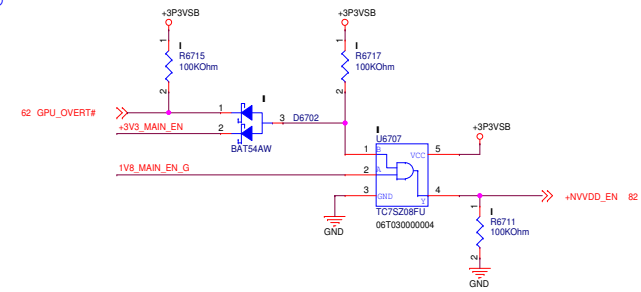
2. 1V8_MAIN



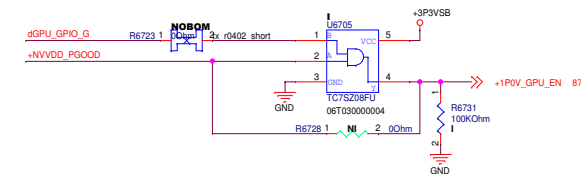
3. 3V3_MAIN



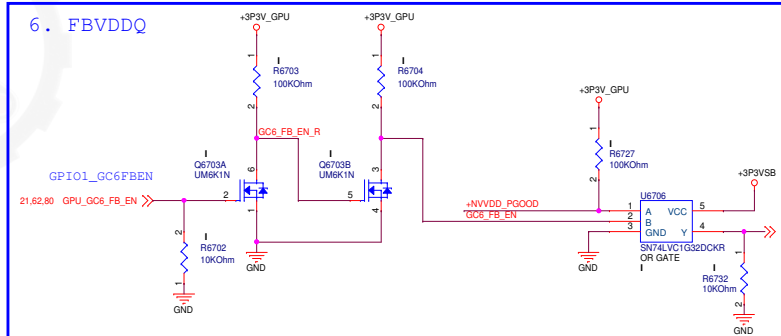
4. NVVDD



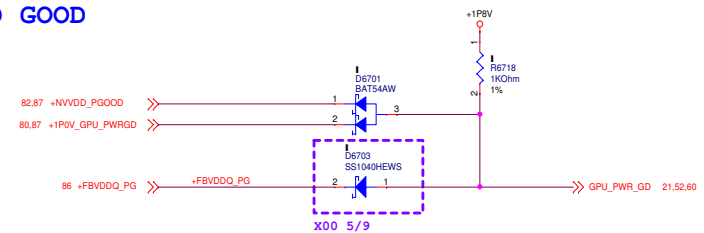
5. PEX_VDD



6. FBVDDQ

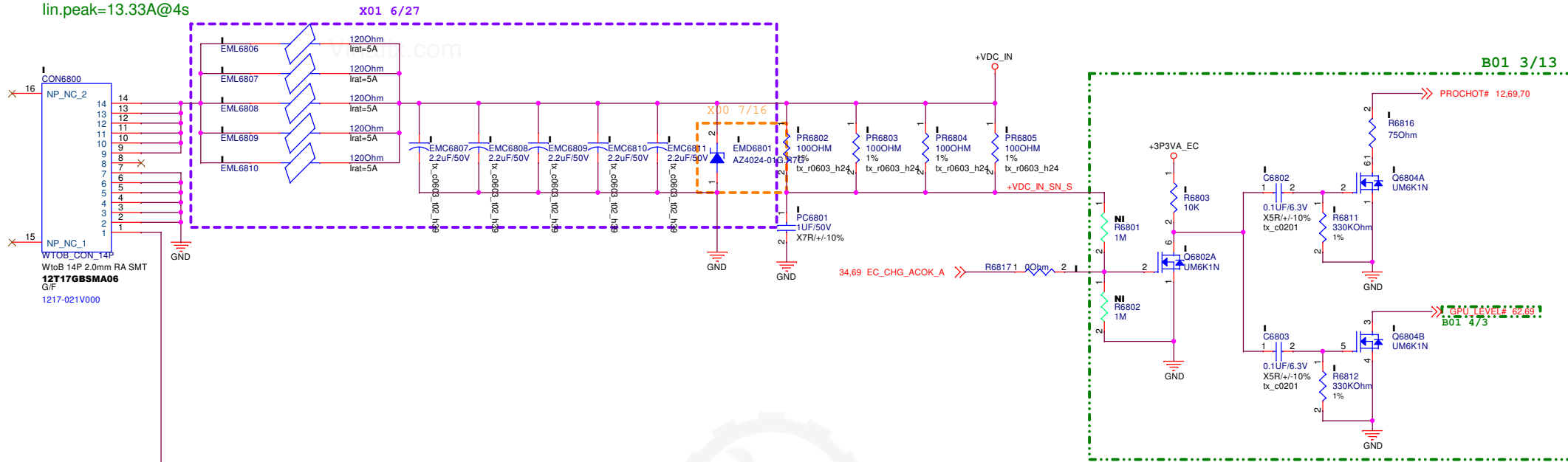


BOARD GOOD

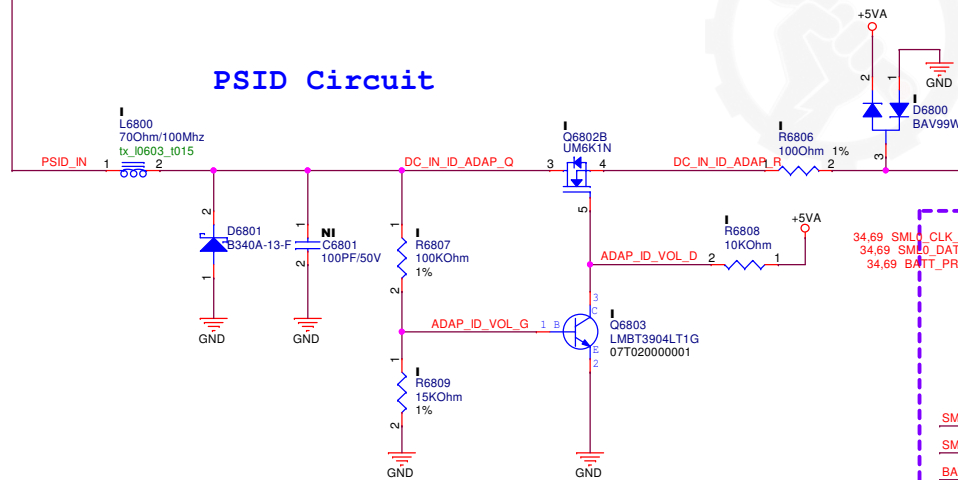


DC-IN connector

lin.cont= 12.31A
lin.peak=13.33A@4s

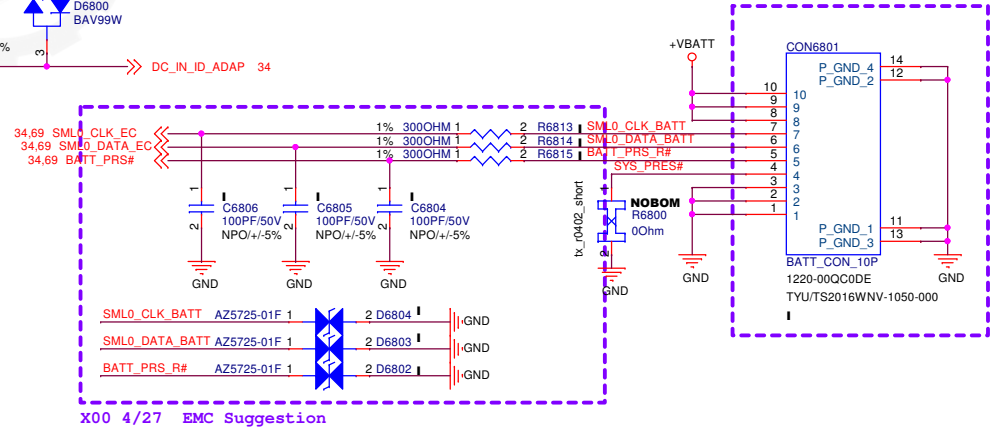


PSID Circuit

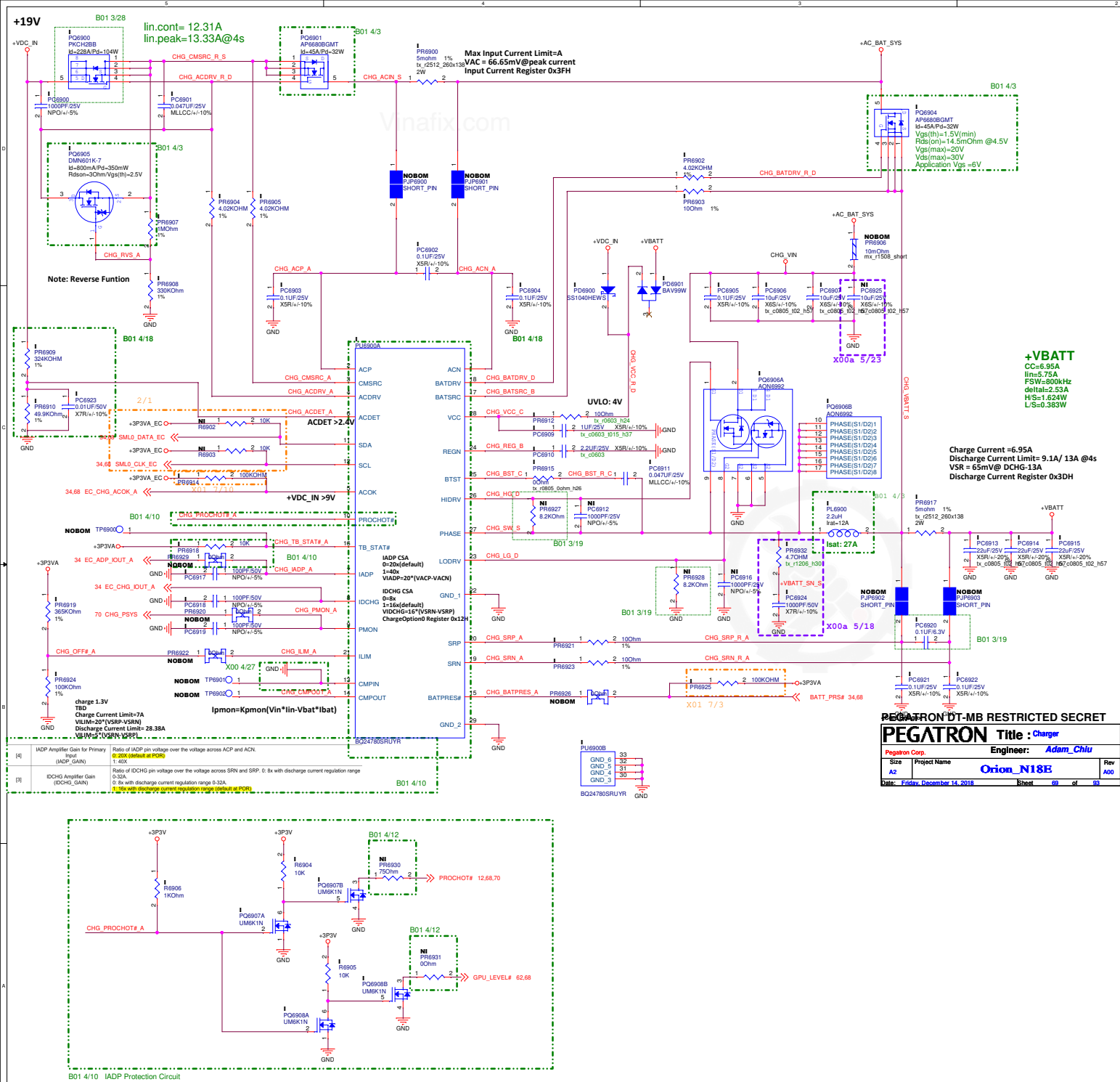


Battery Pack connector

X00a 5/22 changes to G/F type



B01 3/29 Remove Inverting Circuit



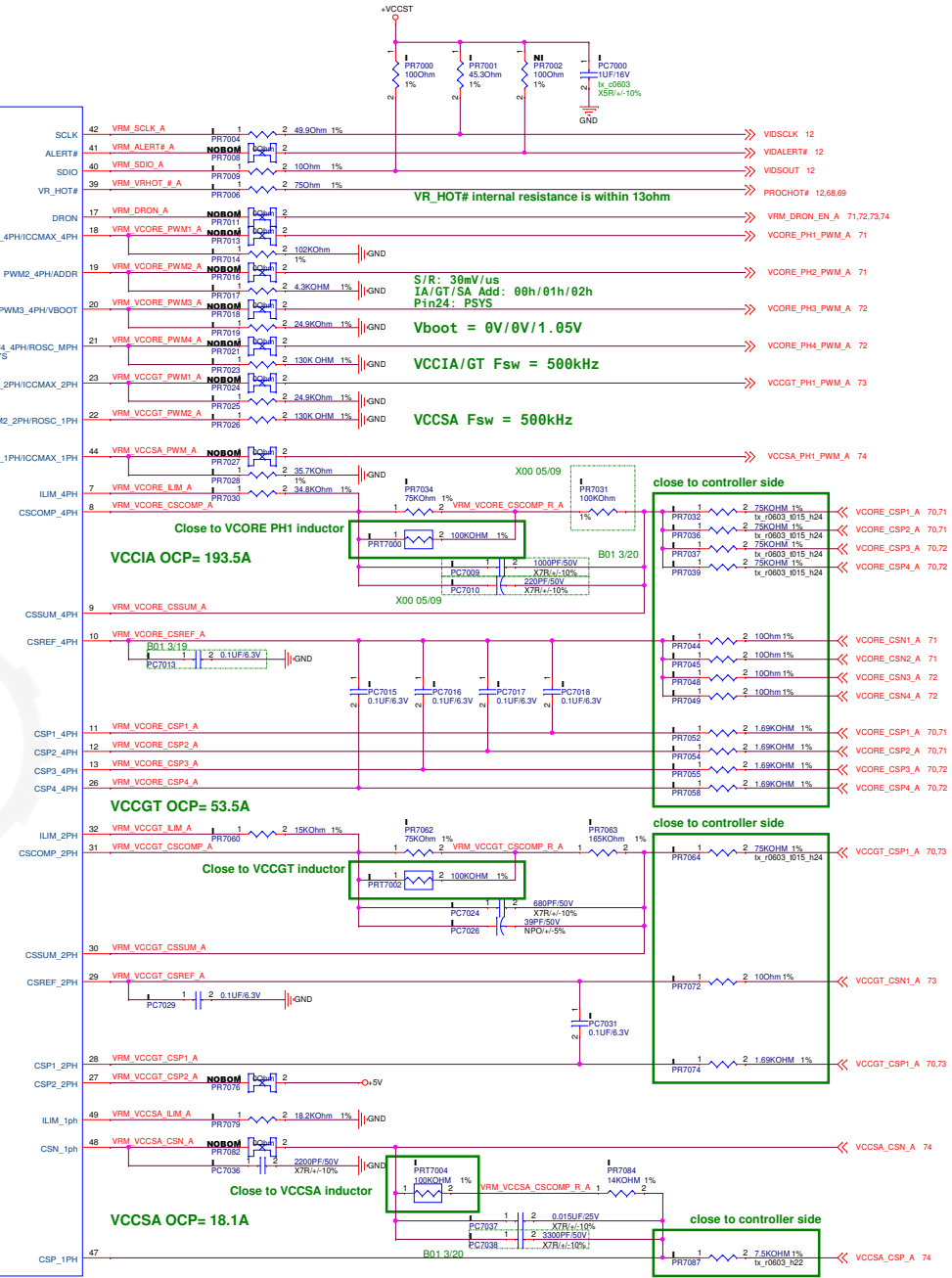
PEGATRON				Title : <i>Charger</i>
Pegatron Corp.		Engineer: <i>Adam_Chui</i>		
Size <i>A2</i>	Project Name <i>Orion_N18E</i>			Rev <i>A00</i>
Date: <i>Friday, December 14, 2018</i>		Sheet <i>69</i>	of <i>93</i>	

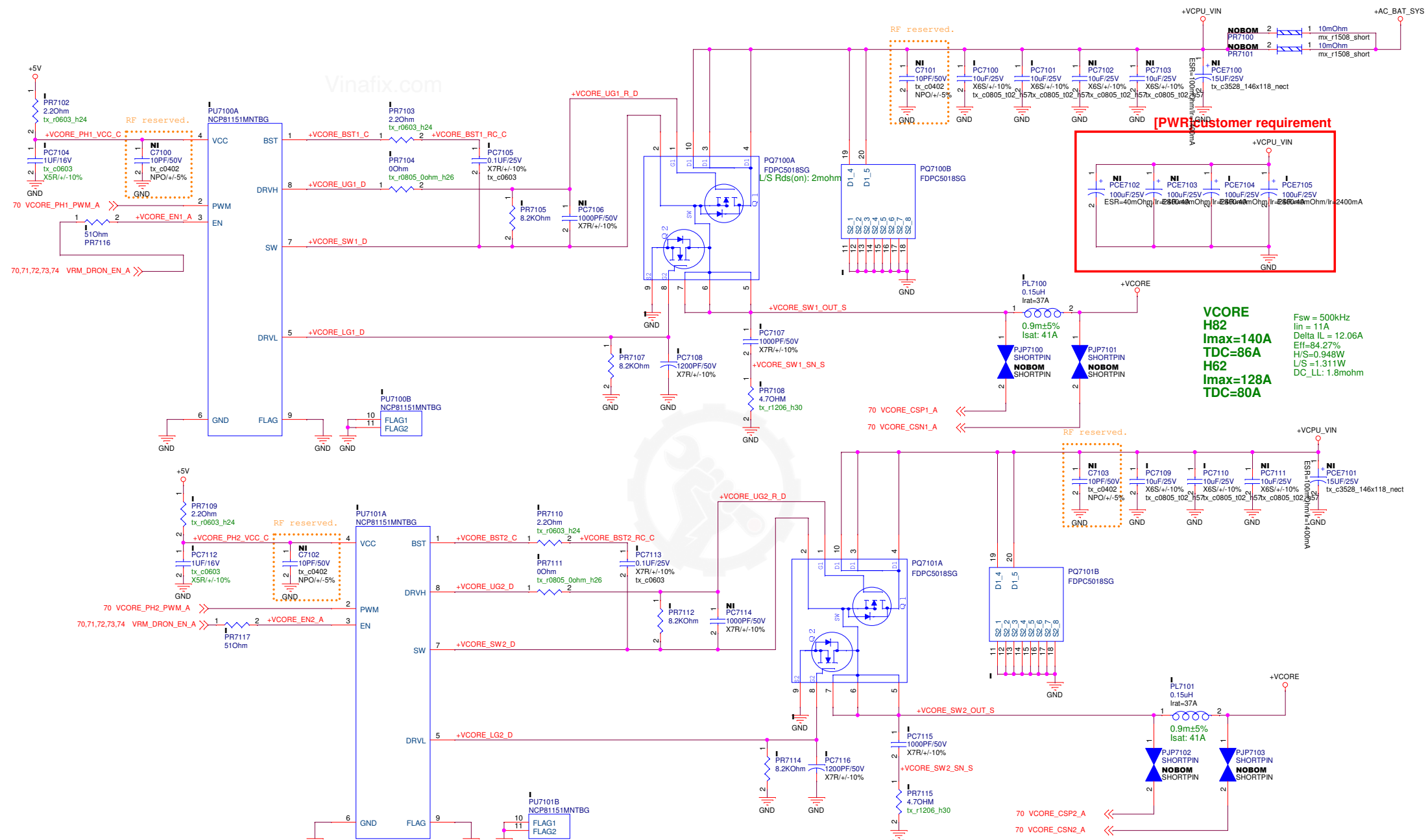
Close to VCORE PH1 input MLCC			
Psys max = 2V			
Close to VCORE PH1 inductor			
Close to VCCGT PH1 inductor			
Close to VCCSA inductor			
Bom difference between H62&H82			
Part Reference	SKU	H62	H82
PR7014 (ICCMAX)		102K	110K
PR7050 (IMON)		30.1K	28.7K

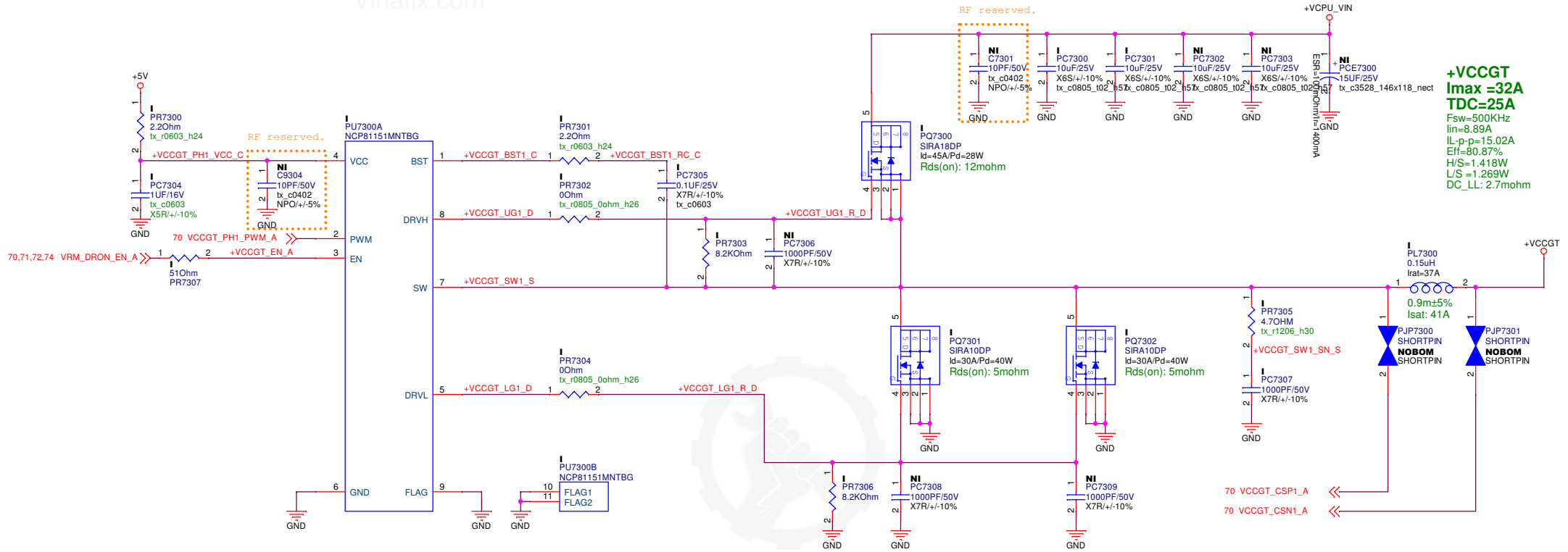
Owner	+VCORE OCP point	Low Limit	High Limit
PinDa	193.5A	128A	48.38A/Phase @L=0.09uH
Arisa	193.5A	128A	48.38A/Phase @L=0.09uH

Owner	+VCCGT OCP point	Low Limit	High Limit
PinDa	53.5A	32A	53.5A/Phase @L=0.08uH
Arisa	53.5A	32A	53.5A/Phase @L=0.08uH

Owner	+VCCSA OCP point	Low Limit	High Limit
PinDa	18.1A	11.1A	18.1A/Phase @L=0.42uH
Arisa	18.1A	11.1A	18.1A/Phase @L=0.42uH

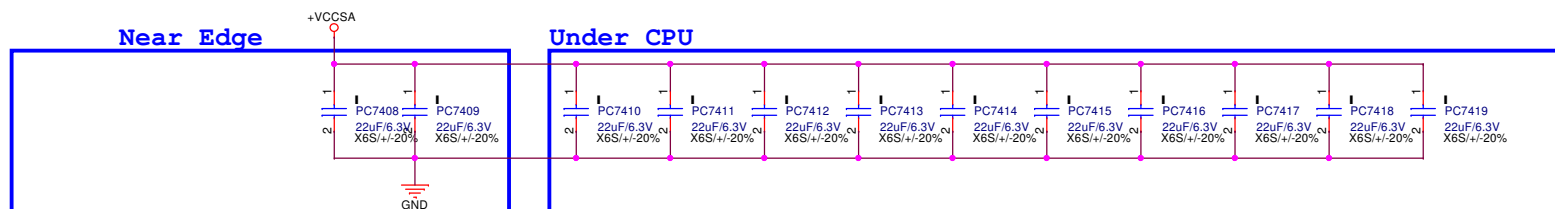
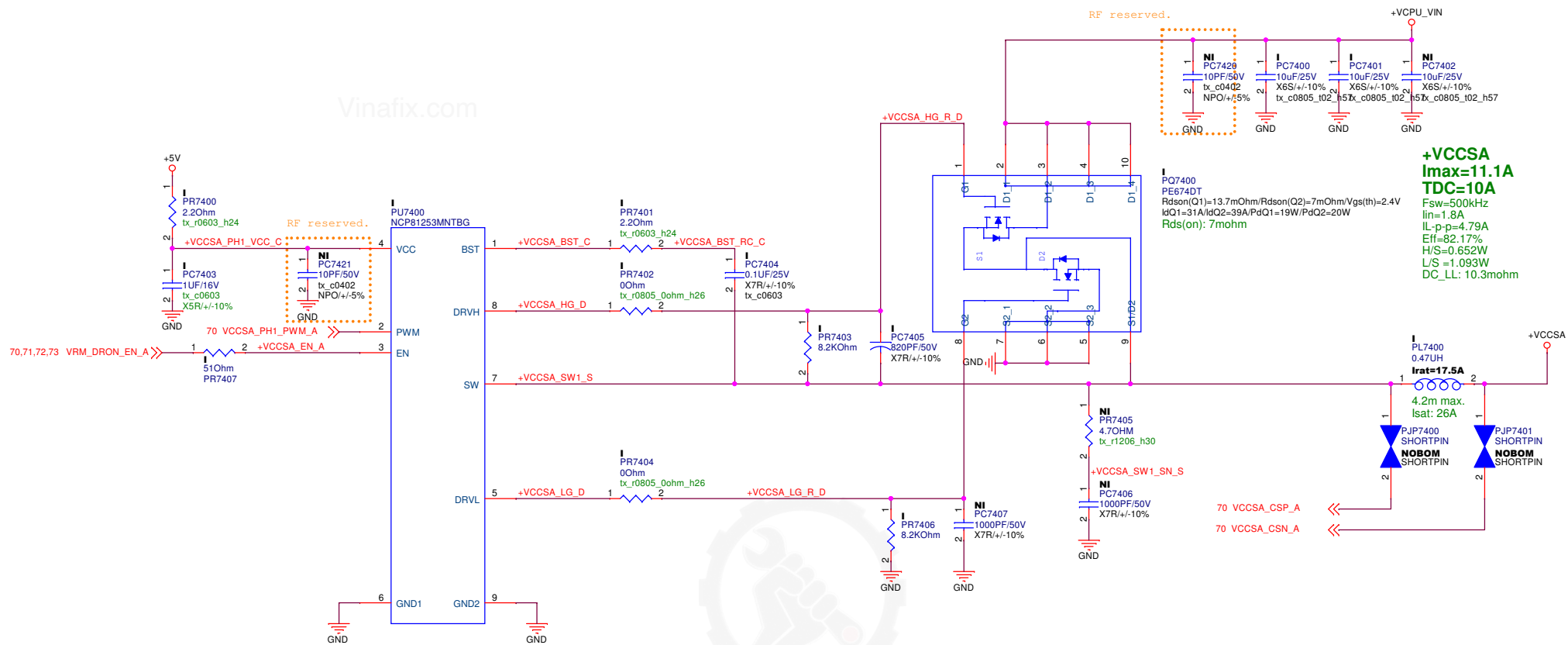






PEGATRON DT-MB RESTRICTED SECRET
 <Core Design>

PEGATRON		Title : VccGT Driver	
Pegatron Corp.		Engineer: Adam_Chui	
Size A3	Project Name Orion_N18E	Rev A00	
Date: Friday, December 14, 2018	Sheet 73 of 93		



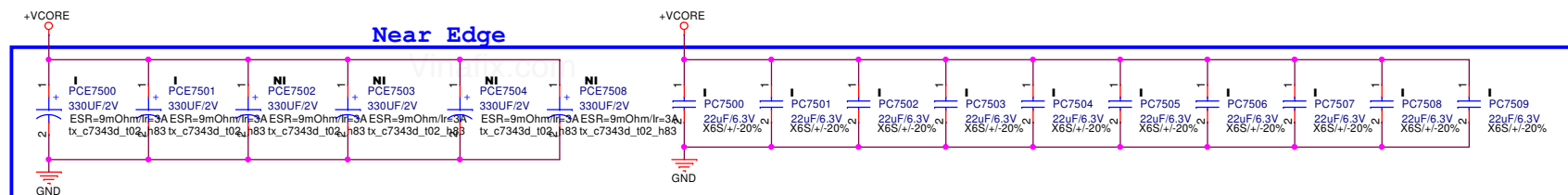
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **VccSa Driver**

Pegatron Corp. Engineer: **Adam Chiu**

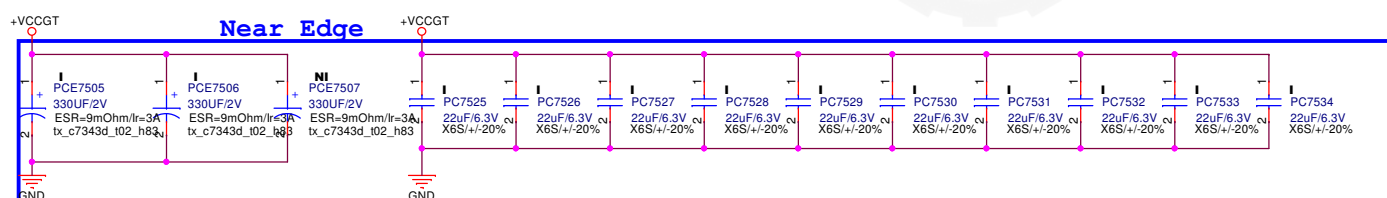
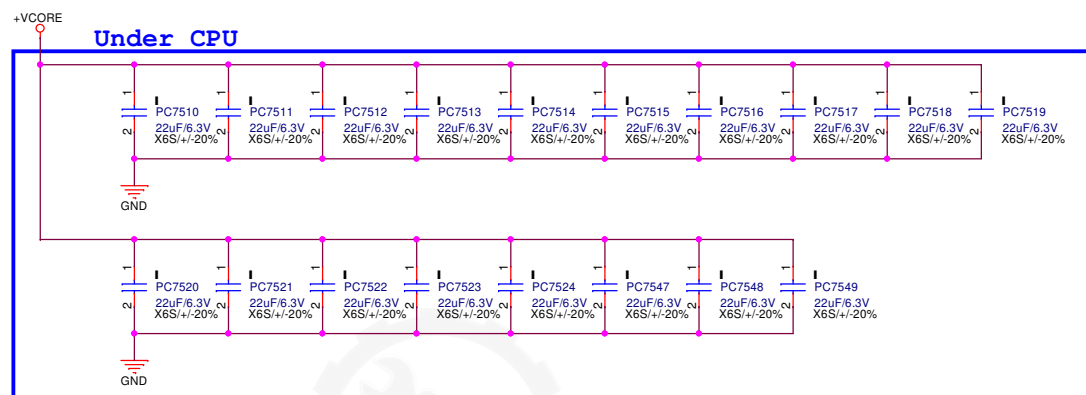
Size A3 Project Name **Orion_N18E** Rev A00

Date: Friday, December 14, 2018 Sheet 74 of 93



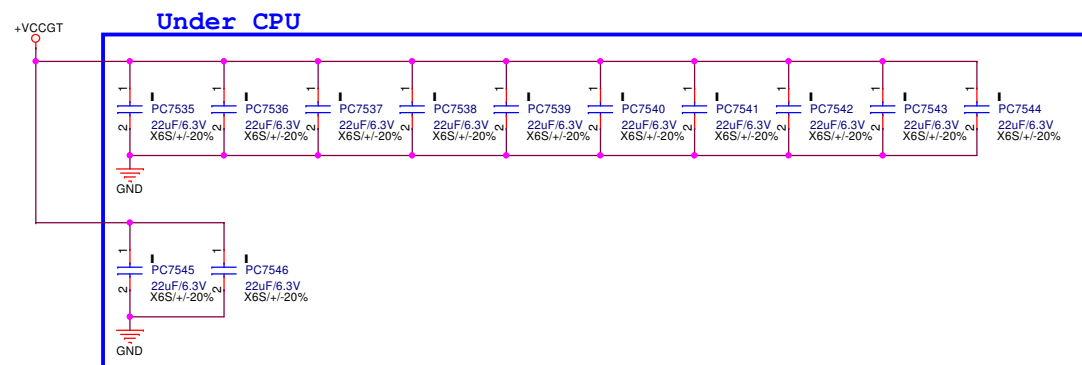
Vcore Output CAP

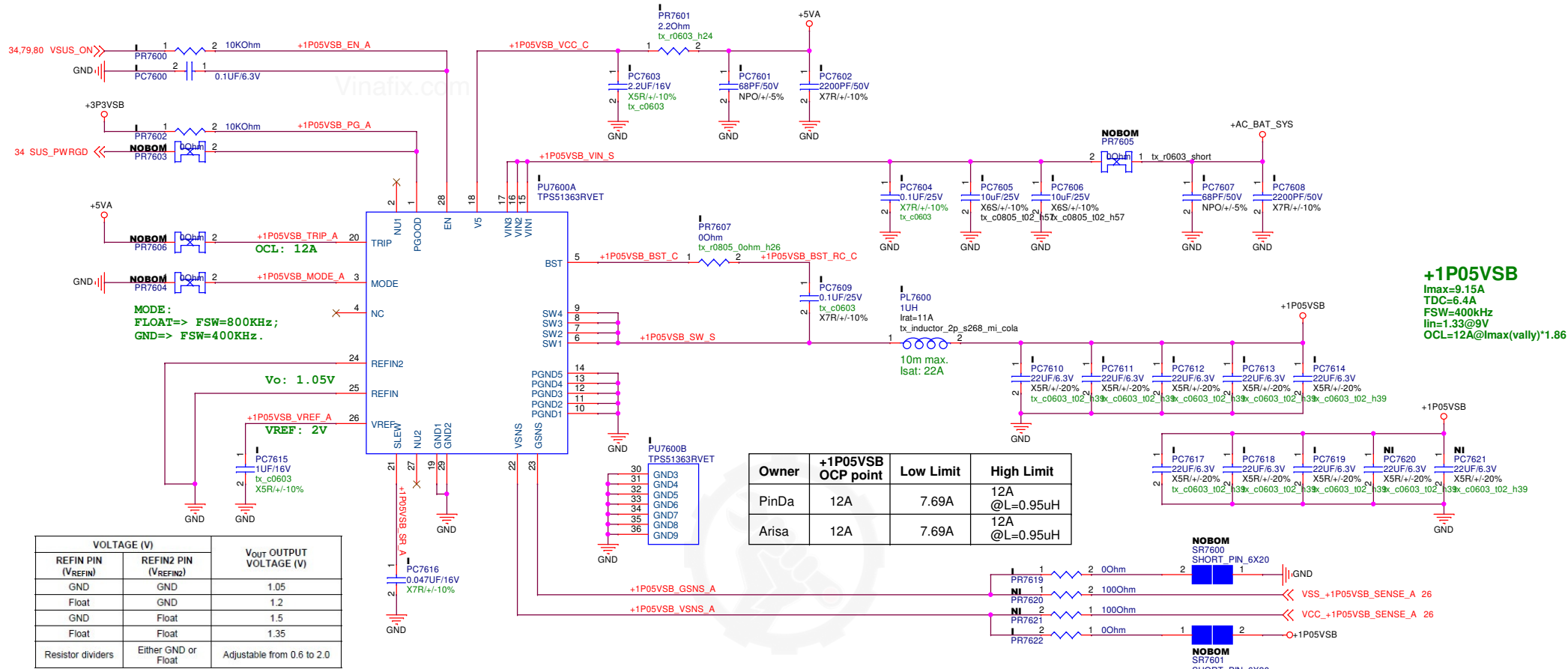
330uF/2V * 4 pcs
22uF/6.3V * 28pcs



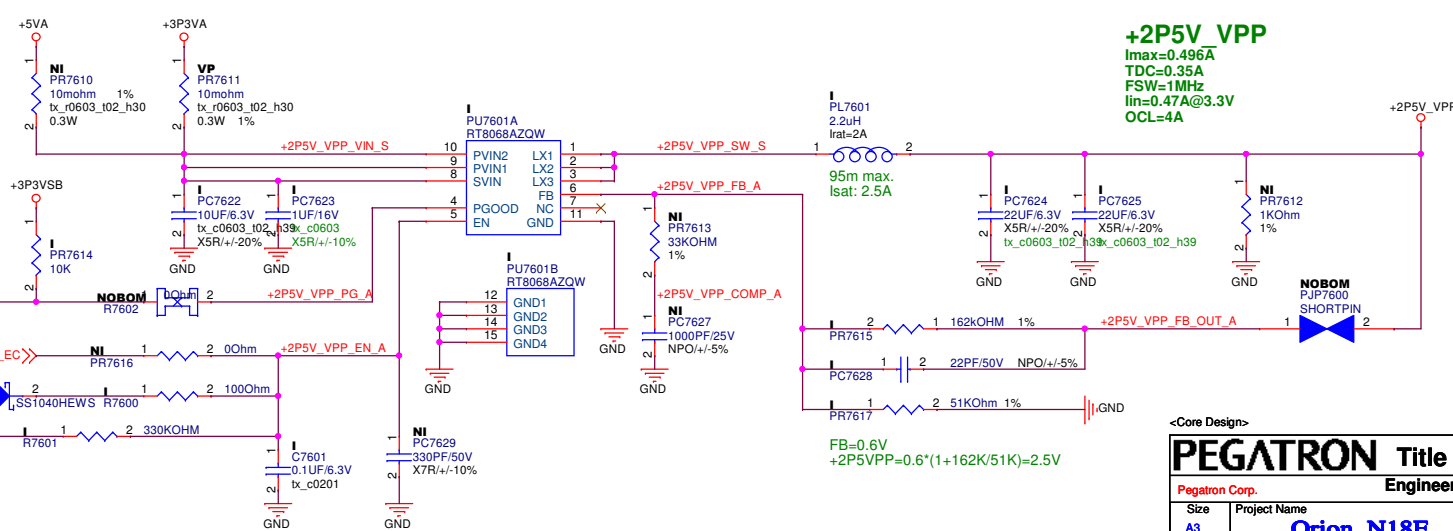
VCCGT Output CAP

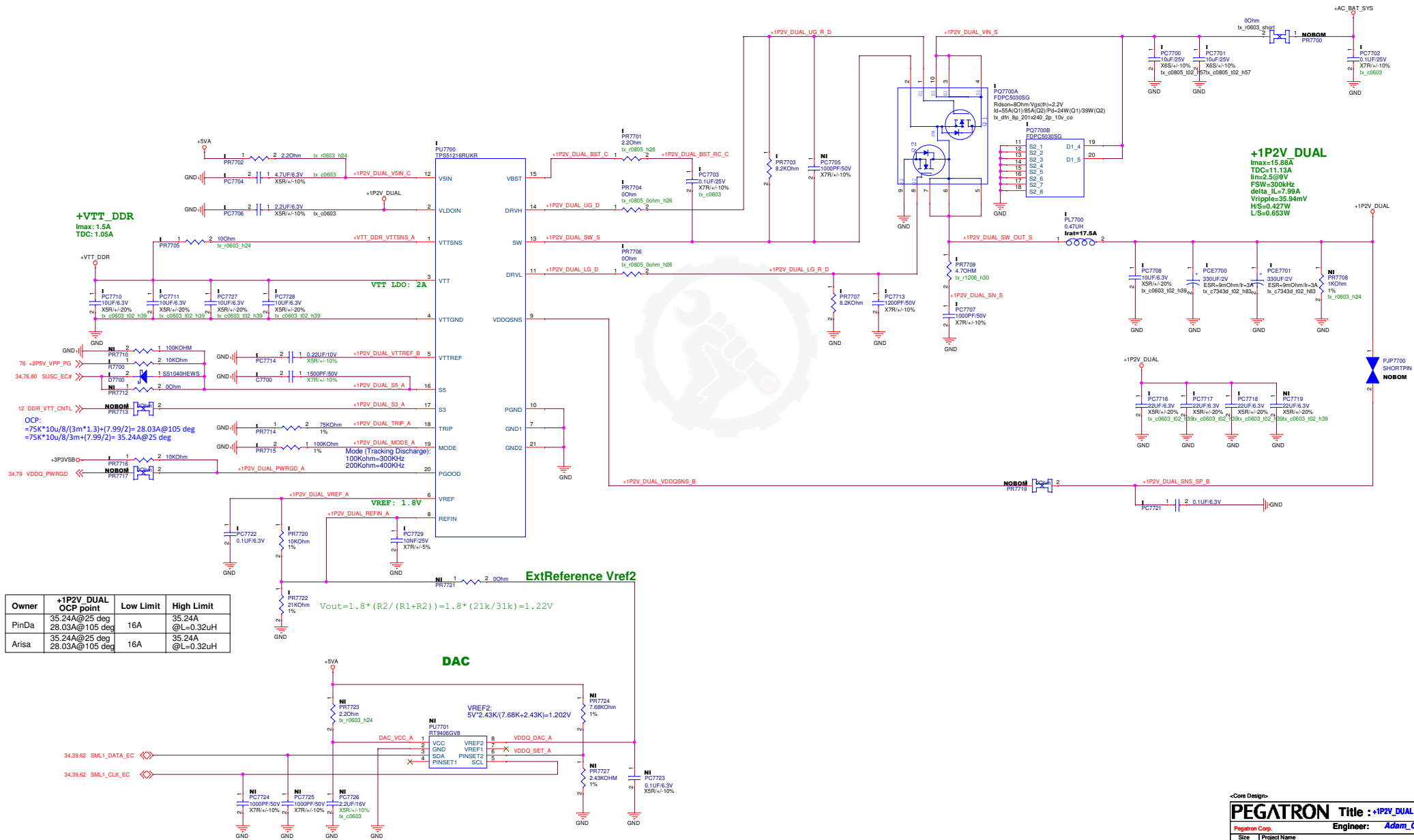
330uF/2V * 3
22uF/6.3V * 22 pcs

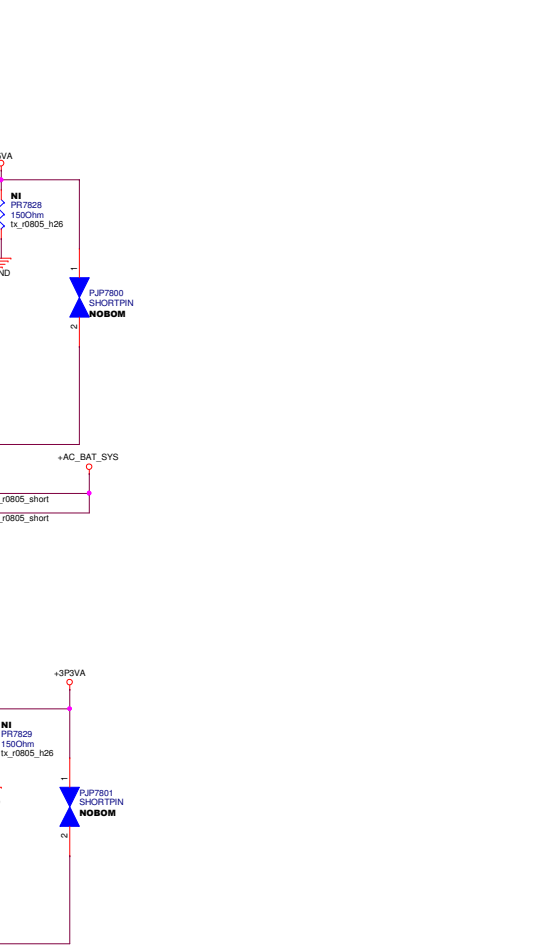
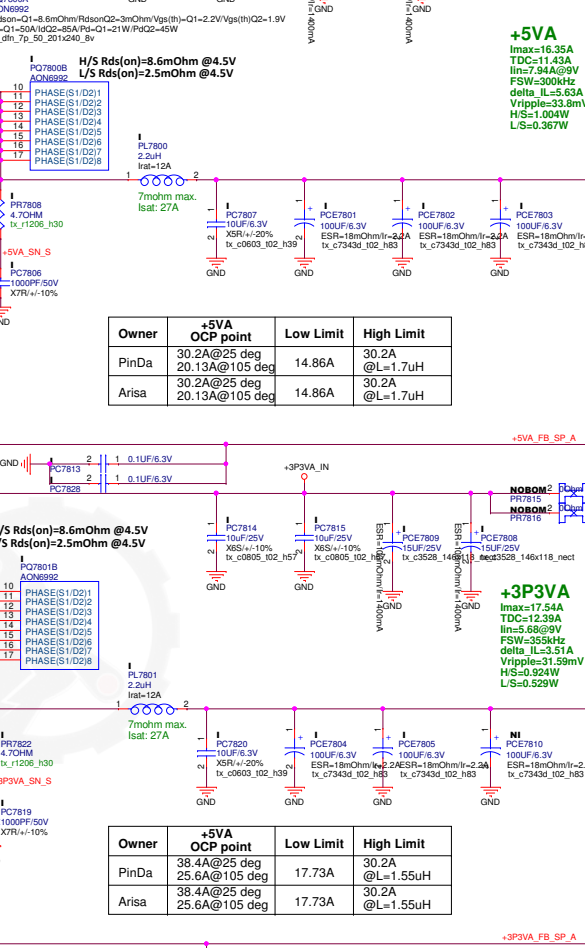
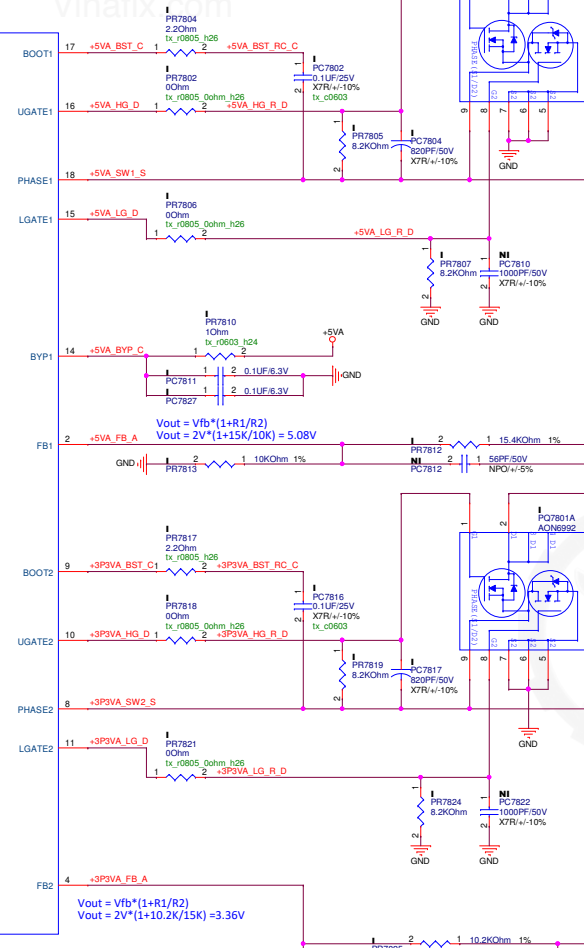
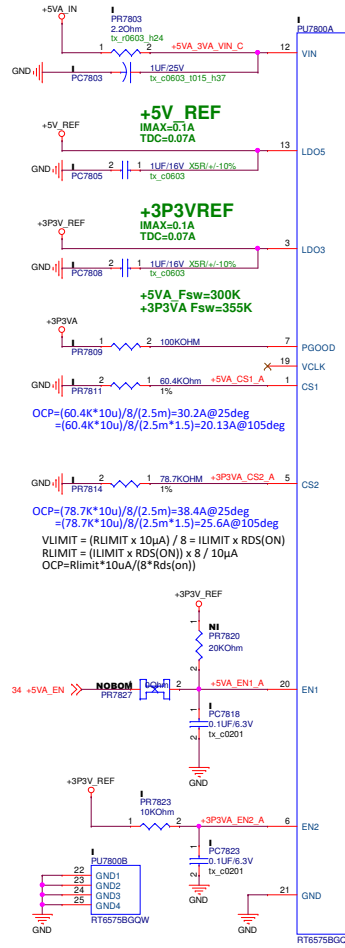




Owner	+2P5V_VPP OCP point	Low Limit	High Limit
PinDa	4A	0.34A	4A @L=1.1uH
Arisa	4A	0.34A	4A @L=1.1uH

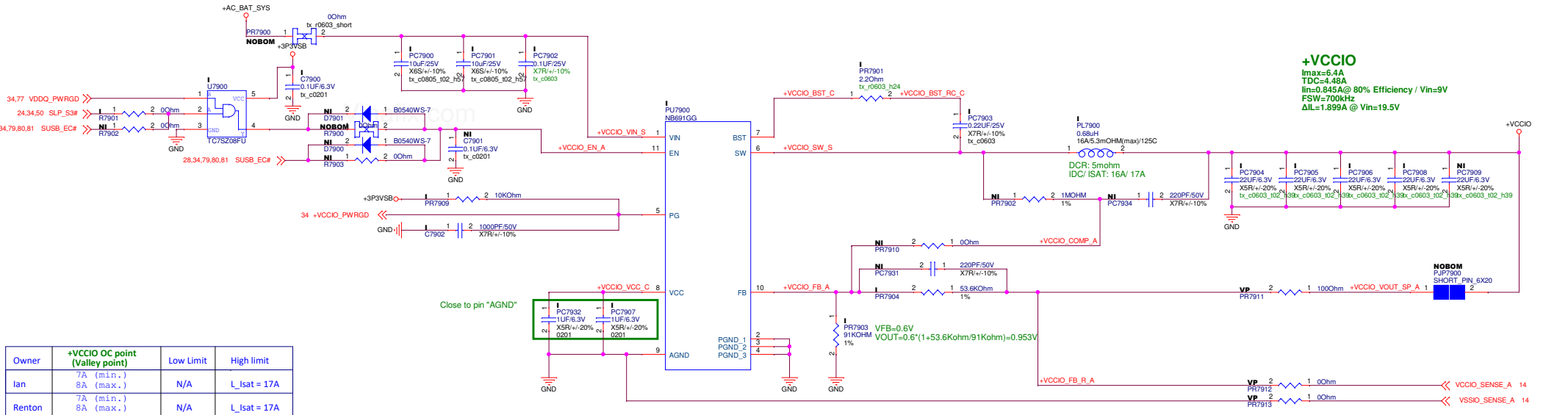




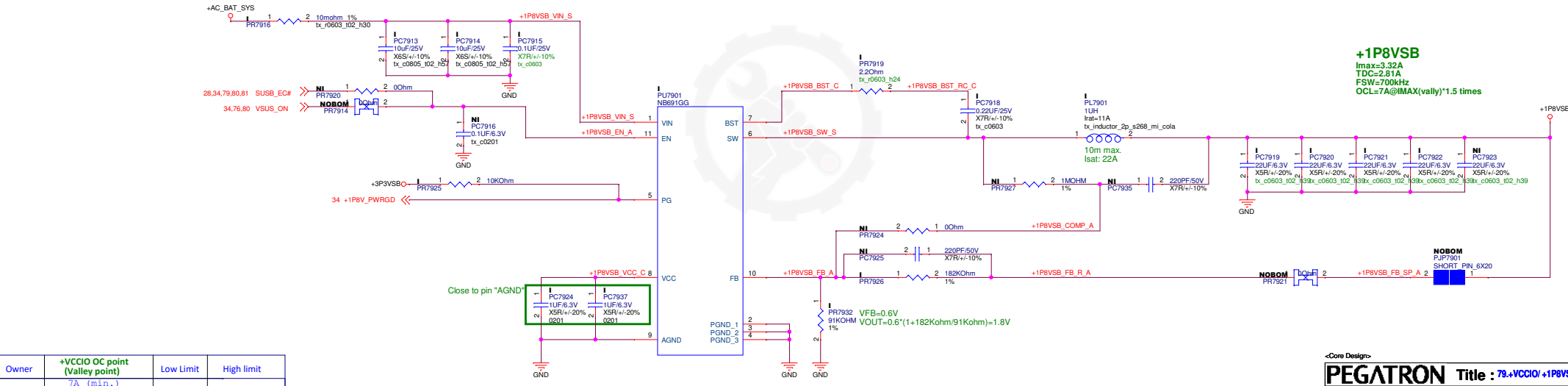


Owner	+5VA OCP point	Low Limit	High Limit
PinDa	30.2A@25 deg 20.13A@105 deg	14.86A	30.2A @L=1.7uH
Arisa	30.2A@25 deg 20.13A@105 deg	14.86A	30.2A @L=1.7uH

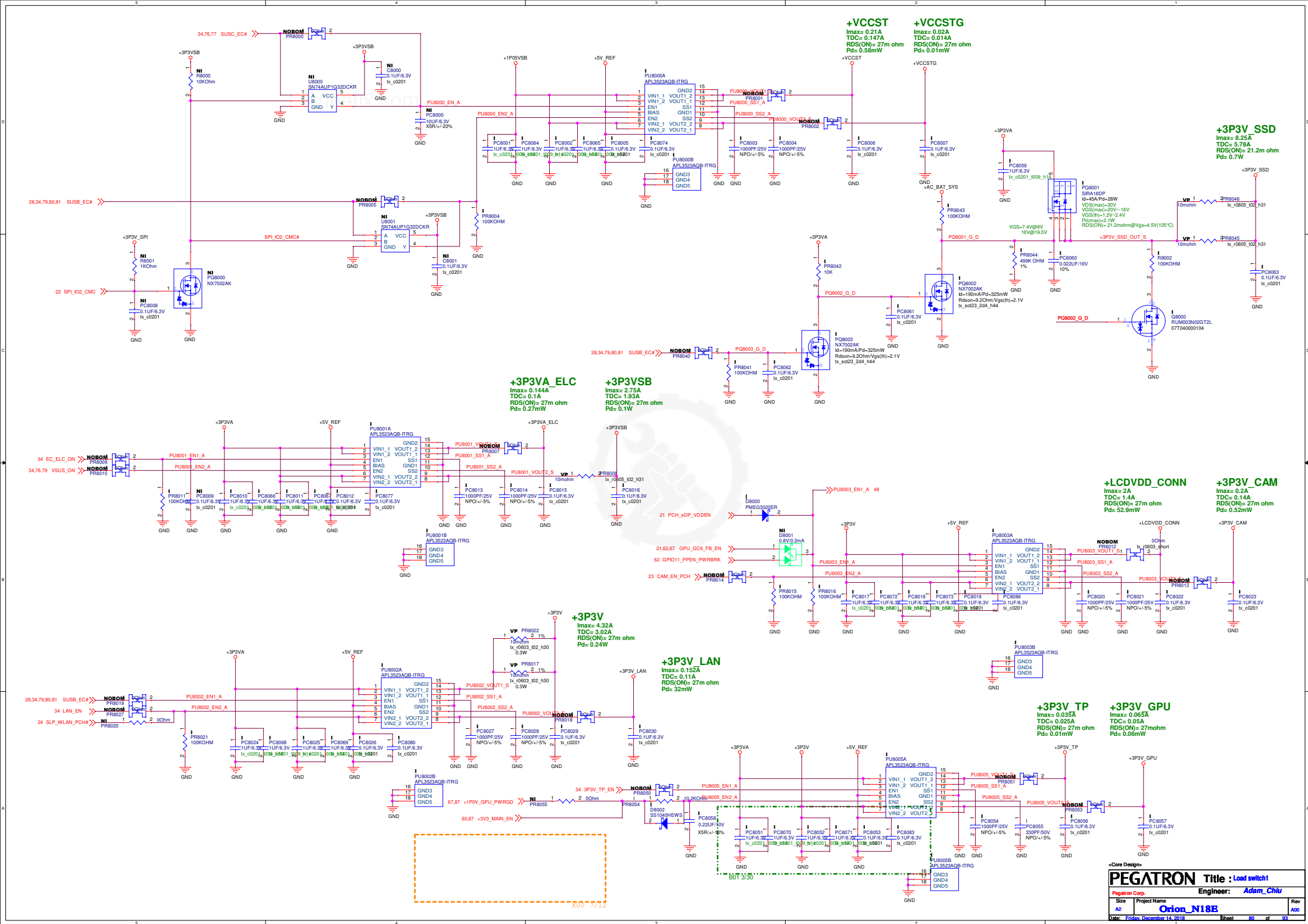
Owner	+5VA OCP point	Low Limit	High Limit
PinDa	38.4A@25 deg 25.6A@105 deg	17.73A	30.2A @L=1.55uH
Arisa	38.4A@25 deg 25.6A@105 deg	17.73A	30.2A @L=1.55uH

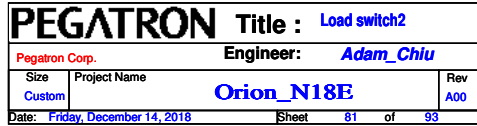


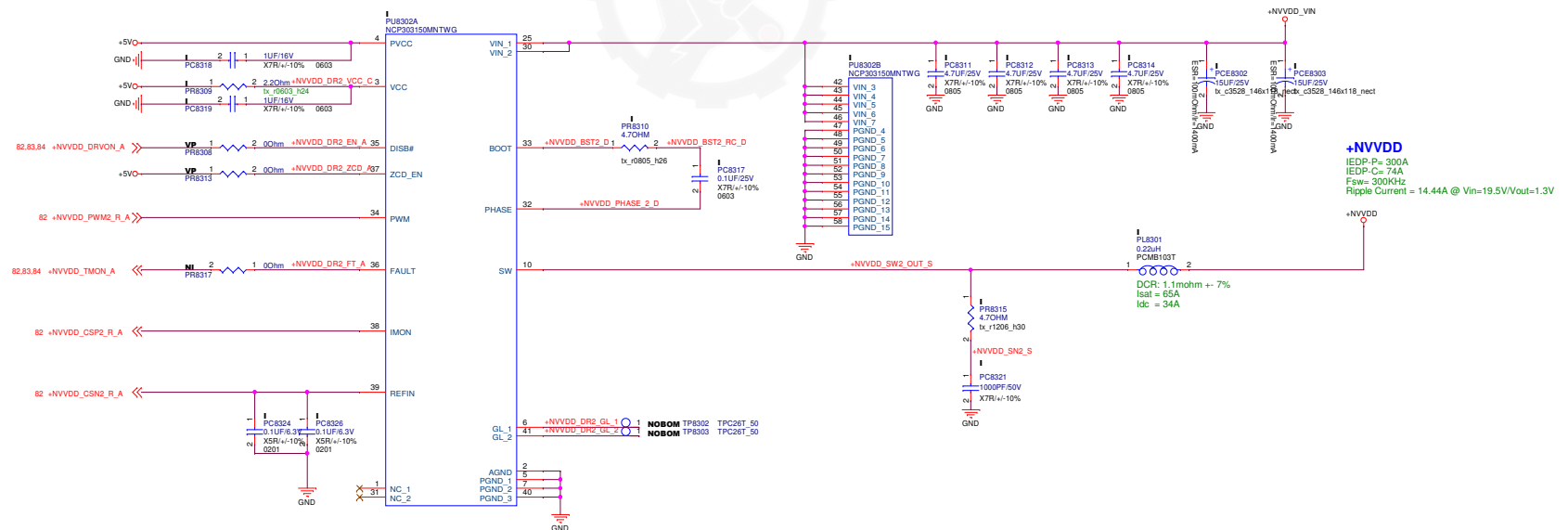
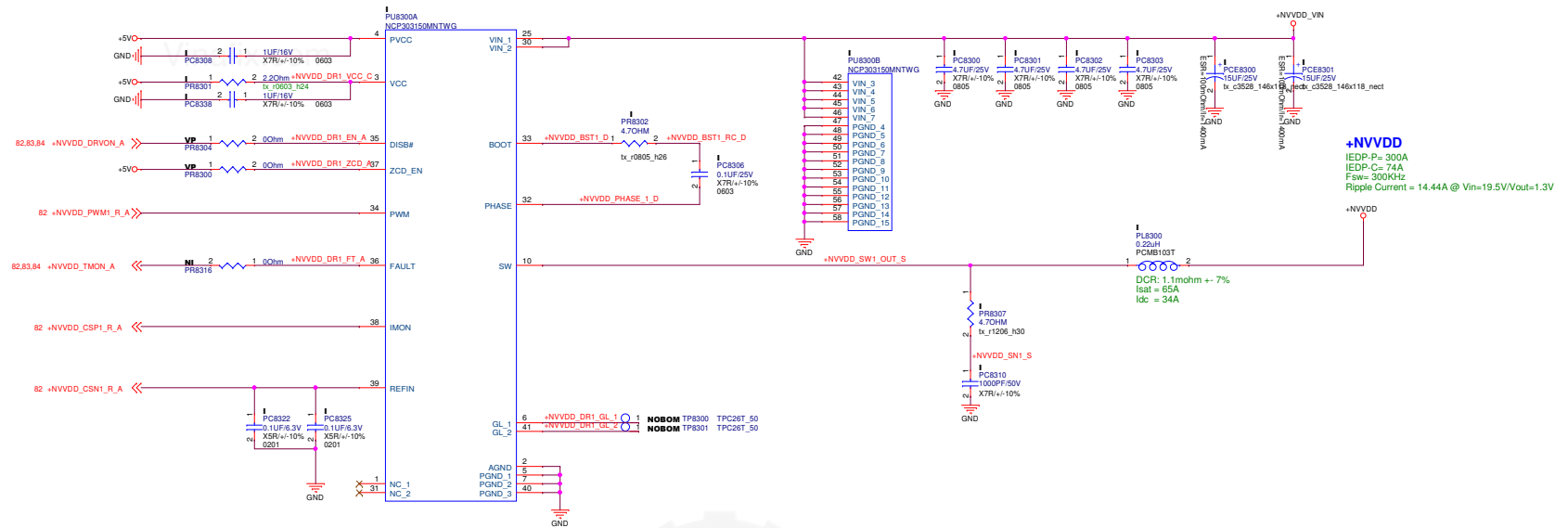
Owner	+VCCIO OC point (Valley point)	Low Limit	High limit
Ian	7A (min.) 8A (max.)	N/A	L_Isat = 17A
Renton	7A (min.) 8A (max.)	N/A	L_Isat = 17A



Owner	+1P8VSB OC point (Valley point)	Low Limit	High limit
Ian	7A (min.) 8A (max.)	N/A	L_Isat = 22A
Renton	7A (min.) 8A (max.)	N/A	L_Isat = 22A



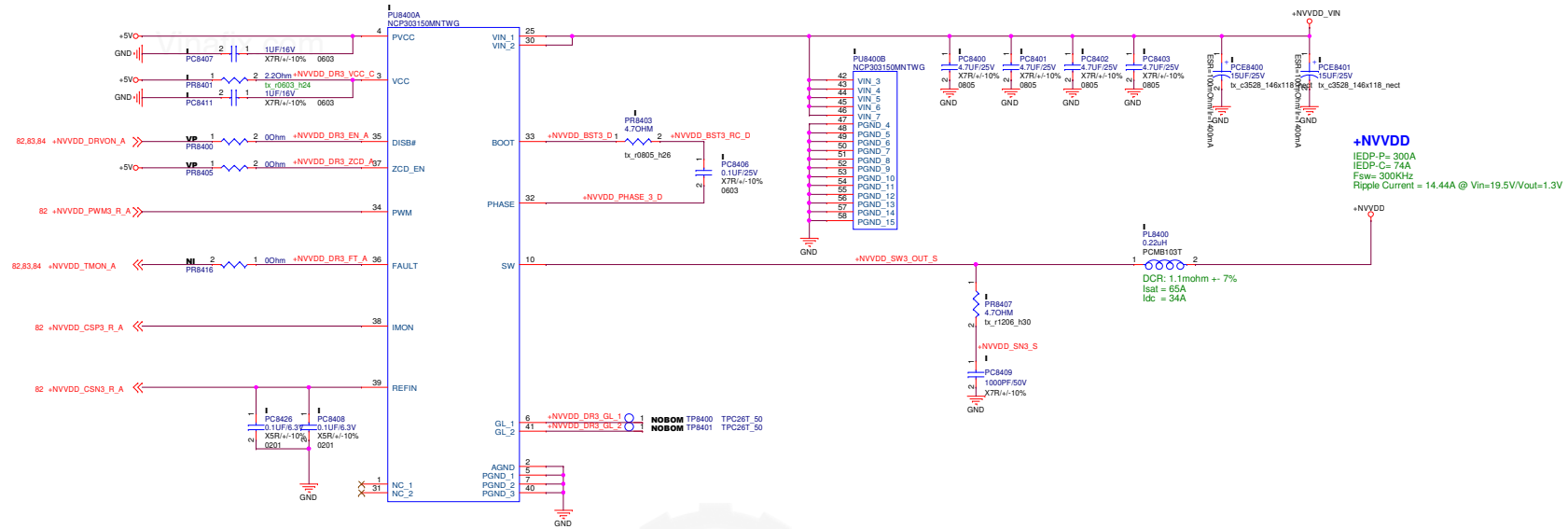




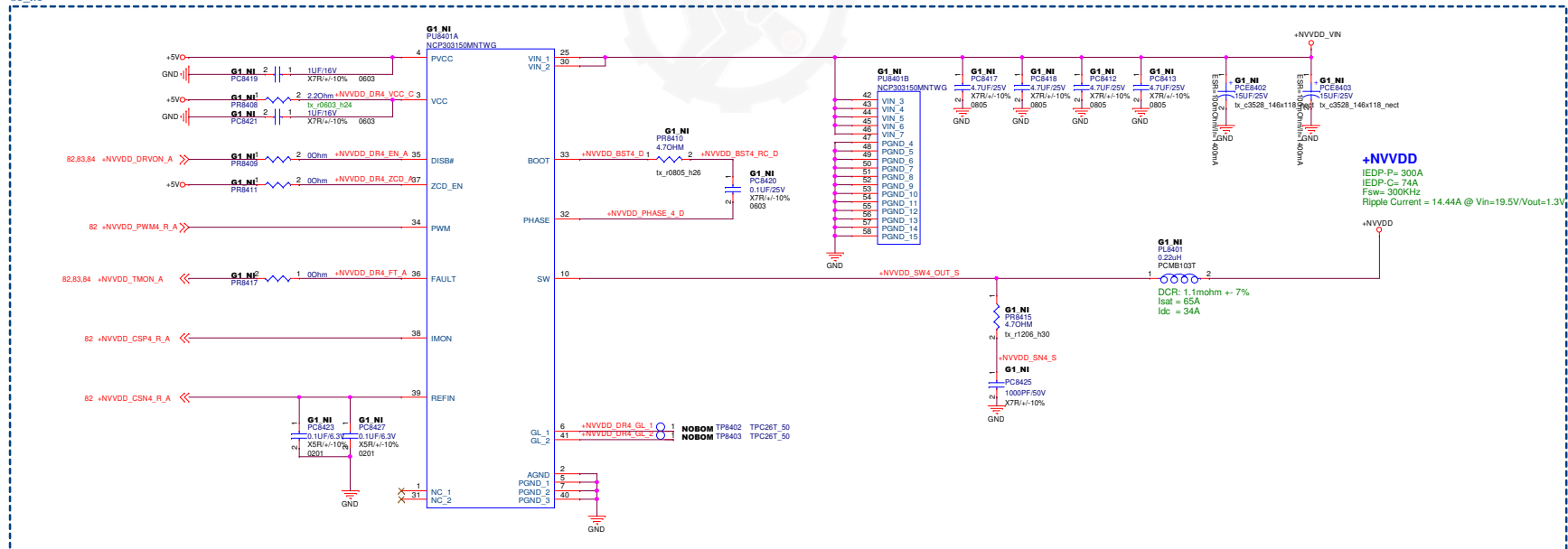
PEGATRON DT-MB RESTRICTED SECRET

Core Design

PEGATRON		Title : NVVDD Driver Cap	
Pegatron Corp.		Engineer:	
Size	Project Name	Rev	Rev
A2	Orion N18E	A00	A00
Date: Friday, December 14, 2018		Sheet	63 of 94



X01 0912
 G1_NI



<Core Design>

PEGATRON Title : +NVDD Drive-2			
Pegatron Corp.		Engineer: Adam Chiu	
Size	Project Name	Rev	
A2	Orion_N18E	A00	
Date: Friday, December 14, 2018	Sheet	84	of 94

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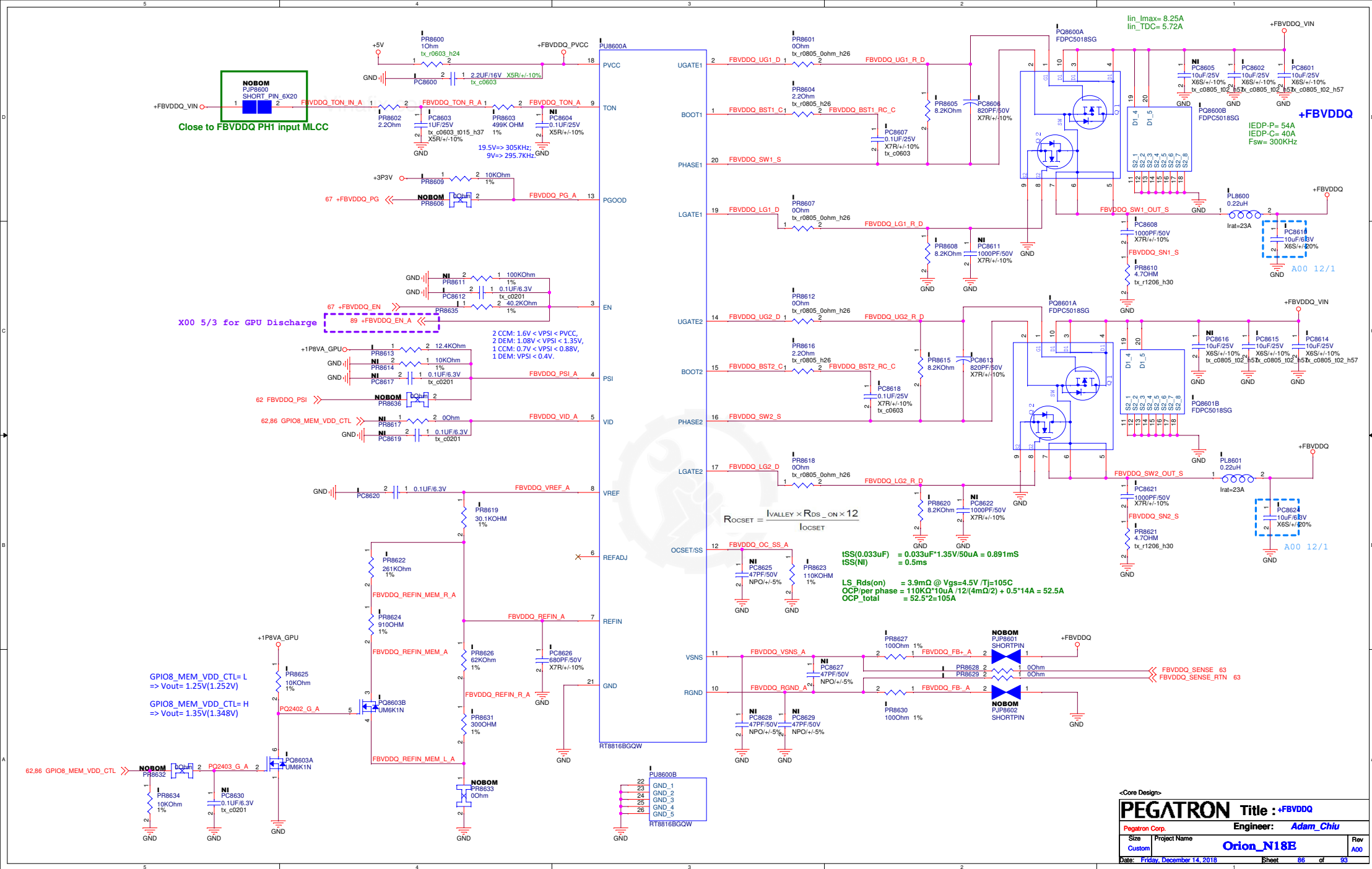


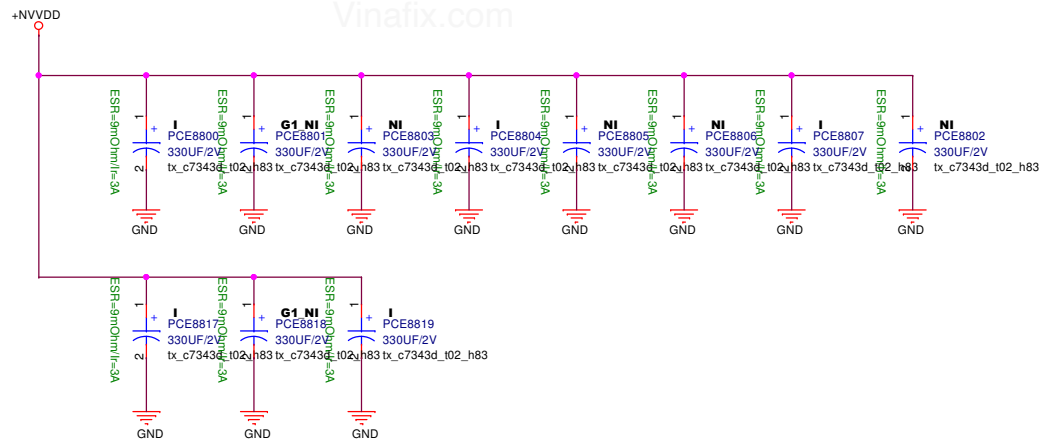
+NVVDDS(merge to NVVDD)

IEDP-P= 53.7A
IEDP-C= 27A
Fsw= 305KHz
Delta I= 15.68A
Vripple= 35.29mV
H/S= 0.546W
L/S= 0.7W

<Core Design>

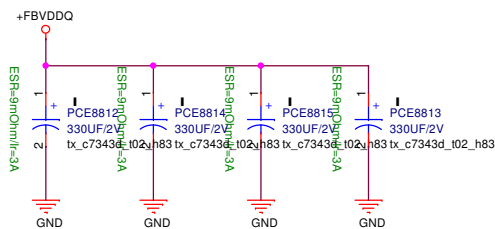
PEGATRON		Title : xxxxxx	
Pegatron Corp.		Engineer: Adam_Chlu	
Size	Project Name	Rev	
A3	Orion_N18E	A00	
Date: Friday, December 14, 2018		Sheet	85 of 93





+NVVDD Output CAP

G3
330uF/2V * 7 pcs
G2
330uF/2V * 5 pcs



+FBVDDQ Output CAP

330uF/2V * 4 pcs

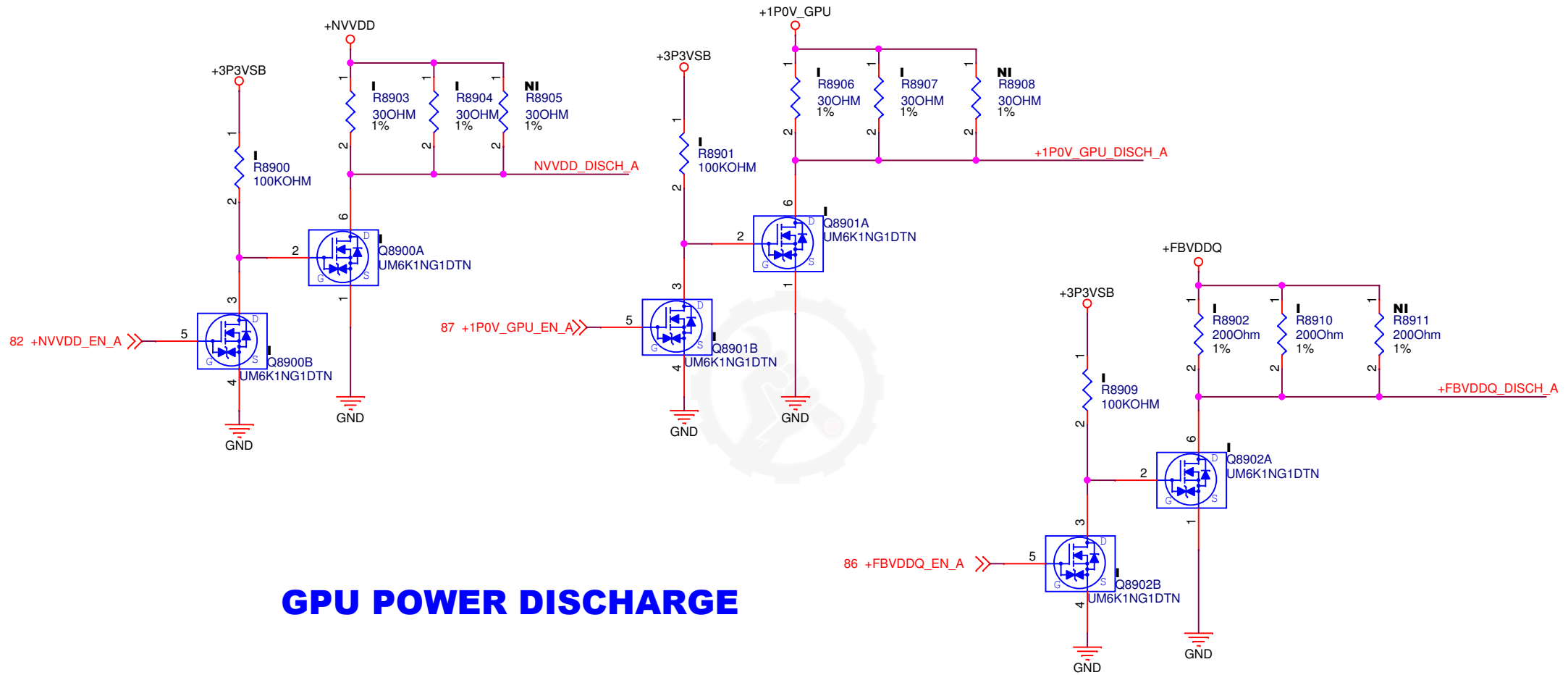
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PEGATRON Title : GPU_POWER_CAP

Pegatron Corp. Engineer: Adam Chiu

Size A3	Project Name Orion_N18E	Rev A00
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GPU POWER DISCHARGE

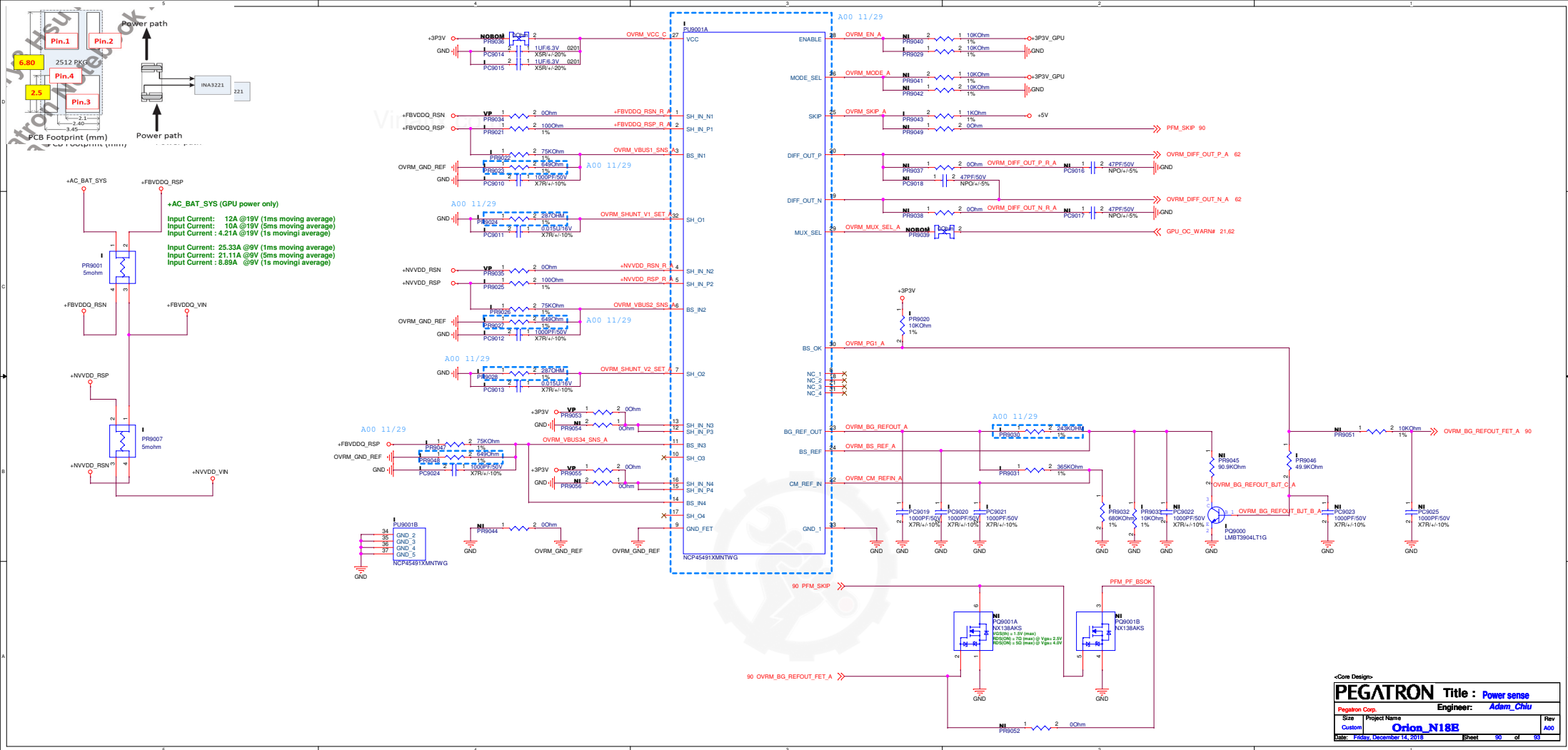
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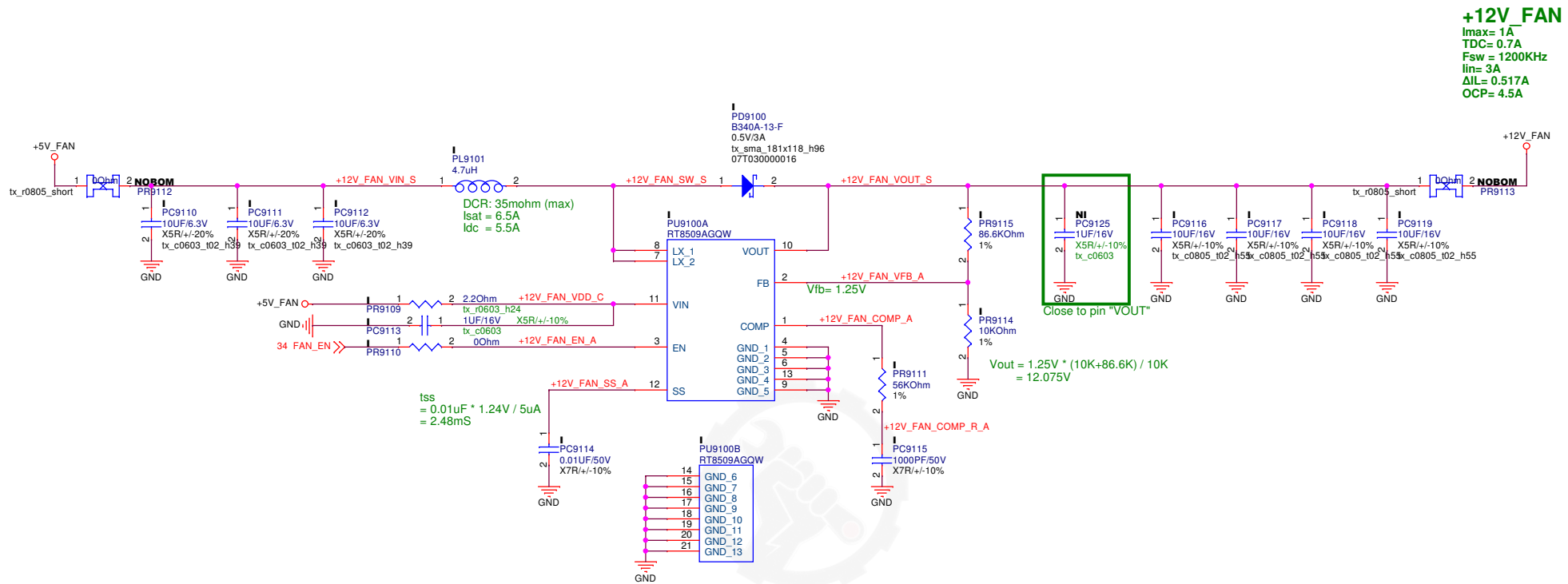
PEGATRON Title : GPU POWER DISCHARGE

Pegatron Corp. Engineer: Adam Chiu

Size	Project Name	Rev
A4	Orion_N18E	A00

Date: Friday, December 14, 2018 Sheet 89 of 94





<Core Design>

PEGATRON		Title : +12V_FAN	
Pegatron Corp.		Engineer: Adam_Chlu	
Size A3	Project Name	Orion_N18E	Rev A00
Date: Friday, December 14, 2018		Sheet	91 of 93

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<Core Design>

PEGATRON		Title : xxxxxx	
Pegatron Corp.		Engineer: Adam_ChIU	
Size A4	Project Name Orion_N18E		Rev A00
Date: Friday, December 14, 2018		Sheet	92 of 93