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## MB



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Title: **Index Page**

| Size | Document Number | Rev |
|---|---|---|
| Custom | TPN-F101/TPN-F102 Montevina | 0.1 |

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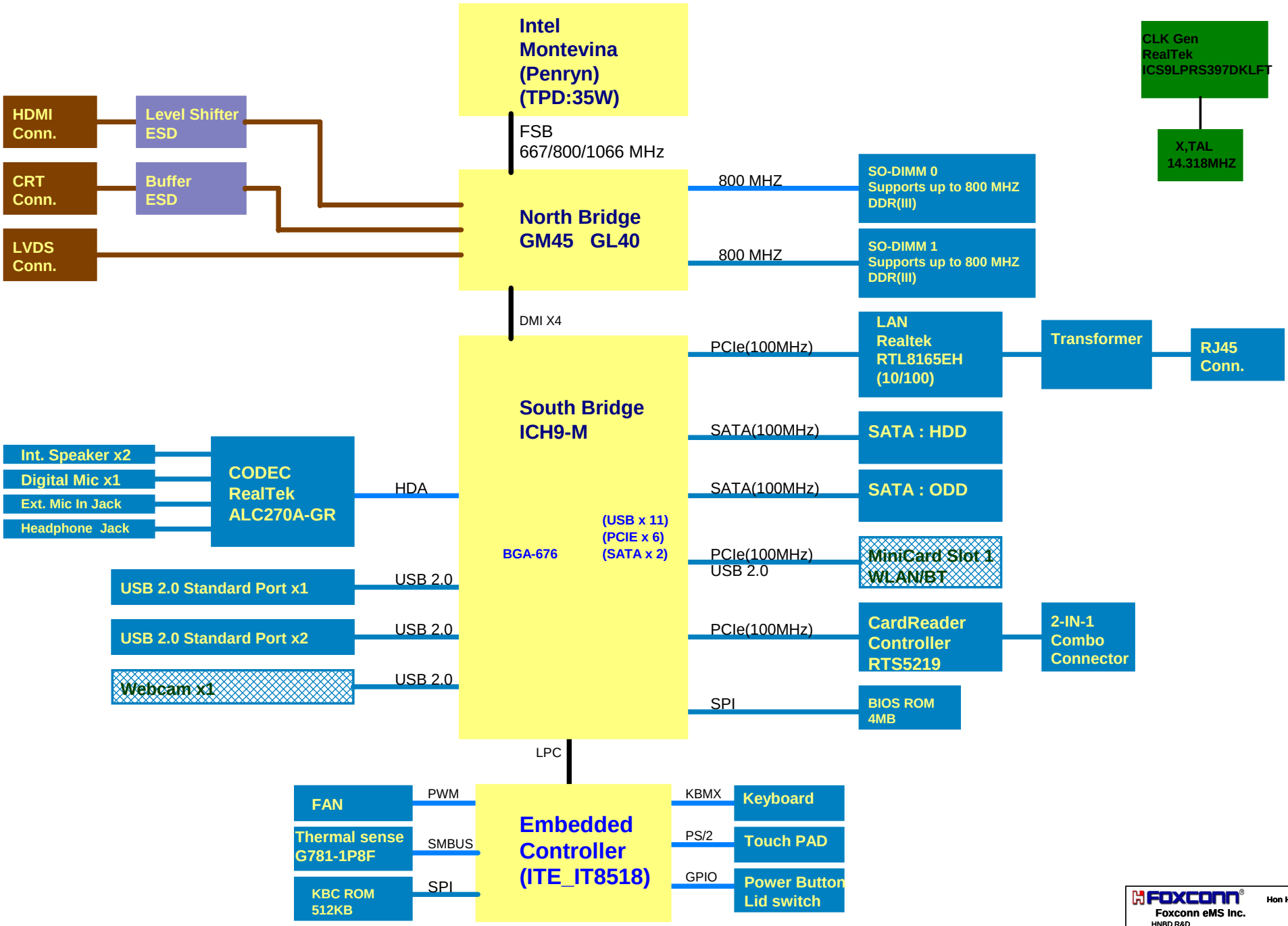


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Title: SYSTEM BLOCK DIAGRAM

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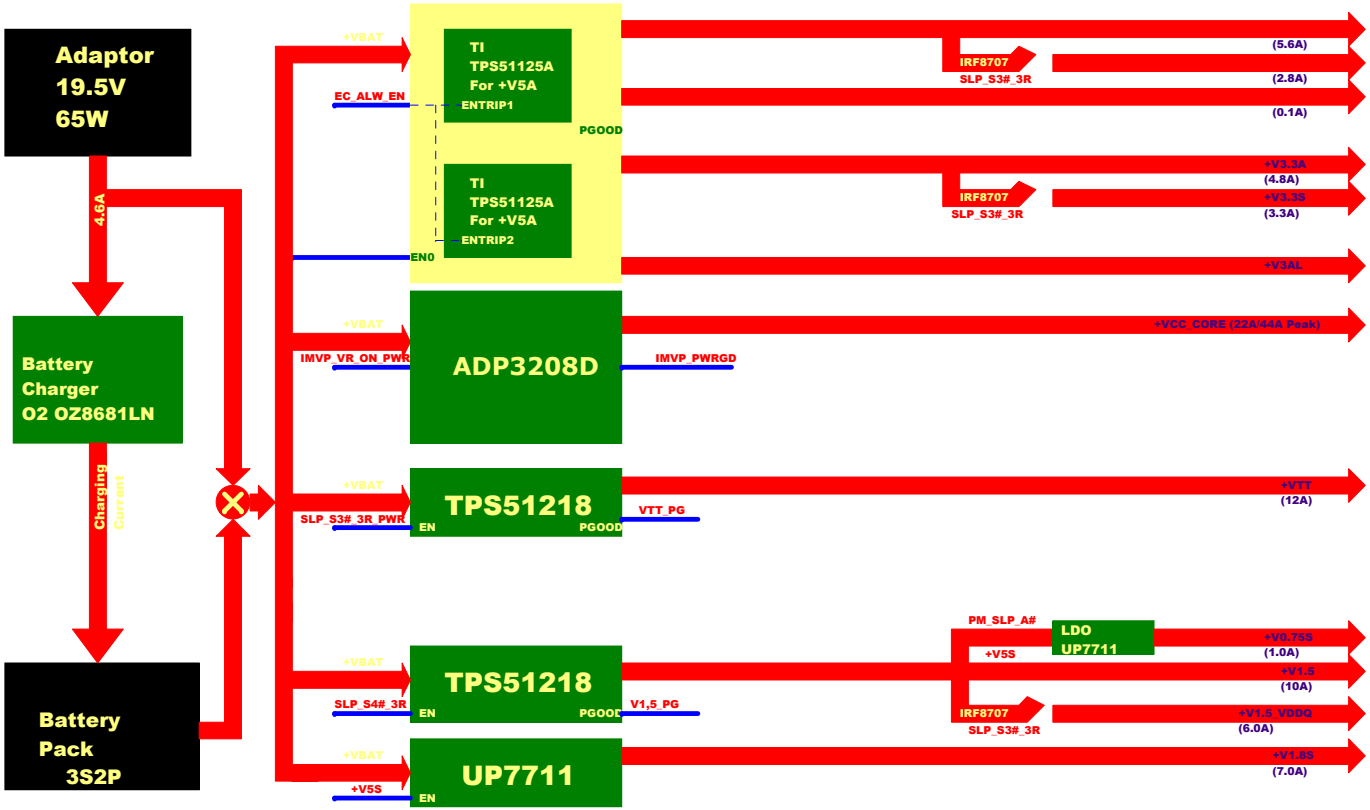
# POWER MAP





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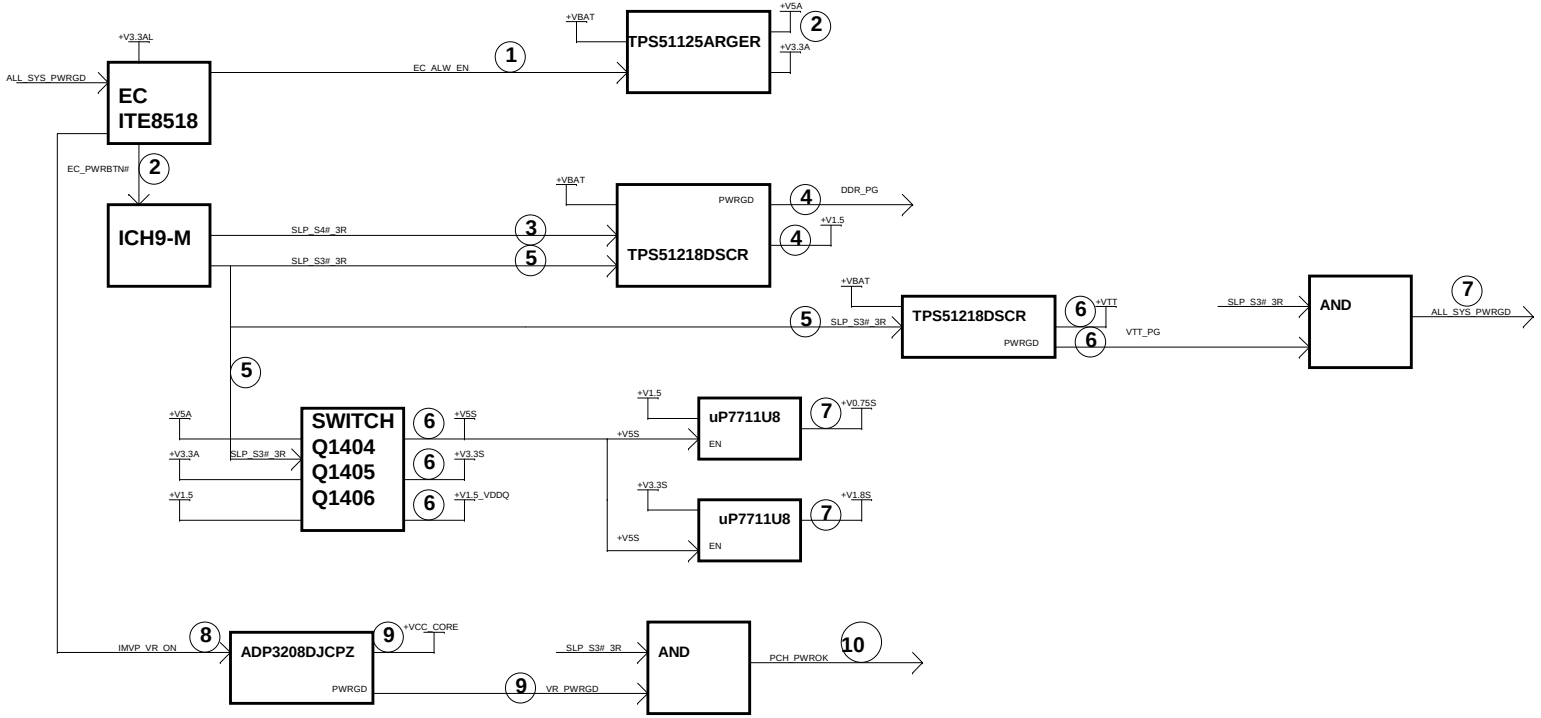


**Power on Sequence required:**

**GL40:**
**1, +V3.3A ramp before +V1.1A**
**2, +V3.3S ramp before +V1.8S**
**3, +V1.8S ramp before +V1.1S**
**4, +V3.3S ramp before +V1.1S**

**ICH9-M:**
**1, 0 <(+V3.3S) - (+V1.8S) < 2.1**
**2, +V1.8S ramp before +V1.1S**
**3. +V1.1S ramp before VCC_NB**


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Title: **POWER SEQUENCY DIAGRAM**

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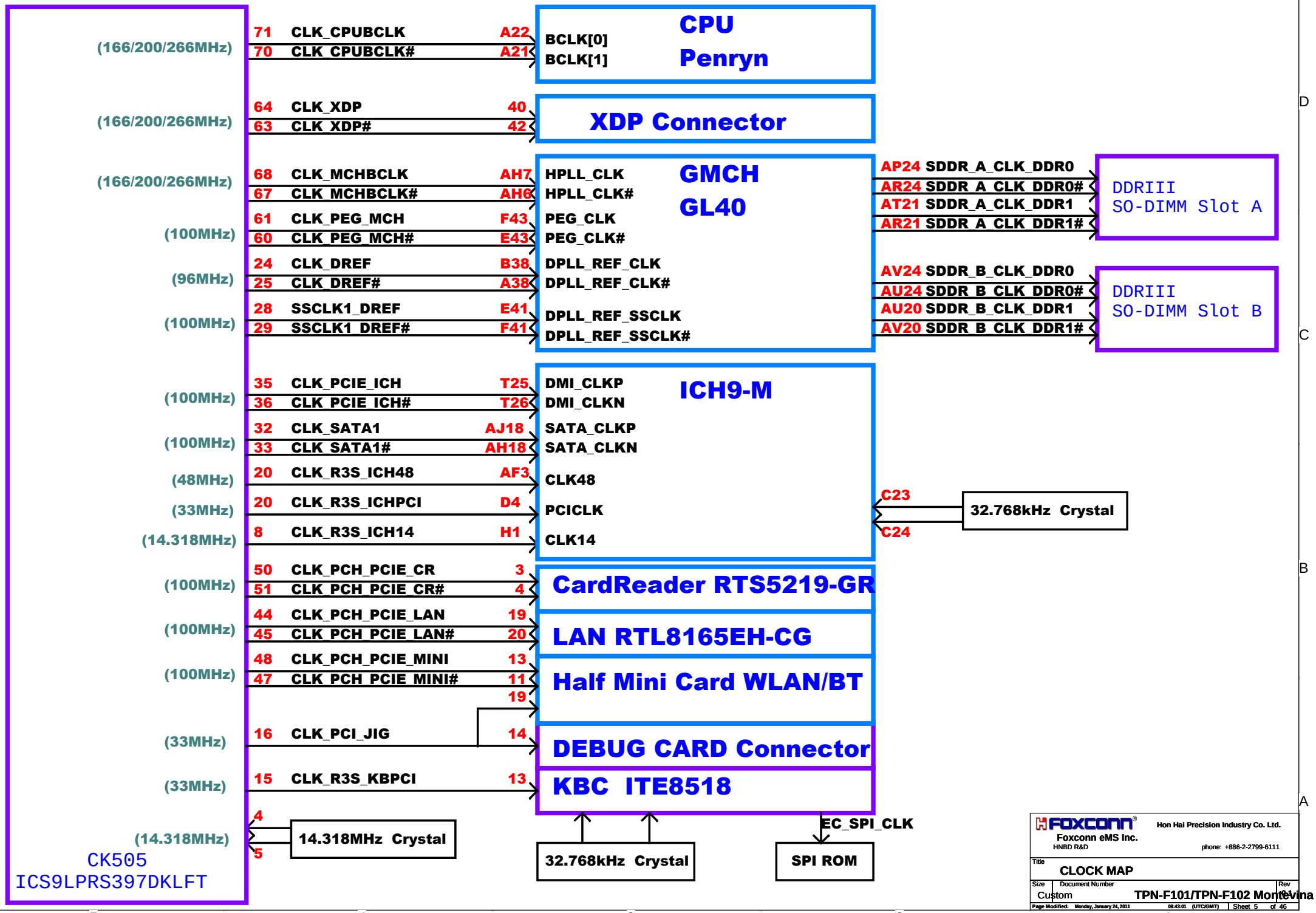
CK505
ICS9LPRS397DKLFT
(166/200/266MHz) 71 CLK_CPUBCLK
70 CLK_CPUBCLK#
CPU
Penryn
BCLK[0] A22
BCLK[1] A21
(166/200/266MHz) 64 CLK_XDP
63 CLK_XDP#
XDP Connector
40
42
(166/200/266MHz) 68 CLK_MCHBCLK
67 CLK_MCHBCLK#
(100MHz) 61 CLK_PEG_MCH
60 CLK_PEG_MCH#
(96MHz) 24 CLK_DREF
25 CLK_DREF#
(100MHz) 28 SSCLK1_DREF
29 SSCLK1_DREF#
GMCH
GL40
HPLL_CLK AH7
HPLL_CLK# AH6
PEG_CLK F43
PEG_CLK# E43
DPLL_REF_CLK B38
DPLL_REF_CLK# A38
DPLL_REF_SSCLK E41
DPLL_REF_SSCLK# F41
AP24 SDDR_A_CLK_DDR0
AR24 SDDR_A_CLK_DDR0#
AT21 SDDR_A_CLK_DDR1
AR21 SDDR_A_CLK_DDR1#
DDRIII
SO-DIMM Slot A
AV24 SDDR_B_CLK_DDR0
AU24 SDDR_B_CLK_DDR0#
AU20 SDDR_B_CLK_DDR1
AV20 SDDR_B_CLK_DDR1#
DDRIII
SO-DIMM Slot B
(100MHz) 35 CLK_PCIE_ICH
36 CLK_PCIE_ICH#
(100MHz) 32 CLK_SATA1
33 CLK_SATA1#
(48MHz) 20 CLK_R3S_ICH48
(33MHz) 20 CLK_R3S_ICHPCI
(14.318MHz) 8 CLK_R3S_ICH14
ICH9-M
DMI_CLKP T25
DMI_CLKN T26
SATA_CLKP AJ18
SATA_CLKN AH18
CLK48 AF3
PCICLK D4
CLK14 H1
C23
C24
32.768kHz Crystal
(100MHz) 50 CLK_PCH_PCIE_CR
51 CLK_PCH_PCIE_CR#
(100MHz) 44 CLK_PCH_PCIE_LAN
45 CLK_PCH_PCIE_LAN#
(100MHz) 48 CLK_PCH_PCIE_MINI
47 CLK_PCH_PCIE_MINI#
(33MHz) 16 CLK_PCI_JIG
(33MHz) 15 CLK_R3S_KBPCI
(14.318MHz) 4
5
14.318MHz Crystal
3
4
19
11
13
14
CardReader RTS5219-GR
LAN RTL8165EH-CG
Half Mini Card WLAN/BT
DEBUG CARD Connector
KBC ITE8518
32.768kHz Crystal
EC_SPI_CLK
SPI ROM
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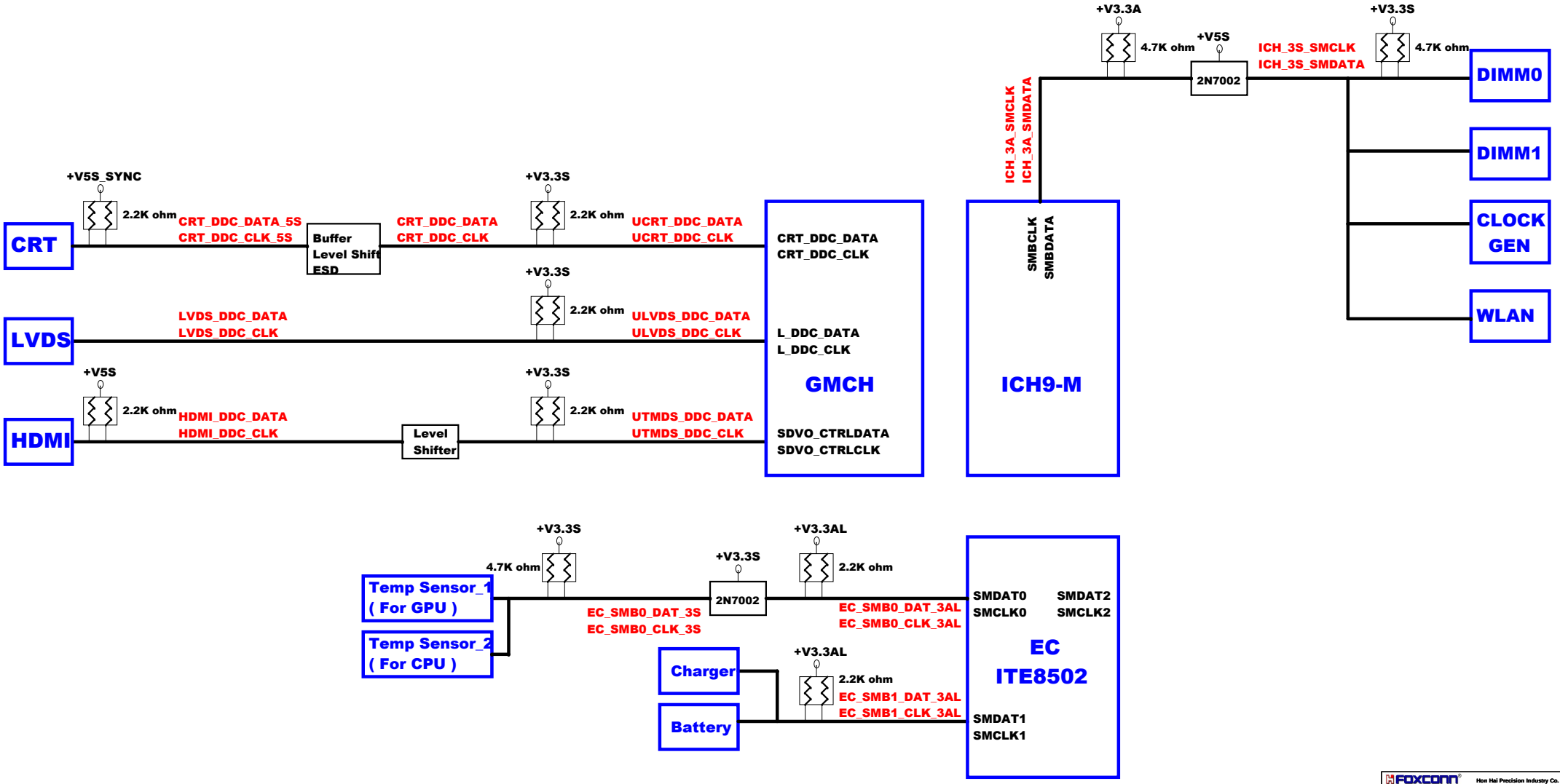


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Title: SMBUS&I2C MAP

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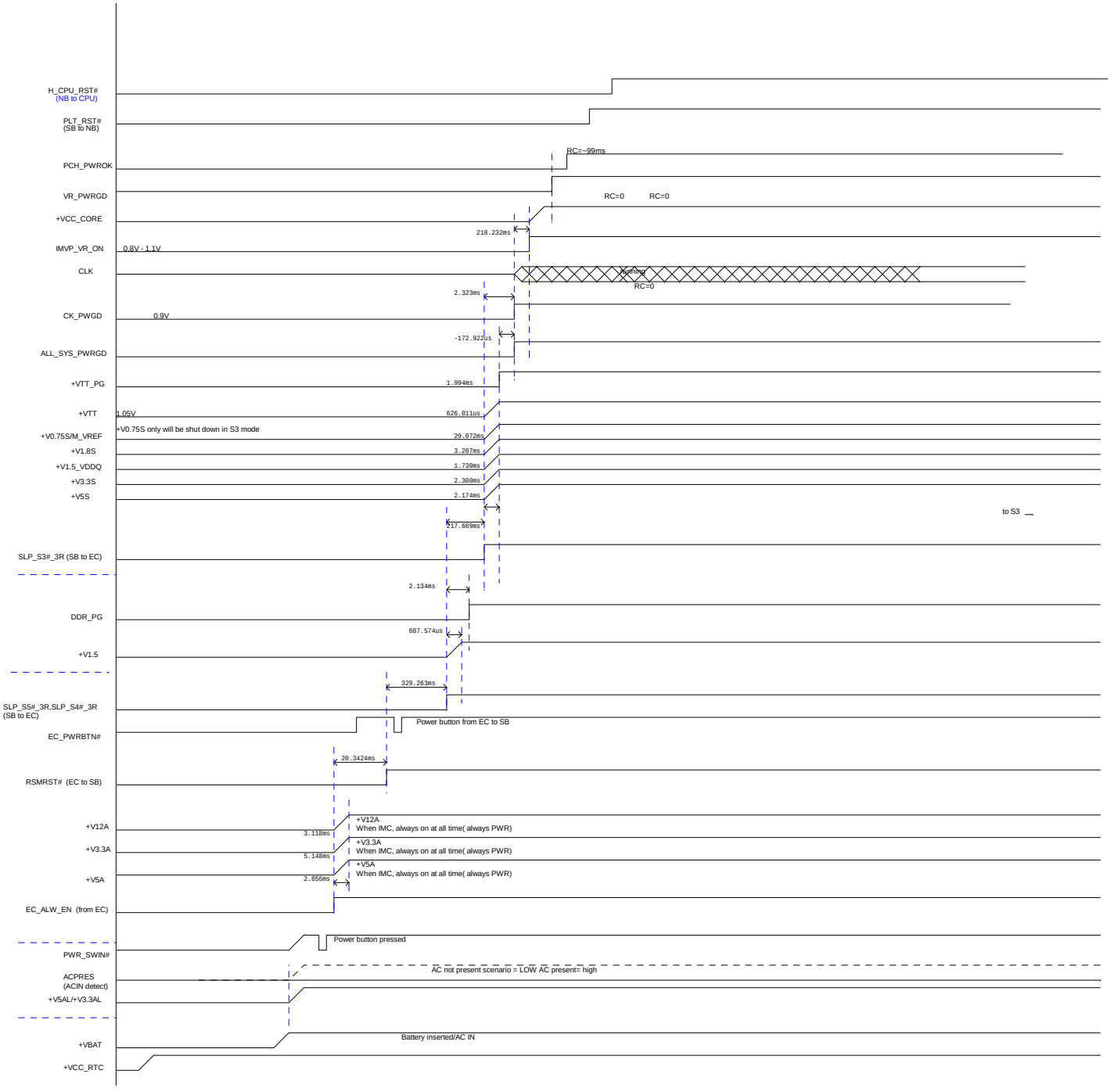


**Power on Sequence required:**

**ICH9M:**
**1, +V3.3A ramp before +V1.1A**
**2, +V3.3S ramp before +V1.8S**
**3, +V1.8S ramp before +V1.1S**
**5, +V3.3A ramping down time > 300us**
**6, 50uS <= All power rails except +V3.3A <= 40mS**
**7, 100uS <= +V3.3A <= 40mS**

**GMCH:**
**1, 0 <(+V3.3S) - (+V1.8S) < 2.1**
**2, +V1.8S ramp before +V1.1S**
**3. +V1.1S ramp before +VCC_NB**

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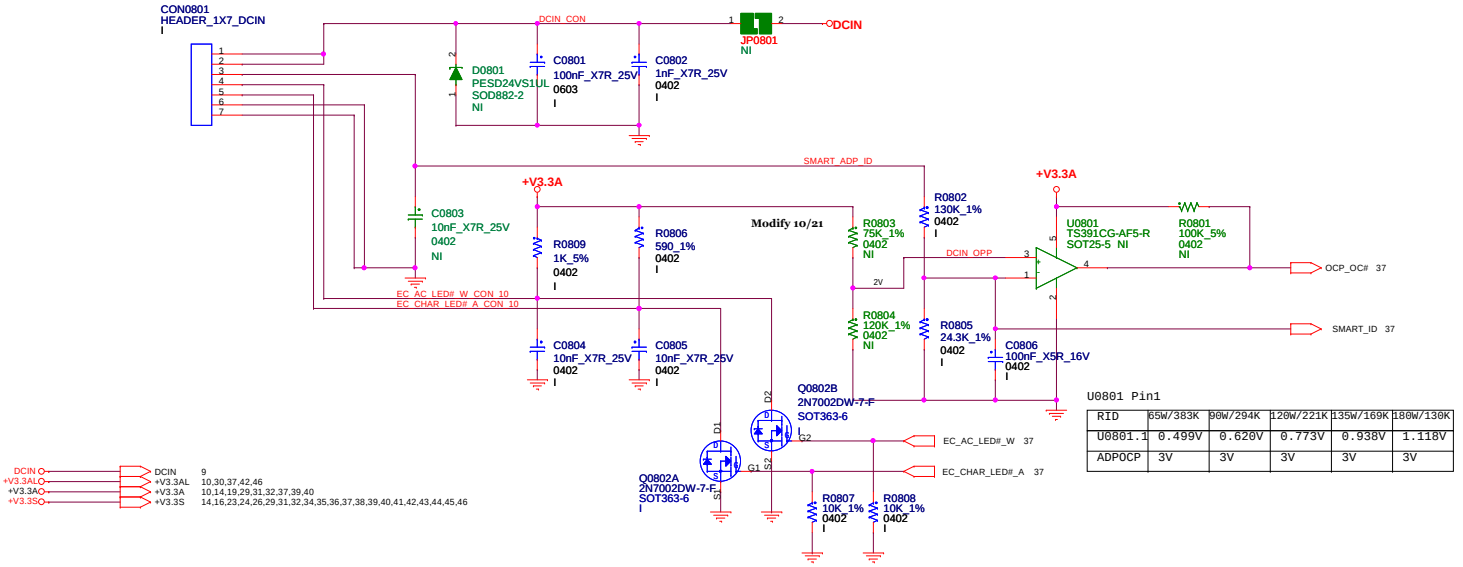
# DC_JACK WIRE to BOARD CONNECTOR

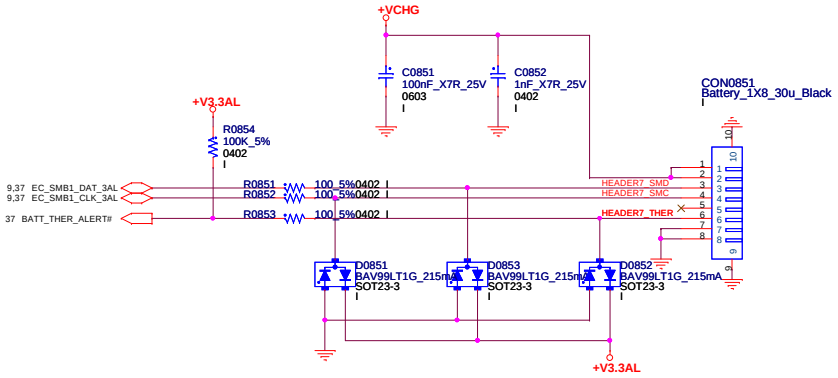



U0801 Pin1

| RID | 65W/383K | 90W/294K | 120W/221K | 135W/169K | 180W/130K |
|---|---|---|---|---|---|
| U0801.1 | 0.499V | 0.620V | 0.773V | 0.938V | 1.118V |
| ADPOCP | 3V | 3V | 3V | 3V | 3V |

# BATTERY CONNECTOR

**2010.0914.0**





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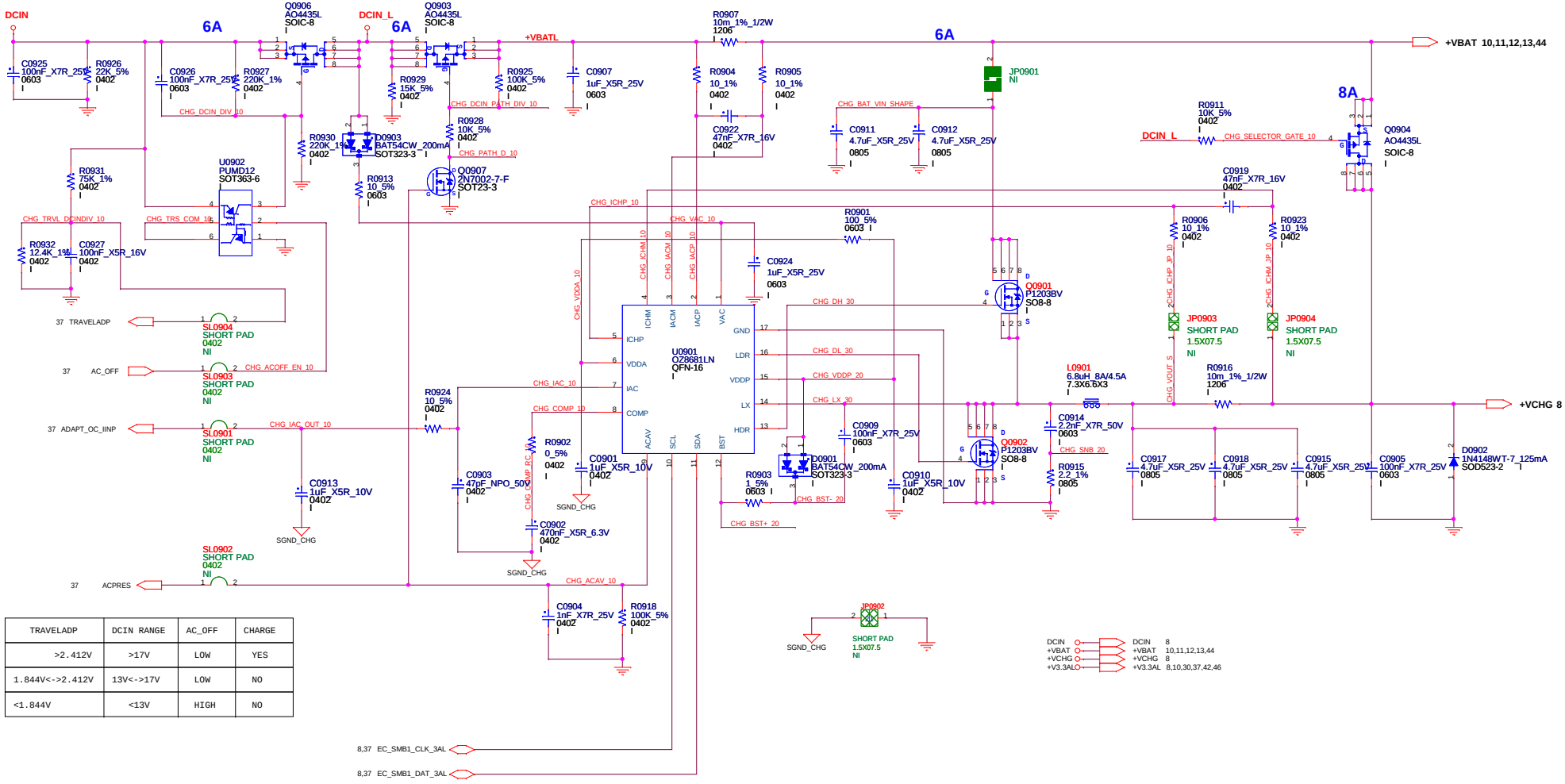
# BATTERY CHARGER




| TRAVELADP | DCIN RANGE | AC_OFF | CHARGE |
|---|---|---|---|
| >2.412V | >17V | LOW | YES |
| 1.844V<->2.412V | 13V<->17V | LOW | NO |
| <1.844V | <13V | HIGH | NO |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# +V5A / +V3.3A POWER SUPPLY

2010.1103.0

**+V5A:**

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=3.7A
2. Ripple Current:
   Irip=3.72A
3. Ripple Voltage:
   ESR/1=15mohm
   Vrip=55.8mV
4. Inductor Spec:
   Isat=13.5A
   Idc=6A
   DCR=30mohm
5. MOSFET Spec:
   H-side MOSFET: IRF8707PBF
   Rds(ON)=17.5mohm (Vgs=4.5 V)
   I cont = 11A (T =25 ℃)
   I peak = 88A (Pause =10 us)
6. Frequency:
   F=300KHz
7. OCP:
   Set = R1002 to 100K
   Vtrip= (R1002*10uA/9)-24mV=0.0655V
   Iocp=Vtrip/Rdson + Iripple/2 = 6.4A

**+V3.3A:**

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=2.2A
2. Ripple Current:
   Irip=2.21A
3. Ripple Voltage:
   ESR/1=15mohm
   Vrip=33.15mV
4. Inductor Spec:
   Isat=13.5A
   Idc=6A
   DCR=30mohm
5. MOSFET Spec:
   L-side MOSFET: IRF8707PBF
   Rds(ON)=17.5mohm (Vgs=4.5 V)
   I cont = 11A (T =25 ℃)
   I peak = 88A (Pause =10 us)
6. Frequency:
   F=375KHz
7. OCP:
   Set = R1003 to 100K
   Vtrip= (R1003*10uA/9)-24mV=0.0655V
   Iocp=Vtrip/Rdson + Iripple/2 = 5.7A

Imax=4.5A
OCP=5.7A

Imax=5A
OCP=6.4A

Vref=2.0V

Vref=2.0V

+V2REF

+V3.3A

+V3.3AL

+VBAT

+V5A

+V5AL

+V12A

U1001 TPS51123RGER QFN-24

Q1003 P1203BV SO8-8

Q1004 P1203BV SO8-8

Q1001 P1203BV SO8-8

Q1002 P1203BV SO8-8

D1004 BAT54CW_200mA SOT323-3

D1001 BAV99LT1G_215mA SOT23-3

D1002 BAV99LT1G_215mA SOT23-3

D1006 SSM5818SPT_1A SOD-123

D1005 SSM5818SPT_1A SOD-123

L1002 3.3uH_13.5A/6A 7.3X6.6X3.0

L1001 3.3uH_13.5A/6A 7.3X6.6X3.0

P_5V3V_VIN_SHAPE

P_5V3V_VIN_SHAPE

P +V3.3AL_OUT_20

P +V3.3A_OUT_S

P +V5A_OUT_S

KBC_PWR_ON_PWR

KBC_PWR_ON_PWR

DCIN_L

+VBAT

SHUTDOWN#

| | | | |
|---|---|---|---|
| DCIN | DCIN | 8,9 |
| +V12A | +V12A | 14 |
| +VBAT | +VBAT | 9,11,12,13,44 |
| +V3.3AL | +V3.3AL | 8,30,37,42,46 |
| +V5AL | +V5AL | 14,16 |
| +V3.3S | +V3.3S | 14,16,23,24,26,29,31,32,34,35,36,37,38,39,40,41,42,43,44,45,46 |
| +V5S | +V5S | 12,14,16,32,38,39,43,44,45,46 |

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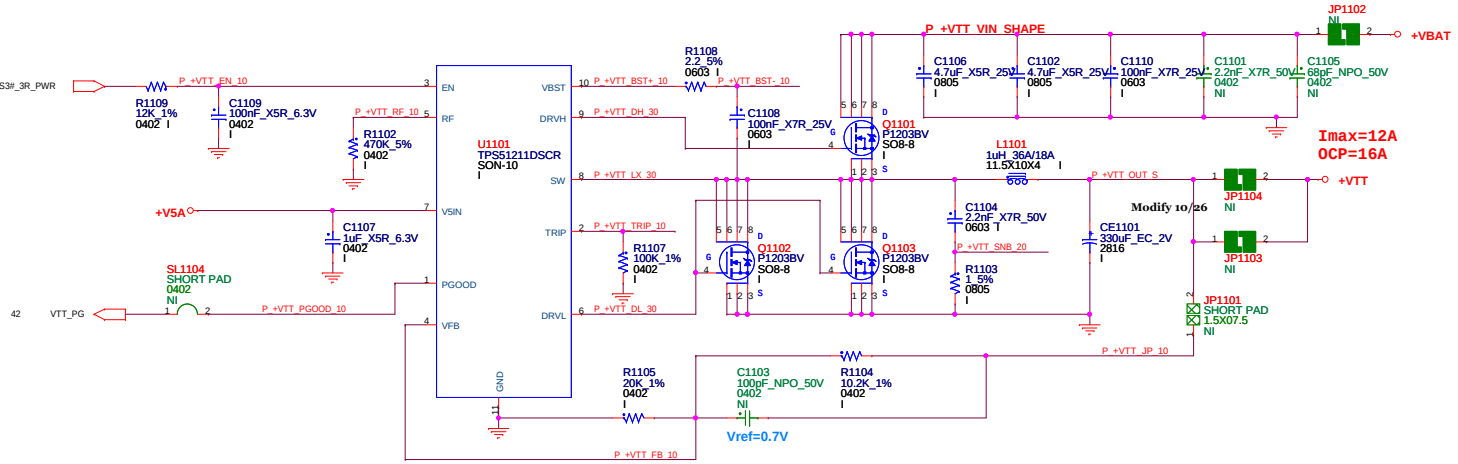
# +VTT POWER SUPPLY




+V3.3S → +V3.3S 14,16,23,24,26,29,31,32,34,35,36,37,38,39,40,41,42,43,44,45,46

+V5S → +V5S 12,14,16,32,38,39,43,44,45,46

+VBAT → +VBAT 9,10,12,13,44

+VTT → +VTT 13,14,19,20,21,22,23,24,26,27,30,32,36,46

**+VTT:**

**1. I/P Current:**

Iin=Vo*Io/(0.75*Vin)=1.86A

**2. Ripple Current:**

Irip=3.42A

**3. Ripple Voltage:**

ESR/1=9mohm
Vrip=30.78mV

**4. Inductor Spec:**

Isat=36A
Idc=18A
DCR=3.3mohm

**5.MOSFET Spec:**

H-side MOSFET: IRF8707PBF
Rds(ON)=17.5mohm (Vgs=4.5 V)
I cont = 11A (T =25 ℃)
I peak = 88A (Pause =10 us)

L-side MOSFET: IRF8707PBF
Rds(ON)=17.5mohm (Vgs=4.5 V)
I cont = 11A (T =25 ℃)
I peak = 88A (Pause =10 us)

**6. Frequency:**

F=290KHz (R0802=470K)

**7. OCP:**

Set = R0807 to 100K
Vtrip= R0807*10uA=1V
Iocp=(Vtrip/8*Rdson) + Iripple/2 = 16A

| | | |
|---|---|---|
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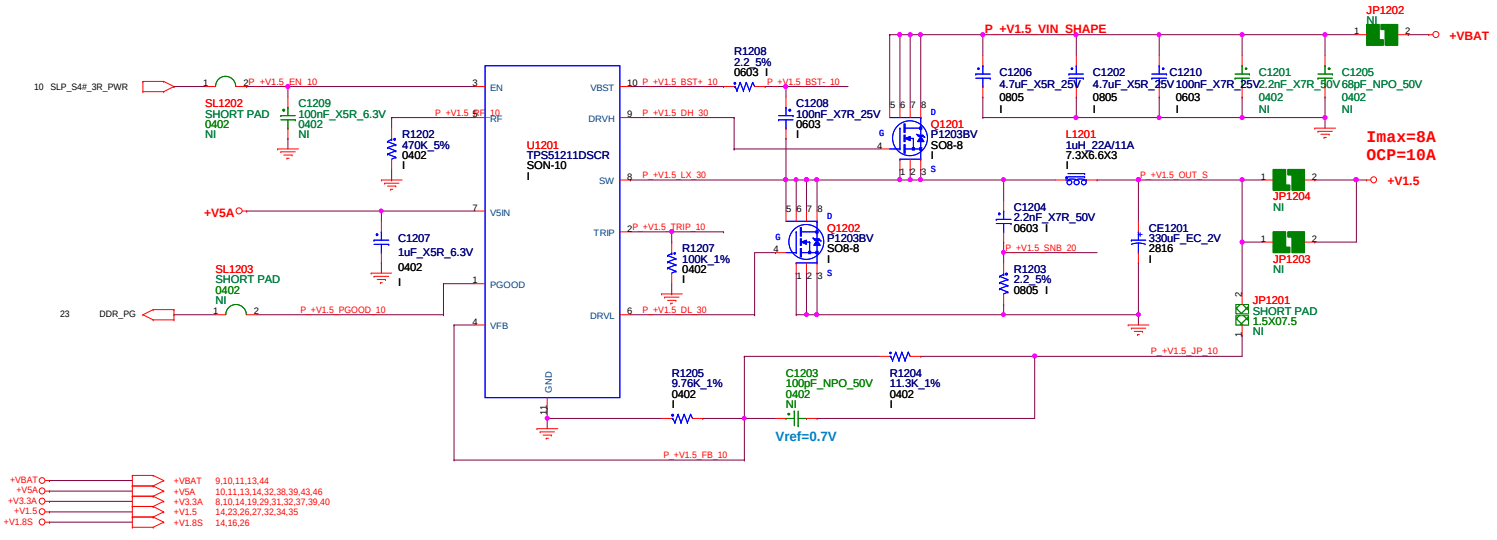
# +V1.5 POWER SUPPLY







**+V1.5:**

**1. I/P Current:**

Iin=Vo*Io/(0.75*Vin)=1.78A

**2. Ripple Current:**

Irip=3.34A

**3. Ripple Voltage:**

ESR/1=9mohm
Vrip=30.6mV

**4. Inductor Spec:**

Isat=36A
Idc=18A
DCR=3.3mohm

**5.MOSFET Spec:**

| H-side MOSFET: IRF8707PBF | | L-side MOSFET: IRF8707PBF | |
|---|---|---|---|
| Rds(ON)=17.5mohm | (Vgs=4.5 V) | Rds(ON)=17.5mohm | (Vgs=4.5 V) |
| I cont = 11A | (T =25 ℃) | I cont = 11A | (T =25 ℃) |
| I peak = 88A | (Pause =10 us) | I peak = 88A | (Pause =10 us) |

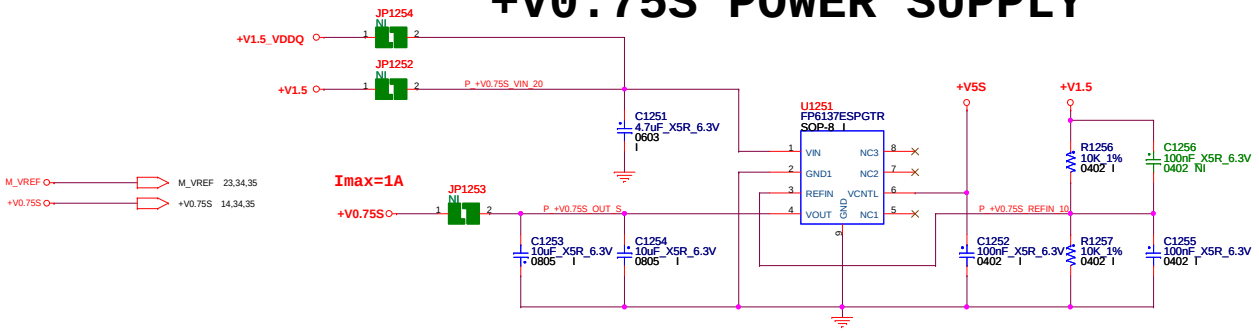
**6. Frequency:**

F=290KHz (R0902=470K)

**7. OCP:**

Set = R0907 to 100K
Vtrip= R0907*10uA=1V
Iocp=(Vtrip/8*Rdson) + Iripple/2 = 9.5A

# +V0.75S POWER SUPPLY







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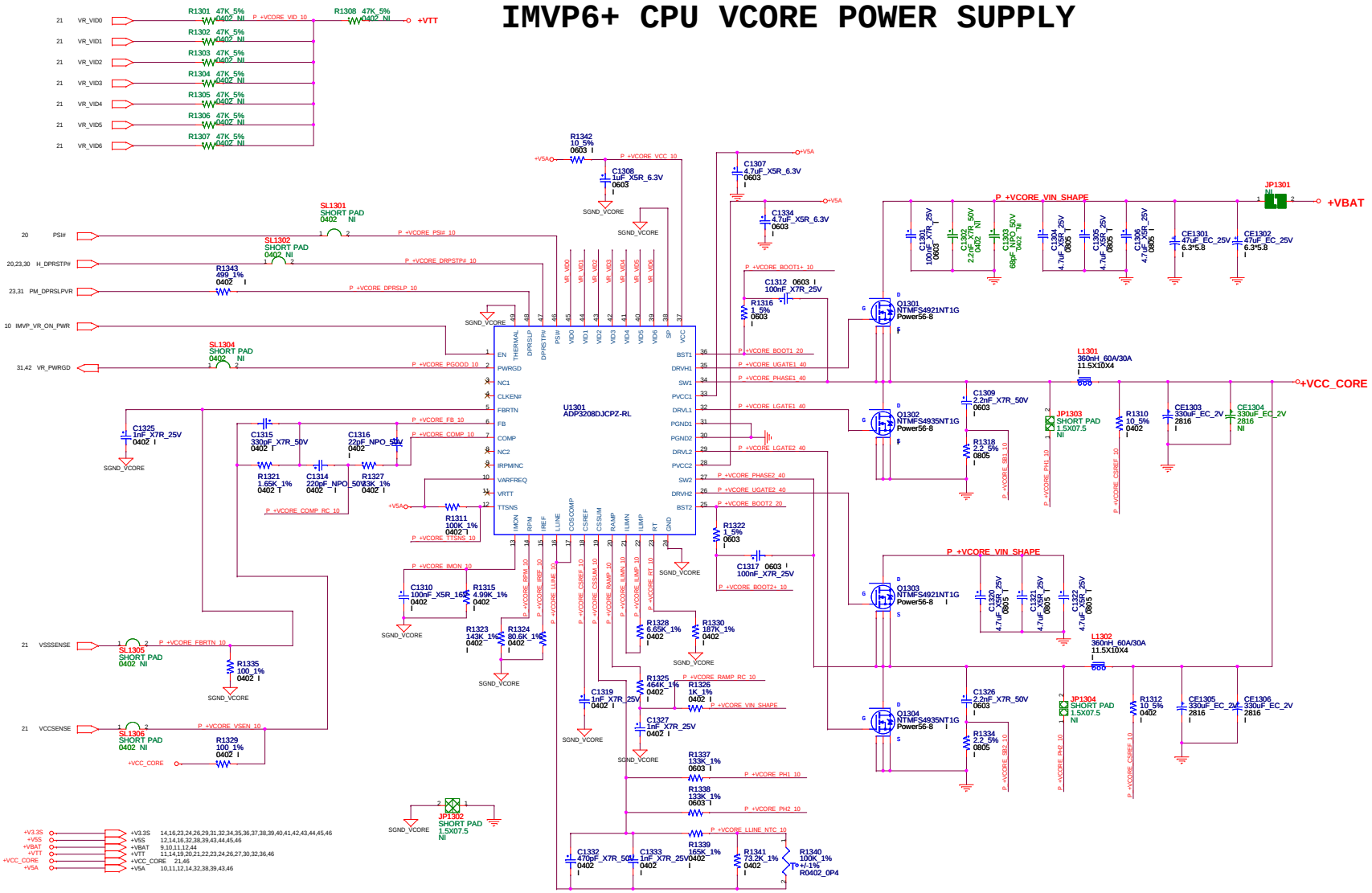
# IMVP6+ CPU VCORE POWER SUPPLY

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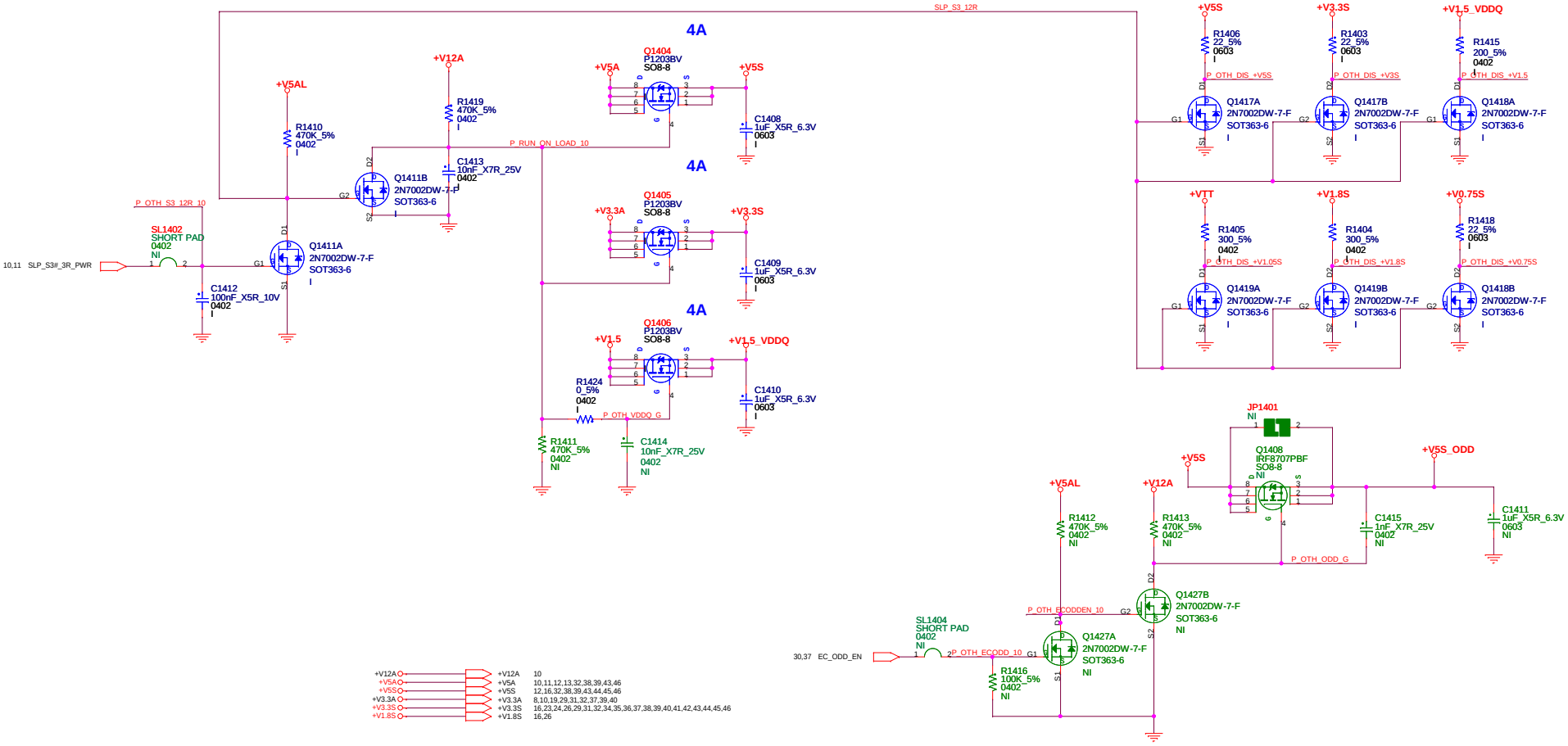
# OTHER POWER / DISCHARGE CIRCUITS




| | |
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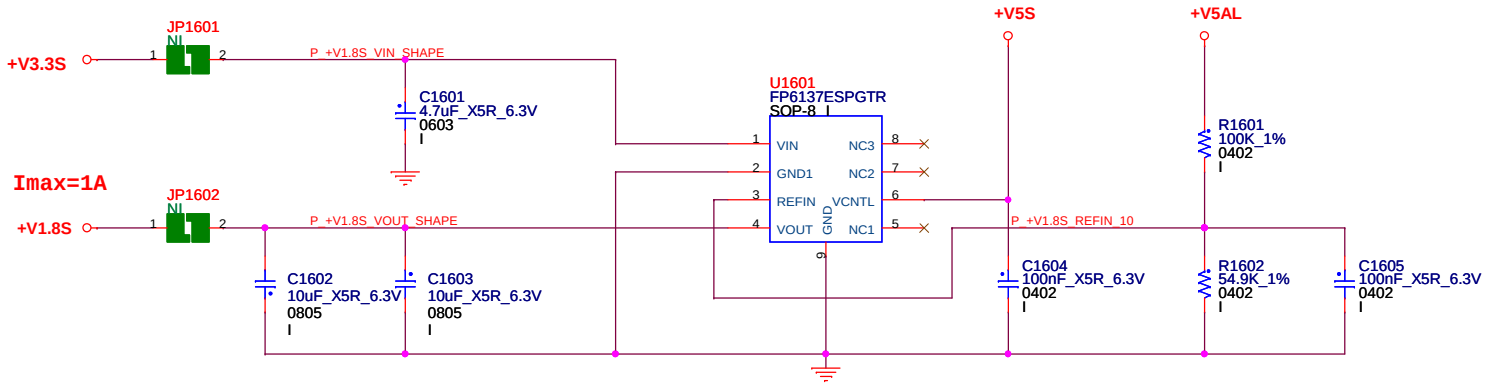
# +V1.8S POWER SUPPLY





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| PWR_1.8VS | | |
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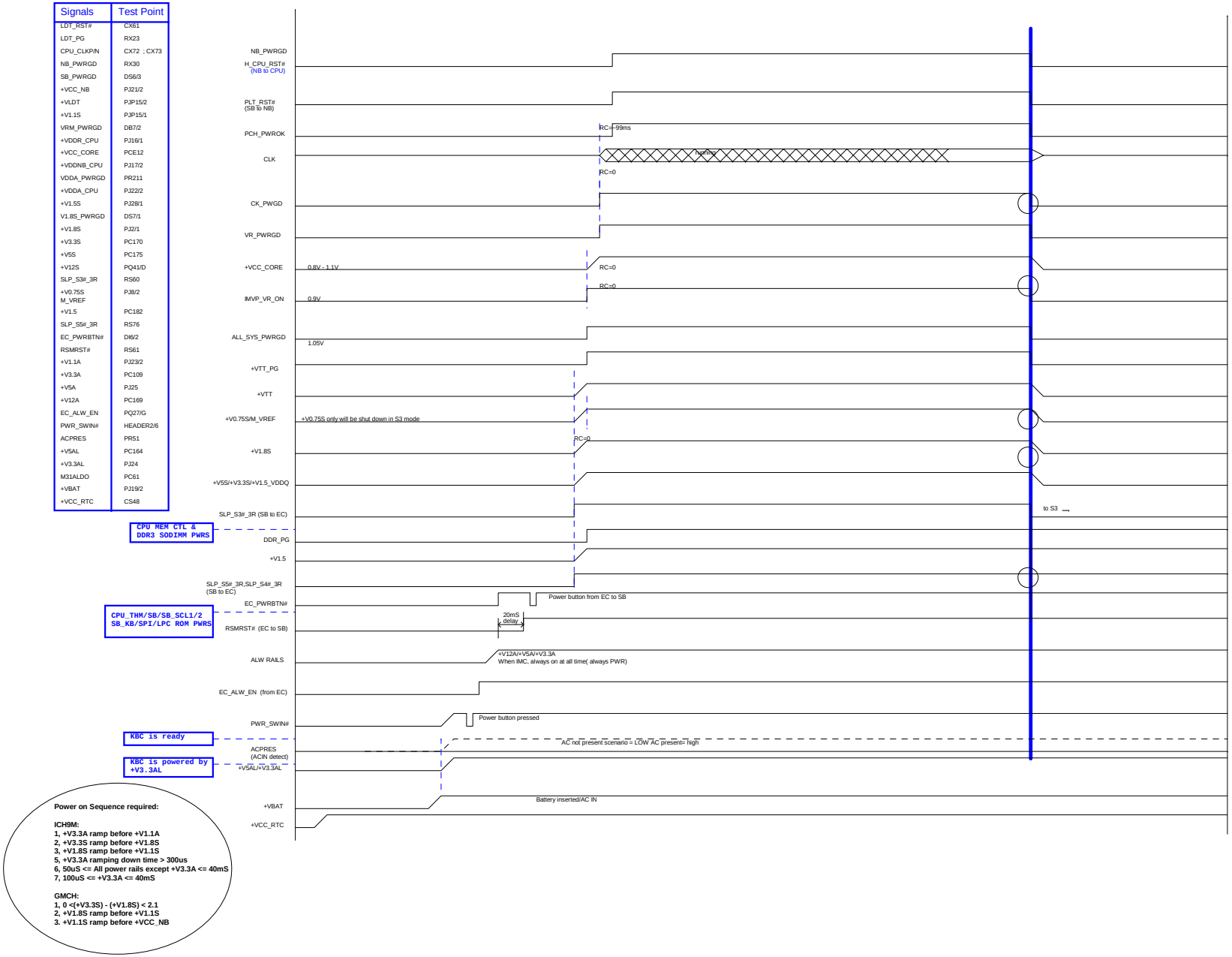
| Signals | Test Point |
|---|---|
| LDT_RST# | CX61 |
| LDT_PG | RX23 |
| CPU_CLKP/N | CX72 ; CX73 |
| NB_PWRGD | RX30 |
| SB_PWRGD | DS6/3 |
| +VCC_NB | PJ21/2 |
| +VLDT | PJP15/2 |
| +V1.1S | PJP15/1 |
| VRM_PWRGD | DB7/2 |
| +VDDR_CPU | PJ16/1 |
| +VCC_CORE | PCE12 |
| +VDDNB_CPU | PJ17/2 |
| VDDA_PWRGD | PR211 |
| +VDDA_CPU | PJ22/2 |
| +V1.5S | PJ28/1 |
| V1.8S_PWRGD | DS7/1 |
| +V1.8S | PJ2/1 |
| +V3.3S | PC170 |
| +V5S | PC175 |
| +V12S | PQ41/D |
| SLP_S3#_3R | RS60 |
| +V0.75S M_VREF | PJ8/2 |
| +V1.5 | PC182 |
| SLP_S5#_3R | RS76 |
| EC_PWRBTN# | DI6/2 |
| RSMRST# | RS61 |
| +V1.1A | PJ23/2 |
| +V3.3A | PC109 |
| +V5A | PJ25 |
| +V12A | PC169 |
| EC_ALW_EN | PQ27/G |
| PWR_SWIN# | HEADER2/6 |
| ACPRES | PR51 |
| +V5AL | PC164 |
| +V3.3AL | PJ24 |
| M31ALDO | PC61 |
| +VBAT | PJ19/2 |
| +VCC_RTC | CS48 |




**Power on Sequence required:**

**ICH9M:**
**1, +V3.3A ramp before +V1.1A**
**2, +V3.3S ramp before +V1.8S**
**3, +V1.8S ramp before +V1.1S**
**5, +V3.3A ramping down time > 300us**
**6, 50uS <= All power rails except +V3.3A <= 40mS**
**7, 100uS <= +V3.3A <= 40mS**

**GMCH:**
**1, 0 <(+V3.3S) - (+V1.8S) < 2.1**
**2, +V1.8S ramp before +V1.1S**
**3. +V1.1S ramp before +VCC_NB**

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Title: **POWER SEQUENCE TIMING**

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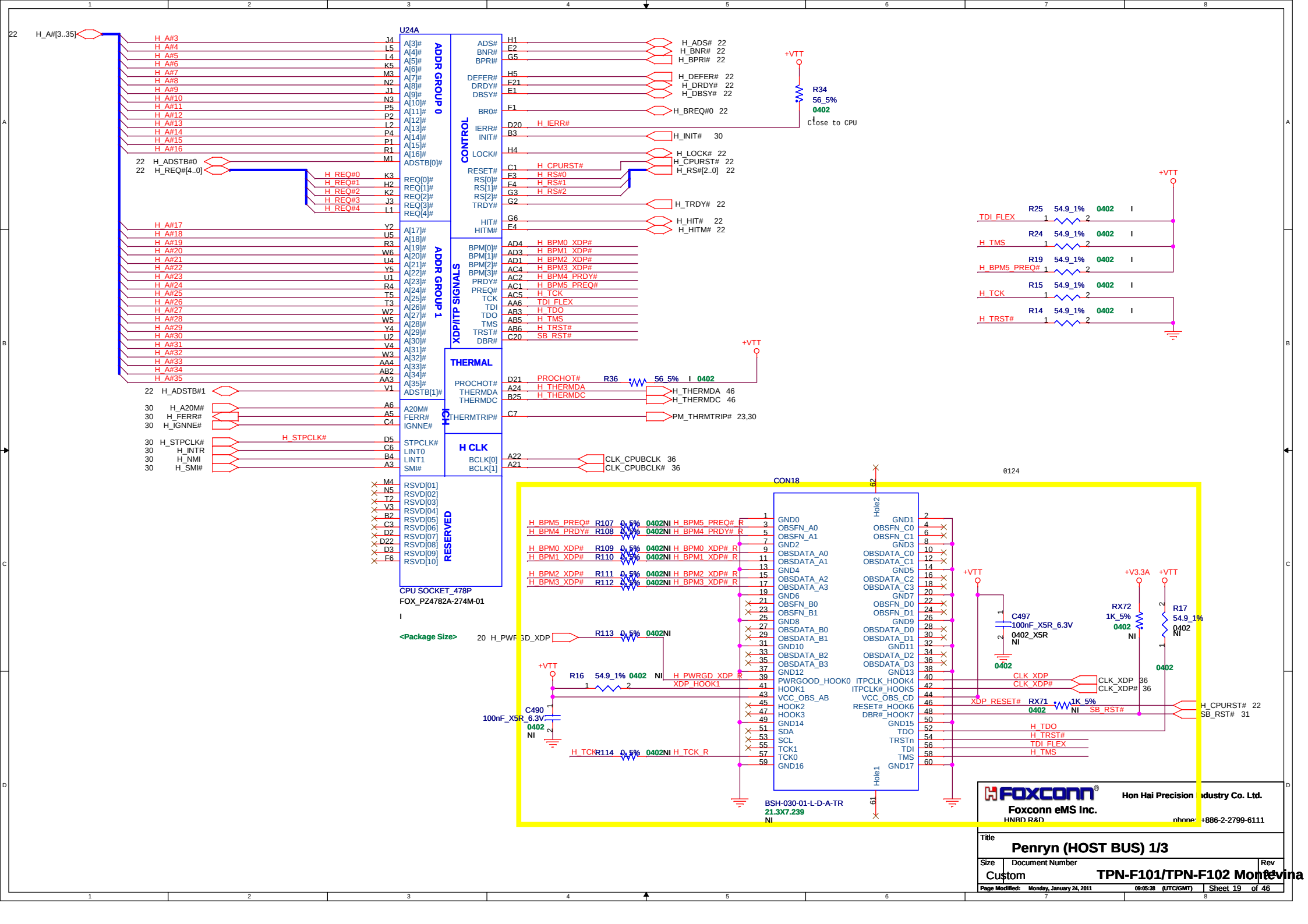
U24A
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ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
H CLK
RESERVED
CPU SOCKET_478P
FOX_PZ4782A-274M-01
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BSH-030-01-L-D-A-TR
21.3X7.239
Penryn (HOST BUS) 1/3
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TPN-F101/TPN-F102 Montevina
Custom
Monday, January 24, 2011
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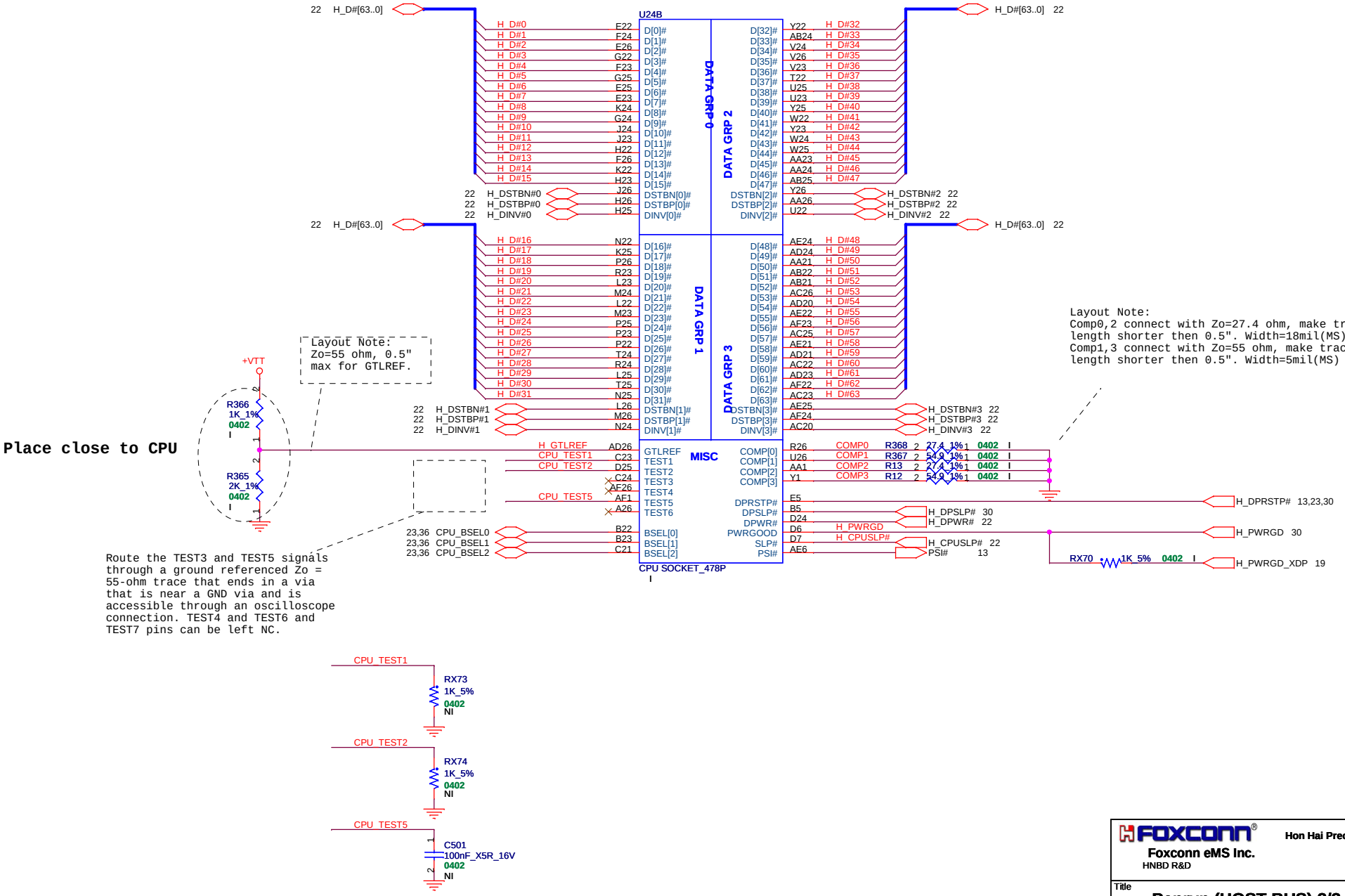


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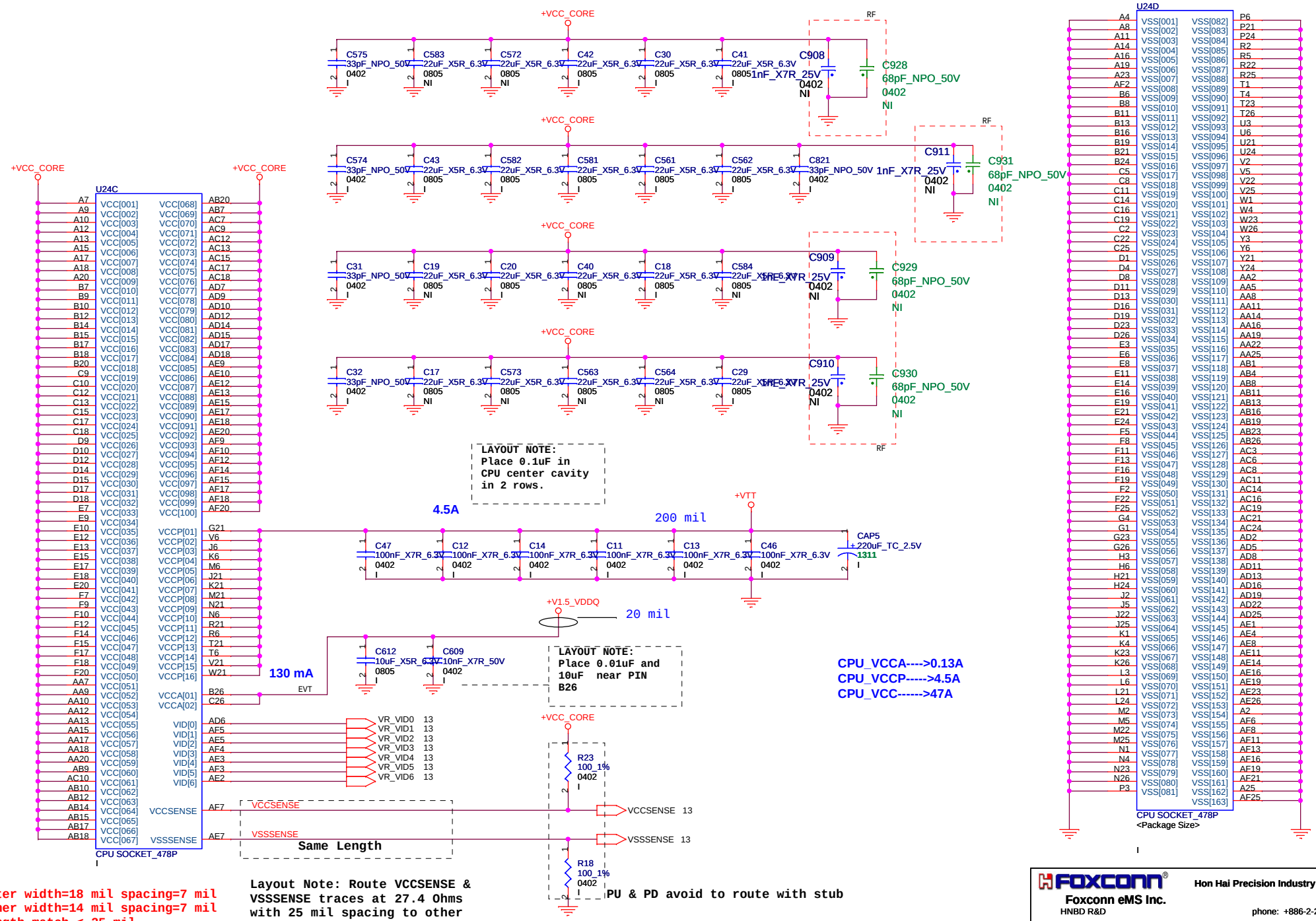


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Title: Penryn (POWER/GROUND) 3/3

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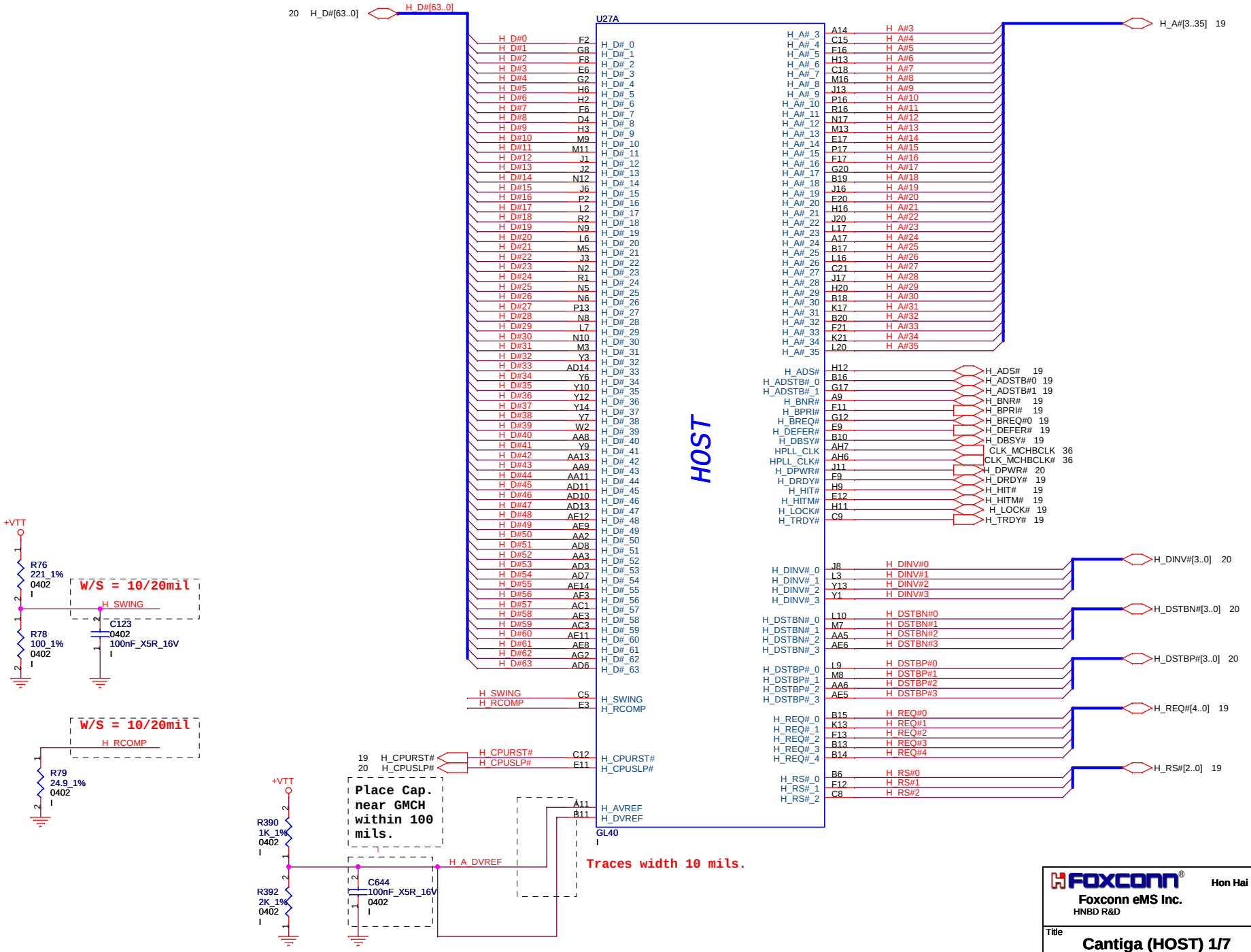


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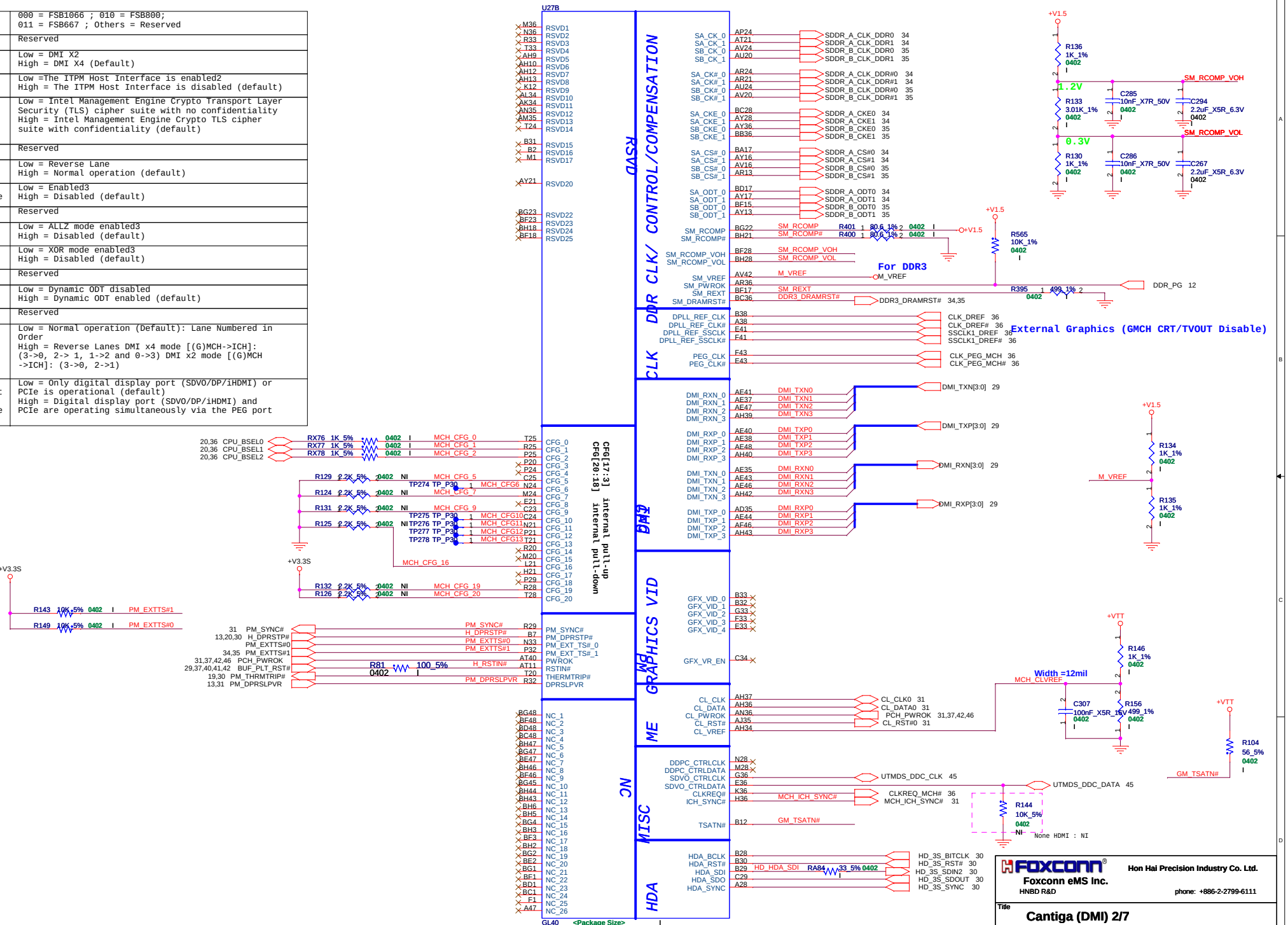
| | |
|---|---|
| MCH_CFG_0~2<br>FSB Frequency | 000 = FSB1066 ; 010 = FSB800;<br>011 = FSB667 ; Others = Reserved |
| MCH_CFG_3~4 | Reserved |
| MCH_CFG_5<br>DMI X2 Select | Low = DMI X2<br>High = DMI X4 (Default) |
| MCH_CFG_6<br>ITPM Host Interface | Low =The ITPM Host Interface is enabled2<br>High = The ITPM Host Interface is disabled (default) |
| MCH_CFG_7<br>Intel Management Engine Crypto Strap | Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality<br>High = Intel Management Engine Crypto TLS cipher suite with confidentiality (default) |
| MCH_CFG_8 | Reserved |
| MCH_CFG_9<br>PCIE Graphics Lane | Low = Reverse Lane<br>High = Normal operation (default) |
| MCH_CFG_10<br>PCIE Loopback enable | Low = Enabled3<br>High = Disabled (default) |
| MCH_CFG_11 | Reserved |
| MCH_CFG_12<br>ALLZ | Low = ALLZ mode enabled3<br>High = Disabled (default) |
| MCH_CFG_13<br>XOR | Low = XOR mode enabled3<br>High = Disabled (default) |
| MCH_CFG_14~15 | Reserved |
| MCH_CFG_16<br>FSB Dynamic ODT | Low = Dynamic ODT disabled<br>High = Dynamic ODT enabled (default) |
| MCH_CFG_17~18 | Reserved |
| MCH_CFG_19<br>DMI Lane Reversal | Low = Normal operation (Default): Lane Numbered in Order<br>High = Reverse Lanes DMI x4 mode [(G)MCH->ICH]: (3->0, 2-> 1, 1->2 and 0->3) DMI x2 mode [(G)MCH ->ICH]: (3->0, 2->1) |
| MCH_CFG_20<br>Digital Display Port (SDVO/ DP/iHDMI) Concurrent with PCIe | Low = Only digital display port (SDVO/DP/iHDMI) or PCIe is operational (default)<br>High = Digital display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via the PEG port |

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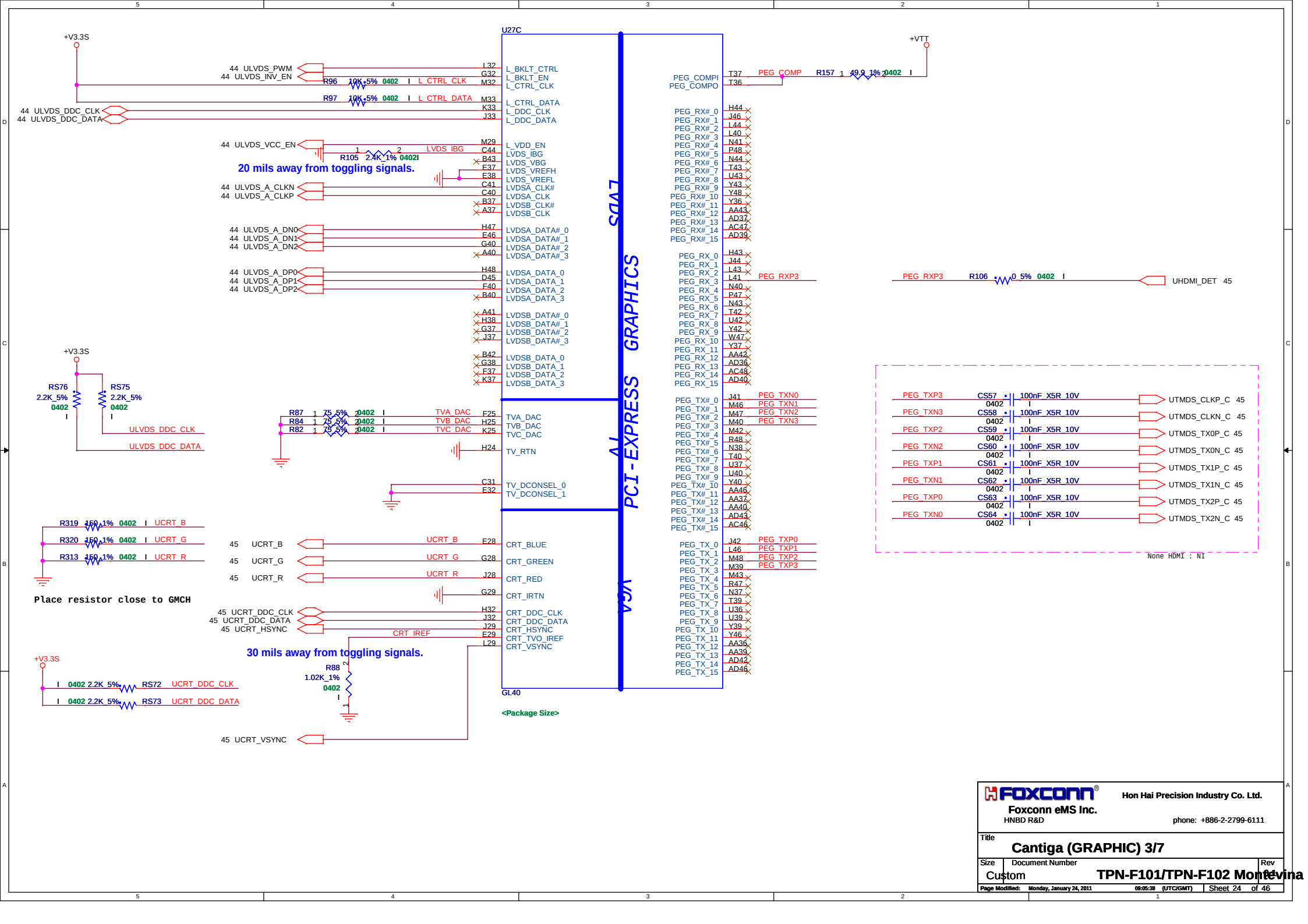
| Page Modified: Monday, January 24, 2011 | 09:05:38 (UTC/GMT) | Sheet 23 of 46 |

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Title: Cantiga (GRAPHIC) 3/7

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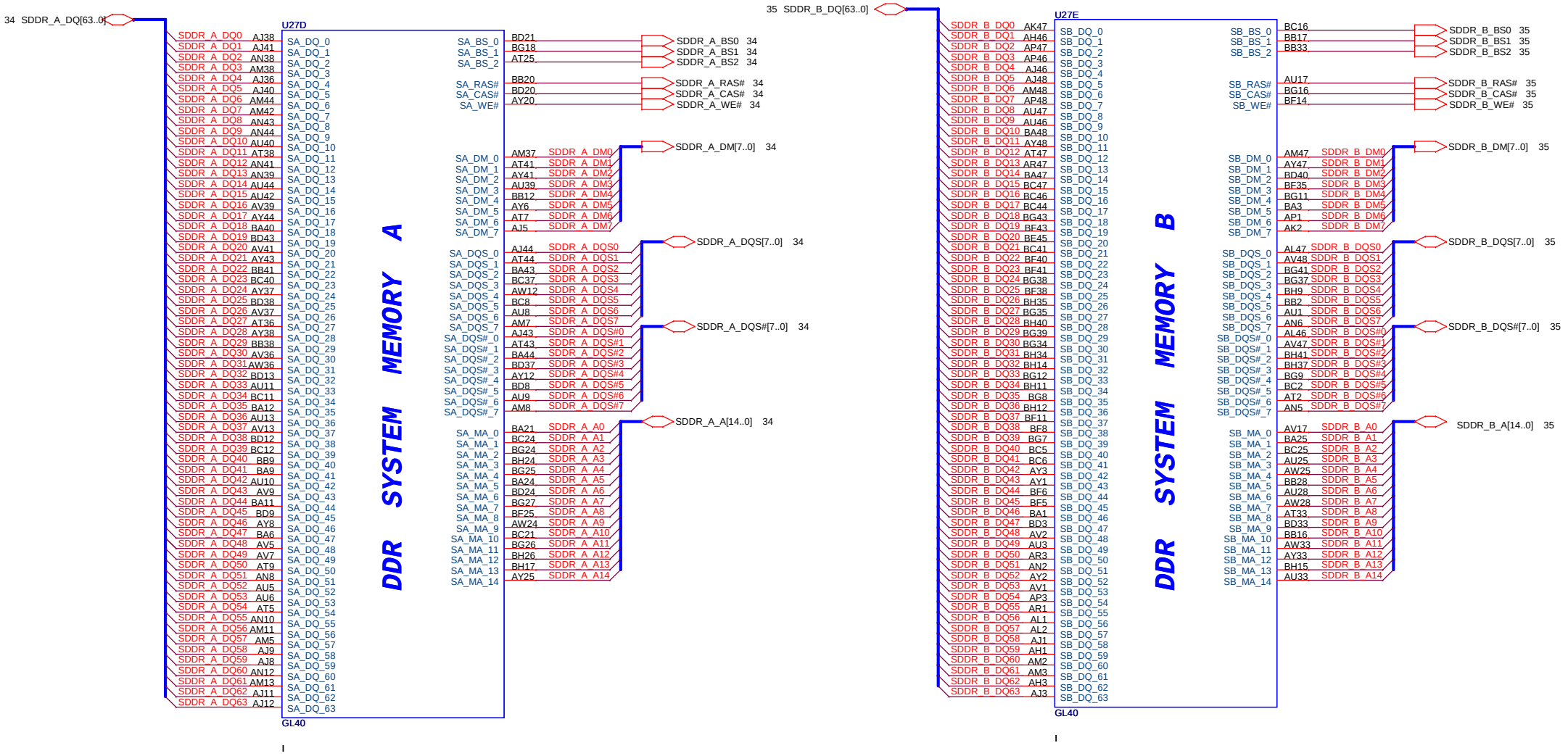


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**Cantiga (DDR3) 4/7**

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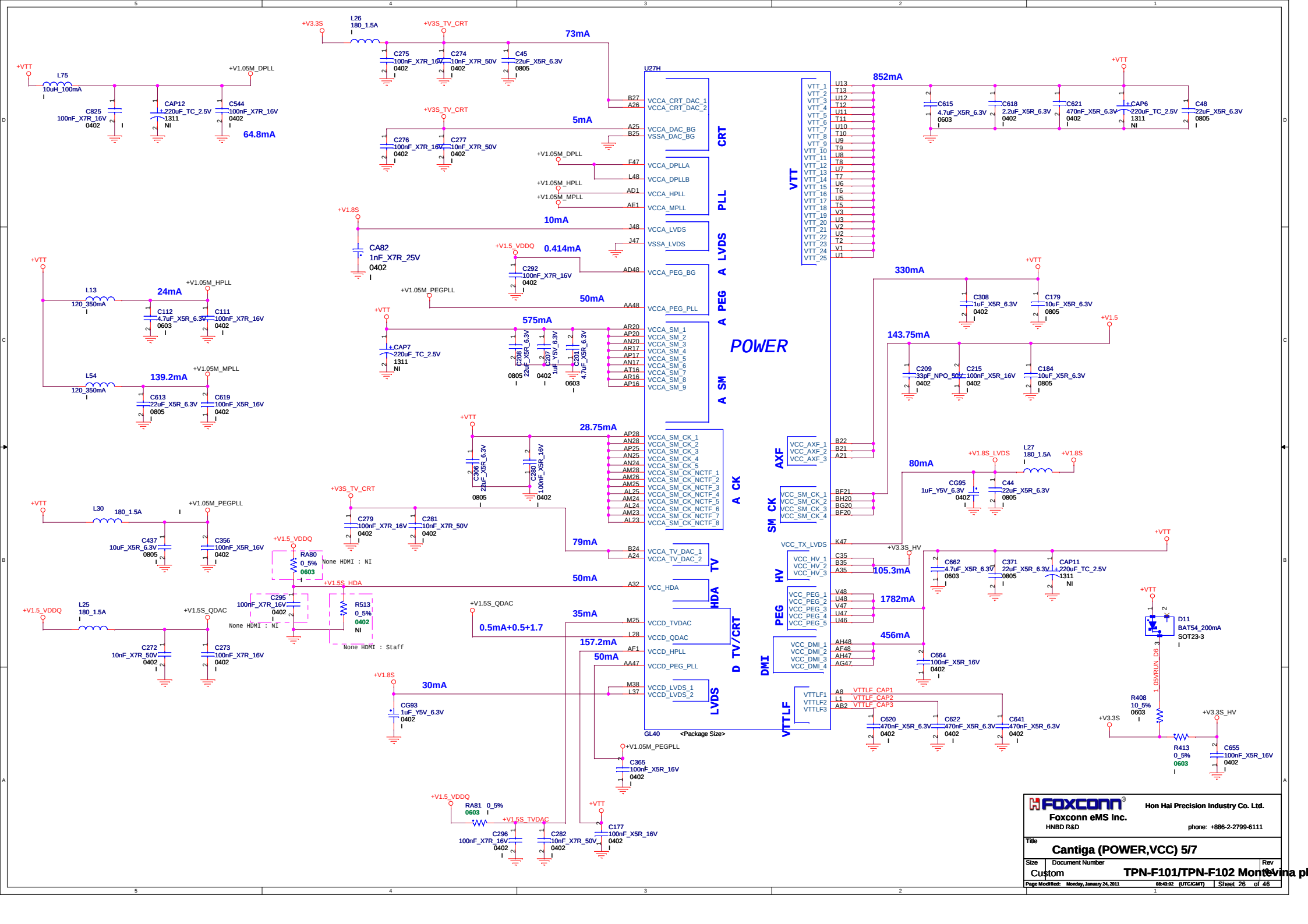
POWER
U27H
CRT
PLL
A LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
LVDS
AXF
SM CK
HV
PEG
DMI
VTTLF
VTT
73mA
5mA
64.8mA
10mA
0.414mA
50mA
575mA
24mA
139.2mA
28.75mA
79mA
50mA
35mA
0.5mA+0.5+1.7
157.2mA
50mA
30mA
852mA
330mA
143.75mA
80mA
105.3mA
1782mA
456mA
L75
10uH_100mA
C825
100nF_X7R_16V
0402
CAP12
220uF_TC_2.5V
1311
NI
C544
100nF_X7R_16V
0402
L26
180_1.5A
C275
100nF_X7R_16V
0402
C274
10nF_X7R_50V
0402
C45
22uF_X5R_6.3V
0805
C276
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C277
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CA82
1nF_X7R_25V
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CAP7
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NI
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22uF_X5R_6.3V
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C207
1uF_Y5V_6.3V
0402
C201
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C112
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C111
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0805
C356
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0402
C279
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0402
C281
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0402
RA80
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0603
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100nF_X7R_16V
0402
None HDMI : NI
R513
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0402
NI
None HDMI : Staff
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C272
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0402
C273
100nF_X7R_16V
0402
CG93
1uF_Y5V_6.3V
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C365
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RA81
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C615
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NI
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C308
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C179
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C209
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0402
C215
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C184
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C641
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SOT23-3
R408
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0603
R413
0_5%
0603
C655
100nF_X5R_16V
0402
1.05VRUN_D6_3
+V3.3S
+V3.3S_HV
+V1.8S
+V1.8S_LVDS
+V1.5
+V1.5_VDDQ
+V1.5S_HDA
+V1.5S_QDAC
+V1.5S_TVDAC
+V1.05M_DPLL
+V1.05M_HPLL
+V1.05M_MPLL
+V1.05M_PEGPLL
+V3S_TV_CRT
+VTT
GL40
<Package Size>
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Cantiga (POWER,VCC) 5/7
Size
Custom
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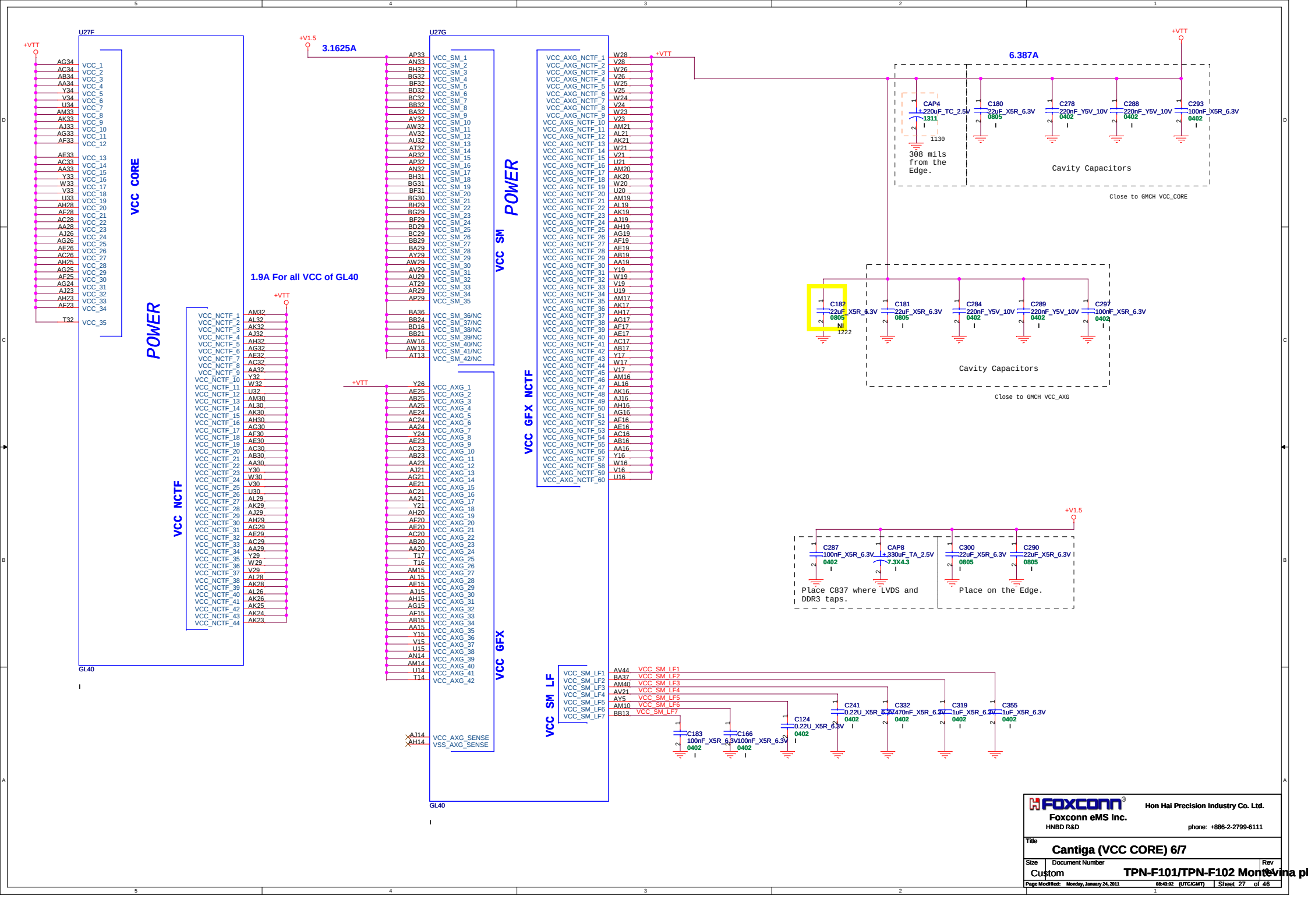


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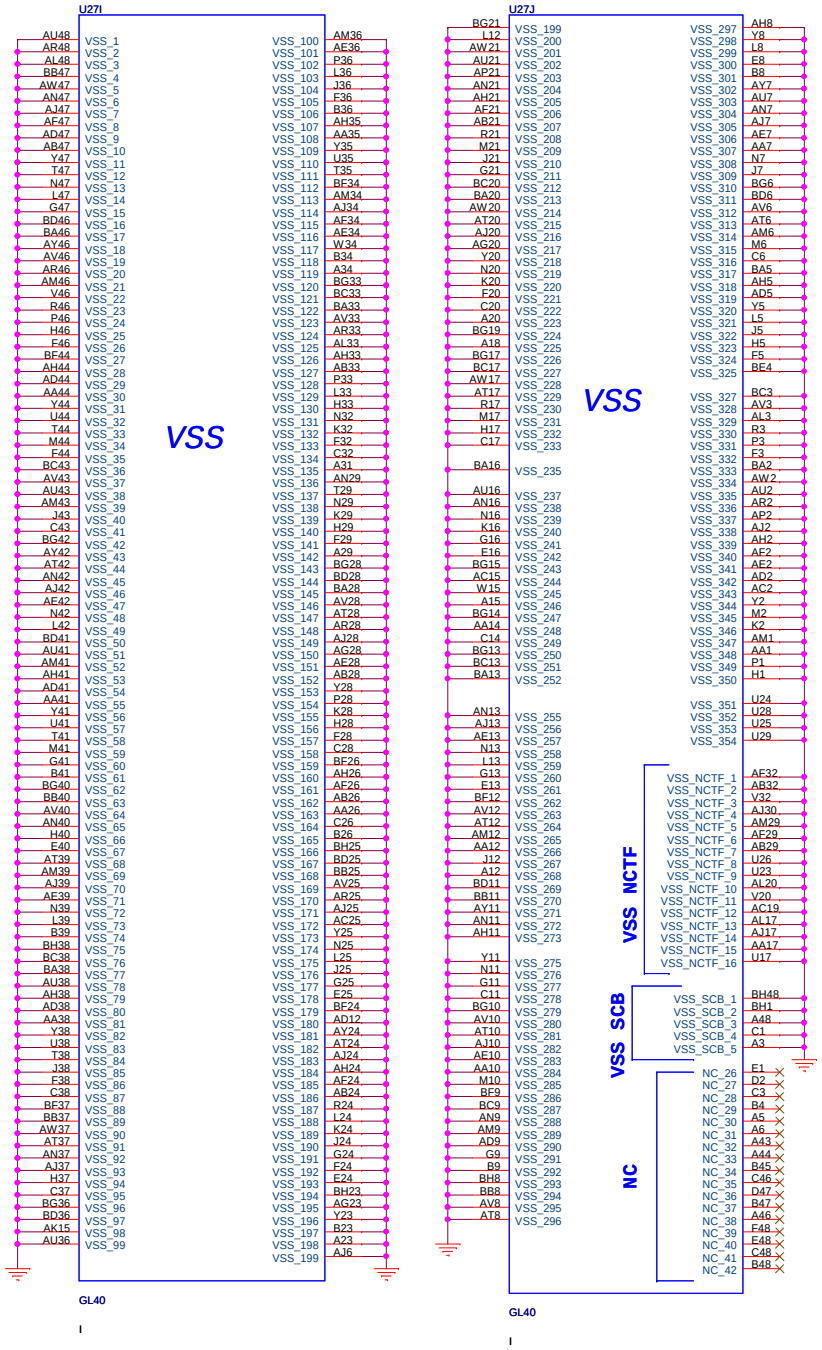


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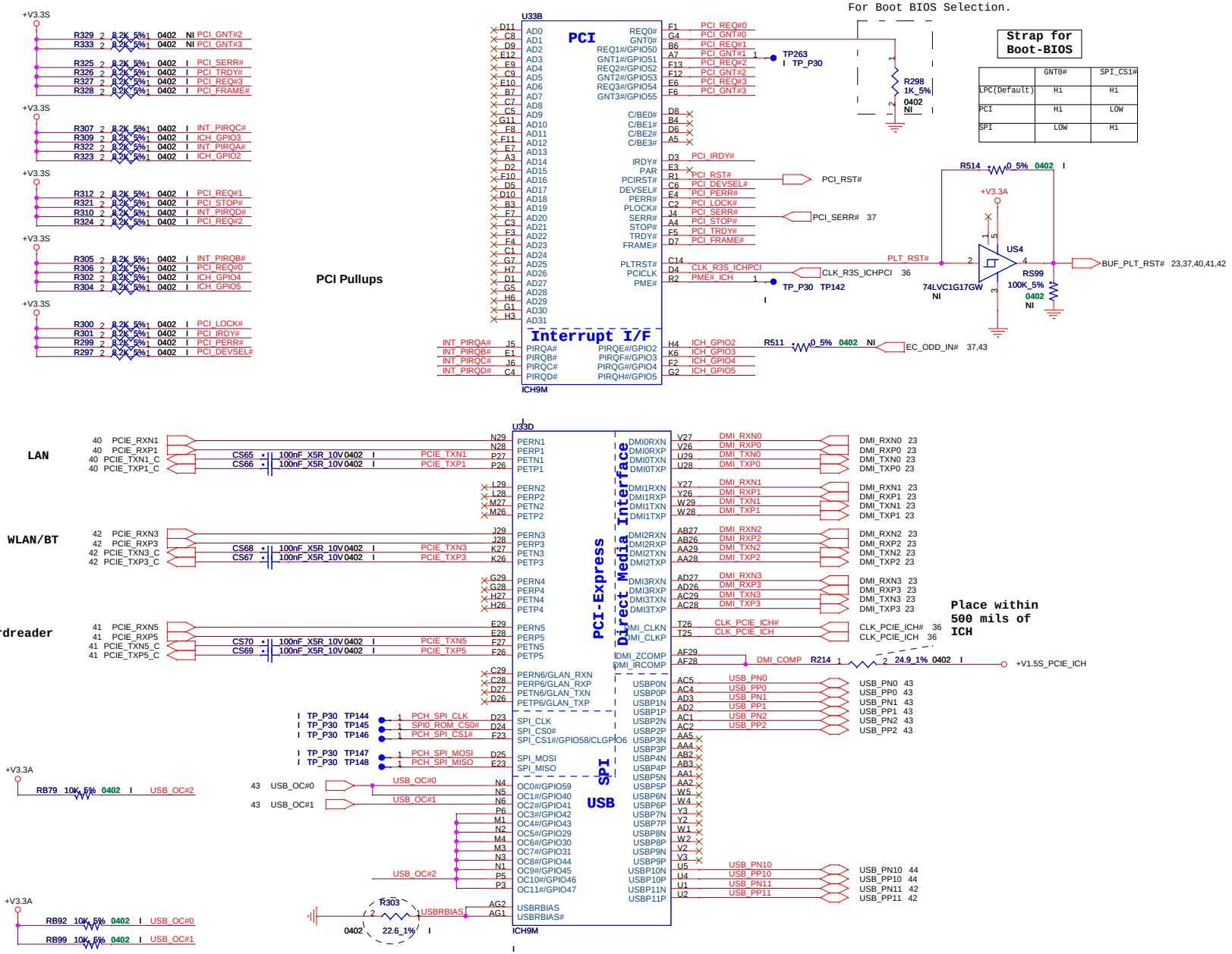


| USB PORT | Function | OC pin |
|---|---|---|
| PORT-0 | Ext. USB 0 | |
| PORT-1 | Ext. USB 1 | |
| PORT-2 | Ext. USB 2 | |
| PORT-3 | | |
| PORT-4 | | |
| PORT-5 | | |
| PORT-6 | | |
| PORT-7 | | |
| PORT-8 | | |
| PORT-9 | | |
| PORT-10 | Camera | |
| PORT-11 | WLAN/BT | |
| PORT-12 | | |
| PORT-13 | | |

| | GNT0# | SPI_CS1# |
|---|---|---|
| LPC(Default) | Hi | Hi |
| PCI | Hi | LOW |
| SPI | LOW | Hi |

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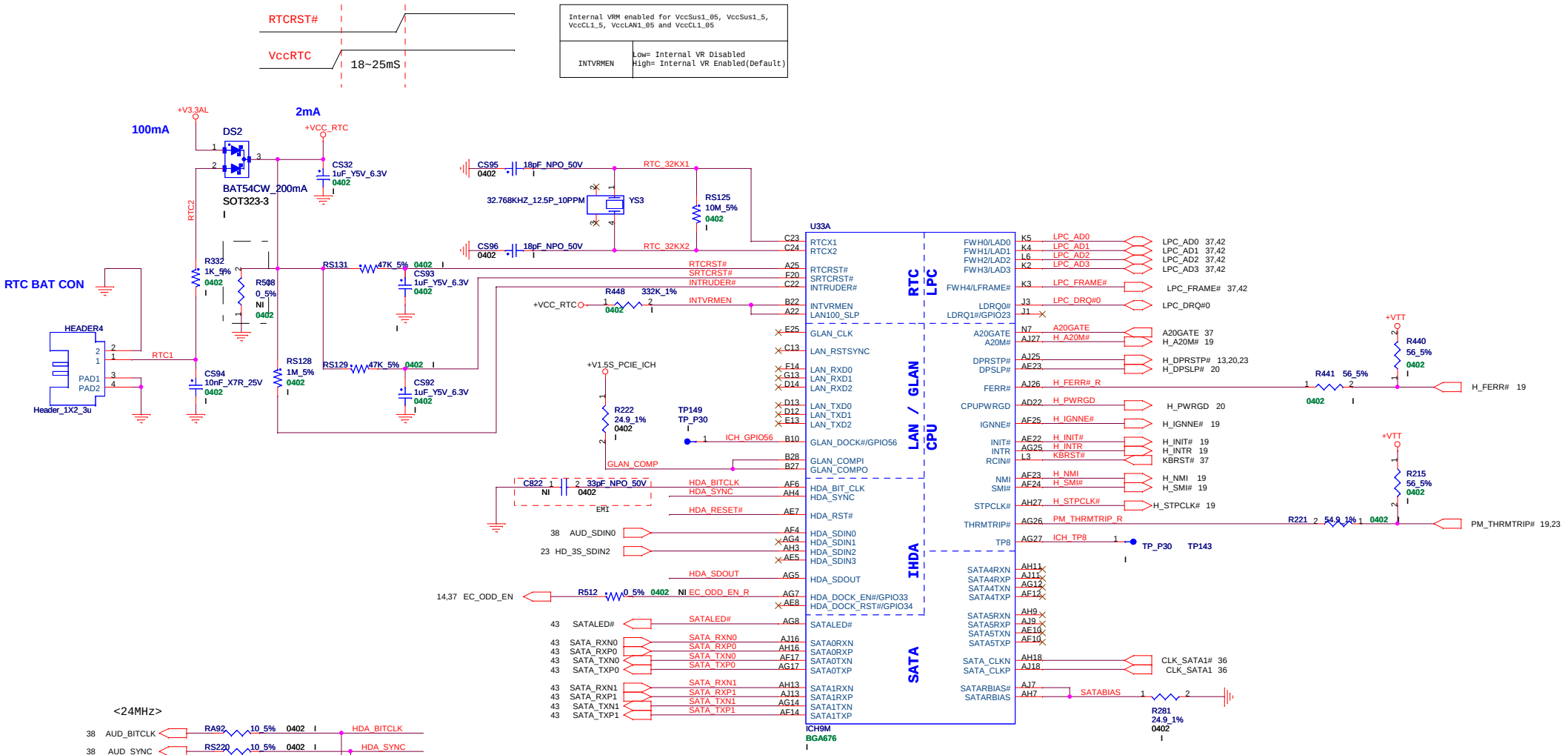


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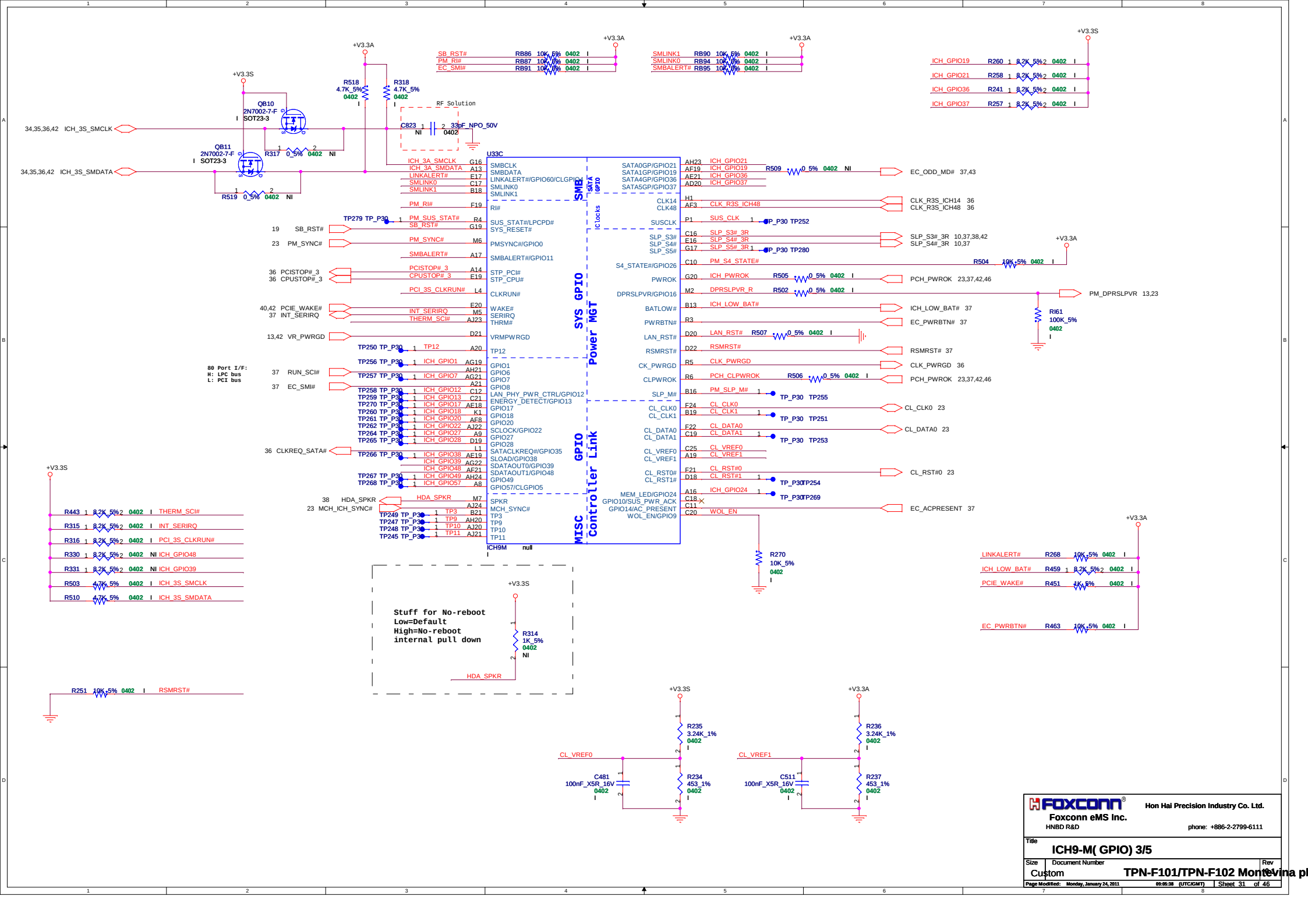


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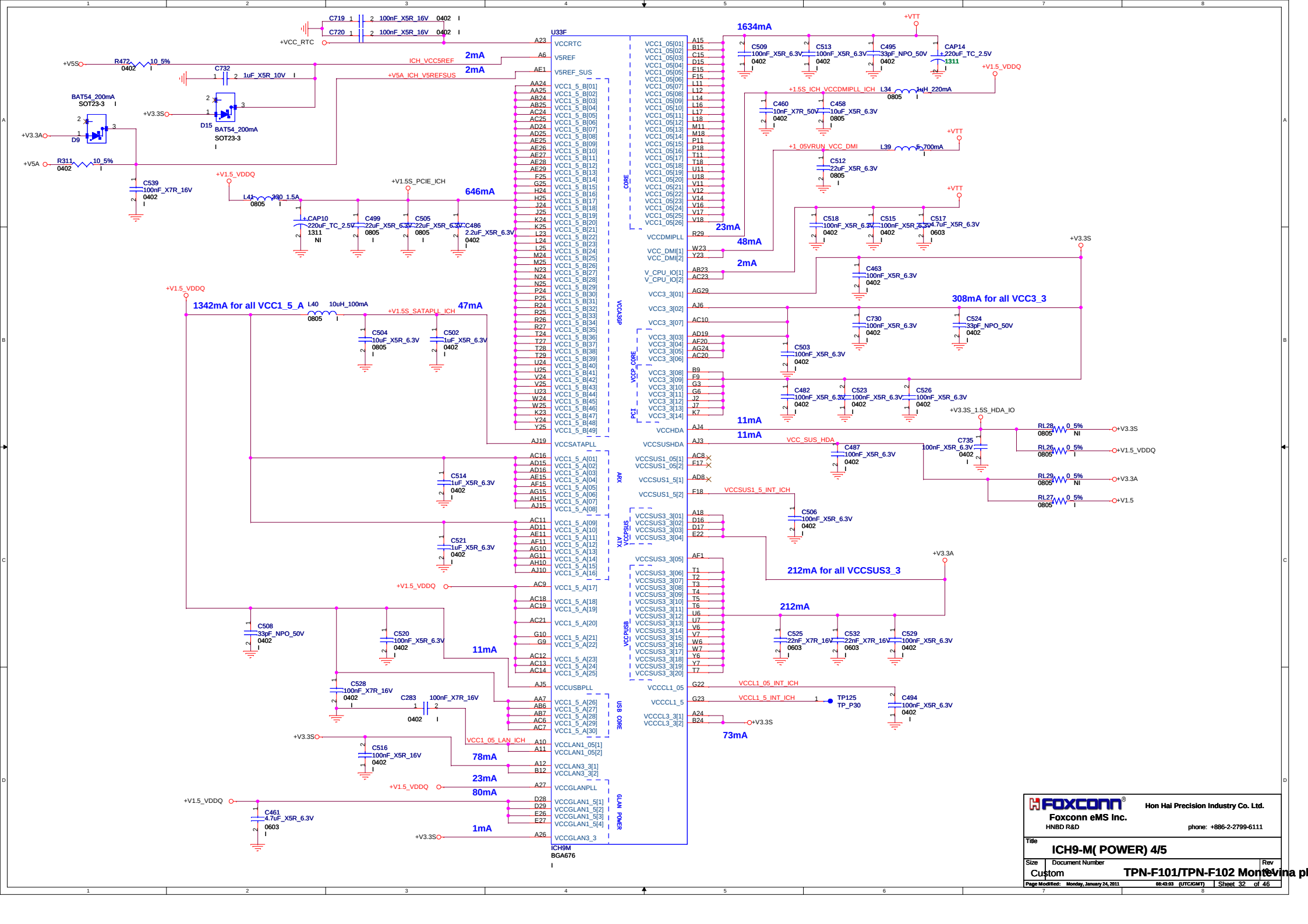


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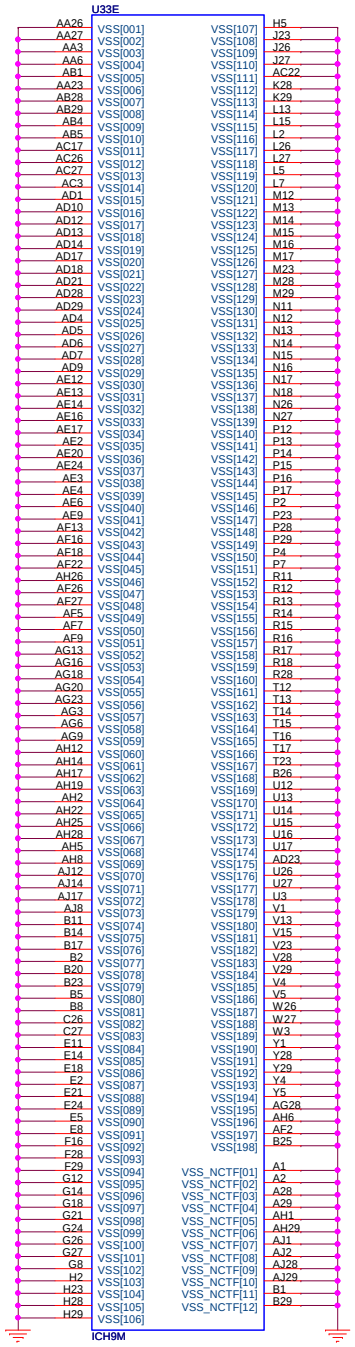


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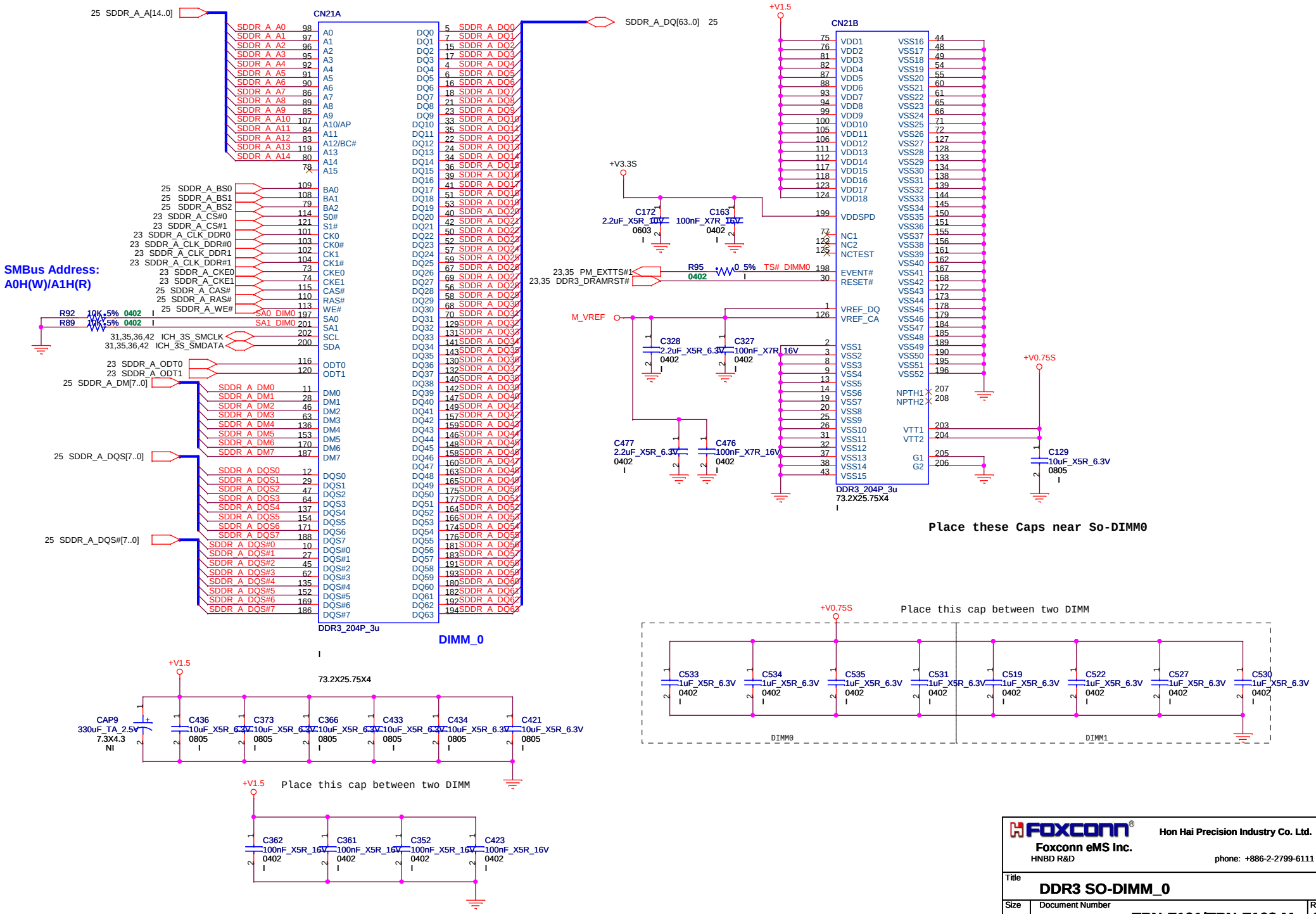
| Page Modified: Monday, January 24, 2011 08:43:02 (UTC/GMT) | Sheet 33 of 46 | |

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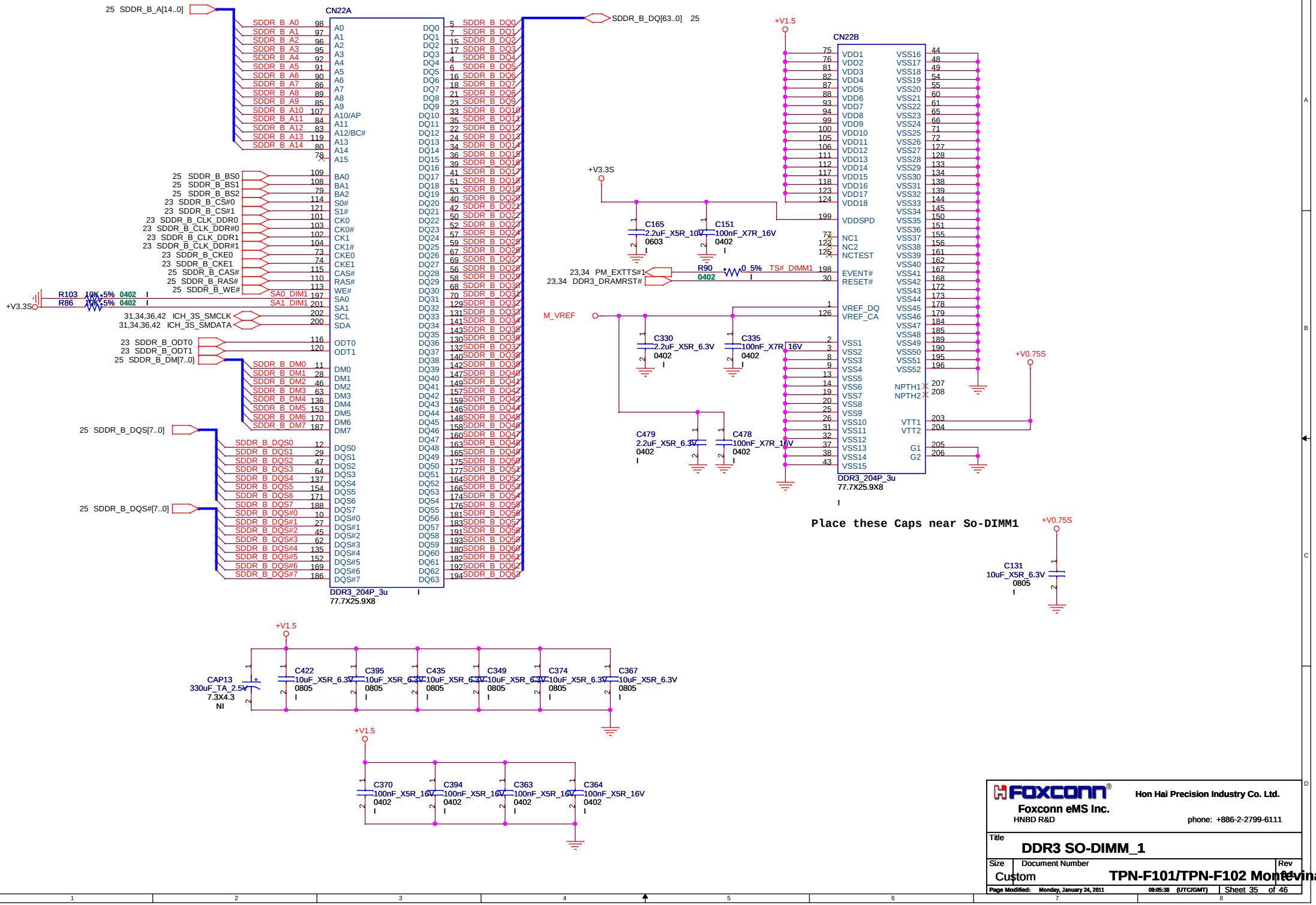


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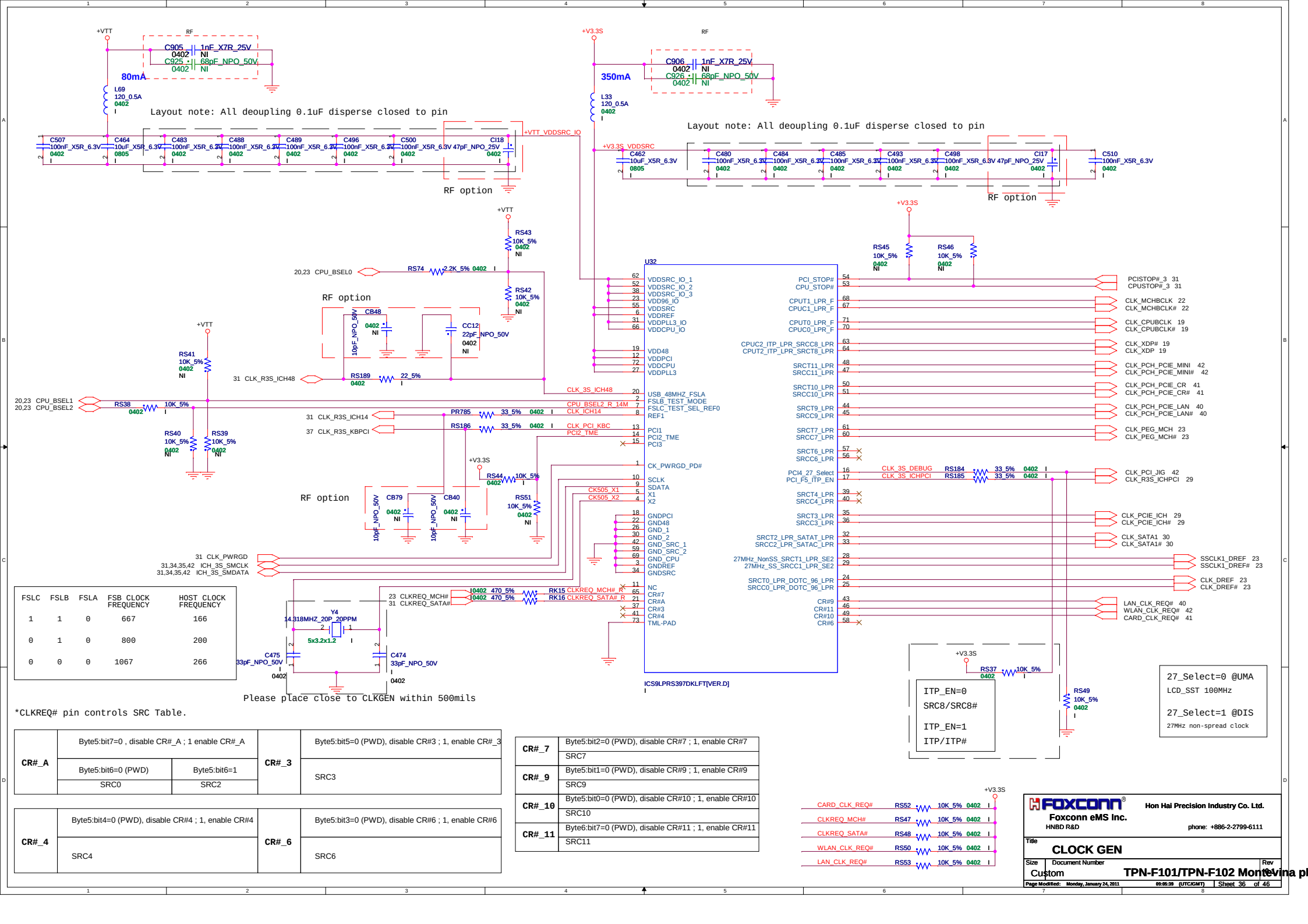


| FSLC | FSLB | FSLA | FSB CLOCK FREQUENCY | HOST CLOCK FREQUENCY |
|---|---|---|---|---|
| 1 | 1 | 0 | 667 | 166 |
| 0 | 1 | 0 | 800 | 200 |
| 0 | 0 | 0 | 1067 | 266 |

*CLKREQ# pin controls SRC Table.

| | | | | |
|---|---|---|---|---|
| **CR#_A** | Byte5:bit7=0 , disable CR#_A ; 1 enable CR#_A | | **CR#_3** | Byte5:bit5=0 (PWD), disable CR#3 ; 1, enable CR#_3 |
| | Byte5:bit6=0 (PWD) | Byte5:bit6=1 | | SRC3 |
| | SRC0 | SRC2 | | |

| | | | | |
|---|---|---|---|---|
| **CR#_4** | Byte5:bit4=0 (PWD), disable CR#4 ; 1, enable CR#4 | | **CR#_6** | Byte5:bit3=0 (PWD), disable CR#6 ; 1, enable CR#6 |
| | SRC4 | | | SRC6 |

| | |
|---|---|
| **CR#_7** | Byte5:bit2=0 (PWD), disable CR#7 ; 1, enable CR#7 |
| | SRC7 |
| **CR#_9** | Byte5:bit1=0 (PWD), disable CR#9 ; 1, enable CR#9 |
| | SRC9 |
| **CR#_10** | Byte5:bit0=0 (PWD), disable CR#10 ; 1, enable CR#10 |
| | SRC10 |
| **CR#_11** | Byte6:bit7=0 (PWD), disable CR#11 ; 1, enable CR#11 |
| | SRC11 |


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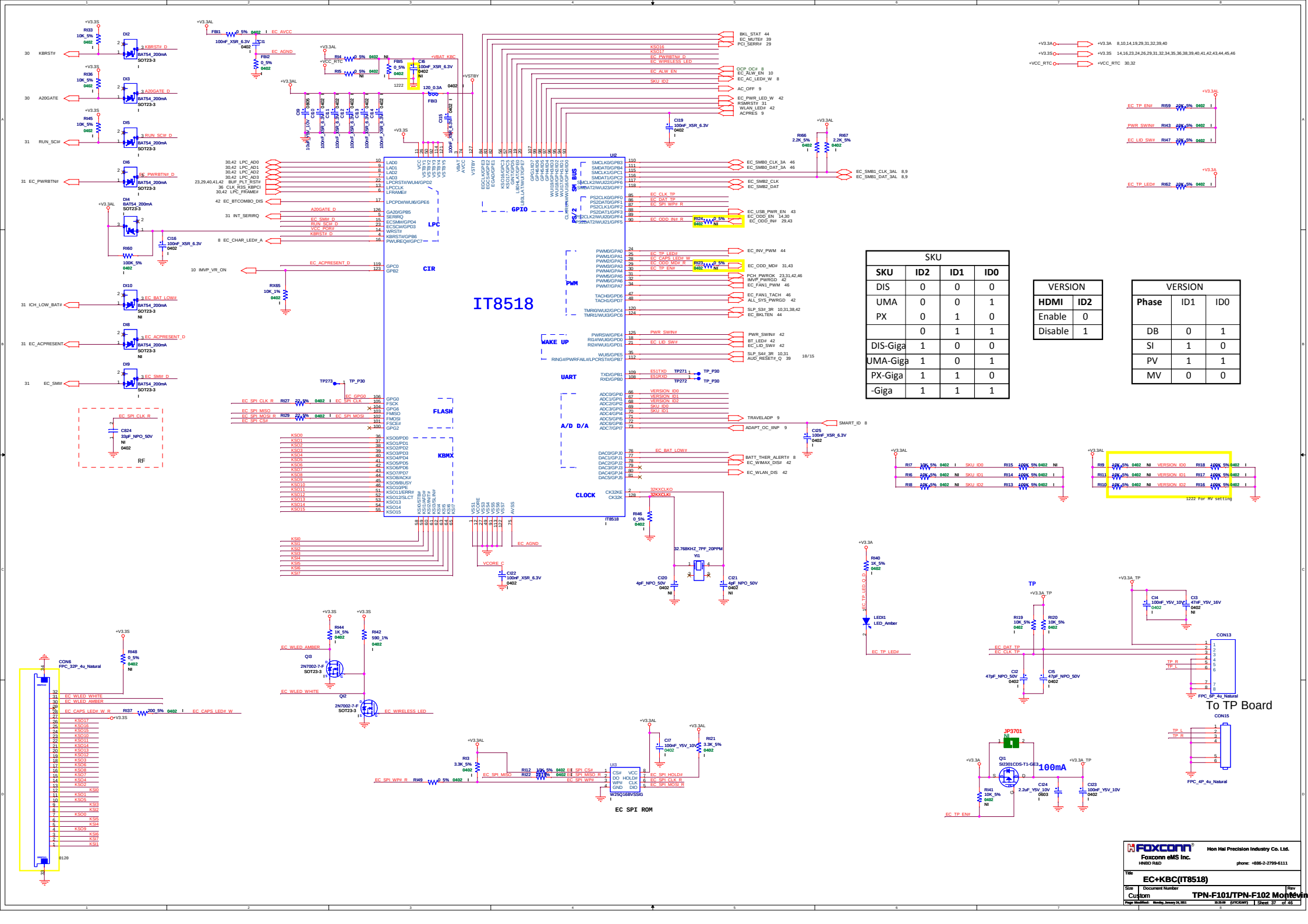
IT8518
SKU
SKU ID2 ID1 ID0
DIS 0 0 0
UMA 0 0 1
PX 0 1 0
0 1 1
DIS-Giga 1 0 0
UMA-Giga 1 0 1
PX-Giga 1 1 0
-Giga 1 1 1
VERSION
HDMI ID2
Enable 0
Disable 1
VERSION
Phase ID1 ID0
DB 0 1
SI 1 0
PV 1 1
MV 0 0
LPC
FWH
CIR
GPIO
SMB BUS
PS/2
PWM
WAKE UP
UART
A/D D/A
FLASH
KBMX
CLOCK
RF
EC SPI ROM
To TP Board
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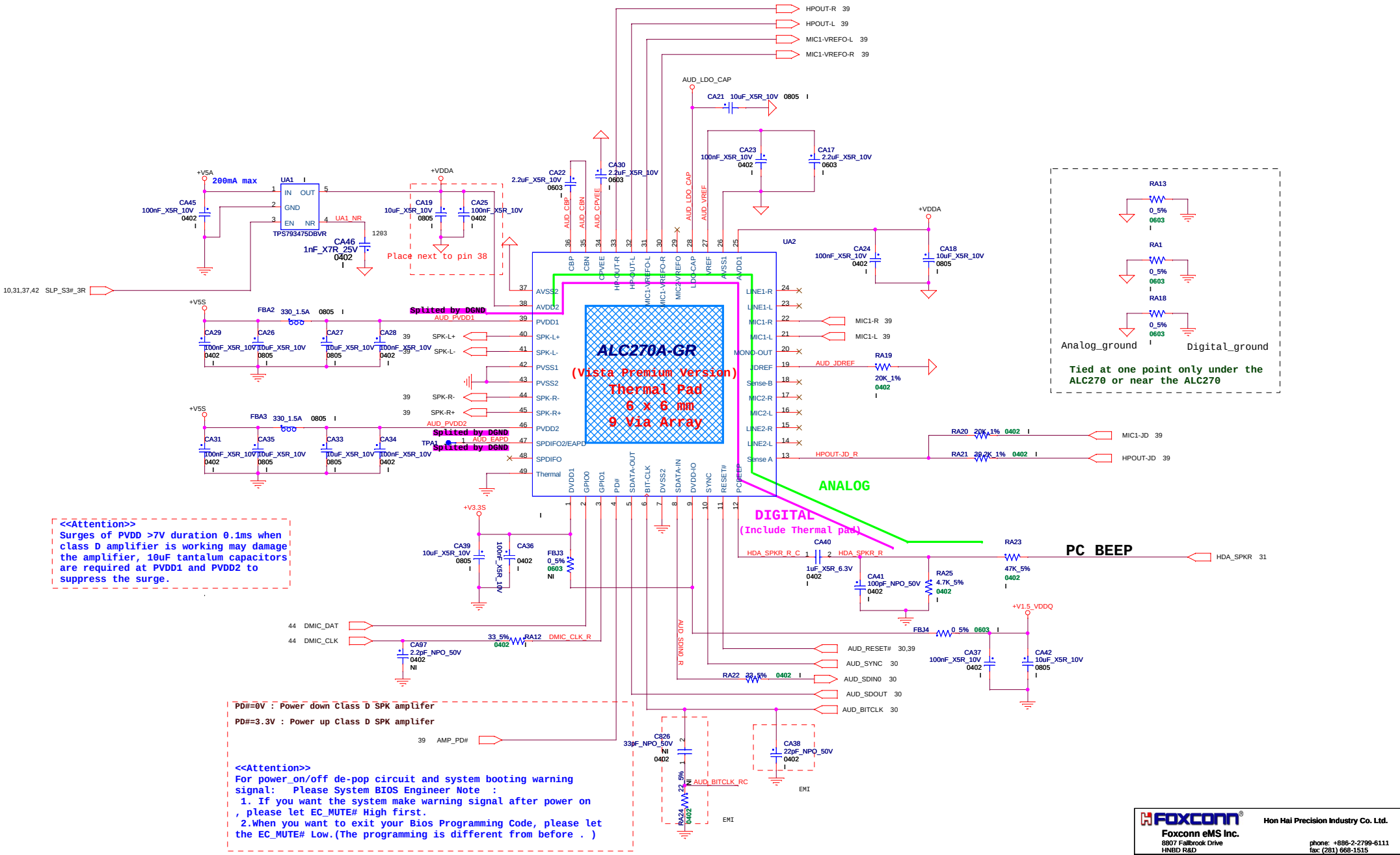
EC+KBC(IT8518)
Custom
TPN-F101/TPN-F102 Monkey
Sheet 37 of 46

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| Rev: 0.1 | |
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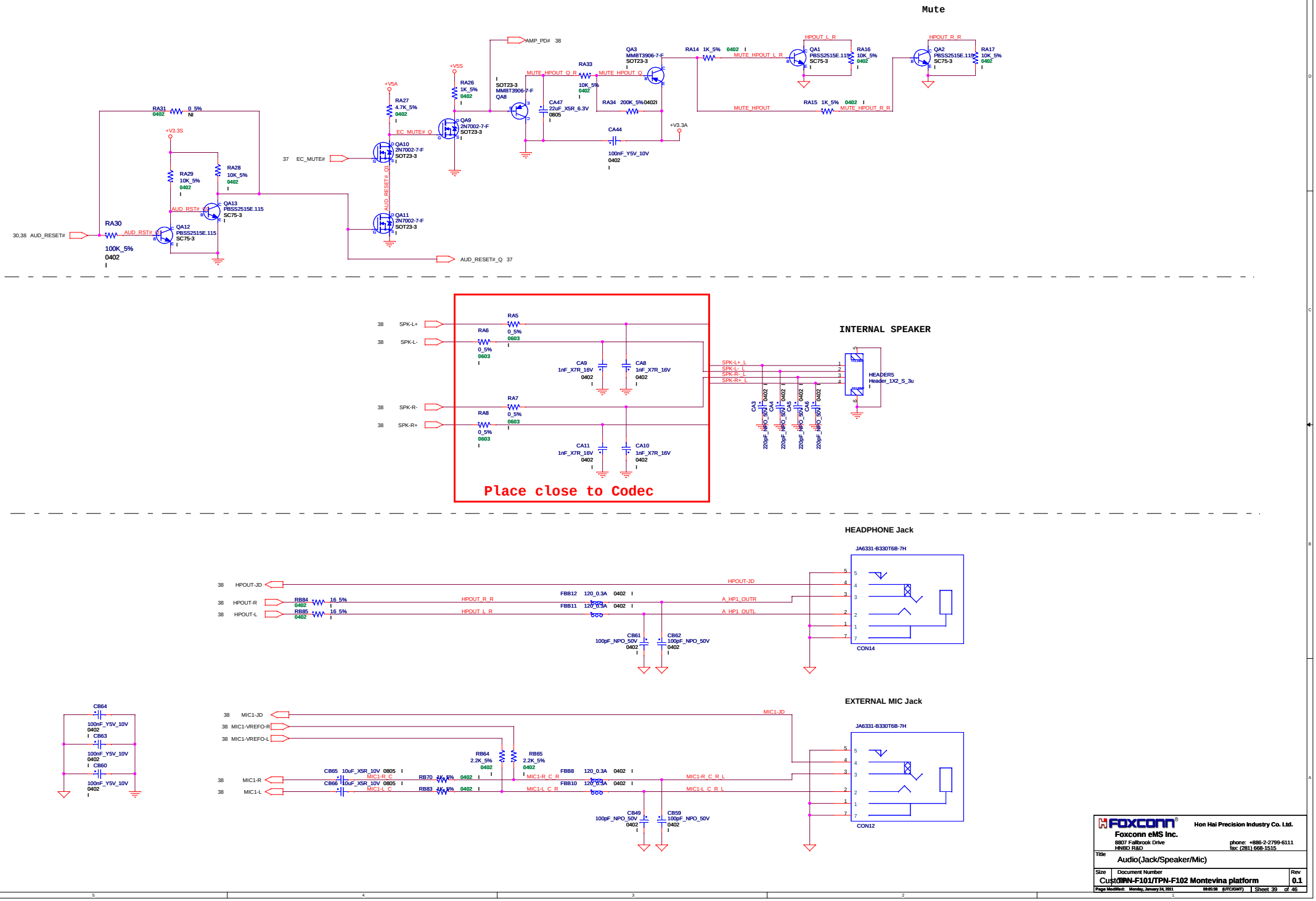


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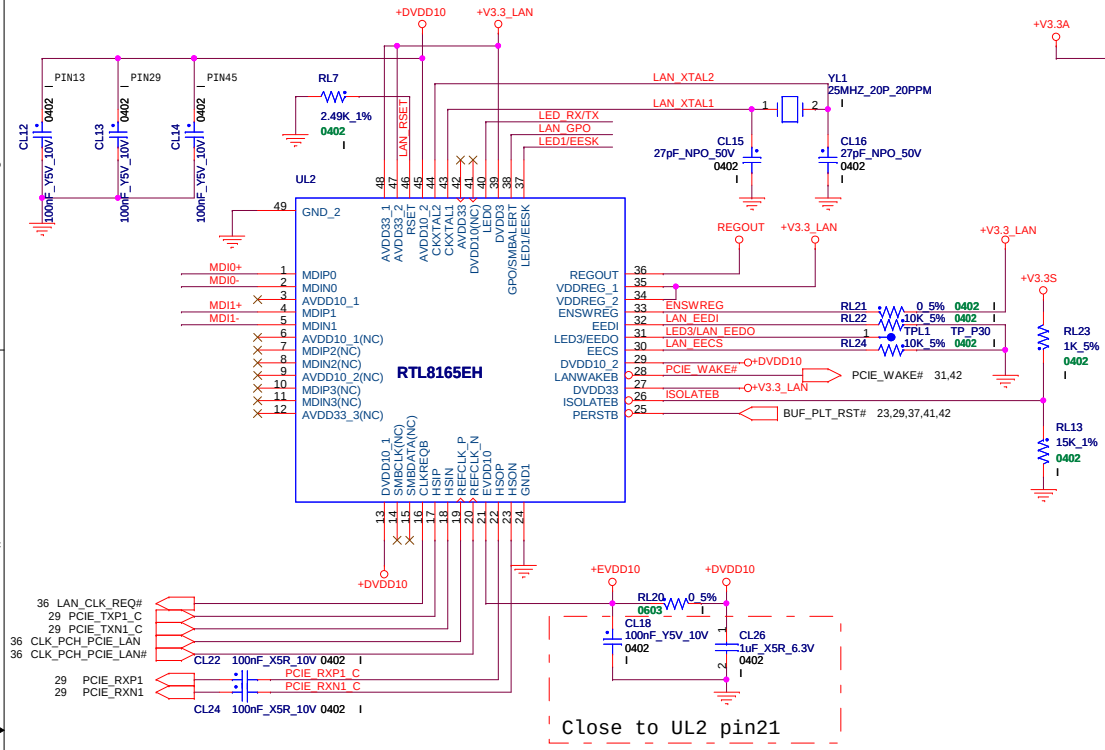
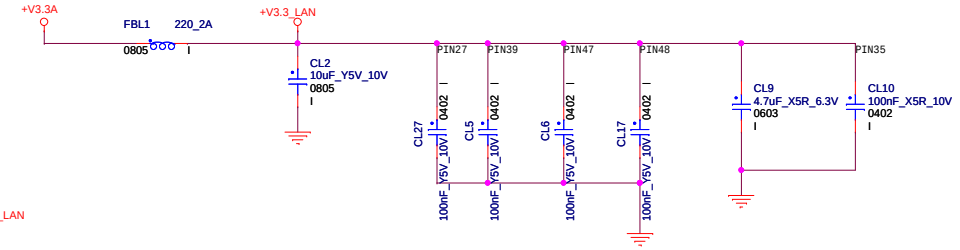
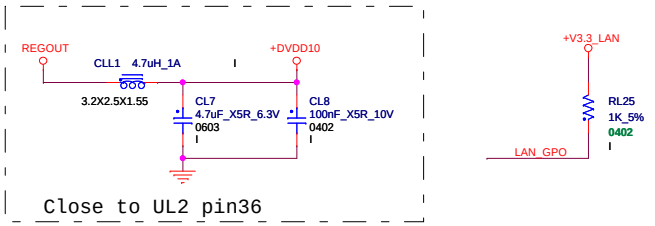
| Title | Audio(Jack/Speaker/Mic) |
| Size | Document Number: Custom TPN-F101/TPN-F102 Montevina platform |
| Rev | 0.1 |
| Page Modified: Monday, January 24, 2011 09:45:38 (UTC/GMT) | Sheet 39 of 46 |



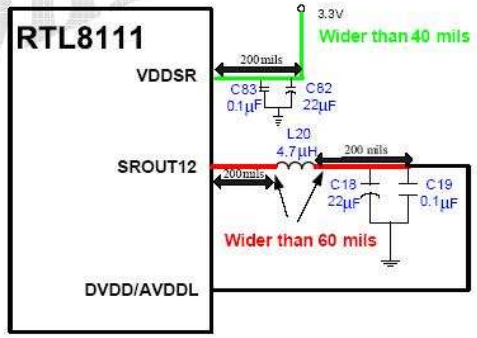



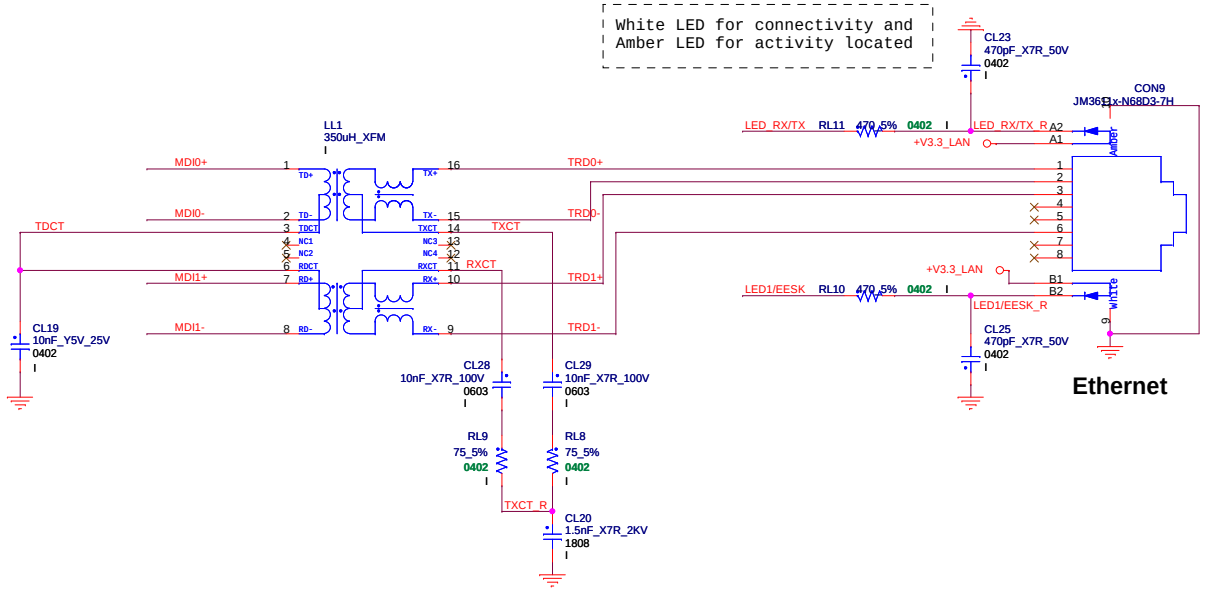




## 7.1. PCB Layout

- The input 3.3V power trace connected to the VDDSR pin should be wider than 40mils.
- The bulk de-coupling capacitors (C82 and C83) should be placed within 200mils (0.5cm) of the VDDSR pin to prevent input voltage overshoot.
- The output power trace out of the SROUT12 pin should be wider than 60mils.
- Keep L20 within 200mils (0.5cm) of the SROUT12 pin.
- Keep C18 and C19 within 200mils (0.5cm) of L20 to ensure stable output power and better power efficiency.
- Both C18 and C82 are strongly recommended to be ceramic capacitors.

*Note: Violation of the above rules will damage the IC.*



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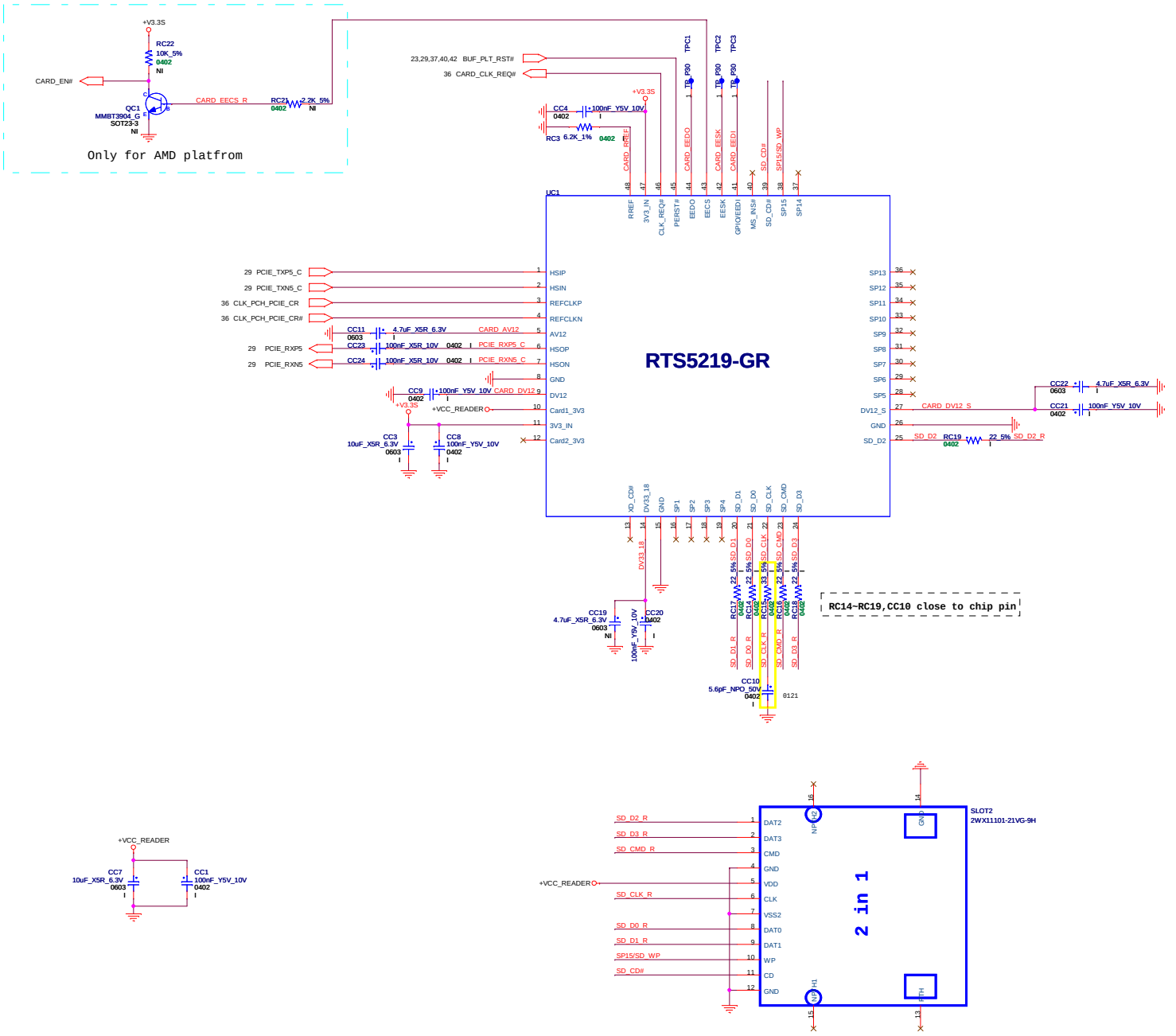


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| Size / Document Number | Custom TPN-F101/TPN-F102 Montevina platform |
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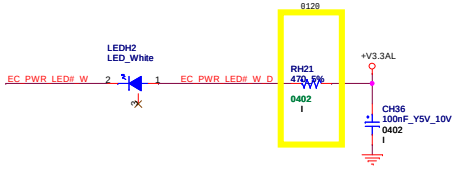
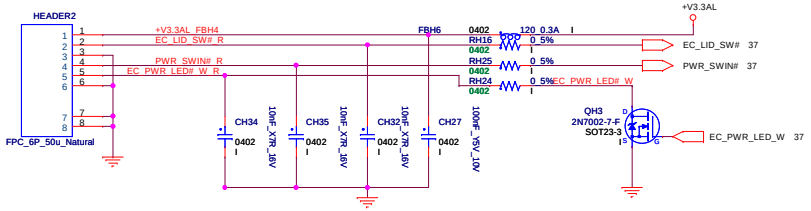
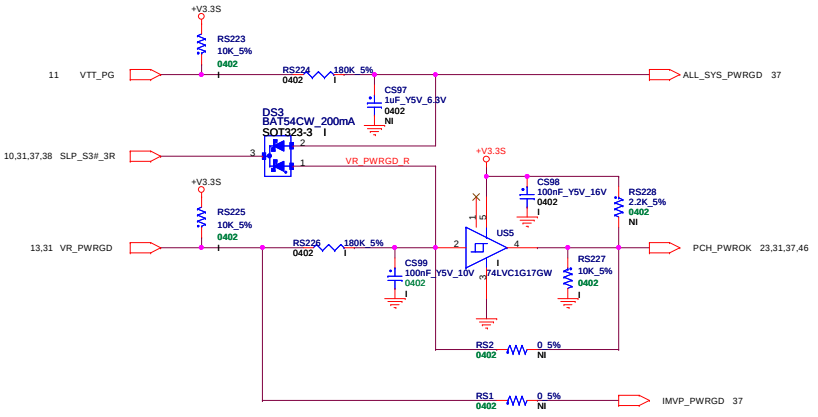


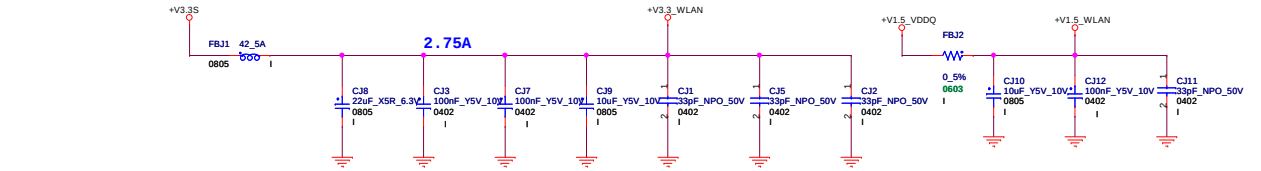

## PWR LED

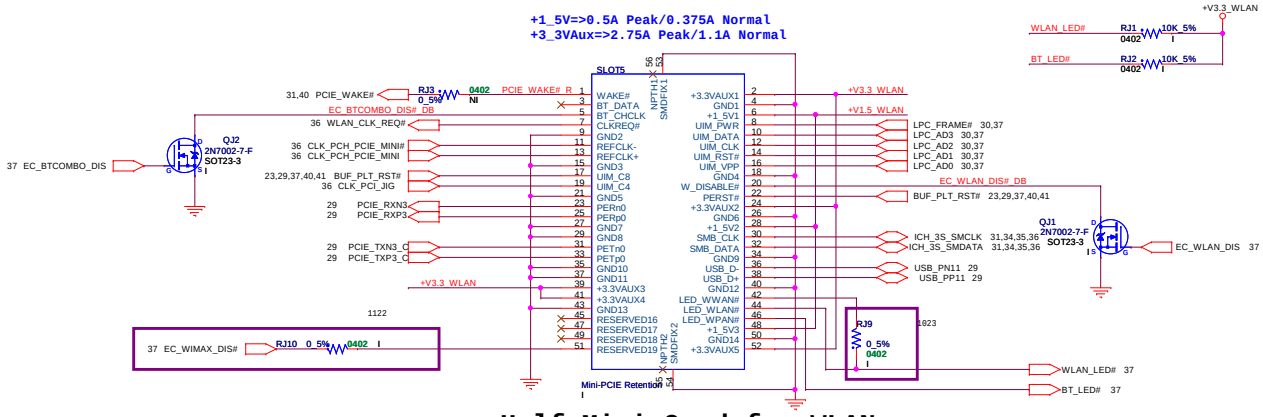



## PWR Board CONN.

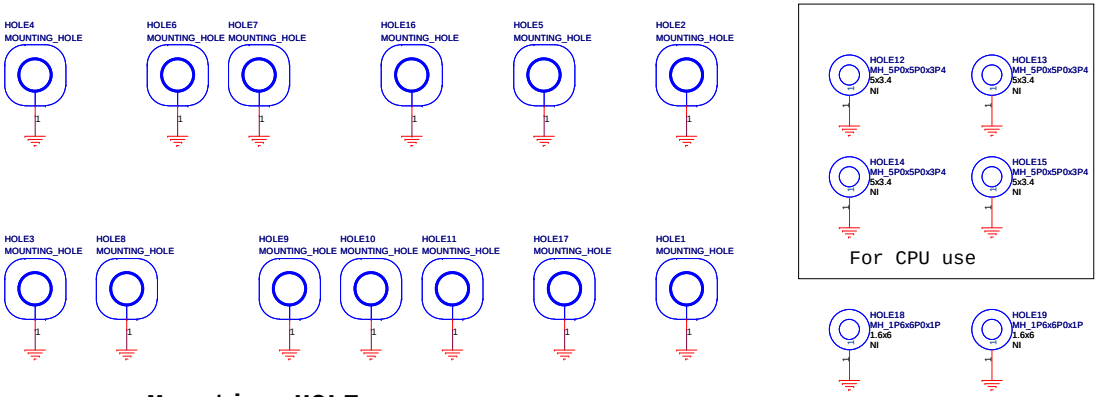



## SEQUENCE CIRCULT

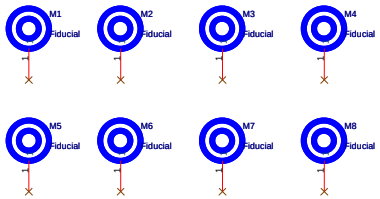



## Half Mini Card for WLAN




## Mounting HOLE




## Fiducial Mark

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| Custom | Rev: 0.1 |
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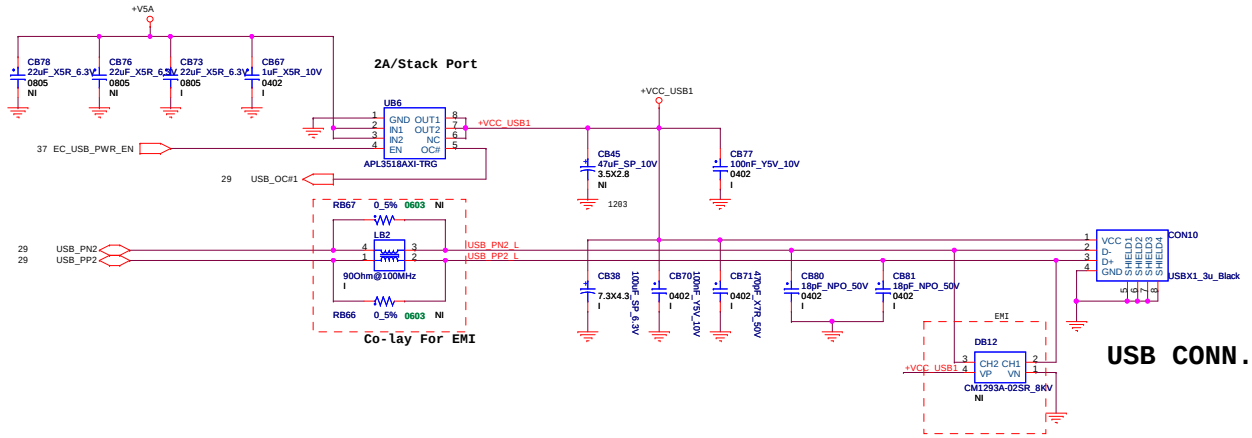
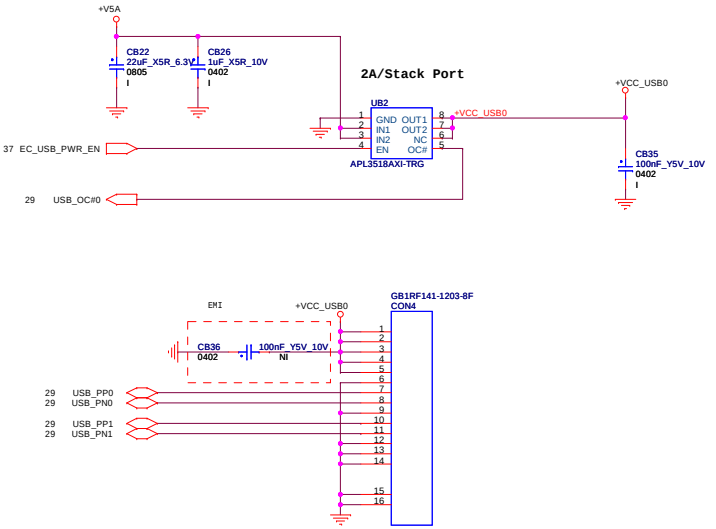
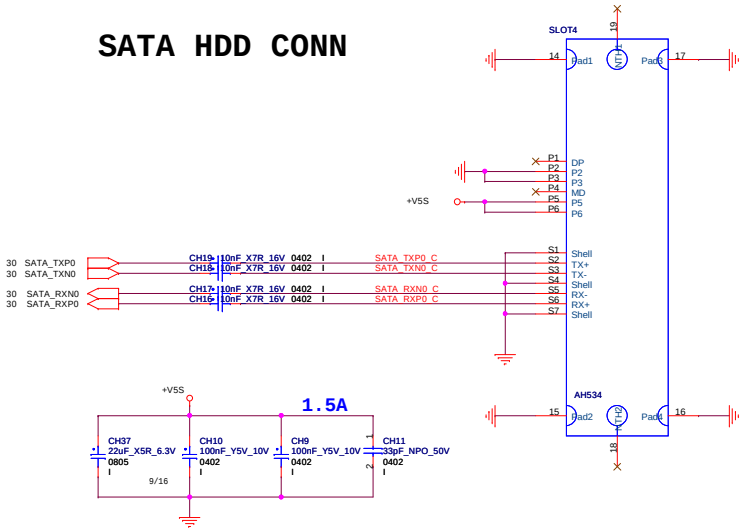
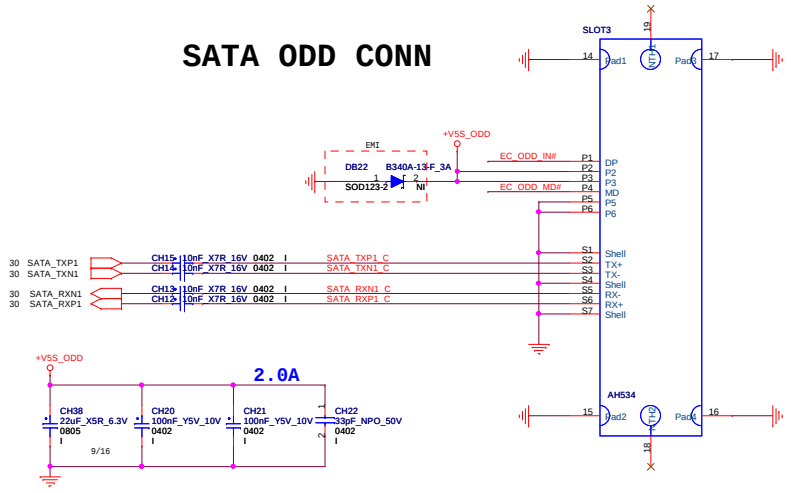
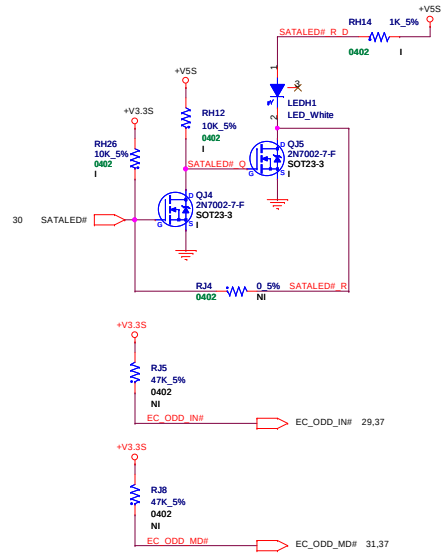



Power pin current
max. 1300 mA (less 2ms)

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| Size | Document Number: Custom TPN-F101/TPN-F102 Montevina platform |
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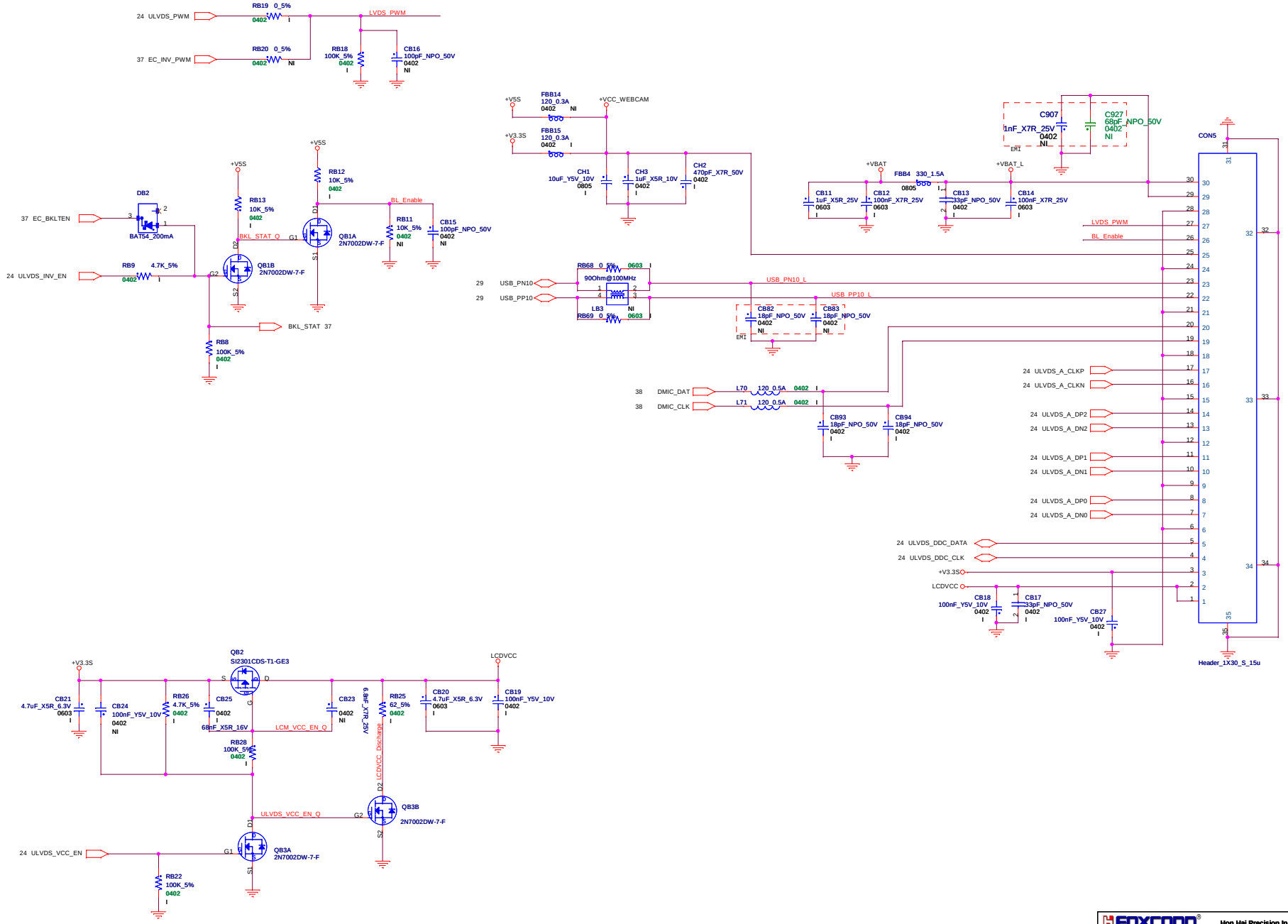
| Page Modified: Monday, January 24, 2011 09:05:38 (UTC/GMT) | Sheet 43 of 46 |

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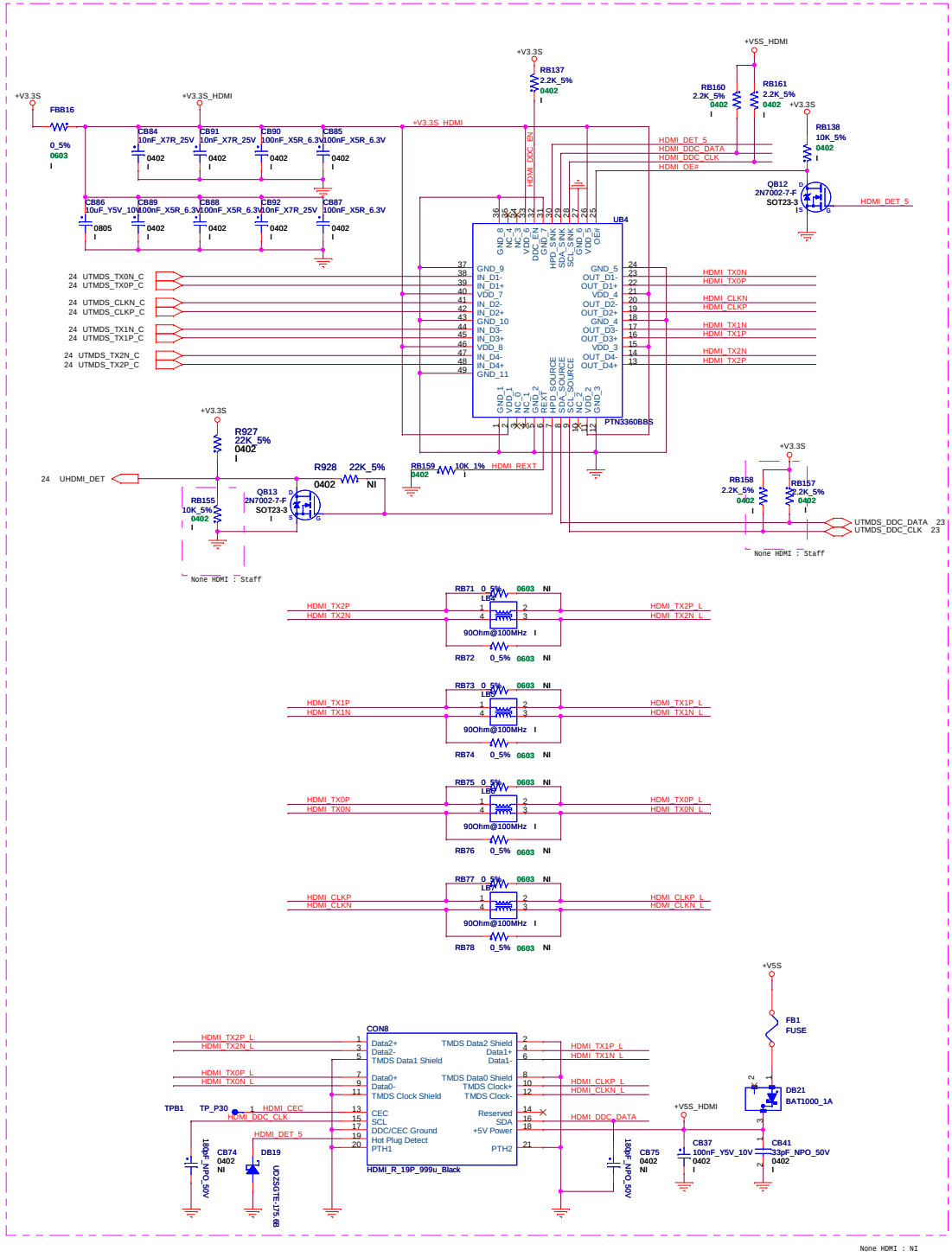
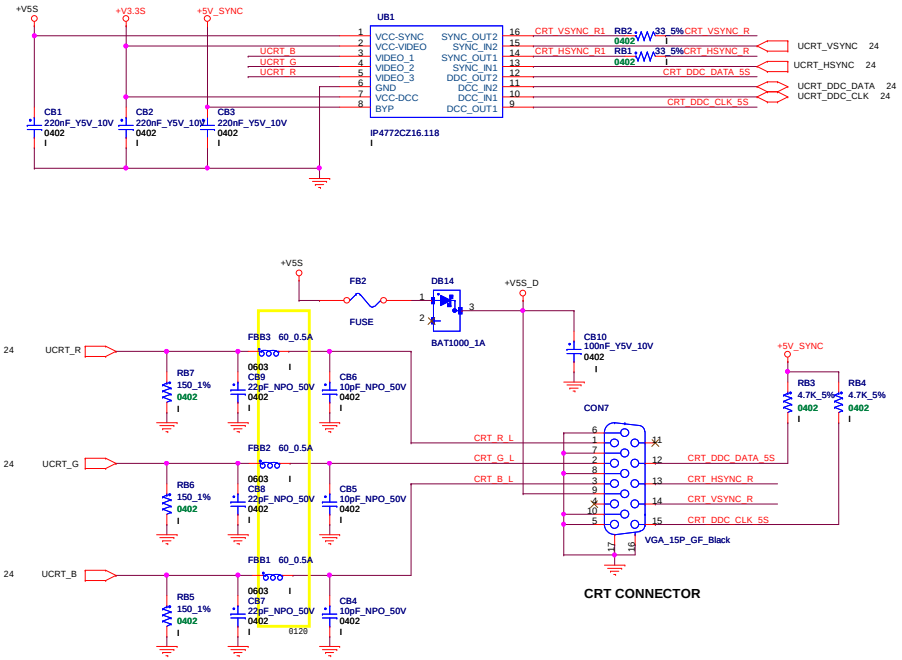



# CRT







CRT CONNECTOR

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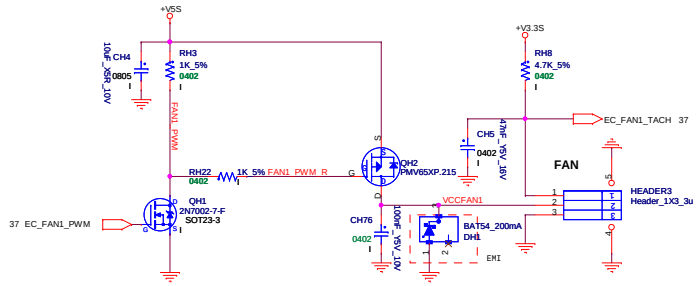
## FAN

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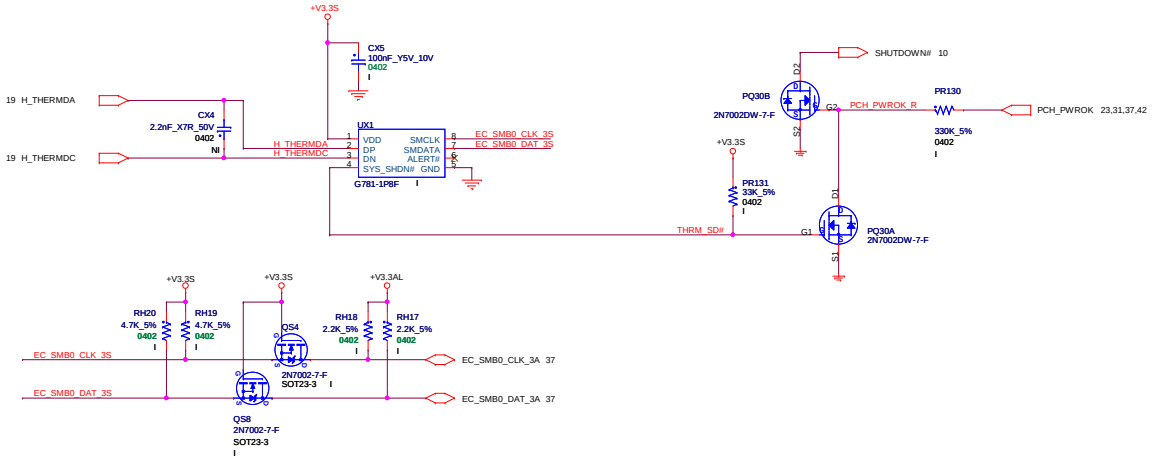
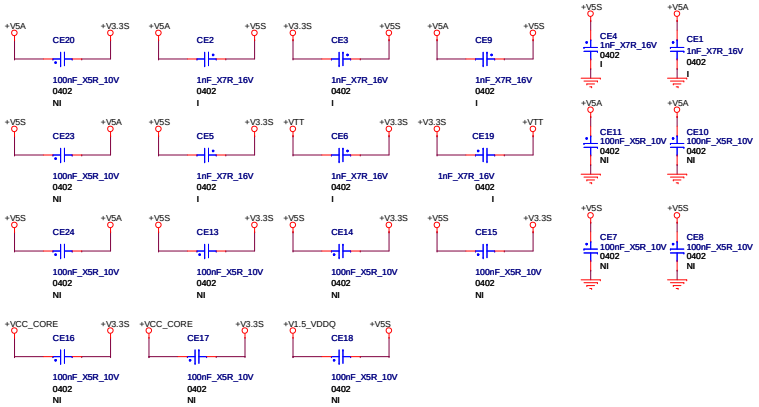



## stitch cap




## RF Solution

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