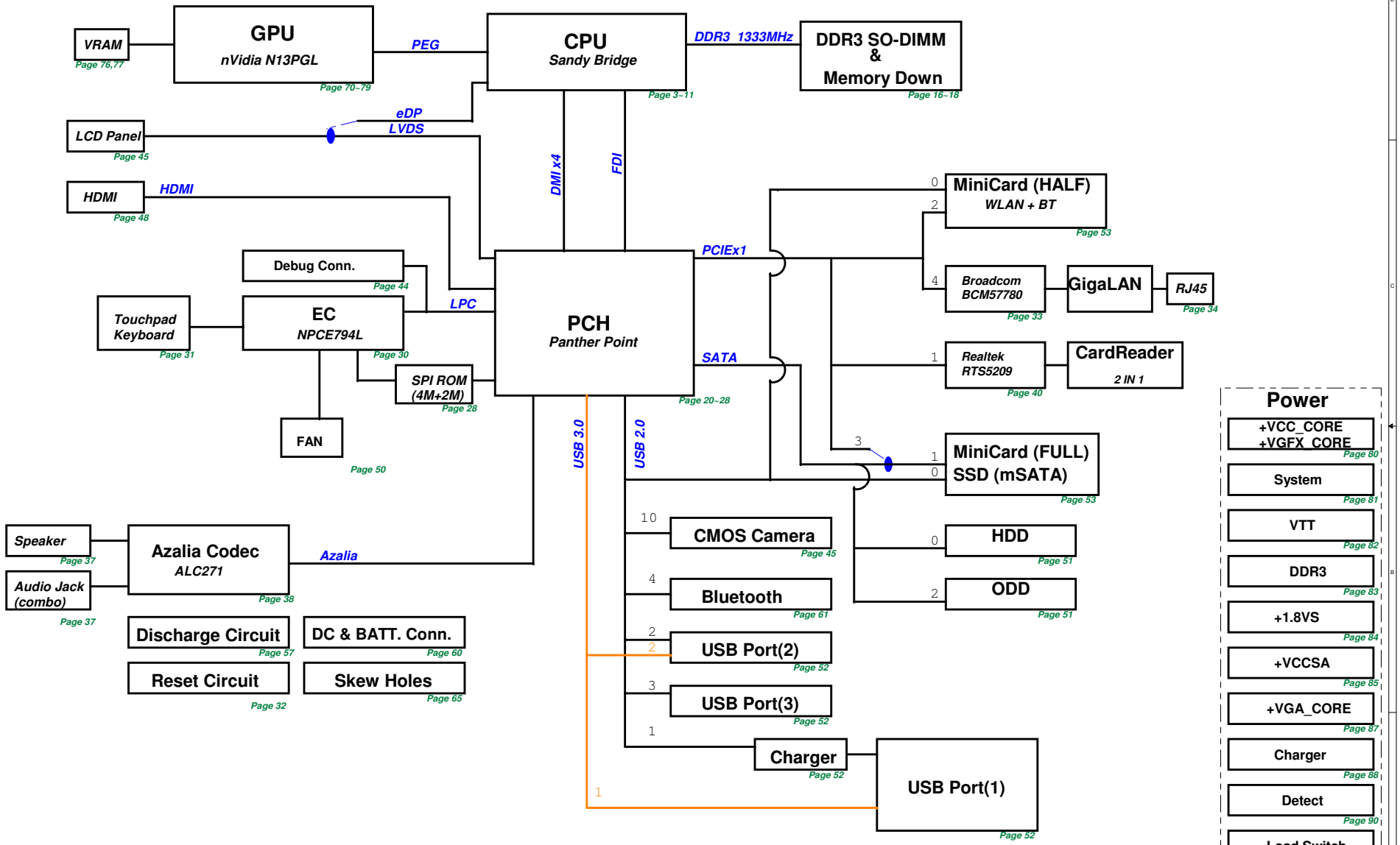
MA50 Ultrabook Block Diagram Rev 1.0



PEGATRON Title : Block Diagram

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	MA50	1.0

Date: Monday, February 13, 2012 Sheet 1 of 93

PCH_CPT GPIO

PCH_CPT GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power
GPIO 00				
GPIO 01				
GPIO [2:5]				
GPIO 06				
GPIO 07				
GPIO 08				
GPIO 09				
GPIO 10				
GPIO 11				
GPIO 12				
GPIO 13				
GPIO 14				
GPIO 15				
GPIO 16				
GPIO 17				
GPIO 18				
GPIO 19				
GPIO 20				
GPIO 21				
GPIO 22				
GPIO 23				
GPIO 24				
GPIO 25				
GPIO 26				
GPIO 27				
GPIO 28				
GPIO 29				
GPIO 30				
GPIO 31				
GPIO 32				
GPIO 33				
GPIO 34				
GPIO 35				
GPIO 36				
GPIO 37				
GPIO 38				
GPIO 39				
GPIO 40				
GPIO 41				
GPIO 42				
GPIO 43				
GPIO 44				
GPIO 45				
GPIO 46				
GPIO 47				
GPIO 48				
GPIO 49				
GPIO 50				
GPIO 51				
GPIO 52				
GPIO 53				
GPIO 54				
GPIO 55				
GPIO 56				
GPIO 57				
GPIO 58				
GPIO 59				
GPIO 60				
GPIO 61				
GPIO 62				
GPIO 63				
GPIO 64				
GPIO 65				
GPIO 66				
GPIO 67				
GPIO 72				
GPIO 73				
GPIO 74				
GPIO 75				

EC NPCE795L

EC GPIO	Use As	Signal Name
GPA0		
GPA1		
GPA2		
GPA3		
GPA4		
GPA5		
GPA6		
GPA7		
GPB0		
GPB1		
GPB2		
GPB3		
GPB4		
GPB5		
GPB6		
GPB7		
GPC0		
GPC1		
GPC2		
GPC3		
GPC4		
GPC5		
GPC6		
GPC7		
GPD0		
GPD1		
GPD2		
GPD3		
GPD4		
GPD5		
GPD6		
GPD7		
GPE0		
GPE1		
GPE2		
GPE3		
GPE4		
GPE5		
GPE6		
GPE7		
GPF0		
GPF1		
GPF2		
GPF3		
GPF4		
GPF5		
GPF6		
GPF7		
GPG0		
GPG1		
GPG2		
GPG6		
GPH0		
GPH1		
GPH2		
GPH3		
GPH4		
GPH5		
GPH6		
GPI0		
GPI1		
GPI2		
GPI3		
GPI4		
GPI5		
GPI6		
GPI7		
GPJ0		
GPJ1		
GPJ2		
GPJ3		
GPJ4		
GPJ5		

SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
SO-DIMM 0	1010000x (A0h)
SO-DIMM 1	1010001x (A4h)

PCIE 1	N/A
PCIE 2	Minicard WLAN
PCIE 3	N/A
PCIE 4	USB3.0
PCIE 5	N/A
PCIE 6	GLAN
PCIE 7	N/A
PCIE 8	N/A

SATA0	SATA HDD
SATA1	N/A
SATA2	SATA ODD
SATA3	N/A
SATA4	N/A
SATA5	N/A

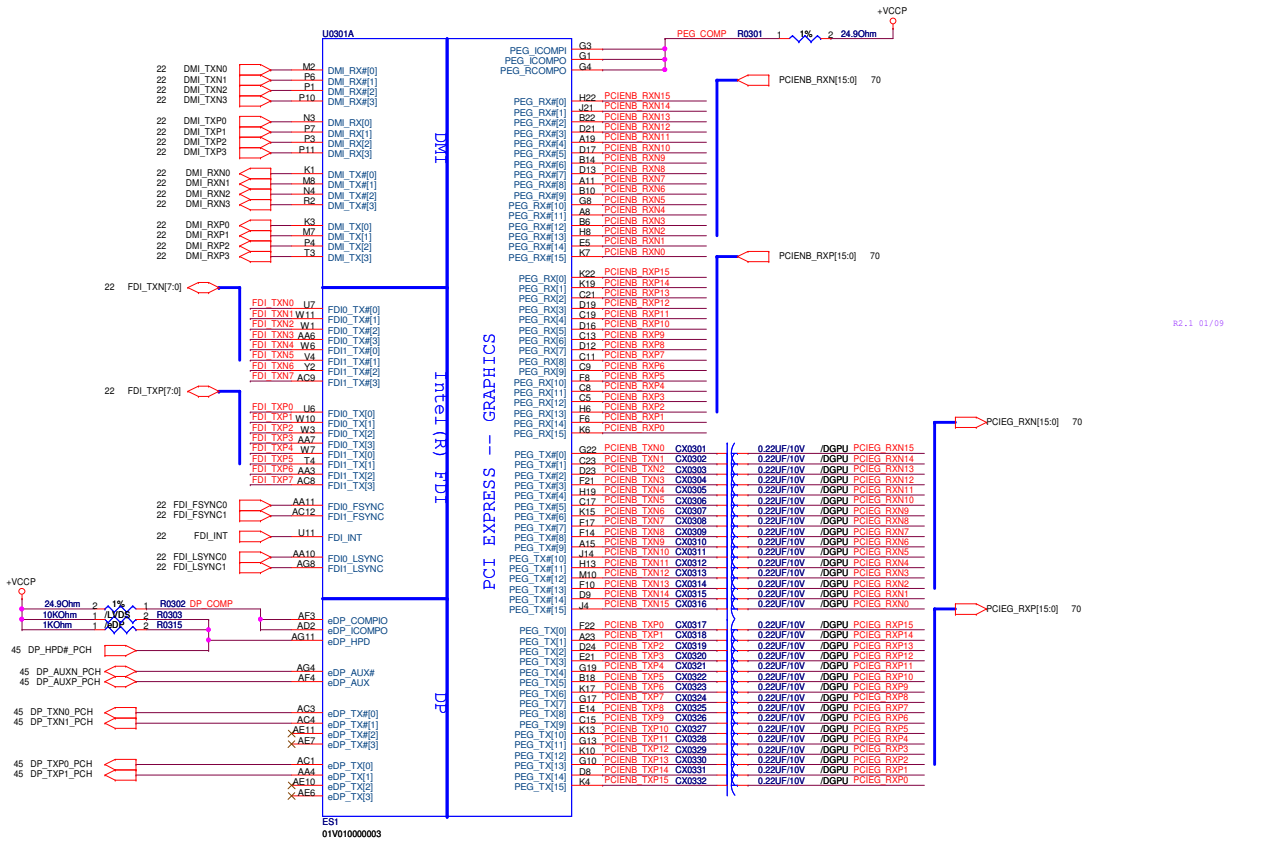
USB 0	USB Port (1)
USB 1	USB Port (2)
USB 2	USB 3.0 Port (3)
USB 3	USB Port (4)
USB 4	N/A
USB 5	N/A
USB 6	N/A
USB 7	N/A
USB 8	CMOS Camera
USB 9	WLAN
USB 10	Card Reader
USB 11	N/A
USB 12	N/A
USB 13	N/A

PEGATRON Title : System Setting

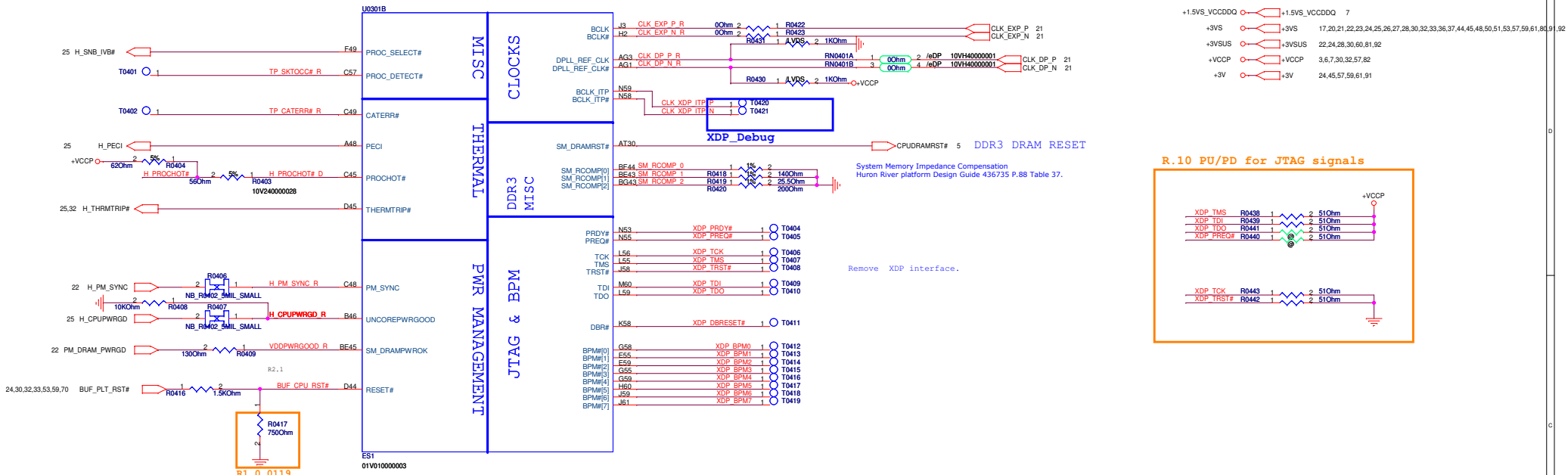
BG1-HW RD Div.2-NB RD Dept.5 Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	MA50	1.0

Date: Monday, February 13, 2012 Sheet 2 of 93



PEGATRON	Title : CPU(1)_DMI,DP,PEG,FDI		
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Joyoung_Chianhg		
Size: C	Project Name: MA50	Rev: 1.0	
Date: Monday, February 13, 2012	Sheet 3 of 93		

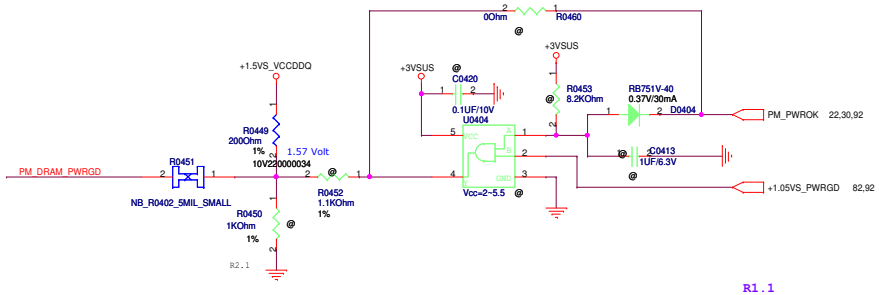


R1.0 0119
Sandy Bridge:R0417 = 750 ohm (10V220000093)
Ivy Bridge:R0417 = 680 ohm (10V240000041)

R.10 PU/PD for JTAG signals

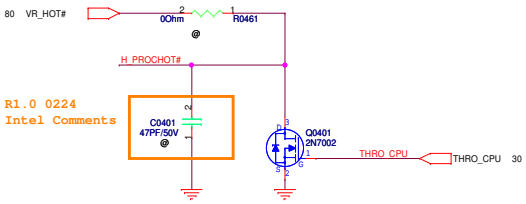
PM_SYS_PWRGD is the power good for +1.5V_VCCDDQ

Different from EVEREST



R1.1
add S3 power reduction

If support S3 power reduction with power good.
1. Mount U0404, D0404, C0413, C0420, R0450, R0452, R0453,
   Unmount R0460
2. Change R0449 to 1kohm from 200ohm, change R0409 to 0ohm from 130ohm - Design Guide 1.0 page 106



R1.0 0224
Intel Comments

PEGATRON	Title : CPU(2)_CLK,MISC,JTAG		
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Joyoung_Chianhg		
Size: C	Project Name: MA50	Rev: 1.0	
Date: Monday, February 13, 2012	Sheet 4 of 93		

+1.5V +1.5V 16,17,18,57,60,83

+1.5V +1.5V 16,17,18,57,60,83

U0301C

DDR SYSTEM MEMORY A

16 M_A_DQ[63:0]

M_A_DQ0 AG6 SA_DQ[0]
M_A_DQ1 AJ6 SA_DQ[1]
M_A_DQ2 AP11 SA_DQ[2]
M_A_DQ3 AL6 SA_DQ[3]
M_A_DQ4 AJ10 SA_DQ[4]
M_A_DQ5 AJ8 SA_DQ[5]
M_A_DQ6 AL8 SA_DQ[6]
M_A_DQ7 AL7 SA_DQ[7]
M_A_DQ8 AR11 SA_DQ[8]
M_A_DQ9 AP6 SA_DQ[9]
M_A_DQ10 AU6 SA_DQ[10]
M_A_DQ11 AV9 SA_DQ[11]
M_A_DQ12 AR6 SA_DQ[12]
M_A_DQ13 AP8 SA_DQ[13]
M_A_DQ14 AT13 SA_DQ[14]
M_A_DQ15 AU13 SA_DQ[15]
M_A_DQ16 BC7 SA_DQ[16]
M_A_DQ17 BB7 SA_DQ[17]
M_A_DQ18 BA13 SA_DQ[18]
M_A_DQ19 BB11 SA_DQ[19]
M_A_DQ20 BA7 SA_DQ[20]
M_A_DQ21 BA9 SA_DQ[21]
M_A_DQ22 BB9 SA_DQ[22]
M_A_DQ23 AY13 SA_DQ[23]
M_A_DQ24 AV14 SA_DQ[24]
M_A_DQ25 AR14 SA_DQ[25]
M_A_DQ26 AY17 SA_DQ[26]
M_A_DQ27 AR19 SA_DQ[27]
M_A_DQ28 BA14 SA_DQ[28]
M_A_DQ29 AU14 SA_DQ[29]
M_A_DQ30 BB14 SA_DQ[30]
M_A_DQ31 BB17 SA_DQ[31]
M_A_DQ32 BA45 SA_DQ[32]
M_A_DQ33 AR43 SA_DQ[33]
M_A_DQ34 AW48 SA_DQ[34]
M_A_DQ35 BC48 SA_DQ[35]
M_A_DQ36 BC45 SA_DQ[36]
M_A_DQ37 AR45 SA_DQ[37]
M_A_DQ38 AT48 SA_DQ[38]
M_A_DQ39 AY48 SA_DQ[39]
M_A_DQ40 BA49 SA_DQ[40]
M_A_DQ41 AV49 SA_DQ[41]
M_A_DQ42 BB51 SA_DQ[42]
M_A_DQ43 AY53 SA_DQ[43]
M_A_DQ44 BB49 SA_DQ[44]
M_A_DQ45 AU49 SA_DQ[45]
M_A_DQ46 BA53 SA_DQ[46]
M_A_DQ47 BB55 SA_DQ[47]
M_A_DQ48 BA55 SA_DQ[48]
M_A_DQ49 AV56 SA_DQ[49]
M_A_DQ50 AP50 SA_DQ[50]
M_A_DQ51 AP53 SA_DQ[51]
M_A_DQ52 AV54 SA_DQ[52]
M_A_DQ53 AT54 SA_DQ[53]
M_A_DQ54 AP56 SA_DQ[54]
M_A_DQ55 AP52 SA_DQ[55]
M_A_DQ56 AN57 SA_DQ[56]
M_A_DQ57 AN53 SA_DQ[57]
M_A_DQ58 AG56 SA_DQ[58]
M_A_DQ59 AG53 SA_DQ[59]
M_A_DQ60 AN55 SA_DQ[60]
M_A_DQ61 AN52 SA_DQ[61]
M_A_DQ62 AG55 SA_DQ[62]
M_A_DQ63 AK56 SA_DQ[63]

SA_CK[0] AU36 M_A_DIM0_CLK_DDR0 16
SA_CK#[0] AV36 M_A_DIM0_CLK_DDR#0 16
SA_CKE[0] AY26 M_A_DIM0_CKE0 16

SA_CK[1] AT40 T0501
SA_CK#[1] AU40 T0502
SA_CKE[1] BB26 T0503

SA_CS#[0] BB40 M_A_DIM0_CS#0 16
SA_CS#[1] BC41

SA_ODT[0] AY40 M_A_DIM0_ODT0 16
SA_ODT[1] BA41

SA_DQS#[0] AL11 M_A_DQS#0
SA_DQS#[1] AR8 M_A_DQS#1
SA_DQS#[2] AV11 M_A_DQS#2
SA_DQS#[3] AT17 M_A_DQS#3
SA_DQS#[4] AV45 M_A_DQS#4
SA_DQS#[5] AY51 M_A_DQS#5
SA_DQS#[6] AT56 M_A_DQS#6
SA_DQS#[7] AK55 M_A_DQS#7
M_A_DQS#[7:0] 16

SA_DQS[0] AJ11 M_A_DQS0
SA_DQS[1] AR10 M_A_DQS1
SA_DQS[2] AY11 M_A_DQS2
SA_DQS[3] AU17 M_A_DQS3
SA_DQS[4] AW45 M_A_DQS4
SA_DQS[5] AV51 M_A_DQS5
SA_DQS[6] AT56 M_A_DQS6
SA_DQS[7] AK54 M_A_DQS7
M_A_DQS[7:0] 16

SA_MA[0] BG35 M_A_A0
SA_MA[1] BB34 M_A_A1
SA_MA[2] BE35 M_A_A2
SA_MA[3] BD36 M_A_A3
SA_MA[4] AT34 M_A_A4
SA_MA[5] AU34 M_A_A5
SA_MA[6] BB32 M_A_A6
SA_MA[7] AT32 M_A_A7
SA_MA[8] AY32 M_A_A8
SA_MA[9] AV32 M_A_A9
SA_MA[10] BE37 M_A_A10
SA_MA[11] BA30 M_A_A11
SA_MA[12] BC30 M_A_A12
SA_MA[13] AW41 M_A_A13
SA_MA[14] AY28 M_A_A14
SA_MA[15] AU26 M_A_A15
M_A_A[15:0] 16

16 M_A_BS0 BD37 SA_BS[0]
16 M_A_BS1 BF36 SA_BS[1]
16 M_A_BS2 BA28 SA_BS[2]

16 M_A_CAS# BE39 SA_CAS#
16 M_A_RAS# BD39 SA_RAS#
16 M_A_WE# AT41 SA_WE#

ES1
01V010000003

U0301D

DDR SYSTEM MEMORY B

17 M_B_DQ[63:0]

M_B_DQ0 AL4 SB_DQ[0]
M_B_DQ1 AL1 SB_DQ[1]
M_B_DQ2 AN3 SB_DQ[2]
M_B_DQ3 AR4 SB_DQ[3]
M_B_DQ4 AK4 SB_DQ[4]
M_B_DQ5 AK3 SB_DQ[5]
M_B_DQ6 AN4 SB_DQ[6]
M_B_DQ7 AR1 SB_DQ[7]
M_B_DQ8 AL4 SB_DQ[8]
M_B_DQ9 AT2 SB_DQ[9]
M_B_DQ10 AV4 SB_DQ[10]
M_B_DQ11 BA4 SB_DQ[11]
M_B_DQ12 AU3 SB_DQ[12]
M_B_DQ13 AR3 SB_DQ[13]
M_B_DQ14 AY2 SB_DQ[14]
M_B_DQ15 BA3 SB_DQ[15]
M_B_DQ16 BE9 SB_DQ[16]
M_B_DQ17 BD9 SB_DQ[17]
M_B_DQ18 BD13 SB_DQ[18]
M_B_DQ19 BF12 SB_DQ[19]
M_B_DQ20 BF8 SB_DQ[20]
M_B_DQ21 BD10 SB_DQ[21]
M_B_DQ22 BD14 SB_DQ[22]
M_B_DQ23 BE13 SB_DQ[23]
M_B_DQ24 BF16 SB_DQ[24]
M_B_DQ25 BE17 SB_DQ[25]
M_B_DQ26 BE18 SB_DQ[26]
M_B_DQ27 BE21 SB_DQ[27]
M_B_DQ28 BE14 SB_DQ[28]
M_B_DQ29 BG14 SB_DQ[29]
M_B_DQ30 BG18 SB_DQ[30]
M_B_DQ31 BF19 SB_DQ[31]
M_B_DQ32 BD50 SB_DQ[32]
M_B_DQ33 BF48 SB_DQ[33]
M_B_DQ34 BD53 SB_DQ[34]
M_B_DQ35 BF52 SB_DQ[35]
M_B_DQ36 BD49 SB_DQ[36]
M_B_DQ37 BE49 SB_DQ[37]
M_B_DQ38 BD54 SB_DQ[38]
M_B_DQ39 BE53 SB_DQ[39]
M_B_DQ40 BF56 SB_DQ[40]
M_B_DQ41 BE57 SB_DQ[41]
M_B_DQ42 BC59 SB_DQ[42]
M_B_DQ43 AY60 SB_DQ[43]
M_B_DQ44 BE54 SB_DQ[44]
M_B_DQ45 BC54 SB_DQ[45]
M_B_DQ46 BA58 SB_DQ[46]
M_B_DQ47 AW59 SB_DQ[47]
M_B_DQ48 AW58 SB_DQ[48]
M_B_DQ49 AU58 SB_DQ[49]
M_B_DQ50 AN61 SB_DQ[50]
M_B_DQ51 AN59 SB_DQ[51]
M_B_DQ52 AU59 SB_DQ[52]
M_B_DQ53 AU61 SB_DQ[53]
M_B_DQ54 AN58 SB_DQ[54]
M_B_DQ55 AR58 SB_DQ[55]
M_B_DQ56 AK58 SB_DQ[56]
M_B_DQ57 AL58 SB_DQ[57]
M_B_DQ58 AG58 SB_DQ[58]
M_B_DQ59 AG59 SB_DQ[59]
M_B_DQ60 AM60 SB_DQ[60]
M_B_DQ61 AL59 SB_DQ[61]
M_B_DQ62 AF61 SB_DQ[62]
M_B_DQ63 AH60 SB_DQ[63]

SB_CK[0] BA34 M_B_DIM0_CLK_DDR0 17
SB_CK#[0] AY34 M_B_DIM0_CLK_DDR#0 17
SB_CKE[0] AR22 M_B_DIM0_CKE0 17

SB_CK[1] BA36 M_B_DIM0_CLK_DDR1 17
SB_CK#[1] BB36 M_B_DIM0_CLK_DDR#1 17
SB_CKE[1] BF27 M_B_DIM0_CKE1 17

SB_CS#[0] BE41 M_B_DIM0_CS#0 17
SB_CS#[1] BE47 M_B_DIM0_CS#1 17

SB_ODT[0] AT43 M_B_DIM0_ODT0 17
SB_ODT[1] BG47 M_B_DIM0_ODT1 17

SB_DQS#[0] AL3 M_B_DQS#0
SB_DQS#[1] AV3 M_B_DQS#1
SB_DQS#[2] BG11 M_B_DQS#2
SB_DQS#[3] BD17 M_B_DQS#3
SB_DQS#[4] BG51 M_B_DQS#4
SB_DQS#[5] BA59 M_B_DQS#5
SB_DQS#[6] AT60 M_B_DQS#6
SB_DQS#[7] AK59 M_B_DQS#7
M_B_DQS#[7:0] 17

SB_DQS[0] AM2 M_B_DQS0
SB_DQS[1] AV1 M_B_DQS1
SB_DQS[2] BE11 M_B_DQS2
SB_DQS[3] BD18 M_B_DQS3
SB_DQS[4] BE51 M_B_DQS4
SB_DQS[5] BA61 M_B_DQS5
SB_DQS[6] AR59 M_B_DQS6
SB_DQS[7] AK61 M_B_DQS7
M_B_DQS[7:0] 17

SB_MA[0] BF32 M_B_A0
SB_MA[1] BE33 M_B_A1
SB_MA[2] BD33 M_B_A2
SB_MA[3] AU30 M_B_A3
SB_MA[4] BD30 M_B_A4
SB_MA[5] AV30 M_B_A5
SB_MA[6] BG30 M_B_A6
SB_MA[7] BD29 M_B_A7
SB_MA[8] BE30 M_B_A8
SB_MA[9] BE28 M_B_A9
SB_MA[10] BD43 M_B_A10
SB_MA[11] AT28 M_B_A11
SB_MA[12] AY28 M_B_A12
SB_MA[13] BD46 M_B_A13
SB_MA[14] AT26 M_B_A14
SB_MA[15] AU22 M_B_A15
M_B_A[15:0] 17

17 M_B_BS0 BG39 SB_BS[0]
17 M_B_BS1 BD42 SB_BS[1]
17 M_B_BS2 AT22 SB_BS[2]

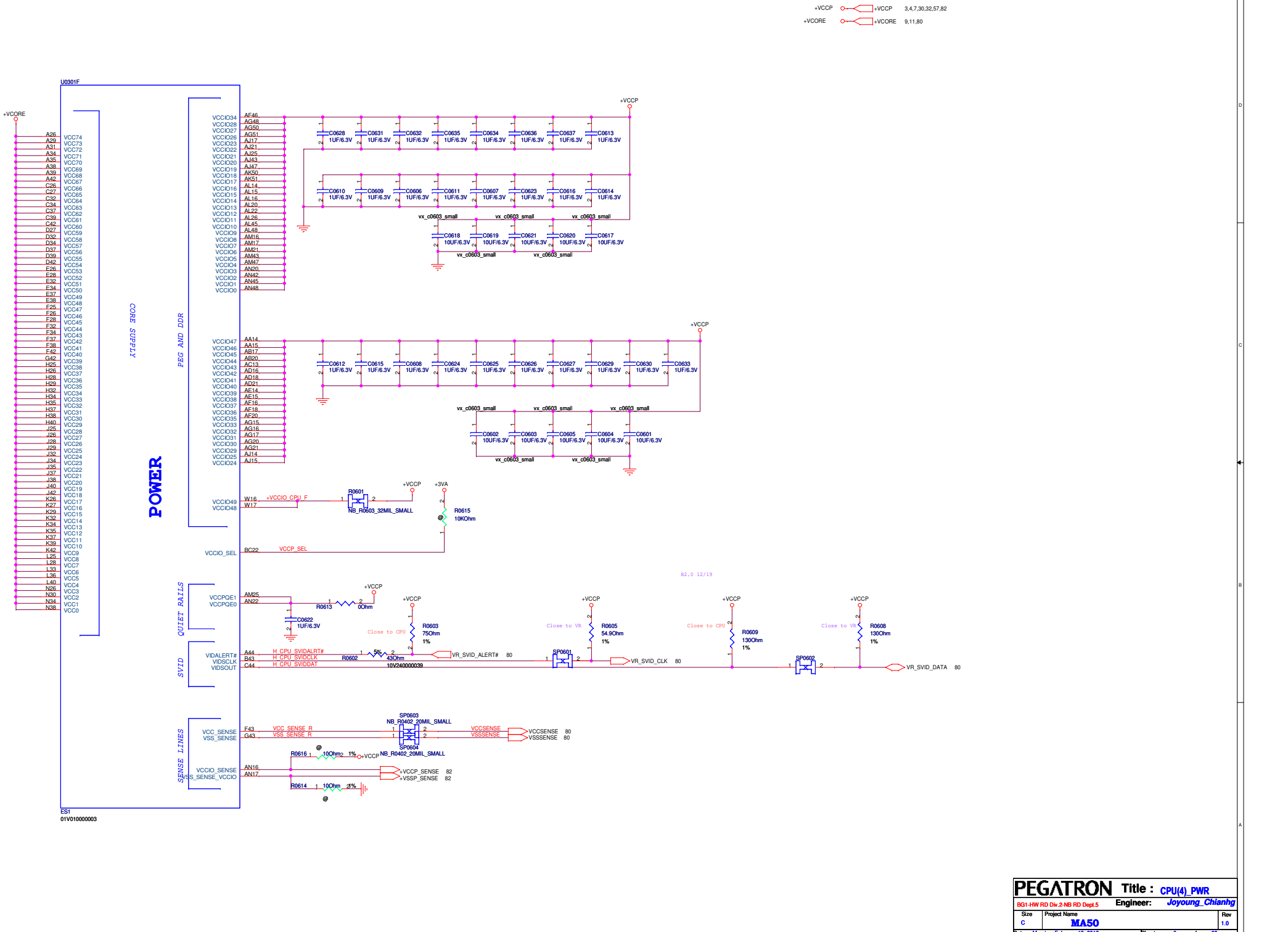
17 M_B_CAS# AV43 SB_CAS#
17 M_B_RAS# BF40 SB_RAS#
17 M_B_WE# BD45 SB_WE#

ES1
01V010000003

R1.0 S3 circuit: DRAM_RST# to memory should be high during S3
R1.1 add S3 power reduction

+1.5V
R0507 1KOhm
always support S3 PWR Reduction
Remove bypass R
Q0501 2N7002
16,17 DDR3_DRAMRST# R0508 1KOhm CPUDRAMRST# 4
R0508 use 1k ohm
Design Guide 0.9 p107(436735)
Close to DIMM
9,21,30 DRAMRST_CNTRL_PCH
R2.0 12/14
C0501 0.1UF/10V
1% 4.99KOhm R0506

PEGATRON Title : CPU(3)_DDR3
BG1-HW RD Div.2-NB RD Dept.5 Engineer: Joyoung_Chianhg
Size C | Project Name MA50 | Rev 1.0
Date: Monday, February 13, 2012 | Sheet 5 of 93


+VCCP +VCCP 3,4,7,30,32,57,82
+VCORE +VCORE 9,11,80
U0301F
+VCORE
POWER
CORE SUPPLY
PEG AND DDR
QUIET RAILS
SVID
SENSE LINES
+VCCP
+3VA
+VCCIO_CPU_F
VCCIO_SEL
VCCP_SEL
R0601
NB_R0603_32MIL_SMALL
R0615
10KOhm
R0613
0Ohm
C0622
1UF/6.3V
R0603
75Ohm
1%
Close to CPU
R0605
54.9Ohm
Close to VR
R0609
130Ohm
Close to CPU
R0608
130Ohm
Close to VR
R2.0 12/19
H_CPU_SVIDALRT#
H_CPU_SVIDCLK
H_CPU_SVIDDAT
R0602
43Ohm
10V240000039
VR_SVID_ALERT# 80
VR_SVID_CLK 80
VR_SVID_DATA 80
SP0601
SP0602
SP0603
NB_R0402_20MIL_SMALL
SP0604
VCC_SENSE_R
VSS_SENSE_R
VCCSENSE
VSSSENSE
R0616
10Ohm
1%
R0614
+VCCP_SENSE 82
+VSSP_SENSE 82
ES1
01V010000003
PEGATRON Title : CPU(4)_PWR
BG1-HW RD Div.2-NB RD Dept.5 Engineer: Joyoung_Chianhg
Size C
Project Name MA50
Rev 1.0
Date: Monday, February 13, 2012
Sheet 6 of 93

Decoupling guide from Intel PDDG R0.8
+VGFX_CORE
1uF * 11pcs
10uF * 6pcs
22uF * 6pcs

+VGFX_CORE
1uF * 11pcs
10uF * 6pcs
22uF * 8pcs(power request)

+VCCP +VCCP 3,4,6,30,32,57,82
+1.5V +1.5V 5,16,17,18,57,60,83
+VCCSA +VCCSA 85
+1.8VS +1.8VS 25,26,57,80,84
+VGFX_CORE +VGFX_CORE 9,80
+1.5VS +1.5VS 26,53,57,91
+V_SM_VREF +V_SM_VREF 83

Graphics core voltage
Voltage range: 0 - 1.52V

+VGFX_CORE
C0725 1UF/6.3V, C0727 1UF/6.3V, C0731 1UF/6.3V, C0726 1UF/6.3V, C0732 1UF/6.3V, C0729 1UF/6.3V, C0730 1UF/6.3V, C0728 1UF/6.3V
C0717 1UF/6.3V, C0719 1UF/6.3V, C0722 1UF/6.3V
vx_c0603_small: C0790 10UF/6.3V, C0791 10UF/6.3V, C0788 10UF/6.3V, C0789 10UF/6.3V, C0787 10UF/6.3V, C0786 10UF/6.3V
C0738 22UF/6.3V, C0739 22UF/6.3V, C0740 22UF/6.3V, C0741 22UF/6.3V, C0742 22UF/6.3V, C0743 22UF/6.3V, C0744 22UF/6.3V, C0745 22UF/6.3V

U0301G

AA46 VAXG21, AB47 VAXG20, AB50 VAXG19, AB51 VAXG18, AB52 VAXG17, AB53 VAXG16, AB55 VAXG15, AB56 VAXG14, AB58 VAXG13, AB59 VAXG12, AC61 VAXG11, AD47 VAXG10, AD48 VAXG9, AD50 VAXG8, AD51 VAXG7, AD52 VAXG6, AD53 VAXG5, AD55 VAXG4, AD56 VAXG3, AD58 VAXG2, AD59 VAXG1, AE46 VAXG0
N45 VAXG55, P47 VAXG54, P48 VAXG53, P50 VAXG52, P51 VAXG51, P52 VAXG50, P53 VAXG49, P55 VAXG48, P56 VAXG47, P61 VAXG46, T48 VAXG45, T58 VAXG44, T59 VAXG43, T61 VAXG42, U46 VAXG41, V47 VAXG40, V48 VAXG39, V50 VAXG38, V51 VAXG37, V52 VAXG36, V53 VAXG35, V55 VAXG34, V56 VAXG33, V58 VAXG32, V59 VAXG31, W50 VAXG30, W51 VAXG29, W52 VAXG28, W53 VAXG27, W55 VAXG26, W56 VAXG25, W61 VAXG24, Y48 VAXG23, Y61 VAXG22

GRAPHICS

POWER

DDR3 - 1.5V RAILS

VDDQ25 AJ28, VDDQ24 AJ33, VDDQ23 AJ36, VDDQ22 AJ40, VDDQ21 AL30, VDDQ20 AL34, VDDQ19 AL38, VDDQ18 AL42, VDDQ17 AM33, VDDQ16 AM36, VDDQ15 AM40, VDDQ14 AN30, VDDQ13 AN34, VDDQ12 AN38, VDDQ11 AR26, VDDQ10 AR28, VDDQ9 AR30, VDDQ8 AR32, VDDQ7 AR34, VDDQ6 AR36, VDDQ5 AR40, VDDQ4 AV41, VDDQ3 AW26, VDDQ2 BA40, VDDQ1 BB28, VDDQ0 BG33

DDR3 Reference Voltage

+V_SM_REF 10mil
SM_VREF AY43 +V_SM_VREF
+V_SM_VREF
R0703 1KOhm
R0710 1KOhm
C0794 0.1UF/10V
+1.5VS_VCCDDQ
R1.1 add S3 power reduction

Processor I/O supply voltage for DDR3 (DC + AC specification)

MAX:5A
C0704 1UF/6.3V, C0709 1UF/6.3V, C0705 1UF/6.3V, C0706 1UF/6.3V, C0707 1UF/6.3V, C0708 1UF/6.3V, C0713 1UF/6.3V, C0710 1UF/6.3V, C0712 1UF/6.3V, C0711 1UF/6.3V
+1.5VS_VCCDDQ, +1.5VS, JP0701 @ 3MM_OPEN_5MIL
ICCMAX_VDDQ 5A
vx_c0603_small: C0775 10UF/6.3V, C0774 10UF/6.3V, C0772 10UF/6.3V, C0769 10UF/6.3V, C0767 10UF/6.3V, C0765 10UF/6.3V, C0770 10UF/6.3V, C0768 10UF/6.3V
CE0702 330UF/2V
R1.1 add S3 power reduction

Chief River

Decoupling guide from Intel (EE)
+1.5VS_VCCDDQ
1uF * 10pcs
10uF * 8pcs
330uF * 1pcs

SENSE LINES

80 VCCGT_SENSE
80 VSSGT_SENSE
SP0701 NB_R0402_20MIL_SMALL
SP0702 NB_R0402_20MIL_SMALL
F45 VAXG_SENSE
G45 VSSAXG_SENSE

PLL supply voltage
(DC + AC specification)

+1.8VS
MAX:1.2A
TDC: 1.2A
CE0701 330UF/2V
C0761 1UF/6.3V
C0764 1UF/6.3V
BB3 VCCPLL2
BC1 VCCPLL1
BC4 VCCPLL0

1.8V RAIL

QUIET RAILS

VCCDQ1 AM28
VCCDQ0 AN26
Filtered(BGA Only)
+1.5VS_VCCDDQ
R0707 0Ohm
C0714 1UF/6.3V

+VCCSA
MAX:10A
TDC: 6A
vx_c0603_small: C0783 10UF/6.3V, C0781 10UF/6.3V, C0792 10UF/6.3V, C0777 10UF/6.3V, C0793 10UF/6.3V
C0735 1UF/6.3V, C0736 1UF/6.3V, C0733 1UF/6.3V, C0734 1UF/6.3V, C0737 1UF/6.3V
L17 VCCSA15, L21 VCCSA14, N16 VCCSA13, N20 VCCSA12, N22 VCCSA11, P17 VCCSA10, P20 VCCSA9, R16 VCCSA8, R18 VCCSA7, R21 VCCSA6, U15 VCCSA5, V16 VCCSA4, V17 VCCSA3, V18 VCCSA2, V21 VCCSA1, W20 VCCSA0

SA RAIL

SENSE LINES

VDDQ_SENSE BC43 T0701
VSS_SENSE_VDDQ BA43 T0702

VCCSA_SENSE U10 R0704 0Ohm @ Close to CPU VCCSA_SENSE 85

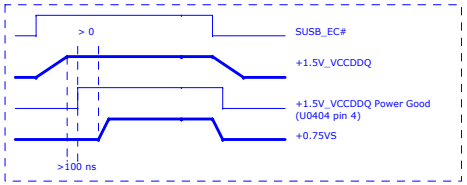
VCCSA_VID[0] D48 VCCSA_SEL0 VCCSA_SEL0 85
VCCSA_VID[1] D49 VCCSA_SEL1 VCCSA_SEL1 85

Chief River

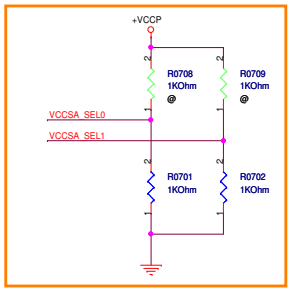
+VCCSA_SEL0	+VCCSA_SEL1	VCCSA
L	L	0.9V
L	H	0.85V
H	L	0.725V
H	H	0.675V

Decoupling guide for A14 (EE)
+VCCSA
1uF * 5pcs
10uF * 5pcs

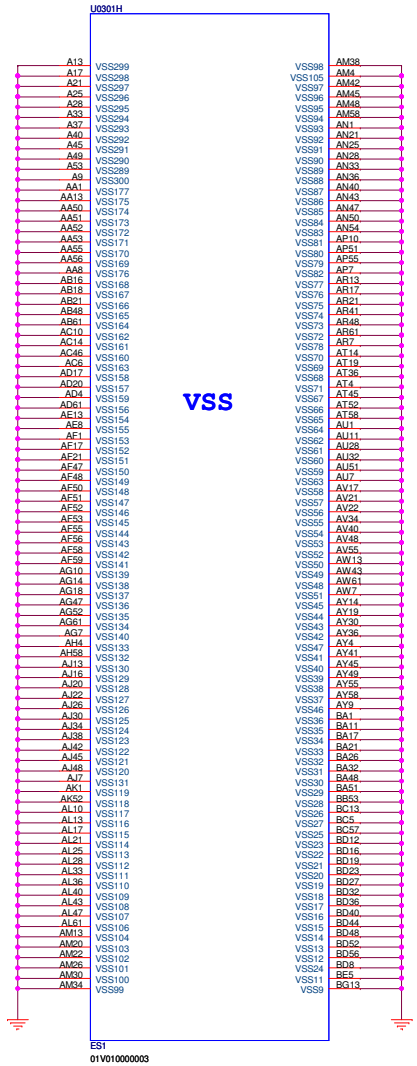
ES1
01V010000003

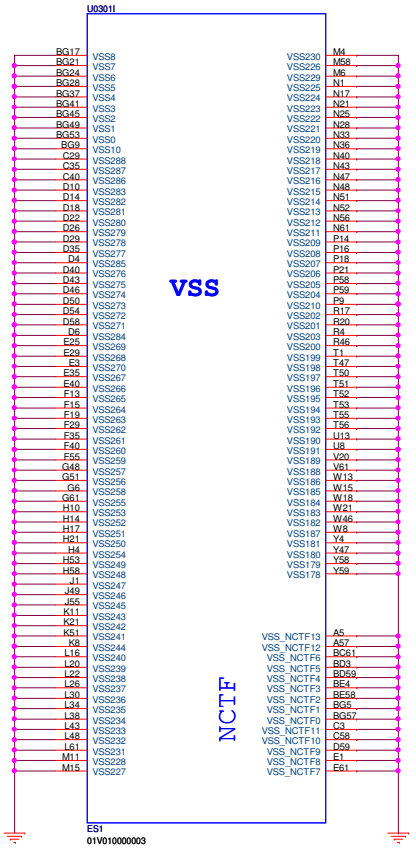


R1.0 0209
Intel Comments



PEGATRON Title : CPU(5)_GFX_PWR
BG1-HW RD Div.2-NB RD Dept.5 Engineer: Joyoung_Chianhg
Size C | Project Name MA50 | Rev 1.0
Date: Monday, February 13, 2012 | Sheet 7 of 93





PEGATRON	Title : CPU(6)_GND		
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Joyoung_Chianhg		
Size: C	Project Name: MA50		Rev: 1.0
Date: Monday, February 13, 2012	Sheet 8 of 93		

CFG strapping information:

CFG[2]: PCIE Static Numbering Lane Reversal- CFG[2] is for the 16x

- 1: (Default) Normal Operation, Lane # definition matches sockect pin map definition
- 0: Lane Numbers Reversed

CFG[4]: Embedded DisplayPort Detection

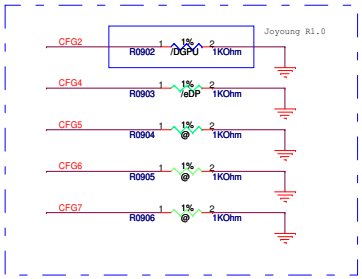
- 1: (Default) Disabled ; No Physical Display Port attached to Embedded DisplayPort
- 0: Enabled ; An external Display Port device is connected to the Embedded Display Port

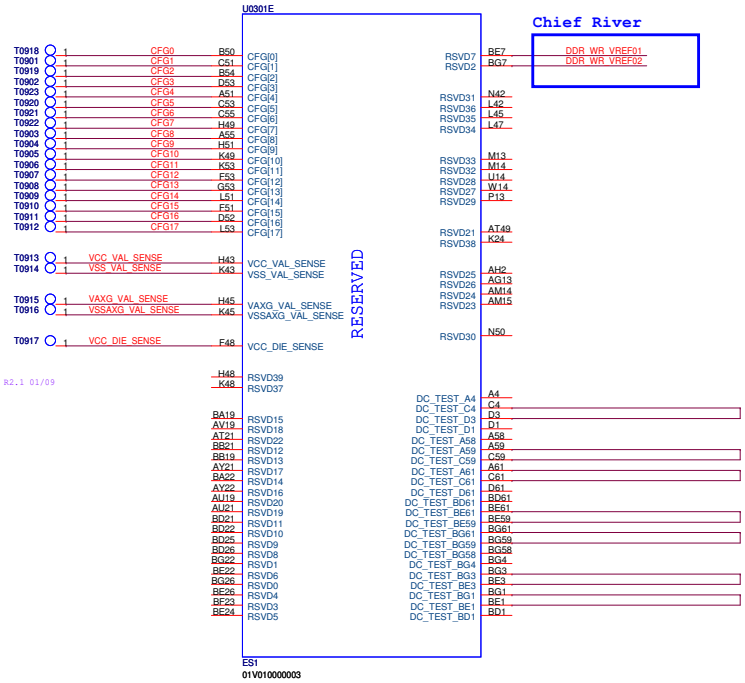
CFG[6:5]: PCI Express Port Bifurcation Straps

- 11 : (Default) x 1 6
- 10 : x 8 , x 8
- 01 : Reserved
- 00 : x 8 , x 4 , x 4

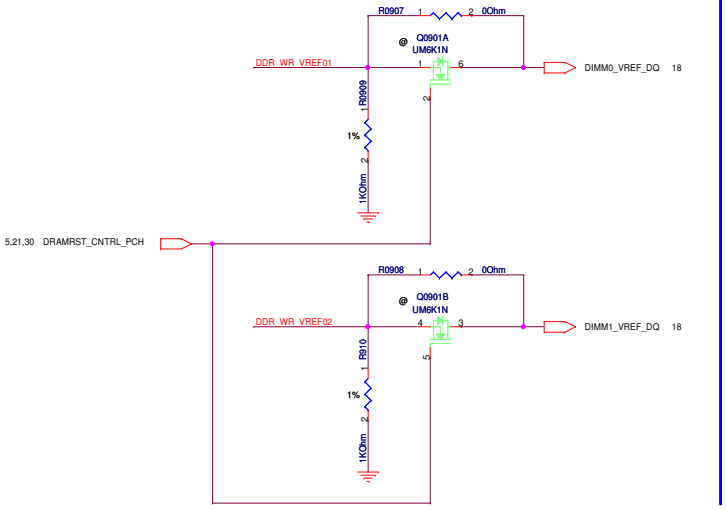
CFG[7]: PEG DEFER TRAINING

- 1: (Default) PEG Train immediately following xxRESETB de assertion
- 0: PEG Wait for BIOS training



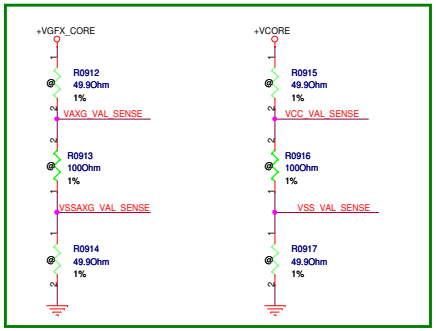


PROCESSOR DRIVEN Vref PATH WAS STUFFED BY DEFAULT:



For iFDIM testing
R0912~ R0917 close to pin < 1 inch

R1.1 0512



PEGATRON Title : CPU(7)_RSVD

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	MA50	1.0

Date: Monday, February 13, 2012 Sheet 9 of 93

Check Connector

CPU XDP connector

PCH XDP connector

PEGATRON	Title : CPU_PCH_XDP	
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Joyoung_Chianhg	
Size: Custom	Project Name: MA50	Rev: 1.0
Date: Monday, February 13, 2012	Sheet 10 of 93	

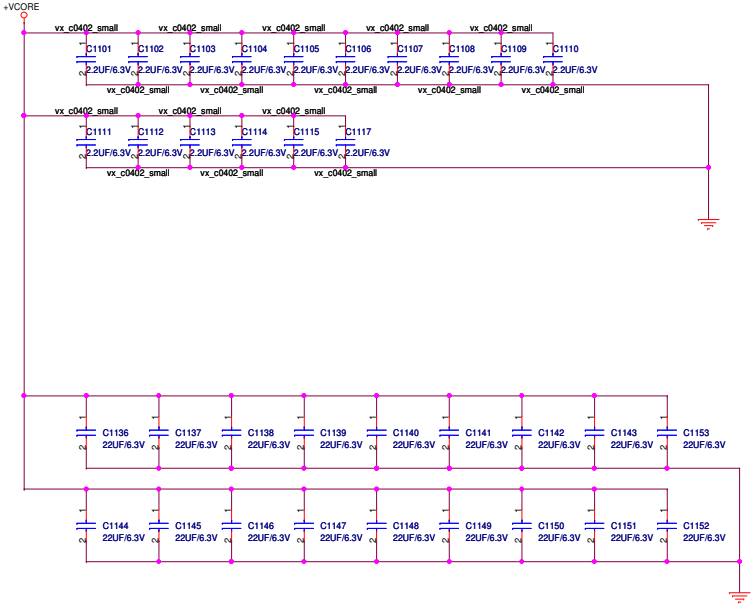
Chief River

Decoupling guide from Intel PDDG R0.8

+VCORE 2.2uF * 16 pcs
22uF * 12 pcs

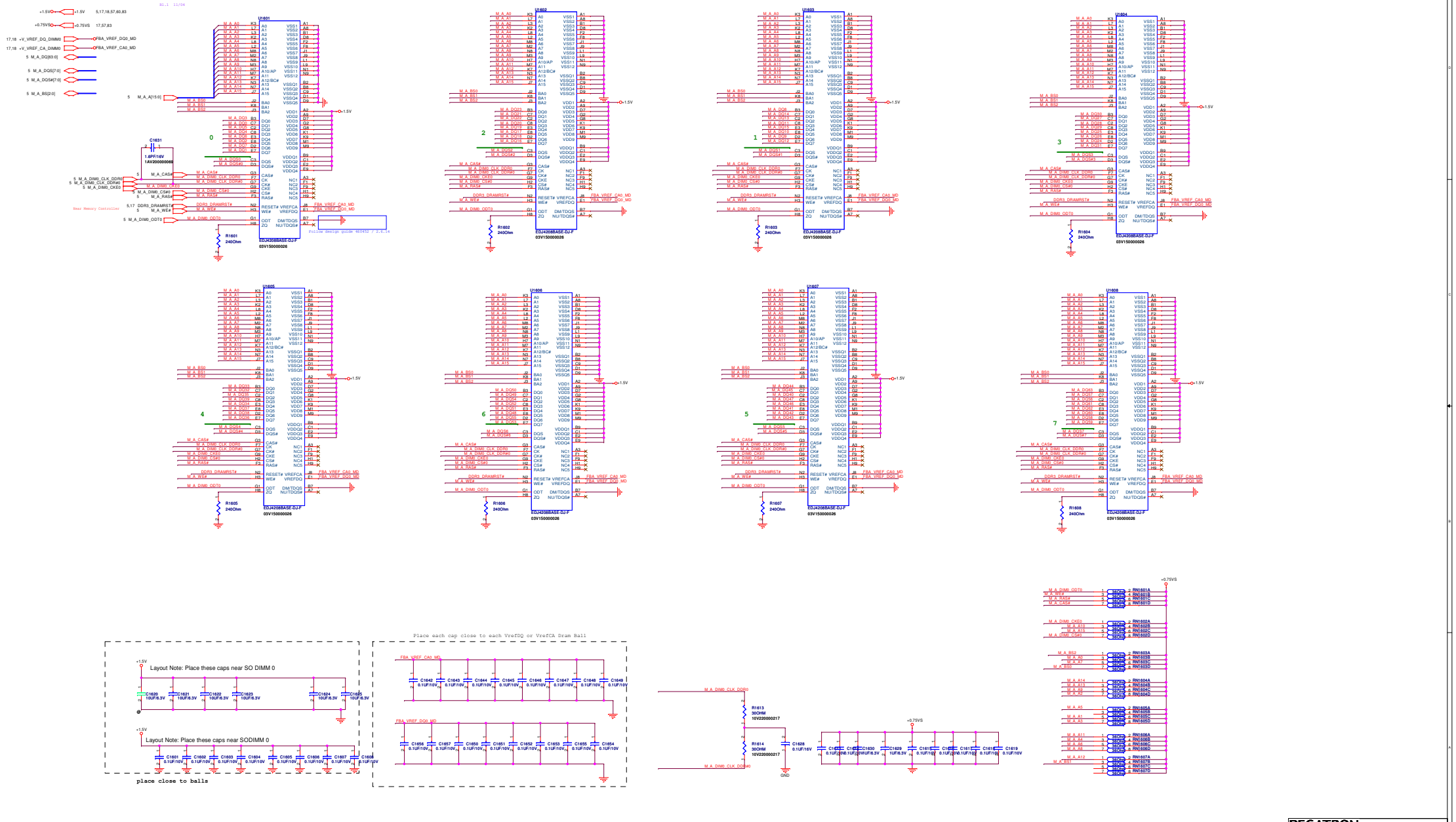
Chief River

+VCORE 2.2uF * 16 pcs
22uF * 18 pcs (power request)



PEGATRON	Title : CPU DECOUPLING	
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Joyoung_Chianhg	
Size: C	Project Name: MA50	Rev: 1.0
Date: Monday, February 13, 2012	Sheet 11 of 93	

Memory Down CH A



PEGATRON Title : DDR3(1) SO-DIMM

SG1-HW RD Div.2-MB RD Dept.5 Engineer: Joyoung_Chiehg

Size	Project Name	Rev
D	MA50	1.0

Date: Monday, February 13, 2012 Sheet 16 of 55

+1.5V — +1.5V 5,16,18,57,60,83

+0.75VS — +0.75VS 16,57,83

+3VS — +3VS 20,21,22,23,24,25,26,27,28,30,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92

+V_VREF_CA_DIMM1 — +V_VREF_CA_DIMM1 16,18

+V_VREF_DQ_DIMM1 — +V_VREF_DQ_DIMM1 16,18

+1.5V — CE1703 220UF/4V @

+1.5V — Layout Note: Place these caps near SO DIMM 1 — C1709 10UF/6.3V @, C1710 10UF/6.3V, C1711 10UF/6.3V @, C1712 10UF/6.3V, C1713 10UF/6.3V @, C1718 10UF/6.3V

+0.75VS — C1716 1UF/6.3V, C1717 1UF/6.3V, C1719 1UF/6.3V @, C1730 1UF/6.3V @

5 M_B_A[15:0]

M_B_A0 98, M_B_A1 97, M_B_A2 96, M_B_A3 95, M_B_A4 92, M_B_A5 91, M_B_A6 90, M_B_A7 86, M_B_A8 89, M_B_A9 85, M_B_A10 107, M_B_A11 84, M_B_A12 83, M_B_A13 119, M_B_A14 80, M_B_A15 78

J1701A

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC# A13 A14 A15

DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 DQ32 DQ33 DQ34 DQ35 DQ36 DQ37 DQ38 DQ39 DQ40 DQ41 DQ42 DQ43 DQ44 DQ45 DQ46 DQ47 DQ48 DQ49 DQ50 DQ51 DQ52 DQ53 DQ54 DQ55 DQ56 DQ57 DQ58 DQ59 DQ60 DQ61 DQ62 DQ63

0 1 2 3 4 5 6 7

M_B_DQ1 5, M_B_DQ5 7, M_B_DQ7 15, M_B_DQ2 17, M_B_DQ4 4, M_B_DQ0 6, M_B_DQ6 16, M_B_DQ3 18, M_B_DQ8 21, M_B_DQ12 23, M_B_DQ10 33, M_B_DQ15 35, M_B_DQ9 22, M_B_DQ13 24, M_B_DQ11 34, M_B_DQ14 36, M_B_DQ16 39, M_B_DQ20 41, M_B_DQ21 51, M_B_DQ17 53, M_B_DQ23 40, M_B_DQ22 42, M_B_DQ18 50, M_B_DQ19 52, M_B_DQ25 57, M_B_DQ28 59, M_B_DQ30 67, M_B_DQ26 69, M_B_DQ29 56, M_B_DQ24 58, M_B_DQ27 68, M_B_DQ31 70, M_B_DQ32 129, M_B_DQ33 131, M_B_DQ38 141, M_B_DQ34 143, M_B_DQ36 130, M_B_DQ37 132, M_B_DQ39 140, M_B_DQ35 142, M_B_DQ44 147, M_B_DQ40 149, M_B_DQ46 157, M_B_DQ41 159, M_B_DQ42 146, M_B_DQ45 148, M_B_DQ47 158, M_B_DQ43 160, M_B_DQ53 163, M_B_DQ52 165, M_B_DQ55 175, M_B_DQ54 177, M_B_DQ49 164, M_B_DQ48 166, M_B_DQ50 174, M_B_DQ51 176, M_B_DQ63 181, M_B_DQ61 183, M_B_DQ57 191, M_B_DQ59 193, M_B_DQ60 180, M_B_DQ56 182, M_B_DQ58 192, M_B_DQ62 194

M_B_DQ[63:0] 5

0~7 8~15 16~23 24~31 32~39 40~47 48~55 56~63

5 M_B_DIM0_CLK_DDR1 — CK1 102
5 M_B_DIM0_CLK_DDR#1 — CK1# 104
5 M_B_DIM0_CLK_DDR0 — CK0 101
5 M_B_DIM0_CLK_DDR#0 — CK0# 103

5 M_B_DIM0_CS#1 — S1# 121
5 M_B_DIM0_CS#0 — S0# 114

5 M_B_DIM0_ODT1 — ODT1 120
5 M_B_DIM0_ODT0 — ODT0 116

5 M_B_WE# — WE# 113
5 M_B_RAS# — RAS# 115
5 M_B_CAS# — CAS#

5 M_B_BS2 — BA2 79
5 M_B_BS1 — BA1 108
5 M_B_BS0 — BA0 109

5 M_B_DIM0_CKE1 — CKE1 74
5 M_B_DIM0_CKE0 — CKE0 73

SA1 201, SA0 197

M_B_DQS7 188, M_B_DQS#7 186, M_B_DQS6 171, M_B_DQS#6 169, M_B_DQS5 154, M_B_DQS#5 152, M_B_DQS4 137, M_B_DQS#4 135, M_B_DQS3 64, M_B_DQS#3 62, M_B_DQS2 47, M_B_DQS#2 45, M_B_DQS1 29, M_B_DQS#1 27, M_B_DQS0 12, M_B_DQS#0 10

DQS7 DQS#7 DQS6 DQS#6 DQS5 DQS#5 DQS4 DQS#4 DQS3 DQS#3 DQS2 DQS#2 DQS1 DQS#1 DQS0 DQS#0

5 M_B_DQS[7:0]
5 M_B_DQS#[7:0]

DM7 187, DM6 170, DM5 153, DM4 136, DM3 63, DM2 46, DM1 28, DM0 11

SCL 202, SDA 200

RESET# 30 — DDR3_DRAMRST# 5,16

J1701B

VDD1 VDD3 VDD5 VDD7 VDD9 VDD11 VDD13 VDD15 VDD17

VDD2 VDD4 VDD6 VDD8 VDD10 VDD12 VDD14 VDD16 VDD18

VSS1 VSS3 VSS5 VSS7 VSS9 VSS11 VSS13 VSS15 VSS17 VSS19 VSS21 VSS23 VSS25 VSS27 VSS29 VSS31 VSS33 VSS35 VSS37 VSS39 VSS41 VSS43 VSS45 VSS47 VSS49 VSS51

VSS2 VSS4 VSS6 VSS8 VSS10 VSS12 VSS14 VSS16 VSS18 VSS20 VSS22 VSS24 VSS26 VSS28 VSS30 VSS32 VSS34 VSS36 VSS38 VSS40 VSS42 VSS44 VSS46 VSS48 VSS50 VSS52

GND1 GND2

EVENT# TEST NC1 NC2

NP_NC1 NP_NC2

VTT1 VTT2

VREFCA VREFDQ VDDSPD

+1.5V — C1705 0.1UF/16V, C1706 0.1UF/16V — C1707 0.1UF/16V, C1708 0.1UF/16V

Layout Note: Place these caps near SO DIMM 1

T1701 PM_EXTTS#0_DIM_B — Reserve

+V_VREF_CA_DIMM1 — C1724 2.2UF/6.3V @, C1723 0.1UF/16V

+V_VREF_DQ_DIMM1 — C1722 2.2UF/6.3V @, C1725 0.1UF/16V

+0.75VS

+3VS — C1715 0.1UF/16V, C1714 2.2UF/6.3V @

Frank
20110513 VREFCA and VREFDQ need to separate
It follow EVEREST and Intel spec.

M_B_DIM0_CLK_DDR0 — C1720 10PF/50V @ — 150Ohm R1707 — M_B_DIM0_CLK_DDR#0

M_B_DIM0_CLK_DDR1 — C1721 10PF/50V @ — 150Ohm R1708 — M_B_DIM0_CLK_DDR#1

PLACE CLOSE TO SODIMM

SMBus Slave Address: A4H

+3VS — R1709 SP1703 — 10KOhm

take care if can't boot or S3 issue

DM should connect to GND directly
Design Guide 1.0 P.88 (436735)

28,53,59 SMB_CLK_S — SP1701 — R0402 SMB_CLK_S_CHB

28,53,59 SMB_DAT_S — SP1702 — R0402 SMB_DAT_S_CHB

DDR3_DIMM_204P
12V02GBRM000

DDR3_DIMM_204P
12V02GBRM000

H:5.2mm

PEGATRON Title : DDR3(2)_SO-DIMM1

PEGATRON COMPUTER INC Engineer: Joyoung_Chianhg

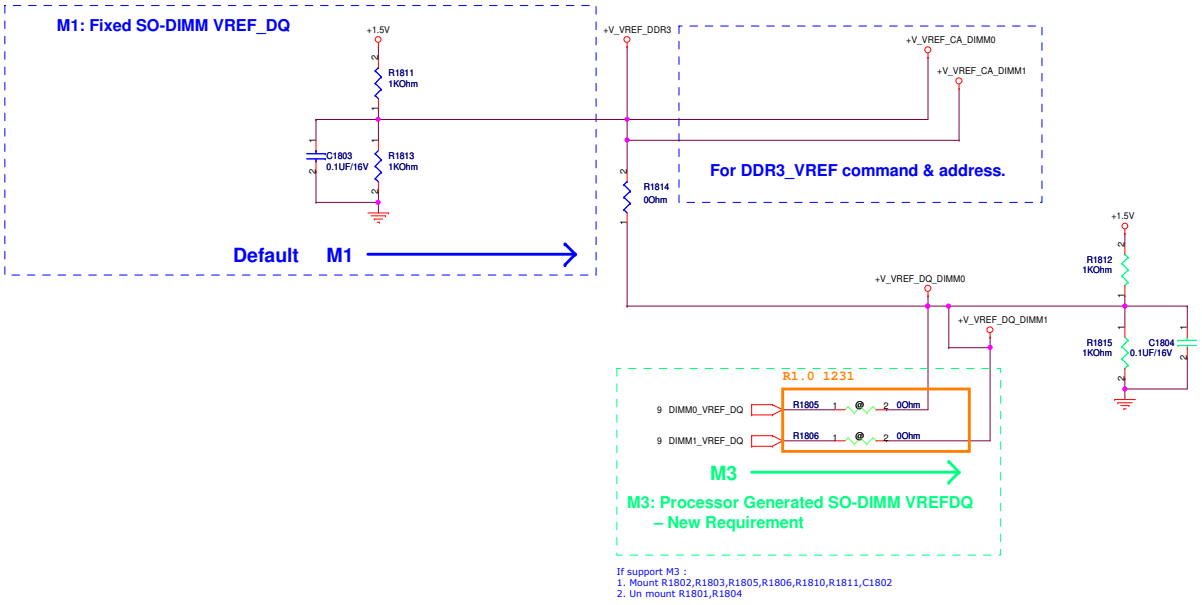
Size	Project Name	Rev
C	MA50	1.0

Date: Monday, February 13, 2012 Sheet 17 of 93

DDR3 Vref

+1.5V — +1.5V — 5,16,17,57,60,83
+V_VREF_CA_DIMM0 — +V_VREF_CA_DIMM0 — 16,17
+V_VREF_DQ_DIMM0 — +V_VREF_DQ_DIMM0 — 16,17

+3V — +3V — 24,45,57,59,61,91
+5VSUS — +5VSUS — 51,57,59,91
+5VA — +5VA — 37,60,81,91



If support M3 :
1. Mount R1802,R1803,R1805,R1806,R1810,R1811,C1802
2. Un mount R1801,R1804

PEGATRON Title : DDR3(3)_CA/DQ Voltage

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	MA50	1.0

Date: Monday, February 13, 2012 Sheet 18 of 93

R1.4--2

PEGATRON Title : VID Controller

PEGATRON COMPUTER INC Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	MA50	1.0

Date: Monday, February 13, 2012 Sheet 19 of 93

RTC battery

PR2.1

+3VA, T2030, +RTCBAT, R2001 1KOhm, D2002 1V/0.2A, +RTC_BAT, +VCC_RTC, C2003 1UF/10V, GND

59,60 +RTCBAT

Request by CSC for CMOS clear function

CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)

+VCC_RTC RTCRST# RC delay should be 18ms~25ms

R2003 20KOhm 5%, C2004 1UF/10V, JRST2001 SGL_JUMP @, GND

R2004 20KOhm 5%, R2005 1MOhm, C2005 1UF/10V, JRST2002 SGL_JUMP @, GND

INTVRMEN: Integrated SUS 1.05V VRM Enables
Low: Enable External VRs
High:Enable Internal VRs

PCH_INTVRMEN R2030 @ 1% 200KOhm GND

TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

Intel 1.5 Design Guide, page 260

isolate schematic for ACZ _SYNC and SDOUT follow EIH31

R1.0
For JTAG to pull high and low.

Remove JTAG schematic

+VCC_RTC +VCC_RTC 22,27 — R1.0 Delete +RTCBAT
+3VA +3VA 6,26,27,30,31,57,59,60,81,88,93
+3VS +3VS 17,21,22,23,24,25,26,27,28,30,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92
+3VSUS_ORG +3VSUS_ORG 21,22,24,25,26,27,33
+1.05VM_ORG +1.05VM_ORG 27
+VTT_PCH_VCCIO +VTT_PCH_VCCIO 26,27

C2001 15PF/50V, X2001 32.768KHZ, C2002 15PF/50V, SP2005, R2002 10MOhm, T2015, T2012

20110718 Frank add C2006 for EMI request
+VCC_RTC 330KOhm C2006 @ 33PF/50V R2006

U2001A

RTC_X1	A20	RTCX1	RTC	
RTC_X2	C20	RTCX2		
RTC_RST#	D20	RTCRST#		
SRTC_RST#	G22	SRTCRST#		
SM_INTRUDER#	K22	INTRUDER#		
PCH_INTVRMEN	C17	INTVRMEN		
ACZ_BCLK	N34	HDA_BCLK	IHDA	
ACZ_SYNC	L34	HDA_SYNC		
	T10	SPKR		
ACZ_RST#	K34	HDA_RST#		
	E34	HDA_SDIN0		
Remove TP	G34	HDA_SDIN1		
ACZ_SDIN2_AUD	C34	HDA_SDIN2		
ACZ_SDIN3_AUD	A34	HDA_SDIN3		
ACZ_SDOUT	A36	HDA_SDO		
HDA_DOCK_EN#	C36	HDA_DOCK_EN#/GPIO33		
CARDREADER_RESET	N32	HDA_DOCK_RST#/GPIO13		
PCH_JTAG_TCK_BUF	J3	JTAG_TCK	JTAG	
PCH_JTAG_TMS	H7	JTAG_TMS		
PCH_JTAG_TDI	K5	JTAG_TDI		
PCH_JTAG_TDO	H1	JTAG_TDO		
SPI_CLK	T3	SPI_CLK	SPI	
SPI_CS#0	Y14	SPI_CS0#		
SPI_CS#1	T1	SPI_CS1#		
SPI_SI	V4	SPI_MOSI		
SPI_SO	U3	SPI_MISO		

COUGAR_POINT_ES1
02V000000001

FWH0/LAD0	C38	LPC_AD0 30,44,59	LPC	
FWH1/LAD1	A38	LPC_AD1 30,44,59		
FWH2/LAD2	B37	LPC_AD2 30,44,59		
FWH3/LAD3	C37	LPC_AD3 30,44,59		
FWH4/LFRAME#	D36	LPC_FRAME# 30,44,59		
LDRQ0#	E36	SNN_PCH_DRQ#0 T2032		
LDRQ1#/GPIO23	K36	SNN_LPC_DRQ#1 T2033		R1.0
SERIRQ	V5	Serial Interrupt Request — INT_SERIRQ 30,44,59		
SATA0RXN	AM3	SATA_RXN0 51	SATA 6G	HDD1
SATA0RXP	AM1	SATA_RXP0 51		
SATA0TXN	AP7	SATA_TXN0 51		
SATA0TXP	AP5	SATA_TXP0 51		
SATA1RXN	AM10	SATA_RXN1 53		HDD2
SATA1RXP	AM8	SATA_RXP1 53		
SATA1TXN	AP11	SATA_TXN1 53		
SATA1TXP	AP10	SATA_TXP1 53		
SATA2RXN	AD7	SATA_RXN2 51		ODD
SATA2RXP	AD5	SATA_RXP2 51		
SATA2TXN	AH5	SATA_TXN2 51		
SATA2TXP	AH4	SATA_TXP2 51		
SATA3RXN	AB8		SATA	mSATA
SATA3RXP	AB10			
SATA3TXN	AF3			
SATA3TXP	AF1			
SATA4RXN	V7			
SATA4RXP	Y5			
SATA4TXN	AD3			
SATA4TXP	AD1			
SATA5RXN	Y3			
SATA5RXP	Y1			
SATA5TXN	AB5			
SATA5TXP	AB3			
SATAICOMPO	Y11			
SATAICOMPI	Y10	SATA_COMP R2007 1% 37.4Ohm +VTT_PCH_VCCIO		
SATA3RCOMPO	AB12			
SATA3COMPI	AB13	SATA3_COMP R2047 1% 49.9Ohm +VTT_PCH_VCCIO		
SATA3RBIAS	AH1	RBIAS_SATA3 R2048 1% 750Ohm GND		
SATALED#	P3	R2025 10KOhm +3VS, SATA_LED#		
SATA0GP/GPIO21	V14	SATA0GP T2034		
SATA1GP/GPIO19	P1	BBS_BIT0 24		

R1.0

R1.1 10/31 IOAC
36 ACZ_SDOUT_AUD SP2011 T2001 R2050 near R2008

T2004 PCH_JTAG_TCK_BUF
T2005 PCH_JTAG_TMS
T2006 PCH_JTAG_TDI
T2007 PCH_JTAG_TDO

28 SPI_CLK
28 SPI_CS#0
28 SPI_CS#1
28 SPI_SI
28 SPI_SO

R1.1 11/04

36,37 ACZ_RST#_AUD SP2010
36 ACZ_SDIN0_AUD
T2021 ACZ_SDIN2_AUD
T2022 ACZ_SDIN3_AUD
36 ACZ_BCLK_AUD SP2009
36 ACZ_SYNC_AUD SP2008
36 SB_SPKR

Strap information:

SB_SPKR: No reboot strap
Low: Disable (Default)
High:Enable
SB_SPKR R2020 @ 1KOhm +3VS

ACZ_SDOUT:
1.Flash descriptor security:
Sampled Low: in effect.
Sampled High: override
2.ACZ_SDOUTwhich sample high on the rising edge of PWROK
Will also disable Intel ME.
ACZ_SDOUT R2034 @ 1KOhm +3VSUS_ORG

ACZ_SYNC: On Die PLL VR voltage selector
Low: 1.8V (Default)
High: 1.5V
note : CRB has no strap
Hrron River Platform Schematic Design Checklist (438390 page 48)
ACZ_SYNC R2036 1KOhm +3VSUS_ORG
VCCVRAM use +1.5VS in mobile

Pull High
+3VS
INT_SERIRQ R2026 10KOhm
SATA0GP R2027 10KOhm

PEGATRON COMPUTER INC
Title : PCH(1)_SATA,IHDA,RTC,LPC
Engineer: Joyoung_Chianhg
Size C | Project Name MA50 | Rev 1.0
Date: Monday, February 13, 2012 | Sheet 20 of 93

Frank
0513_Add USB3.0 and Card Reader PCIE and CLKRQ

Frank
0517_Add 3G PCIE and CLKRQ in Port3.

+3VS 17,20,22,23,24,25,26,27,28,30,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92
+VTT_PCH_ORG 22,26,27
+3VSUS_ORG 20,22,24,25,26,27,33

Joyoung R1.0

U2001B

PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS
COUGAR_POINT_ES1

R1.1
remove /niAMT remark

R2.0 12/14
R1.0

To EC

R1.1
S3 RAM reset CTRL

R2.0 12/20
R2.0 12/14

CLOCK TERMINATION for FCIM
Default power-on mode is ICC.

Joyoung R1.0
modify CLK_REQ

25-MHz is required in:
1. FCIM
2. BTM for PCH Display Clock gereration in Integrated Graphics platforms

PCH CLKREQ Setting:
Not connected to device.
R1.0 0118

Connected to device.
Default : Clock free run. (PD 10K).
Reserver 10K PU for power saving purpose.
Eric Fang to Alan Chien on 11/15/2010

Remove XDP.

02V000000001

R2.0 12/15

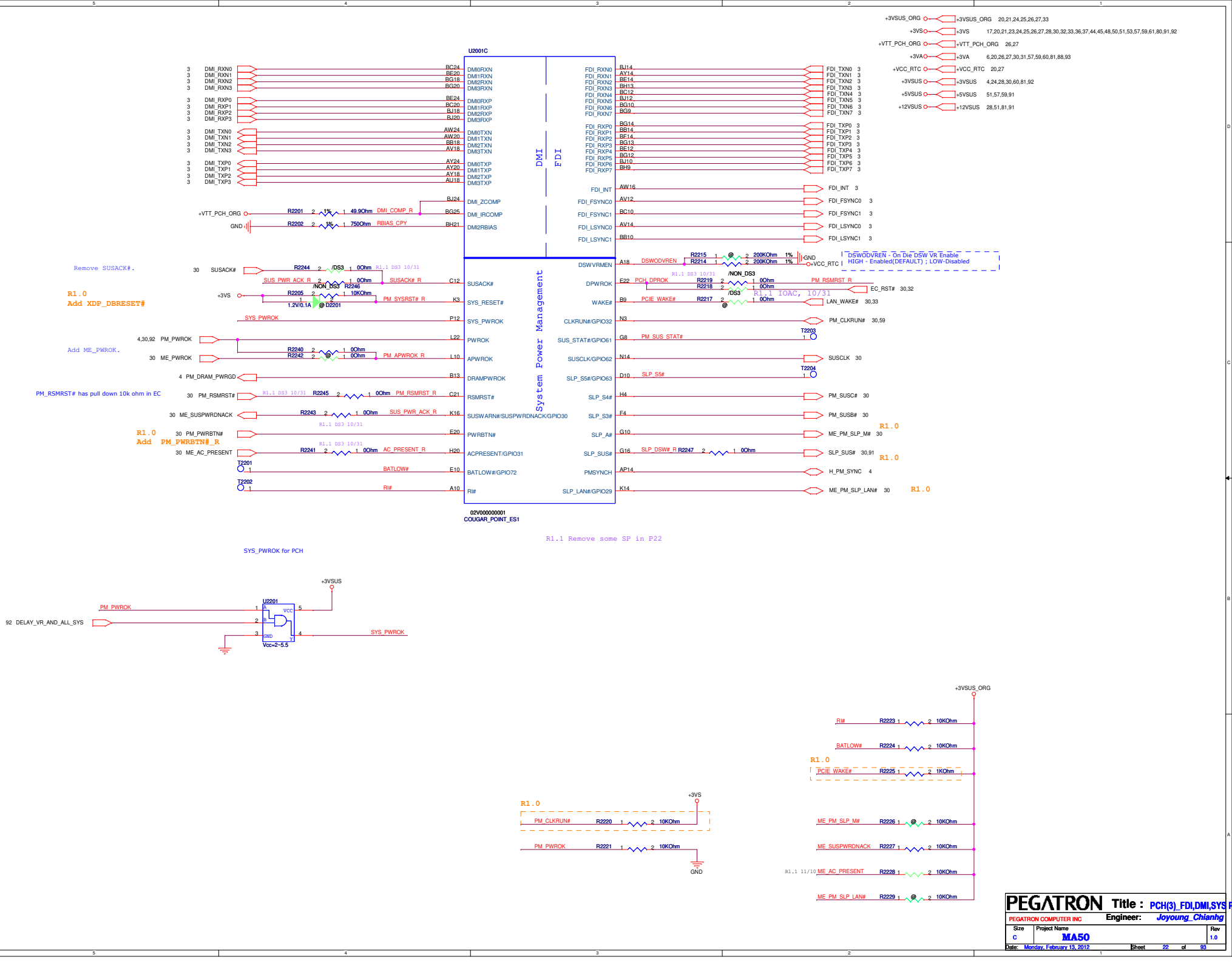
R2.0
Modify RAM Strap PIN

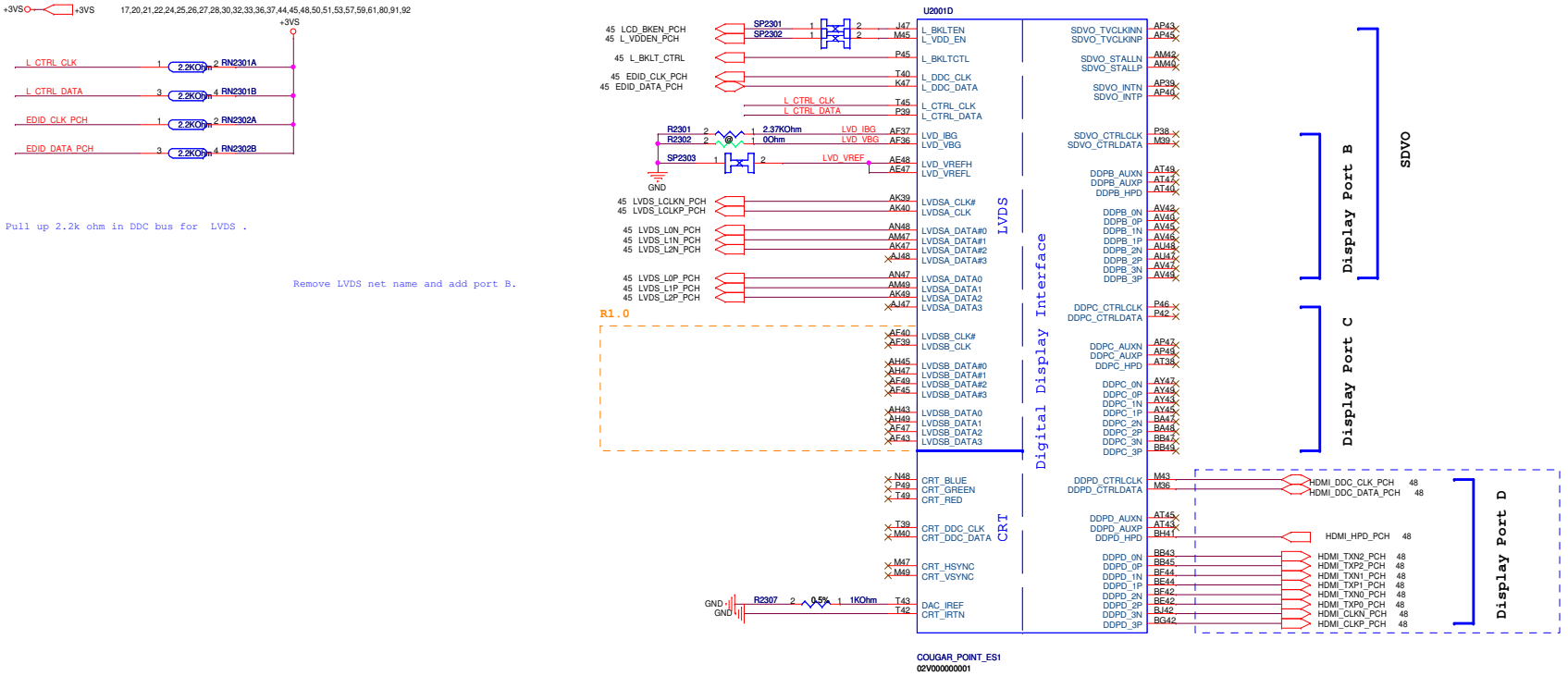
Joyoung R2.0
add GPIO Table for on board RAM Strap.

On Board RAM Setting

GPIO67	GPIO66	GPIO65	GPIO64	On Board RAM Setting
0	0	0	0	No on board RAM
0	0	0	1	Micron 1333MHz 4GB
0	0	1	0	Elpida 1333MHz 4GB
0	1	1	0	Elpida 1333MHz 2GB
0	1	0	1	Micron 1333MHz 2GB
X	X	X	X	TBD
1	0	0	0	Common Definition 1333MHz 4GB
1	0	0	1	Common Definition 1600MHz 4GB

PEGATRON Title : PCH(2)_PCIE,CLK,SMB,PEG
PEGATRON COMPUTER INC Engineer: Joyoung_Chianhg
Size C | Project Name MA50 | Rev 1.0
Date: Monday, February 13, 2012 | Sheet 21 of 93


U2001C
DMI
FDI
System Power Management
DMI_RXN0
DMI_RXN1
DMI_RXN2
DMI_RXN3
DMI_RXP0
DMI_RXP1
DMI_RXP2
DMI_RXP3
DMI_TXN0
DMI_TXN1
DMI_TXN2
DMI_TXN3
DMI_TXP0
DMI_TXP1
DMI_TXP2
DMI_TXP3
DMI_COMP_R
RBIAS_CPY
FDI_TXN0
FDI_TXN1
FDI_TXN2
FDI_TXN3
FDI_TXN4
FDI_TXN5
FDI_TXN6
FDI_TXN7
FDI_RXP0
FDI_RXP1
FDI_RXP2
FDI_RXP3
FDI_RXP4
FDI_RXP5
FDI_RXP6
FDI_RXP7
FDI_INT
FDI_FSYNC0
FDI_FSYNC1
FDI_LSYNC0
FDI_LSYNC1
DSWODVREN
PCH_DPROK
PCIE_WAKE#
SUSACK#
SYS_RESET#
SYS_PWROK
PWROK
APWROK
DRAMPWROK
RSMRST#
SUSWARN#/SUSPWRDNACK/GPIO30
PWRBTN#
ACPRESENT/GPIO31
BATLOW#/GPIO72
RI#
CLKRUN#/GPIO32
SUS_STAT#/GPIO61
SUSCLK/GPIO62
SLP_S5#/GPIO63
SLP_S4#
SLP_S3#
SLP_A#
SLP_SUS#
PMSYNCH
SLP_LAN#/GPIO29
02V000000001
COUGAR_POINT_ES1
+3VSUS_ORG
+3VS
+VTT_PCH_ORG
+3VA
+VCC_RTC
+5VSUS
+12VSUS
DSWODVREN - On Die DSW VR Enable
HIGH - Enabled(DEFAULT) ; LOW-Disabled
Remove SUSACK#.
R1.0
Add XDP_DBRESET#
SYS_PWROK for PCH
R1.1 Remove some SP in P22
R1.1 IOAC, 10/31
Add ME_PWROK.
PM_RSMRST# has pull down 10k ohm in EC
R1.0
Add PM_PWRBTN#_R
U2201
Vcc=2~5.5
PM_PWROK
DELAY_VR_AND_ALL_SYS
SYS_PWROK
R1.0
PM_CLKRUN#
PM_PWROK
GND
RI#
BATLOW#
R1.0
PCIE_WAKE#
ME_PM_SLP_M#
ME_SUSPWRDNACK
ME_AC_PRESENT
ME_PM_SLP_LAN#
PEGATRON
PEGATRON COMPUTER INC
Title : PCH(3)_FDI,DMI,SYS PWR
Engineer: Joyoung_Chianhg
Size C
Project Name MA50
Rev 1.0
Date: Monday, February 13, 2012
Sheet 22 of 93



CRT Disable: (For discrete graphic)

1. NC:
   CRT_RED,CRT_GREEN,CRT_BLUE
   CRT_HSYCN,CRT_VSYNC
2. 1-kΩ ±0.5% pull-down to GND:
   DAC_IREF
3. Connected to GND:
   CRT_ITRN
4. Connect to +V3.3:
   VCCADAC

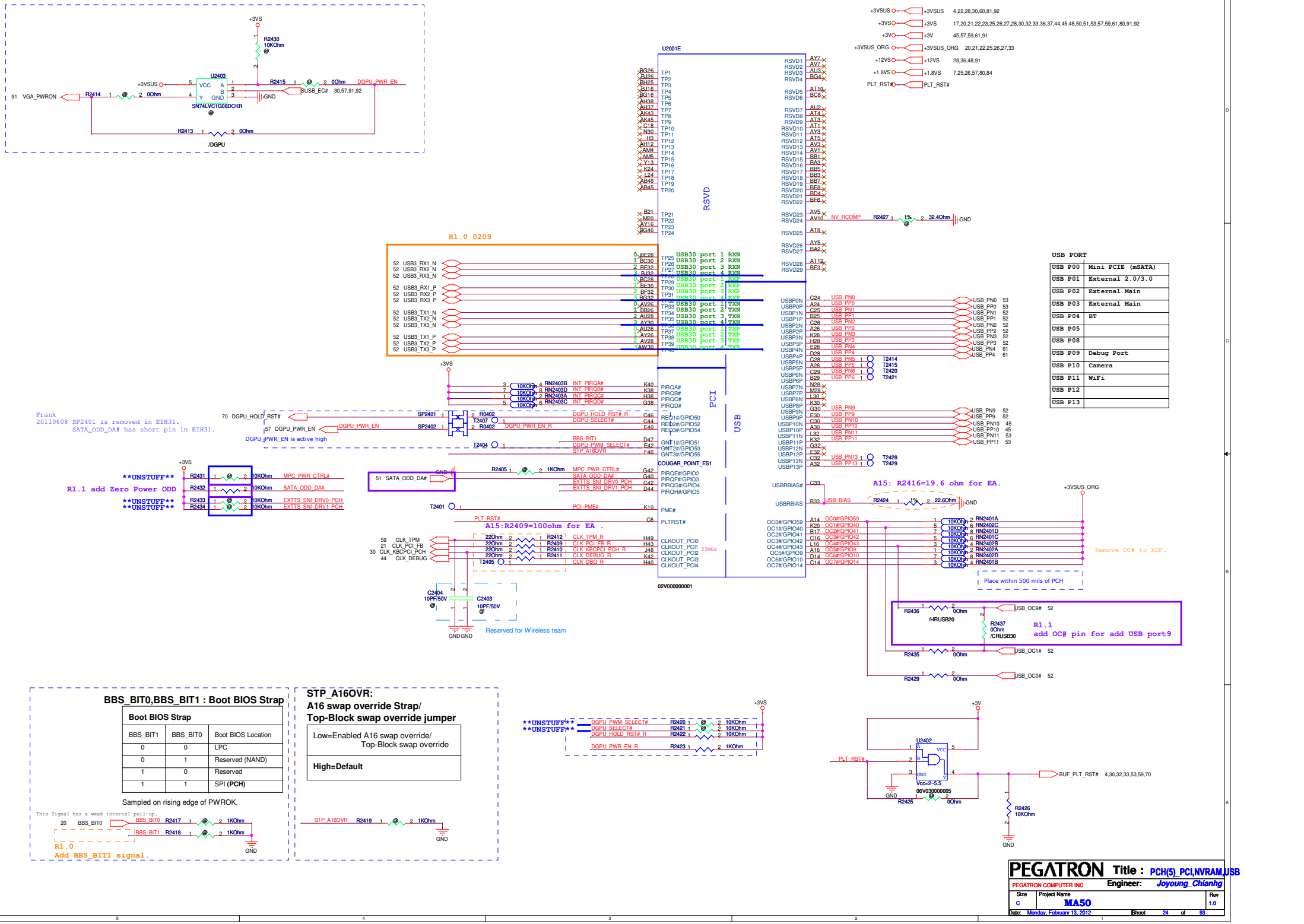
DisPlay Port Disable: (For discrete graphic)

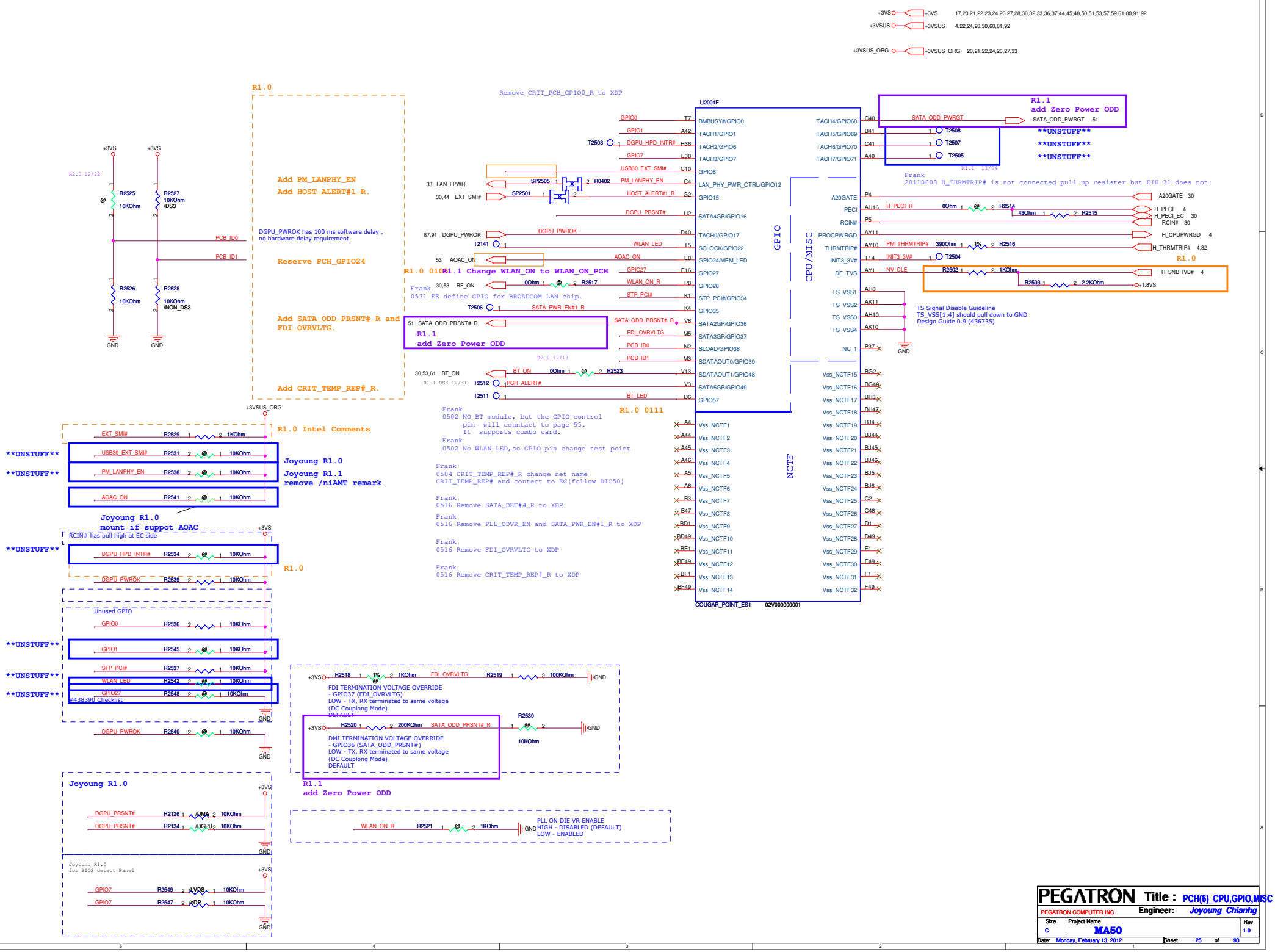
1. NC:
   ALL

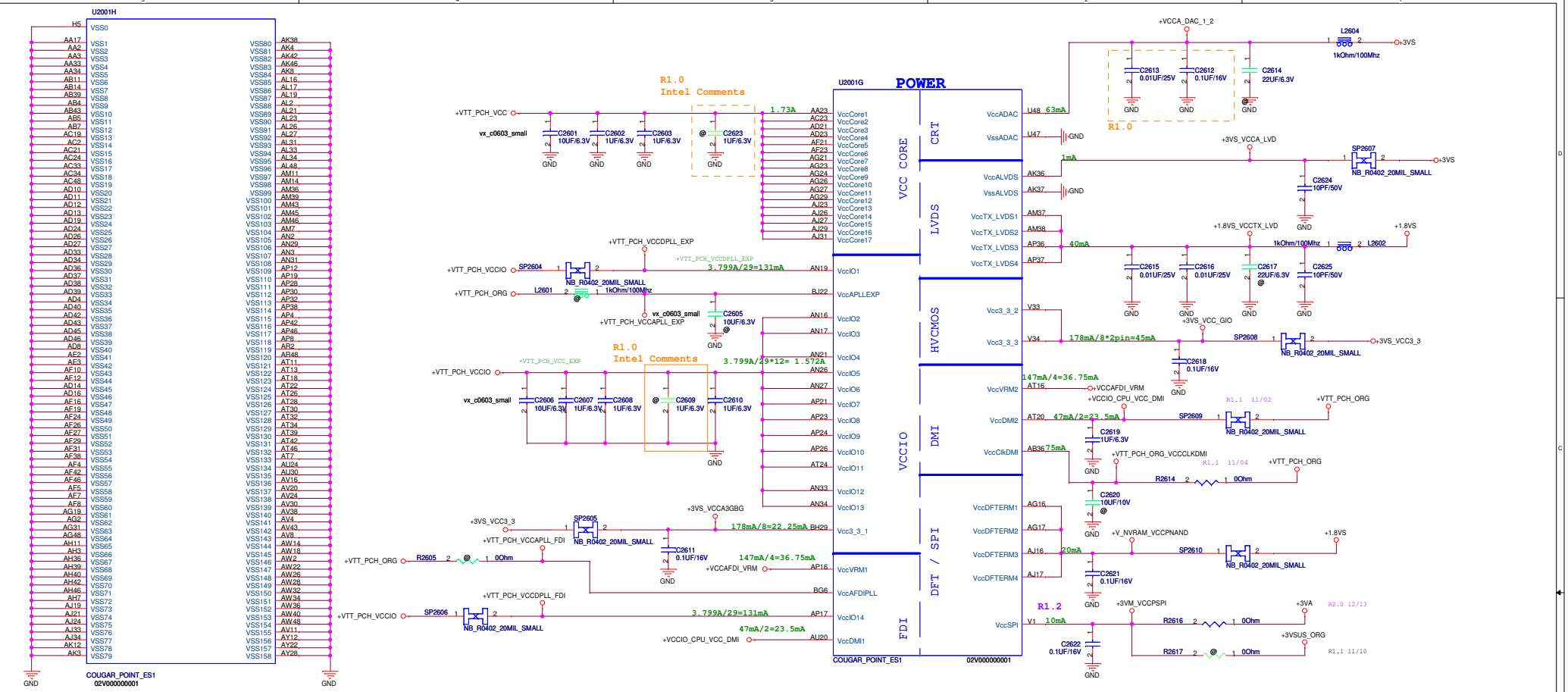
LVDS Disable: (For discrete graphic)

1. NC:
   LVDSA_DATA [3:0], LVDSA_DATA# [3:0],
   LVDSA_CLK, LVDSA_CLK#, LVDSB_DATA [3:0],
   LVDSB_DATA# [3:0], LVDSB_CLK, LVDSB_CLK#
   L_VDD_EN, L_BKLTEN, L_BKLTCTL, LVD_VREFH
   LVD_VREFL, LVD_IBG, LVD_VBG
2. Connected to GND:
   VccALVDS,VccTX_LVDS

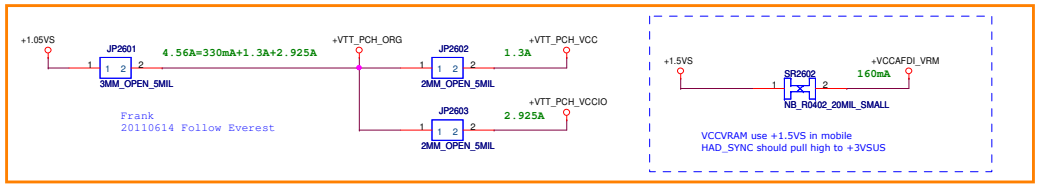
PEGATRON Title : PCH(4)_DP,LVDS,CRT
PEGATRON COMPUTER INC Engineer: Joyoung_Chianhg
Size: C | Project Name: MA50 | Rev: 1.0
Date: Monday, February 13, 2012 | Sheet 23 of 93


U2001E
RSVD
PCI
USB
COUGAR_POINT_ES1
02V000000001
R1.0 0209
USB PORT
USB P00 Mini PCIE (mSATA)
USB P01 External 2.0/3.0
USB P02 External Main
USB P03 External Main
USB P04 BT
USB P05
USB P08
USB P09 Debug Port
USB P10 Camera
USB P11 WiFi
USB P12
USB P13
Frank
20110608 SP2401 is removed in EIH31.
SATA_ODD_DA# has short pin in EIH31.
DGPU_PWR_EN is active high
UNSTUFF
R1.1 add Zero Power ODD
A15:R2409=100ohm for EA .
A15: R2416=19.6 ohm for EA.
Remove OC# to XDP.
Place within 500 mils of PCH
R1.1
add OC# pin for add USB port9
Reserved for Wireless team
BBS_BIT0,BBS_BIT1 : Boot BIOS Strap
Boot BIOS Strap
BBS_BIT1 BBS_BIT0 Boot BIOS Location
0 0 LPC
0 1 Reserved (NAND)
1 0 Reserved
1 1 SPI (PCH)
Sampled on rising edge of PWROK.
This Signal has a weak internal pull-up.
R1.0
Add BBS_BIT1 signal.
STP_A16OVR:
A16 swap override Strap/
Top-Block swap override jumper
Low=Enabled A16 swap override/
Top-Block swap override
High=Default
PEGATRON
Title : PCH(5)_PCI,NVRAM,USB
PEGATRON COMPUTER INC
Engineer: Joyoung_Chianhg
Size C
Project Name MA50
Rev 1.0
Date: Monday, February 13, 2012
Sheet 24 of 93


+3VS +3VS 17,20,21,22,23,24,26,27,28,30,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92
+3VSUS +3VSUS 4,22,24,28,30,60,81,92
+3VSUS_ORG +3VSUS_ORG 20,21,22,24,26,27,33
R1.0
Add PM_LANPHY_EN
Add HOST_ALERT#1_R.
DGPU_PWROK has 100 ms software delay , no hardware delay requirement
Reserve PCH_GPIO24
Add SATA_ODD_PRSNT#_R and FDI_OVRVLTG.
Add CRIT_TEMP_REP#_R.
Remove CRIT_PCH_GPIO0_R to XDP
U2001F
GPIO
CPU/MISC
NCTF
COUGAR_POINT_ES1 02V000000001
R1.1 add Zero Power ODD
UNSTUFF
UNSTUFF
UNSTUFF
Frank 20110608 H_THRMTRIP# is not connected pull up resister but EIH 31 does not.
R1.0 0106 R1.1 Change WLAN_ON to WLAN_ON_PCH
Frank 0531 EE define GPIO for BROADCOM LAN chip.
R1.0 0111
Frank 0502 NO BT module, but the GPIO control pin will conntact to page 55. It supports combo card.
Frank 0502 No WLAN LED,so GPIO pin change test point
Frank 0504 CRIT_TEMP_REP#_R change net name CRIT_TEMP_REP# and contact to EC(follow BIC50)
Frank 0516 Remove SATA_DET#4_R to XDP
Frank 0516 Remove PLL_ODVR_EN and SATA_PWR_EN#1_R to XDP
Frank 0516 Remove FDI_OVRVLTG to XDP
Frank 0516 Remove CRIT_TEMP_REP#_R to XDP
TS Signal Disable Guideline
TS_VSS[1:4] should pull down to GND
Design Guide 0.9 (436735)
R1.0 Intel Comments
Joyoung R1.0
Joyoung R1.1
remove /niAMT remark
Joyoung R1.0
mount if suppot AOAC
RCIN# has pull high at EC side
R1.0
Unused GPIO
#438390 Checklist
FDI TERMINATION VOLTAGE OVERRIDE
- GPIO37 (FDI_OVRVLTG)
LOW - TX, RX terminated to same voltage
(DC Couplong Mode)
DEFAULT
DMI TERMINATION VOLTAGE OVERRIDE
- GPIO36 (SATA_ODD_PRSNT#)
LOW - TX, RX terminated to same voltage
(DC Couplong Mode)
DEFAULT
R1.1 add Zero Power ODD
PLL ON DIE VR ENABLE
HIGH - DISABLED (DEFAULT)
LOW - ENABLED
Joyoung R1.0
Joyoung R1.0 for BIOS detect Panel
PEGATRON
Title : PCH(6)_CPU,GPIO,MISC
PEGATRON COMPUTER INC
Engineer: Joyoung_Chianhg
Size C
Project Name MA50
Rev 1.0
Date: Monday, February 13, 2012
Sheet 25 of 93



R1.0

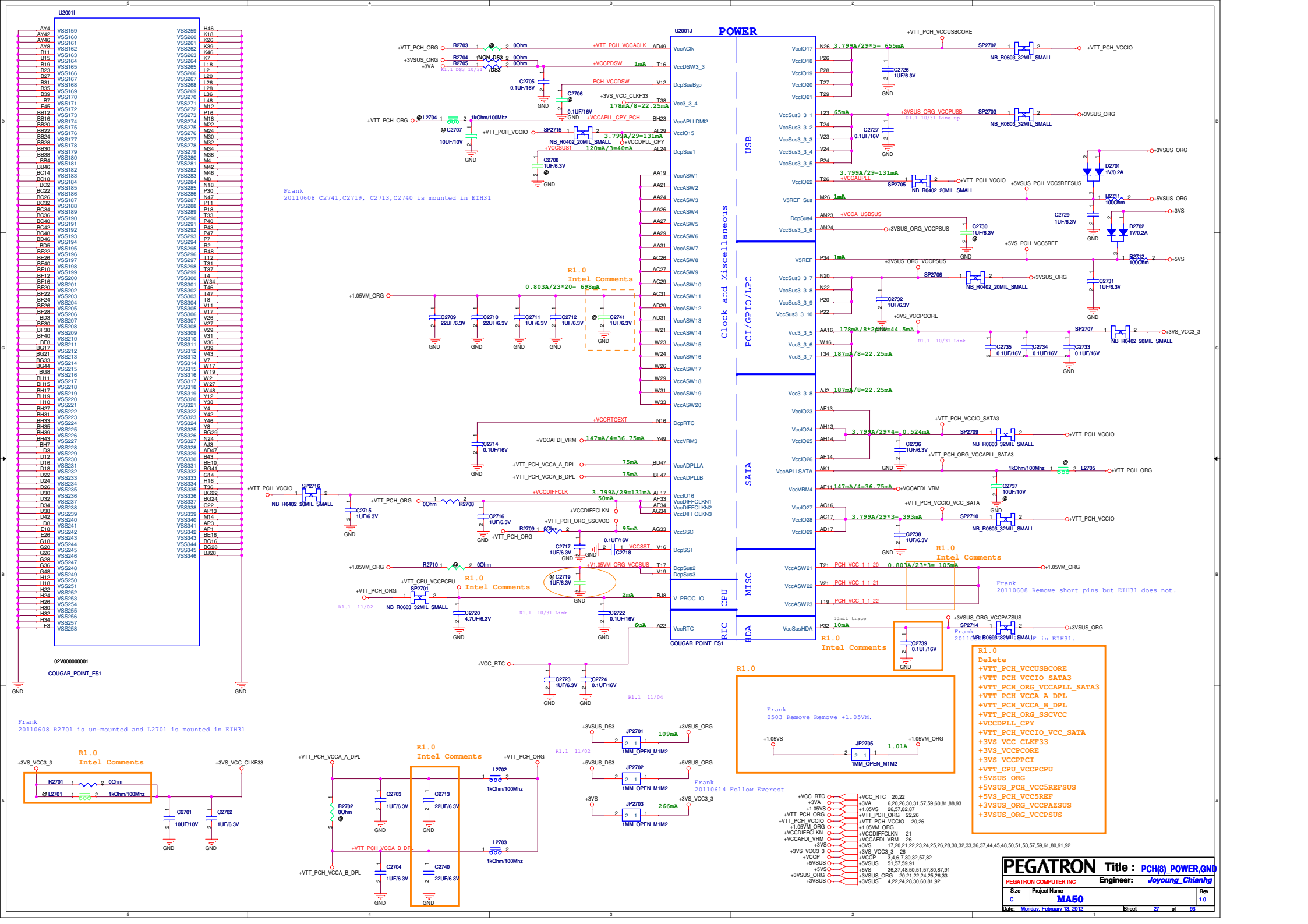


Frank
20110608 EVERST remove 1.8VS and +VTT_PCH_ORG

+VTT_PCH_VCCIO	+VTT_PCH_VCCIO	20,27
+VTT_PCH_ORG	+VTT_PCH_ORG	22,27
+1.05VS	+1.05VS	27,57,82,87
+1.5VS	+1.5VS	7,53,57,91
+VCCAFDI_VRM	+VCCAFDI_VRM	27
+3VS	+3VS	17,20,21,22,23,24,25,27,28,30,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92
+3VS_VCC3_3	+3VS_VCC3_3	27
+3VM_SPI	+3VM_SPI	28
+1.8VS	+1.8VS	7,25,57,80,84
+VCCP	+VCCP	3,4,6,7,30,32,57,82

R1.0
Delete
+VTT_PCH_VCC
+VTT_PCH_VCCDPLL_EXP
+VTT_PCH_VCCAPLL_EXP
+VTT_PCH_VCCDPLL_FDI
+VTT_PCH_VCCAPLL_FDI
+3VS_VCCA3GBG
+3VS_VCC_GIO
+VCCA_DAC_1_2
+3VS_VCCA_LVDS
+3VM_VCCPSPI
+V_NVRAM_VCCPNAND
+1.8VS_VCCTX_LVD
+VCCIO_CPU_VCC_DMI
+VTT_PCH_ORG_VCCCLKDMI

PEGATRON	Title :	PCH(7)_POWER,GND			
PEGATRON COMPUTER INC	Engineer:	Joyoung_Chianhg			
Size	Project Name		Rev		
C	MA50		1.0		
Date: Monday, February 13, 2012	Sheet	26	of	93	


POWER
U2001I
U2001J
COUGAR_POINT_ES1
02V000000001
USB
Clock and Miscellaneous
PCI/GPIO/LPC
SATA
MISC
CPU
RTC
HDA
Frank
20110608 C2741,C2719, C2713,C2740 is mounted in EIH31
R1.0
Intel Comments
0.803A/23*20= 698mA
Frank
20110608 R2701 is un-mounted and L2701 is mounted in EIH31
Frank
0503 Remove Remove +1.05VM.
Frank
20110614 Follow Everest
Frank
20110608 Remove short pins but EIH31 does not.
R1.0
Delete
+VTT_PCH_VCCUSBCORE
+VTT_PCH_VCCIO_SATA3
+VTT_PCH_ORG_VCCAPLL_SATA3
+VTT_PCH_VCCA_A_DPL
+VTT_PCH_VCCA_B_DPL
+VTT_PCH_ORG_SSCVCC
+VCCDPLL_CPY
+VTT_PCH_VCCIO_VCC_SATA
+3VS_VCC_CLKF33
+3VS_VCCPCORE
+3VS_VCCPPCI
+VTT_CPU_VCCPCPU
+5VSUS_ORG
+5VSUS_PCH_VCC5REFSUS
+5VS_PCH_VCC5REF
+3VSUS_ORG_VCCPAZSUS
+3VSUS_ORG_VCCPSUS
PEGATRON
Title : PCH(8)_POWER,GND
PEGATRON COMPUTER INC
Engineer: Joyoung_Chianhg
Size C
Project Name MA50
Rev 1.0
Date: Monday, February 13, 2012
Sheet 27 of 93

PCH SPI ROM

SHARE ROM CONFIG1

U2801	@	
U2802	@	
U2803	ME+BIOS+CONFIG	4MB

ummount:
R2855, R2856, R2864, R2865, R2853, R2852, R2834, R2850, R2851, R2832, C2803, U2802,R2869, R2870, R2868, D2802, U2801

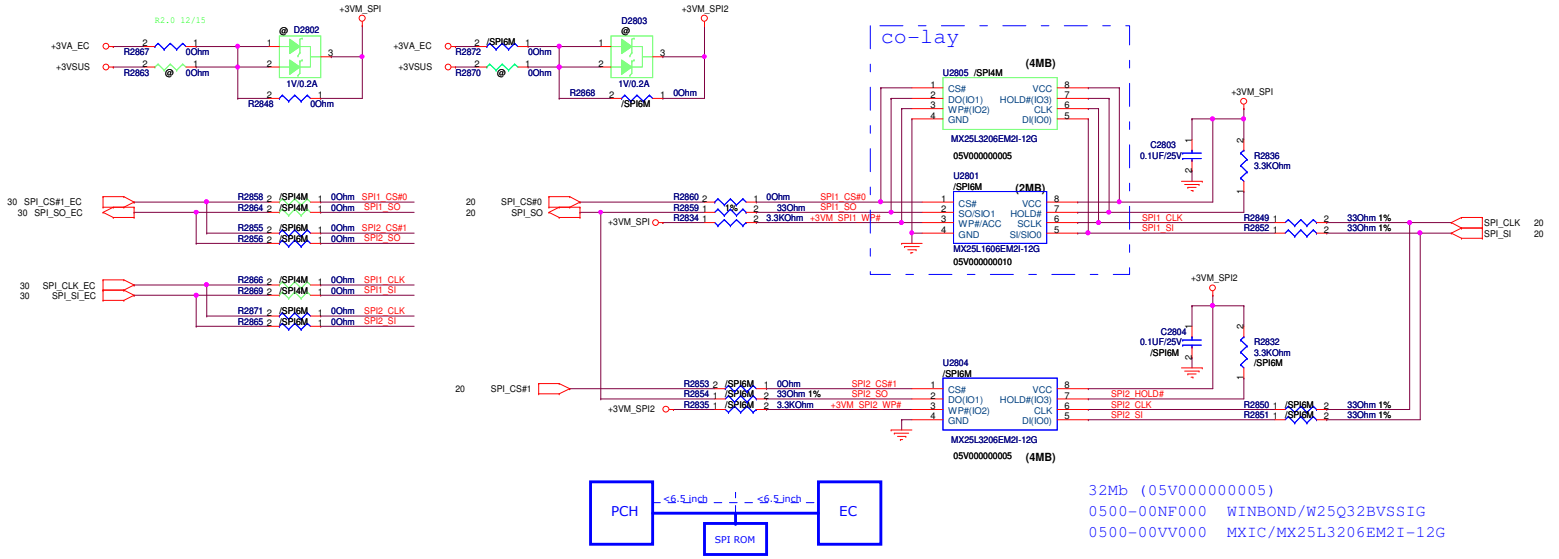
SHARE ROM CONFIG2

U2801	ME Firmware	2MB
U2802	EC+BIOS	4MB

ummount:
R2858, R2862, R2866, R2867, U2803

PCH SPI ROM

+3VA_EC reserved for share ROM

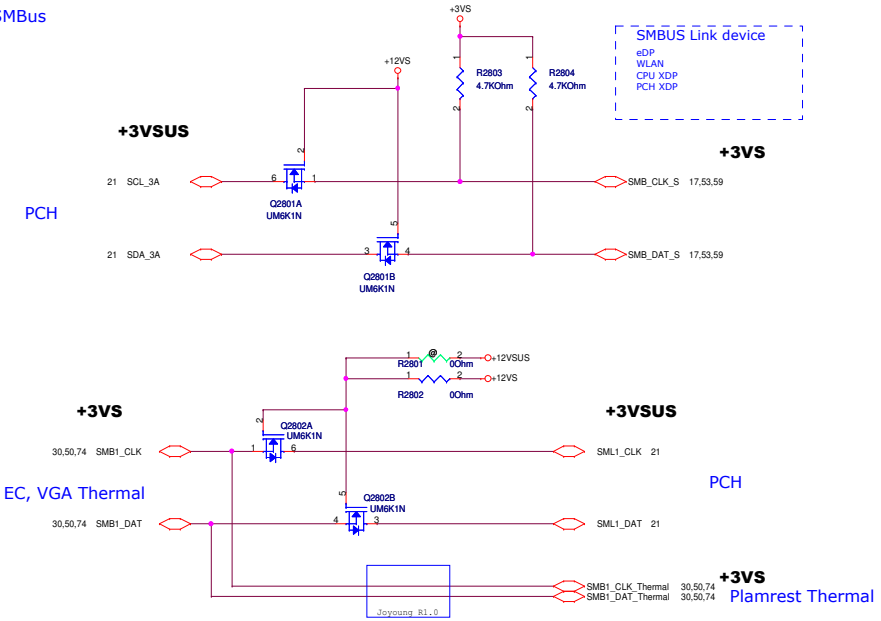


32Mb (05V000000005)
0500-00NF000 WINBOND/W25Q32BVSSIG
0500-00VV000 MXIC/MX25L3206EM2I-12G

SPI Debug Connector

layout space issue, so remove J2801.

PCH SMBus



PEGATRON Title : PCH(9)_SPI,SMB
PEGATRON COMPUTER INC Engineer: Joyoung_Chianhg
Size C | Project Name MA50 | Rev 1.0
Date: Monday, February 13, 2012 | Sheet 28 of 93

PEGATRON

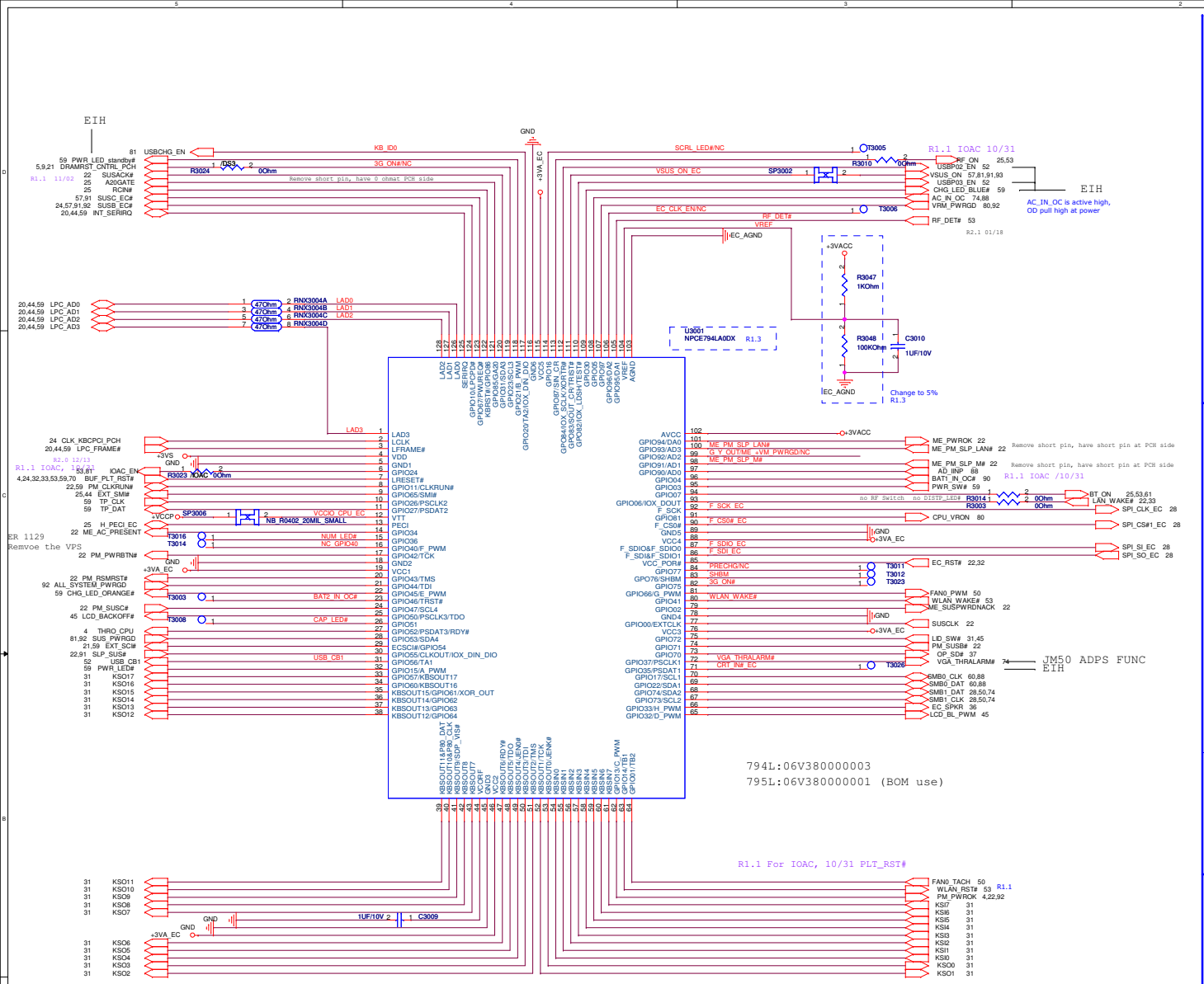
Title : CLK_ICS9LRS3197

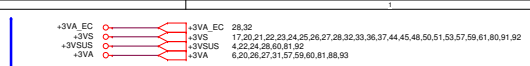
PEGATRON COMPUTER INC

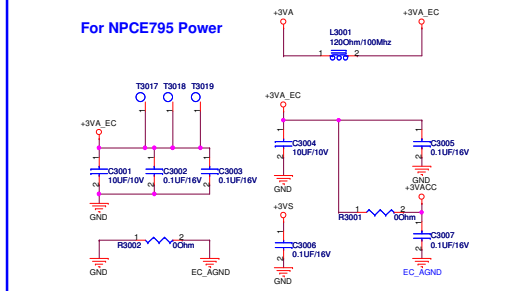
Engineer: Joyoung_Chianhg

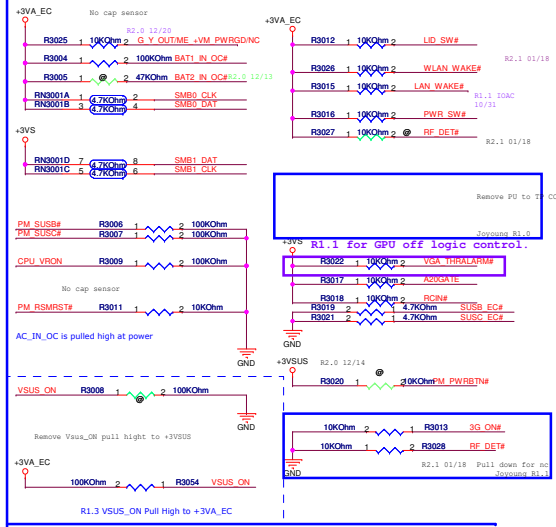
Size	Project Name	Rev
Custom	MA50	1.0

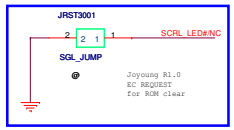
Date: Monday, February 13, 2012 Sheet 29 of 93











PEGATRON Title : NPCE794L

Engineer: Joyoung_Chianhg

Size	Project Name	Rev
Custom	MA50	1.3

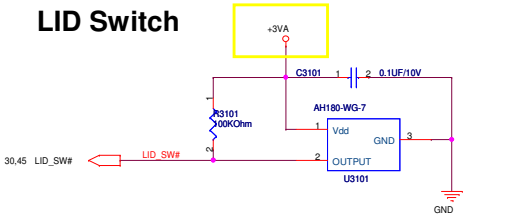
Date: Monday, February 13, 2012 Sheet 30 of 93

+5VS +5VS 27,36,37,48,50,51,57,80,87,91

SR=85

R1.0 change net name. Joyoung 0630

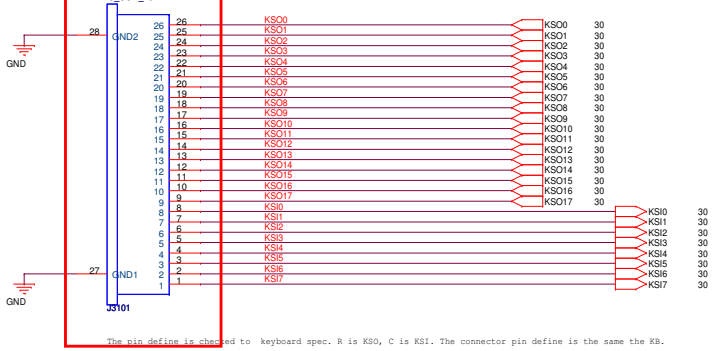
LID Switch



Keyboard

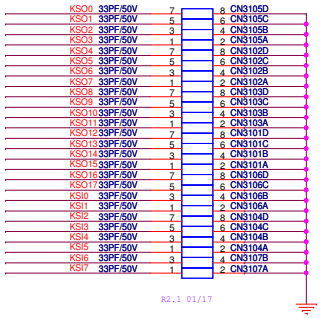
12V18ABSM012

FPC_CON_26P



The pin define is checked to keyboard spec. R is KSO, C is KSI. The connector pin define is the same the KB.

need check



R2.1 01/17

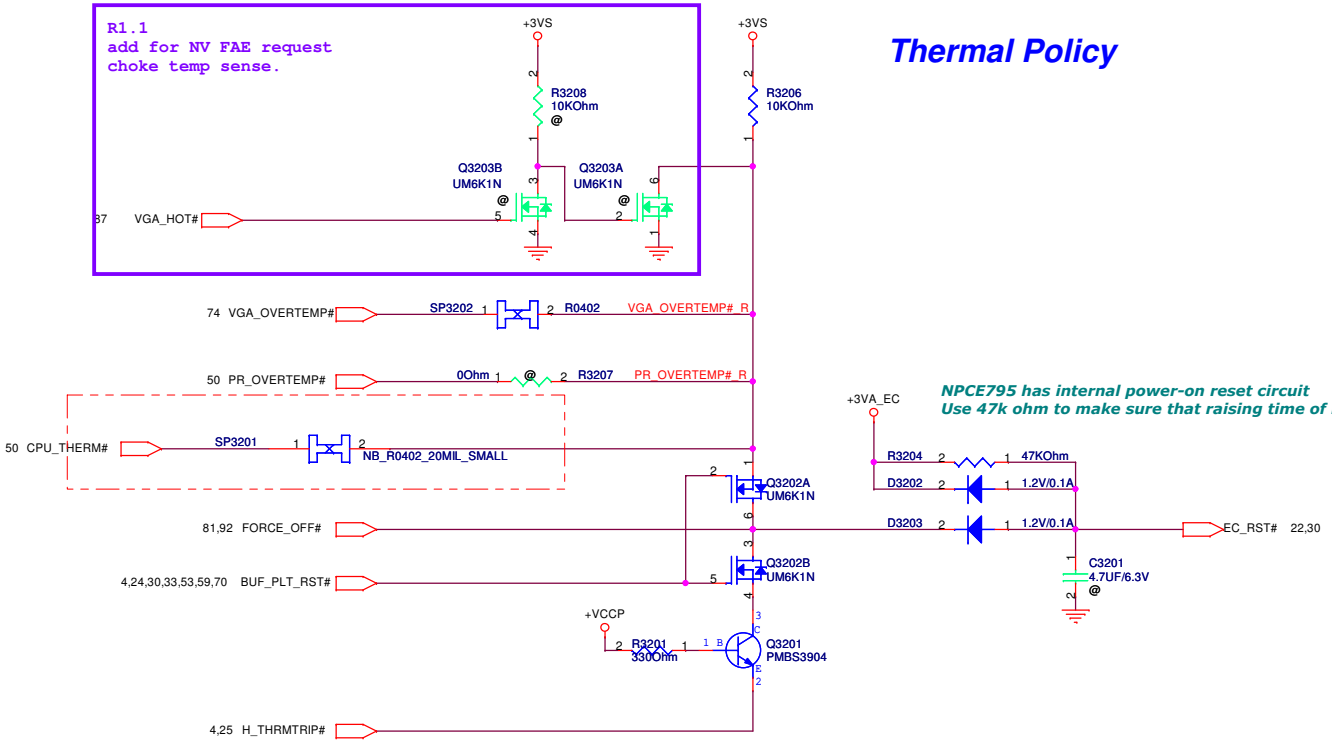
PEGATRON	Title : EC_IT8512(2)KB, TP,FP	
	Engineer: Joyoung_Chianhg	
Size: C	Project Name: MA50	Rev: 1.3
Date: Monday, February 13, 2012	Sheet 31 of 93	

+VCCP → +VCCP 3,4,6,7,30,57,82

+3VA_EC → +3VA_EC 28,30

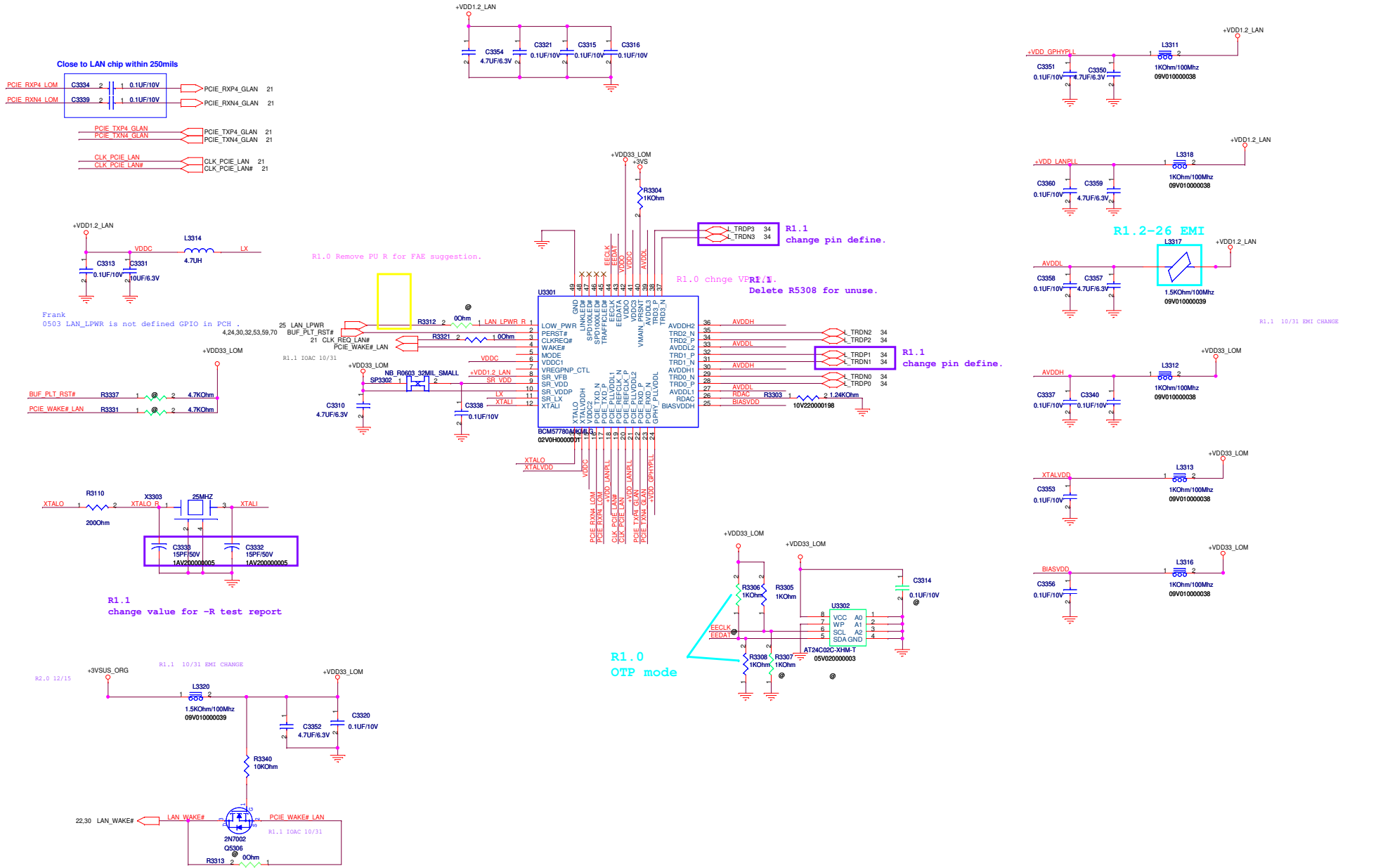
+3VS → +3VS 17,20,21,22,23,24,25,26,27,28,30,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92

Thermal Policy



NPCE795 has internal power-on reset circuit
Use 47k ohm to make sure that raising time of POR is less than 10us

PEGATRON	Title : RST_Reset Circuit		
<OrgName>	Engineer: Joyoung_Chianhg		
Size: Custom	Project Name: MA50		Rev: 1.0
Date: Monday, February 13, 2012	Sheet 32 of 93		



PEGATRON	Title : LAN_BCM57780		
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Joyoung_Chianhg		
Size: C	Project Name: MA50	Rev: 1.0	
Date: Monday, February 13, 2012	Sheet 33 of 93		

Joyoung R1.0
FAE suggest common mode choke is on chip side.

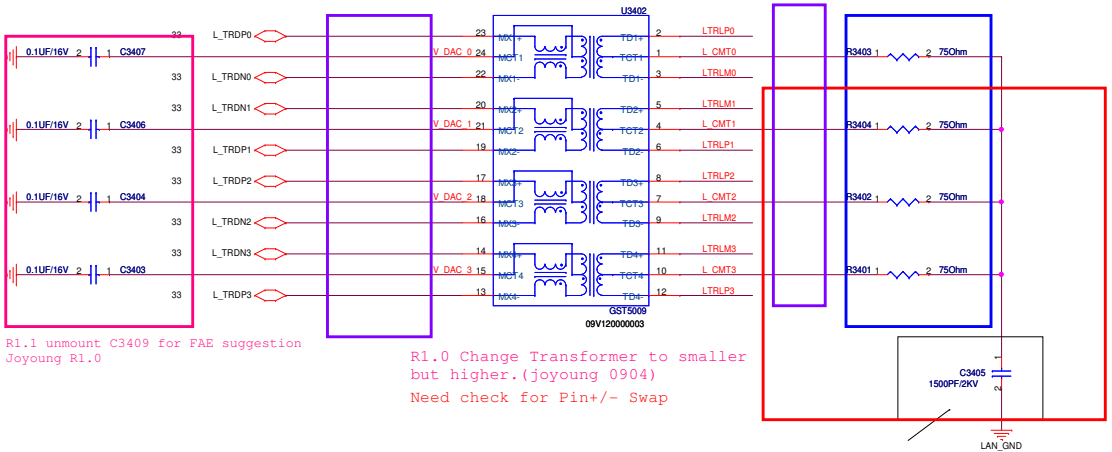
R1.1 Add 0 OHM for FAE suggestion 0809
JM50: FAE suggest remove

R1.1 Swap L_TRDP3 L_TRDN3 & L_TRDP1 L_TRDN1

R1.1 remove CAP of V_DAC_3, V_DAC_2 and V_DAC_1 for FAE suggestion

R1.1 Remove R3405~R3407 & C3409

R1.1 Mount R3401~R3403 for FAE suggestion 0809



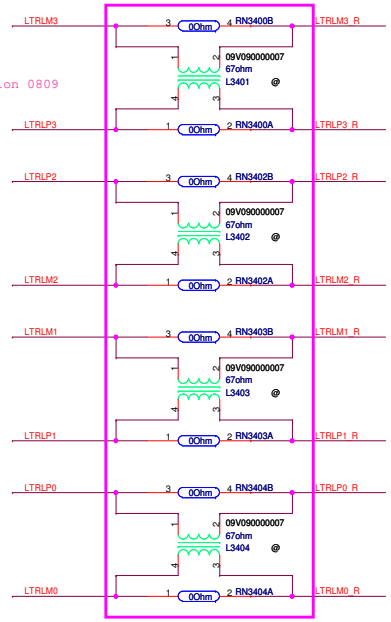
R1.1 unmount C3409 for FAE suggestion
Joyoung R1.0

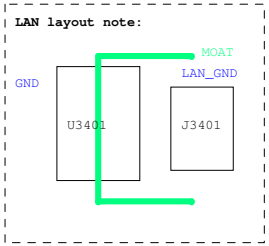
R1.0 Change Transformer to smaller but higher.(joyoung 0904)

Need check for Pin+/- Swap

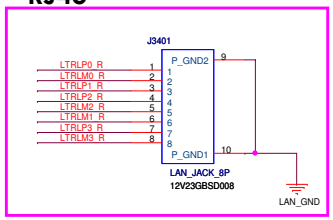
PR_S12

Co-lay C3409 & C3411
Co-lay C3410 & C3412



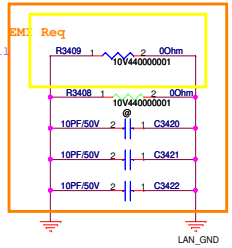


RJ45



Change RJ45 CON3401

R1.1 EMI Request 4.7PF & Set Close to Connector, then removed all



R1.0 Reserve D3401 for EMI.

R1.0 Mount R3408 for FAE suggestion

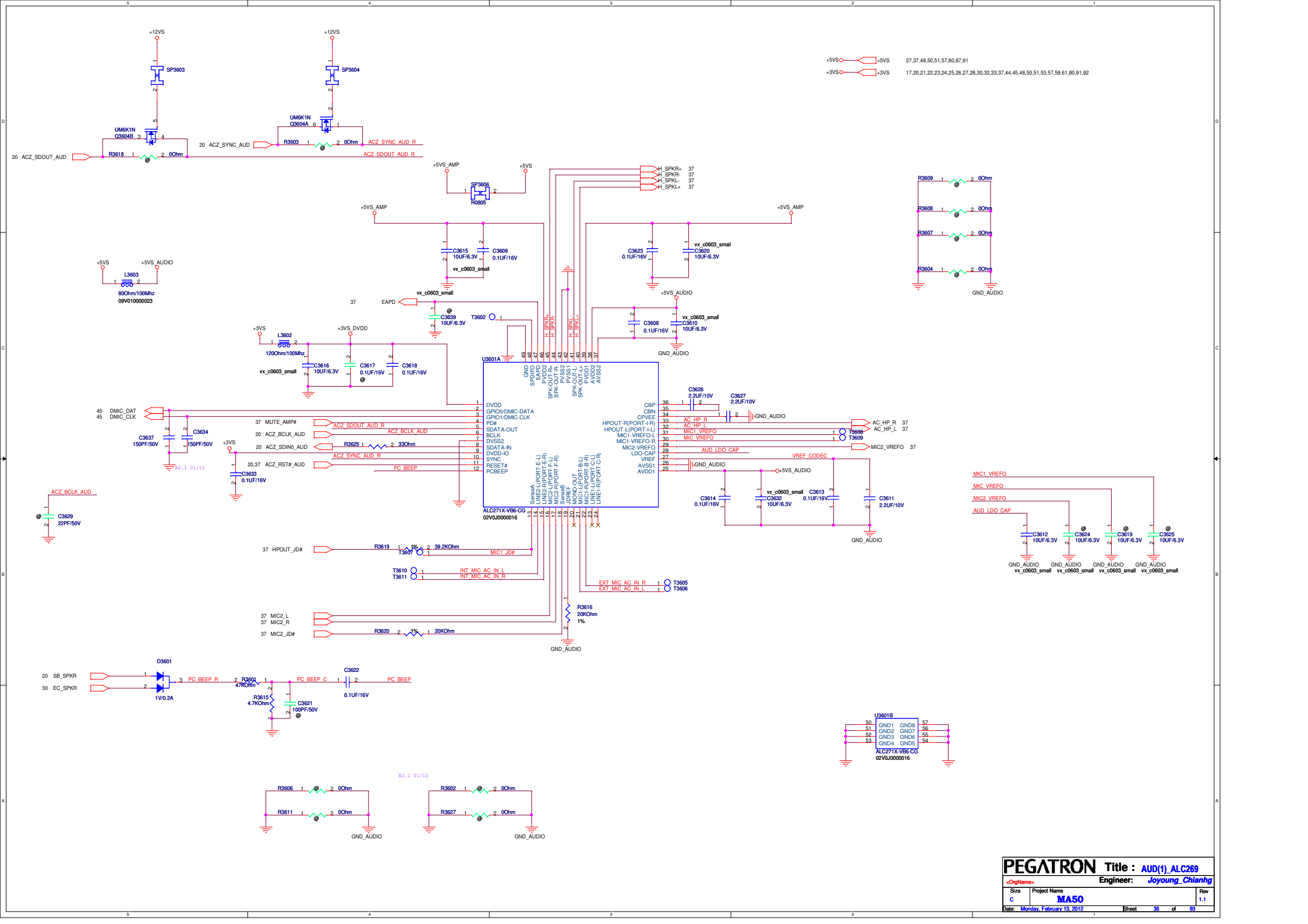
PEGATRON	Title : RJ45	
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Joyoung_Chianhg	
Size: C	Project Name: MA50	Rev: 1.0
Date: Monday, February 13, 2012	Sheet 34 of 93	

PEGATRON Title : MDC CONN

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	MA50	1.3

Date: Monday, February 13, 2012 Sheet 35 of 93



PEGATRON	Title : AUD(1)_ALC269		
<OrgName>	Engineer: Joyoung_Chianhg		
Size: C	Project Name: MA50		Rev: 1.1
Date: Monday, February 13, 2012	Sheet 36 of 93		

+5VS → +5VS 27,36,48,50,51,57,80,87,91

+3VS → +3VS 17,20,21,22,23,24,25,26,27,28,30,32,33,36,44,45,48,50,51,53,57,59,61,80,91,92

+5VS_AUDIO → +5VS_AUDIO 36

Internal Speaker Conn.

add R3706, R3707, R3708, R3709 for EMI request

H_SPKR+ 36
H_SPKR- 36
H_SPKL+ 36
H_SPKL- 36

R3706 1 2 0Ohm
R3707 1 2 0Ohm
R3708 1 2 0Ohm
R3709 1 2 0Ohm

J3704
1 SIDE1
2
3
4 SIDE2
5
6
WtoB_CON_4P
12V17GIRM002

C3710 1000PF/50V @
C3711 1000PF/50V @
C3712 1000PF/50V @
C3713 1000PF/50V @

R1.1 Reserved for EMI & Change to 1000PF

MIC2_JD# 36

COMBO_MIC
R3701 1 2 22KOhm R1.1 10/31 KEVIN
C3701 10UF/6.3V
Q3701 2N7002
GND_AUDIO
GND_AUDIO

Need change 0702-0028000 in next stage

R2.0 12/16
R1.1 10/31 KEVIN

36 MIC2_VREFO
R3710 1 2 2.2KOhm
COMBO_MIC
R3714 1 2 1KOhm
R3711 22KOhm 10V240000016
GND_AUDIO

C3702 2.2UF/10V → MIC2_R 36
C3703 2.2UF/10V → MIC2_L 36

add R3722, R3723 and C3723, C3725 change 100pFfor EMI request

ER1.11

COMBO_MIC
36 AC_HP_L
36 AC_HP_R
36 HPOUT_JD#

L3701 1 2 120Ohm/100Mhz
L3703 1 2 120Ohm/100Mhz
L3702 1 2 120Ohm/100Mhz

R3713 1 2 51Ohm
R3712 1 2 51Ohm

COMBO_MIC_CON
GND_AUDIO
HP_L_CON
HP_R_CON
GND_AUDIO
HPOUT_JD#

J3701
M6
M5_1
M5_2
M4
M1
MP
MO
PHONE_JACK_7P
12V14GBSD015
need check

C3704 100PF/50V
C3705 100PF/50V
C3709 100PF/50V
GND_AUDIO GND_AUDIO GND_AUDIO

Close J6701

+3VS
+5VS
R3704 10KOhm @
R3702 1KOhm @
D3702 @ RB751V-40
07V030000013
D3701 BAT54AW
1V/0.1A

36 EAPD
20,36 ACZ_RST#_AUD
30 OP_SD#
MUTE_AMP# 36

+5VA
+5VS
R3705 100KOhm
R3703 10KOhm
MUTE_AMP#
Q3704 2N7002
Q3705A UM6K1N
OP_SD#
Q3705B UM6K1N
ACZ_RST#_AUD
GND

COMBO_MIC
C3706 10PF/50V @
C3707 33PF/50V @
GND_AUDIO

ER1.32

COMBO_MIC
D3706
AZ2025-01H.R7G
07V220000006
GND_AUDIO

R2.1 01/17

HP_R_CON
D3705
AZ2025-01H.R7G
07V220000006
GND_AUDIO

HPOUT_JD#
D3704
AZ2025-01H.R7G
07V220000006
GND_AUDIO

HP_L_CON
D3703
AZ2025-01H.R7G
07V220000006
GND_AUDIO

EMI request

C3708 0.1UF/16V
GND GND_AUDIO

PEGATRON	Title : AUD(2)_AMP,JACK	
<OrgName>	Engineer: Joyoung_Chianhg	
Size: C	Project Name: MA50	Rev: 1.3
Date: Monday, February 13, 2012	Sheet 37 of 93	

PEGATRON Title : AUD(3)_FM2010

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	MA50	1.3

Date: Monday, February 13, 2012 Sheet 38 of 93

PEGATRON Title : AUD(4)_****

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
Custom	MA50	1.3

Date: Monday, February 13, 2012 Sheet 39 of 93

PEGATRON Title : TPM_****

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
B	MA50	1.3

Date: Monday, February 13, 2012 Sheet 40 of 93

PEGATRON Title : CB(2)_R5C833

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	MA50	1.3

Date: Monday, February 13, 2012 Sheet 41 of 93

17,20,21,22,23,24,25,26,27,28,30,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92

60,91

PEGATRON Title : CB(3)_4in1 CardReader

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	MA50	1.3

Date: Monday, February 13, 2012 Sheet 42 of 93

PEGATRON Title : CB(4)_NewCard

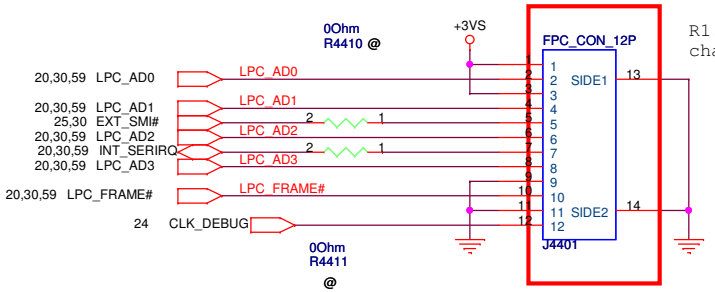
<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	MA50	1.3

Date: Monday, February 13, 2012 Sheet 43 of 93

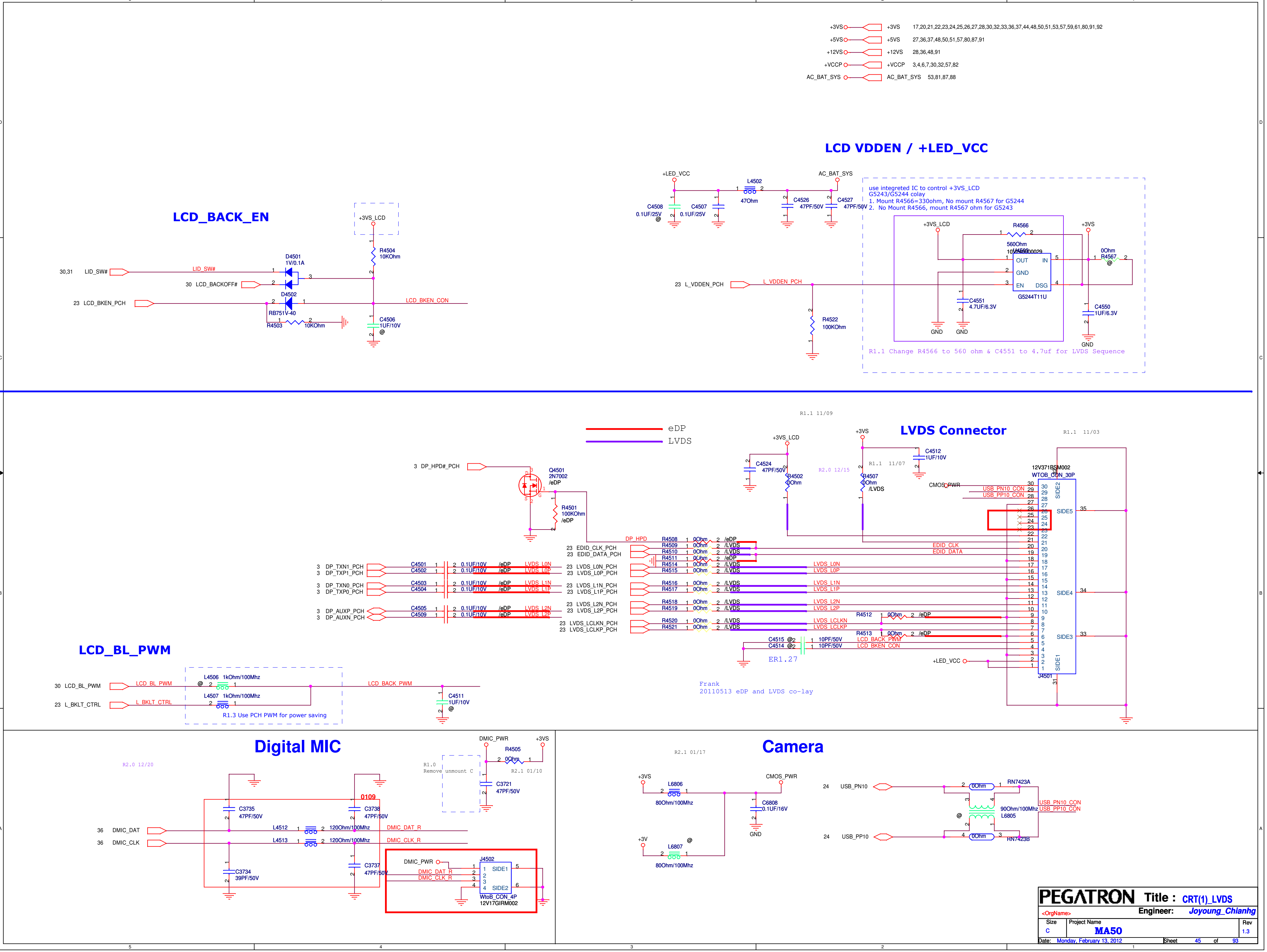
+3VS +3VS 17,20,21,22,23,24,25,26,27,28,30,32,33,36,37,45,48,50,51,53,57,59,61,80,91,92

LPC Debug Port



R1.1
change pin define to IEIE cable.

PEGATRON	Title : BUG_Debug	
<OrgName>	Engineer: Joyoung_Chianhg	
Size: B	Project Name: MA50	Rev: 1.3
Date: Monday, February 13, 2012	Sheet 44 of 93	


LCD VDDEN / +LED_VCC
LCD_BACK_EN
LVDS Connector
LCD_BL_PWM
Digital MIC
Camera
eDP
LVDS
use integreted IC to control +3VS_LCD
G5243/G5244 colay
1. Mount R4566=330ohm, No mount R4567 for G5244
2. No Mount R4566, mount R4567 ohm for G5243
R1.1 Change R4566 to 560 ohm & C4551 to 4.7uf for LVDS Sequence
R1.3 Use PCH PWM for power saving
Frank
20110513 eDP and LVDS co-lay
+3VS 17,20,21,22,23,24,25,26,27,28,30,32,33,36,37,44,48,50,51,53,57,59,61,80,91,92
+5VS 27,36,37,48,50,51,57,80,87,91
+12VS 28,36,48,91
+VCCP 3,4,6,7,30,32,57,82
AC_BAT_SYS 53,81,87,88
PEGATRON
Title : CRT(1)_LVDS
Engineer: Joyoung_Chianhg
Project Name MA50
Size C
Rev 1.3
Date: Monday, February 13, 2012
Sheet 45 of 93

PEGATRON Title : CRT

BU1-RD Div.1-HW RD Dept.1 Engineer: Joyoung_Chianhg

Size	Project Name	Rev
Custom	MA50	1.0

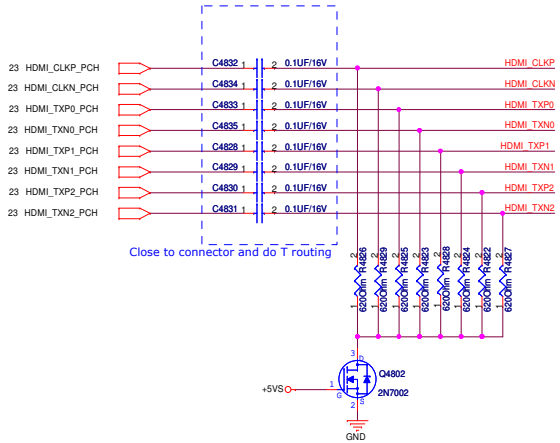
Date: Monday, February 13, 2012 Sheet 46 of 93

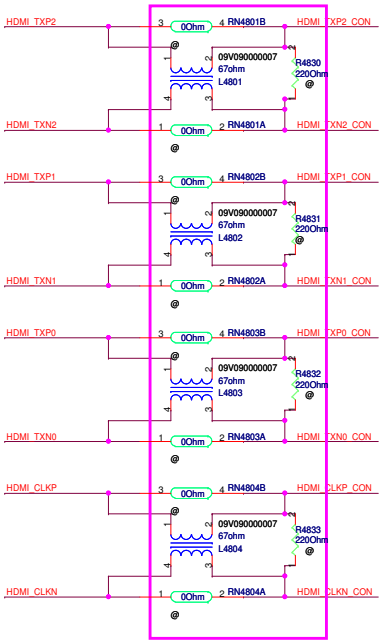
PEGATRON Title : CRT(3)_Display Port

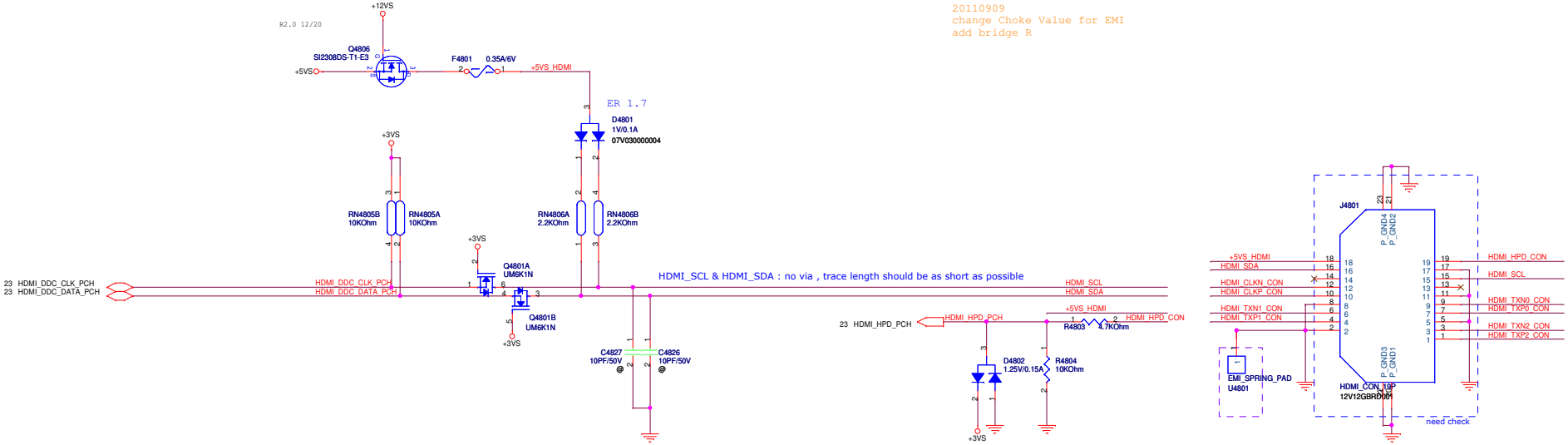
<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	MA50	1.3

Date: Monday, February 13, 2012 Sheet 47 of 93







R1.1 EMI Request for Spring PAD(close to HDMI conn)

+12VS	+12VS	28,36,91
+3VS	+3VS	17,20,21,22,23,24,25,26,27,28,30,32,33,36,37,44,45,50,51,53,57,59,61,80,91,92
+5VS	+5VS	27,36,37,50,51,57,80,87,91

PEGATRON Title : TV(1)_HDMI

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	MA50	1.3

Date: Monday, February 13, 2012 Sheet 48 of 93

PEGATRON Title : TV(2)_****

<OrgName> Engineer: Joyoung_Chianhg

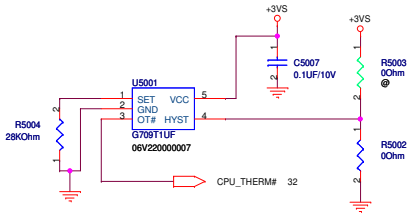
Size	Project Name	Rev
C	MA50	1.3

Date: Monday, February 13, 2012 Sheet 49 of 93

+3VS +3VS 17,20,21,22,23,24,25,26,27,28,30,32,33,36,37,44,45,48,51,53,57,59,61,80,91,92

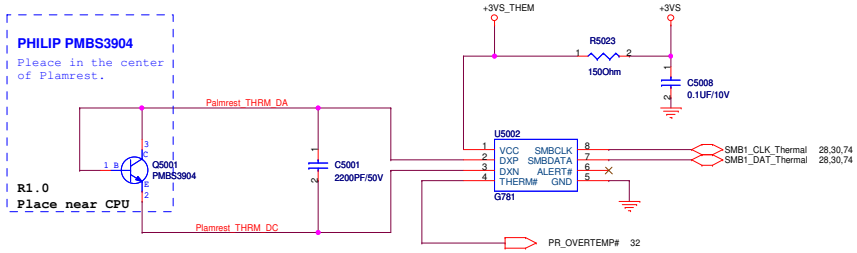
+5VS +5VS 27,36,37,48,51,57,80,87,91

CPU Thermal Sensor



(10°C for HYST =VCC)
(2°C for HYST = GND)
Hysteresis prevents the output from oscillating when the temperature is near the trip point.

DIMM Thermal Sensor

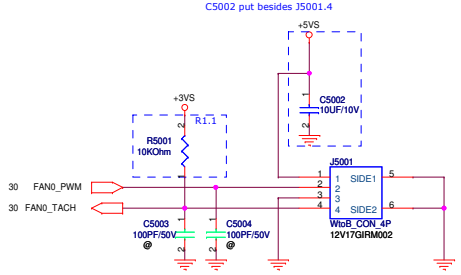


U5002 place neer power, CPU, PCH area,

SMBUS addr=1001100x (98)

U5002: Remote(Local) thermal sensor,use remote mode.

PWM Fan

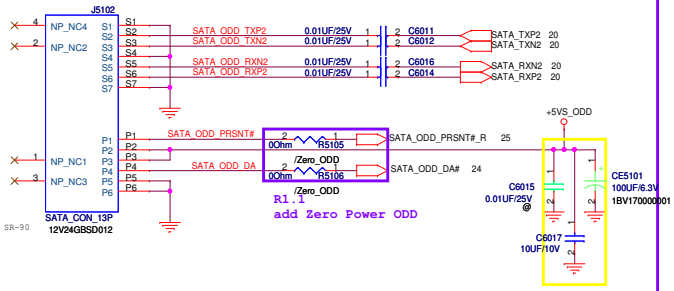


PEGATRON	Title : FAN_Fan,Sensor		
<OrgName>	Engineer: Joyoung_Chianhg		
Size: C	Project Name: MA50		Rev: 2.0
Date: Monday, February 13, 2012	Sheet 50 of 93		

+3VS +3VS 17,20,21,22,23,24,25,26,27,28,30,32,33,36,37,44,45,48,50,53,57,59,61,80,91,92

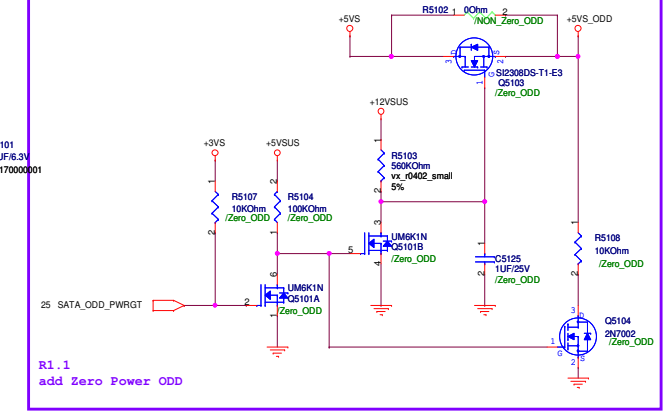
+5VS +5VS 27,36,37,48,50,57,80,87,91

ODD

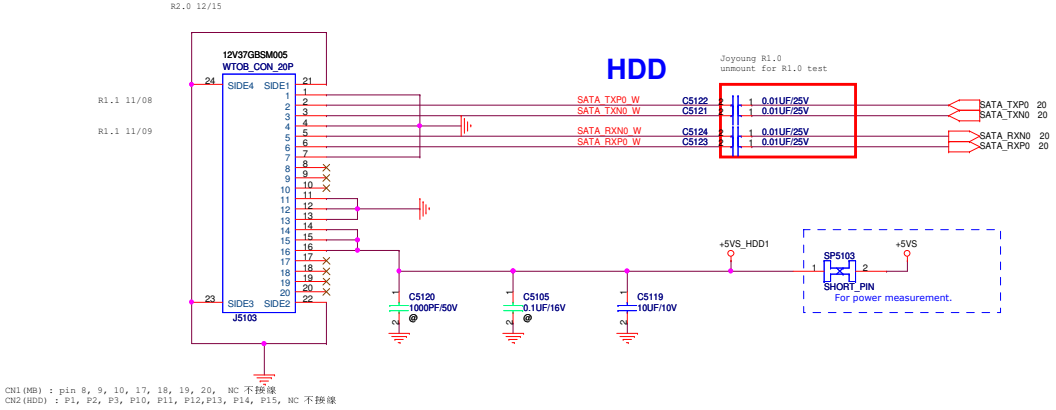


ZERO POWER ODD SUPPORT

support Hokey turn off ODD power



Connector for Cable



CN1(MB) : pin 8, 9, 10, 17, 18, 19, 20, NC 不接線
CN2(HDD) : P1, P2, P3, P10, P11, P12,P13, P14, P15, NC 不接線

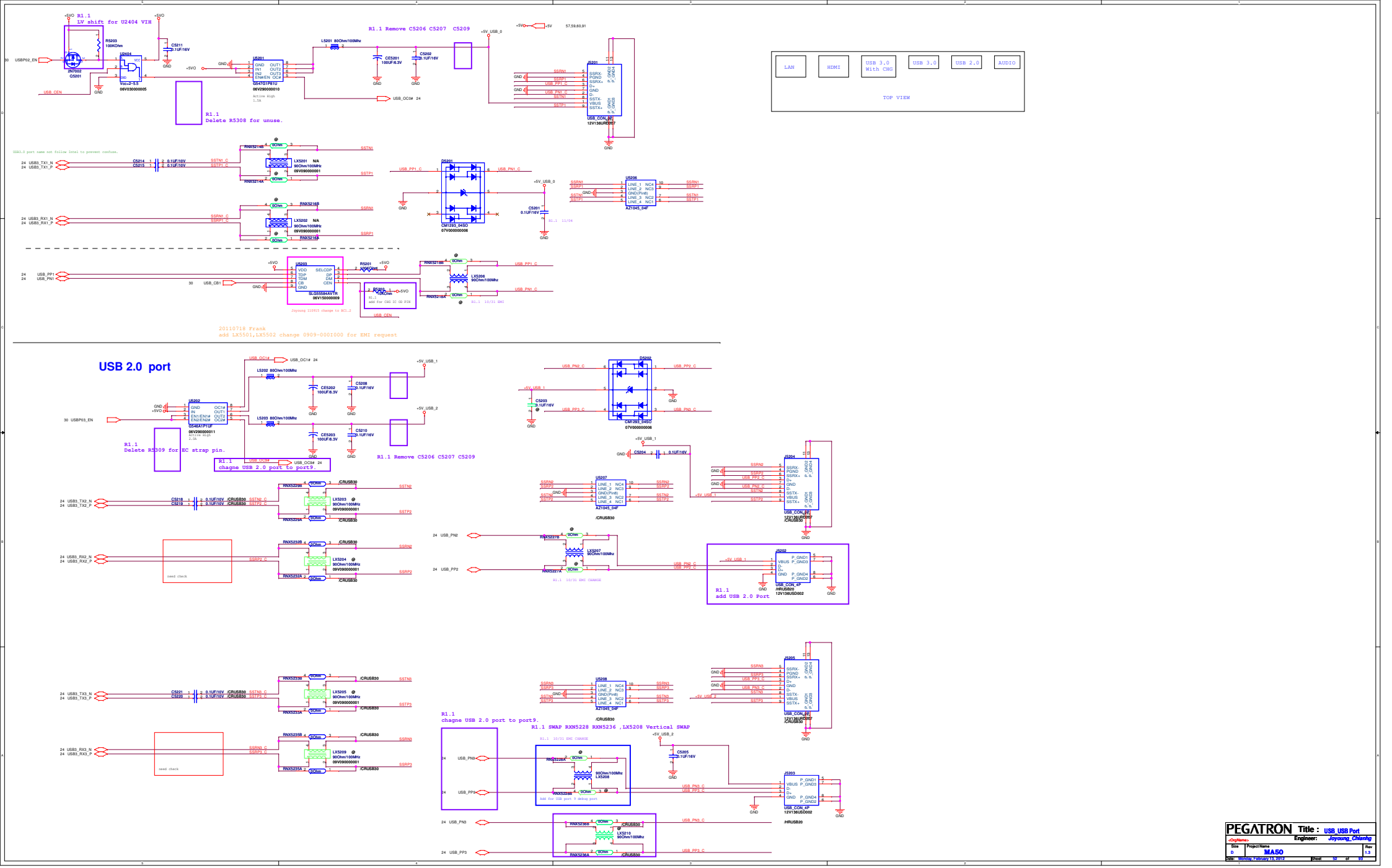
R1.1 11/02 Remove HDD SATA CONN PART

PEGATRON Title : XDD_HDD,ODD

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	MA50	1.3

Date: Monday, February 13, 2012 Sheet 51 of 93

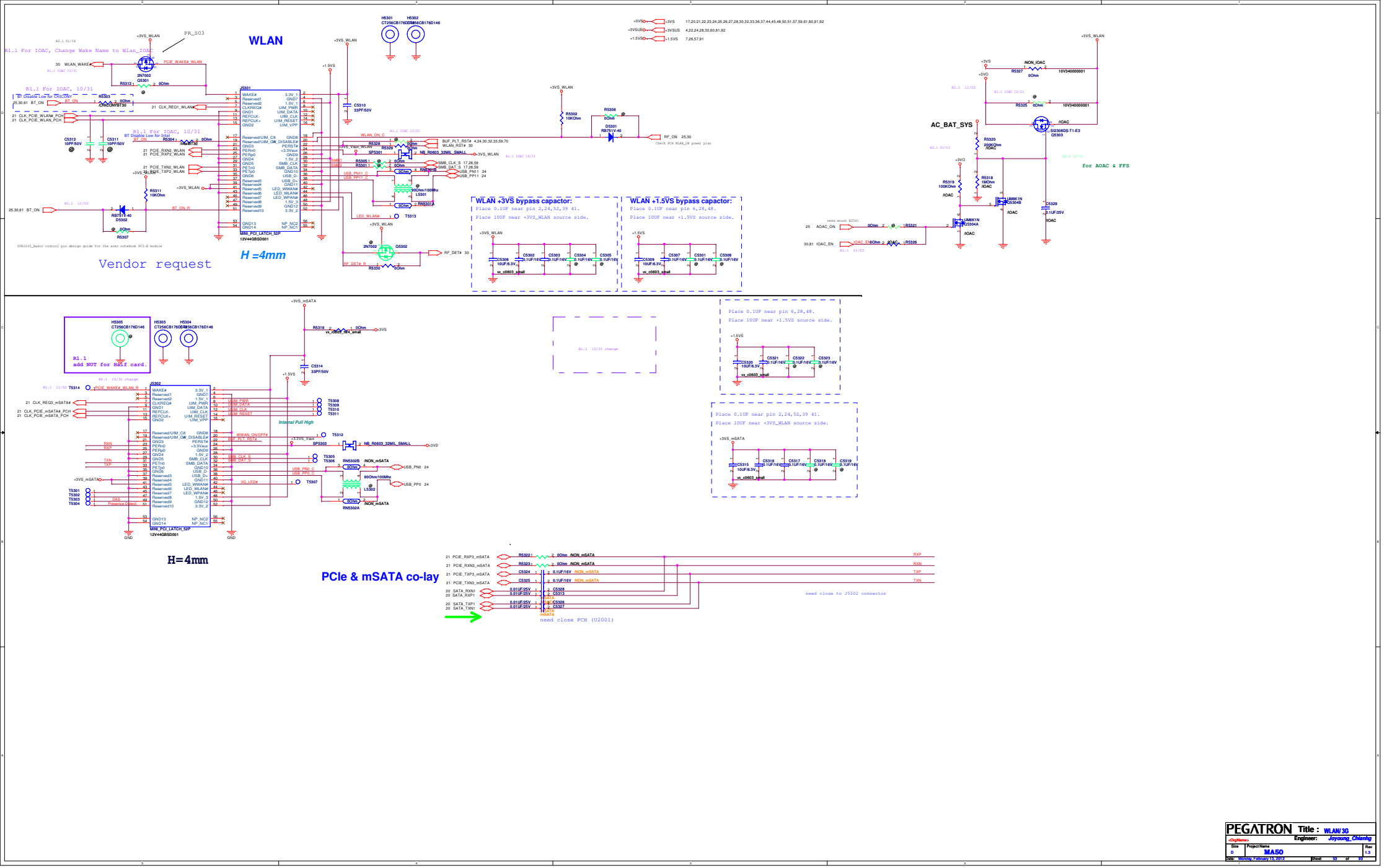


PEGATRON Title : USB_USB Port

Engineer: Joyoung_Chiang

Size: D | Project Name: MA50 | Rev: 1.3

Date: Monday, February 13, 2012 | Sheet 52 of 93



PEGATRON Title : WLAN/ 3G

Engineer: Joyoung_Chiang

Size: D | Project Name: MA50 | Rev: 1.3

Date: Monday, February 13, 2012 | Sheet 53 of 93

PEGATRON Title : USB3.0

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
B	MA50	1.3

Date: Monday, February 13, 2012 Sheet 54 of 93

PEGATRON Title : Fersco USB 3.0

BG1-CSC-HW R&D Dept.5 Engineer: Joyoung_Chianhg

Size	Project Name	Rev
A2	MA50	0.1

Date: Monday, February 13, 2012 Sheet 55 of 93

+3VA +3VA 6,20,26,27,30,31,57,59,60,81,88,93

+3VS +3VS 17,20,21,22,23,24,25,26,27,28,30,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92

+5VSUS +5VSUS 51,57,59,91

+5VA +5VA 37,60,81,91

+5V +5V 57,59,60,91

+5VS +5VS 27,36,37,48,50,51,57,80,87,91

AC_BAT_SYS AC_BAT_SYS 45,53,81,87,88

+3V +3V 24,45,57,59,61,91

30,59 PWR_LED#

30,59 PWR_LED_standby#

30,59 CHG_LED_BLUE#

30,59 CHG_LED_ORANGE#

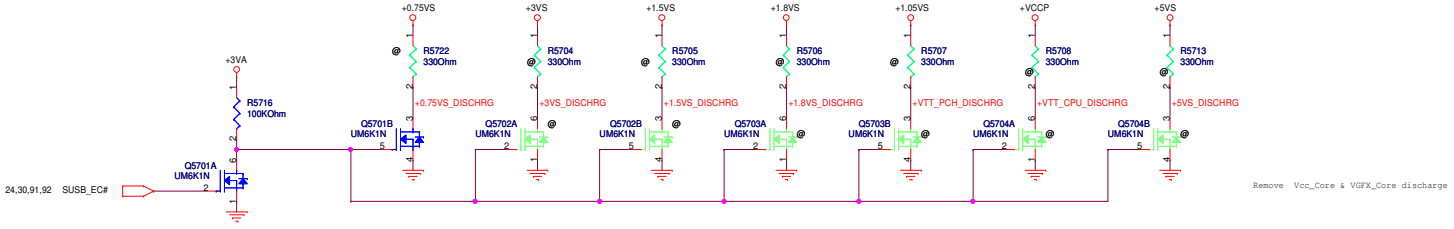
PEGATRON Title : LED_Indicator

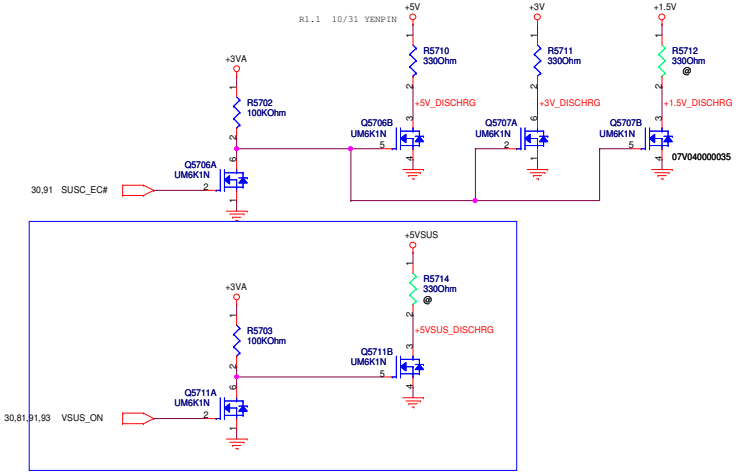
<OrgName> Engineer: Joyoung_Chianhg

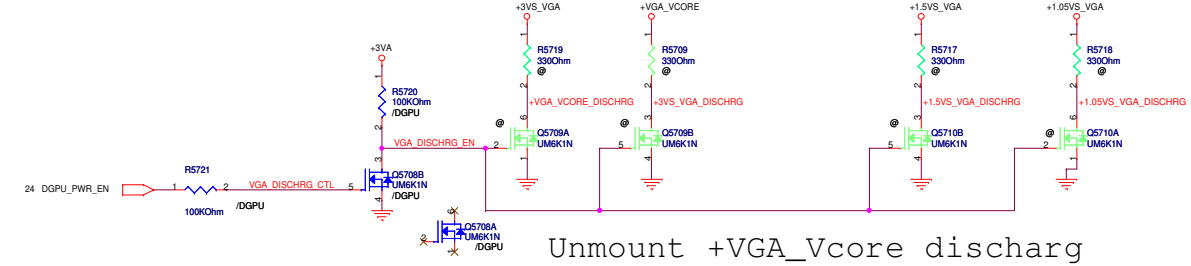
Size	Project Name	Rev
C	MA50	1.3

Date: Monday, February 13, 2012 Sheet 56 of 93

+3VA	+3VA	6,20,26,27,30,31,59,60,81,88,93
+VCORE	+VCORE	6,9,11,80
+VGFX_CORE	+VGFX_CORE	7,9,80
+VCCP	+VCCP	3,4,6,7,30,32,82
+0.75VS	+0.75VS	16,17,83
+1.05VS	+1.05VS	26,27,82,87
+1.5VS	+1.5VS	7,26,53,91
+1.8VS	+1.8VS	7,25,26,80,84
+3VS	+3VS	17,20,21,22,23,24,25,26,27,28,30,32,33,36,37,44,45,48,50,51,53,59,61,80,91,92
+5VS	+5VS	27,36,37,48,50,51,80,87,91
+1.5V	+1.5V	5,16,17,18,60,83
+3V	+3V	24,45,59,61,91
+5V	+5V	59,60,91







Unmount +VGA_Vcore discharg

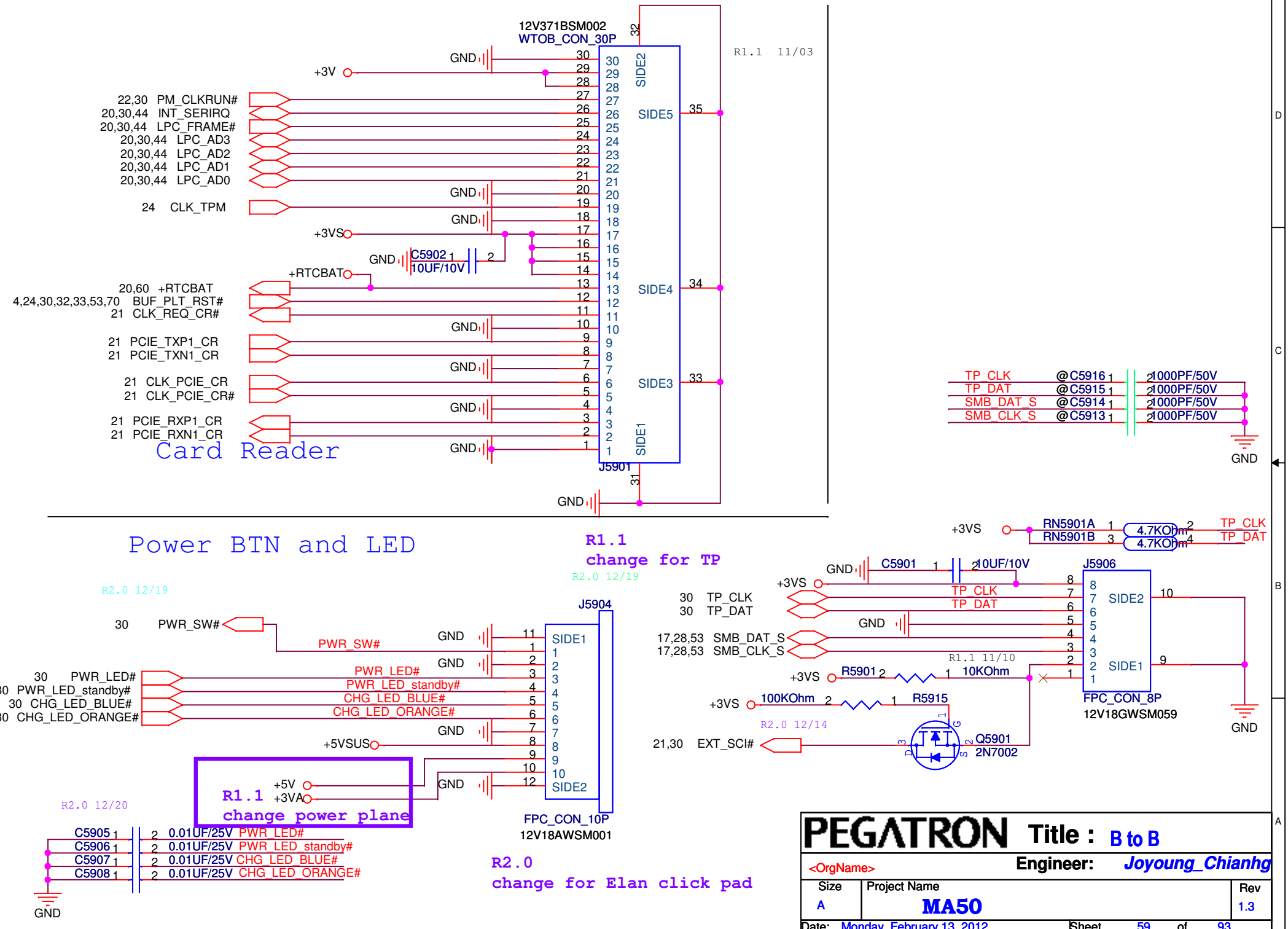
PEGATRON	Title : DSG_Discharge		
<OrgName>	Engineer: Joyoung_Chianhg		
Size: C	Project Name: MA50		Rev: 1.3
Date: Monday, February 13, 2012	Sheet 57 of 93		

PEGATRON Title : System Setting

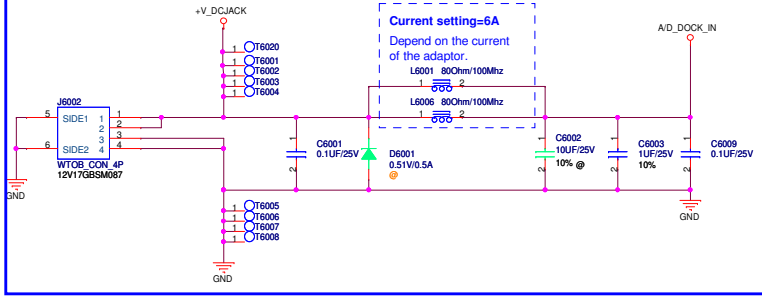
<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
Custom	MA50	1.3

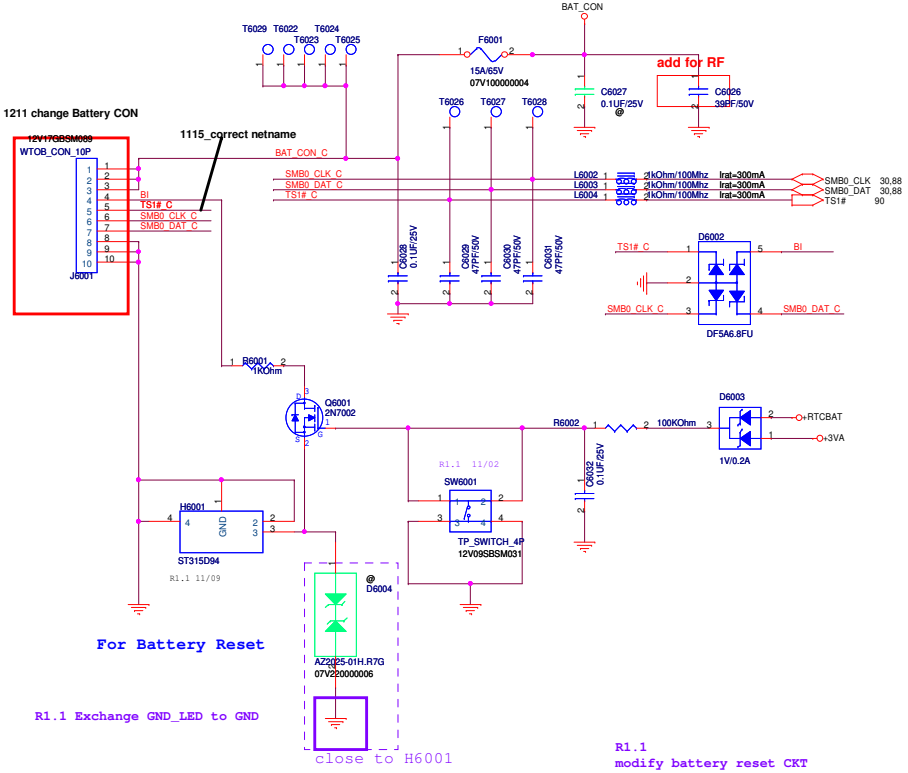
Date: Monday, February 13, 2012 Sheet 58 of 93

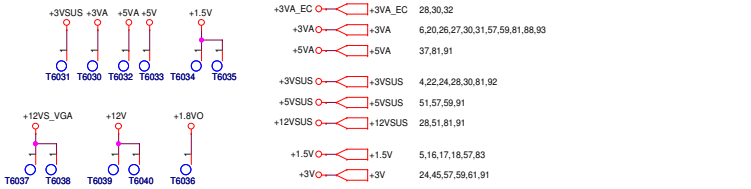

12V371BSM002
WTOB_CON_30P
J5901
SIDE1
SIDE2
SIDE3
SIDE4
SIDE5
R1.1 11/03
22,30 PM_CLKRUN#
20,30,44 INT_SERIRQ
20,30,44 LPC_FRAME#
20,30,44 LPC_AD3
20,30,44 LPC_AD2
20,30,44 LPC_AD1
20,30,44 LPC_AD0
24 CLK_TPM
+3V
+3VS
GND
C5902 10UF/10V
+RTCBAT
20,60 +RTCBAT
4,24,30,32,33,53,70 BUF_PLT_RST#
21 CLK_REQ_CR#
21 PCIE_TXP1_CR
21 PCIE_TXN1_CR
21 CLK_PCIE_CR
21 CLK_PCIE_CR#
21 PCIE_RXP1_CR
21 PCIE_RXN1_CR
Card Reader
TP_CLK @C5916 1000PF/50V
TP_DAT @C5915 1000PF/50V
SMB_DAT_S @C5914 1000PF/50V
SMB_CLK_S @C5913 1000PF/50V
Power BTN and LED
R1.1
change for TP
R2.0 12/19
30 PWR_SW#
30 PWR_LED#
30 PWR_LED_standby#
30 CHG_LED_BLUE#
30 CHG_LED_ORANGE#
PWR_SW#
PWR_LED#
PWR_LED_standby#
CHG_LED_BLUE#
CHG_LED_ORANGE#
+5VSUS
+5V
+3VA
R1.1
change power plane
R2.0 12/20
C5905 0.01UF/25V PWR_LED#
C5906 0.01UF/25V PWR_LED_standby#
C5907 0.01UF/25V CHG_LED_BLUE#
C5908 0.01UF/25V CHG_LED_ORANGE#
J5904
FPC_CON_10P
12V18AWSM001
R2.0
change for Elan click pad
+3VS
RN5901A 4.7KOhm
RN5901B 4.7KOhm
TP_CLK
TP_DAT
C5901 10UF/10V
30 TP_CLK
30 TP_DAT
17,28,53 SMB_DAT_S
17,28,53 SMB_CLK_S
R1.1 11/10
R5901 10KOhm
R5915 100KOhm
R2.0 12/14
21,30 EXT_SCI#
Q5901 2N7002
J5906
FPC_CON_8P
12V18GWSM059
PEGATRON
Title : B to B
<OrgName>
Engineer: Joyoung_Chianhg
Size A
Project Name MA50
Rev 1.3
Date: Monday, February 13, 2012
Sheet 59 of 93

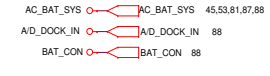
DC Jack WtoB CONN

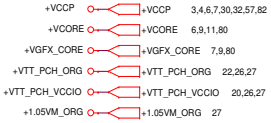


Battery Connector









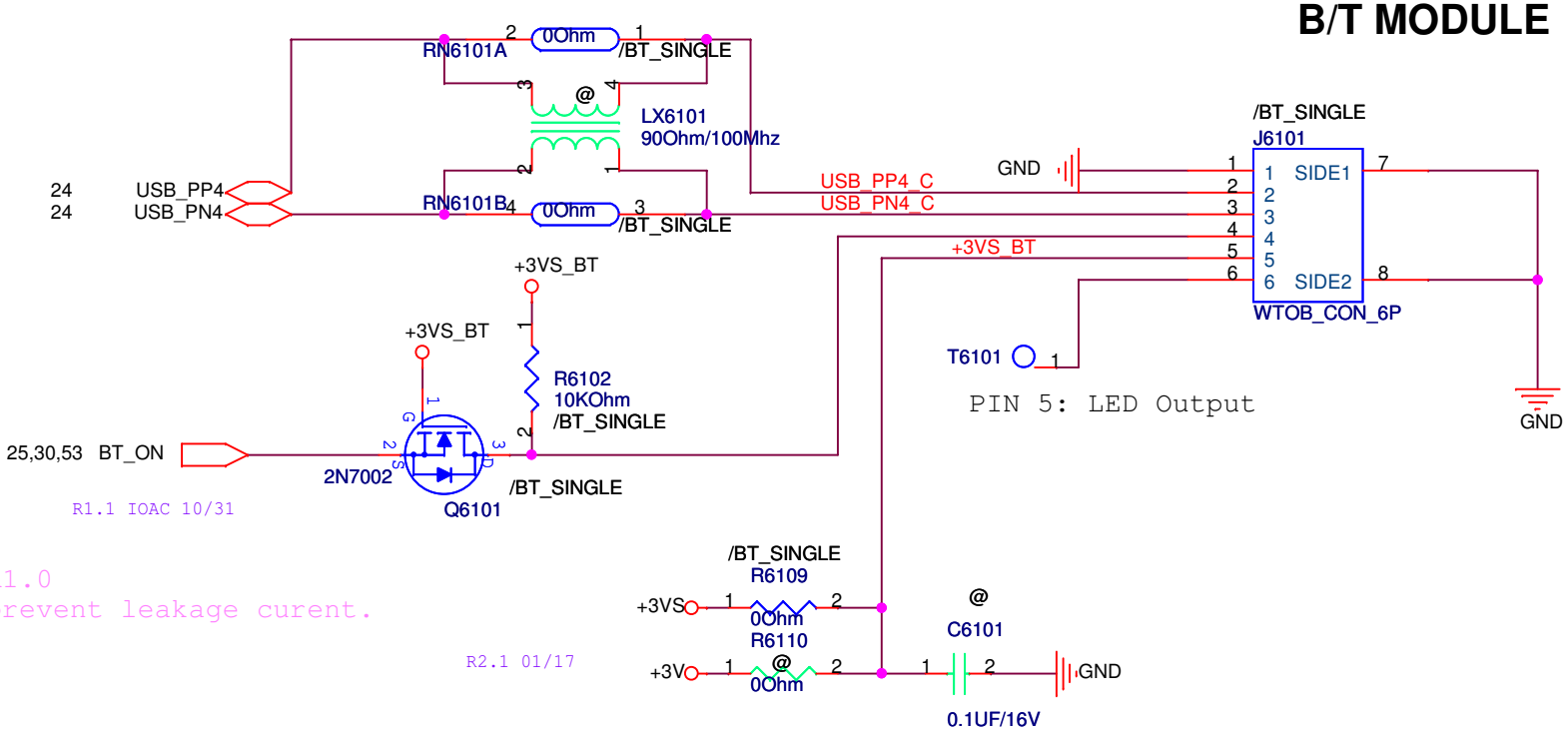
PEGATRON Title : DC_DC/BAT CONN

<OrgName> Engineer: Joyoung_Colanhg

Size	Project Name	Rev
C	MA50	1.3

Date: Monday, February 13, 2012 Sheet 60 of 93

B/T MODULE



PEGATRON	Title : Fersco USB 3.0		
Pegatron Corp.	Engineer: Joyoung_Chianhg		
Size: A	Project Name: MA50		Rev: 1.00
Date: Monday, February 13, 2012	Sheet 61 of 93		

PEGATRON

Title : System Setting

<OrgName>

Engineer: Joyoung_Chianhg

Size	Project Name	Rev
Custom	MA50	1.3

Date: Monday, February 13, 2012 Sheet 62 of 93

PEGATRON	Title : B to B			
<OrgName>	Engineer: Joyoung_Chianhg			
Size: A	Project Name: MA50			Rev: 1.3
Date: Monday, February 13, 2012		Sheet 63 of 93		

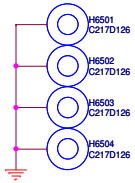
PEGATRON Title : B to B

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	MA50	1.3

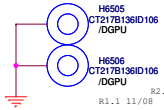
Date: Monday, February 13, 2012 Sheet 64 of 93

CPU Bracket Hole



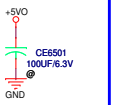
ME B Type

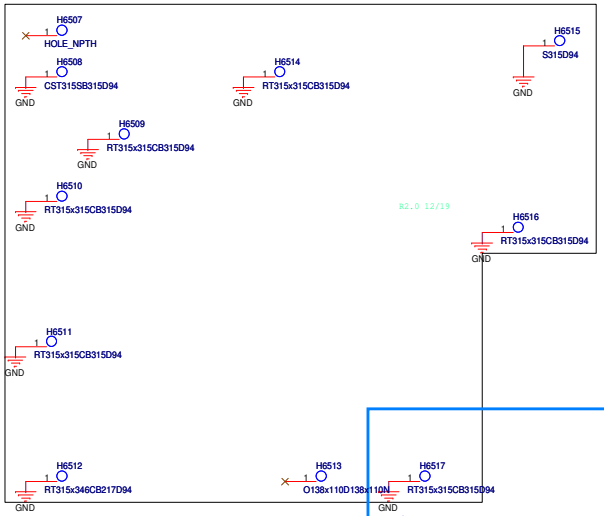
VGA Bracket Hole



R2.0 12/15
R1.1 11/08

place between J5204 /J5205





This screw hole should be Upside down(TOP and BOTTOM).

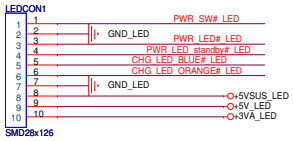
PEGATRON Title : ME_CONN,Skew Hole

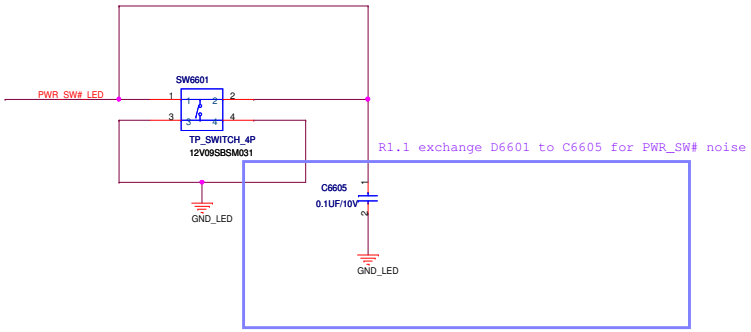
<OrgName> Engineer: Joyoung_Chianhg

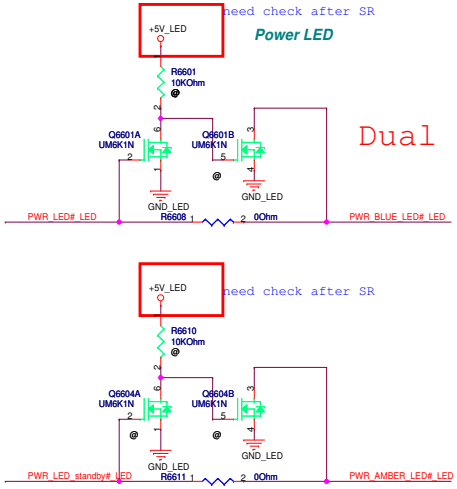
Size	Project Name	Rev
C	MA50	1.3

Date: Monday, February 13, 2012 Sheet 65 of 93

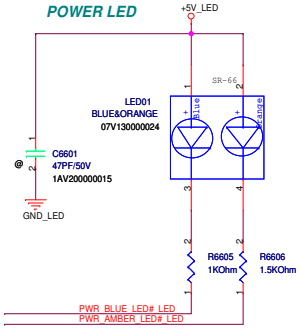
Power Button

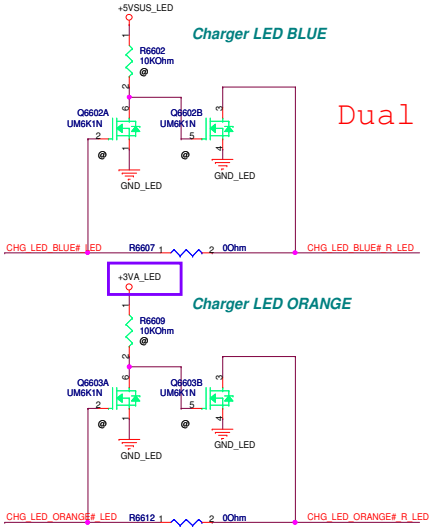




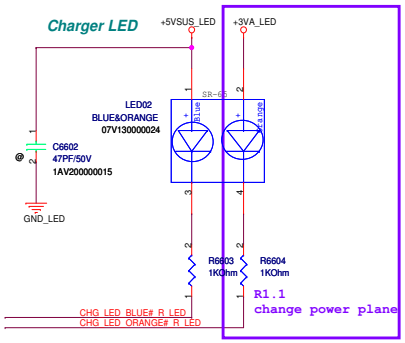


Dual Color





Dual Color



PEGATRON	Title : TP_M	
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Joyoung_Chianhg	
Size: C	Project Name: MA50	Rev: 1.0
Date: Monday, February 13, 2012	Sheet 66 of 93	

From System's PCIE interface

R2.0 move back

+3VS_MB — R6706 0Ohm 10V340000001 — +3VS_CR

trace width 60mils — trace width 60mils

C6701 1UF/10V — GND_CR

C6704 0.1UF/10V @ — GND_CR

SD_CLK — R6703 0Ohm — SD_CLK_R

C6720 10PF/50V @ — 1AV200000001 — GND_CR

20110909 Joyoung EMI request

SDCLK trace length shorter,surround with GND.

H6701 C315D110 GND_CR H6703 HOLE_NPTH

H6704 O110X138DC110X138N

H6702 C315D110 GND_CR

R1.1 change to 30P

J6701 WTOB_CON_30P 12V37BSM002

SIDE1 SIDE2 SIDE3 SIDE4 SIDE5

GND_CR +3V_TPM PM_CLKRUN#_TPM LPCSERIRQ_TPM LPC_FRAME#_TPM

R2.0 12/13

/TPM 0Ohm RN6702A LPC_AD3_TPM

/TPM 0Ohm RN6702B LPC_AD2_TPM

/TPM 0Ohm RN6702C LPC_AD1_TPM

/TPM 0Ohm RN6702D LPC_AD0_TPM

GND_CR LPCCLK_TPM 10PF/50V C6711 GND_CR

+3VS_TPM +3VS_MB +3V_CARD_CR

BUF_PLT_RST#_CR CLKREQ0_CR# PCIE_TXP0_CR PCIE_TXN0_CR CLK_PCIE_CR_P CLK_PCIE_CR_N PCIE_RXP0_CR PCIE_RXN0_CR

GND_CR

RTC

+RTCBAT_CR

J6702 BATT_HOLDER_2P

12V20GBSM000

GND_CR

CR_LED# — T6706

1AV200000042 C6724 0.1UF/16V — GND_CR

GND_CR — R6725 6.2KOhm 10V220000088 — T6702 T6703 T6704

+3VS_CR CLKREQ0_CR# BUF_PLT_RST#_CR SD_CD# SD_WP

U6701

PCIE_TXP0_CR PCIE_TXN0_CR CLK_PCIE_CR_P CLK_PCIE_CR_N AV12 HSOP_R HSON_R DV12 +3VS_CR

HSIP HSIN REFCLKP REFCLKN AV12 HSOP HSON GND1 DV12 Card1_3V3 3V3_IN1 Card2_3V3

RREF XVR_IN2 CLK_REQ# PERST# EEDO EECS EESK GPIO/EEDI MS_INS# SD_CD# SP15 SP14

SP13 SP12 SP11 SP10 SP9 SP8 SP7 SP6 SP5 DV12_S GND3 SD_D2

RTS5209-GR

1AV200000042 C6722 0.1UF/16V — GND_CR

PCIE_RXP0_CR PCIE_RXN0_CR

C6719 0.1UF/16V — 1AV200000042 — GND_CR

C6723 4.7UF/6.3V — 1AV300000023 — GND_CR

C6717 0.1UF/16V — 1AV200000042 — GND_CR

C6736 10UF/10V — C6735 0.1UF/16V — 1AV200000042 — GND_CR GND_CR

+3V_CARD — trace width 40mils

C6726 4.7UF/6.3V — 1AV300000023

C6725 0.1UF/16V — 1AV200000042 — GND_CR

DV12_S — SD_D2

Part number:020J-007D000

AV12 — R6731 @ 0Ohm — DV12

vx_r0603_h28_small

xD_CD# DV33_18 GND2 SP1 SP2 SP3 SP4 SD_D1 SD_D0 SD_CLK SD_CMD SD_D3

DV33_18 — C6730 @ 4.7UF/6.3V — 1AV300000023 — C6728 0.1UF/16V — 1AV200000042 — GND_CR

J6703 SD_SOCKET_9P 12V211BSD000

SD_D2 SD_D3 SD_CMD SD_CLK_R SD_D1 SD_D0

+3V_CARD — P_GND2 P_GND1 — SD_WP SD_CD#

GND_CR GND_CR

+3V_CARD — C6702 10UF/10V — 1AV500000008 — C6703 0.1UF/16V — 1AV200000042 — GND_CR

C4008 C4002 SD CARD CAP

Close to connector

+3V_TPM +3VS_TPM +3VS_TPM — R6707 4.7KOhm @

/TPM J6705 BTOB_CON_16P 12V162BSM003

LPCSERIRQ_TPM LPC_AD0_TPM LPC_AD1_TPM LPC_FRAME#_TPM LPCCLK_TPM LPC_AD2_TPM LPC_AD3_TPM

BUF_PLT_RST#_CR PM_CLKRUN#_TPM

C6715 @ 1UF/6.3V — C6712 @ 0.1UF/16V — C6714 @ 1UF/6.3V — C6713 @ 0.1UF/16V — GND_CR — GND_CR

Pin Name	Description
SP1	SD_D7/XD_RDY
SP2	SD_D6/XD_RE#
SP3	SD_D5/XD_CE#
SP4	SD_D4/XD_WE#
SP5	MS_BS/XD_CLE
SP6	MS_D5/XD_ALE
SP7	MS_D1/XD_WP#
SP8	MS_D4/XD_D0
SP9	MS_D0/XD_D1
SP10	MS_D2/XD_D2
SP11	MS_D6/XD_D3
SP12	MS_D3/XD_D4
SP13	MS_D7/XD_D5
SP14	MS_CLK/XD_D6
SP15	SD_WP/XD_D7

Remove Serial Flash

Reserve for BIOS boot function

When EECS switch to be D3-Delink sideband signal, Serial Flash function is disabled.

PEGATRON Title : RTS5209

Engineer: JAY TSAI

Size	Project Name	Rev
C	MA50	1.0

Date: Monday, February 13, 2012 Sheet 67 of 93

PEGATRON

Title : USB_USB Port

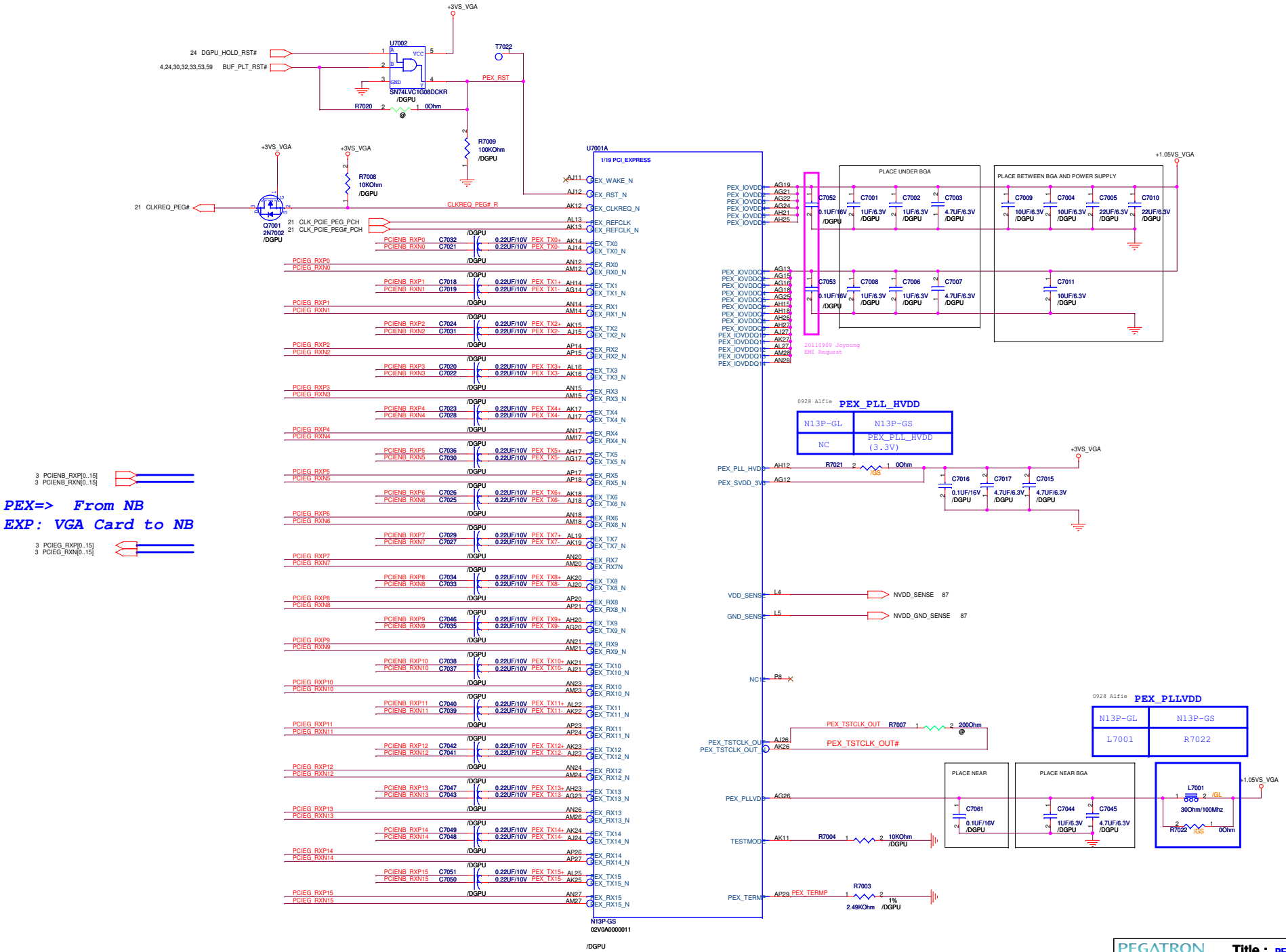
<OrgName>

Engineer: Joyoung_Chianhg

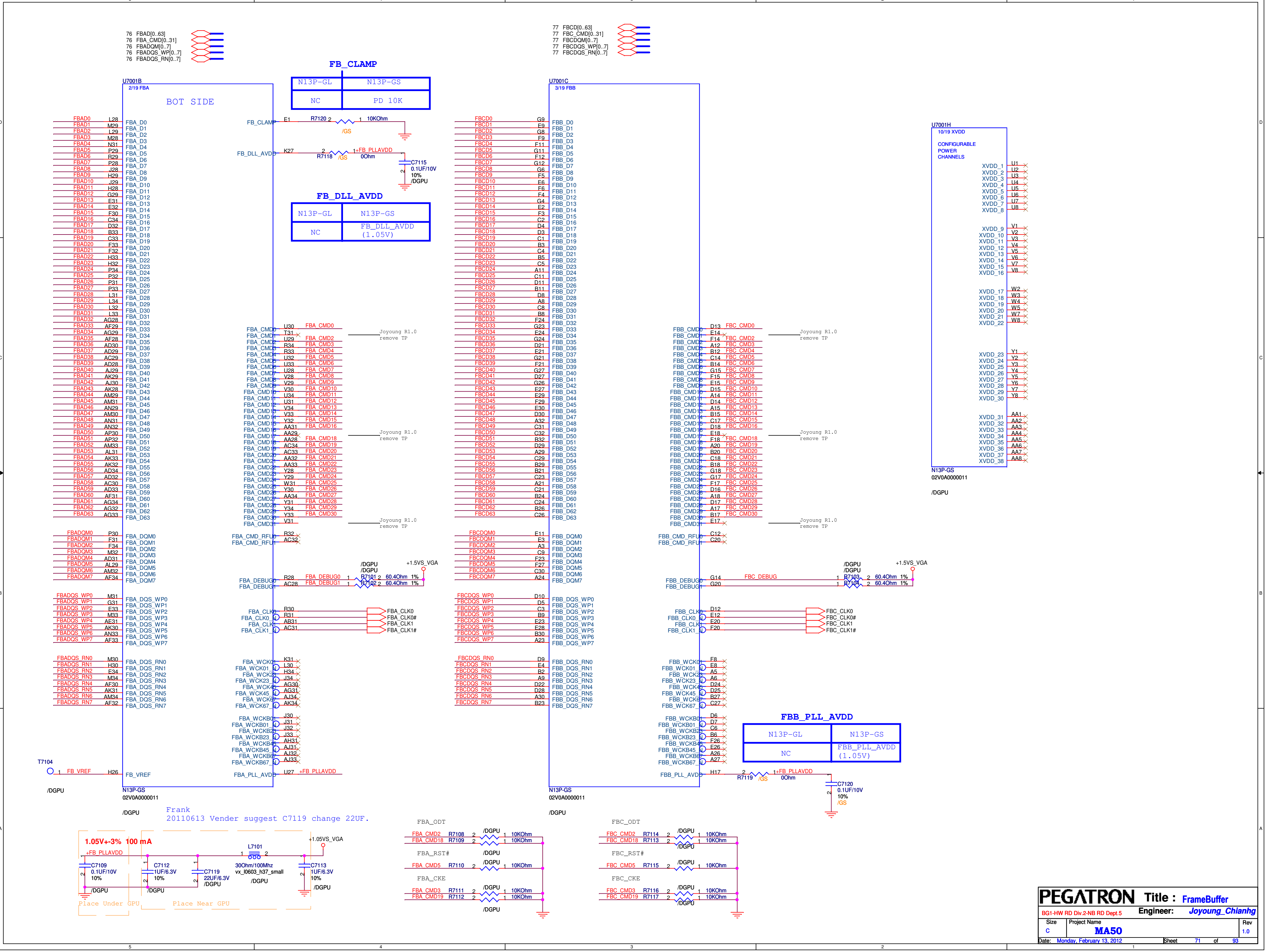
Size	Project Name	Rev
B	MA50	1.3

Date: Monday, February 13, 2012 Sheet 69 of 93

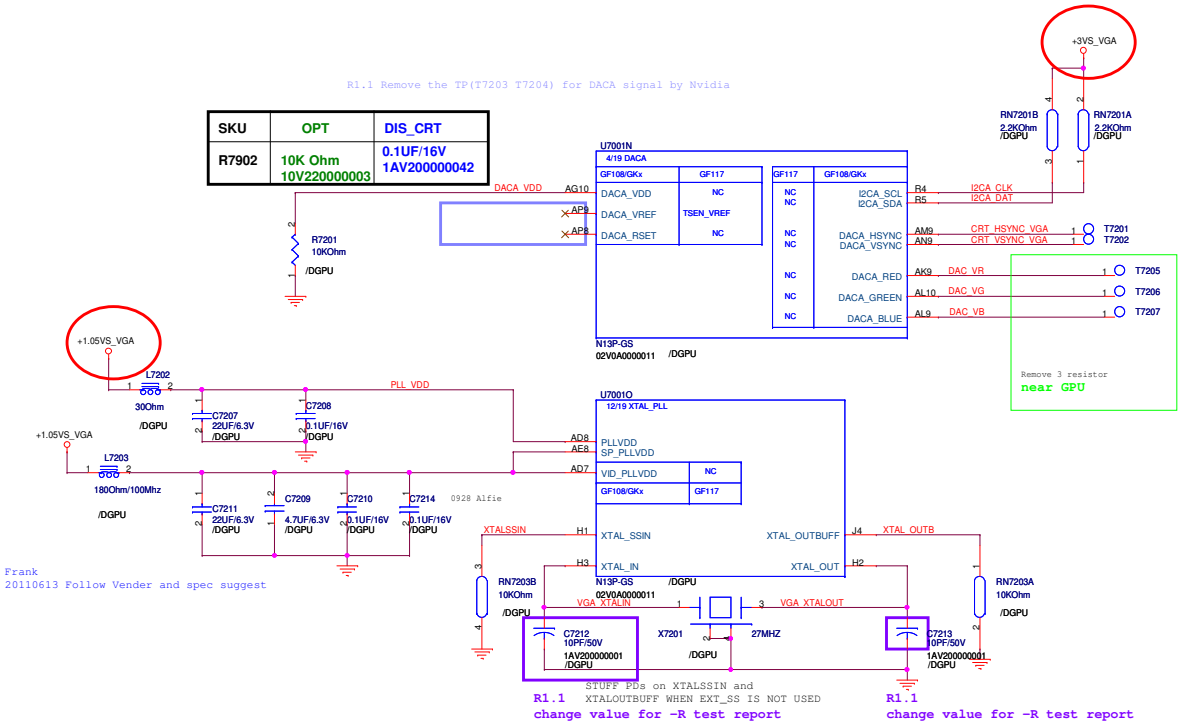
Frank
20110513 Change N13P GPU.



PEGATRON	Title : PEG		
PEGATRON COMPUTER INC	Engineer: Joyoung_Chianhg		
Size C	Project Name MA50		Rev 1.3
	P/N <OrgAddr2>		
Date: Monday, February 13, 2012	Sheet 70 of 93		



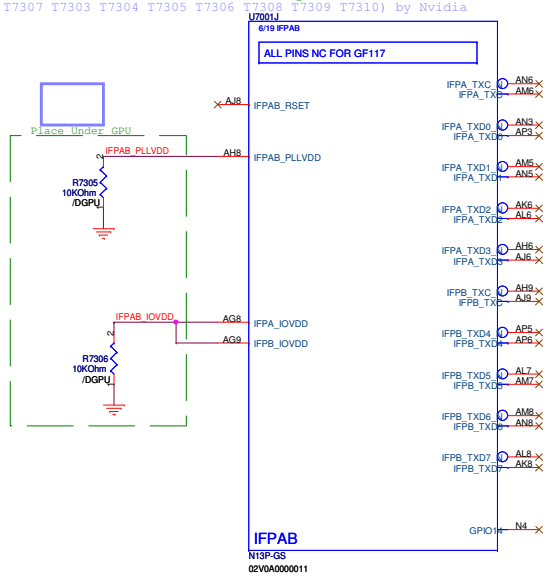
76 FBAD[0..63]
76 FBA_CMD[0..31]
76 FBADQM[0..7]
76 FBADQS_WP[0..7]
76 FBADQS_RN[0..7]
77 FBCD[0..63]
77 FBC_CMD[0..31]
77 FBCDQM[0..7]
77 FBCDQS_WP[0..7]
77 FBCDQS_RN[0..7]
FB_CLAMP
N13P-GL
N13P-GS
NC
PD 10K
FB_DLL_AVDD
N13P-GL
N13P-GS
NC
FB_DLL_AVDD (1.05V)
U7001B
2/19 FBA
BOT SIDE
U7001C
3/19 FBB
U7001H
10/19 XVDD
CONFIGURABLE POWER CHANNELS
N13P-GS
02V0A0000011
/DGPU
Joyoung R1.0 remove TP
+1.5VS_VGA
FBB_PLL_AVDD
N13P-GL
N13P-GS
NC
FBB_PLL_AVDD (1.05V)
T7104
Frank
20110613 Vender suggest C7119 change 22UF.
1.05V+-3% 100 mA
+FB_PLLAVDD
+1.05VS_VGA
L7101
30Ohm/100Mhz
C7109 0.1UF/10V
C7112 1UF/6.3V
C7119 22UF/6.3V
C7113 1UF/6.3V
Place Under GPU
Place Near GPU
FBA_ODT
FBA_RST#
FBA_CKE
FBC_ODT
FBC_RST#
FBC_CKE
PEGATRON
Title : FrameBuffer
BG1-HW RD Div.2-NB RD Dept.5
Engineer: Joyoung_Chiang
Size C
Project Name MA50
Rev 1.0
Date: Monday, February 13, 2012
Sheet 71 of 93



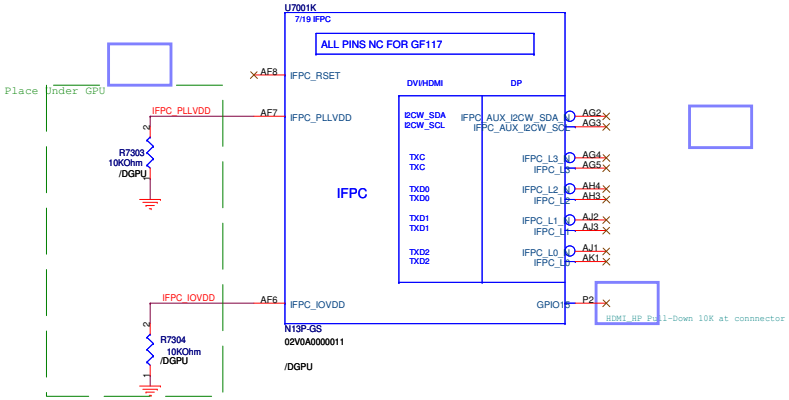
PEGATRON	Title :	FRAME BUFFER C
PEGATRON COMPUTER INC	Engineer:	Joyoung_Chianhg
Size: C	Project Name: MA50	Rev: 1.0
	P/N: <OrgAddr2>	
Date: Monday, February 13, 2012	Sheet 72 of 93	

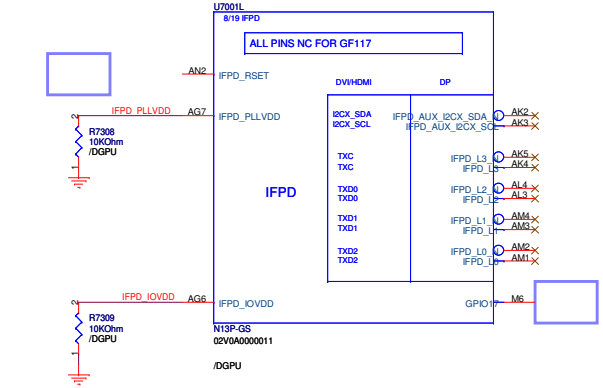
R1.1 Remove the TP (T7301 T7311 T7302 T7307 T7303 T7304 T7305 T7306 T7308 T7309 T7310) by Nvidia

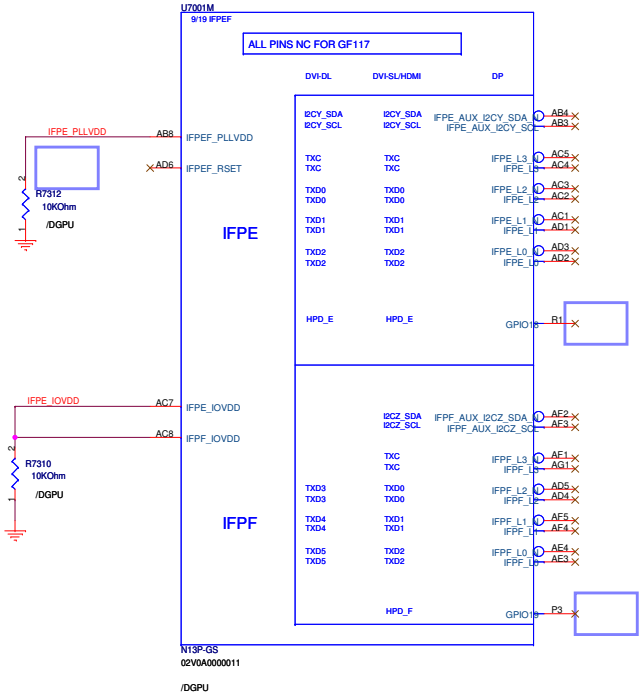
LVDS



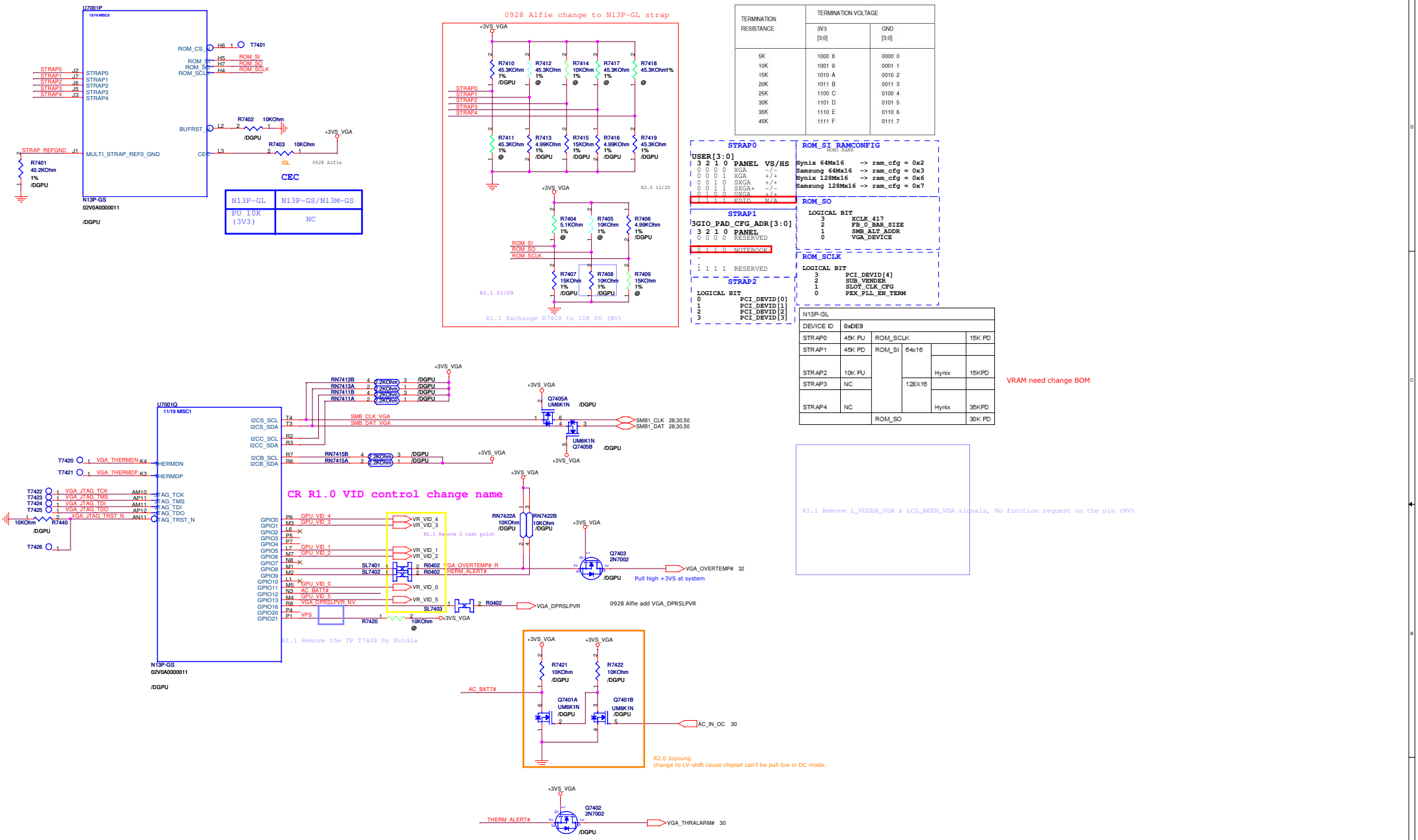
HDMI



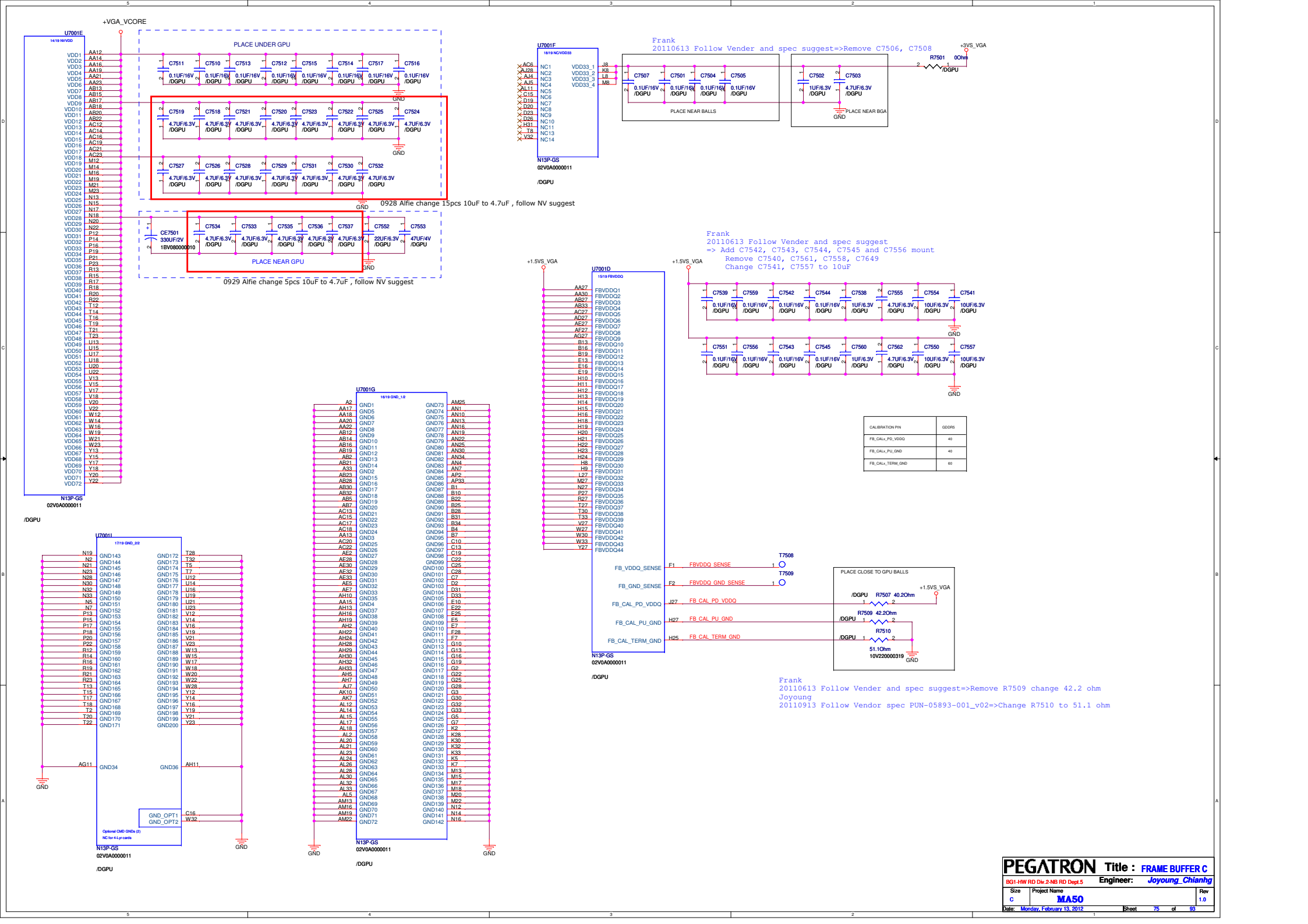




PEGATRON	Title : FRAME BUFFER C		
PEGATRON COMPUTER INC	Engineer: Joyoung_Chianhg		
Size: C	Project Name: MA50		Rev: 1.0
	P/N: <OrgAddr2>		
Date: Monday, February 13, 2012	Sheet 73 of 93		

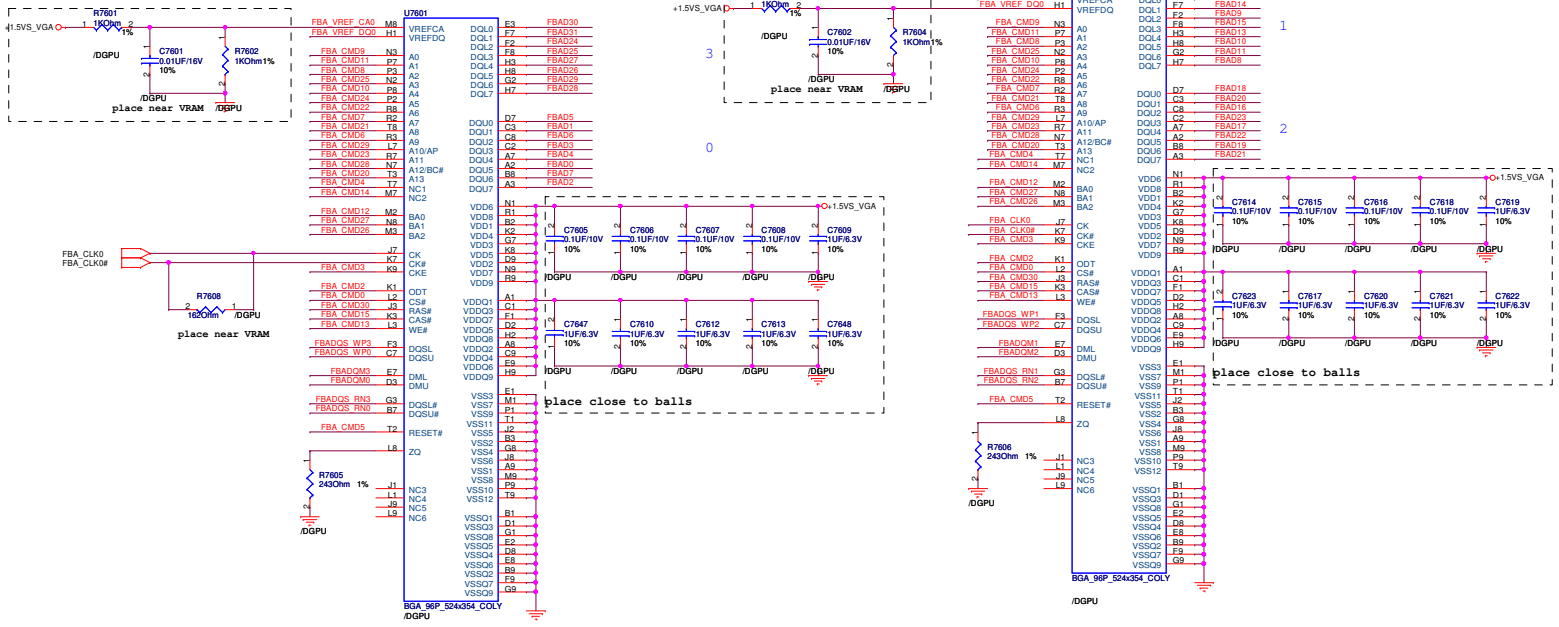


PEGATRON	Title : FRAME BUFFER A
PEGATRON COMPUTER INC	Engineer: Joyoung_Chianhg
Size: A2	Project Name: MA50 / P/N: <OrgAddr2>
Rev: 1.0	
Date: Monday, February 13, 2012	Sheet 74 of 93


+VGA_VCORE
U7001E
14/19 NVVDD
PLACE UNDER GPU
C7511 C7510 C7513 C7512 C7515 C7514 C7517 C7516
0.1UF/16V /DGPU
C7519 C7518 C7521 C7520 C7523 C7522 C7525 C7524
4.7UF/6.3V /DGPU
C7527 C7526 C7528 C7529 C7531 C7530 C7532
GND
0928 Alfie change 15pcs 10uF to 4.7uF , follow NV suggest
CE7501
330UF/2V
1BV080000010
C7534 C7533 C7535 C7536 C7537 C7552 C7553
22UF/6.3V /DGPU
47UF/4V /DGPU
PLACE NEAR GPU
0929 Alfie change 5pcs 10uF to 4.7uF , follow NV suggest
N13P-GS
02V0A0000011
/DGPU
U7001F
18/19 NC/VDD33
Frank
20110613 Follow Vender and spec suggest=>Remove C7506, C7508
+3VS_VGA
R7501 0Ohm
C7507 C7501 C7504 C7505
C7502 C7503
PLACE NEAR BALLS
PLACE NEAR BGA
U7001D
15/19 FBVDDQ
+1.5VS_VGA
Frank
20110613 Follow Vender and spec suggest
=> Add C7542, C7543, C7544, C7545 and C7556 mount
Remove C7540, C7561, C7558, C7649
Change C7541, C7557 to 10uF
C7539 C7559 C7542 C7544 C7538 C7555 C7554 C7541
C7551 C7556 C7543 C7545 C7560 C7562 C7550 C7557
1UF/6.3V /DGPU
4.7UF/6.3V /DGPU
10UF/6.3V /DGPU
CALIBRATION PIN
GDDR5
FB_CALx_PD_VDDQ 40
FB_CALx_PU_GND 40
FB_CALx_TERM_GND 60
FB_VDDQ_SENSE
FB_GND_SENSE
FB_CAL_PD_VDDQ
FB_CAL_PU_GND
FB_CAL_TERM_GND
FBVDDQ_SENSE
FBVDDQ_GND_SENSE
FB_CAL_PD_VDDQ
FB_CAL_PU_GND
FB_CAL_TERM_GND
T7508
T7509
PLACE CLOSE TO GPU BALLS
R7507 40.2Ohm
R7509 42.2Ohm
R7510
51.1Ohm
10V220000319
Frank
20110613 Follow Vender and spec suggest=>Remove R7509 change 42.2 ohm
Joyoung
20110913 Follow Vendor spec PUN-05893-001_v02=>Change R7510 to 51.1 ohm
U7001G
18/19 GND_1/2
U7001I
17/19 GND_2/2
GND_OPT1
GND_OPT2
Optional CMO GNDs (2)
NC for 4-Lyr cards
PEGATRON
Title : FRAME BUFFER C
BG1-HW RD Div.2-NB RD Dept.5
Engineer: Joyoung_Chianhg
Size C
Project Name MA50
Rev 1.0
Date: Monday, February 13, 2012
Sheet 75 of 93

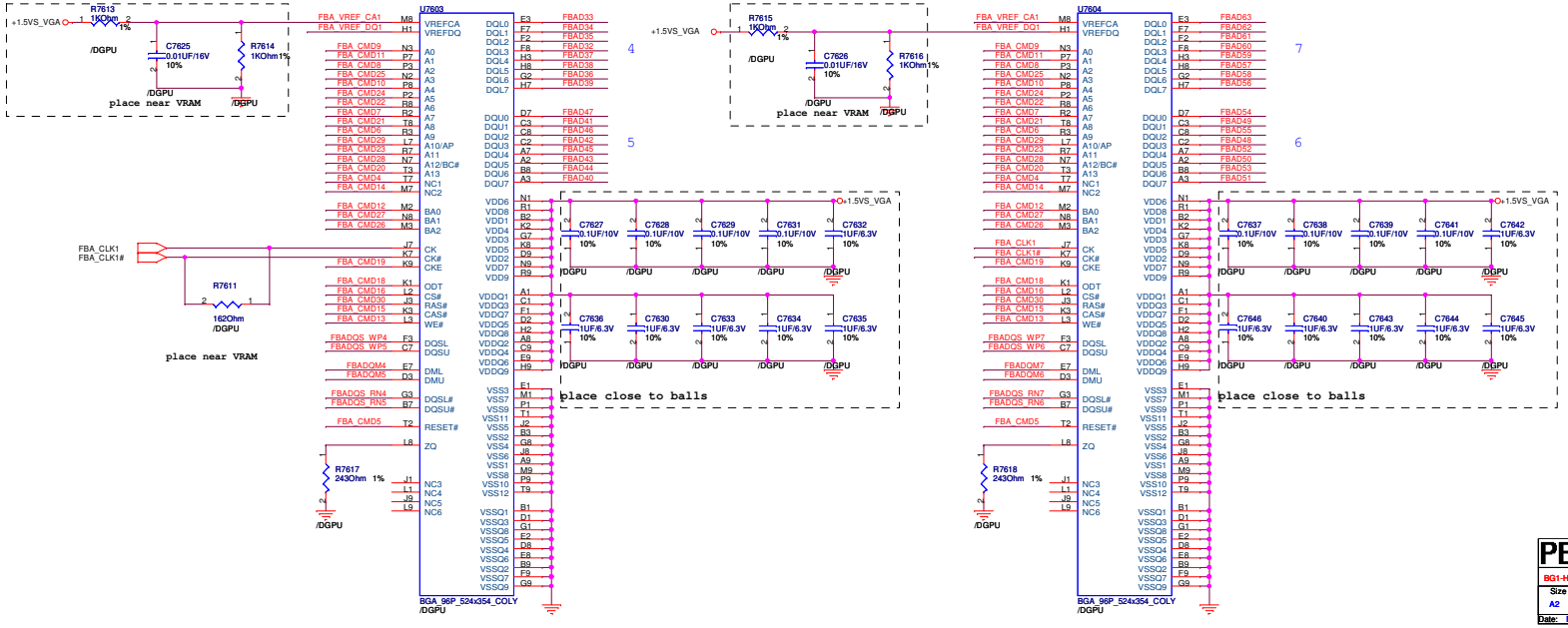
VRAM CH A

TOP SIDE



BOT SIDE

TOP SIDE

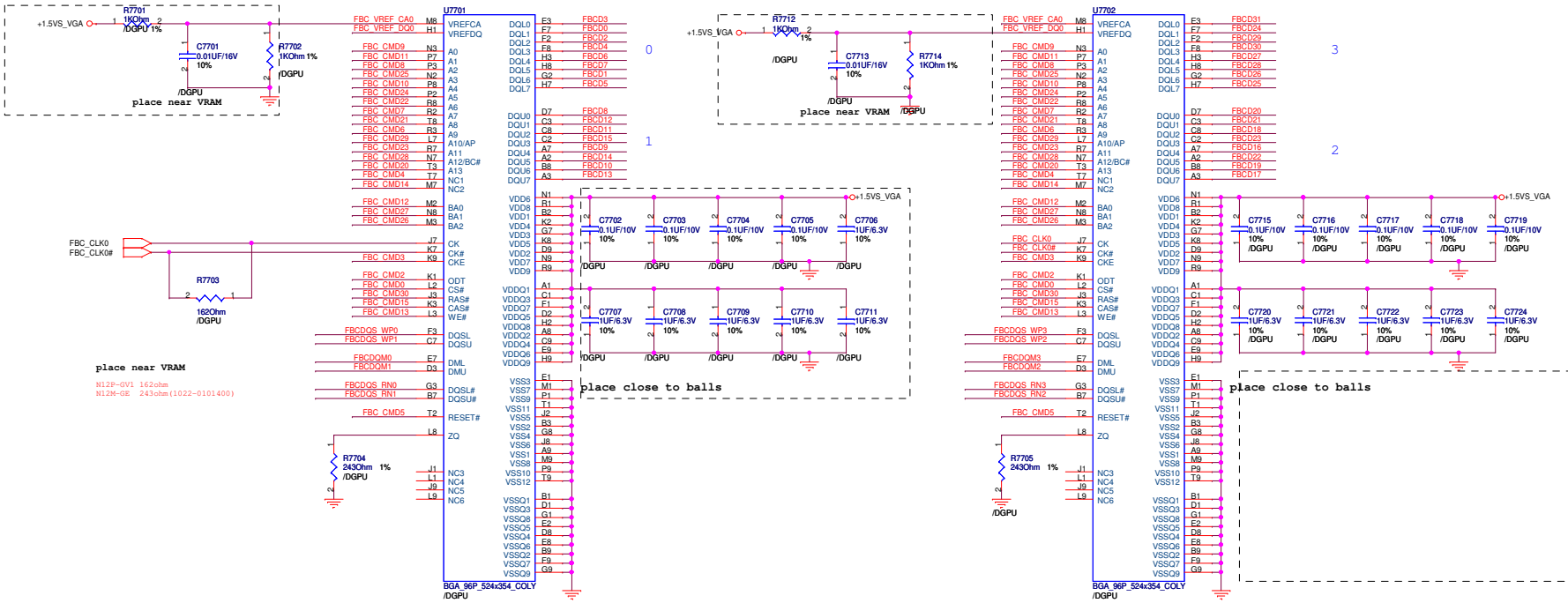


BOT SIDE

PEGATRON	Title : FRAME BUFFER A	
BG1-HW RD Div.2-NB RD Dep15	Engineer: Joyoung_Chianhg	
Size: A2	Project Name: MA50	Rev: 1.0
Date: Monday, February 13, 2012	Sheet 76 of 93	

VRAM CH C

TOP SIDE

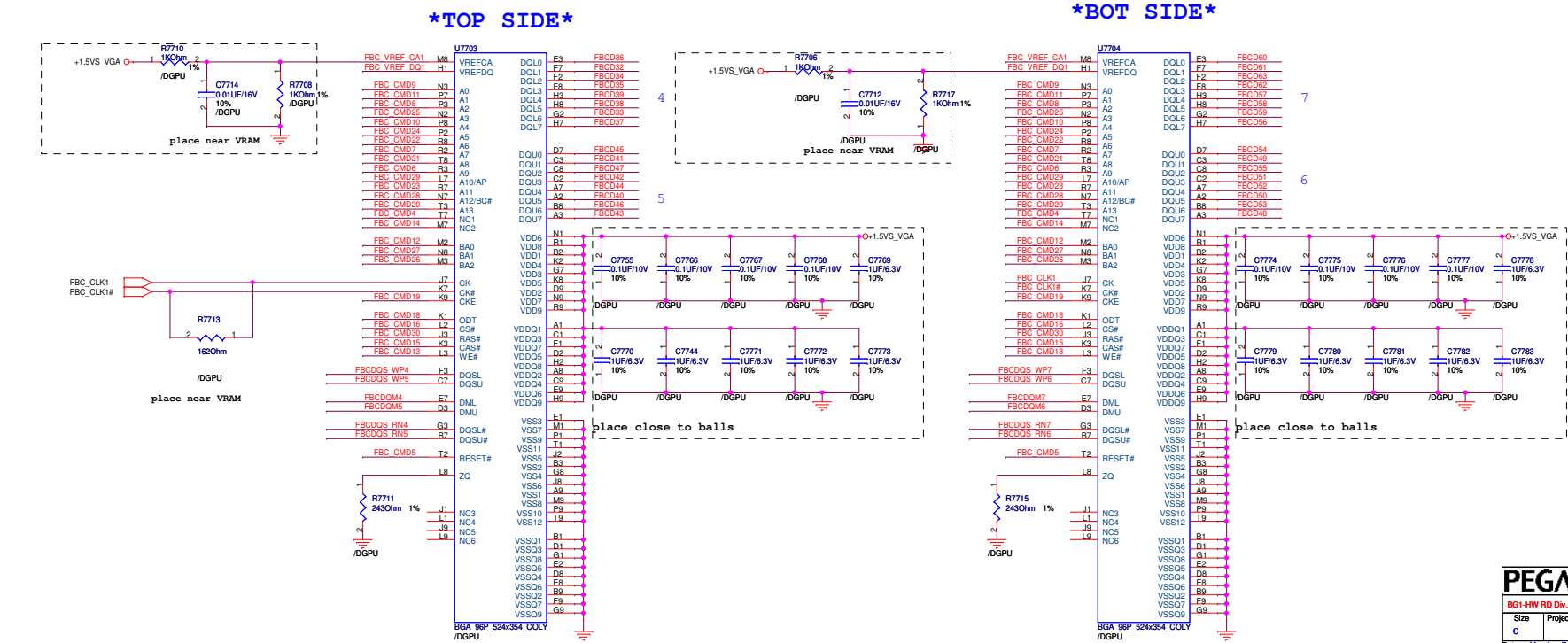


N12P-GV1 162ohm
N12M-GE 243ohm(1022-0101400)

71 FBCD[0..63]
71 FBC_CMD[0..31]
71 FBCDQM[0..7]
71 FBCDQS_WP[0..7]
71 FBCDQS_RN[0..7]

BOT SIDE

TOP SIDE



BOT SIDE

PEGATRON	Title : FRAME BUFFER B		
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Joyoung_Chianhg		
Size: C	Project Name: MA50	Rev: 1.0	
Date: Monday, February 13, 2012	Sheet 77 of 93		

PEGATRON

Title : Connector, LED

PEGATRON COMPUTER INC

Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	MA50	1.0
	P/N <OrgAddr2>	

Date: Monday, February 13, 2012 Sheet 78 of 93

PEGATRON

Title : GPU PWR/GND

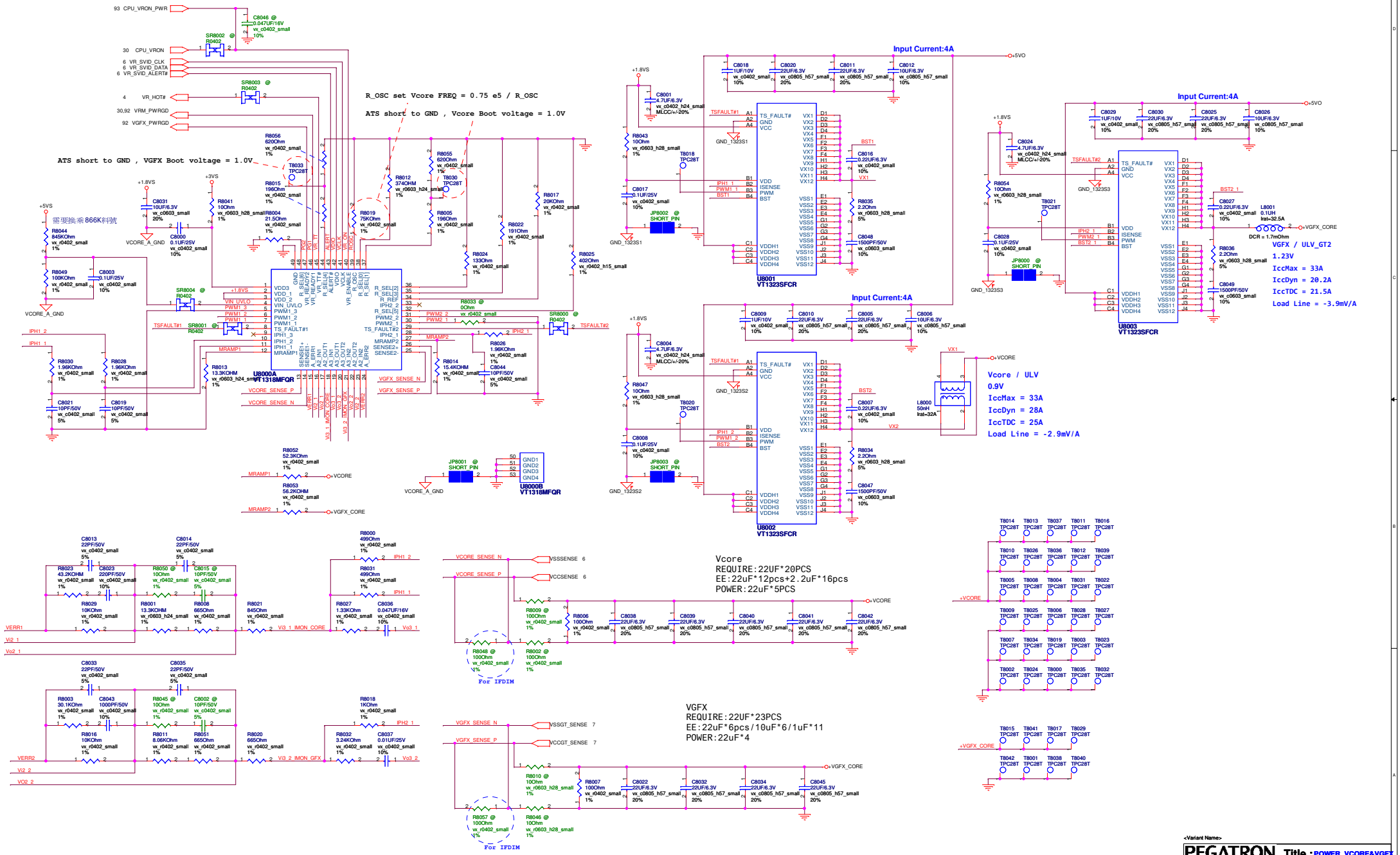
PEGATRON COMPUTER INC

Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	MA50	1.0
	P/N <OrgAddr2>	

Date: Monday, February 13, 2012 Sheet 79 of 93

+VCORE & +VGFX POWER SUPPLY Huron River



<variant_name>

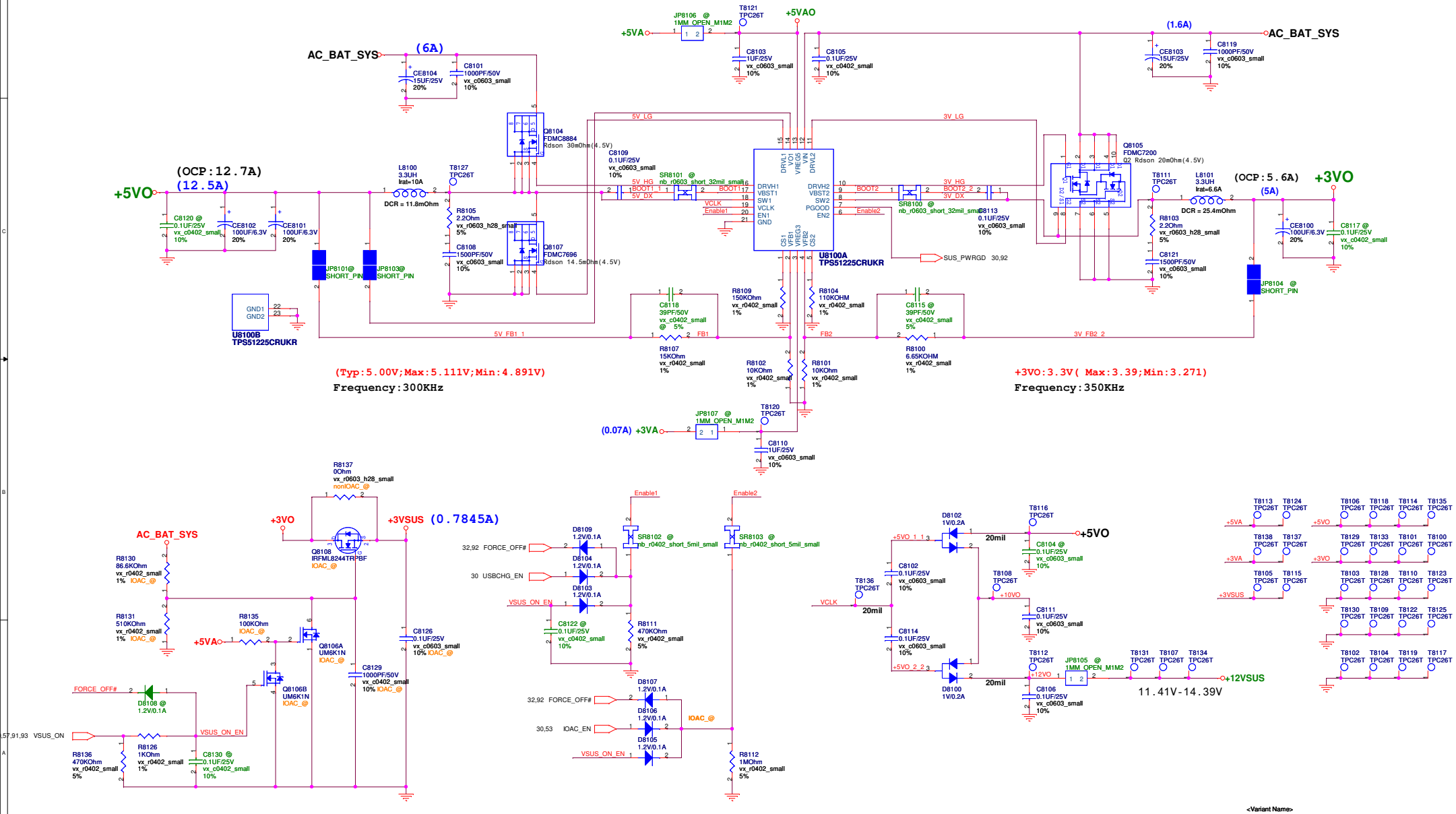
PEGATRON Title : POWER_VCORE&VGFX

Engineer: Clark Liang

Size	Project Name	Rev
Custom	MA50	1.0

Date: Monday, February 13, 2012 Sheet 80 of 94

+5VO & +3VO POWER SUPPLY



<Variant Name>

PEGATRON Title : POWER_SYSTEM

Engineer: Clark Liang

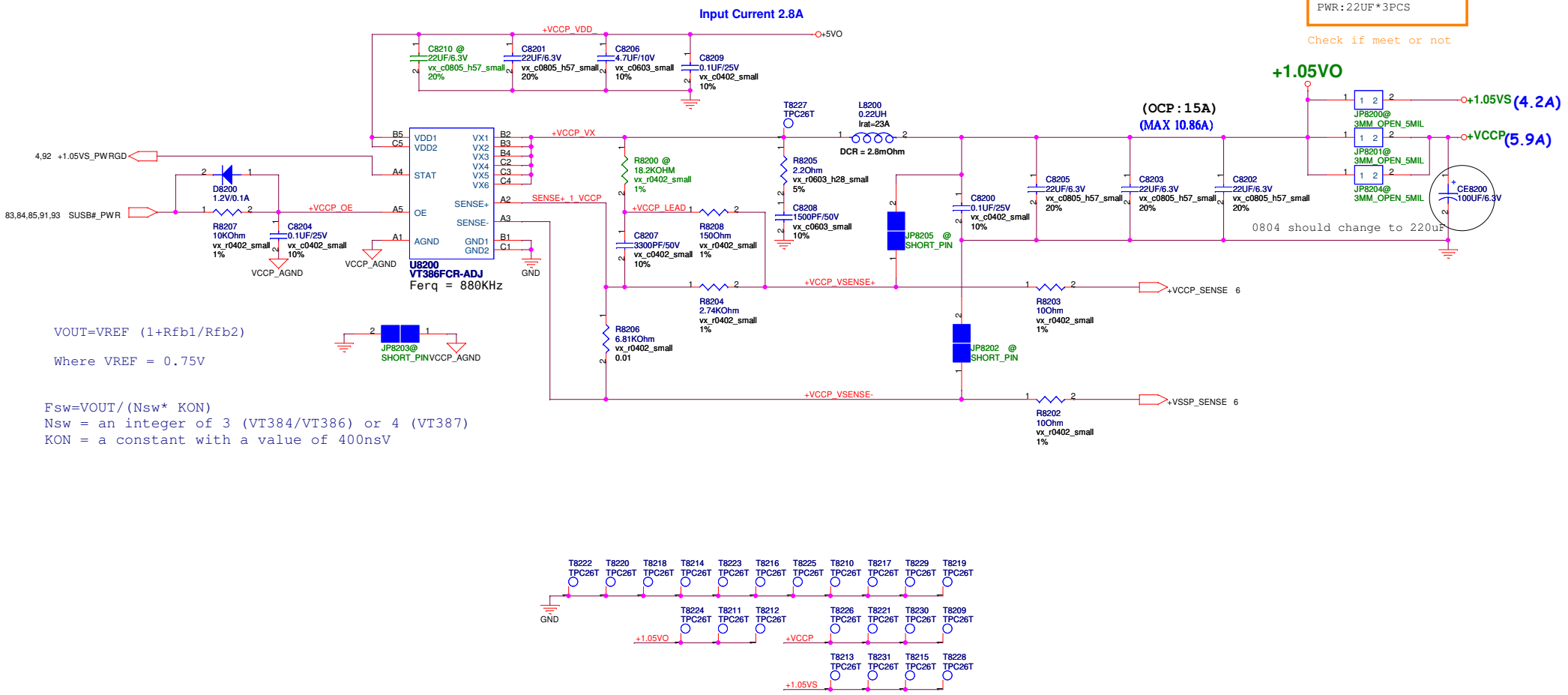
Size	Project Name	Rev
Custom	MA50	1.0

Date: Monday, February 13, 2012 Sheet 81 of 94

+1.05VO POWER SUPPLY

11/07/21
+1.05VS & +VCCP
REQUIRE:22UF*18PCS
EE:10UF*10PCS/1uF*26
PWR:22UF*3PCS

Check if meet or not



<Variant Name>

PEGATRON Title : POWER_+VCCP

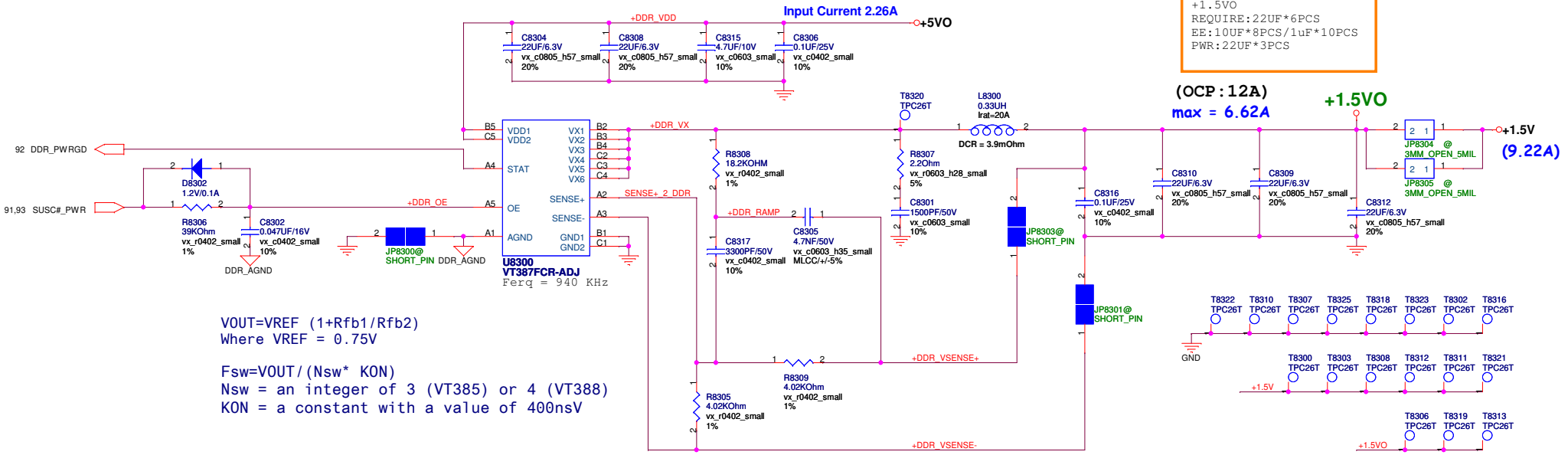
Engineer: Clark Liang

Size	Project Name	Rev
Custom	MA50	1.0

Date: Monday, February 13, 2012 Sheet 82 of 94

+1.5VO POWER SUPPLY

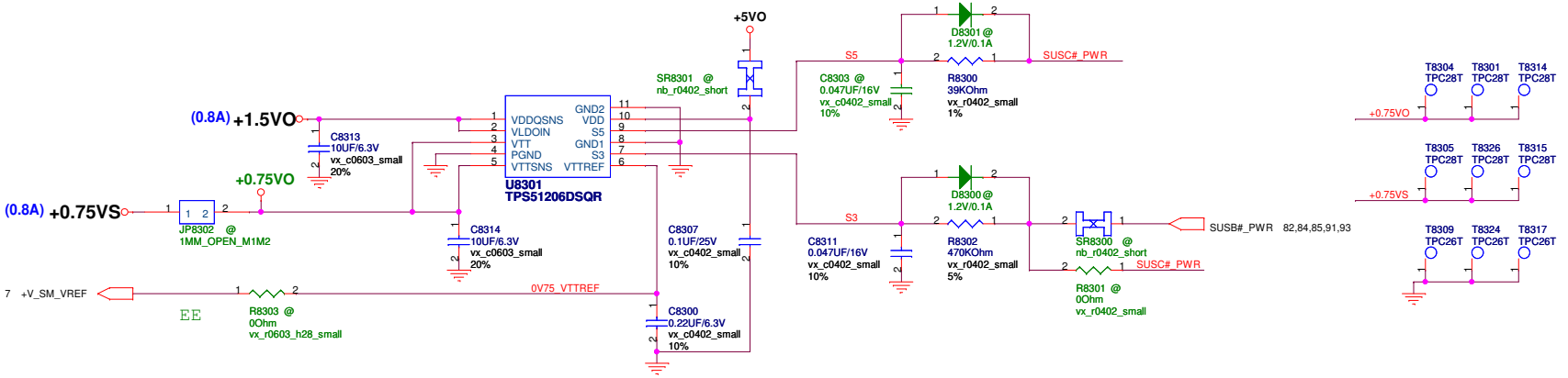
11/07/21
+1.5VO
REQUIRE:22UF*6PCS
EE:10UF*8PCS/1uF*10PCS
PWR:22UF*3PCS



VOUT=VREF (1+Rfb1/Rfb2)
Where VREF = 0.75V

Fsw=VOUT/(Nsw* KON)
Nsw = an integer of 3 (VT385) or 4 (VT388)
KON = a constant with a value of 400nsV

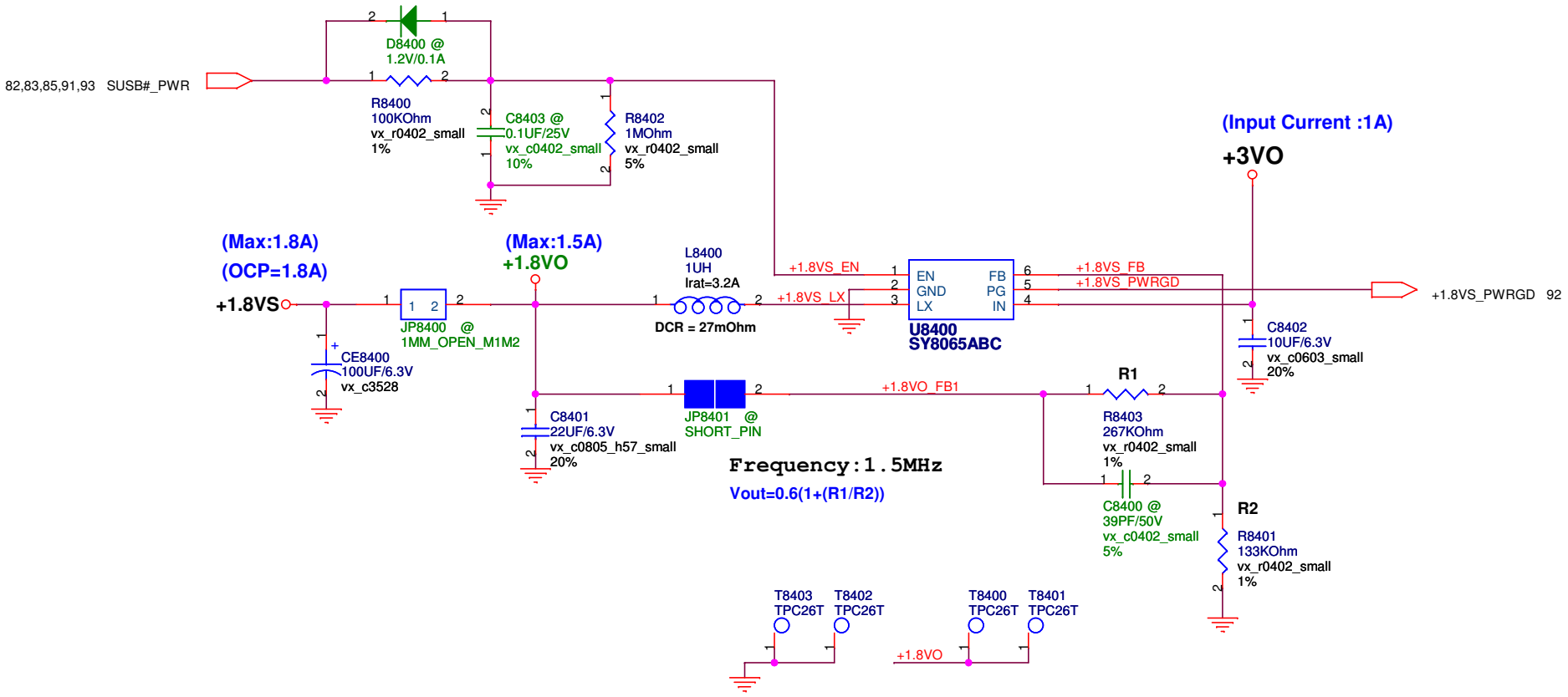
+0.75VS POWER SUPPLY



<Variant Name>

PEGATRON	Title : POWER_DDR & VTT	
	Engineer: Clark Liang	
Size: Custom	Project Name: MA50	Rev: 1.0
Date: Monday, February 13, 2012	Sheet 83 of 94	

+1.8VS POWER SUPPLY



<Variant Name>

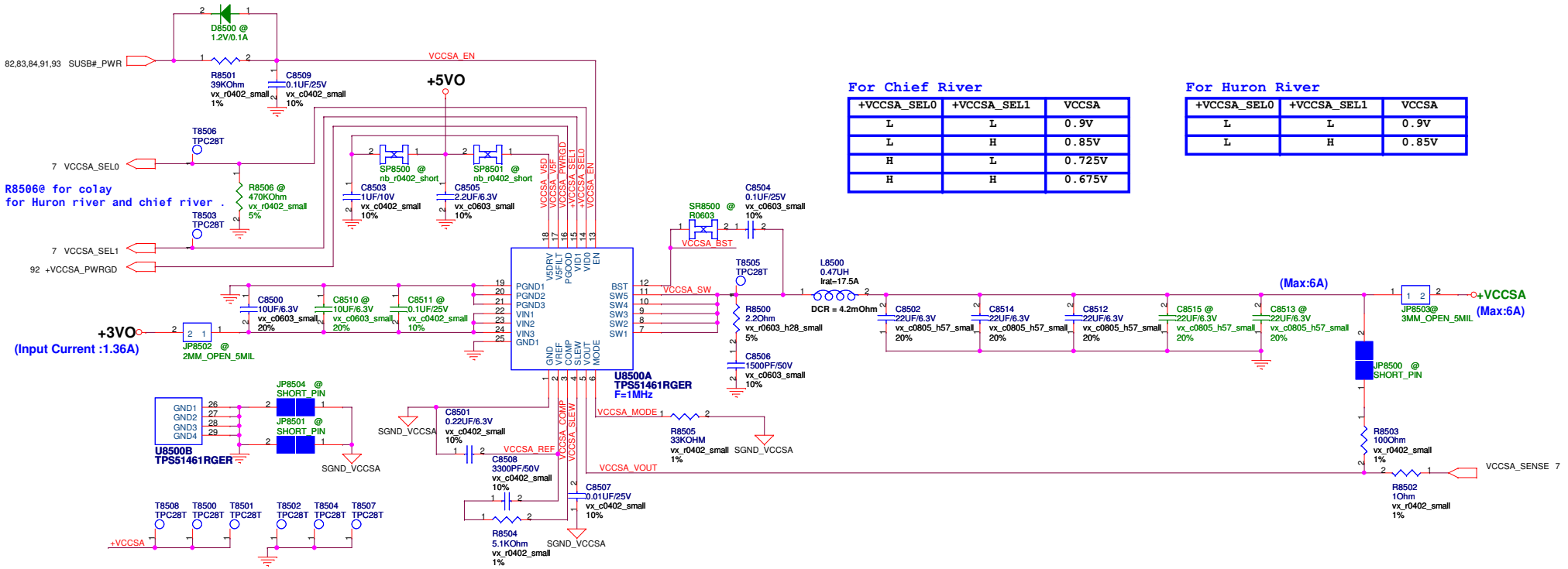
PEGATRON Title : POWER_+1.8VS

Engineer: Clark Liang

Size	Project Name	Rev
Custom	MA50	1.0

Date: Monday, February 13, 2012 Sheet 84 of 94

IVB VCCSA POWER SUPPLY



For Chief River

+VCCSA_SEL0	+VCCSA_SEL1	VCCSA
L	L	0.9V
L	H	0.85V
H	L	0.725V
H	H	0.675V

For Huron River

+VCCSA_SEL0	+VCCSA_SEL1	VCCSA
L	L	0.9V
L	H	0.85V

<Variant Name>

PEGATRON Title :POWER_+VCCSA_0.85VS

Engineer: Clark Liang

Size	Project Name	Rev
Custom	MA50	1.0

Date: Monday, February 13, 2012 Sheet 85 of 94

<Variant Name>

PEGATRON

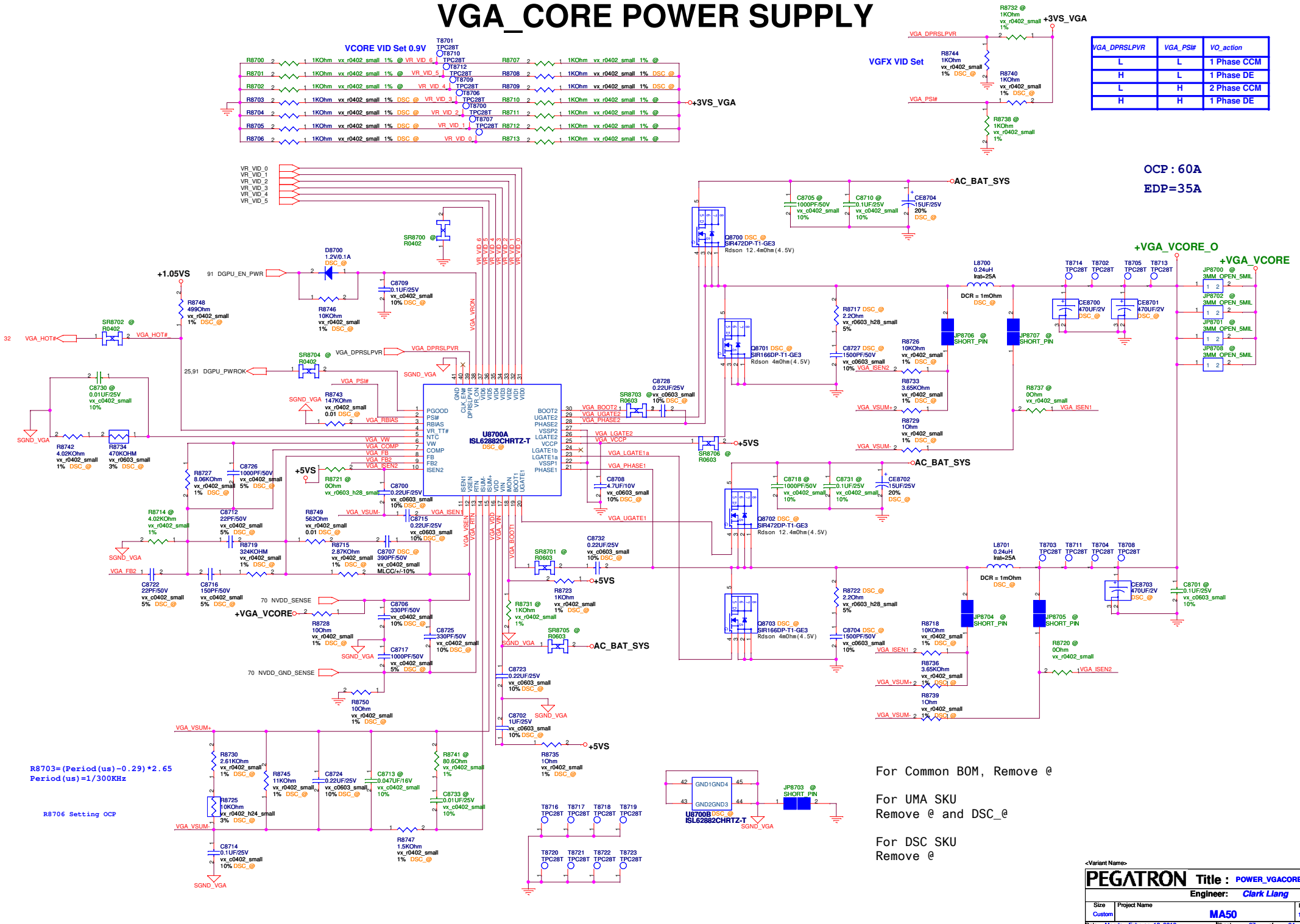
Title : POWER_N/A

Engineer: *Clark Liang*

Size	Project Name	Rev
Custom	MA50	1.0

Date: Monday, February 13, 2012 Sheet 86 of 94

VGA_CORE POWER SUPPLY



VGA_DPRSLPVR	VGA_PSI#	VO_action
L	L	1 Phase CCM
H	L	1 Phase DE
L	H	2 Phase CCM
H	H	1 Phase DE

<variant_name>

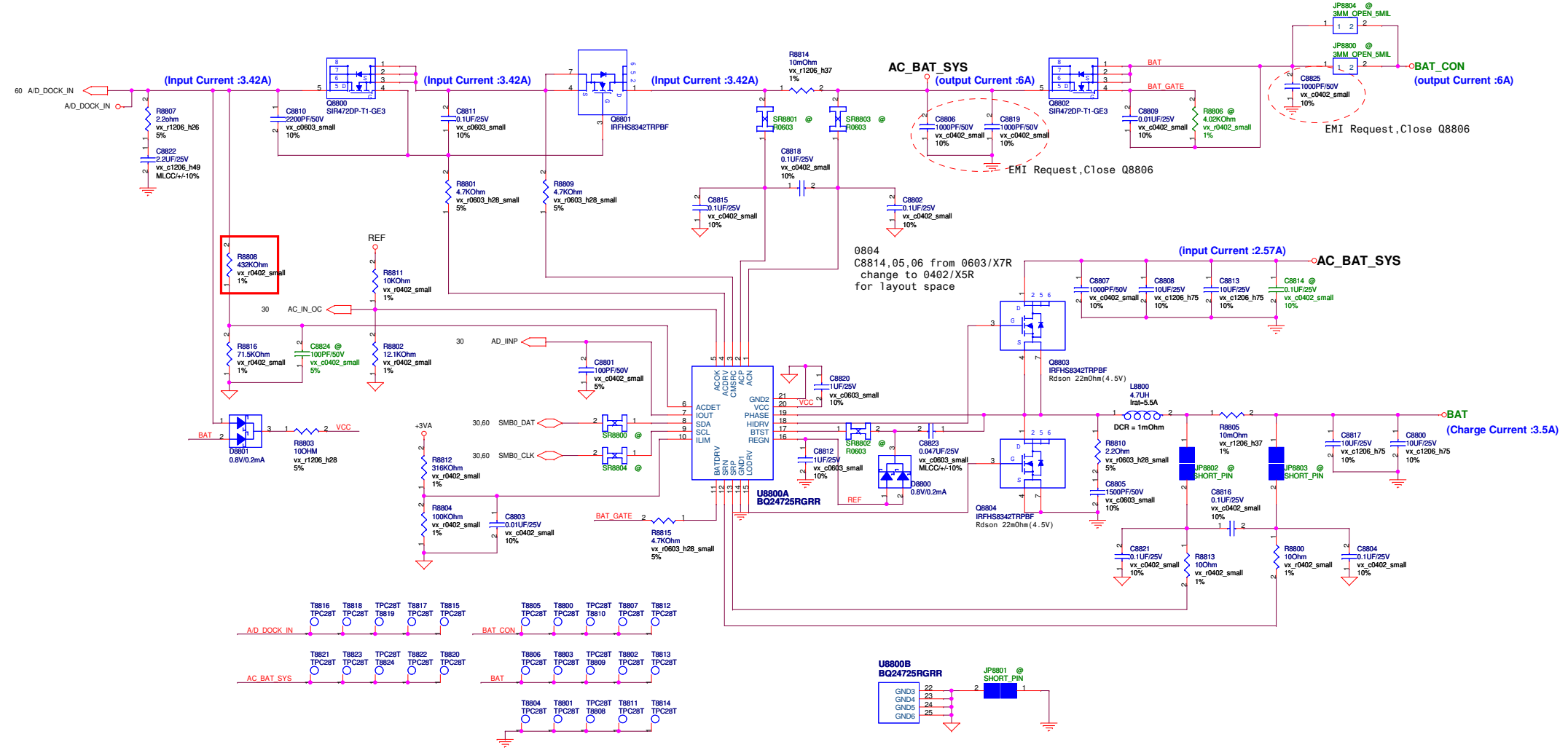
PEGATRON Title : POWER_VGACORE

Engineer: Clark Liang

Size	Project Name	Rev
Custom	MA50	1.0

Date: Monday, February 13, 2012 Sheet 87 of 94

BATTERY CHARGER



<Variant Name>

PEGATRON Title : POWER_CHARGER

Engineer: Clark Liang

Size	Project Name	Rev
Custom	MA50	1.0

Date: Monday, February 13, 2012 Sheet 88 of 94

<Variant Name>

PEGATRON

Title : POWER_N/A

Engineer: *Clark Liang*

Size	Project Name	Rev
Custom	MA50	1.0

Date: Monday, February 13, 2012 Sheet 89 of 94

BATTERY IN DETECT

<Variant Name>

PEGATRON

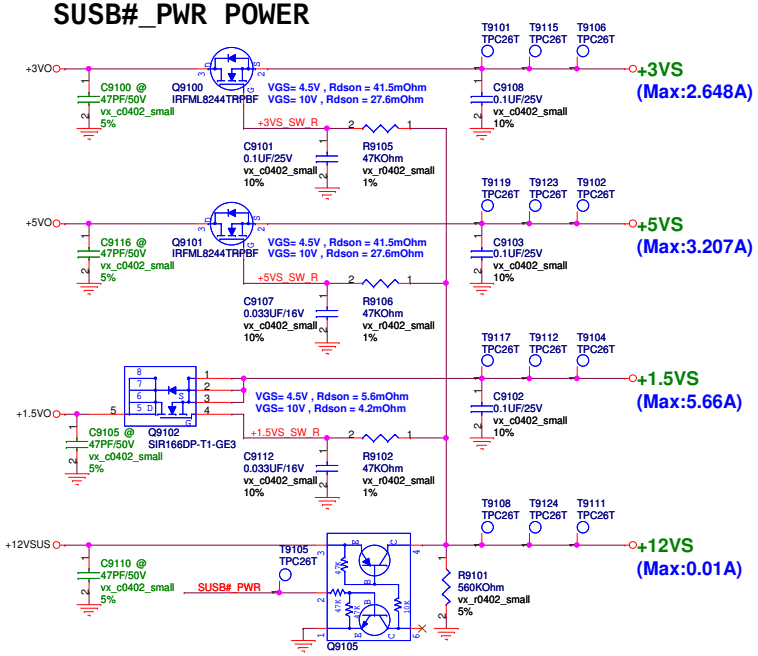
Title : POWER_DETECT

Engineer: Clark Liang

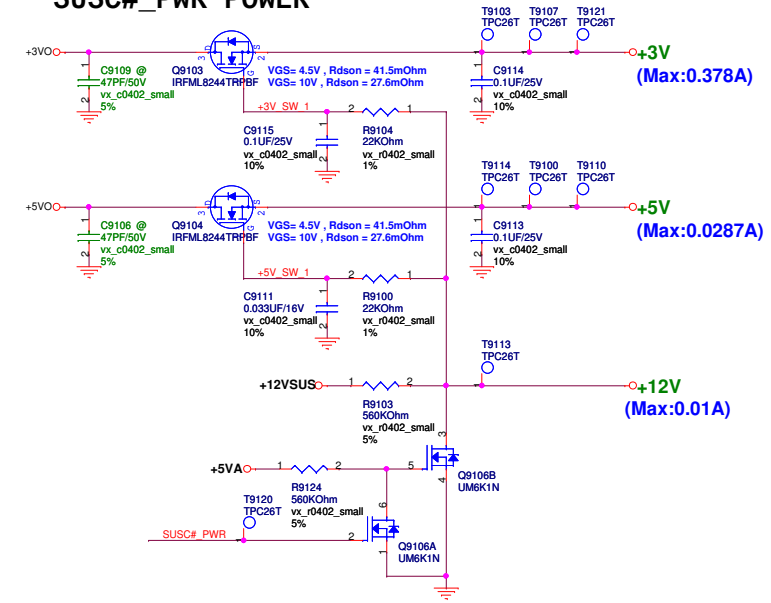
Size	Project Name	Rev
Custom	MA50	1.0

Date: Monday, February 13, 2012 Sheet 90 of 94

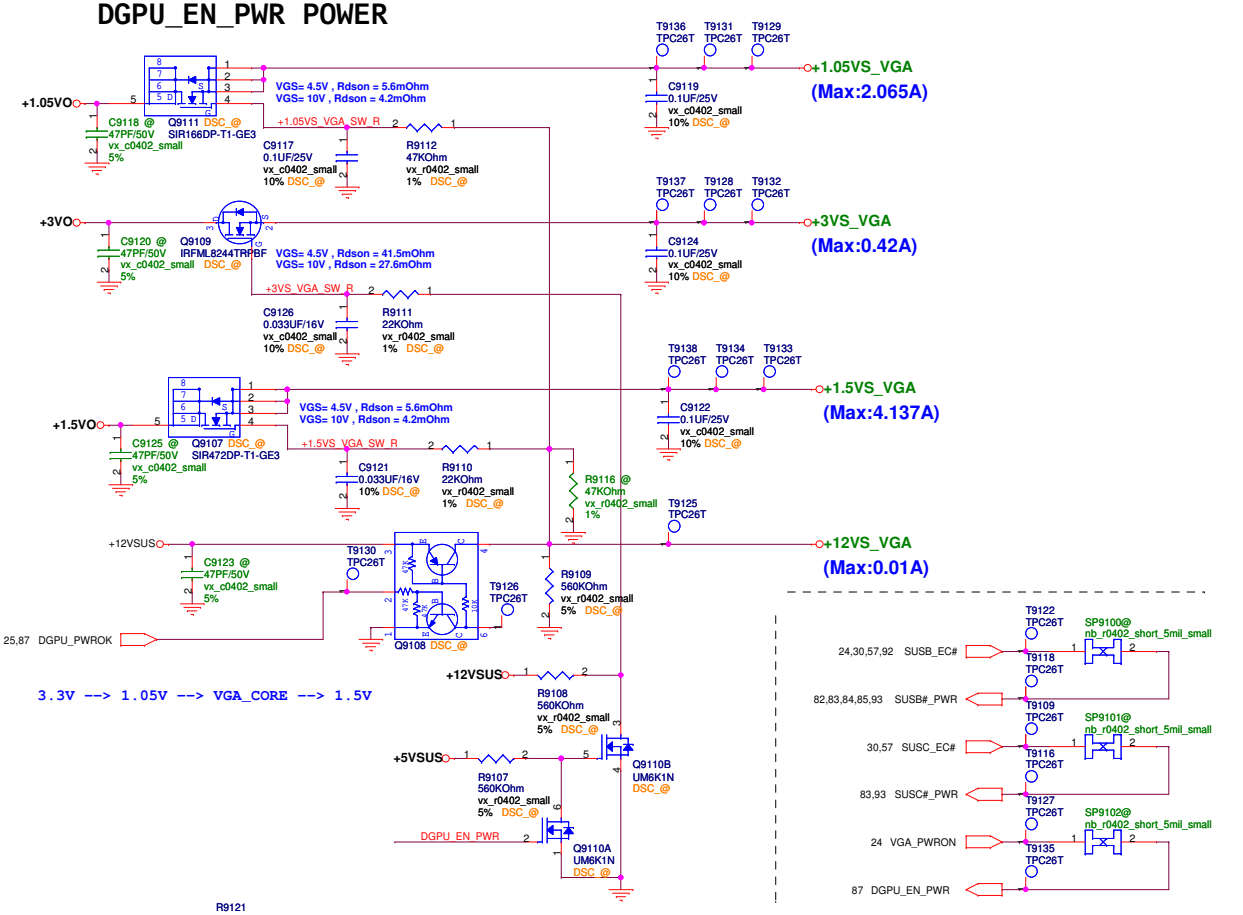
SUSB#_PWR POWER

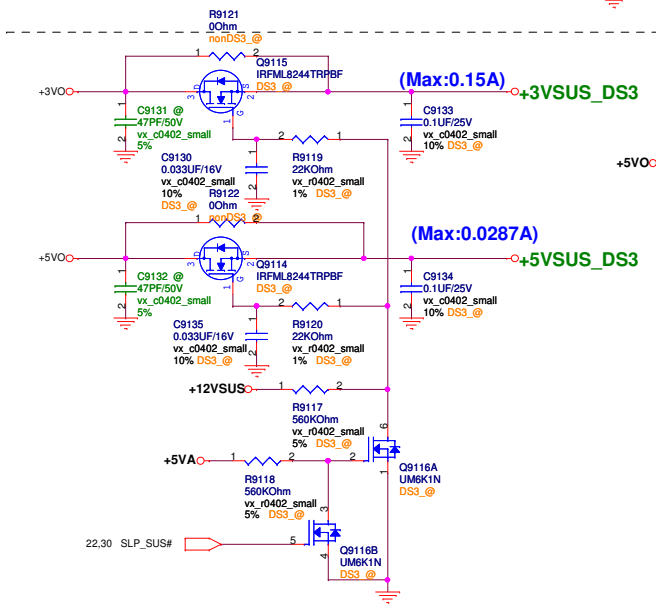


SUSC#_PWR POWER

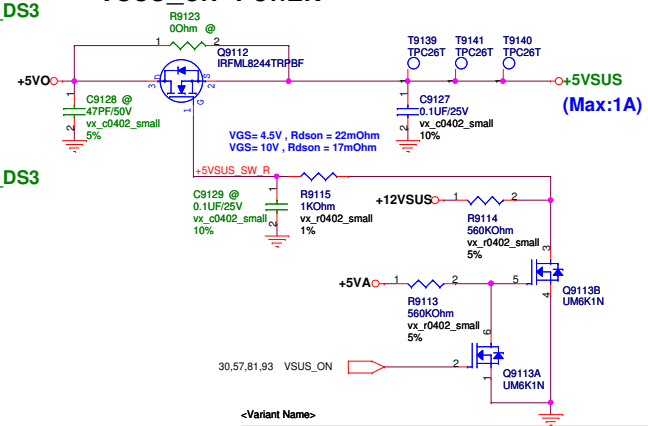


DGPU_EN_PWR POWER





VSUS_ON POWER



<Variant Name>

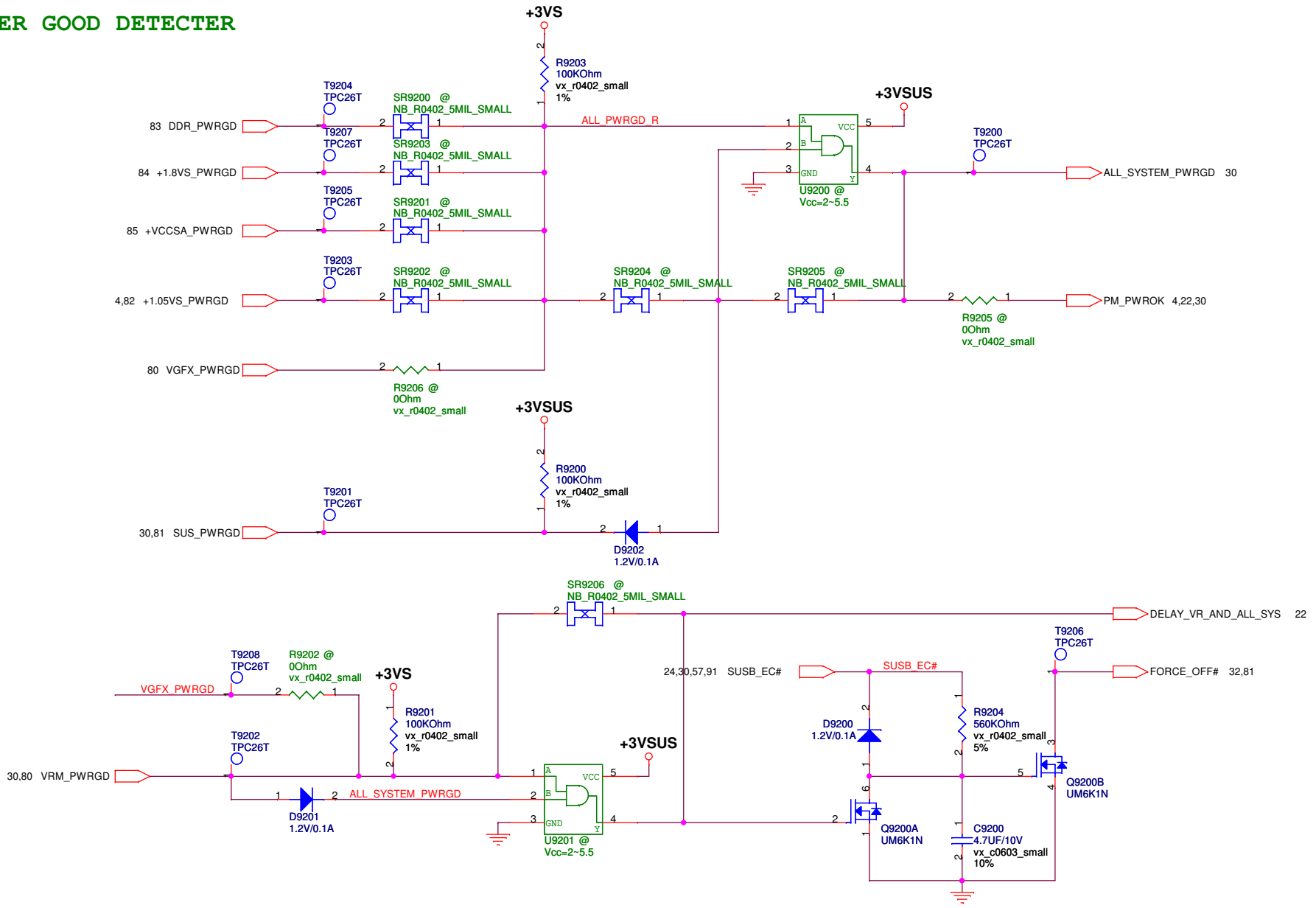
PEGATRON Title : POWER_LOAD SWITCH

Engineer: Clark Liang

Size	Project Name	Rev
Custom	MA50	1.0

Date: Monday, February 13, 2012 Sheet 91 of 94

POWER GOOD DETECTER



<Variant Name>

PEGATRON	Title : POWER_PROTECT	
	Engineer: Clark Liang	
Size: Custom	Project Name: MA50	Rev: 1.0
Date: Monday, February 13, 2012	Sheet 92 of 94	

AC_BAT_SYS
BAT
BAT_CON

AC_BAT_SYS 45,53,81,87,88
BAT 88
BAT_CON 60,88

+5VA
+3VA

+5VA 37,60,81,91
+3VA 6,20,26,27,30,31,57,59,60,81,88

+5VO
+3VO
+1.8VO
+1.5VO
+1.05VO
+0.75VO

+5VO 52,65,80,81,82,83,85,91
+3VO 53,81,84,85,91
+1.8VO 60,84
+1.5VO 83,91
+1.05VO 82,91
+0.75VO 83

+12VSUS
+5VSUS
+3VSUS

+12VSUS 28,51,81,91
+5VSUS 51,57,59,91
+3VSUS 4,22,24,28,30,60,81,92

+12V
+5V
+3V
+1.5V

+12V 60,91
+5V 57,59,60,91
+3V 24,45,57,59,61,91
+1.5V 5,16,17,18,57,60,83

+12VS
+5VS
+3VS
+1.8VS
+1.5VS
+1.05VS
+VCCSA
+0.75VS

+12VS 28,36,48,91
+5VS 27,36,37,48,50,51,57,80,87,91
+3VS 17,20,21,22,23,24,25,26,27,28,30,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92
+1.8VS 7,25,26,57,80,84
+1.5VS 7,26,53,57,91
+1.05VS 26,27,57,82,87
+VCCSA 7,85
+0.75VS 16,17,57,83

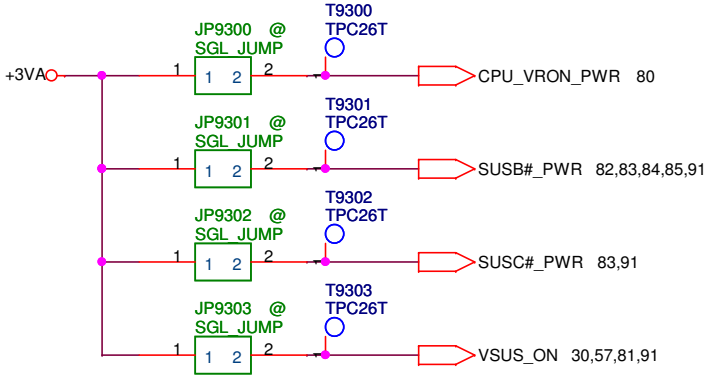
+VCORE
+VGFX_CORE

+VCORE 6,9,11,80
+VGFX_CORE 7,9,80

+12VS_VGA
+3VS_VGA
+1.5VS_VGA
+1.05VS_VGA

+12VS_VGA 60,91
+3VS_VGA 57,70,72,74,75,87,91
+1.5VS_VGA 57,71,75,76,77,91
+1.05VS_VGA 57,70,71,72,91

FOR POWER TEST



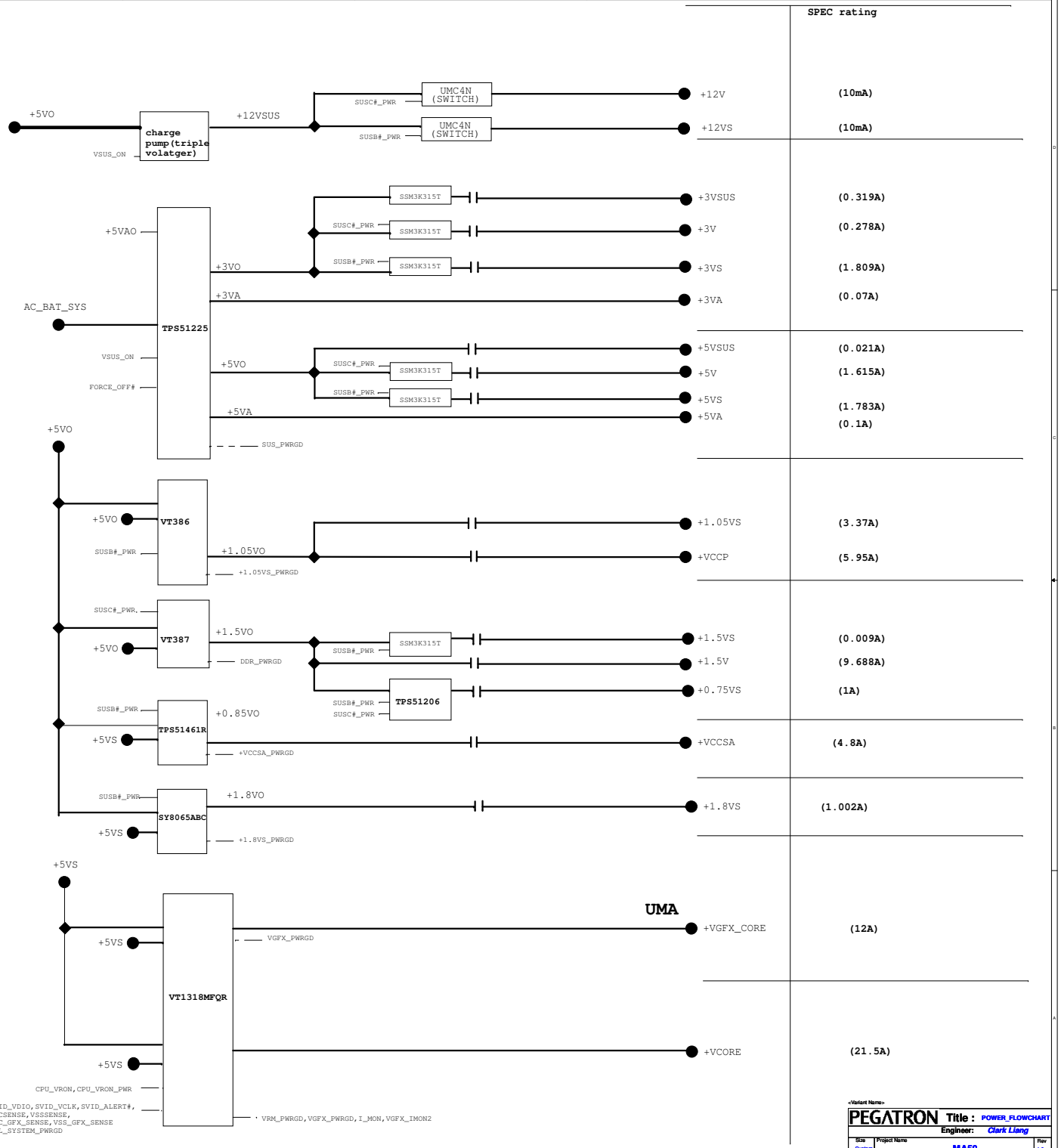
<Variant Name>

PEGATRON Title : POWER_SIGNAL

Engineer: Clark Liang

Size	Project Name	Rev
Custom	MA50	1.0

Date: Monday, February 13, 2012 Sheet 93 of 94



<Variant Name>

PEGATRON Title : POWER_FLOWCHART

Engineer: Clark Liang

Size	Project Name	Rev
Custom	MA50	1.0

Date: Monday, February 13, 2012 Sheet 84 of 94

PEGATRON	Title : ****
BG1\HW1	Engineer: *Joyoung_Chianhg*
Size: A	Project Name: **MA50**
Rev: 1.3	
Date: Monday, February 13, 2012	Sheet 96 of 93

SR BOM change

SR1.1 Un-mount Q5602, Q5601 and mount R5323 and R5310

SR1.2 CE5001 un-mount

SR1.3 L3602 mount

SR1.4 R7005 un-mount

SR1.5 R7410 change 10K ohm

SR1.6 R4504 change 10K ohm for LVDS backlight

SR1.7 R7430, R7432, R7433 un-mount

SR1.8 R7608, R7611 change 162 ohm

ER

ER1.1 PI pin connect to ESD and VDD pin reserve 0.1 uF cap
ER1.2 Add diode and reserve 0 ohm for AC adapter plug in /out voice
ER1.3 U5201 change G547G1P81U for Desing IP
ER1.4 Add Card Reader LED
ER1.5 J3701, J3702, J4601, J5201, J5304,J5001 chang connector
ER1.6 R6505~R6508 change 0603 size
ER1.7 D4801 contact to 2.2K ohm for EA solution in HDMI issue
ER1.8 CPU_THERM# contact to FORCE_OFF#
ER1.9 RTC battery connector (J2001)Pin1, Pin2 swap
ER1.10 D3707, D4618, D5201, D5301, D6502, D6503, D6802 VDD pin reserve 0.1 uF cap
ER1.11 R3720 R3721 change 51ohm for consumer spec in HP
ER1.12 L4601, L4602, L4603 change 27nH and add C4622, C4623, C4624 for EA solution in CRT
ER1.13 L5301, L5302, L5306 change 0 ohm and L5305 change short pin,
C5321, C5327,C5307, C5322, C5315, C5305, C5313 change umount
ER1.14 Change R4566 from 300(0603) to 150(0402) for LVDS power sequence solution
ER1.15 USB port 0 and port 1 swap
ER1.16 Vcore_add CE8002&CE8006 to replace CE0601&CE0602
ER1.17 VGFX_CORE(IGPU) add CE8007 to replace CE0705
ER1.18 reserve M_VREF schematic
ER1.19 Reserve C2623, C2624, C4514, C4515 for WLAN solution
ER1.20 Reserve C4510, C4512, C4513 for 3G and L6002~L6004, L4502 change 47 ohm Bead
ER1.21 C6007, C6006 mount for WLAN
ER1.22 RN3002 change 2R4P
ER1.23 LED and BT schematic change to LED board
ER1.24 LED power change 5VSUS, so R5618, R5616, R5623 change 560 ohm
ER1.25 VRAM change co-lay footprint
ER1.26 Reserve C5601, C5602, C5603, C6356, C6357 to 47pF for RF request
ER1.27 Reserve C4516, C4517 to 10pF for RF request
ER1.28 U6504,U6505 change AZ3028 for EMI request
ER1.29 D6401, D6501, D6502 change ESD AZ5023 in for EMI request in LAN function
ER1.30 Add C6010 C6011 for EMI request
ER1.31 Merge Q6704 and remove U6704
ER1.32 D3720 change to mount for EMI request
ER1.34 Reserve C6913(47PF), C6902(0.1uF), C6623(47PF), C6606(22uF) for 3G
ER1.35 L6601=>0901-00HI000 FERRITE BEAD(1206)390 OHM/2A

PR

PR2.1 RTC pin define swap

PR_S01:Change C3627,C3626 from X5R to Y5V

PR_S02:According with INTEL datasheet suggest.(Power circuit mount)

PR_S03:To prevent 誤動作 PCIE Wake.

PR_S04:To change WLAN LED control by MODULE then gate control by 3G LED.

PR_S05:To change 3G LED control by MODULE.

PR_S06:To prevent leakage current and mount R for cost down.

PR_S07:RF reserve.

PR_S08:Move P.U 10K near 3G connector.

PR_S09:Change LED POWER rail from +5VSUS_LEDDB(+5VSUS) to
+5VA_LEDDB(+5VA) .(To resolve Battery LL issue)

PR_S10:Change LED POWER rail from
+5VSUS_LEDDB(+5VSUS) to +5V_LEDDB(+5V)

PR_S11:Del JP, +3VS_CR change Net name to +3VS

PR_S12:ESD change solution ,Add U6512 ,Del C6509,D6501~3,U6502,U6503,D6401

PR_S13:Change NET name to +3VS

PR_S14:Change 10uF to 22uF for wave of CRT display.

PR_S15:Add 10uF (C6803)for USB droop test.

PR_S16:D5201 PIN Swap

PR_S17:ME modify.(H6532,8,1,9,4,3,5,H6945),DEL H6944

PR_S18:EMI add.

PR_S19:Change to unmount for ME

PR_S20:RF request.

PR_S21:LED light fine-tune.

PR_S22:BIOS request for UMA and DSC platform identifying.

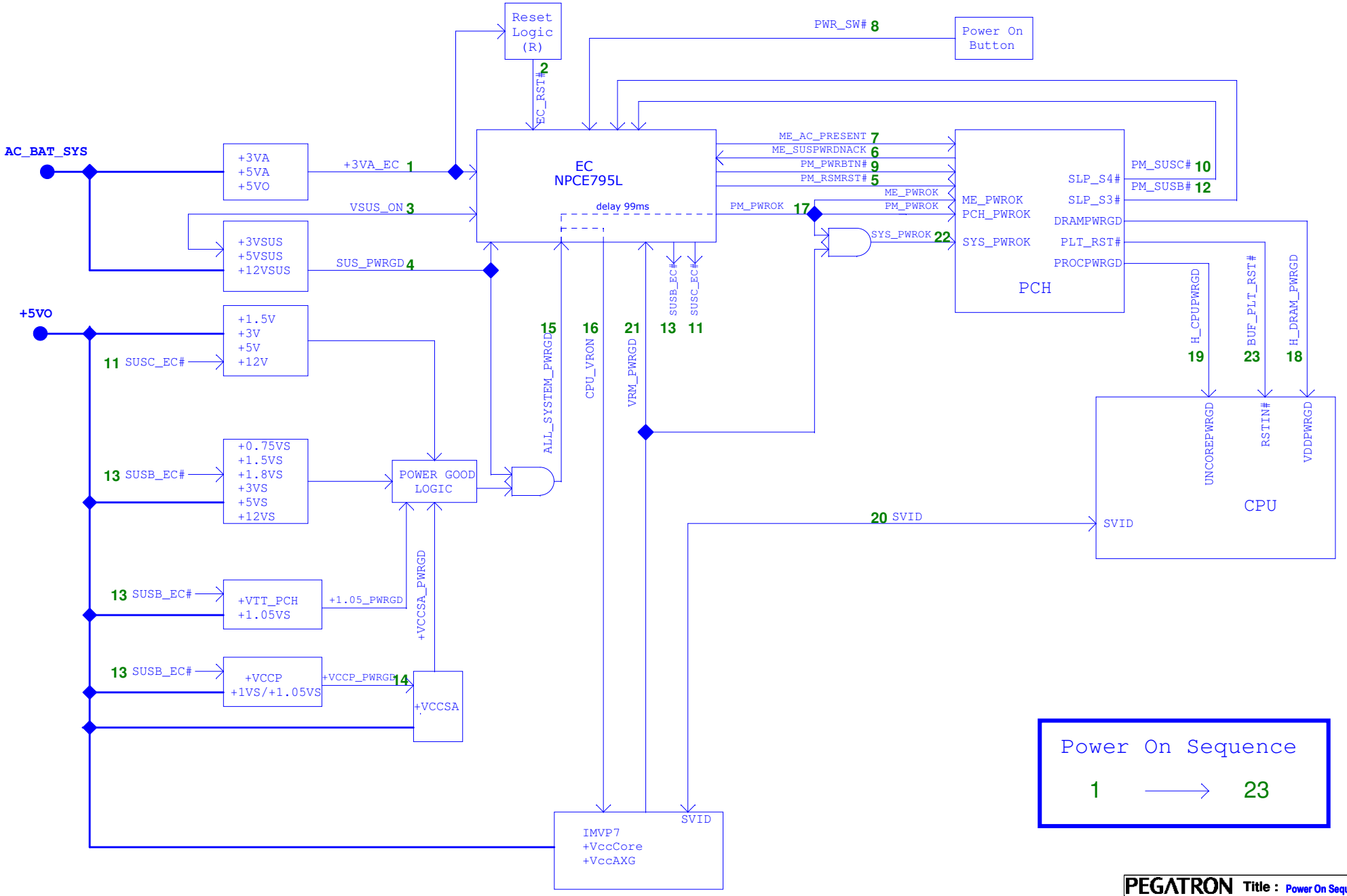
PEGATRON Title : ****

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	MA50	1.3

Date: Monday, February 13, 2012 Sheet 97 of 93

Power On Sequence Diagram G3-S0 R0.3 (non-iAMT,non-Deep Sx)



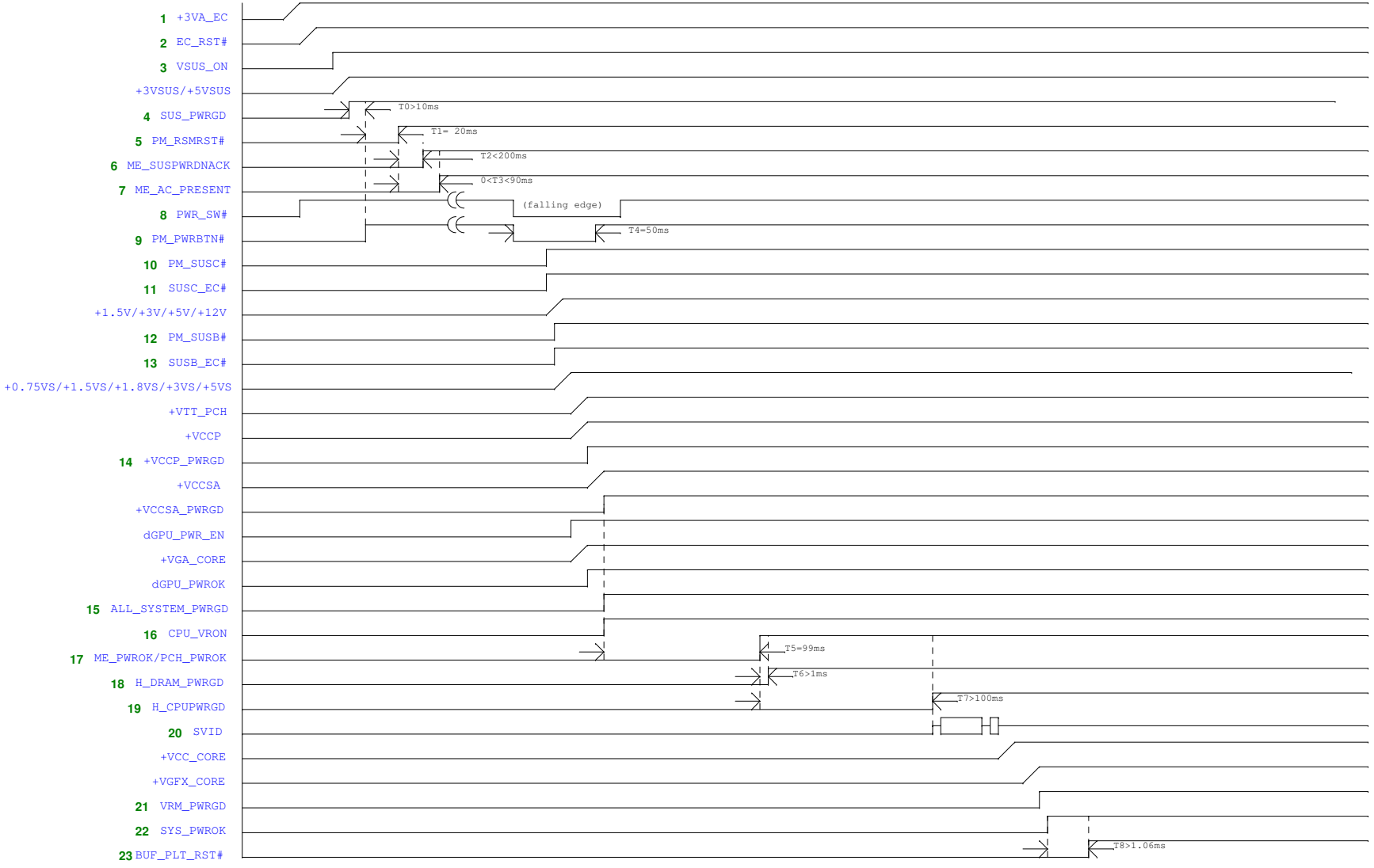
PEGATRON Title : Power On Sequence

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	MA50	1.3

Date: Monday, February 13, 2012 Sheet 98 of 93

Power On Sequence Diagram G3-S0 R0.3 (non-iAMT,non-Deep Sx)



PEGATRON	Title : Power On Timing	
<OrgName>	Engineer: Joyoung_Chianhg	
Size: C	Project Name: MA50	Rev: 1.3
Date: Monday, February 13, 2012	Sheet 99 of 93	