Eiger Block Diagram

Project code: 91.4Z501.001
PCB P/N : 48.4Z501.001
REVISION : 07246- -1

CLK GEN.
ICS 9LPRS365BKLFT 3

Mobile CPU
Penryn 4, 5

THERMAL EMC2102 23

HOST BUS 667/800/1067MHz@1.05V

DDR2 DIMM1
667/800 MHz 12

DDR2 DIMM2
667/800 MHz 13

667/800MHz

667/800MHz

Cantiga 6,7,8,9,10,11
- AGTL+ CPU I/F
- DDR Memory I/F
- INTEGRATED GRAHPICS
- LVDS, CRT I/F

CRT 17
LCD 15
HDMI 18

PCIex16

MXM CONN 30

X4 DMI 400MHz

C-Link0

ICH9M 19,20,21,22
- 6 PCIe ports
- PCI/PCI BRIDGE
- ACPI 2.0
- 4 SATA
- 12 USB 2.0/1.1 ports
- ETHERNET (10/100/1000MbE)
- High Definition Audio
- LPC I/F
- Serial Peripheral I/F
- Matrix Storage Technology(DO)
- Active Managemnet Technology(DO)

INT.MIC 35
Line In 35
MIC In 35
INT.SPKR 35
Line Out (SPDIF) 35
RJ11

Codec ALC888S VC 33

AZALIA

OP AMP G1431Q 34

OP AMP G1412 34

MODEM MDC Card 25

SPI

BIOS/DASH 2Mb 37

SATA

HDD SATA 24

ODD SATA 24

SATA

PCIex1 CardReader JMicro JMB385 27 → MS/MS Pro/xD /MMC/SD 5 in 1 27

PCIex1 LAN Giga LAN 88E8071 28 → TXFM 29 → RJ45 29

PCIex1 New card 31 → PWR SW G577BR91U 31

PCIex1 Mini Card Kedron a/b/g/n 32

PCIex1 Mini Card Kedron a/b/g/n 32

LPC BUS

USB

Blue Tooth (USB) 25

eSATA 24

Camera (USB) 15

USB 4 Port 26

KBC ENE3310 36
- Touch Pad 36
- Finger Printer
- INT. KB 36
- Launch Buttom 14
- CIR 36

BIOS Winbond W25X80 8M Bits 37

LPC DEBUG CONN 37

Port Replicator 38

PCB STACKUP

TOP
VCC
S
S
GND
BOTTOM

SYSTEM DC/DC TPS51125 43	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC TPS51124 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

RT9026 44	
1D8V_S3	DDR_VREF_S0 DDR_VREF_S3

RT9018A 44	
1D8V_S3	1D5V_S0

G9131 44	
3D3V_S0	2D5V_S0

GFXCORE DC/DC ISL6263 46	
INPUTS	OUTPUTS
DCBATOUT	VGFXCORE 0.7~1.25V

CPU DC/DC ISL6266A 42	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0.35~1.5V

CHARGER BQ24745 47	
INPUTS	OUTPUTS
DCBATOUT	BT+ DCBATOUT

UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM
Size: Custom | Document Number: Eiger | Rev: -1
Date: Tuesday, April 01, 2008 | Sheet 1 of 50

ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

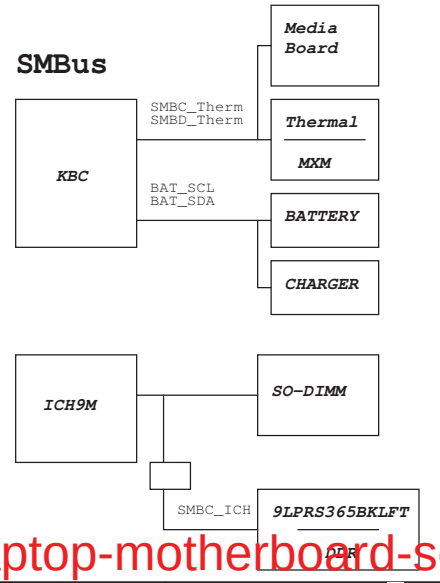
PCIE Routing

LANE1	LAN MARVELL 88E8071
LANE2	MiniCard WLAN
LANE3	MiniCard WWAN/TV
LANE4	JMB385 Card Reader
LANE5	NewCard
LANE6	*NC*

USB Table

USB	
Pair	*Device*
0	*USB1*
1	*USB4*
2	*USB2*
3	*USB5(DOCK)*
4	*USB3*
5	*Bluetooth*
6	*FP*
7	*MINIC1*
8	*WEBCAM*
9	*NEW1*
10	*MINIC2*
11	*NC*

SMBus



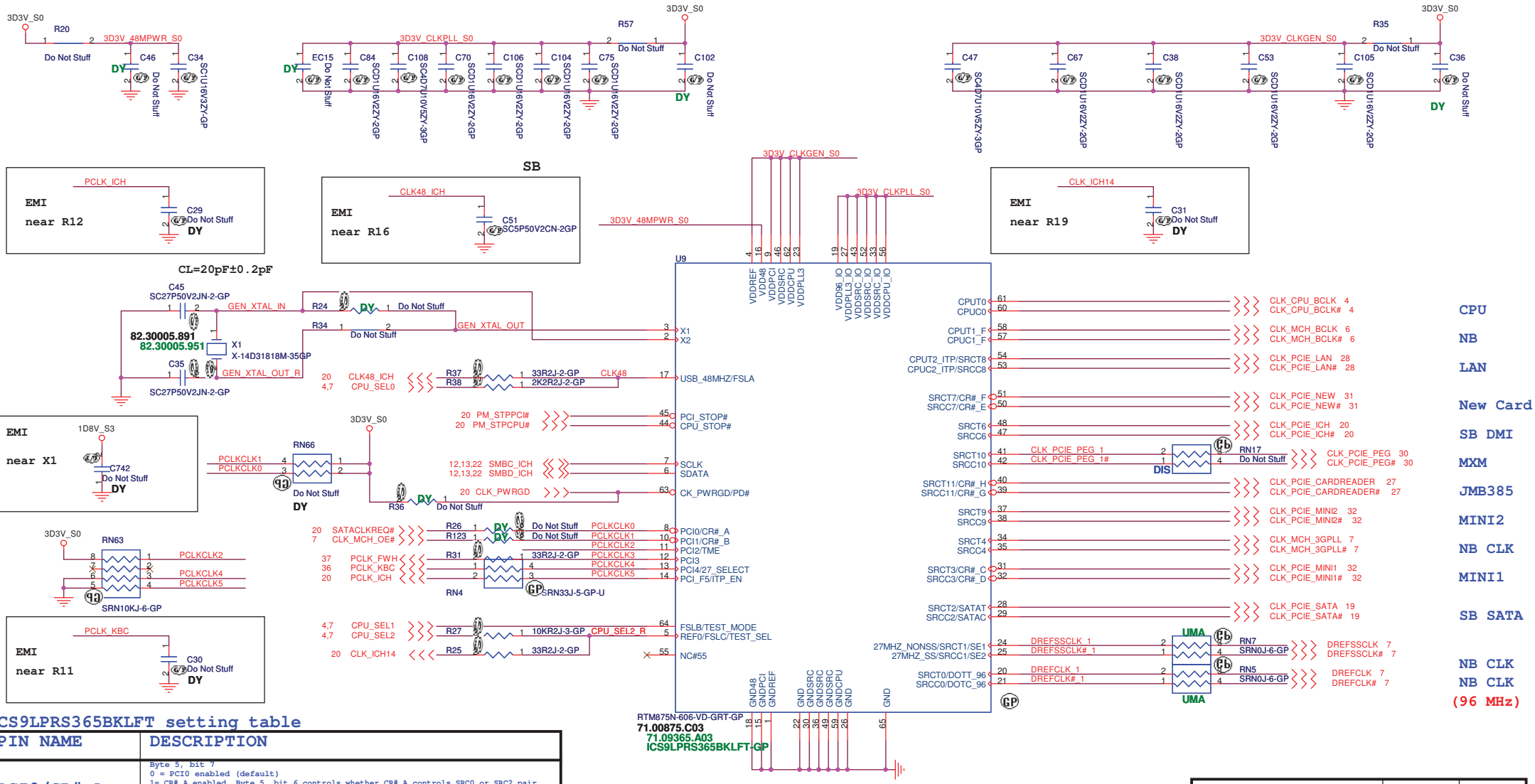
UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Reference**

Size: A3 | Document Number: **Eiger** | Rev: **-1**

Date: Tuesday, April 01, 2008 | Sheet 2 of 50



ICS9LPRS365BKLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	3.3V PCI clock output
PCI4/27M_SEL	0 = Pin24 as SRC-1, Pin25 as SRC-1#, Pin20 as DOT96, Pin21 as DOT96# 1 = Pin24 as 27MHz, Pin25 as 27MHz_SS, Pin20 as SRC-0, Pin21 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1066M

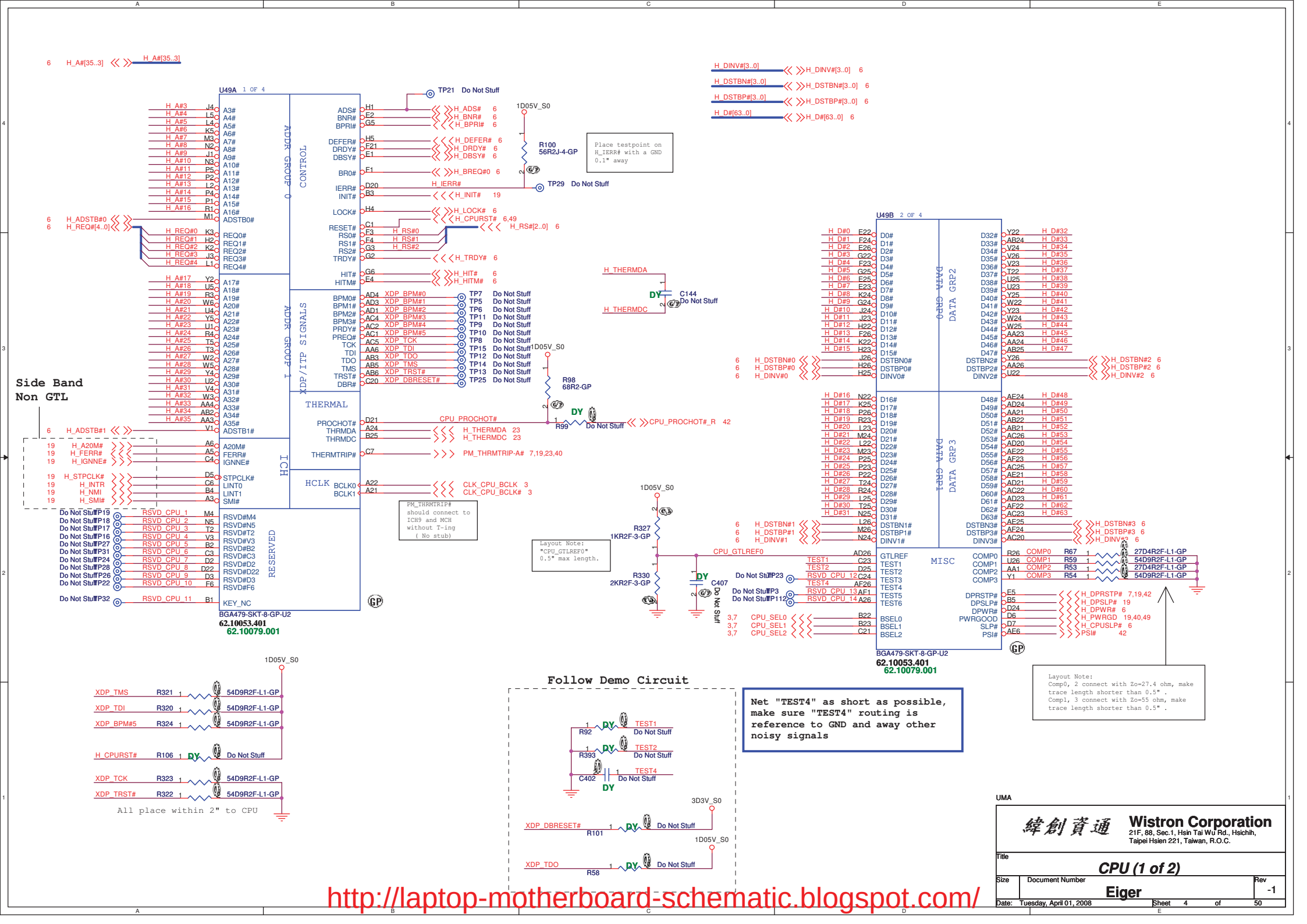
UMA

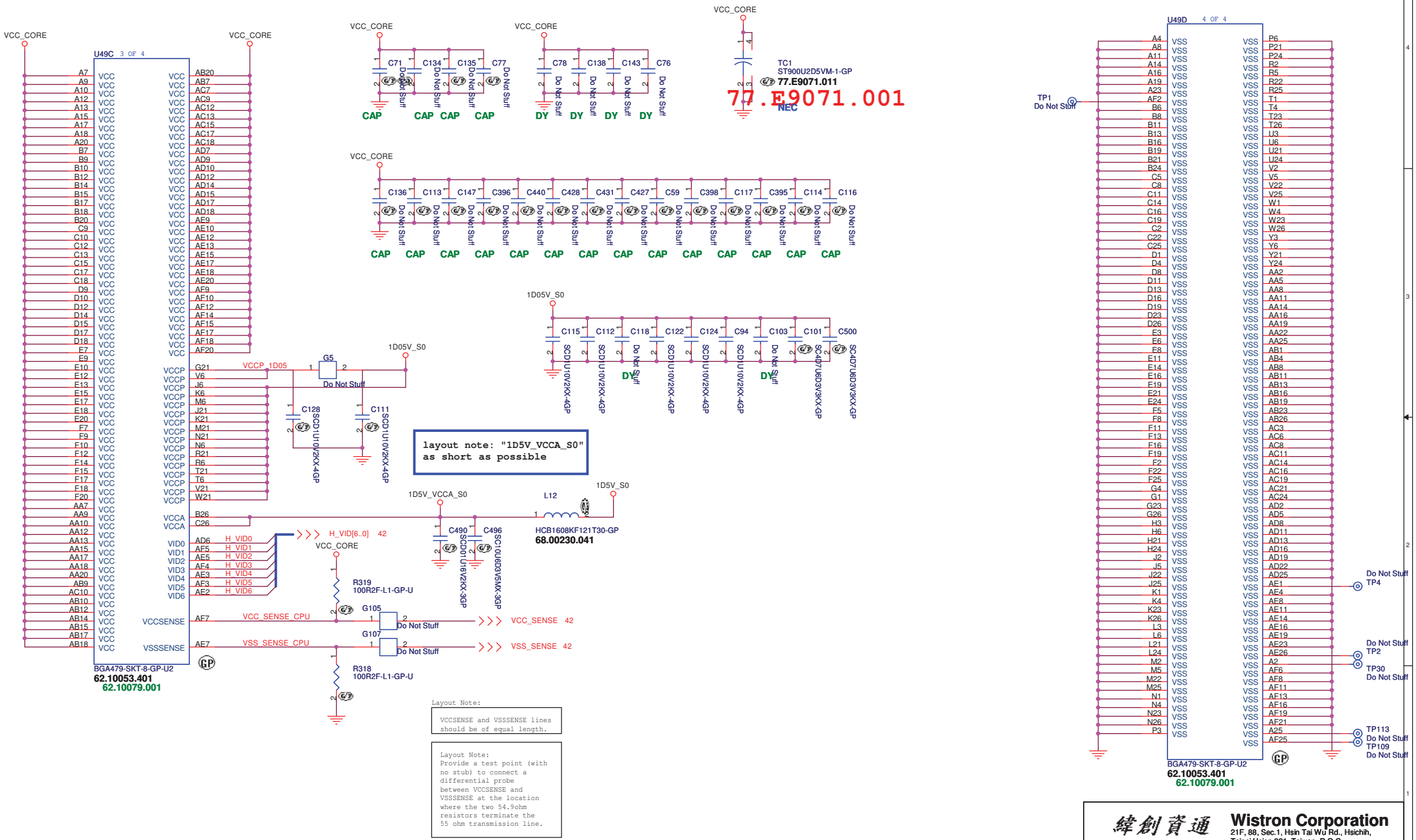
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Clock Generator

Size | Document Number: Eiger | Rev: -1

Date: Tuesday, April 01, 2008 | Sheet 3 of 50


U49A 1 OF 4
U49B 2 OF 4
BGA479-SKT-8-GP-U2
62.10053.401
62.10079.001
Side Band
Non GTL
Follow Demo Circuit
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
All place within 2" to CPU
Layout Note: "CPU_GTLREF0" 0.5" max length.
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5". Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5".
Place testpoint on H_IERR# with a GND 0.1" away
PM_THRMTRIP# should connect to ICH9 and MCH without T-ing (No stub)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
UMA
CPU (1 of 2)
Eiger
Date: Tuesday, April 01, 2008
Sheet 4 of 50
http://laptop-motherboard-schematic.blogspot.com/

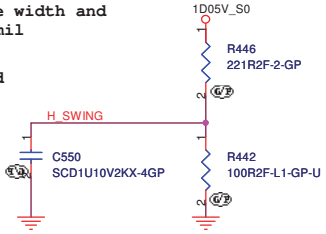


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (2 of 2)
Size | Document Number: Eiger | Rev: -1
Date: Tuesday, April 01, 2008 | Sheet 5 of 50

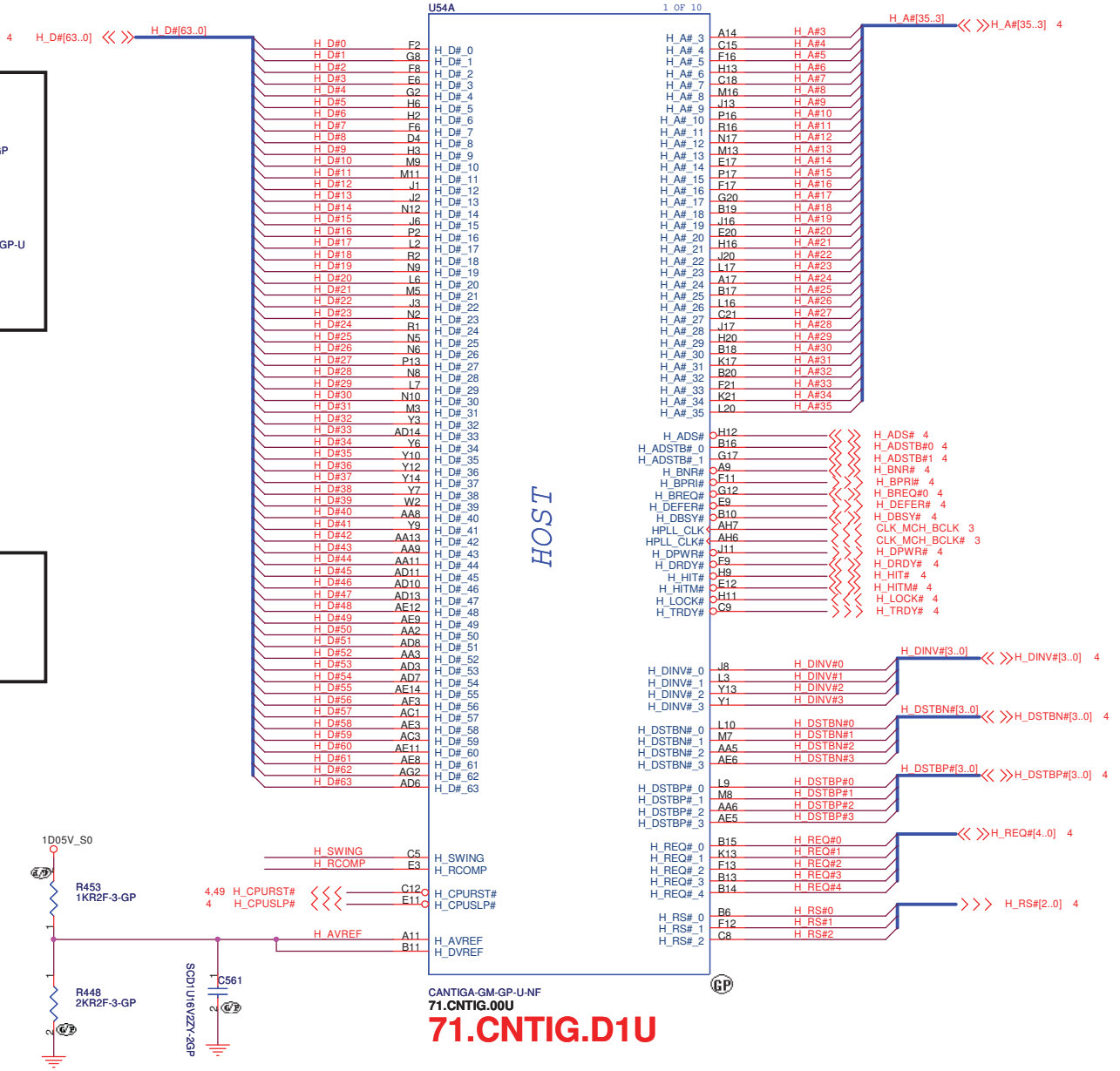
H_SWING routing Trace width and Spacing use 10 / 20 mil

H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil

Place them near to the chip (< 0.5")



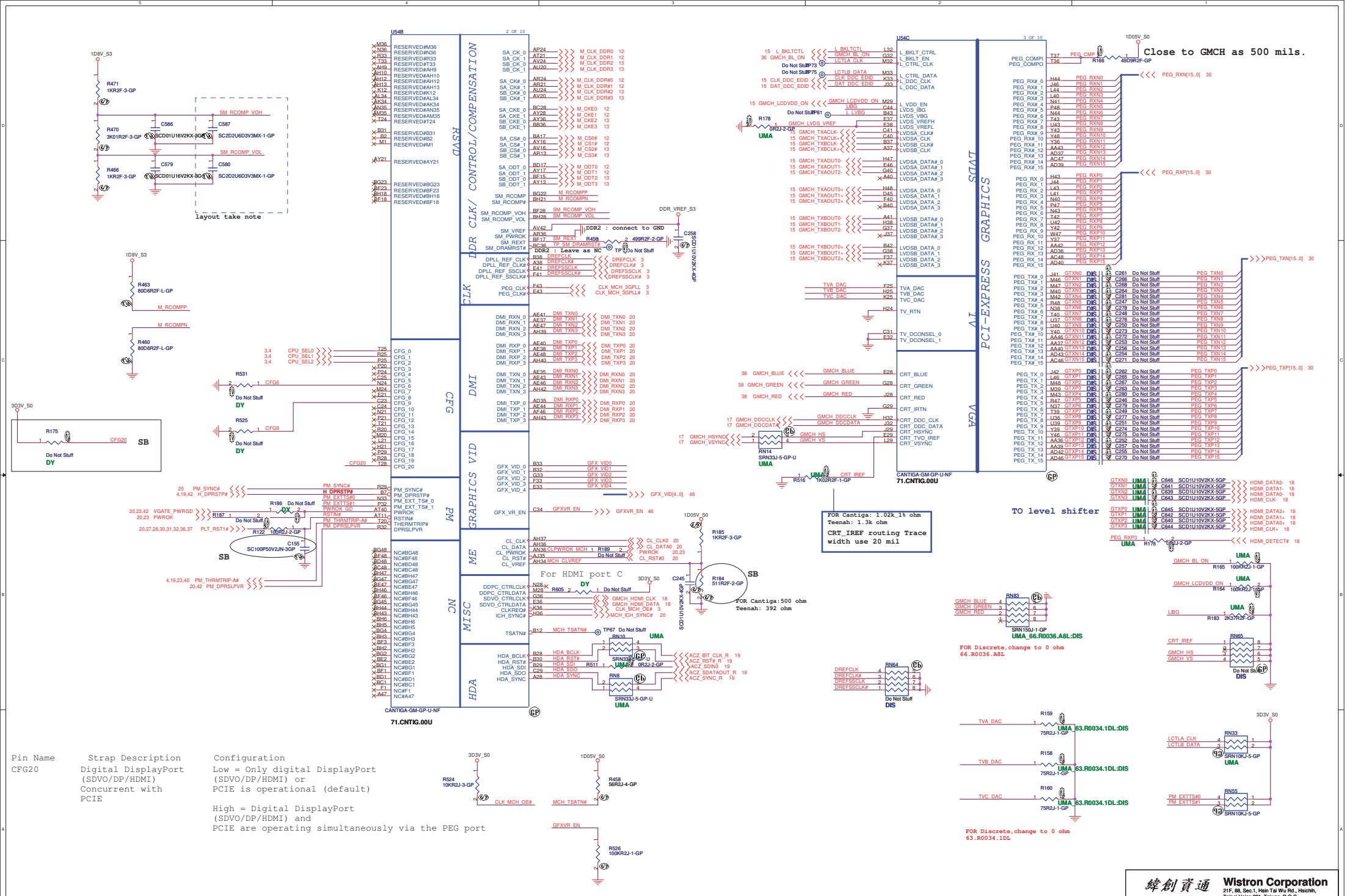
UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga (1 of 6)

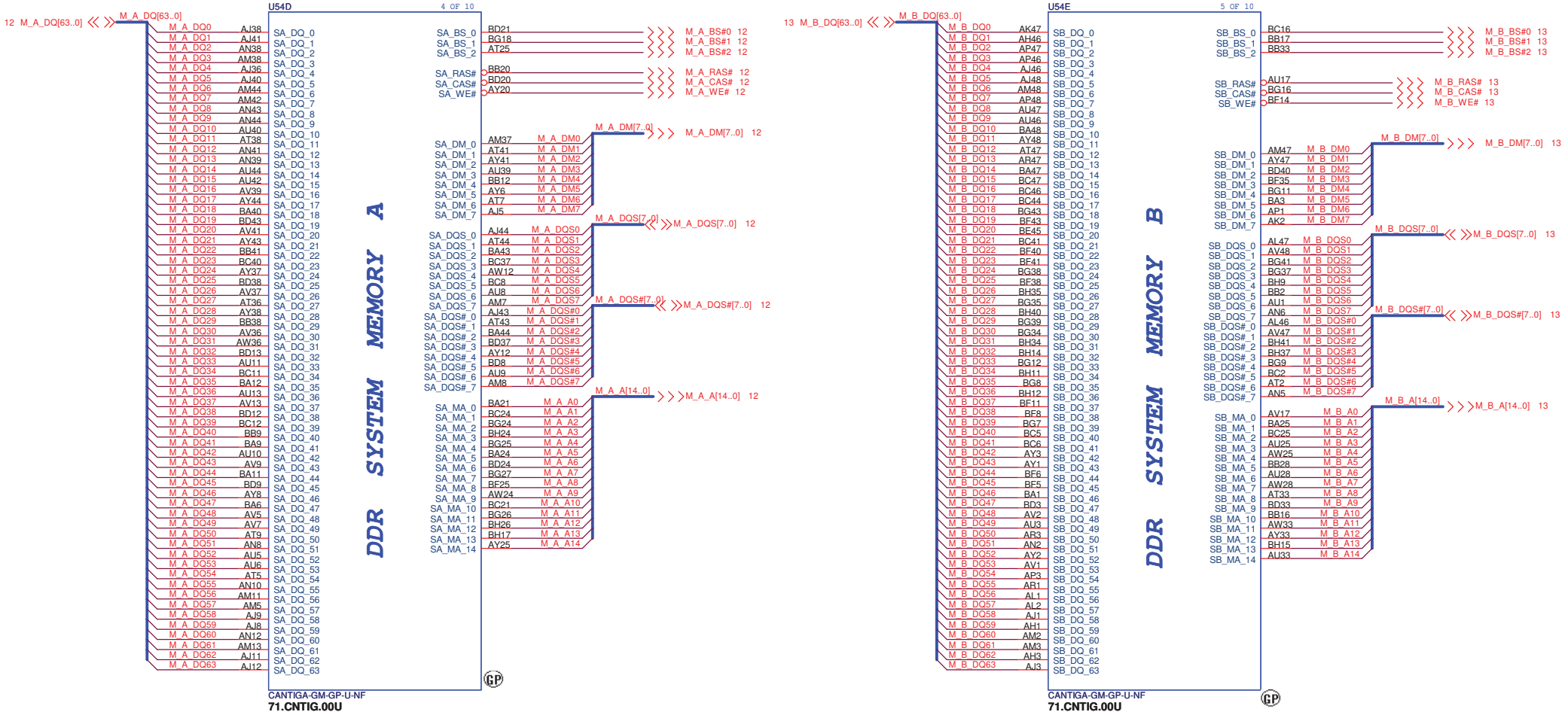
Size | Document Number: Eiger | Rev: -1

Date: Tuesday, April 01, 2008 | Sheet 6 of 50



Pin Name	Strap Description	Configuration
CFG20	Digital DisplayPort (SDVO/DP/HDMI) Concurrent with PCIE	Low = Only digital DisplayPort (SDVO/DP/HDMI) or PCIE is operational (default)
		High = Digital DisplayPort (SDVO/DP/HDMI) and PCIE are operating simultaneously via the PEG port

Wistron Corporation	Title: Cantiga (2 of 6)		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	Size:	Document Number: Elger	Rev: -1
	Date: Tuesday, April 01, 2008	Sheet 7 of 50	

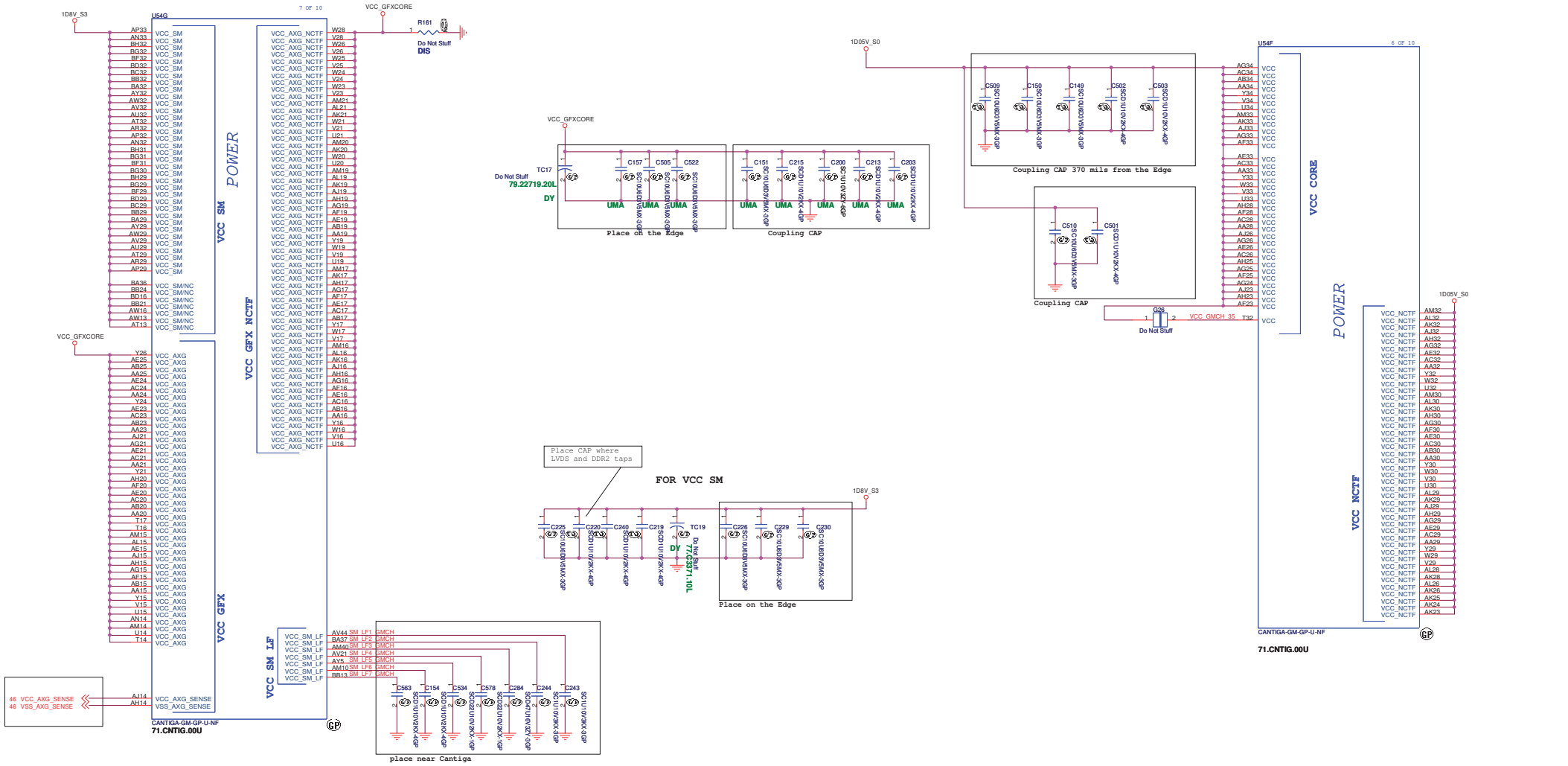


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

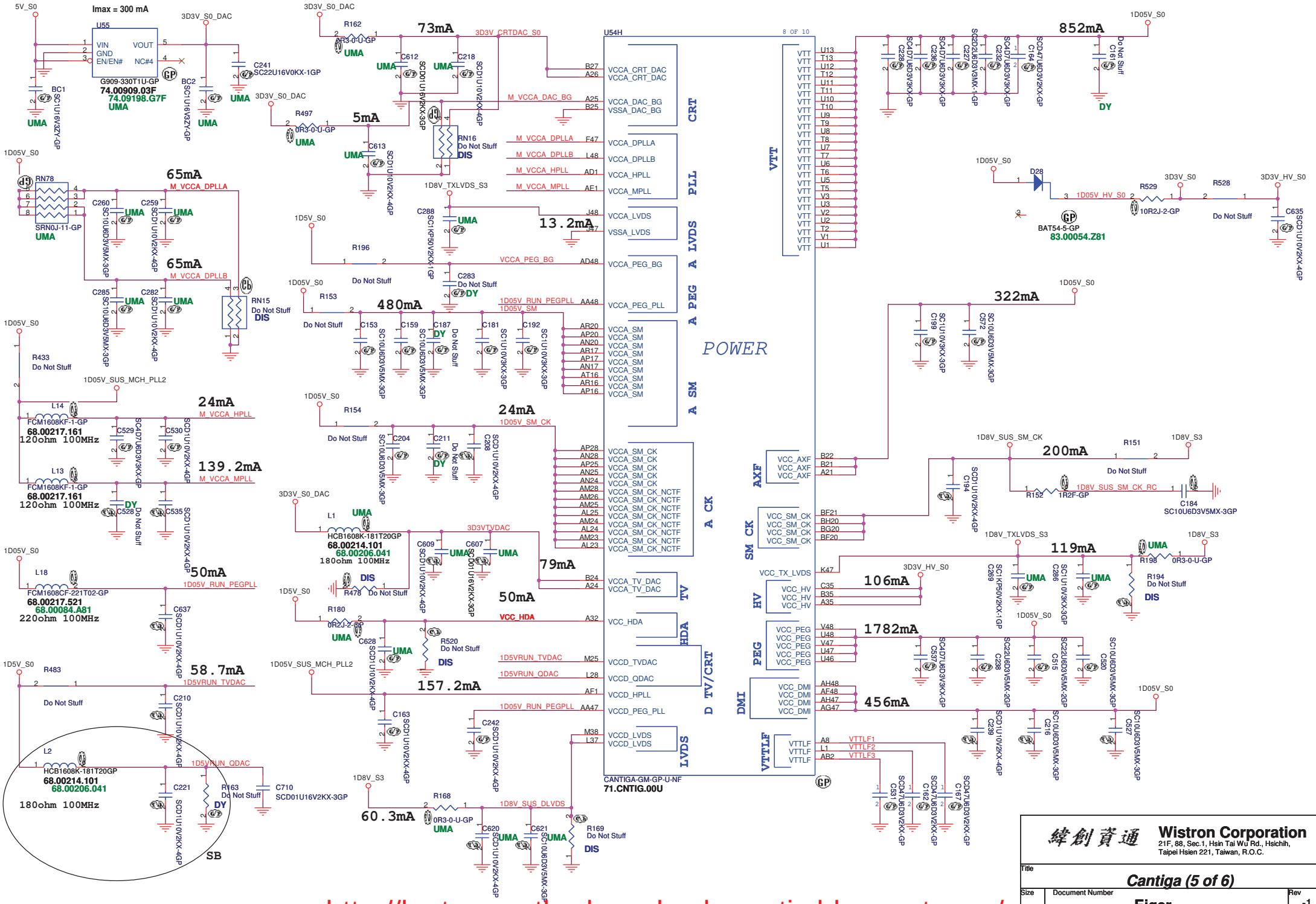
Title: Cantiga (3 of 6)

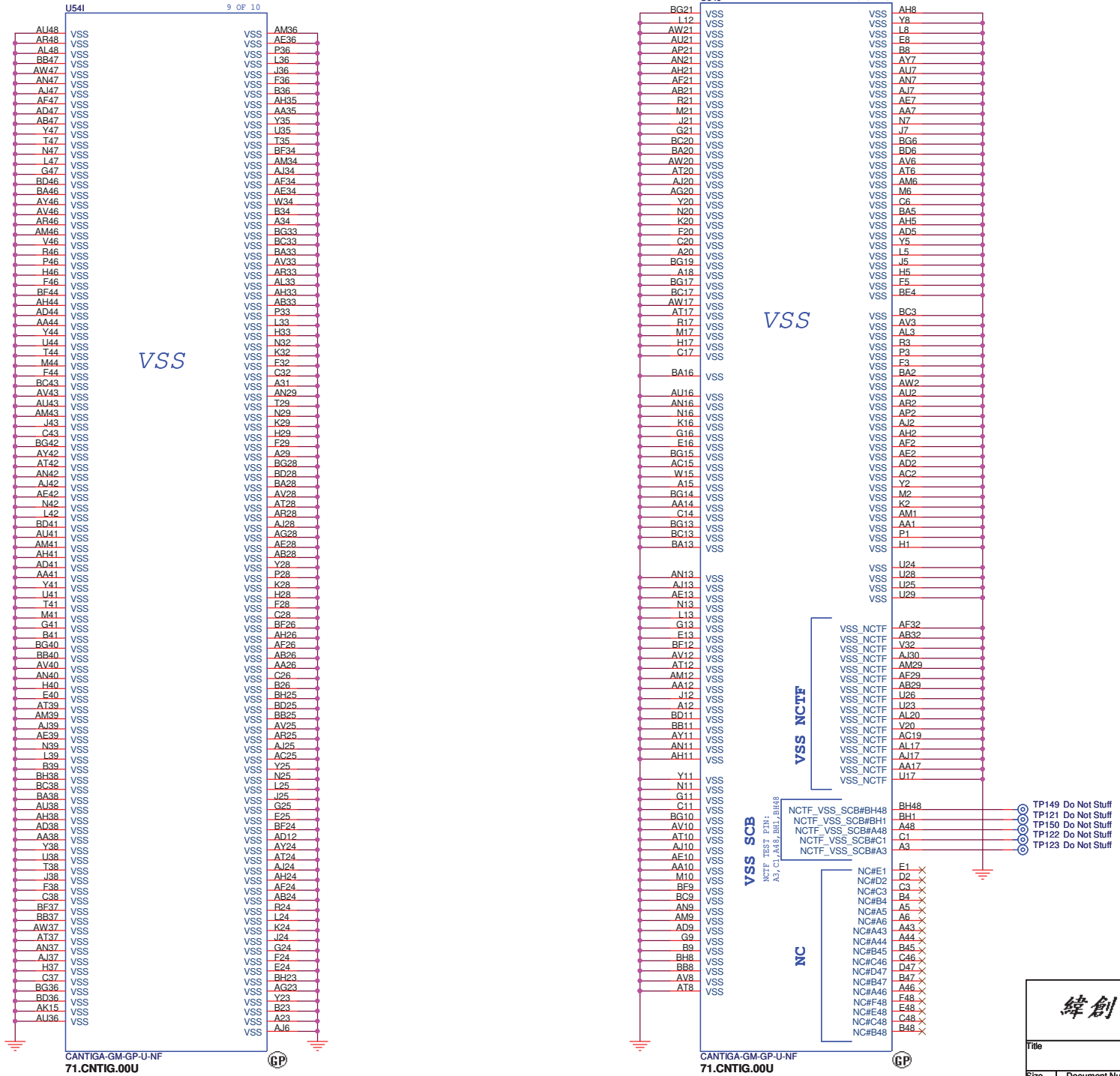
Size | Document Number: Eiger | Rev: -1

Date: Tuesday, April 01, 2008 | Sheet 8 of 50



緯創資通	Wistron Corporation	
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Cantiga (4 of 6)	
Size	Document Number	Rev
	Elger	-1
Date: Tuesday, April 01, 2008	Sheet 9 of 50	



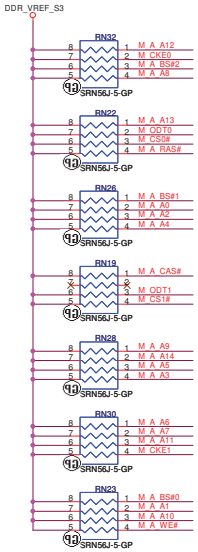


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Cantiga (6 of 6)***	
Size	Document Number: **Eiger**	Rev: -1
Date: Tuesday, April 01, 2008	Sheet 11 of 50	

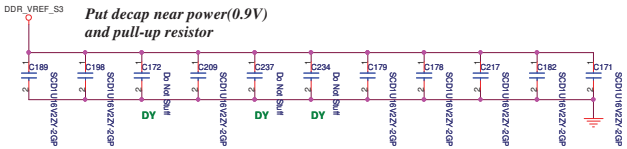
PARALLEL TERMINATION

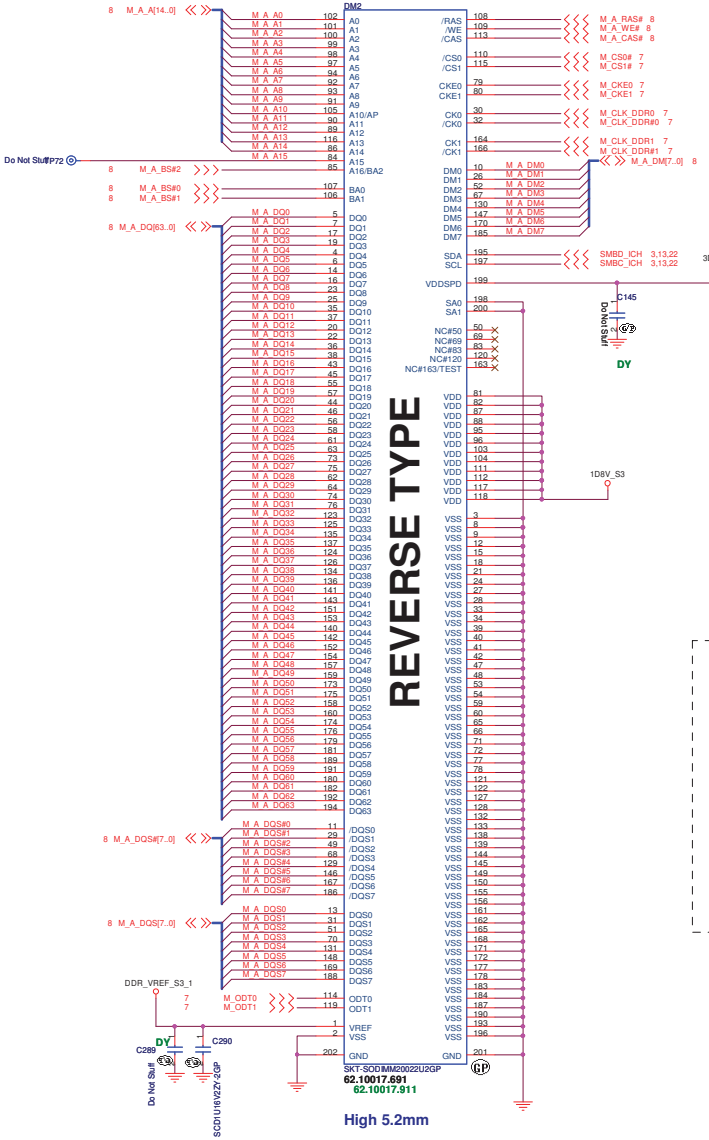
Put decap near power(0.9V) and pull-up resistor

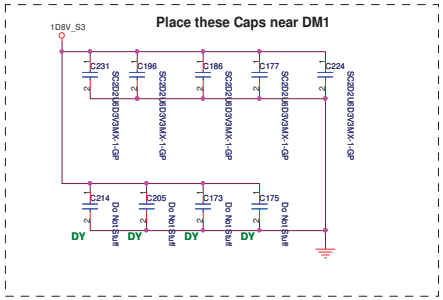


Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor



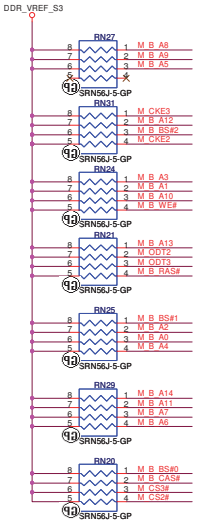




緯創資通	Wistron Corporation	
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	DDR2 Socket 0 (DM1)	
Size	Document Number	Rev
	Eiger	-1
Date: Tuesday, April 01, 2008	Sheet 12 of 50	

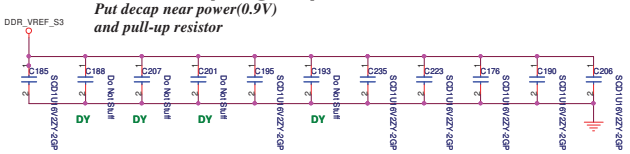
PARALLEL TERMINATION

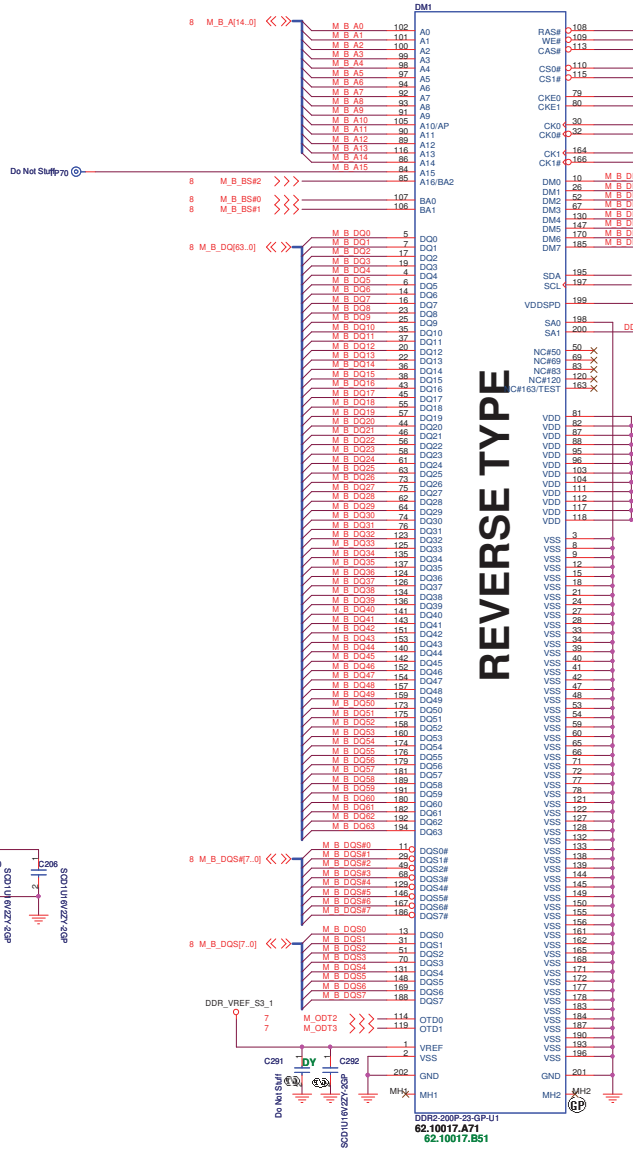
Put decap near power(0.9V) and pull-up resistor

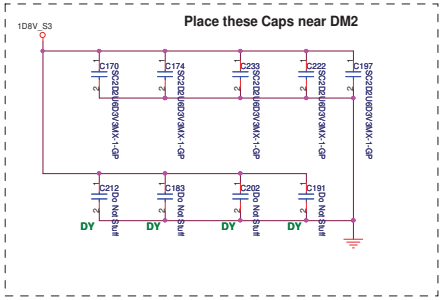


Decoupling Capacitor

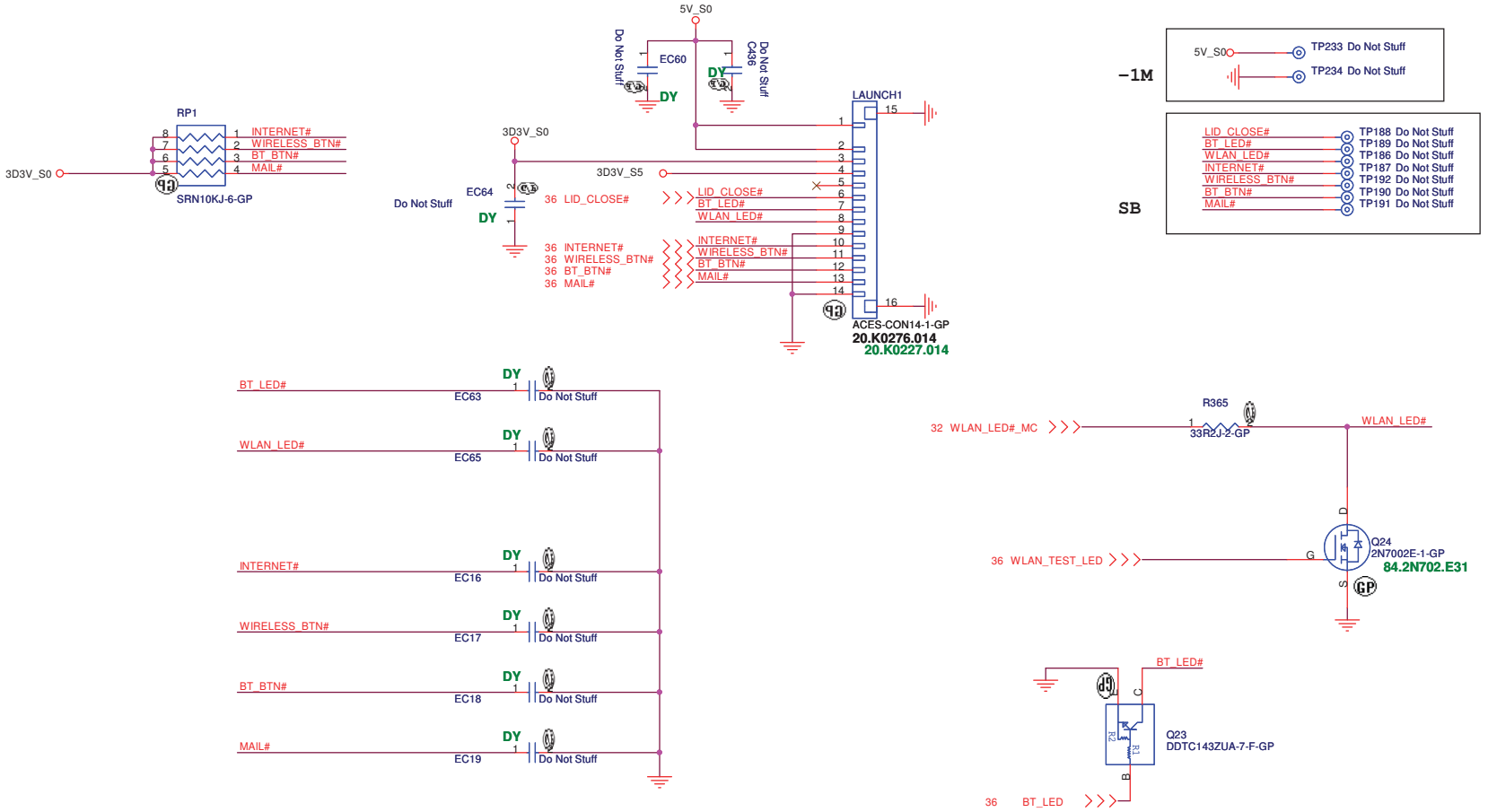
Put decap near power(0.9V) and pull-up resistor







Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: DDR2 Socket 1 (DM2)		
Size	Document Number: Eiger	Rev: -1
Date: Tuesday, April 01, 2008	Sheet 13 of 50	



UMA

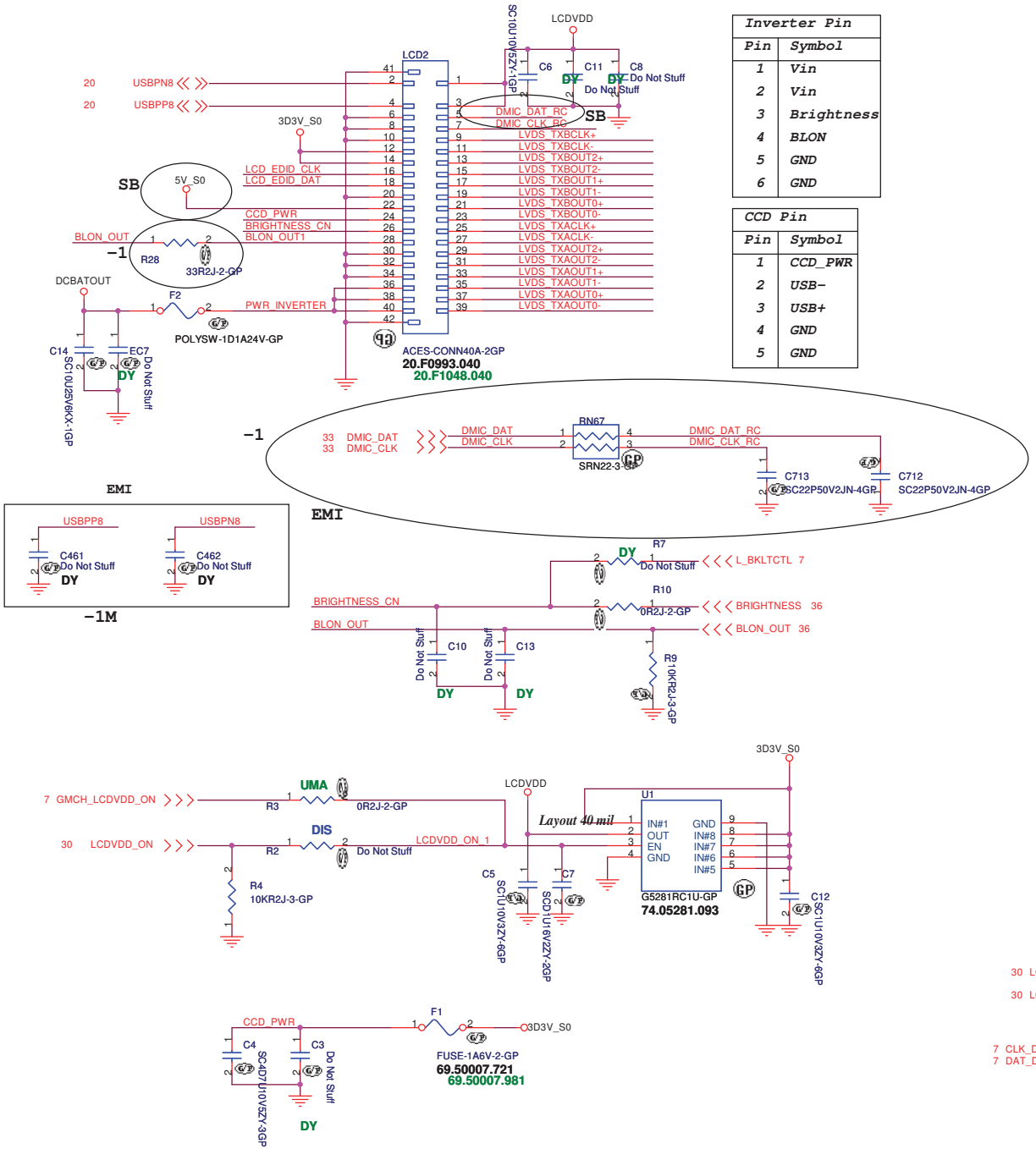
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAUNCH**

Size | Document Number: **Eiger** | Rev: -1

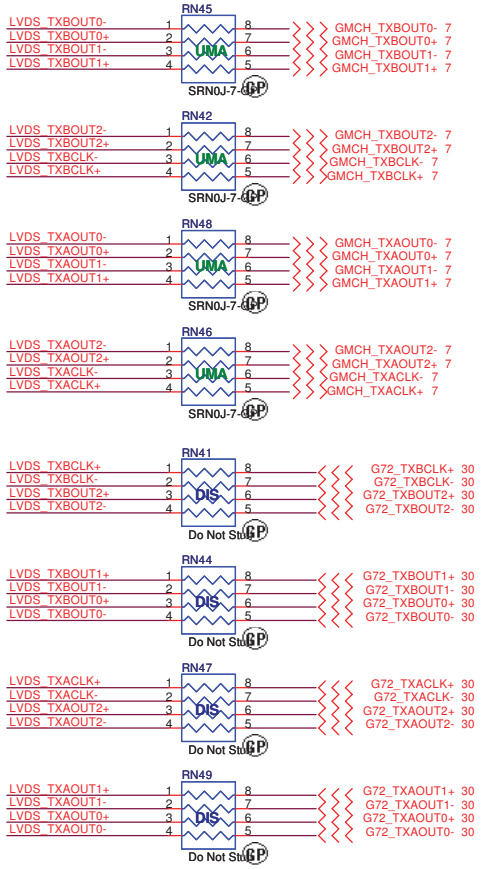
Date: Tuesday, April 01, 2008 | Sheet 14 of 50

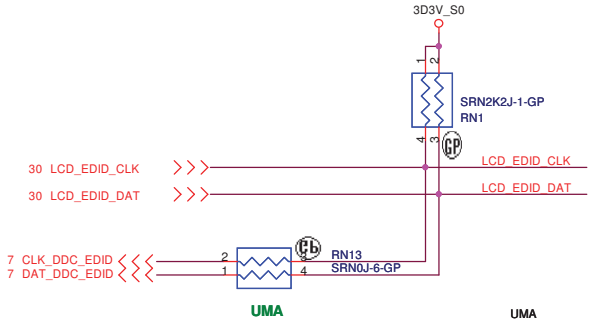
LCD/INVERTER/CCD CONN



Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND





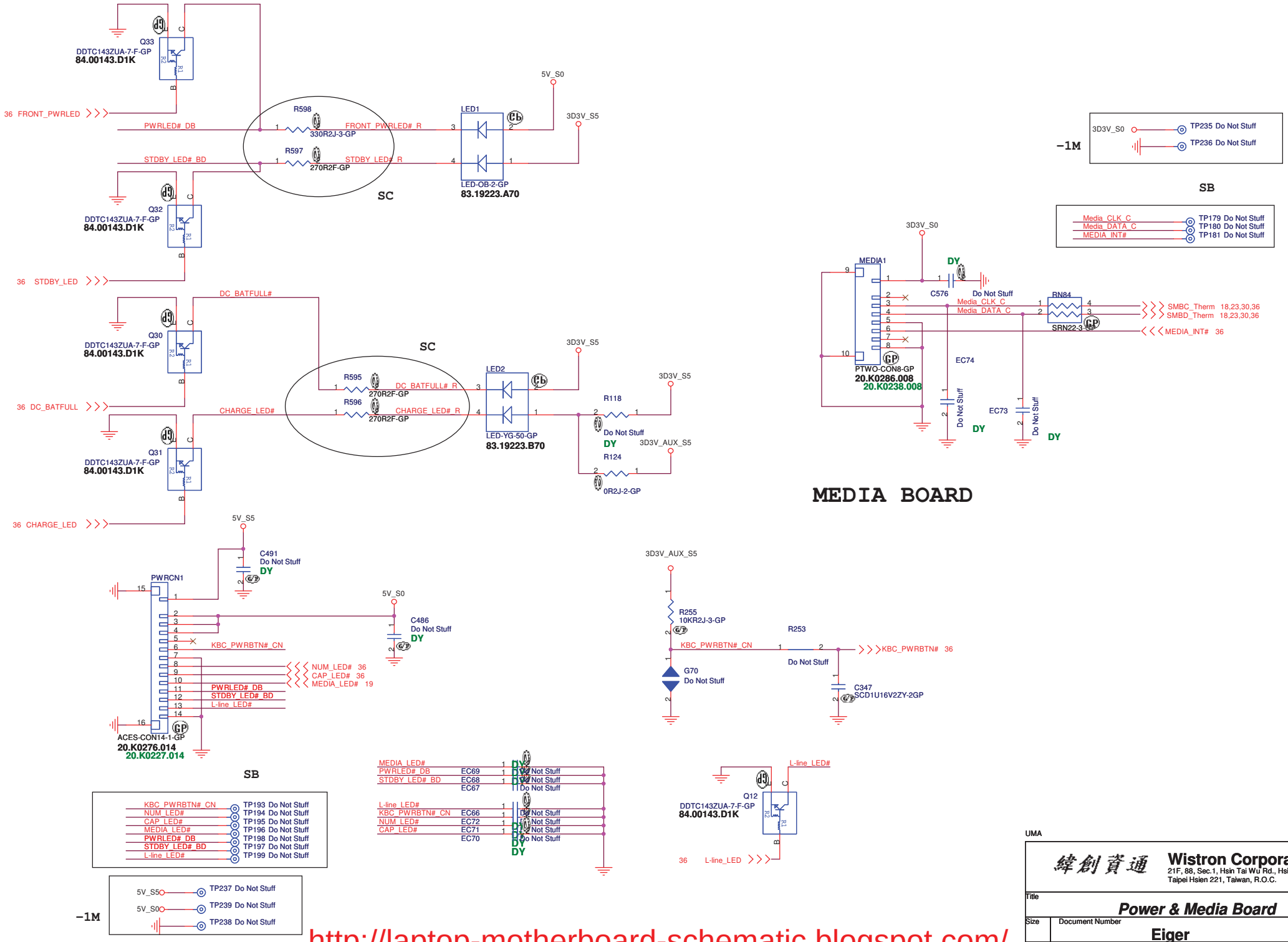
UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN

Size | Document Number: Eiger | Rev: -1

Date: Tuesday, April 01, 2008 | Sheet 15 of 50



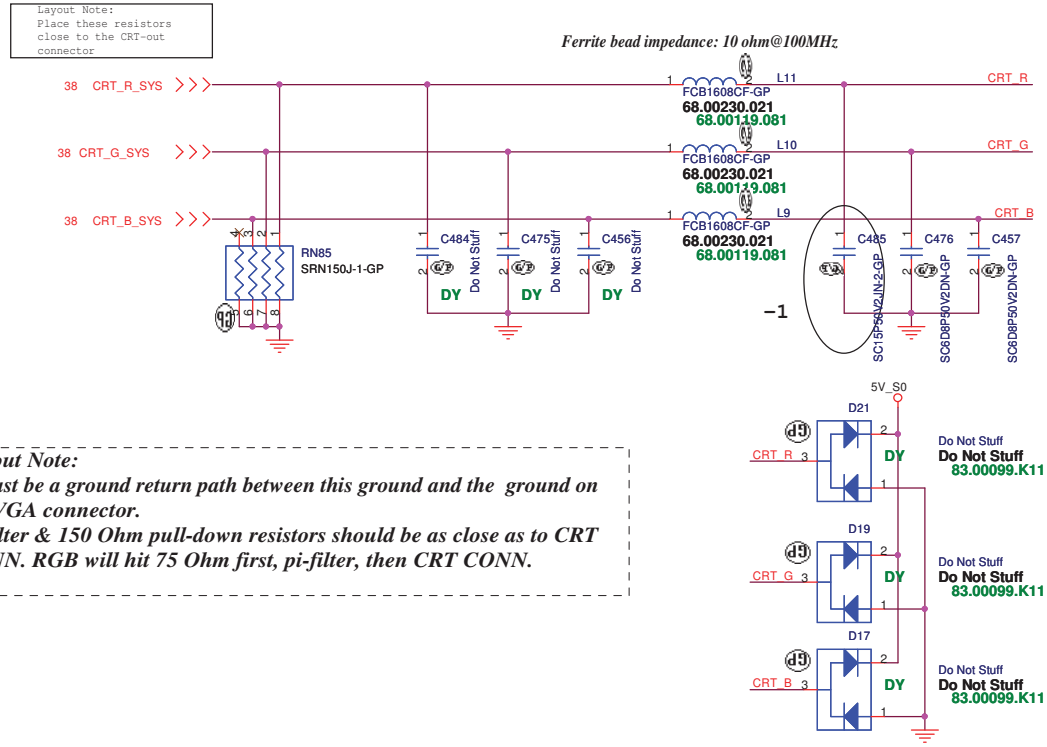
UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power & Media Board**

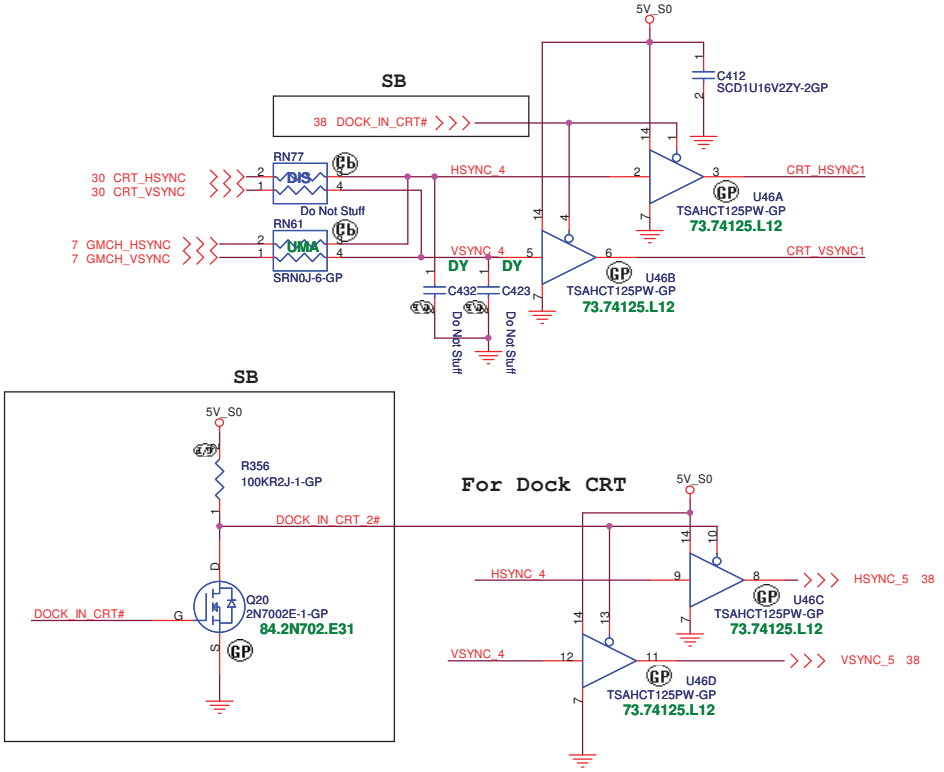
Size	Document Number	Rev
	Eiger	-1

Date: Tuesday, April 01, 2008 Sheet 16 of 50

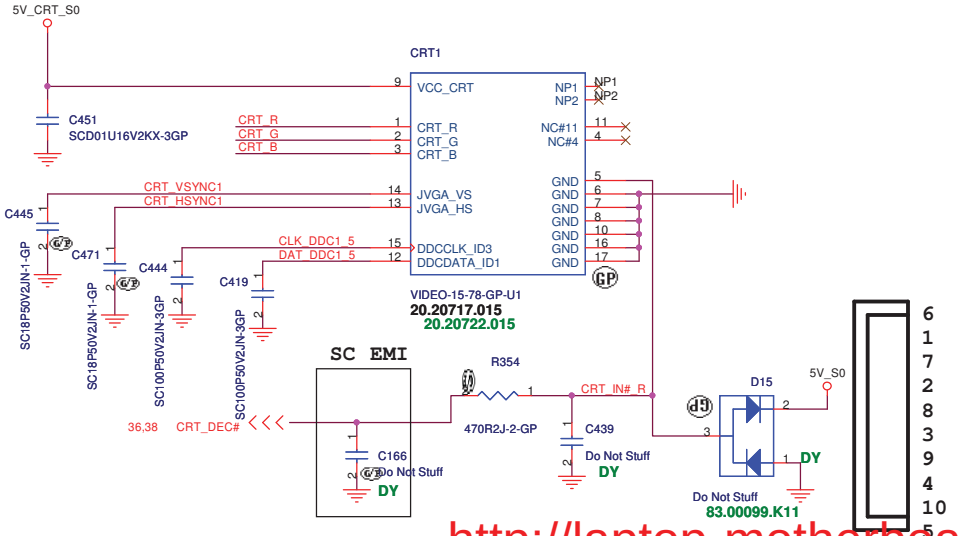


Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

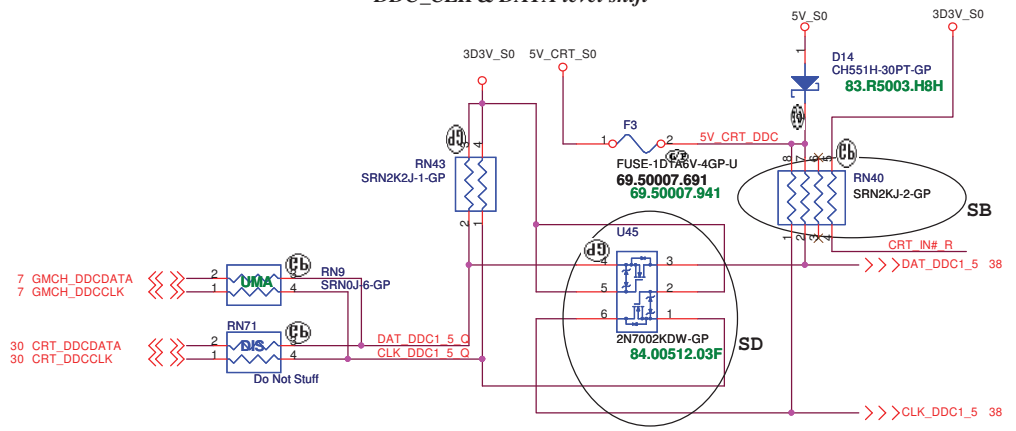
Hsync & Vsync level shift



CRT I/F & CONNECTOR



DDC_CLK & DATA level shift

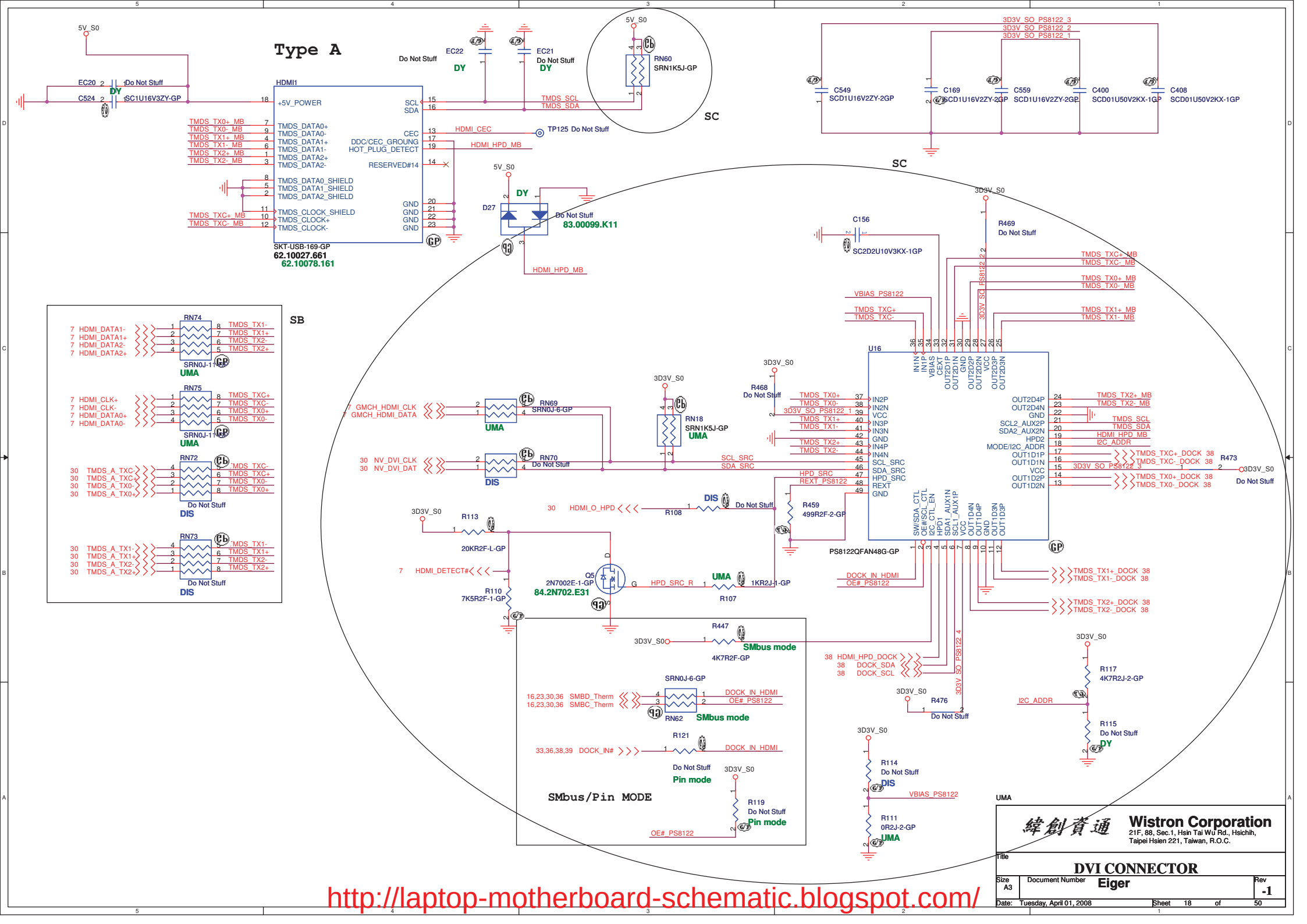


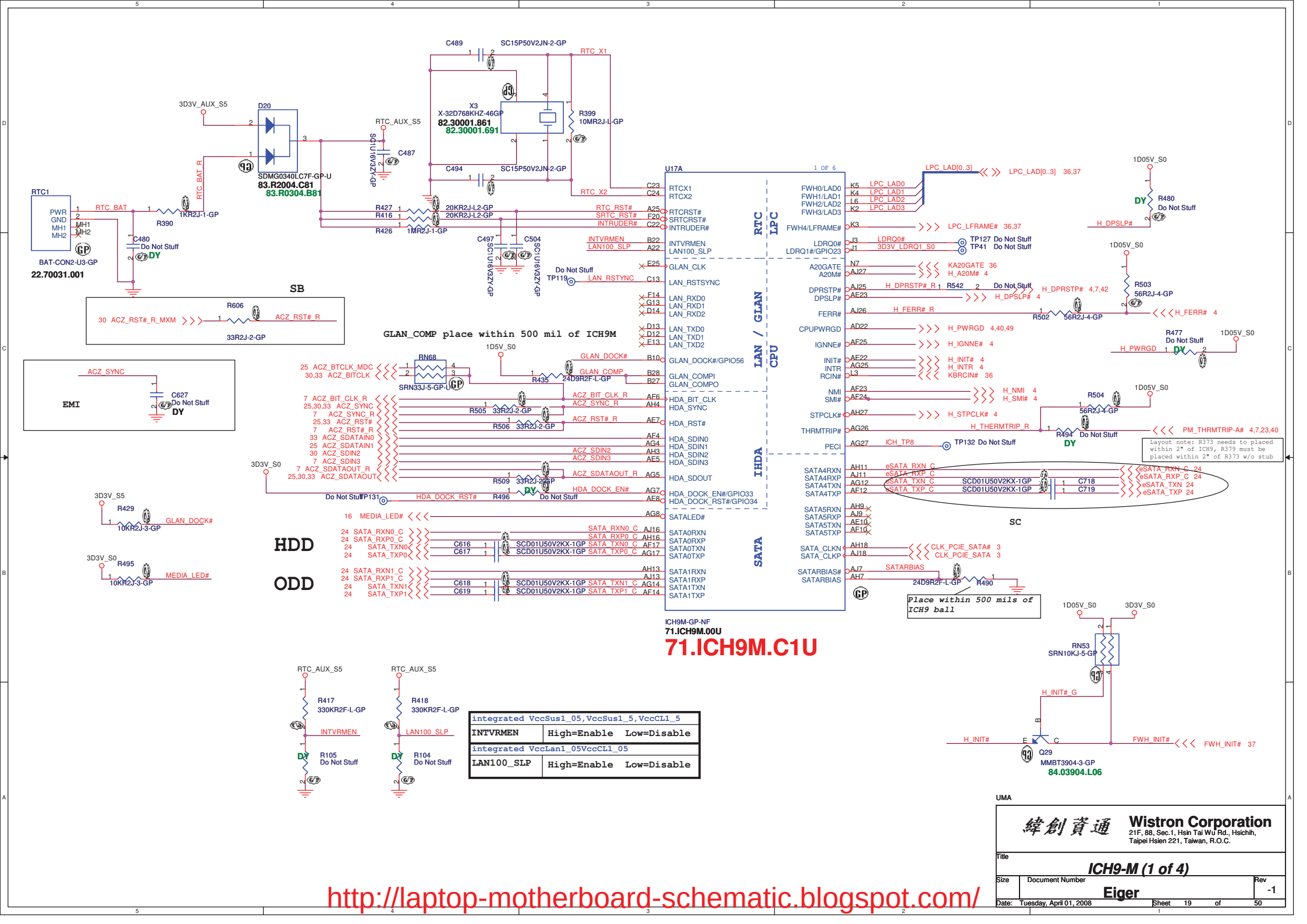
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT Connector**

Size | Document Number: Eiger | Rev: -1

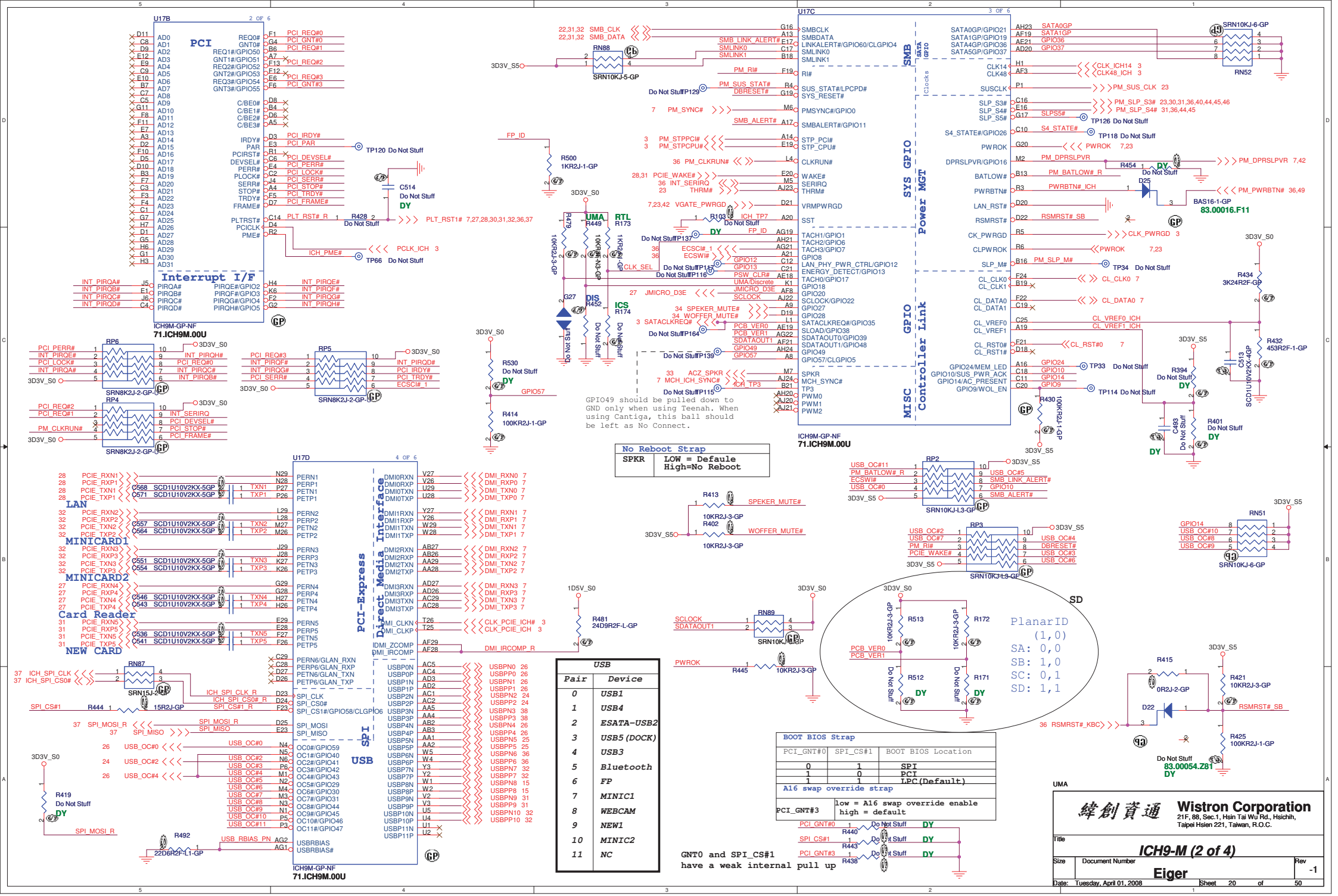
Date: Tuesday, April 01, 2008 | Sheet 17 of 50

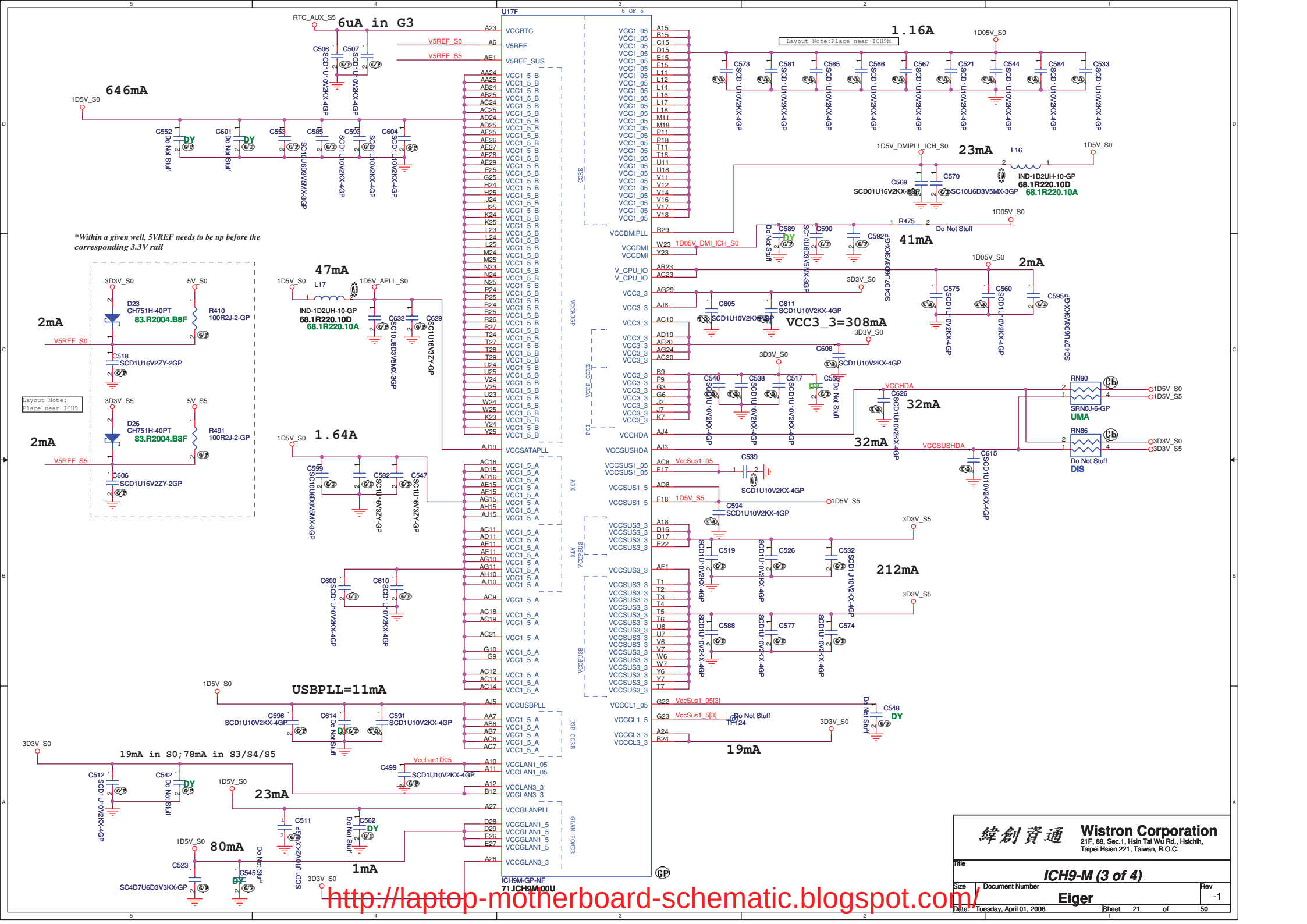

Type A
SC
SB
UMA
DIS
SMbus/Pin MODE
HDMI1
SKT-USB-169-GP
62.10027.661
62.10078.161
U16
PS8122QFAN48G-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DVI CONNECTOR
Eiger
Size A3
Rev -1
Date: Tuesday, April 01, 2008
Sheet 18 of 50
http://laptop-motherboard-schematic.blogspot.com/

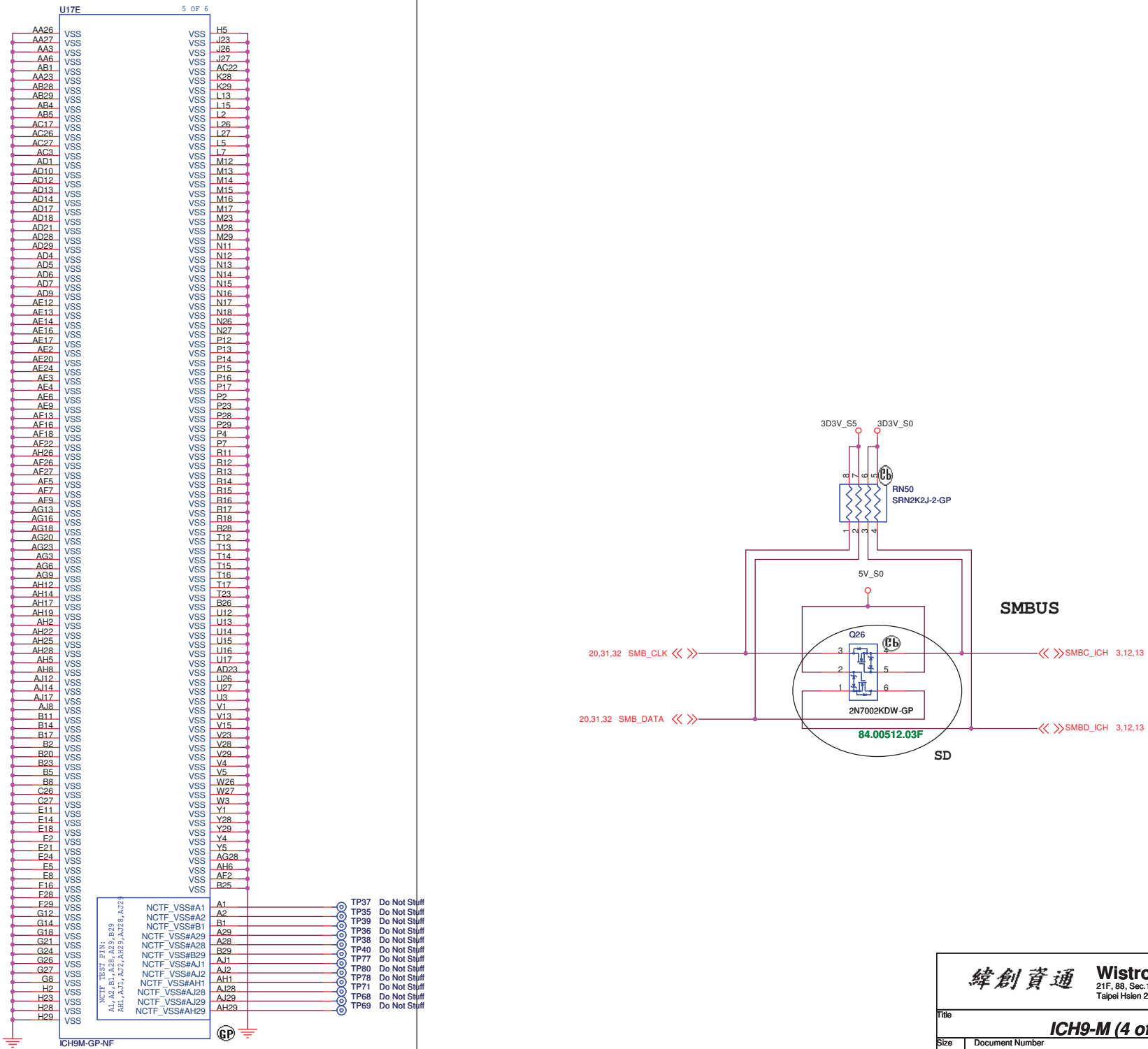


UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***ICH9-M (1 of 4)***
Size	Document Number: **Eiger** — Rev: -1
Date: Tuesday, April 01, 2008	Sheet 19 of 50




U17F
6 OF 6
ICH9M-GP-NF
71.ICH9M.00U
6uA in G3
646mA
1.16A
23mA
41mA
2mA
47mA
1.64A
VCC3_3=308mA
32mA
212mA
USBPLL=11mA
19mA in S0;78mA in S3/S4/S5
80mA
1mA
19mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note:Place near ICH9M
Layout Note: Place near ICH9
Do Not Stuff
UMA
DIS
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ICH9-M (3 of 4)
Eiger
Tuesday, April 01, 2008
http://laptop-motherboard-schematic.blogspot.com/

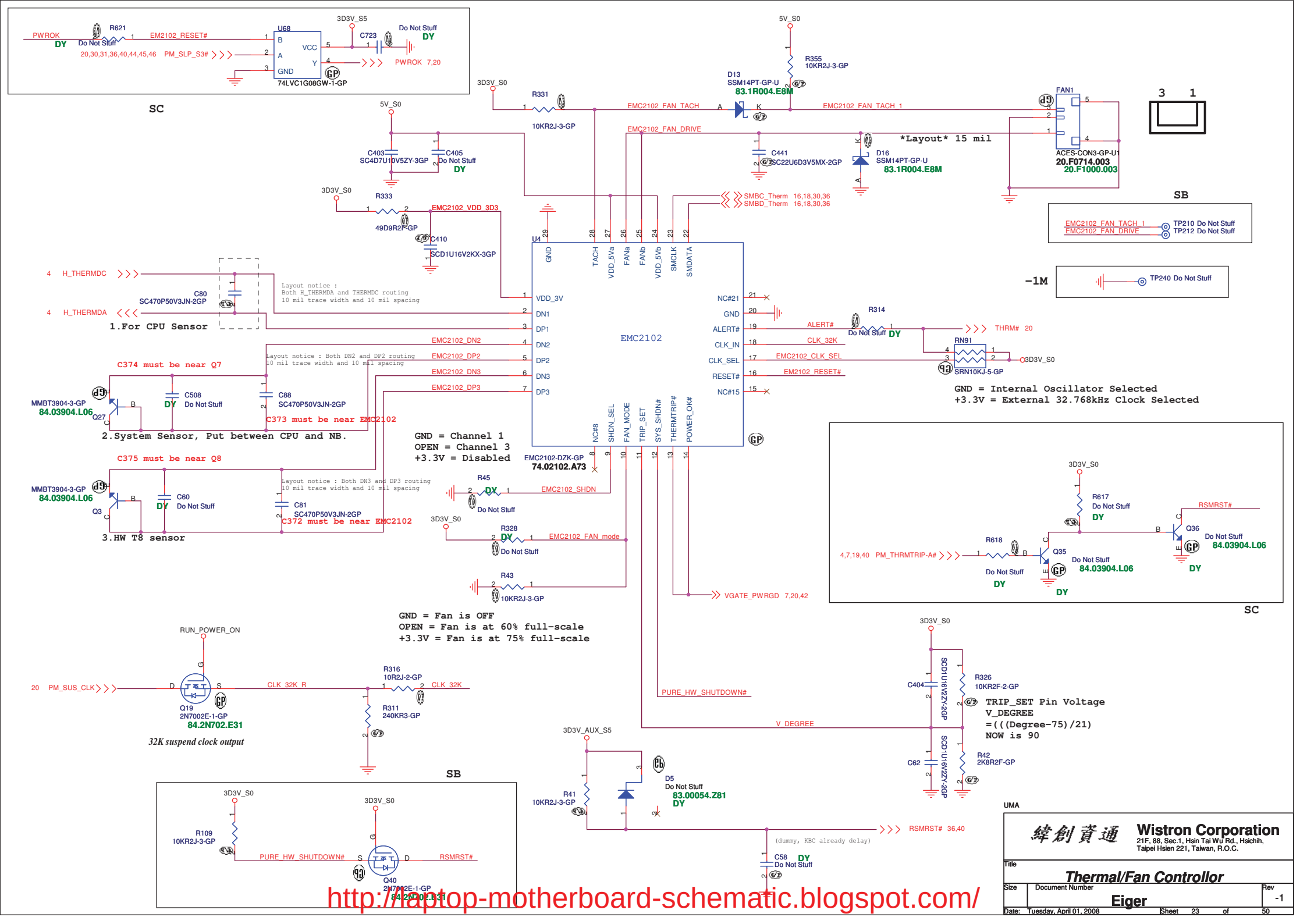


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

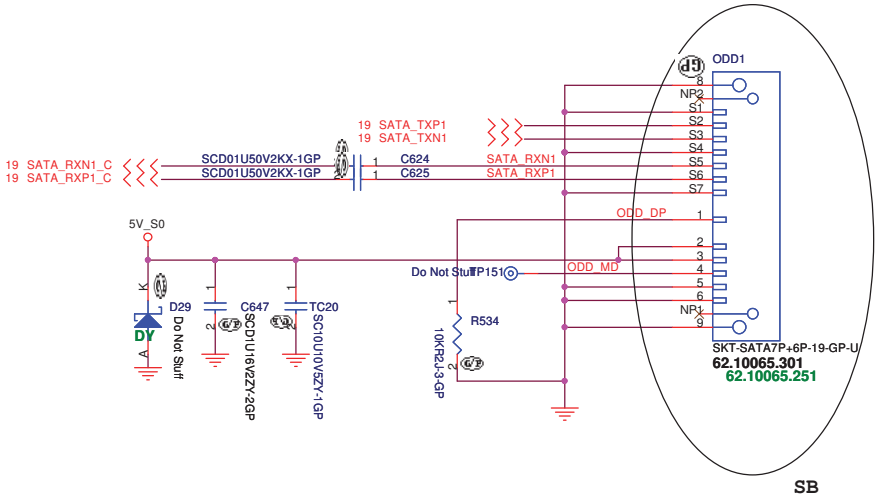
Title: ***ICH9-M (4 of 4)***

Size	Document Number	Rev
	Eiger	-1

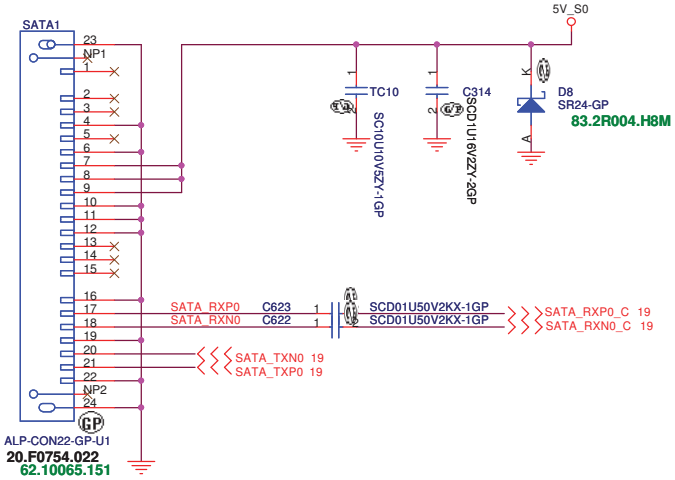
Date: Tuesday, April 01, 2008 Sheet 22 of 50



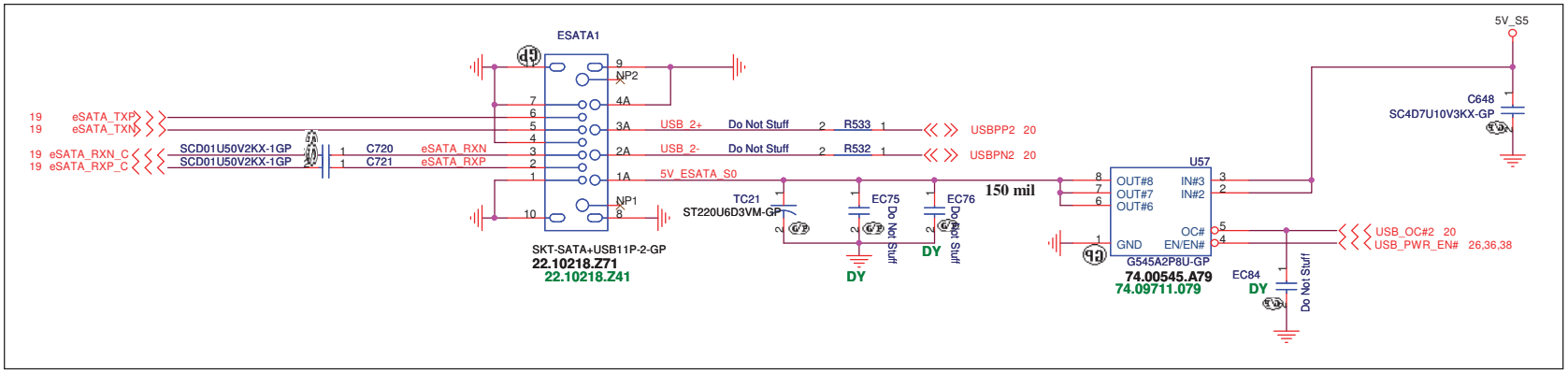
SATA ODD Connector



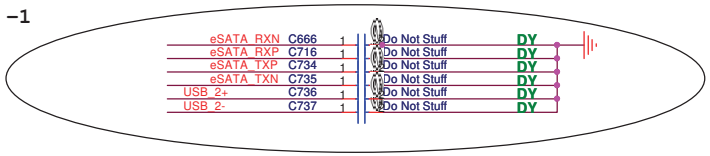
SATA Connector



SC



-1



EMI

UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

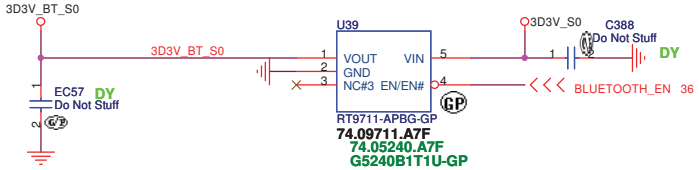
Title: HDD & CDROM & ESATA

Size | Document Number: Eiger | Rev: -1

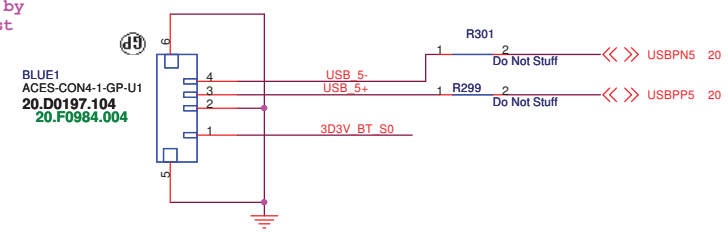
Date: Tuesday, April 01, 2008 | Sheet 24 of 50

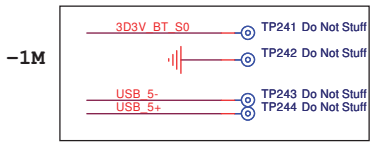
BLUETOOTH MODULE

1.5A / High Active Voltage 2V

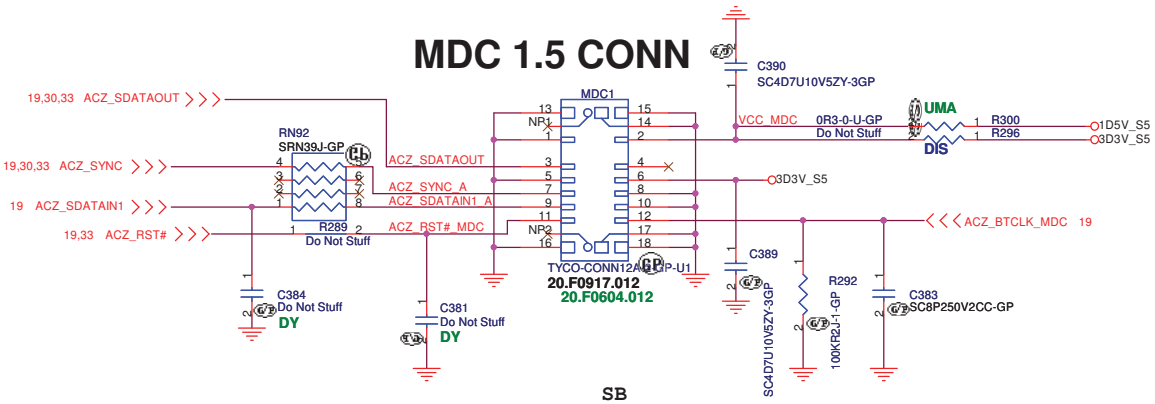


EC21 put near BLUE1 / all USB put one choke near connector by EMI request

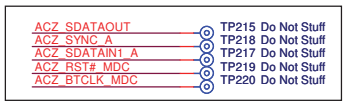


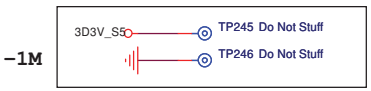


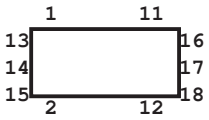
MDC 1.5 CONN



SB







Finger printer

MOVE TO Page 36

UMA

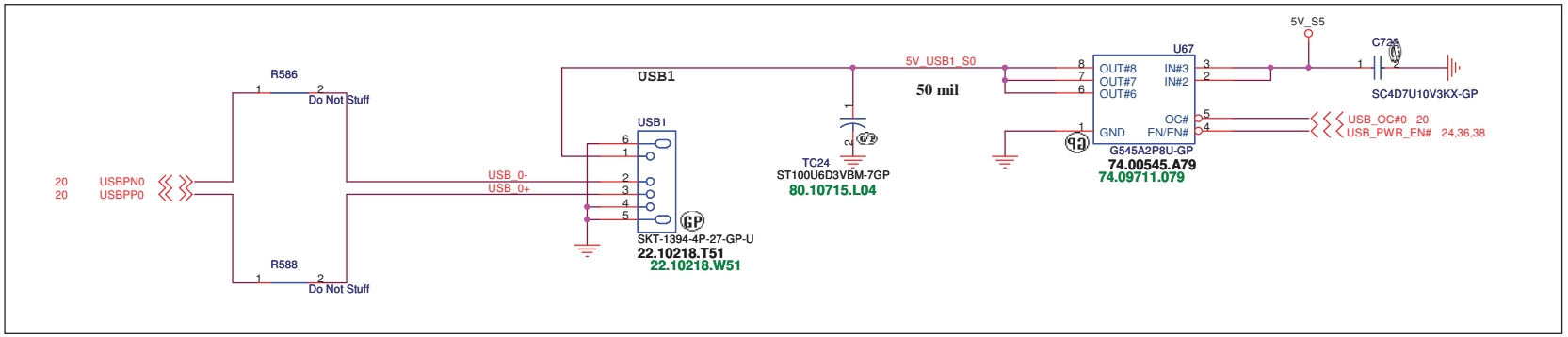
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

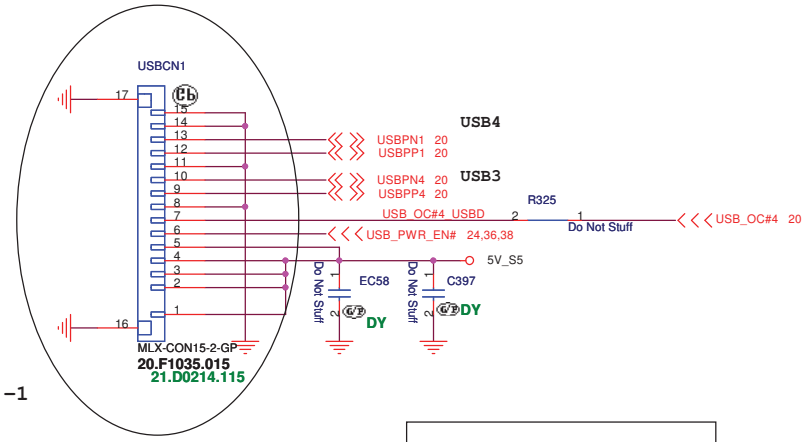
Title: BLUETOOTH MDC Finger printer

Size | Document Number: Eiger | Rev: -1

Date: Tuesday, April 01, 2008 | Sheet 25 of 50

SC

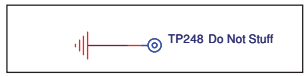




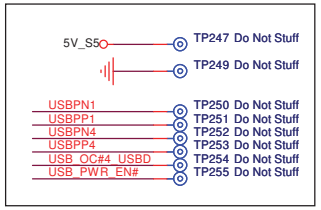
-1

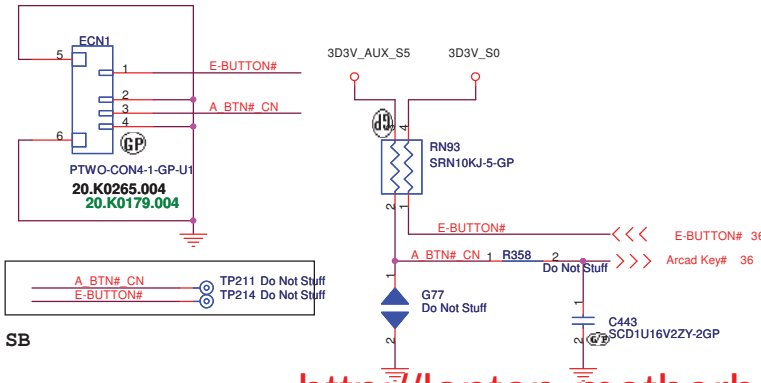
ECN BOARD

-1M



-1M





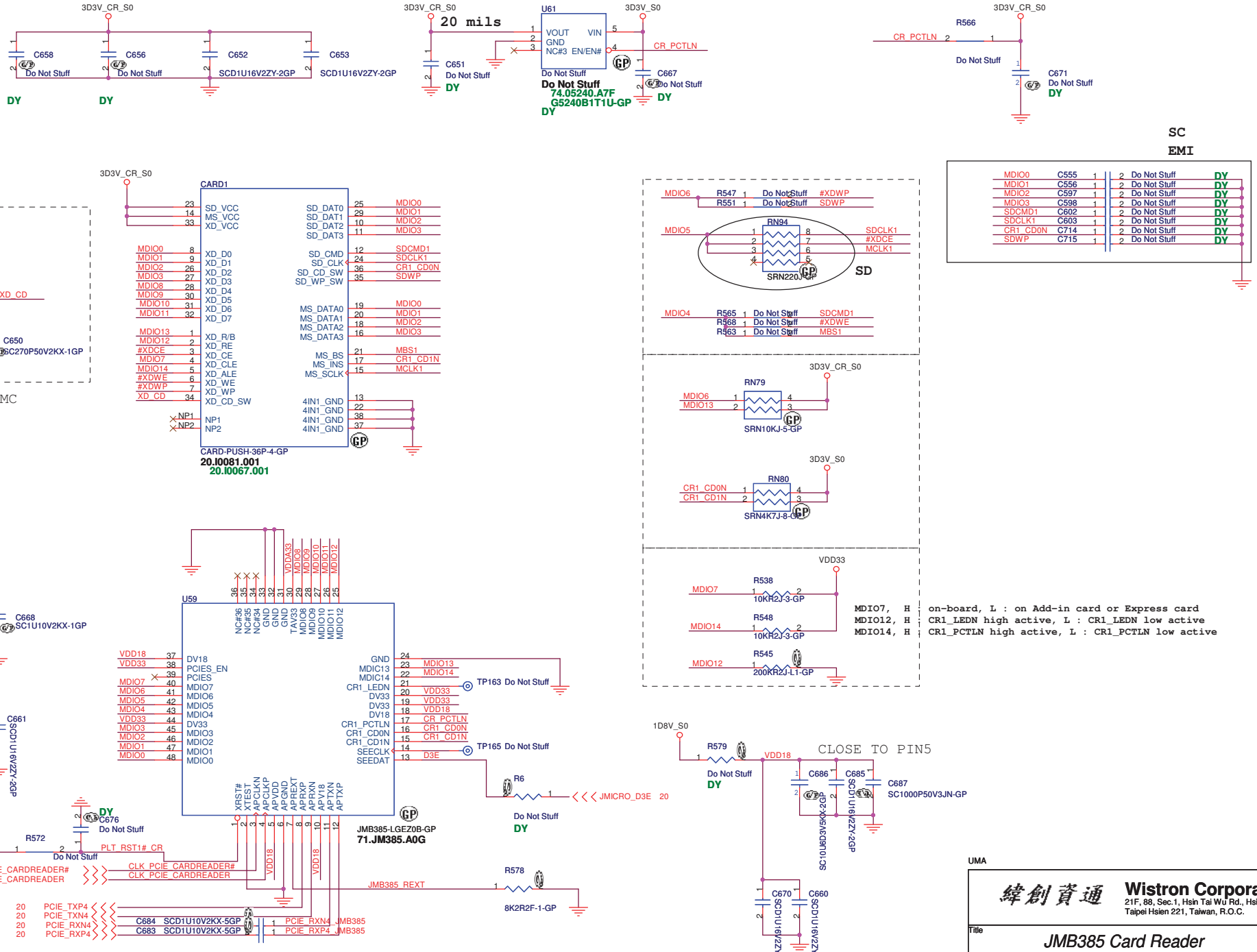
UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB & ECN	
Size	Document Number: Eiger	Rev: -1
Date: Tuesday, April 01, 2008	Sheet 26 of 50	

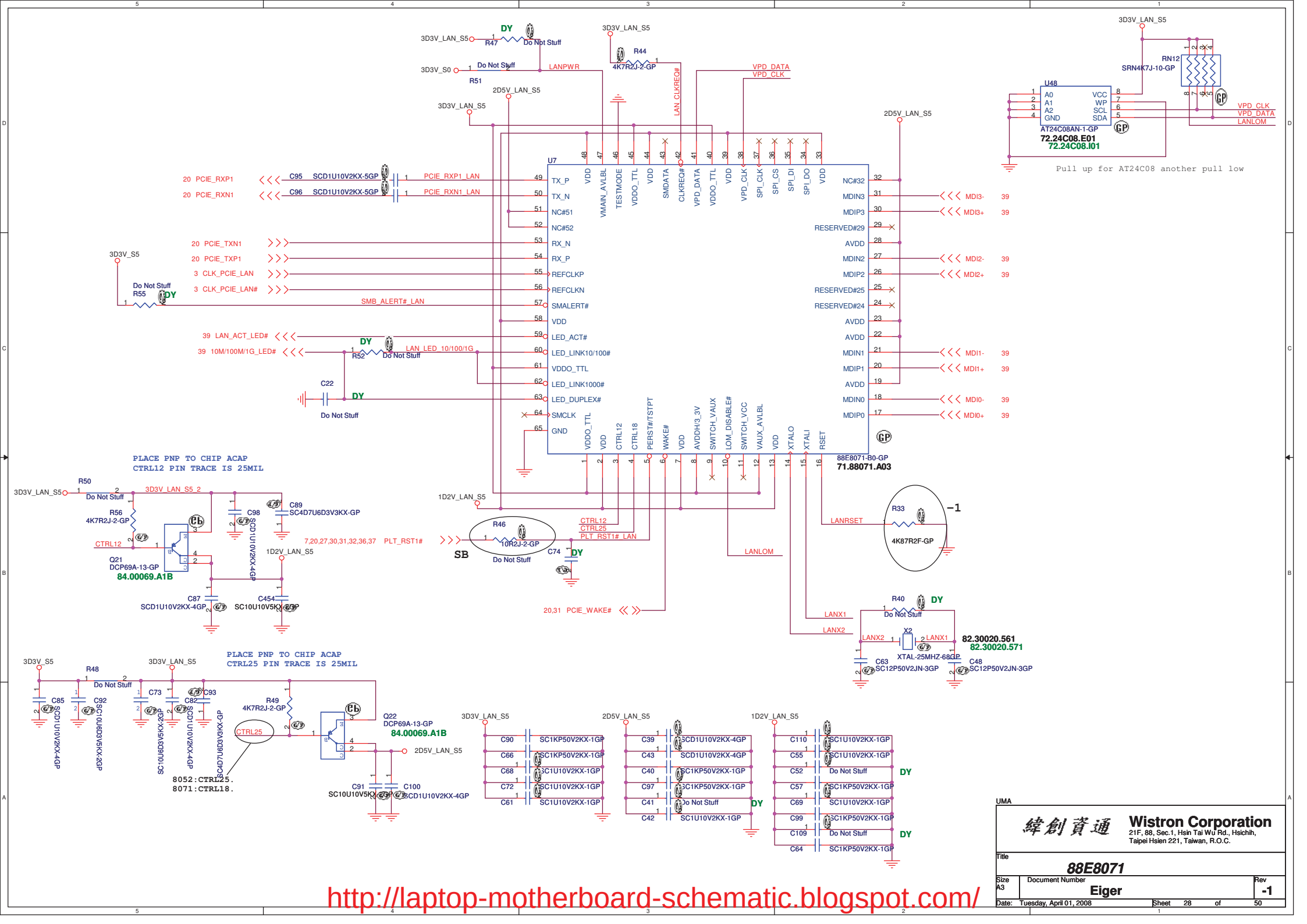
5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)

1.5A / High Active Voltage 2V



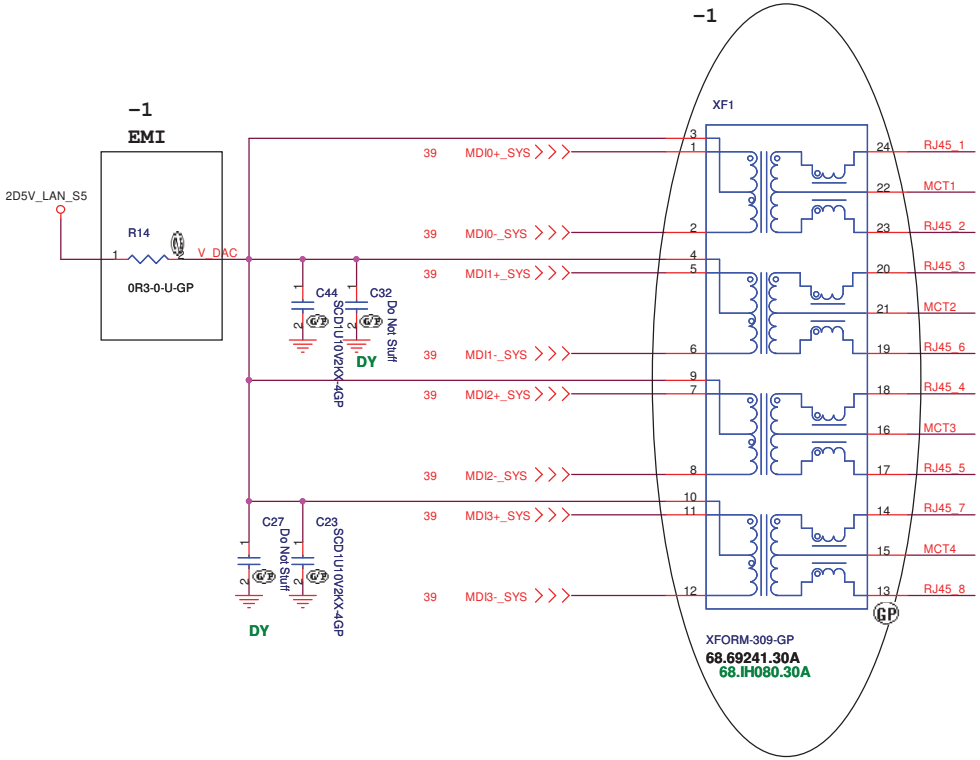
UMA

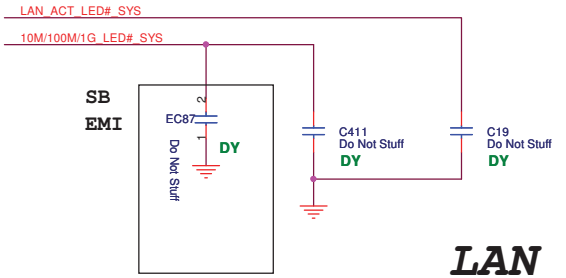
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*JMB385 Card Reader*	
Size	Document Number: Eiger	Rev: -1
Date: Tuesday, April 01, 2008	Sheet 27 of 50	



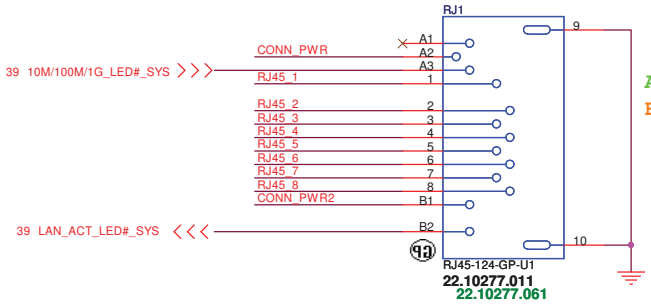
LAN Connector

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.





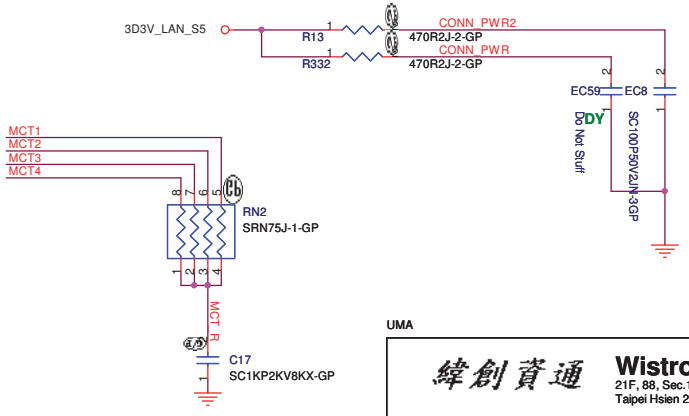
LAN Connector



LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transfering data.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers



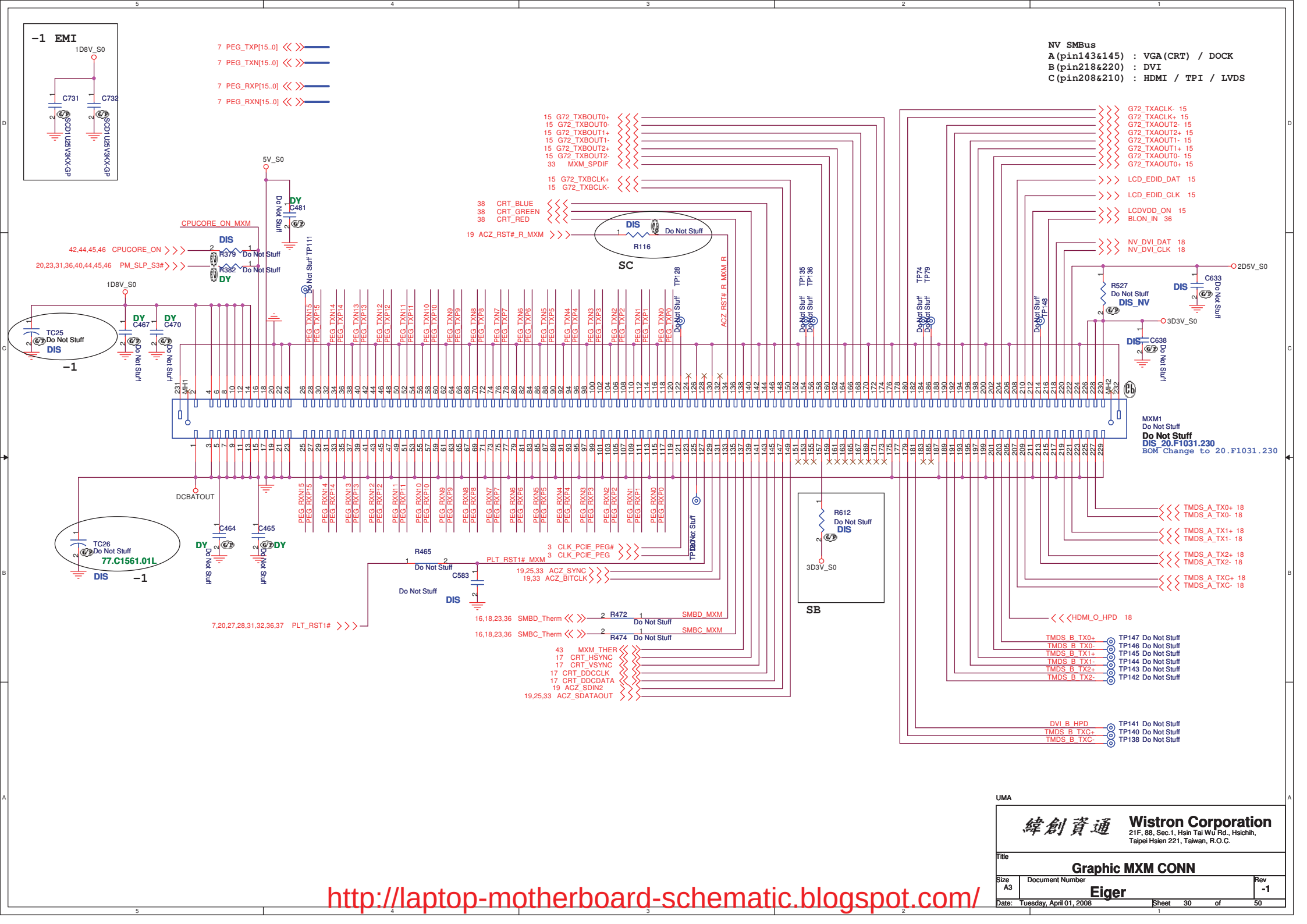
UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN CONN

Size	Document Number	Rev
A3		-1

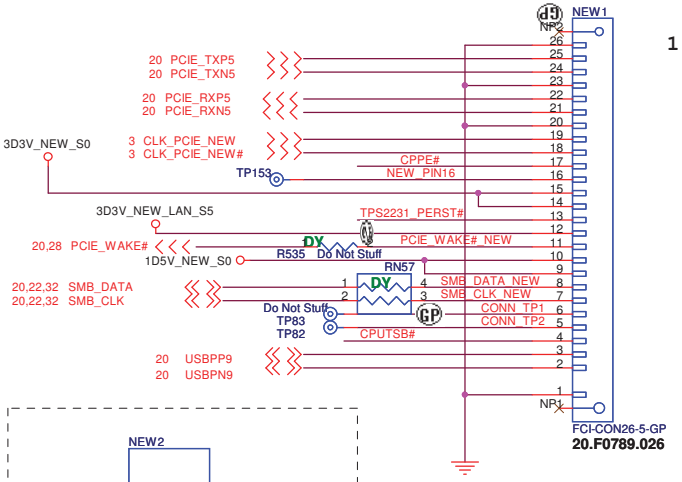
Date: Tuesday, April 01, 2008 Sheet 29 of 50

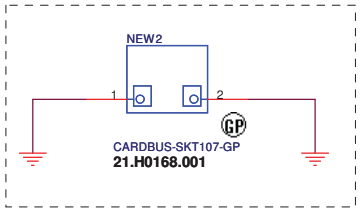


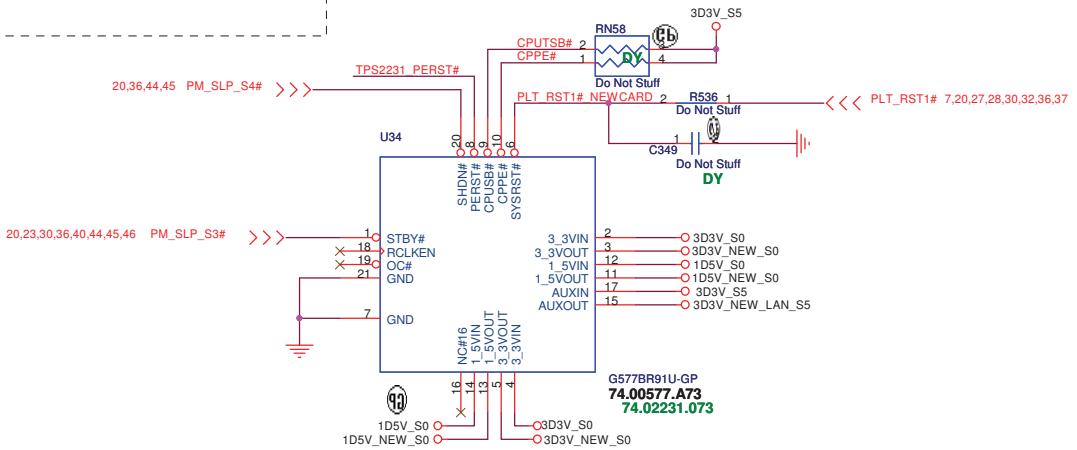
NEWCARD Connector

Reserve the symbol
for bottom side
connector

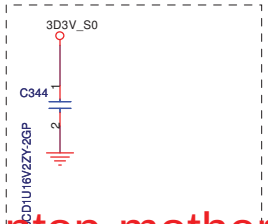
TOP VIEW



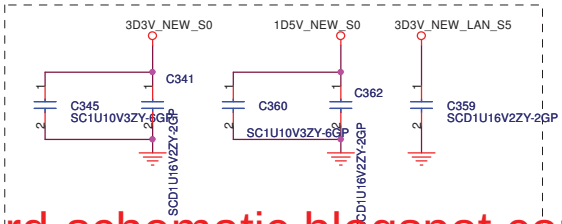




Place them Near to Chip



Place them Near to Connector



UMA

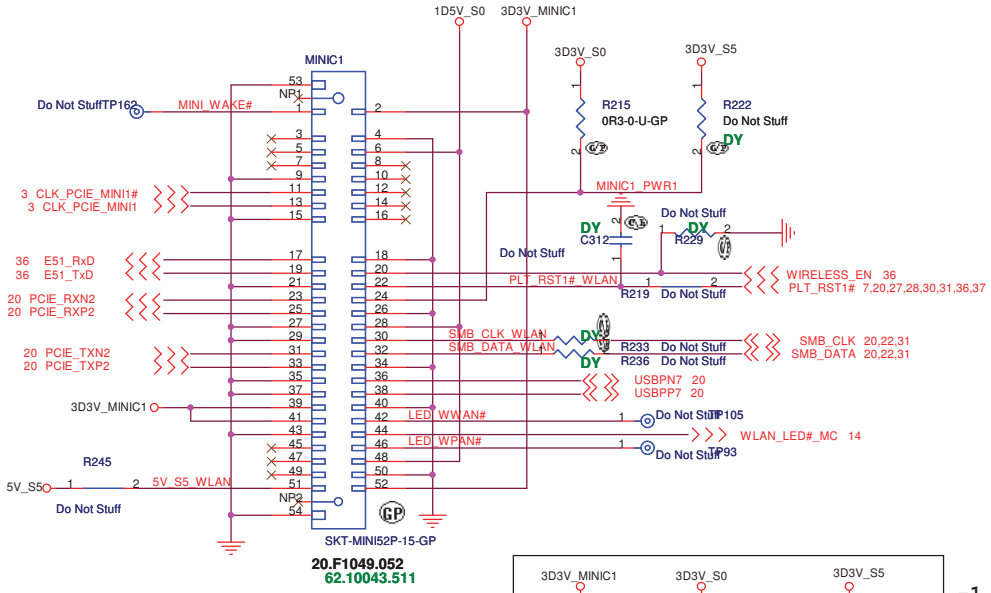
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NEW CARD

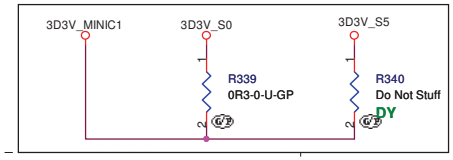
Size | Document Number: Eiger | Rev: -1

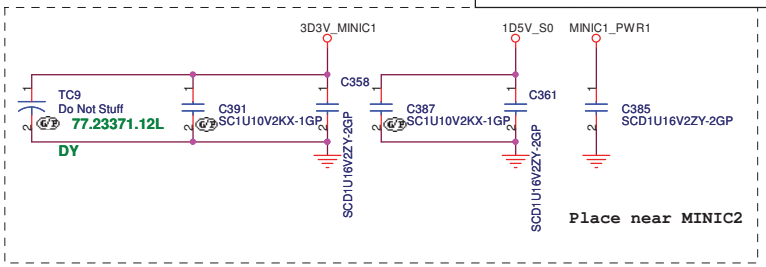
Date: Tuesday, April 01, 2008 | Sheet 31 of 50

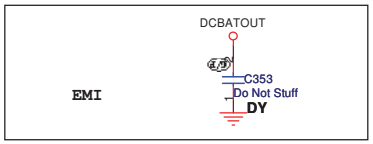
Mini Card Connector(WLAN)



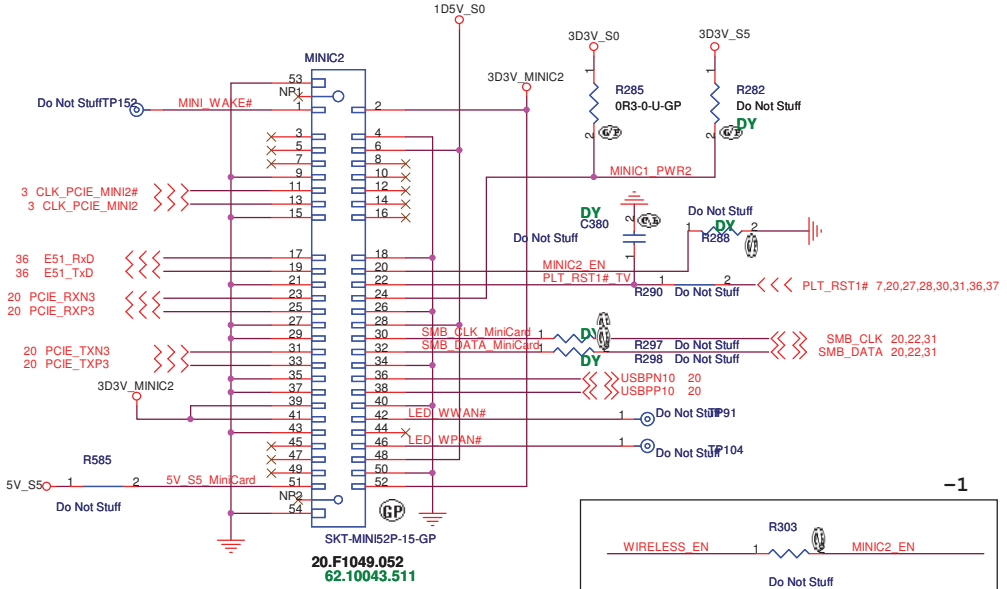
20.F1049.052
62.10043.511



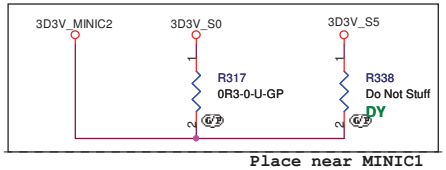


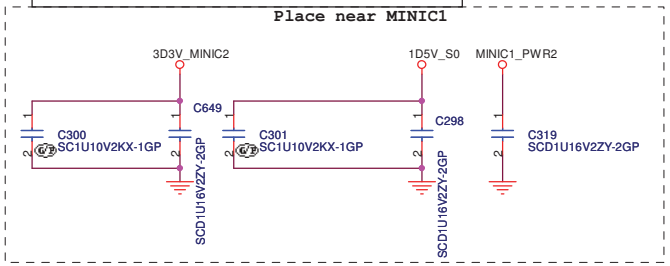


Mini Card Connector(TV)



20.F1049.052
62.10043.511





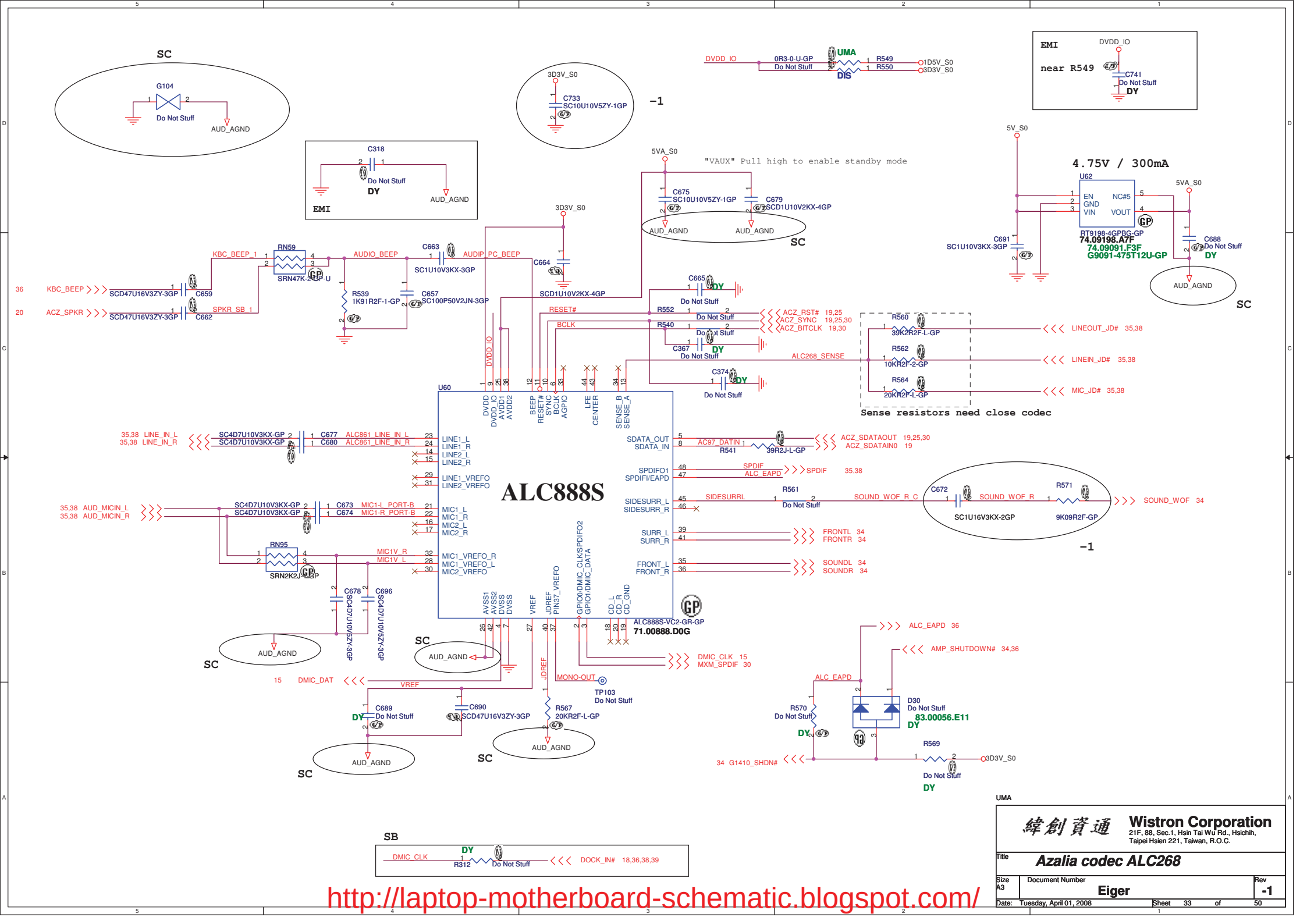
UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

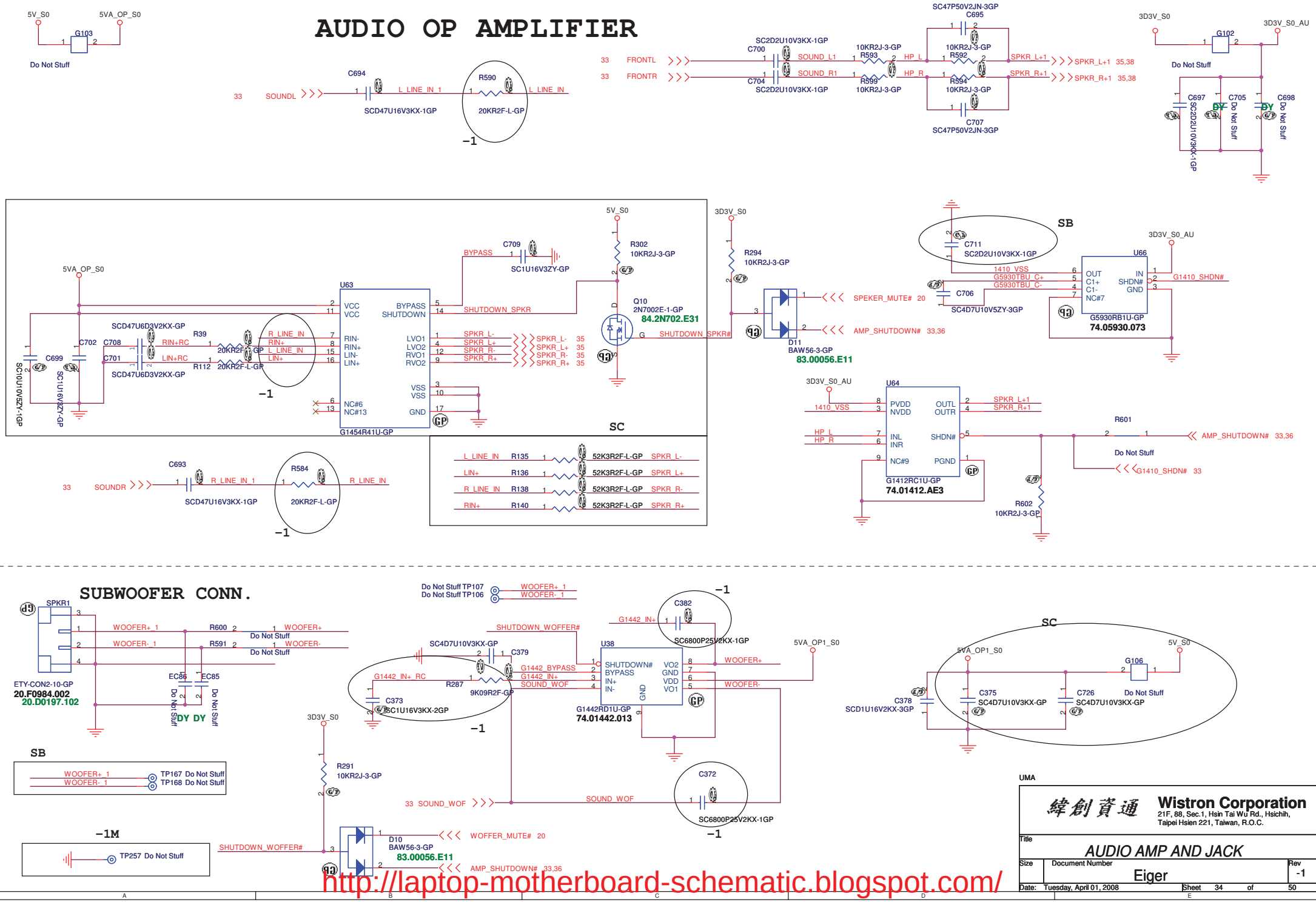
Title: MINI CARD

Size	Document Number	Rev
A3	Eiger	-1

Date: Tuesday, April 01, 2008 Sheet 32 of 50



AUDIO OP AMPLIFIER



SUBWOOFER CONN.

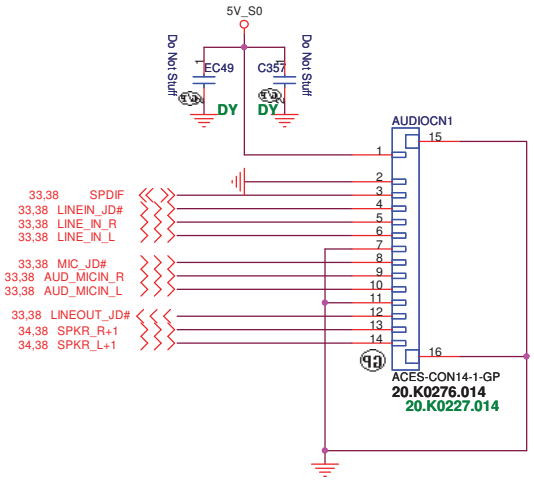
UMA

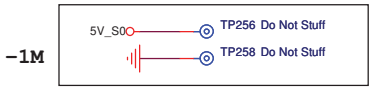
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

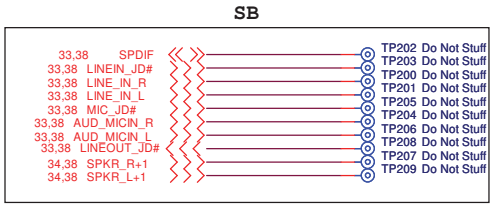
Title: *AUDIO AMP AND JACK*

Size	Document Number	Rev
	Eiger	-1

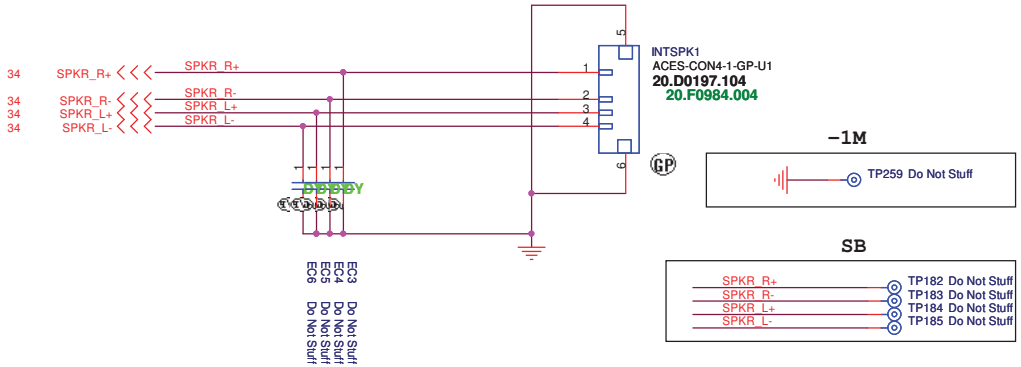
Date: Tuesday, April 01, 2008 Sheet 34 of 50







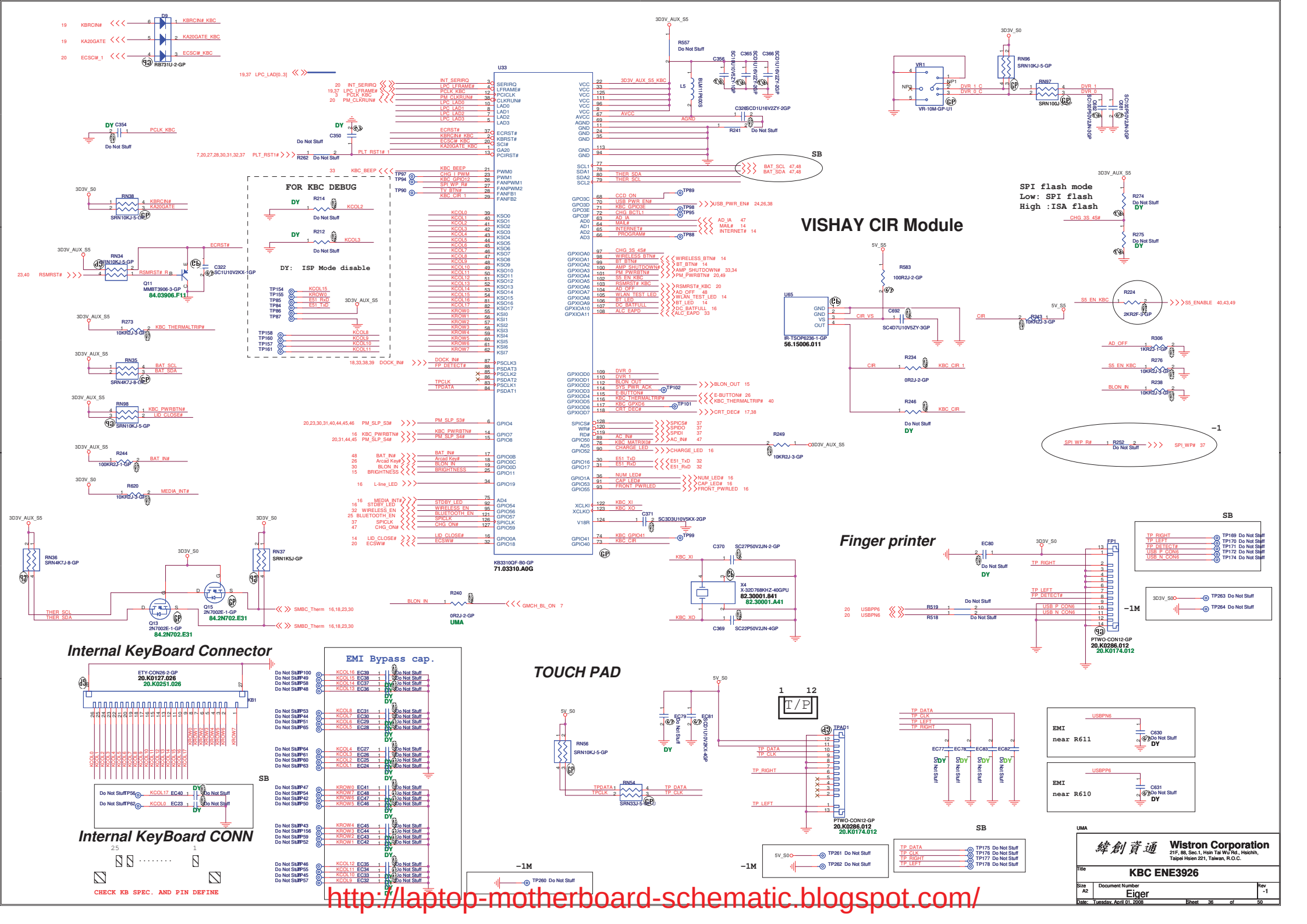
Internal Speaker

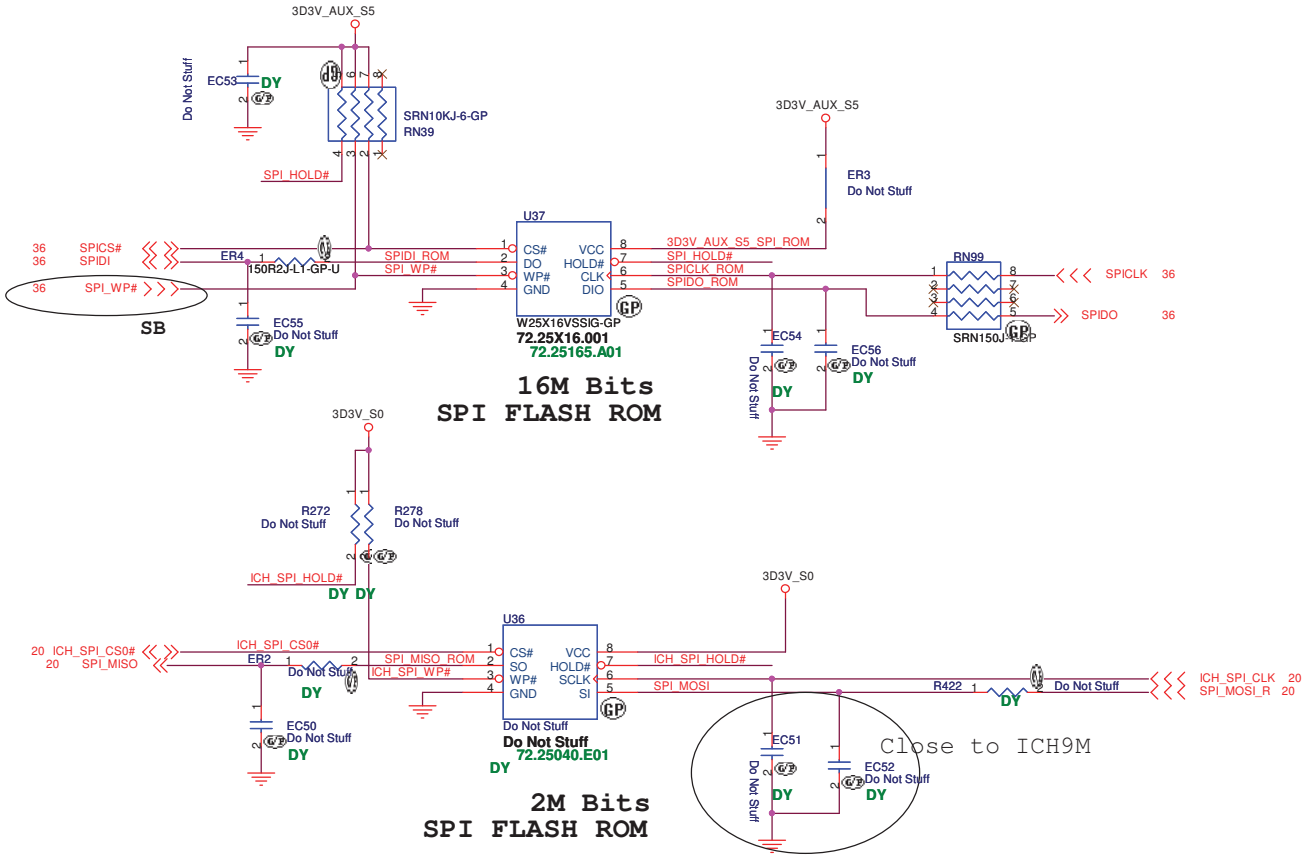


UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
AUDIO JACK		
Size	Document Number: Eiger	Rev: -1
Date: Tuesday, April 01, 2008	Sheet 35 of 50	

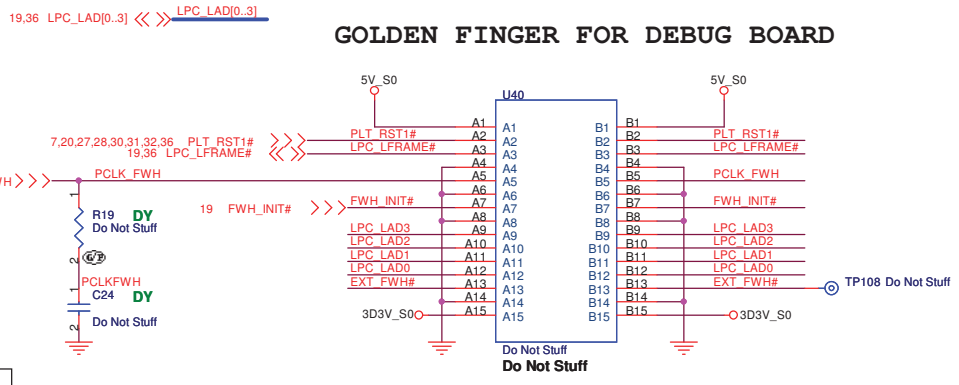


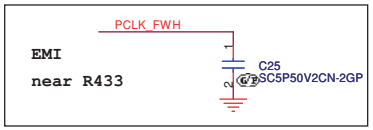


TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

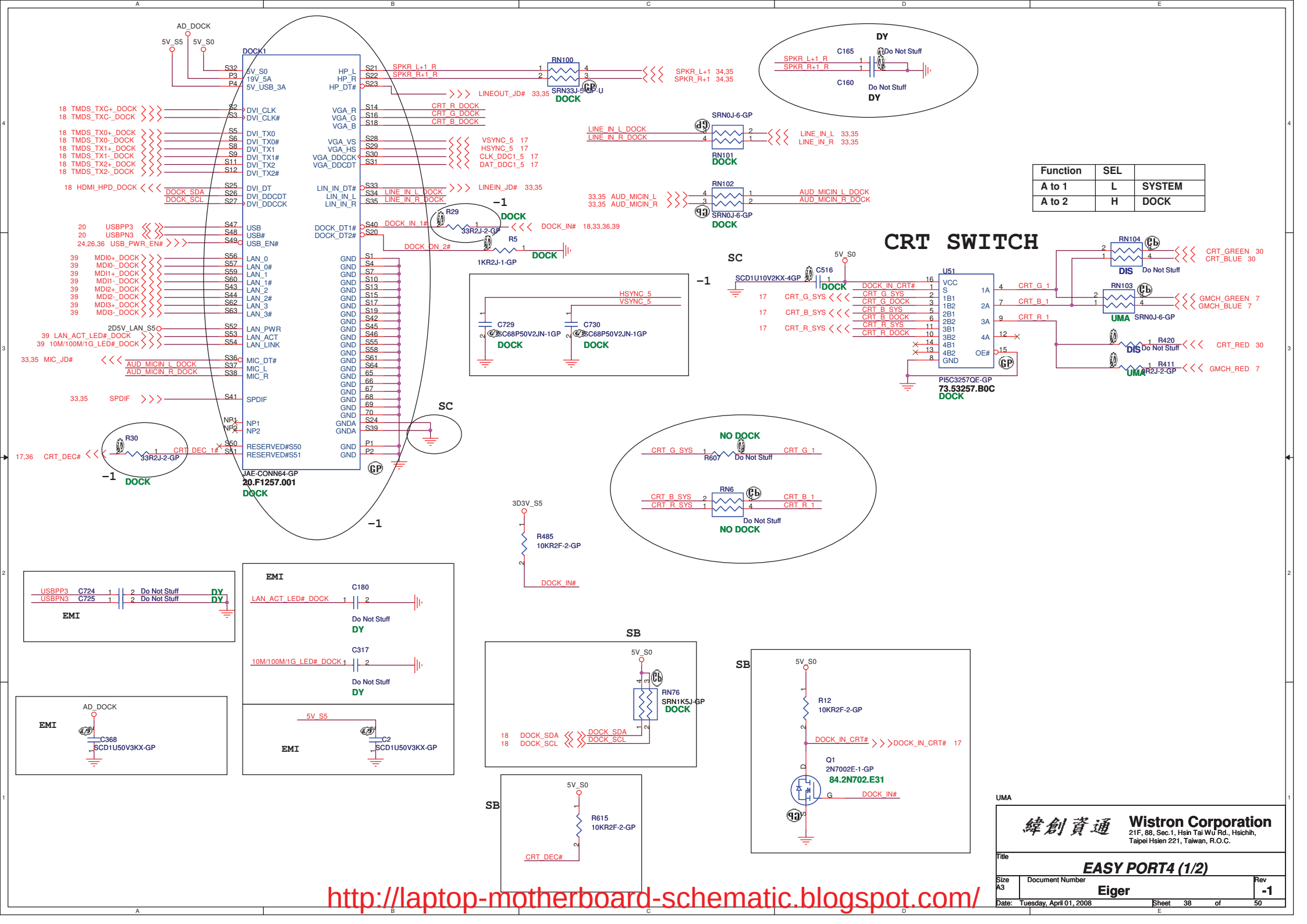




UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

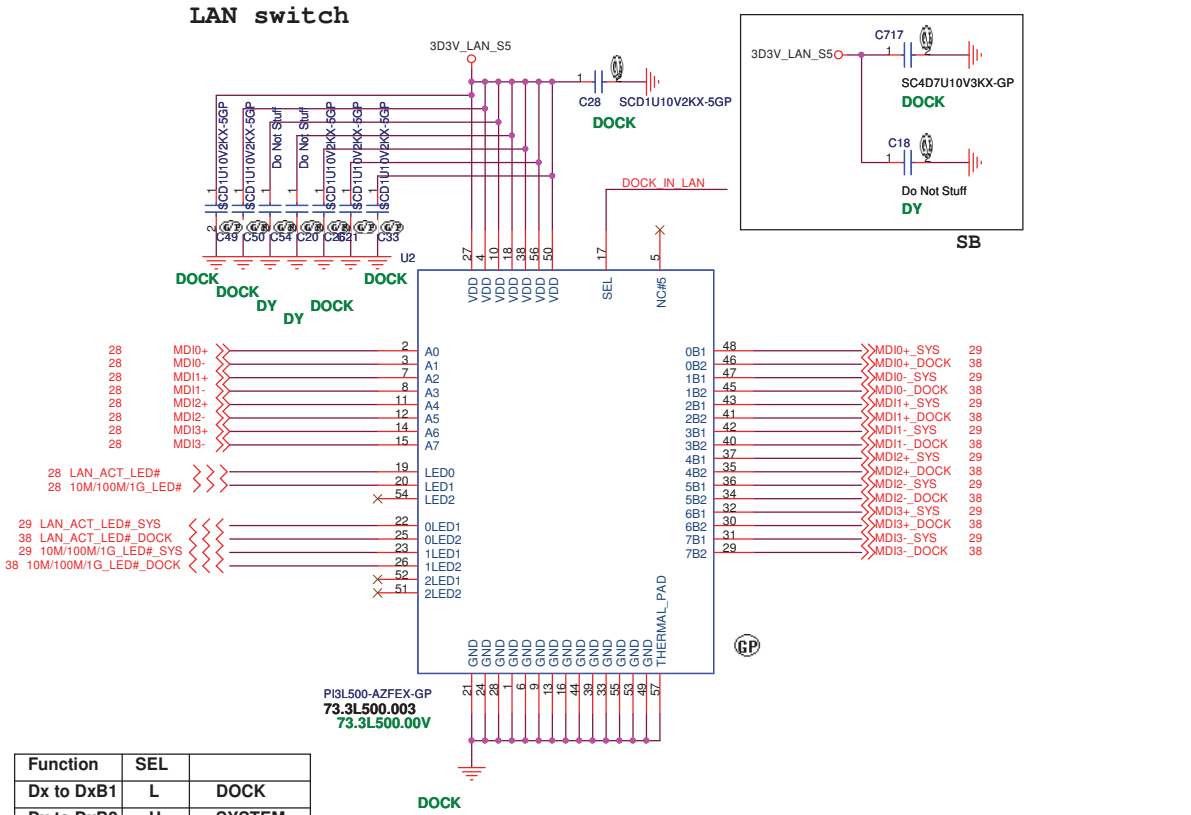
Title	***BIOS***	
Size	Document Number: **Eiger**	Rev: -1
Date: Tuesday, April 01, 2008	Sheet 37 of 49	



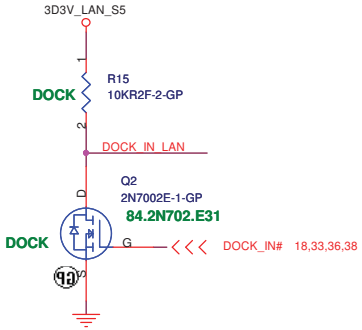
UMA

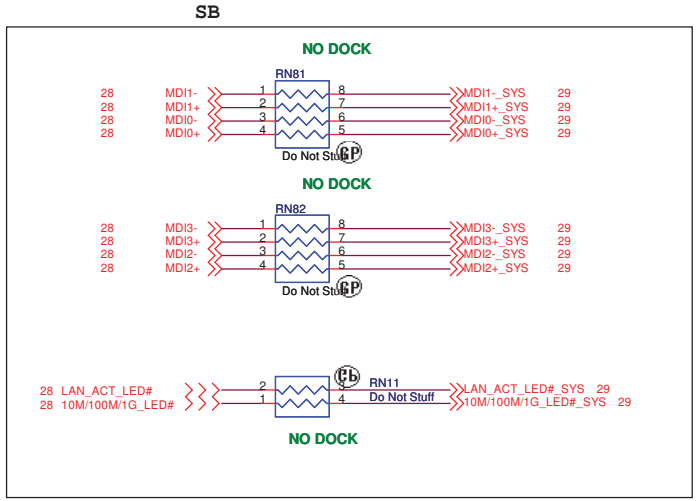
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***EASY PORT4 (1/2)***	
Size A3	Document Number **Eiger**	Rev **-1**
Date: Tuesday, April 01, 2008	Sheet 38 of 50	

LAN switch



Function	SEL	
Dx to DxB1	L	DOCK
Dx to DxB2	H	SYSTEM





UMA

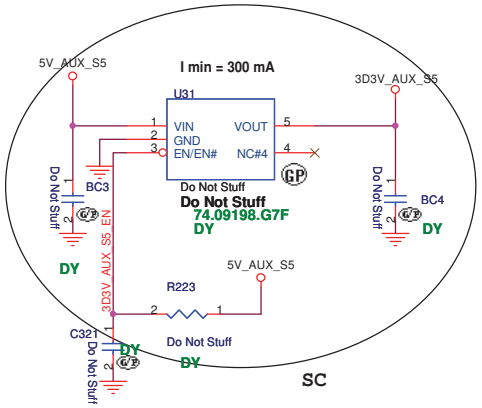
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EASY PORT4 (2/2)***

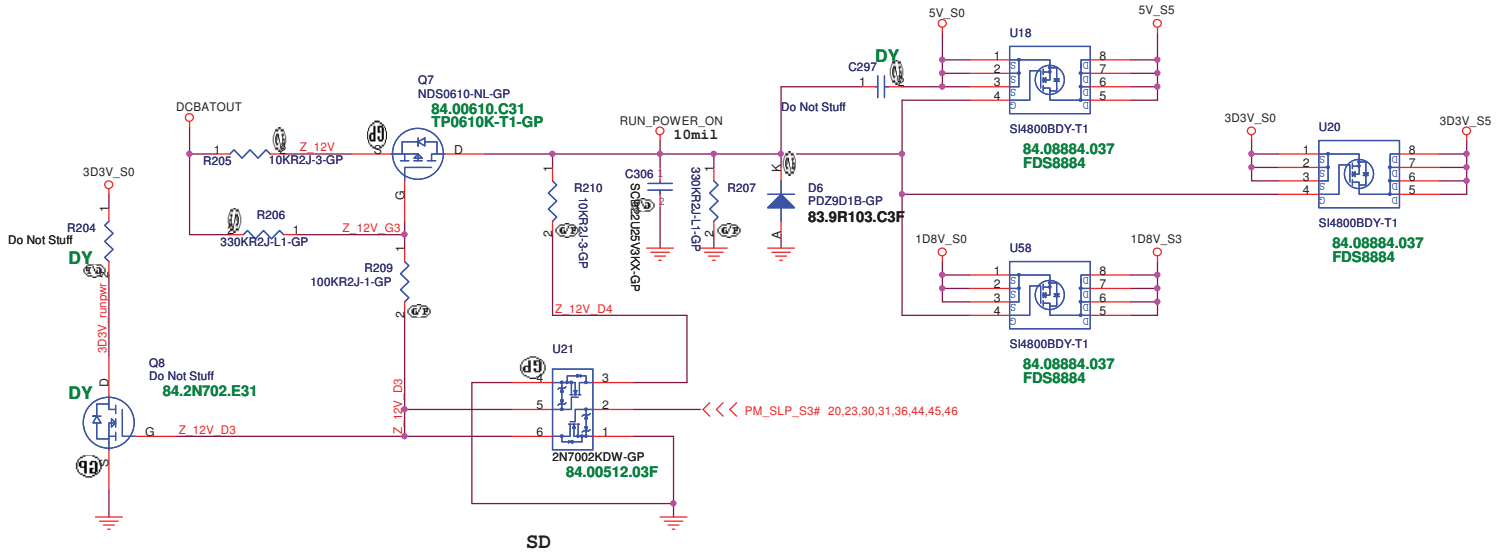
Size	Document Number	Rev
A3	Eiger	-1

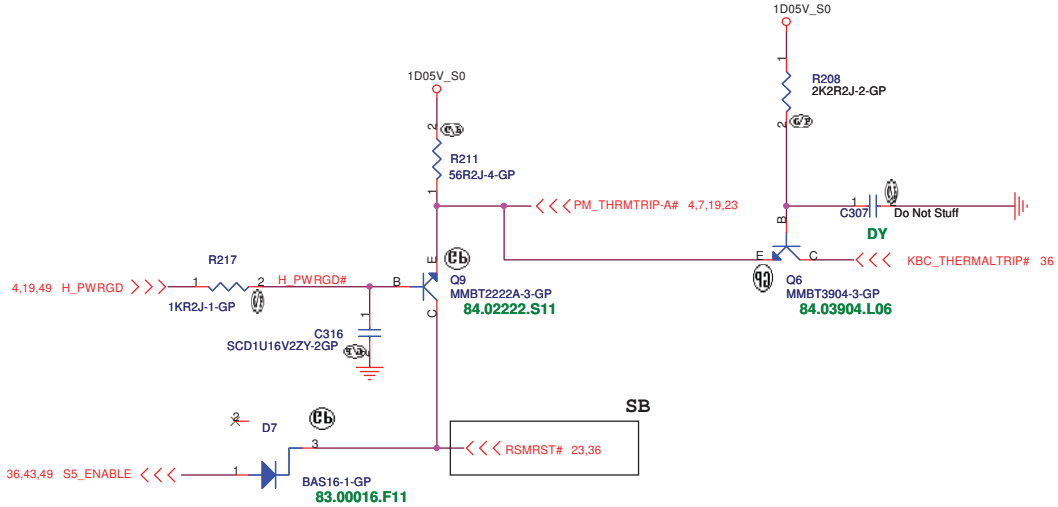
Date: Tuesday, April 01, 2008 Sheet 39 of 49

Aux Power 3D3V_AUX_S5



Run Power





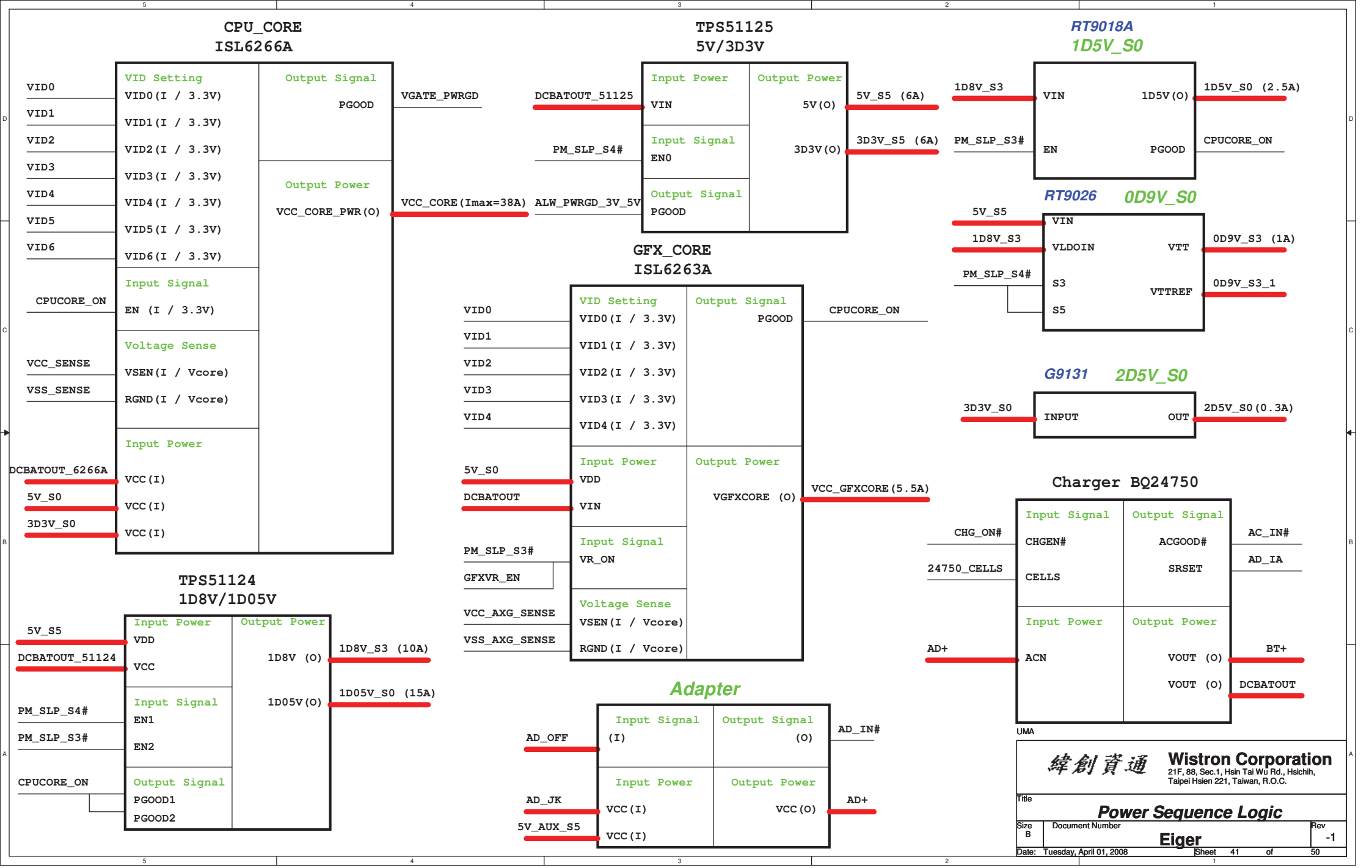
UMA

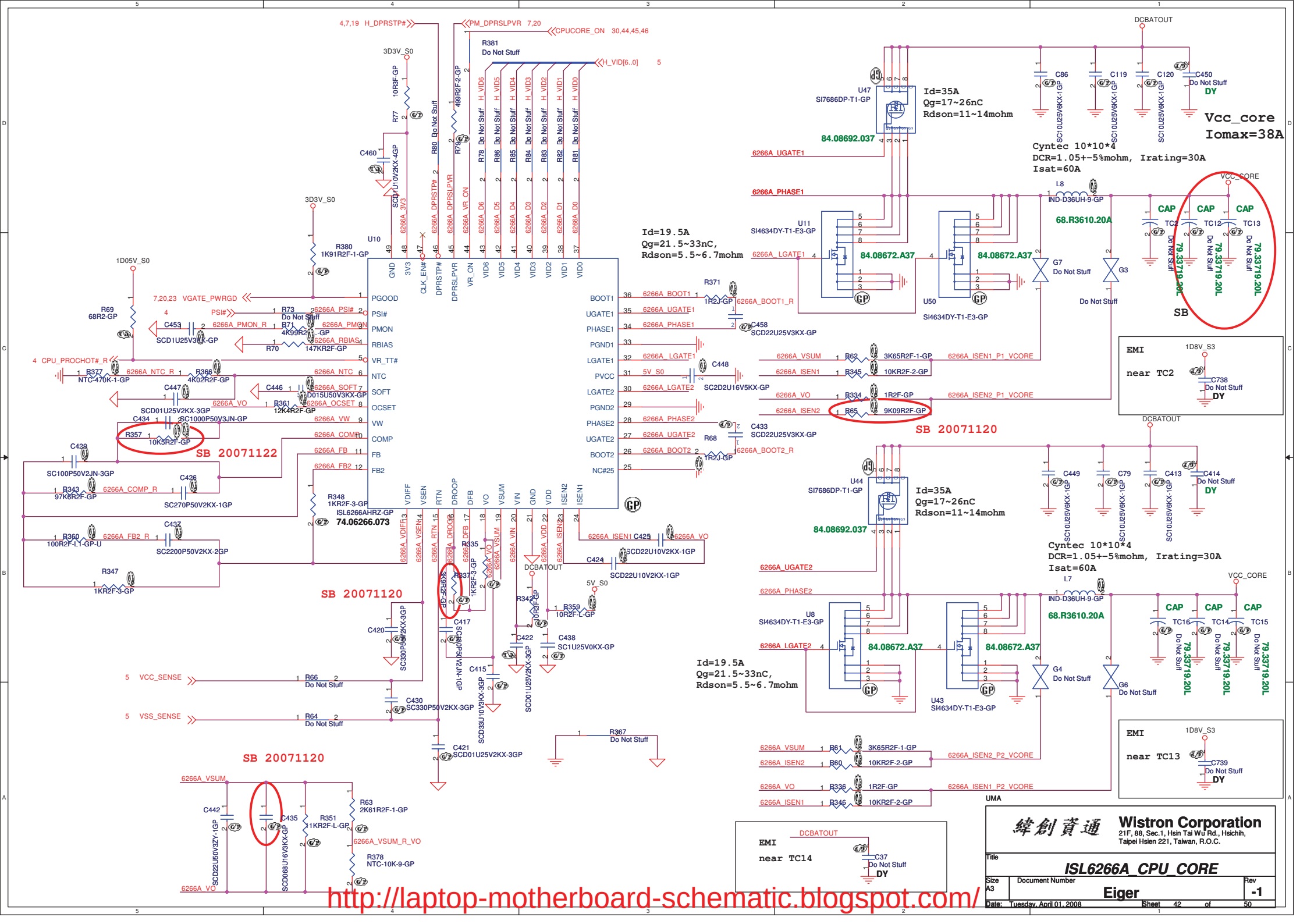
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

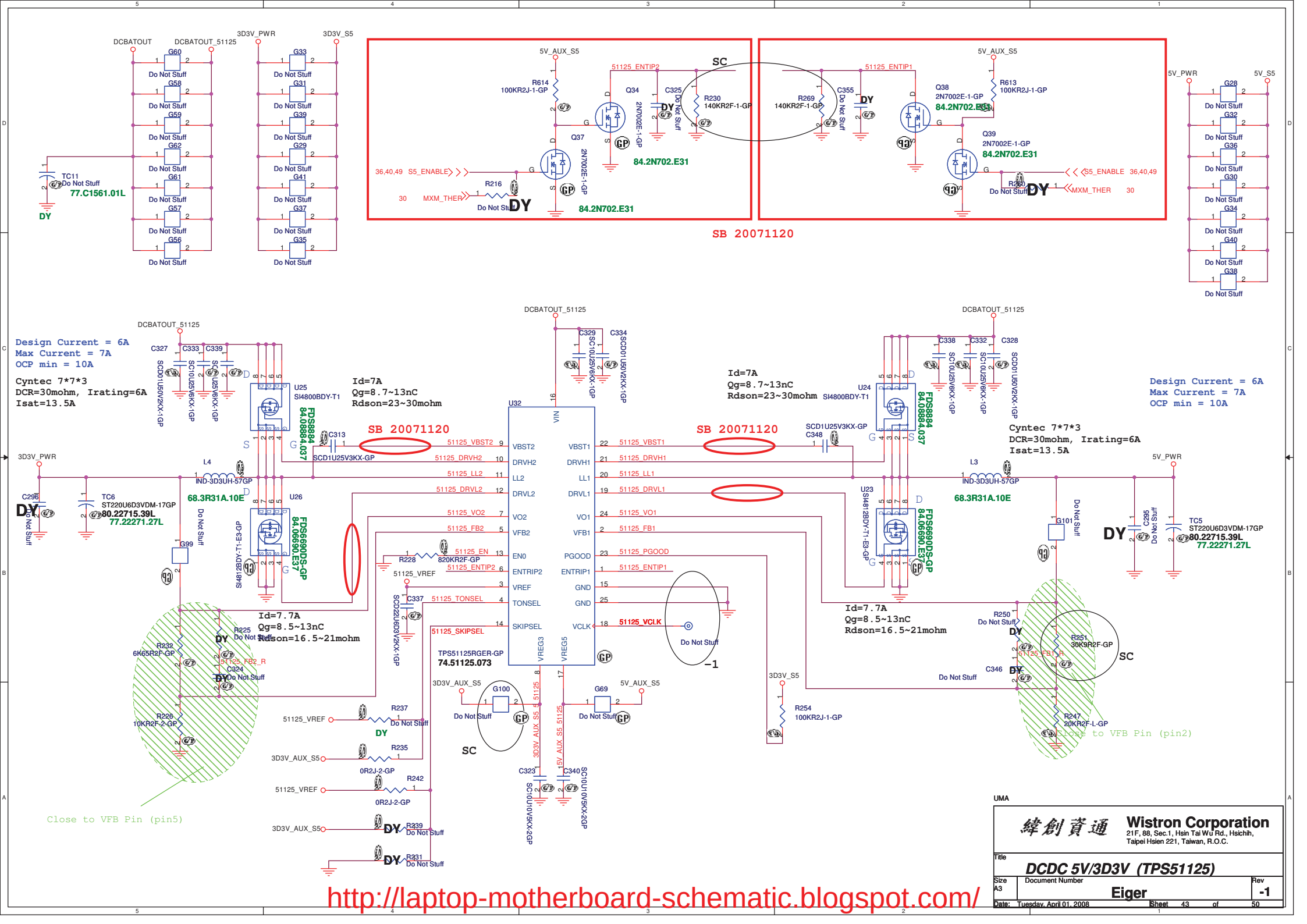
Title: RUN POWER and 3D3V_AUX_S5

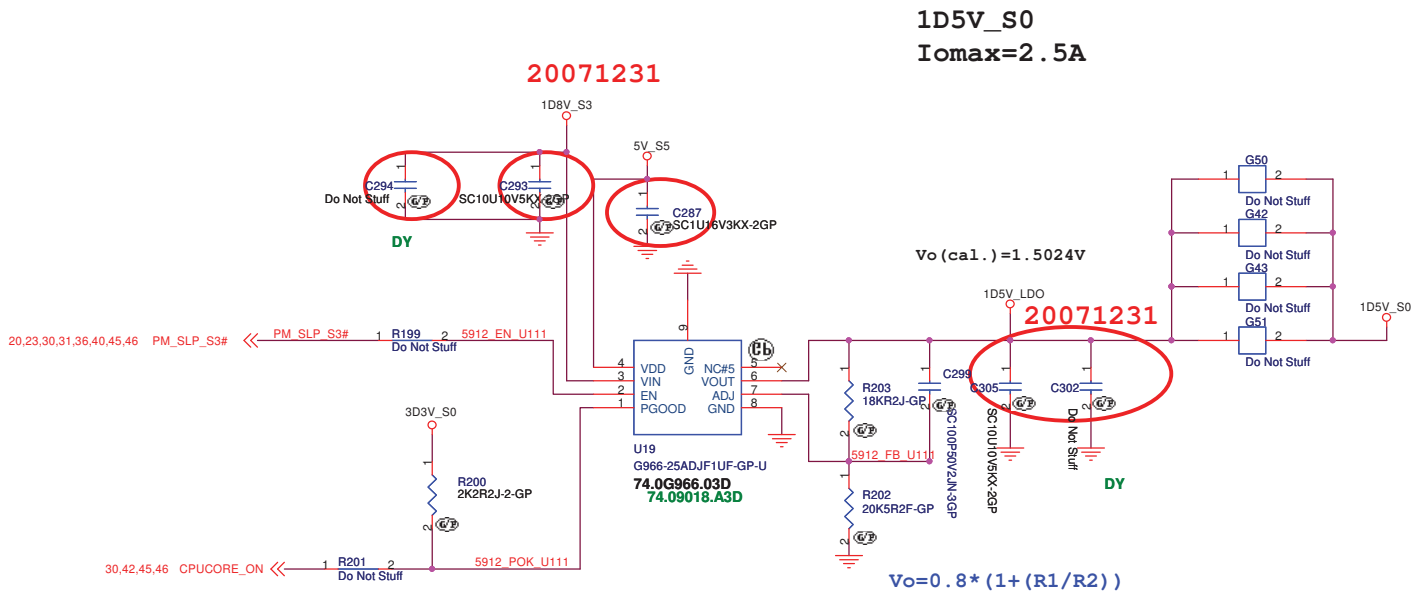
Size	Document Number	Rev
	Eiger	-1

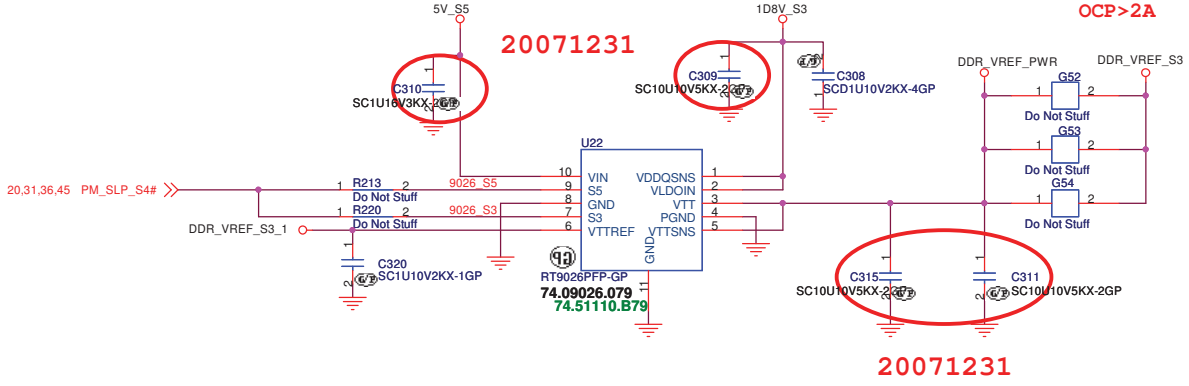
Date: Tuesday, April 01, 2008 Sheet 40 of 50

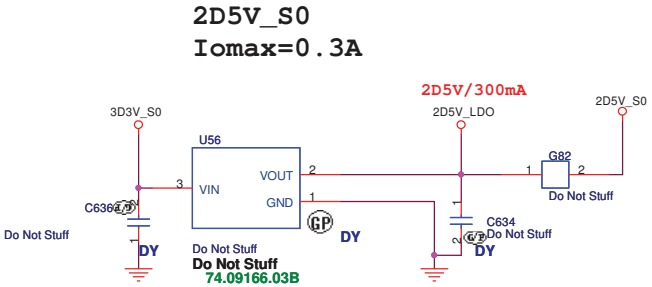












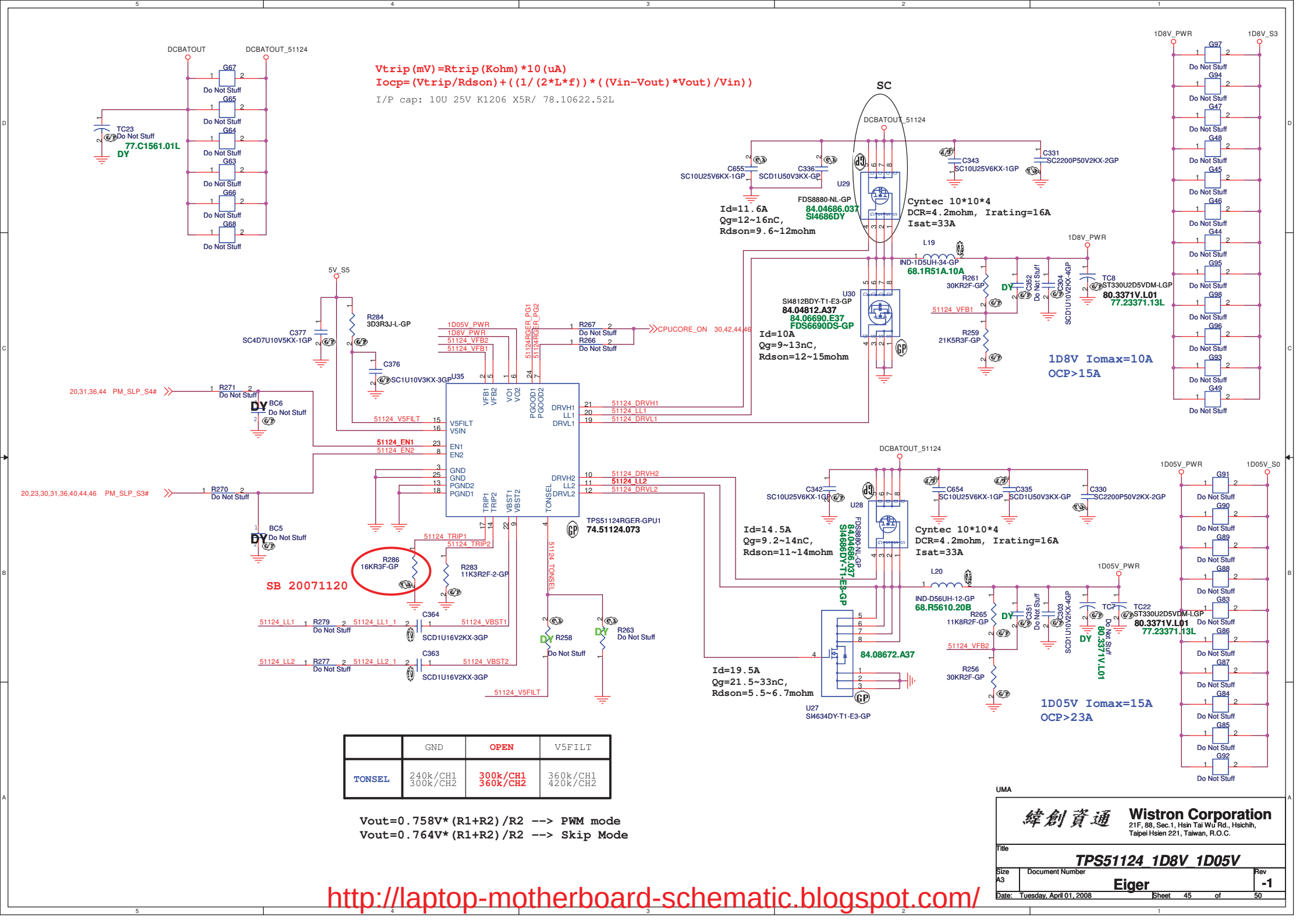
UMA

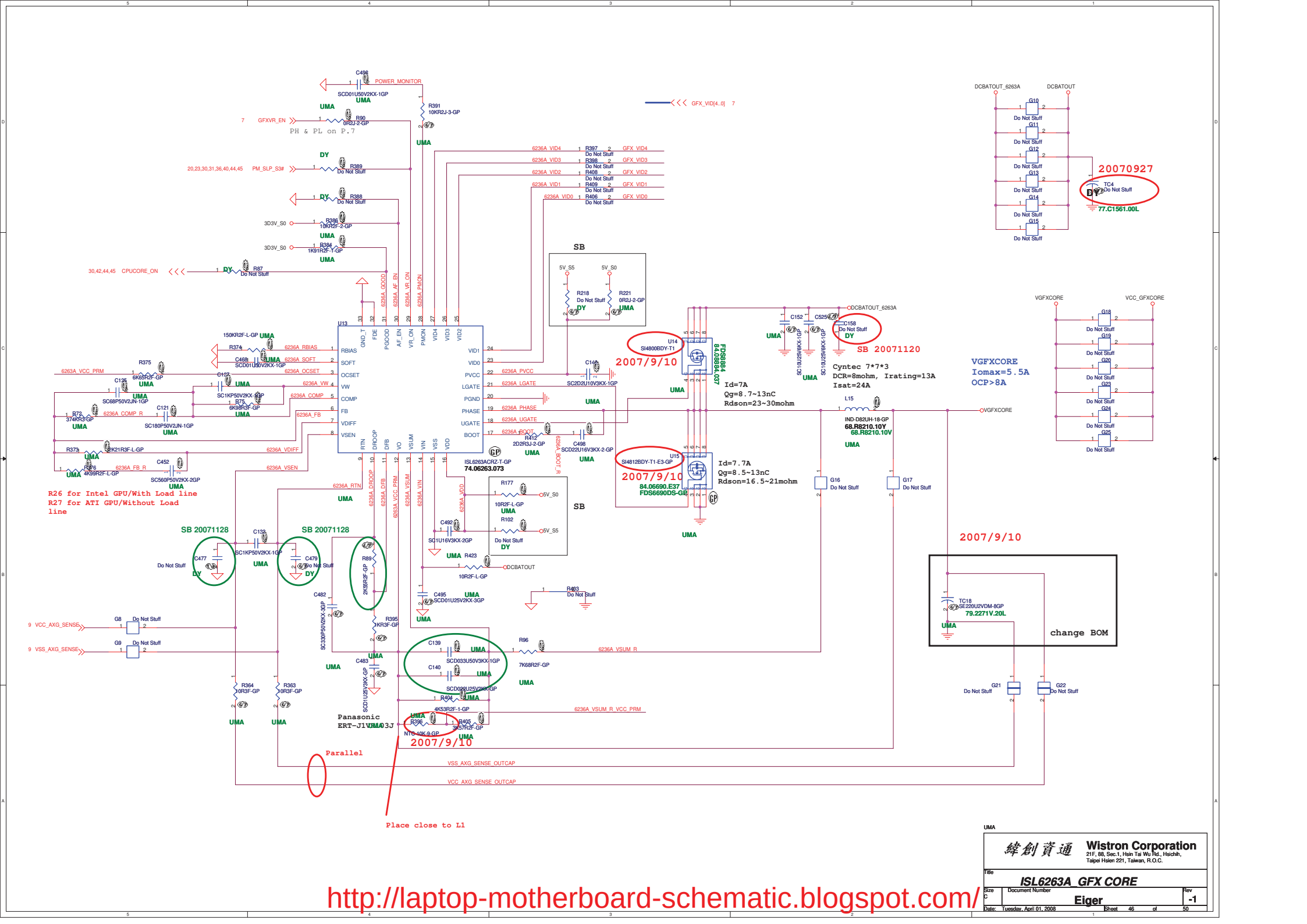
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

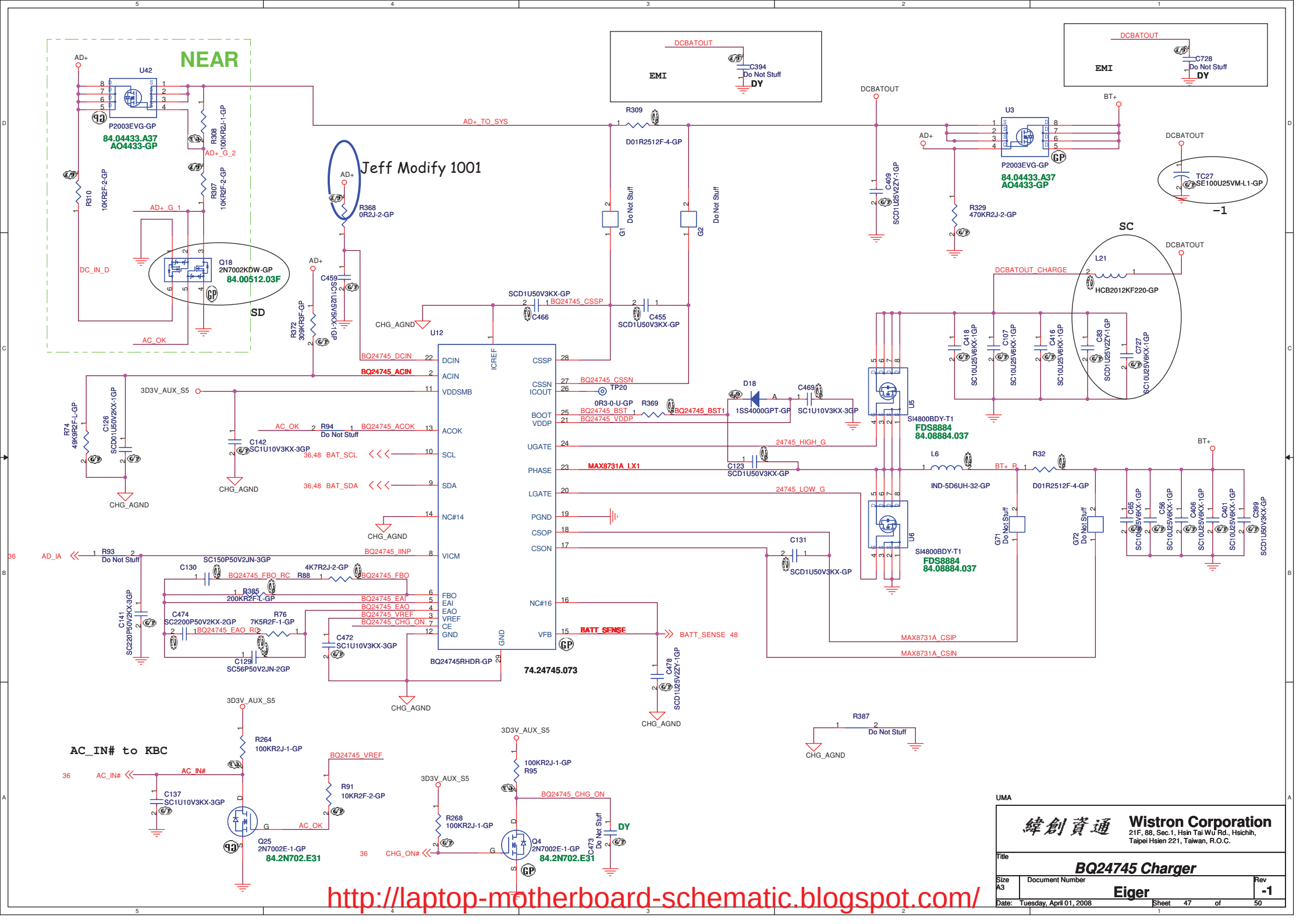
Title: 1D5V & 0D9V & 2D5V

Size	Document Number	Rev
A3	Eiger	-1

Date: Tuesday, April 01, 2008 Sheet 44 of 50




ISL6263A_GFX CORE
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Eiger
Tuesday, April 01, 2008
http://laptop-motherboard-schematic.blogspot.com/
VGFXCORE
Iomax=5.5A
OCP>8A
Cyntec 7*7*3
DCR=8mohm, Irating=13A
Isat=24A
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
R26 for Intel GPU/With Load line
R27 for ATI GPU/Without Load line
SB 20071128
SB 20071120
2007/9/10
change BOM
Parallel
Place close to L1
Panasonic
ERT-J1VR103J
ISL6263ACRZ-T-GP
74.06263.073
SI4800BDY-T1
SI4812BDY-T1-E3-GP
FDS6690DS-GP
FDS8884
84.08884.037
IND-D82UH-18-GP
68.R8210.10Y
68.R8210.10V
TC18
SE220U2VDM-8GP
79.2271V.20L
TC4
20070927
77.C1561.00L
VSS_AXG_SENSE_OUTCAP
VCC_AXG_SENSE_OUTCAP



UMA

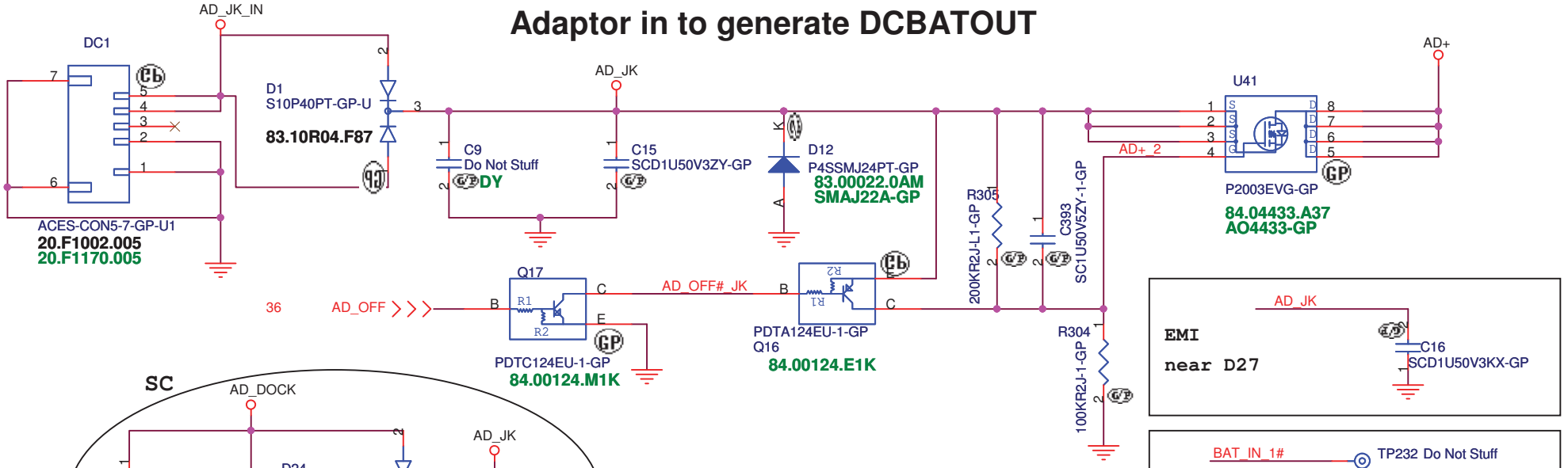
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BQ24745 Charger**

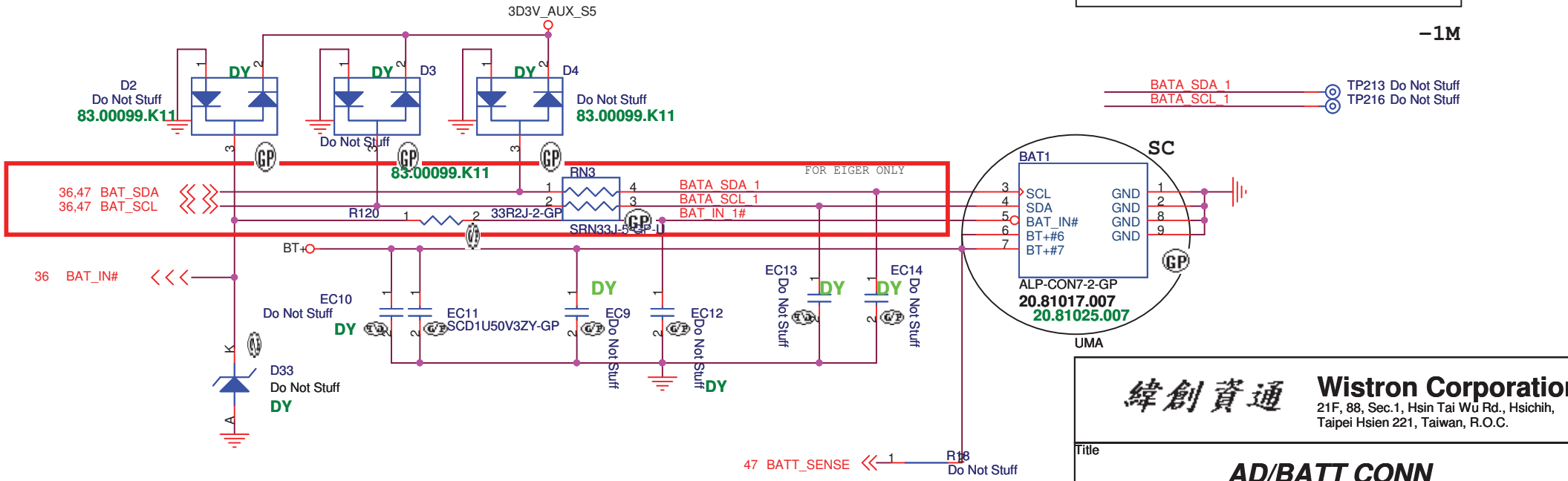
Size	Document Number	Rev
A3	Eiger	-1

Date: Tuesday, April 01, 2008 Sheet 47 of 50

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



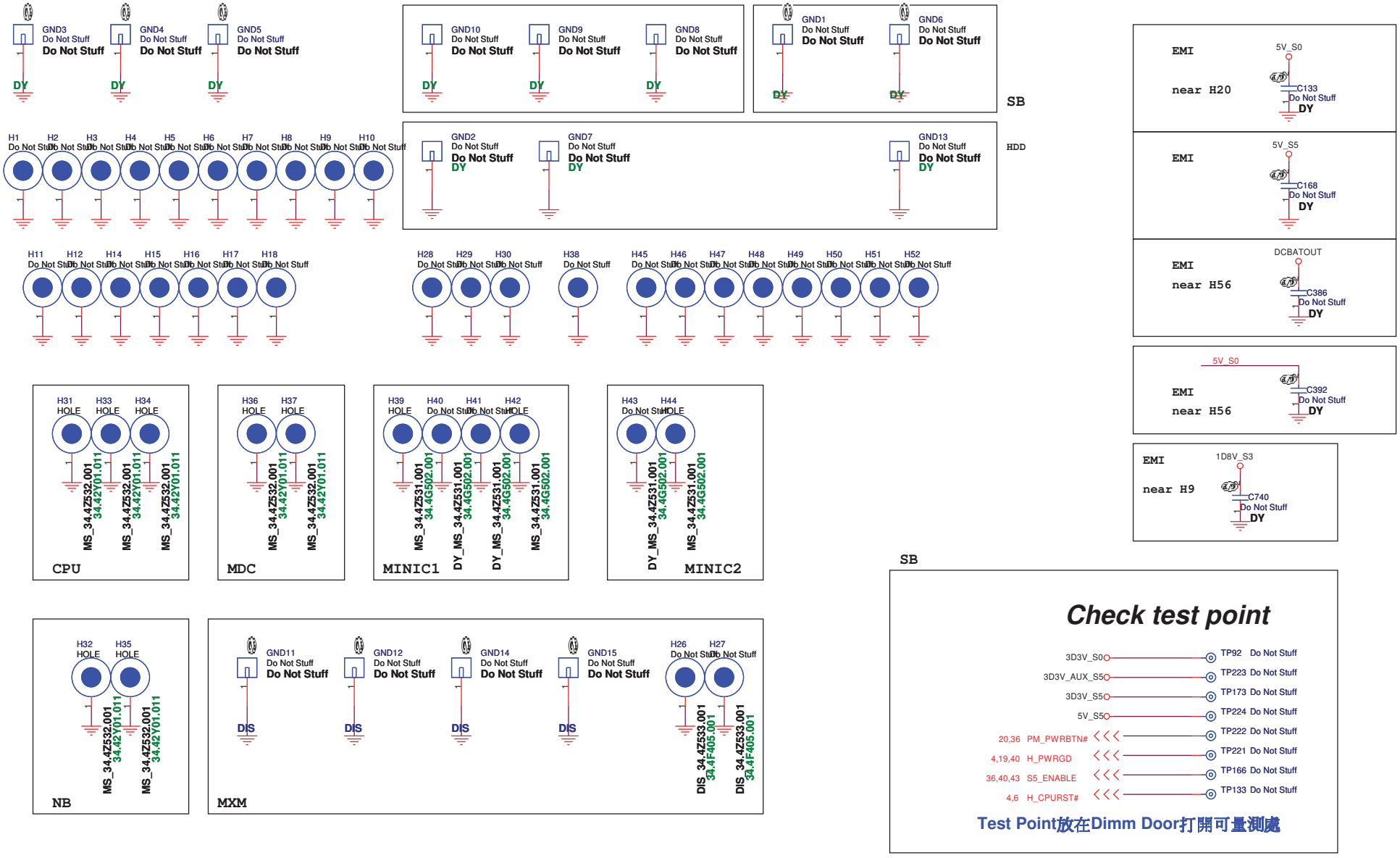
-1M

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**

Size	Document Number	Rev
	Eiger	-1

Date: Tuesday, April 01, 2008 Sheet 48 of 50



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EMI/Spring/Boss***

Size | Document Number: **Eiger** | Rev: -1

Date: Tuesday, April 01, 2008 | Sheet 49 of 50

Eiger Schematic EC Tracking Record LAB Dec.10 , 2007
EC #/ Page / Description / Part Affected

EC SB01/07/ DY R175 (fix can not boot)
EC SB02/07/ change R184 (intel spec change)
EC SB03/10/ mount L2,C221 (intel spec change)
EC SB04/15/ modify LCD2 pin define(add dig-MIC,backlight)
EC SB05/17/ DOCK_IN_CRT# logic change
EC SB06/18/ change HDMI level shift IC setting
EC SB07/19/ change R606(meet HDA SPEC)
EC SB08/23/ change PURE_HW_SHUTDOWN# ,PM_THRMTRIP-A# schematic
EC SB09/26/ change C648 ,deltree poly switch
EC SB10/27/ change R555,R557,R559 (vendor request)
EC SB11/30/ change R612 (vendor request)
EC SB12/34/ add C711 (fix audio noise)
EC SB13/36/ add SPI_WP# (BIOS wirte protect)
EC SB14/38/ add CRT_DEC# (Acer change spec)
EC SB15/38/ add dock/no dock option schematic
EC SB16/40/ D7(power sequencing)
EC SC01/16/ R595,R596,R597,R598(LED)
EC SC02/18/ HEMI level shift & switch solution change
EC SC03/19/ ESATA function
EC SC04/23/ H/W Thermal shut down,power off Sequence
EC SC05/24/ Add ESATA circuit
EC SC06/30/ Add R116(MXM aczrst# Acer request)
EC SC07/33/ Add audio gound
EC SC08/34/ Change audio AMP circuit
EC SC09/38/ Add RC circuit to reduce audio noise
EC SC10/40/ 3D3V_AUX_S5 from U32 internal LDO
EC SC11/43/ Change 5V to 5.1V
EC SC12/47/ Isolate Change IC switching high side MOS input power
EC SC13/48/ Isolate AD19V in and Dock19V in

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EC Tracking Record***

Size	Document Number	Rev
	Eiger	-1

Date: Tuesday, April 01, 2008 Sheet 50 of 50