

Compal Confidential

Model Name : P5LJ0 & P5LS0

File Name : LA-7221P

Compal Confidential

JM50-HR M/B Schematics Document

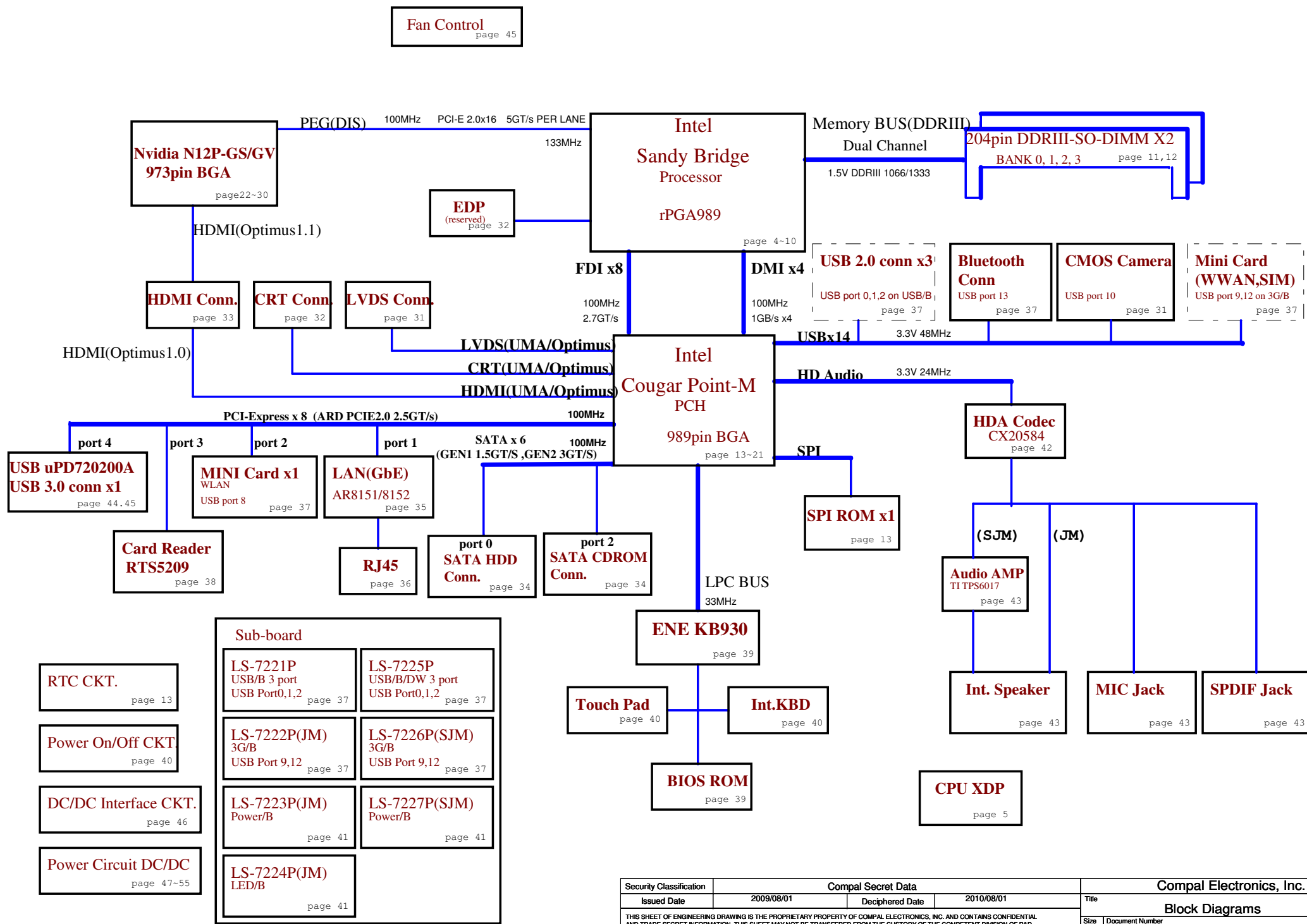
Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH  
Nvidia N12P-GS/GV

2010-02-16

REV : 0.5

MB PCB	
Part Number	Description
DA80000MA00	PCB 01N LA-7221P REV0 M/B

Security Classification		Compal Secret Data		Compal Electronics, Inc.				
Issued Date		2009/08/01		Deciphered Date		2010/08/01		
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VCCP	+1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCP to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

EC SM Bus2 address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

3G & BT Config

3G SKU: 3G@

BT SKU: BT@

BOM Config

JM UMA Only: BT@/3G@/UMA@/UMAO@/JM@/8151@  
JM OPTIMUS: BT@/3G@/UMA@/OPT@/JM@/8151@/GV@/GS@  
SJM UMA Only: BT@/3G@/UMA@/UMAO@/SJM@/8151@  
SJM OPTIMUS: BT@/3G@/UMA@/OPT@/SJM@/8151@/GV@/GS@

BOM P/N(JM/SJM)

4319BOBOL01/L21 UMA W3G HDMI  
4319BOBOL02/L22 UMA N3G HDMI  
4319BOBOL03/L23 N12PGS 1GW3G HDMI  
4319BOBOL04/L24 N12PGS 1GN3G HDM  
4319BOBOL05/L25 N12PGS 2GW3G HDMI  
4319BOBOL06/L26 N12PGS 2GN3G HDMI  
4319BOBOL07/L27 N12PGV 512W3G HDMI  
4319BOBOL08/L28 N12PGV 512N3G HDMI

VRAM BOM Config

X76289BOL01 512M SAM 64M16  
X76289BOL02 512M HYN 64M16  
X76289BOL03 1G SAM 64M16  
X76289BOL04 1G HYN 64M16  
X76289BOL05 2G SAM 128M16  
X76289BOL06 2G HYN 128M16

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
UMA Only	UMAO@
UMA with OPTIMUS	UMA@
OPTIMUS1.0	OPT@
OPTIMUS1.1	OPT11@
N12P-GS@	GS@
N12P-GV@	GV@
VRAM	X76@
Connector	CONN@
3G	3G@
Blue Tooth	BT@
EDP	EDP@
LAN Chip AR8151	8151@
LAN Chip AR8152	8152@
JM Board	JM@
SJM Board	SJM@
Unpop	@
Power GPU	VGA@

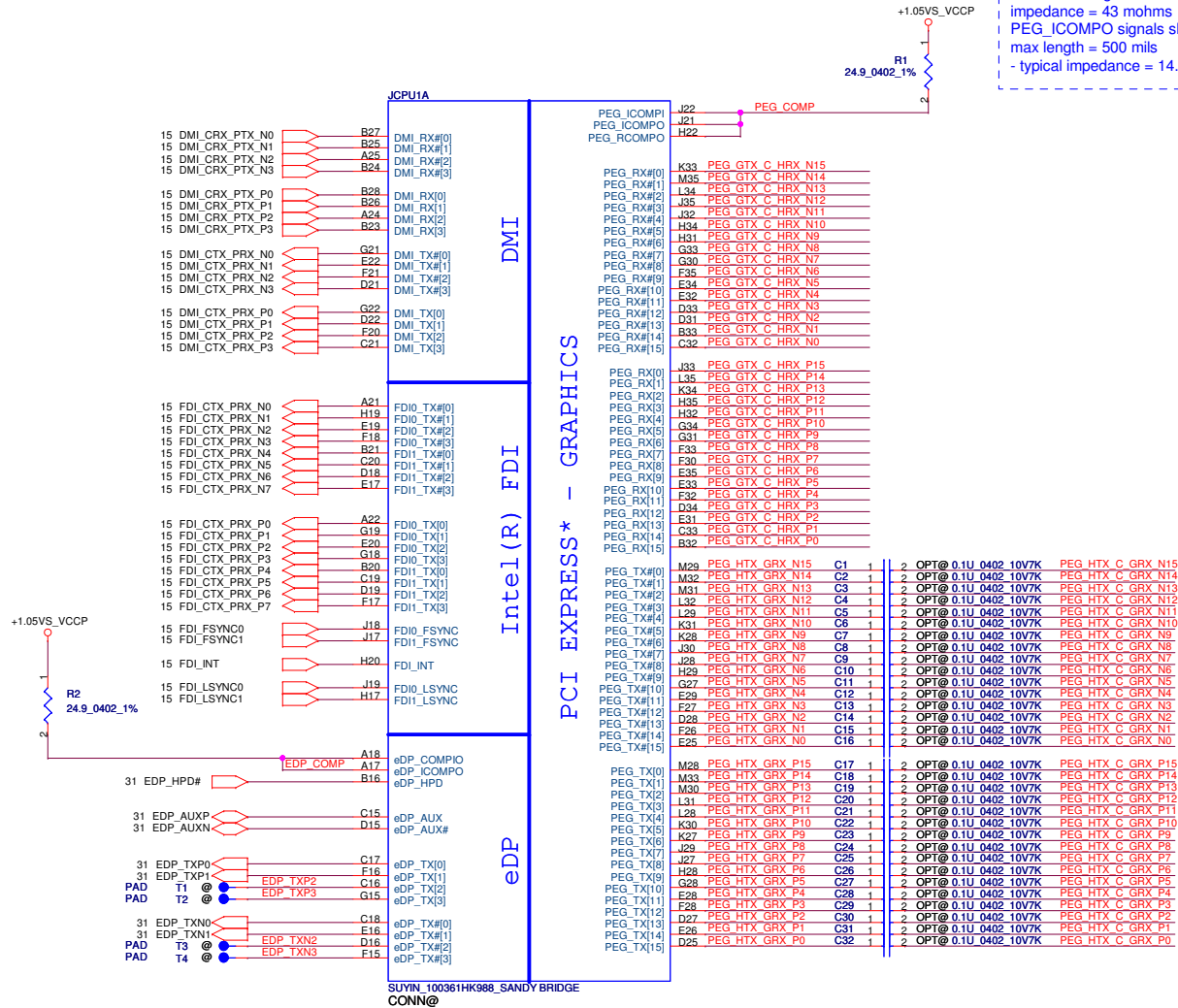
USB Port Table

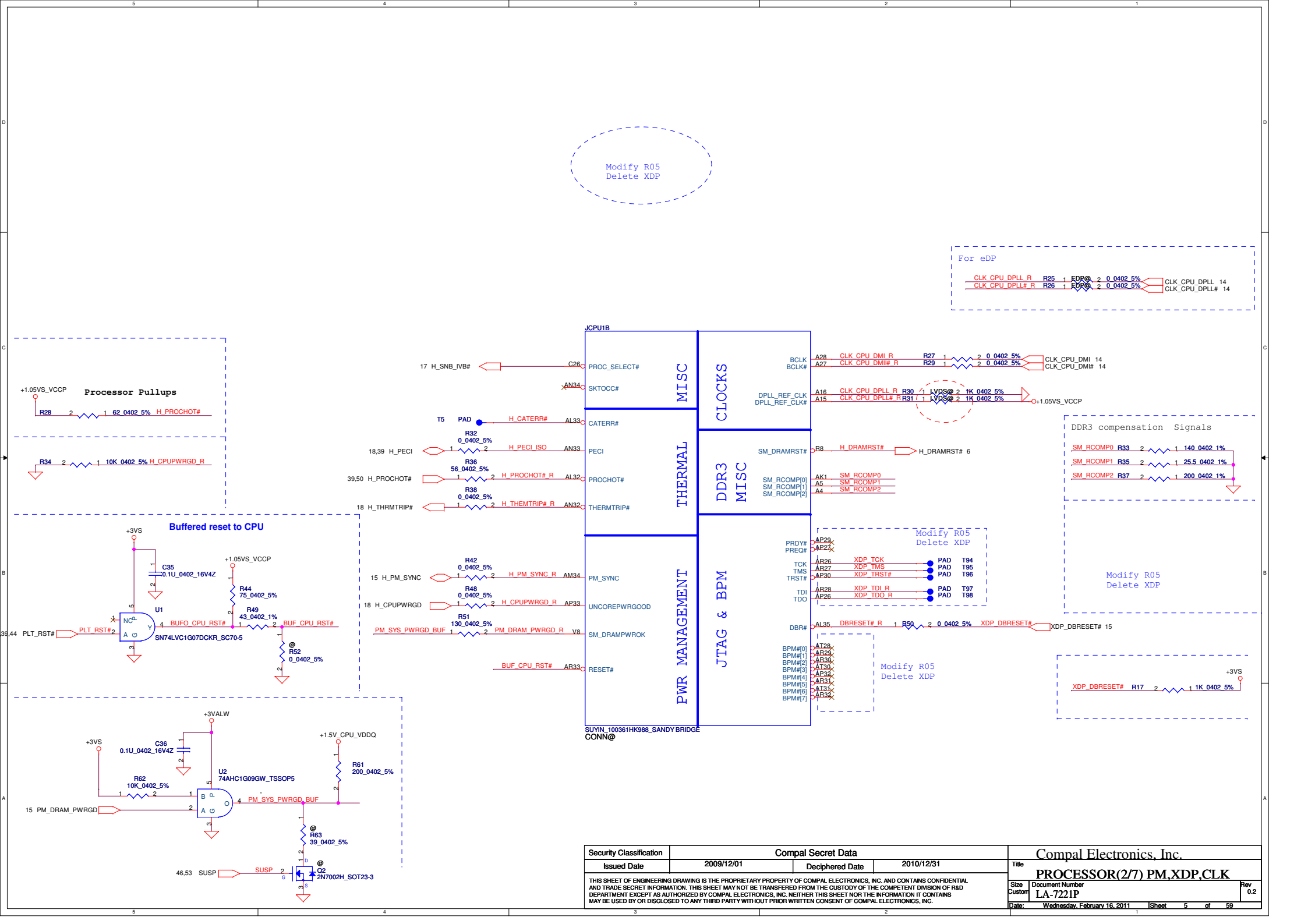
USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB/B (Right Side)
		2	USB/B (Right Side)
	UHCI1	3	
		4	
		5	
EHCI2	UHCI2	6	
		7	
		8	Mini Card(WLAN)
	UHCI3	9	Mini Card(WWAN)
		10	Camera
		11	
	UHCI4	12	SIM Card
		13	Blue Tooth

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Issued Date	2009/08/01	Deciphered Date	2010/08/01	Notes List		
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eDP\_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

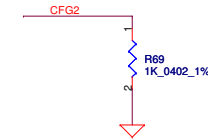
PEG\_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms  
PEG\_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms



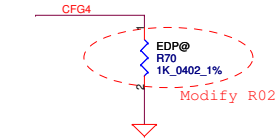




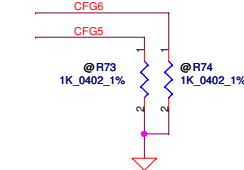
# CFG Straps for Processor



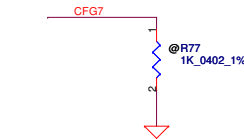
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



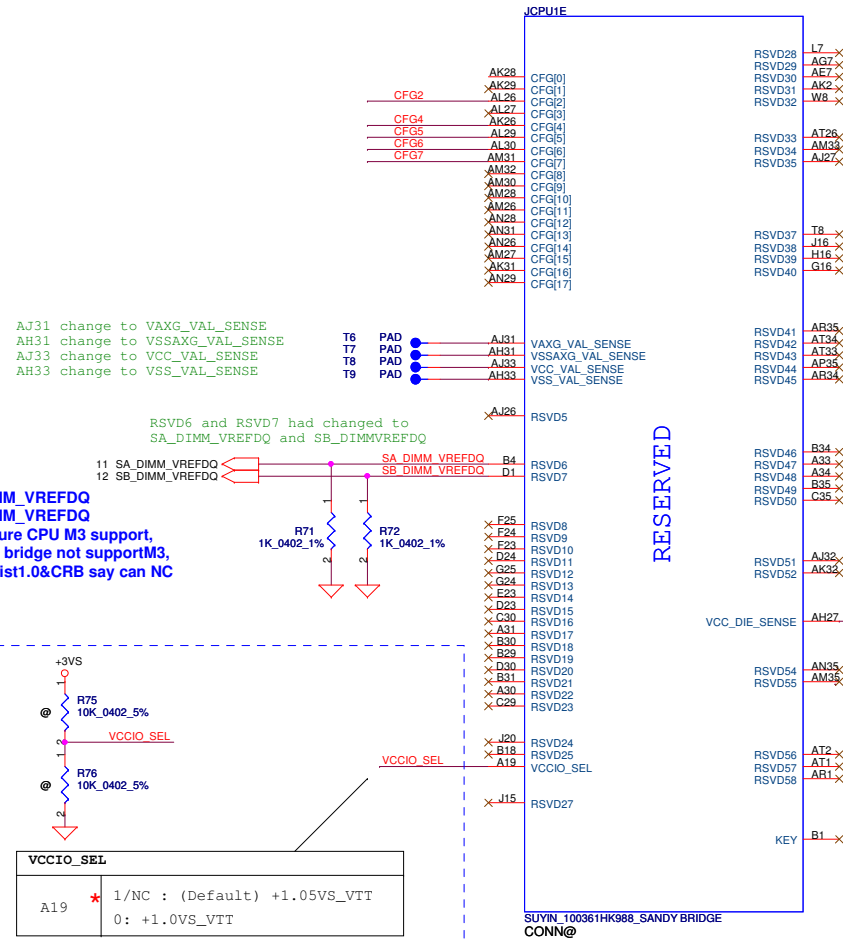
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



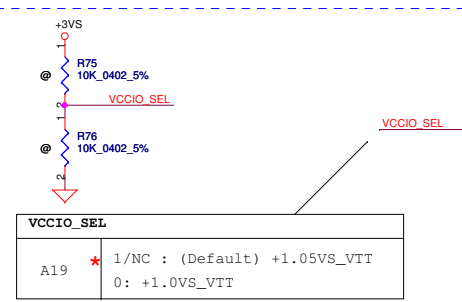
PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



AJ31 change to VAXG\_VAL\_SENSE  
AH31 change to VSSAXG\_VAL\_SENSE  
AJ33 change to VCC\_VAL\_SENSE  
AH33 change to VSS\_VAL\_SENSE

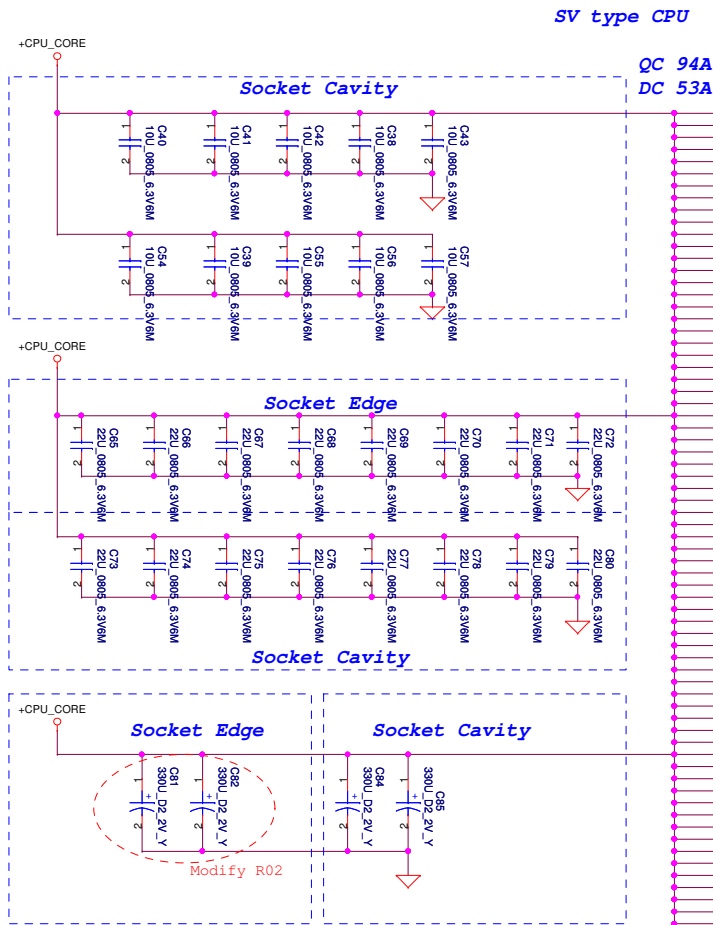
RSVD6 and RSVD7 had changed to  
SA\_DIMM\_VREFDQ and SB\_DIMM\_VREFDQ

**SA\_DIMM\_VREFDQ**  
**SB\_DIMM\_VREFDQ**  
For Future CPU M3 support,  
Sandy bridge not support M3,  
Check list1.0&CRB say can NC



**VCCIO\_SEL** For 2012 CPU support  
RSVD26 had changed the name to VCCIO\_SEL  
Need PH +3VS 10K at +1.05VS\_VTT source  
for 2012 processor +1.05V and +1.0V select

4x 470  $\mu$ F Bottom Socket Edge  
8x 22  $\mu$ F Top Socket Cavity  
8x 22  $\mu$ F Top Socket Edge  
10x 10  $\mu$ F Bottom Socket Cavity



JCPU1F

AG35	VCC1
AG34	VCC2
AG33	VCC3
AG32	VCC4
AG31	VCC5
AG30	VCC6
AG29	VCC7
AG28	VCC8
AG27	VCC9
AG26	VCC10
AF35	VCC11
AF34	VCC12
AF33	VCC13
AF32	VCC14
AF31	VCC15
AF30	VCC16
AF29	VCC17
AF28	VCC18
AF27	VCC19
AF26	VCC20
AD35	VCC21
AD34	VCC22
AD33	VCC23
AD32	VCC24
AD31	VCC25
AD30	VCC26
AD29	VCC27
AD28	VCC28
AD27	VCC29
AD26	VCC30
AC35	VCC31
AC34	VCC32
AC33	VCC33
AC32	VCC34
AC31	VCC35
AC30	VCC36
AC29	VCC37
AC28	VCC38
AC27	VCC39
AC26	VCC40
AA35	VCC41
AA34	VCC42
AA33	VCC43
AA32	VCC44
AA31	VCC45
AA30	VCC46
AA29	VCC47
AA28	VCC48
AA27	VCC49
AA26	VCC50
Y35	VCC51
Y34	VCC52
Y33	VCC53
Y32	VCC54
Y31	VCC55
Y30	VCC56
Y29	VCC57
Y28	VCC58
Y27	VCC59
Y26	VCC60
Y25	VCC61
V34	VCC62
V33	VCC63
V32	VCC64
V31	VCC65
V30	VCC66
V29	VCC67
V28	VCC68
V27	VCC69
V26	VCC70
U35	VCC71
U34	VCC72
U33	VCC73
U32	VCC74
U31	VCC75
U30	VCC76
U29	VCC77
U28	VCC78
U27	VCC79
U26	VCC80
R35	VCC81
R34	VCC82
R33	VCC83
R32	VCC84
R31	VCC85
R30	VCC86
R29	VCC87
R28	VCC88
R27	VCC89
R26	VCC90
P35	VCC91
P34	VCC92
P33	VCC93
P32	VCC94
P31	VCC95
P30	VCC96
P29	VCC97
P28	VCC98
P27	VCC99
P26	VCC100

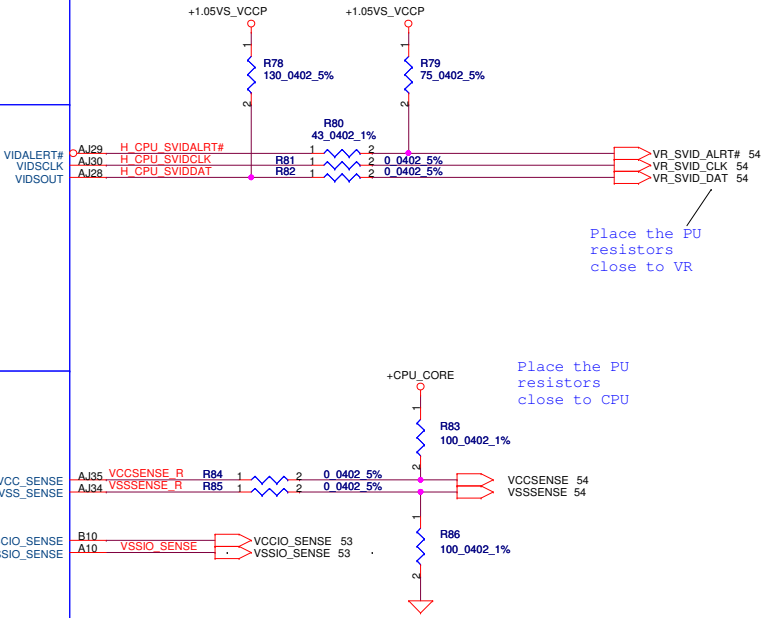
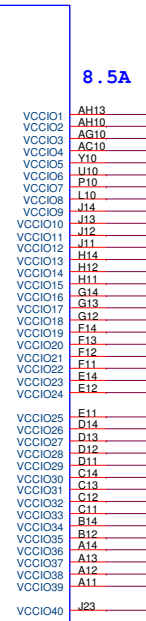
## POWER

PEG AND DDR

CORE SUPPLY

SVID

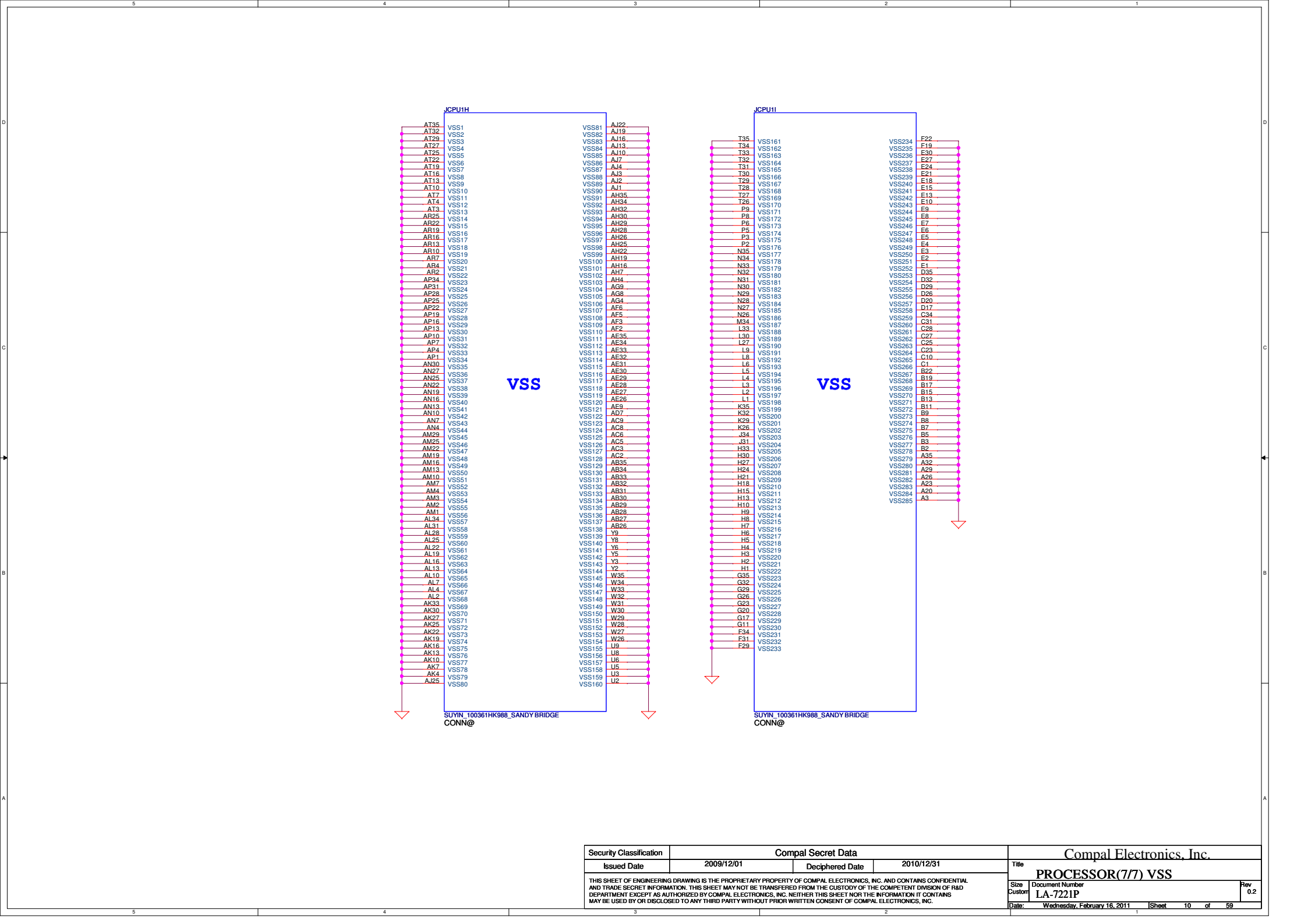
SENSE LINES

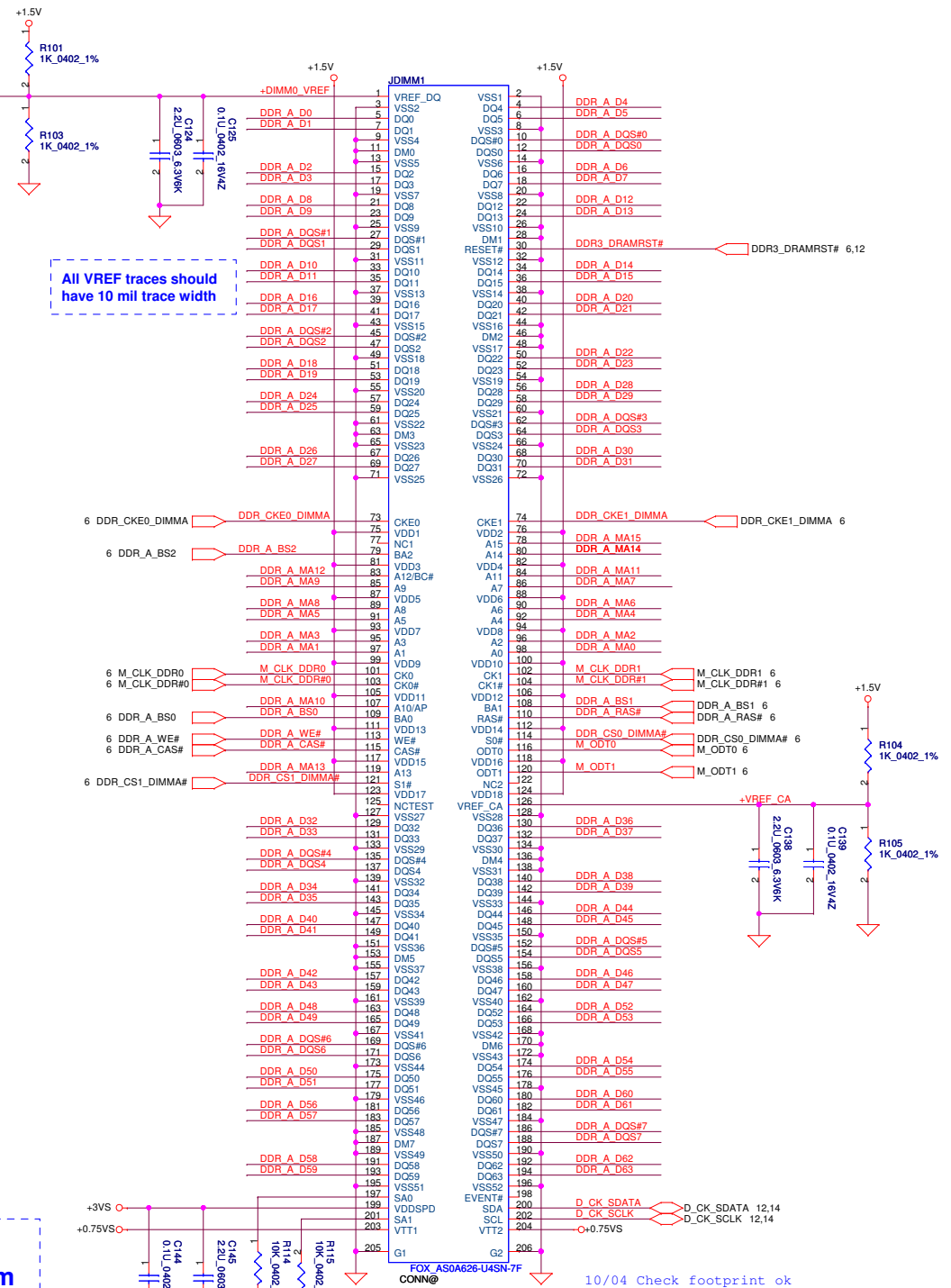


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								PROCESSOR(5/7) PWR,BYPASS			
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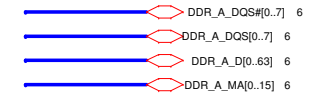




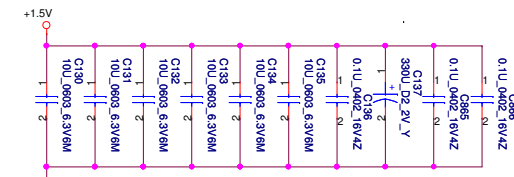
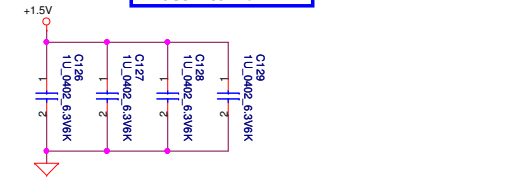
**All VREF traces should have 10 mil trace width**

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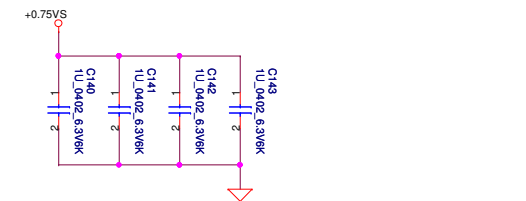
**DIMM A Reserve H:4mm**



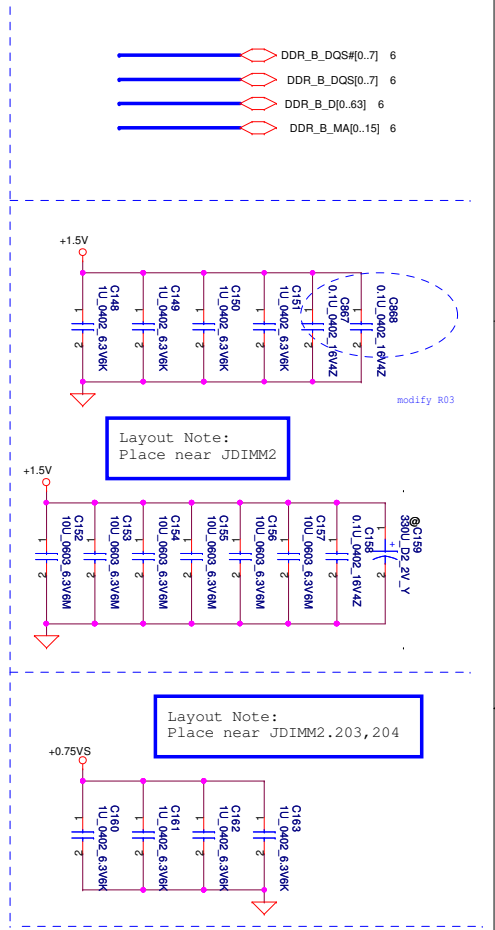
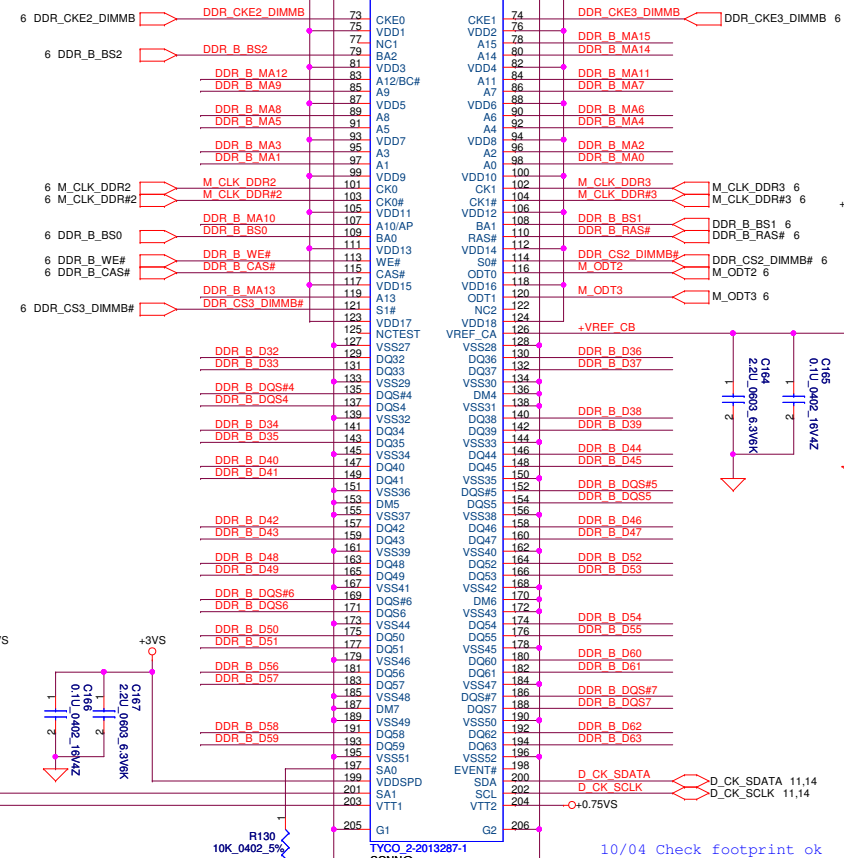
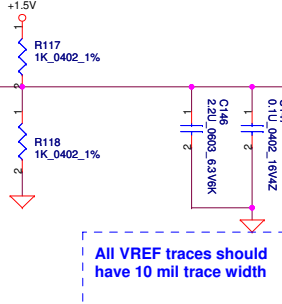
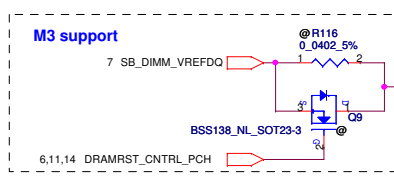
Layout Note:  
Place near JDIMM1



Layout Note:  
Place near JDIMM1.203,204

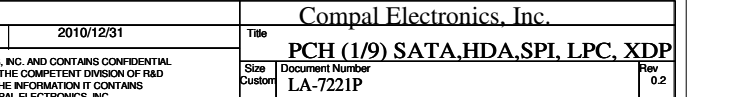
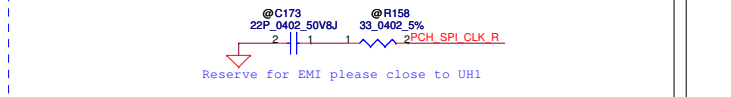
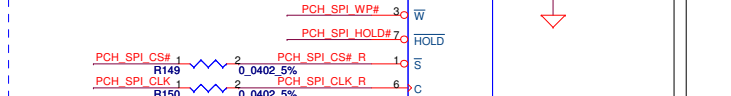
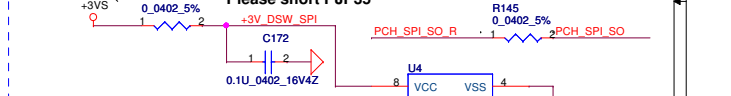
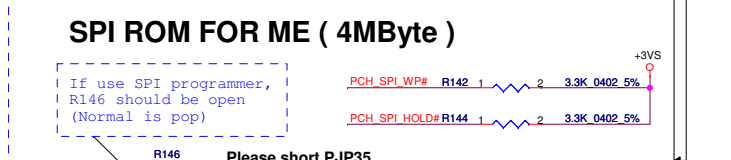
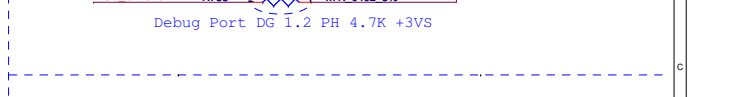
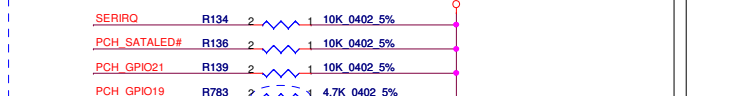
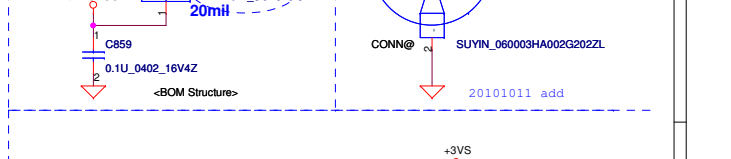
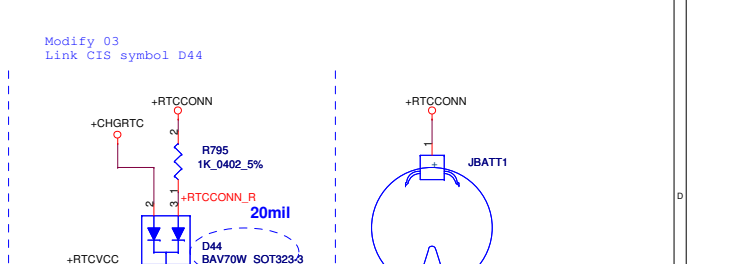
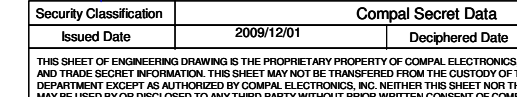
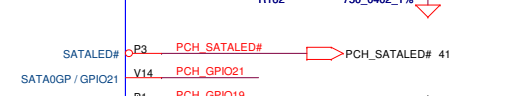
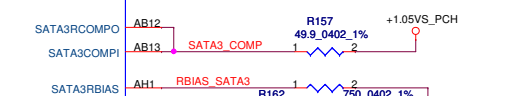
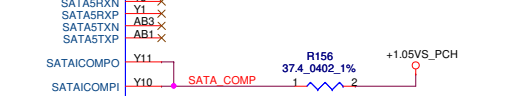
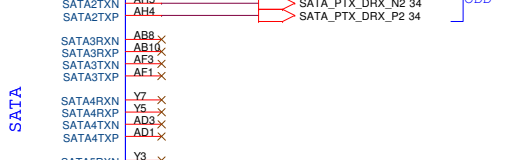
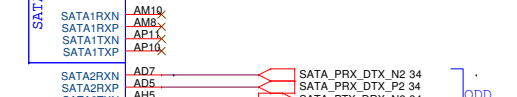
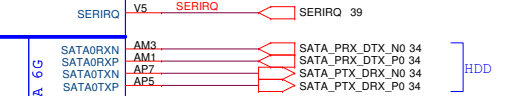
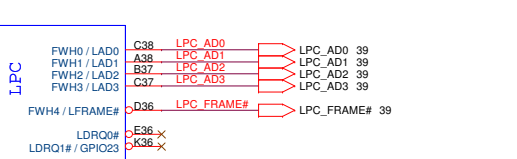
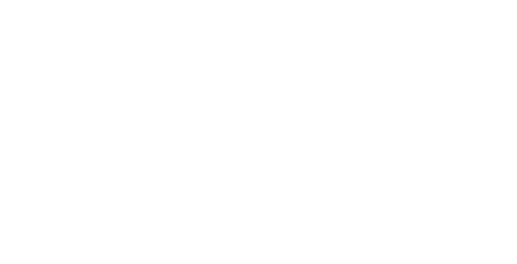
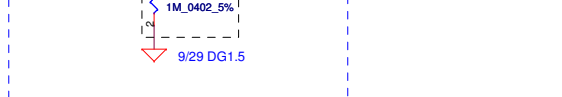
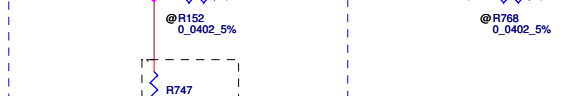
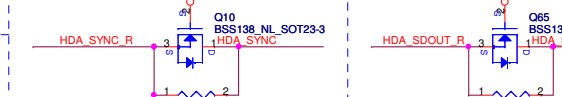
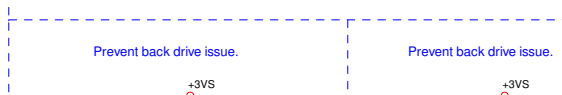
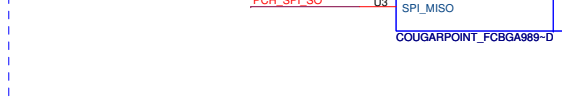
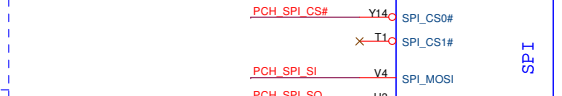
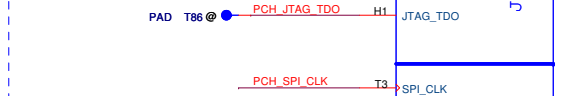
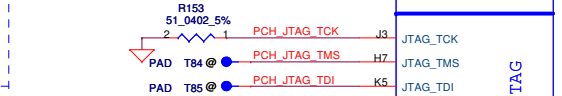
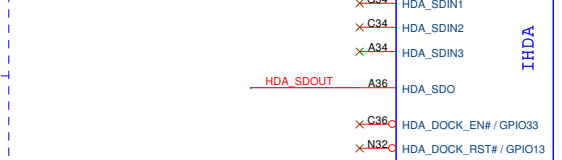
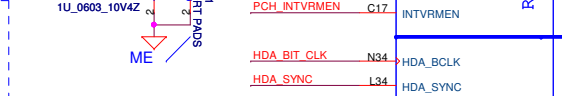
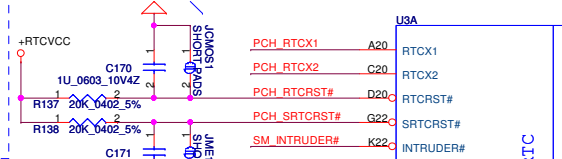
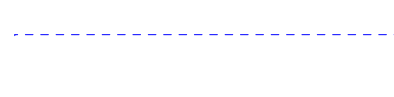
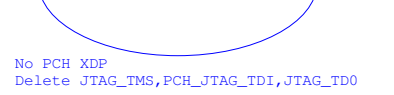
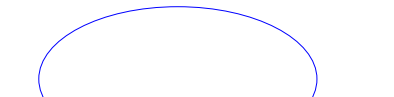
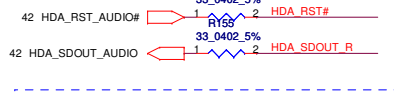
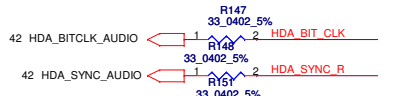
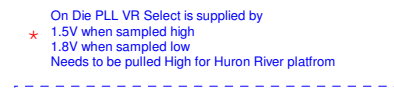
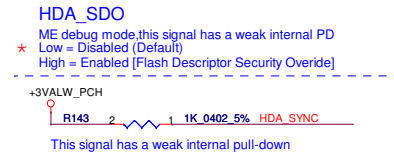
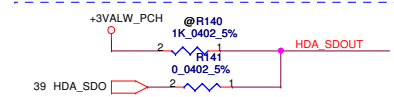
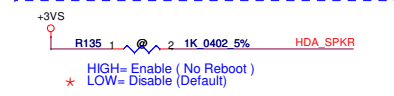
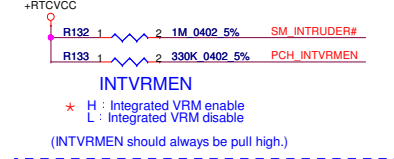
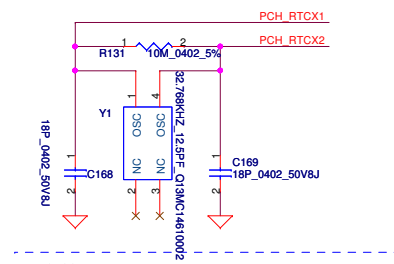


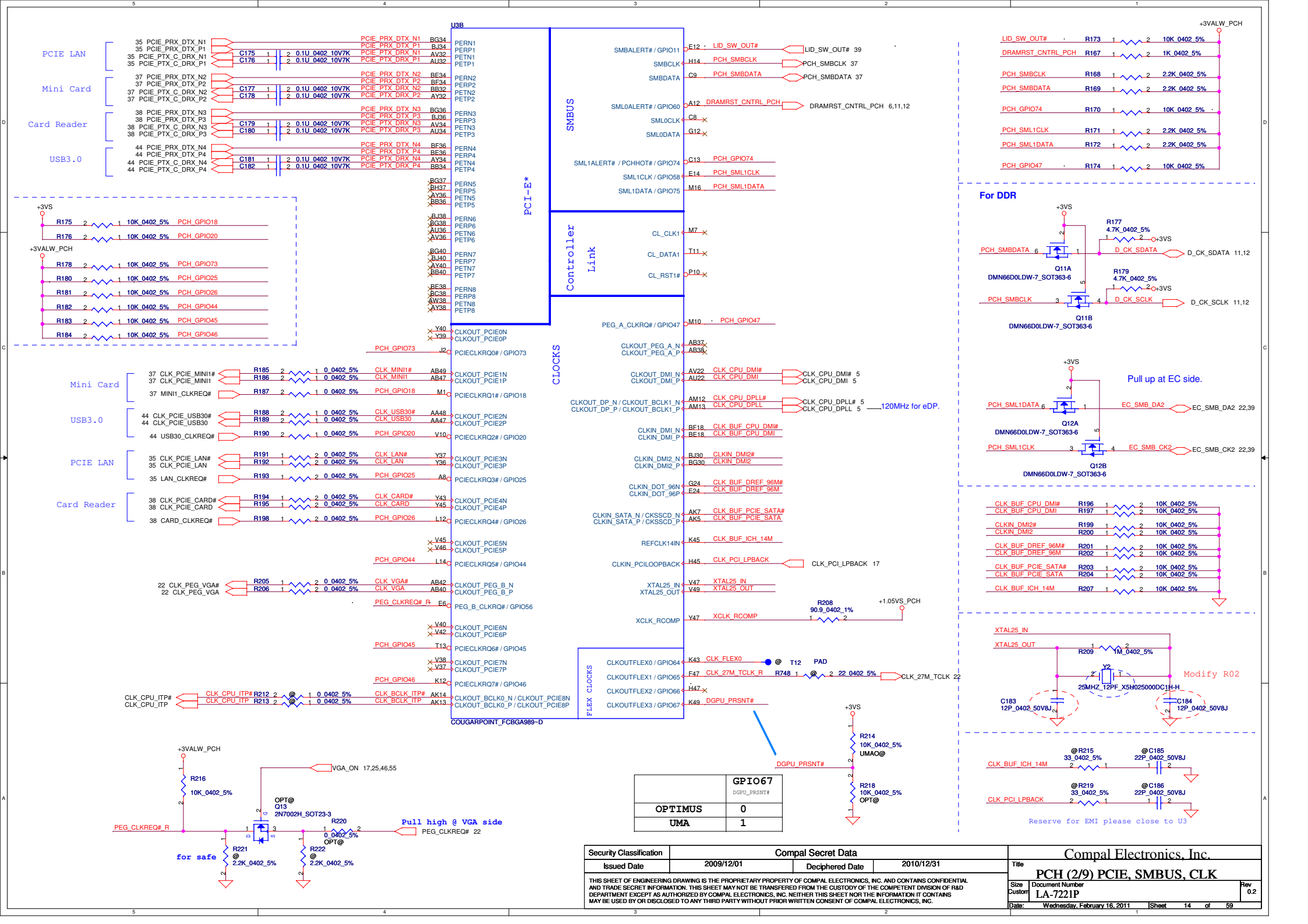
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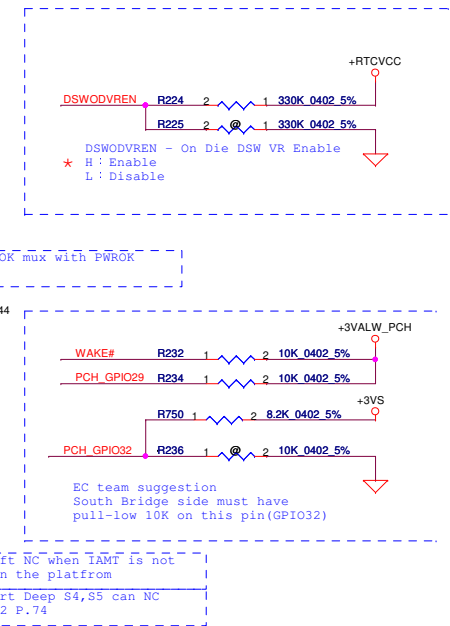
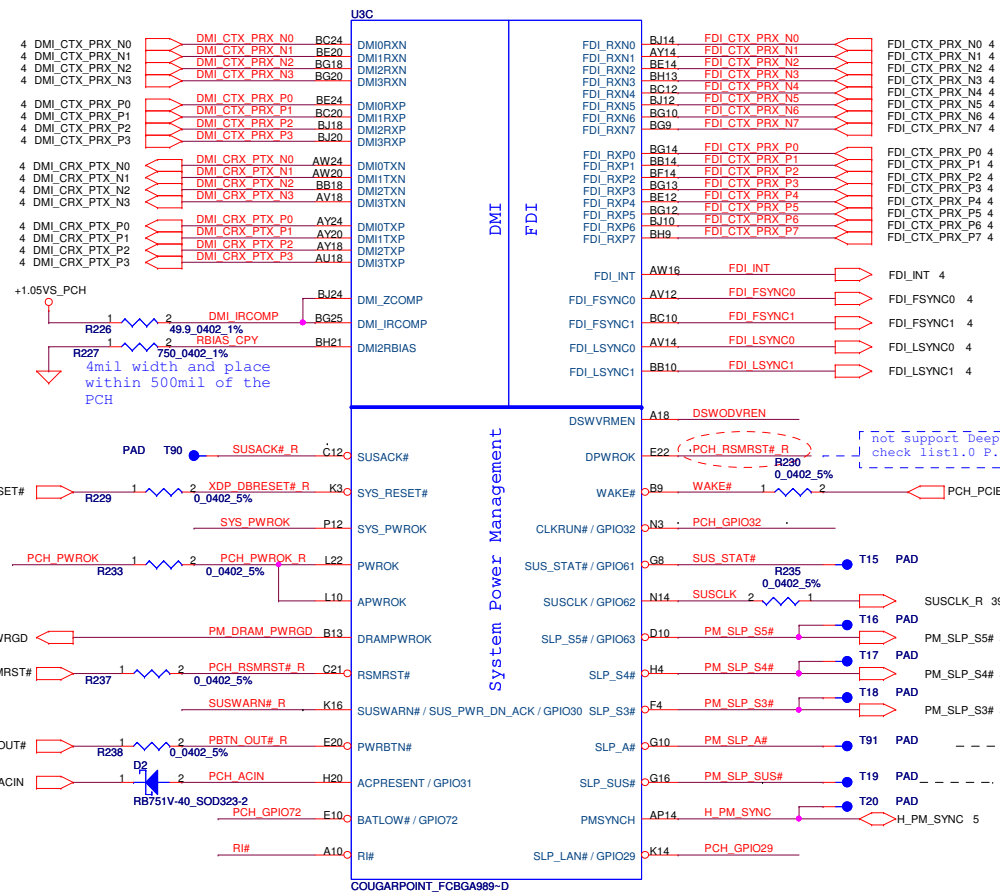
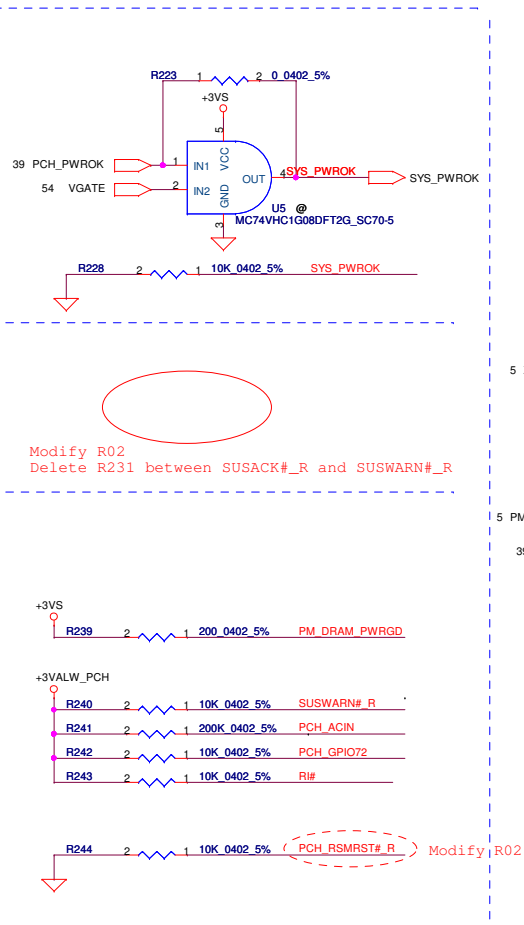


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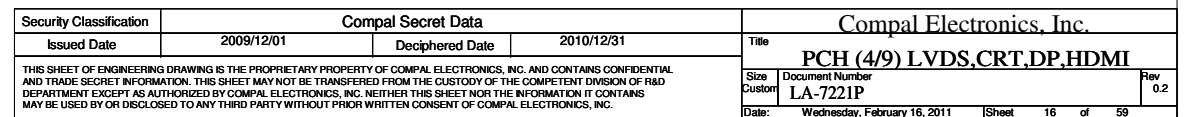
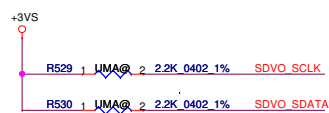




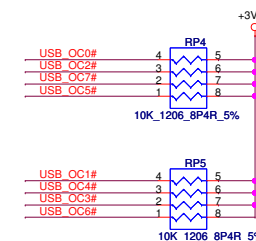
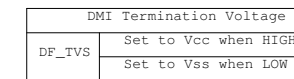
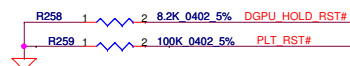


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Issued Date	2009/12/01	Deciphered Date	2010/12/31	Title PCH (3/9) DMI,FDI,PM,		
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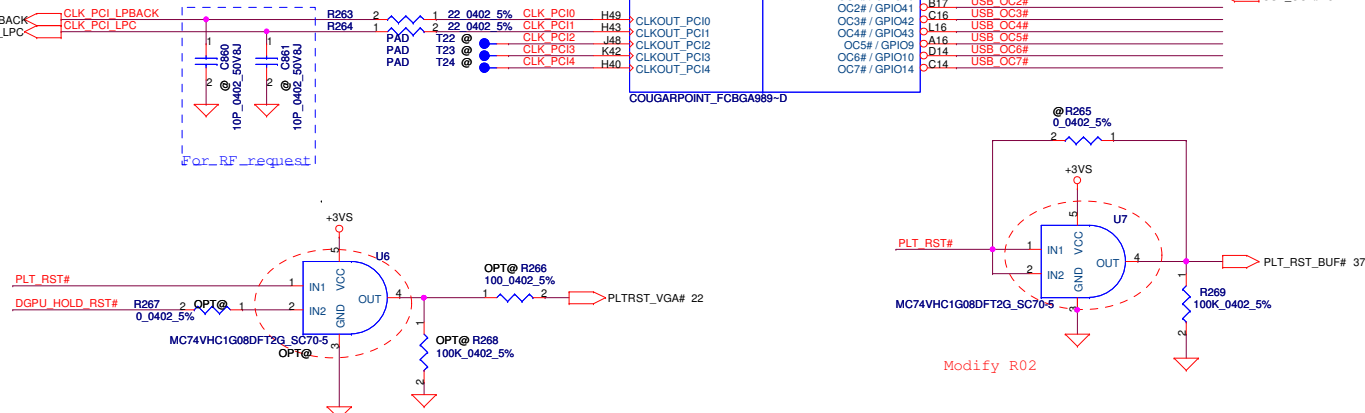






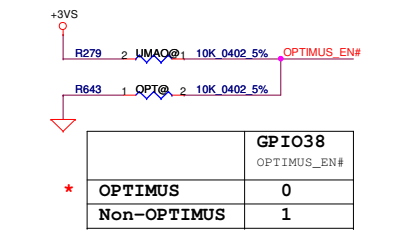


Boot BIOS Strap bit1 BBS1			
GNT1#/ GPIO51	Bit11	Bit10	Boot BIOS Destination
	0	1	Reserved
	1	0	PCI
	1	1	SPI
	0	0	LPC



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Title	PCH (5/9) PCI, USB, NVRAM		
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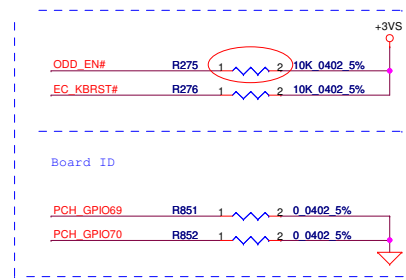
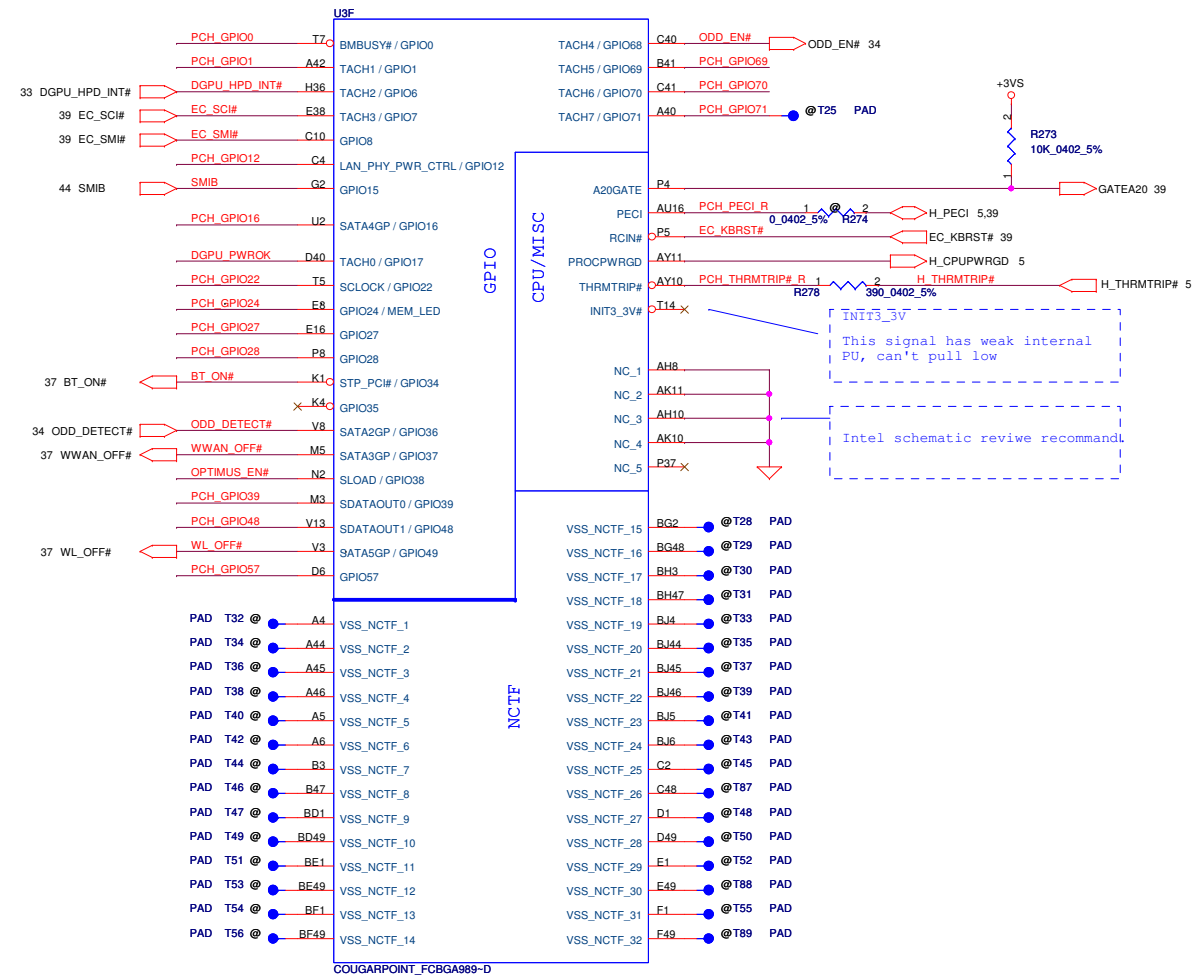
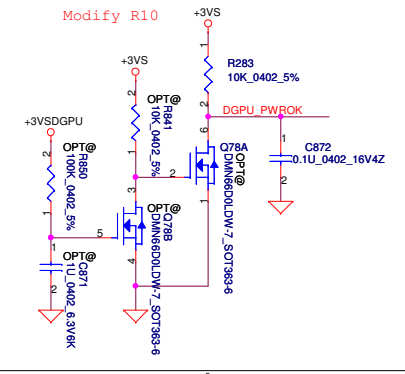
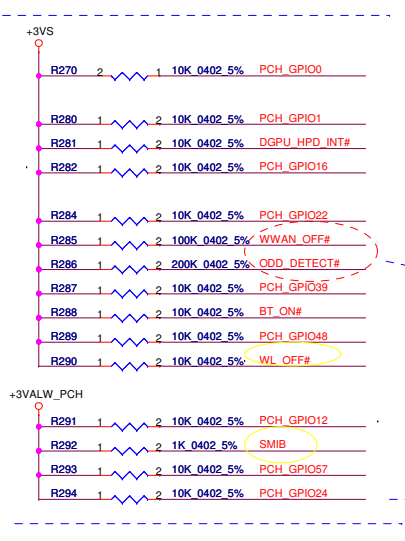
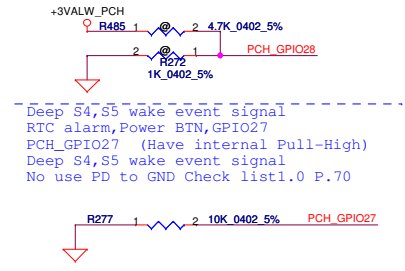


On-Die PLL Voltage Regulator

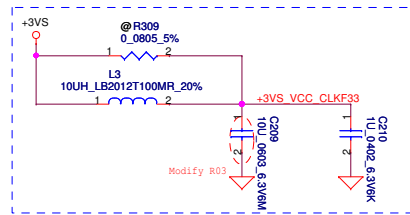
This signal has a weak internal pull up

\* H : On-Die PLL voltage regulator enable

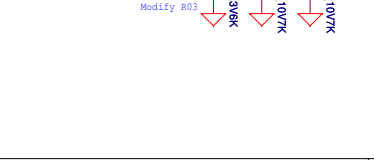
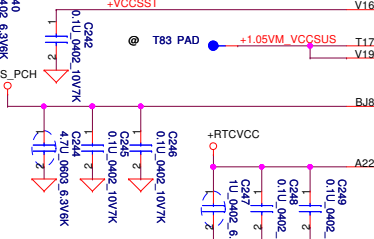
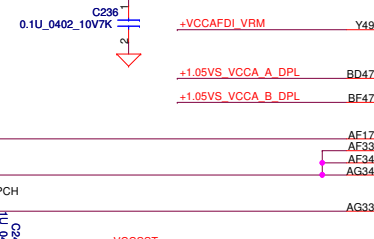
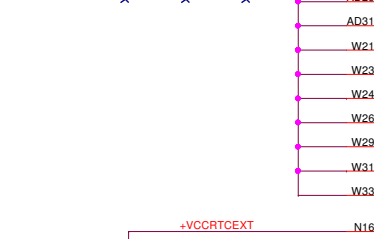
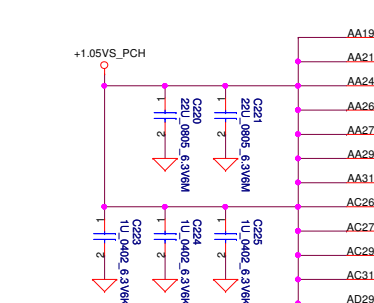
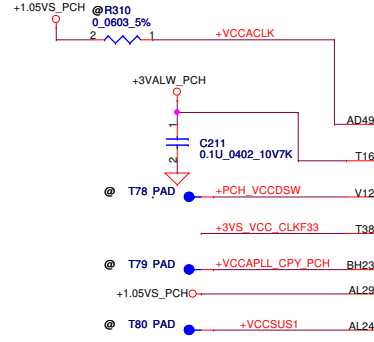
L : On-Die PLL Voltage Regulator disable







Have internal VRM



## POWER

### USB

### Clock and Miscellaneous

### PCI/GPIO/LPC

### SATA

### MISC

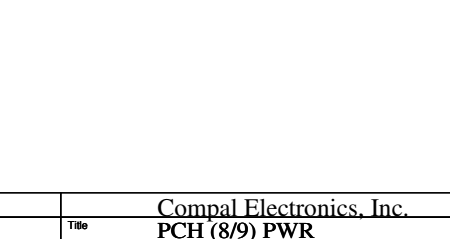
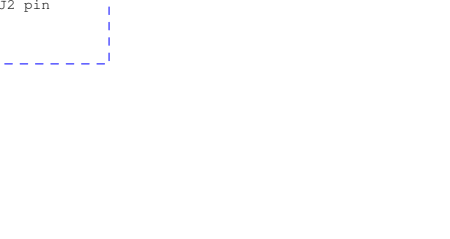
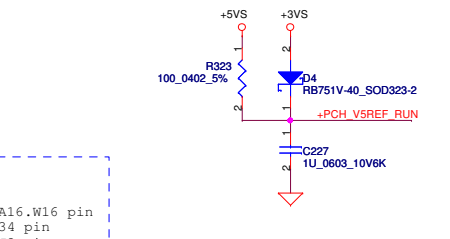
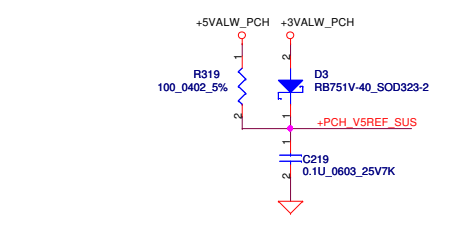
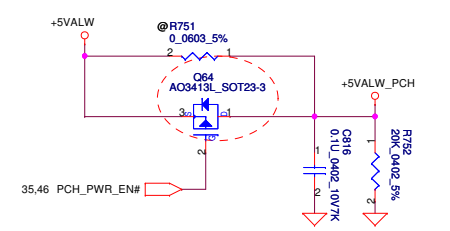
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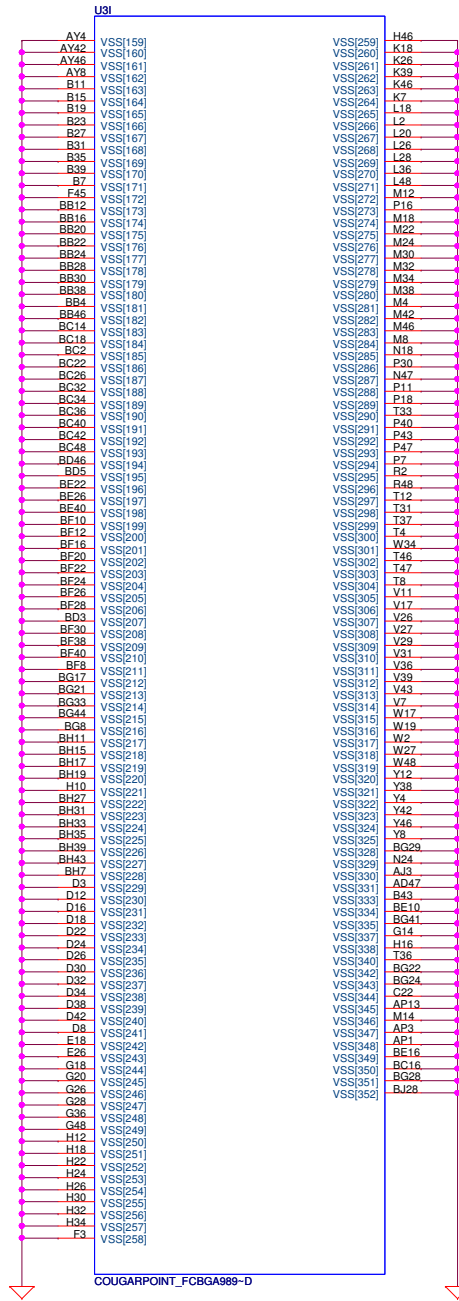
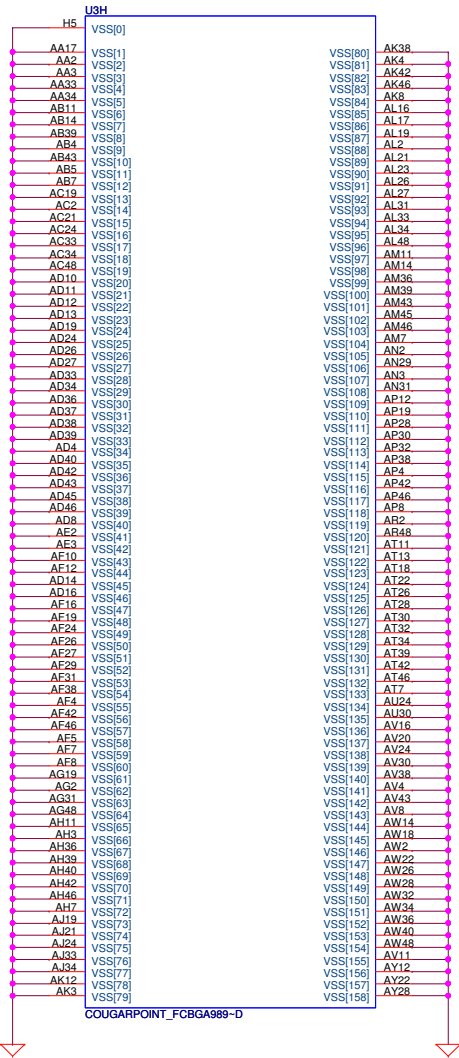
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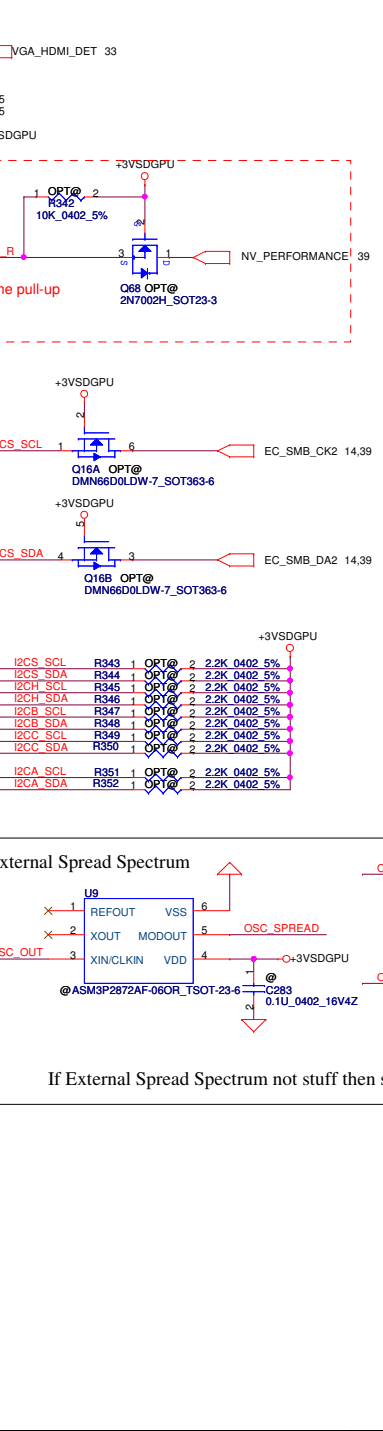
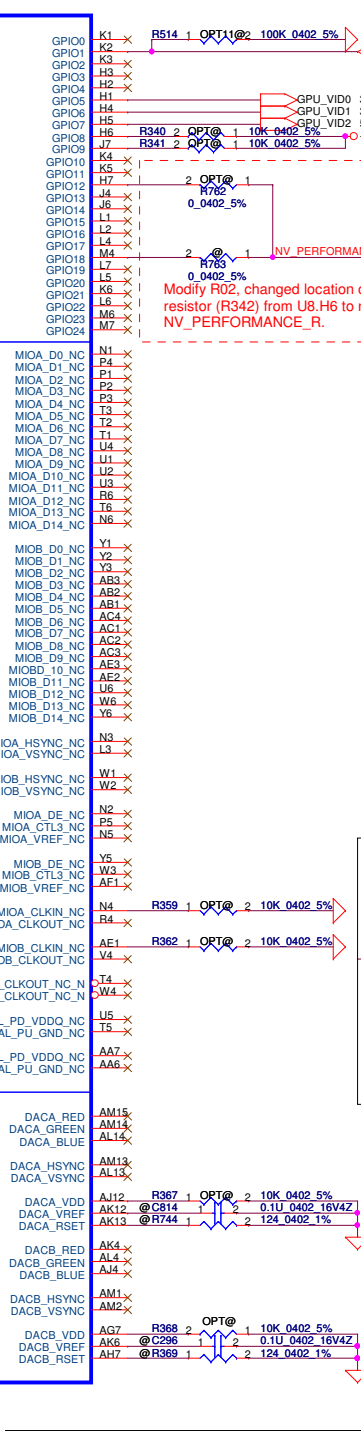
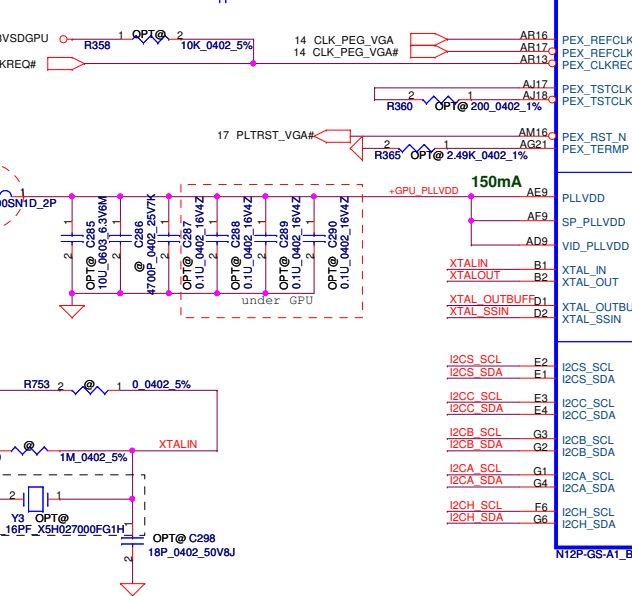
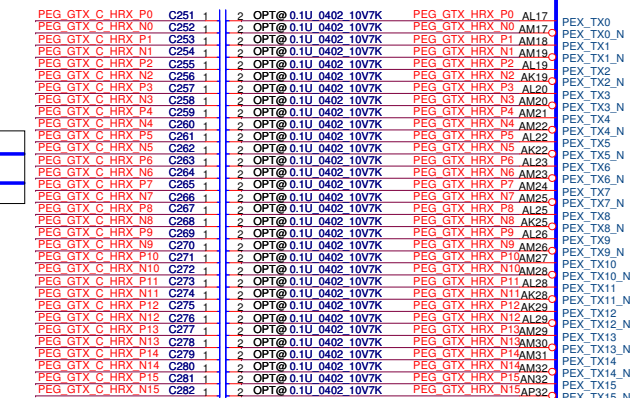
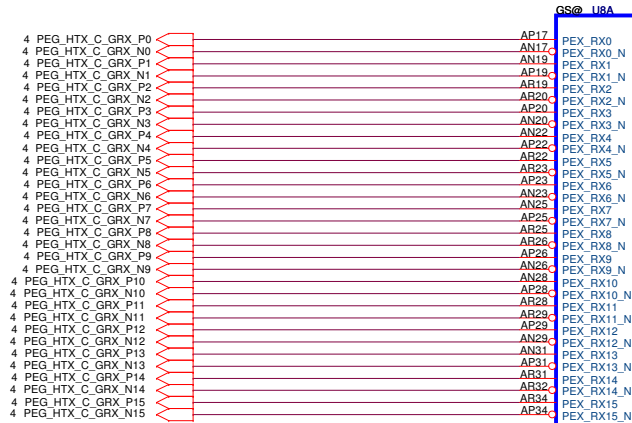
VCC3\_3 = 266mA detail waiting for newest spec  
VCCDMI = 42mA detail waiting for newest spec



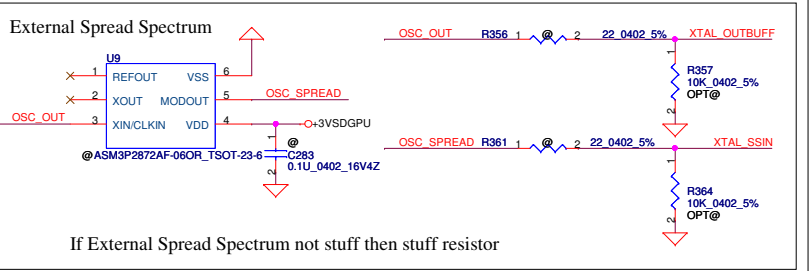
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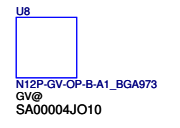




GPIO	I/O	FUNCTION
GPIO0	IN	HPD_C
GPIO5	OUT	GPU_VID0
GPIO6	OUT	GPU_VID1
GPIO7	OUT	GPU_VID2
GPIO8	IN	OVERT
GPIO9	IN	ALERT
GPIO12	IN	AC/DC detection
GPIO18	IN	Reserve for VPS

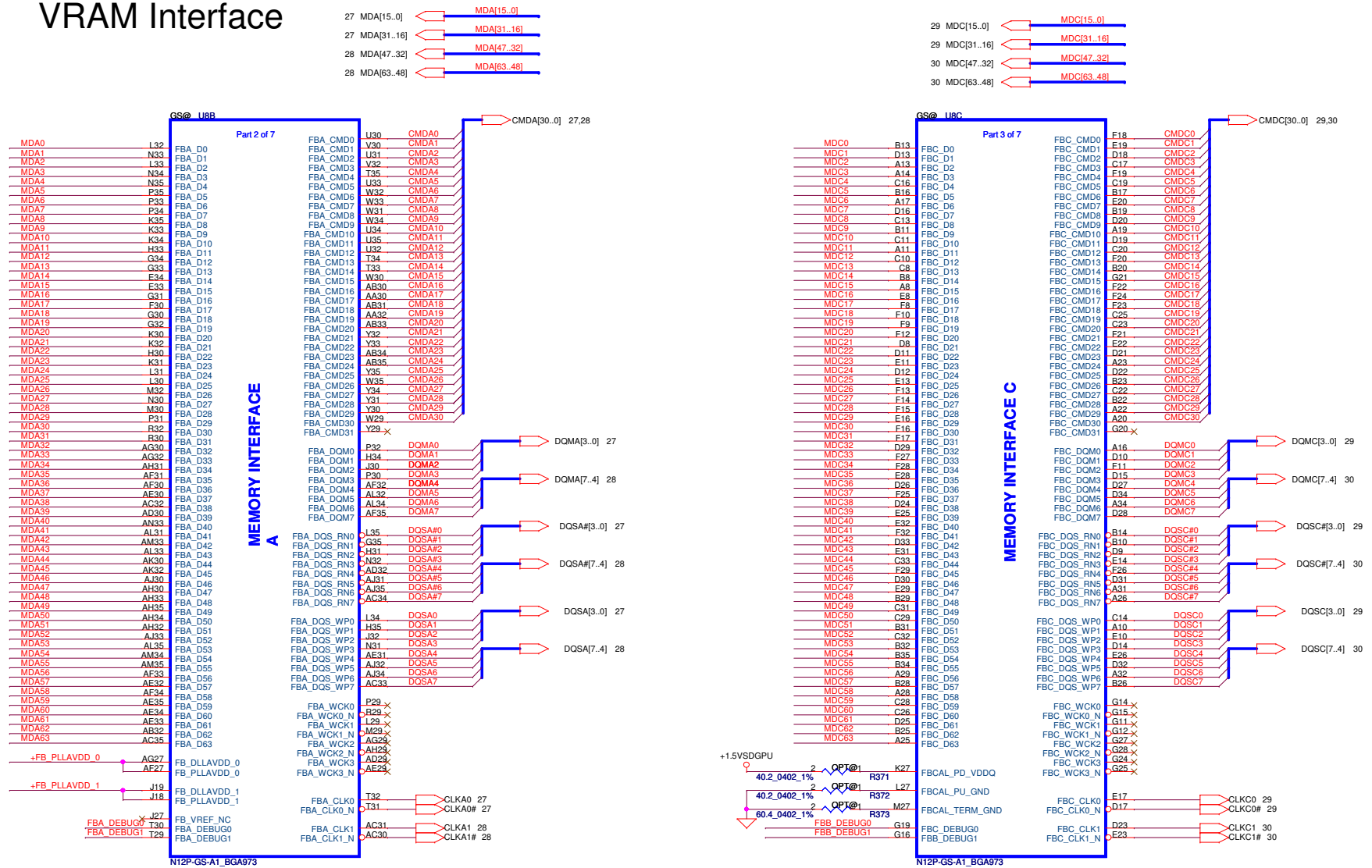


Option Component



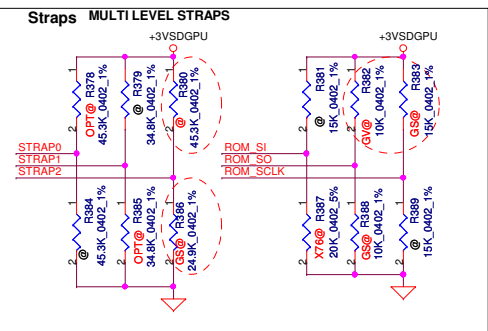


# VRAM Interface



11/8, For GB2-128(GS) & GB2b-128(GV) colayout.  
the circuit is for GB2b-128(GV-B) package.

```
N12P-GV QS DevID: 0x1050, detail
additional strap setting, please refer
to N12P-GV DG and PUN-05515-001_v03
1. ROM_SCLK: pull up 5K ohm.
2. STRAP2: pull down 5K ohm.
3. ROM_SO: pull up 10K ohm.
4. STRAP3: pull down 5K ohm.
5. STRAP4: pull down 10K ohm.
6. STRAP_REF2, need to stuff with 40K
ohm 1%.
7. PGOOD (pin E7) stuff 10K ohm.
```



N11P-GS	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung SA00004GS10	H 45K	L 35K	L 25K(GS@) L 5k (GV@)	L 20K	H (GV@) L (GS@)	H 15K(GS@) H 5K(GV@)
64MX16 Hynix SA000041S40	H 45K	L 35K	L 25K(GS@) L 5k (GV@)	L 15K	H (GV@) L (GS@)	H 15K(GS@) H 5K(GV@)
128MX16 Samsung SA00003MQ60	H 45K	L 35K	L 25K(GS@)	L 45K	H (GV@) L (GS@)	H 15K(GS@)
128MX16 Hynix SA00003VS10	H 45K	L 35K	L 25K(GS@)	L 35K	H (GV@) L (GS@)	H 15K(GS@)

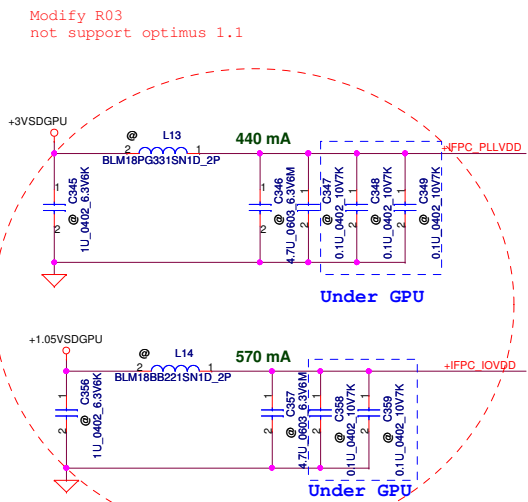
Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

GPU	DeviceID	ROM_SCLK	STRAP2
N12P-GS	0x0DF4	Pull up 15K	Pull down 25K
N12P-GE	0x0DF5	Pull up 15K	Pull down 30K
N12P-GV	0x1050	Pull up 5K	Pull down 5K

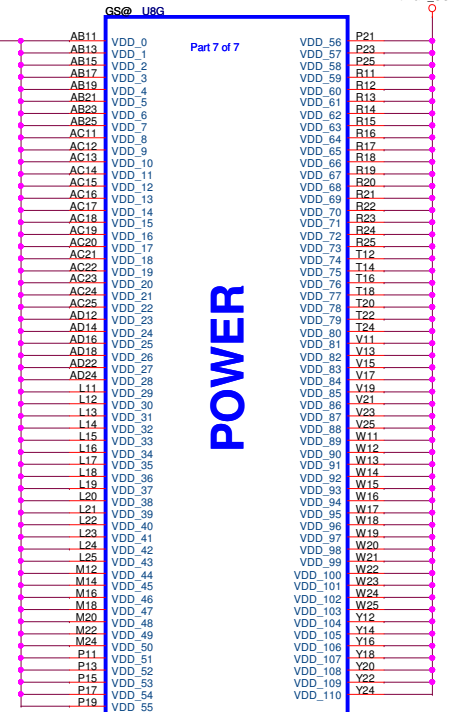
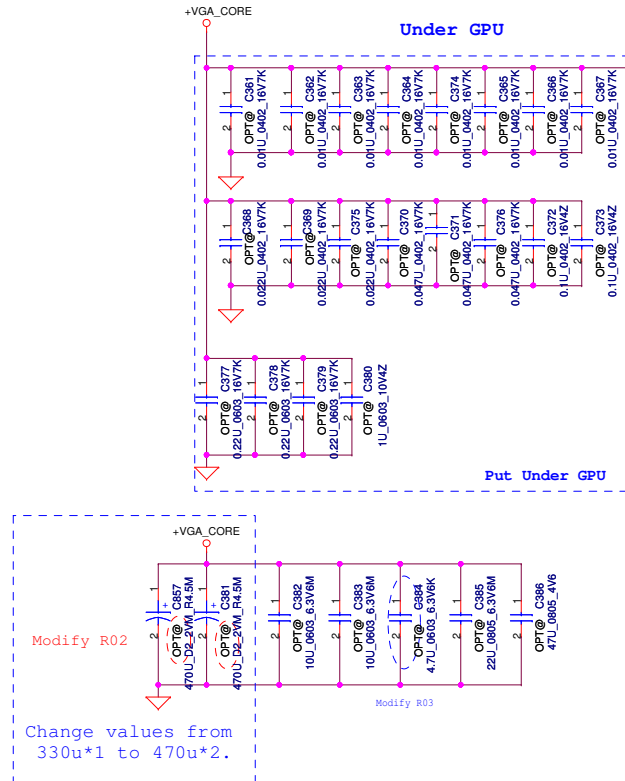
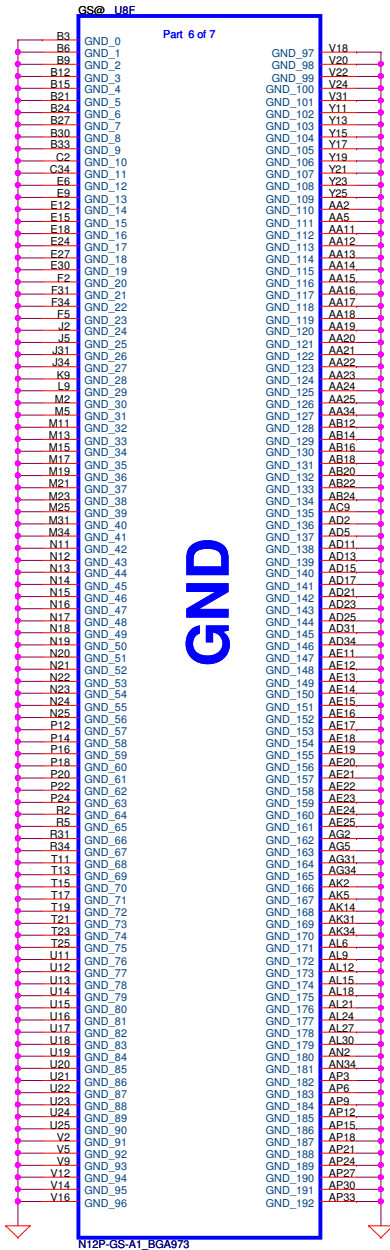
Hynix (900MHZ) 64MX16 H5TQ1G63DFR-11C SA000041S40	512MB	0010	PD 15K (SD034150280)
	1GB	0010	PD 15K (SD034150280)
Hynix 2G 128MX16 H5TQ2G63BFR-12C SA00003VS10	2GB	0110	PD 34.8k(SD034348280)
Samsung (900MHZ) 64MX16 K4W1G1646G-BC11 SA00004GS10	512MB	0011	PD 20K (SD028200280)
	1GB	0011	PD 20K (SD028200280)
Samsung 2G 128M16 K4W2G1646C-HC12 SA00003MQ60	2GB	0111	PD 45.3K(SD034453280)

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				Date:	Wednesday, February 16, 2011	Sheet



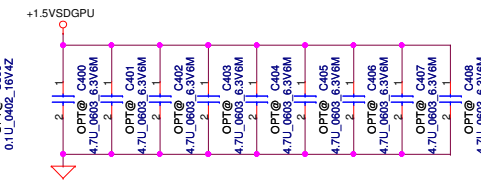
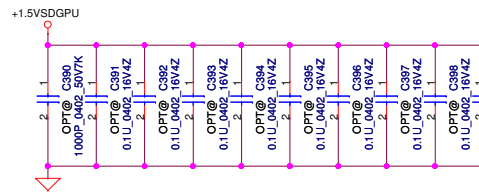
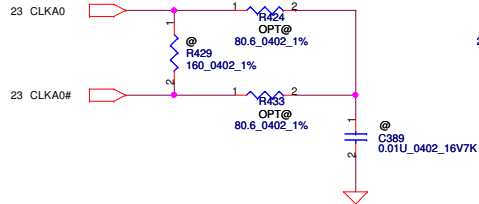


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**(The 512M DDR3\*4 are used at MEMORY INTERFACE A for GV)**



	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

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				Customer	LA-7221P	
Date:				Wednesday, February 16, 2011	Sheet	27 of 59

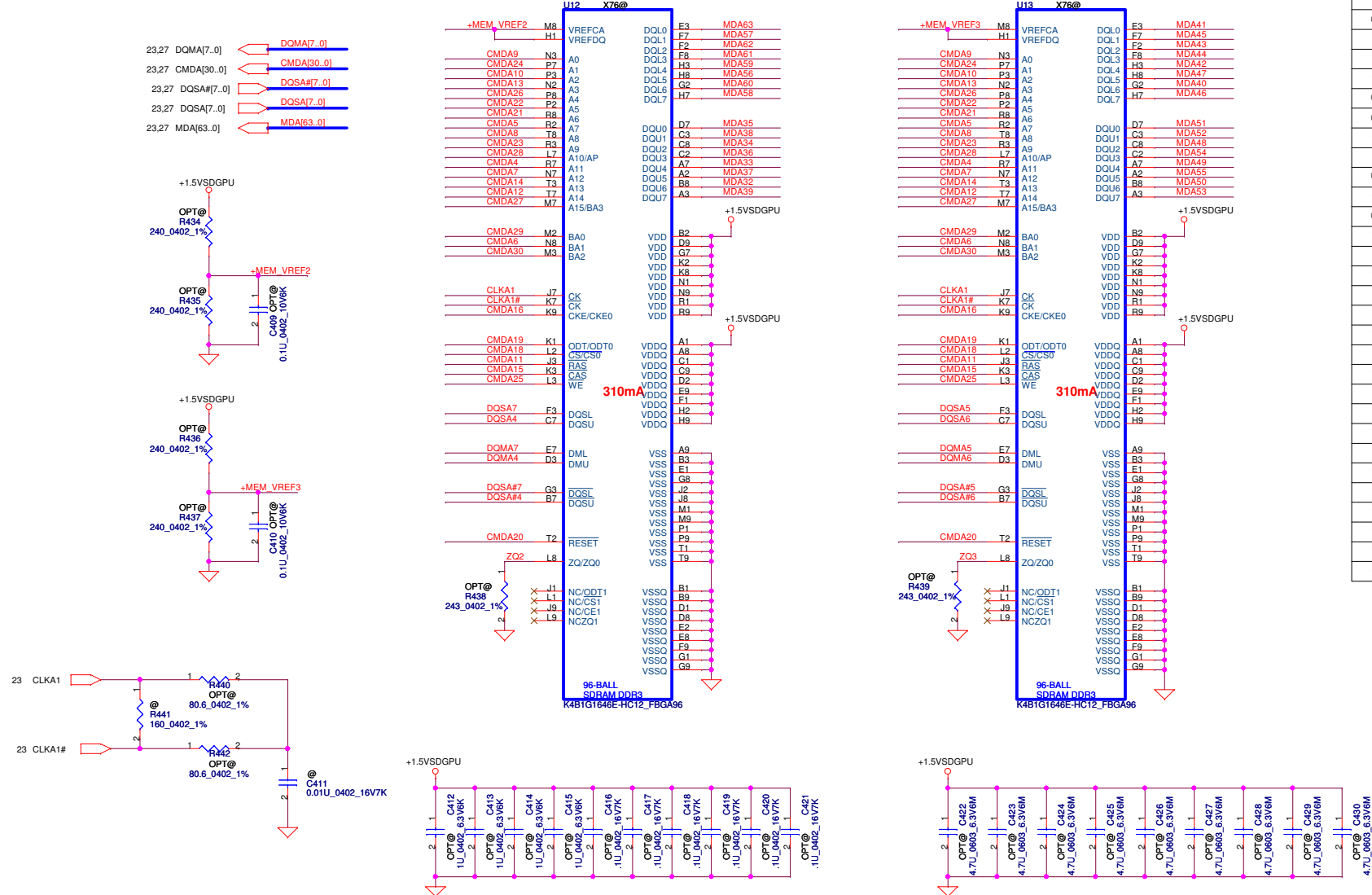
VRAM DDR3 chips (GS=1GB, GV=512M)

128Mx16 DDR3\*8==>2GB (GS)

64Mx16 DDR3\*8==>1GB (GS)

64Mx8 DDR3\*4==>512M

(The 512M DDR3\*4 are used at MEMORY INTERFACE A for GV)



Mode B Address	Mode C Address	0..31	32..63
CMD3	CMD0	CKE_L	
CMD8	CMD1	A8	A8
CMD2	CMD2	CS0_L#	
CMD21	CMD3	A7	A6
CMD24	CMD4	A2	A1
CMD23	CMD5	A11	A9
CMD26	CMD6	A5	A4
CMD7	CMD7	A0	A12
CMD15	CMD8	CAS*	CAS*
CMD13	CMD9	BA1	A3
CMD4	CMD10	A9	A11
CMD18	CMD11		CS0_H#
CMD29	CMD12	BA0	BA0
CMD27	CMD13	BA2	A15
CMD6	CMD14	A3	BA1
CMD17	CMD15		CS1_H#
CMD19	CMD16		ODT_H
CMD22	CMD17	A4	A5
CMD12	CMD18	A13	A14
CMD28	CMD19	WE*	A10
CMD10	CMD20	A1	A2
CMD25	CMD21	A10	WE*
CMD9	CMD22	A12	A0
CMD1	CMD23	CS1_L#	
CMD11	CMD24	RAS*	RAS*
CMD0	CMD25	ODT_L	
CMD5	CMD26	A6	A7
CMD16	CMD27		CKE_H
CMD20	CMD28	RST	RST
CMD14	CMD29	A14	A13
CMD30	CMD30	A15	BA2
CMD31	Not Available		
		LOW	HIGH

# VRAM DDR3 chips (GS=1GB, GV=512M)

128Mx16 DDR3\*8==>2GB (GS)

64Mx16 DDR3\*8==>1GB (GS)

Mode E Address	Mode C Address	0..31	32..63
CMD3	CMD0	CKE_L	
CMD8	CMD1	A8	A8
CMD2	CMD2	CS0_L#	
CMD21	CMD3	A7	A6
CMD24	CMD4	A2	A1
CMD23	CMD5	A11	A9
CMD26	CMD6	A5	A4
CMD7	CMD7	A0	A12
CMD15	CMD8	CAS*	CAS*
CMD13	CMD9	BA1	A3
CMD4	CMD10	A9	A11
CMD18	CMD11		CS0_H#
CMD29	CMD12	BA0	BA0
CMD27	CMD13	BA2	A15
CMD6	CMD14	A3	BA1
CMD17	CMD15		CS1_H#
CMD19	CMD16		ODT_H
CMD22	CMD17	A4	A5
CMD12	CMD18	A13	A14
CMD28	CMD19	WE*	A10
CMD10	CMD20	A1	A2
CMD25	CMD21	A10	WE*
CMD9	CMD22	A12	A0
CMD1	CMD23	CS1_L#	
CMD11	CMD24	RAS*	RAS*
CMD0	CMD25	ODT_L	
CMD5	CMD26	A6	A7
CMD16	CMD27		CKE_H
CMD20	CMD28	RST	RST
CMD14	CMD29	A14	A13
CMD30	CMD30	A15	BA2
CMD31	Not Available		
		LOW	HIGH

	Command Bit	Default Pull-downs
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

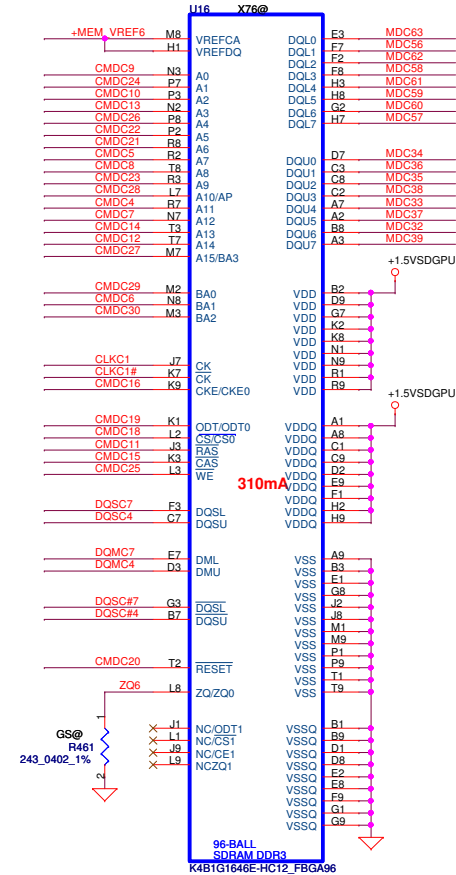
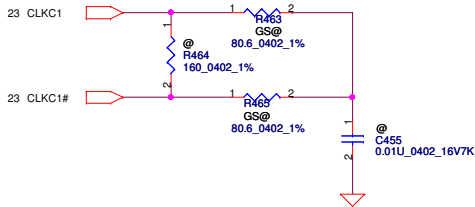
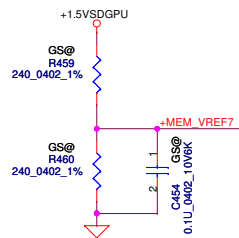
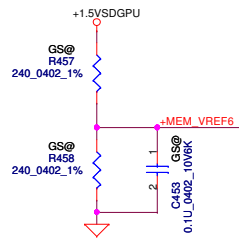
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				Size	Document Number	Rev
				Custom	LA-7221P	0.2
				Date:	Wednesday, February 16, 2011	Sheet 29 of 59

# VRAM DDR3 chips (GS=1GB, GV=512M)

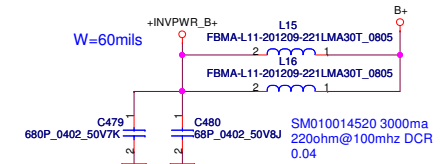
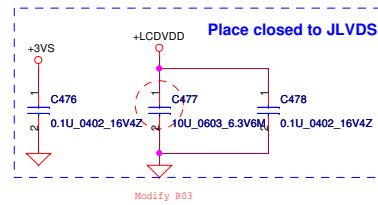
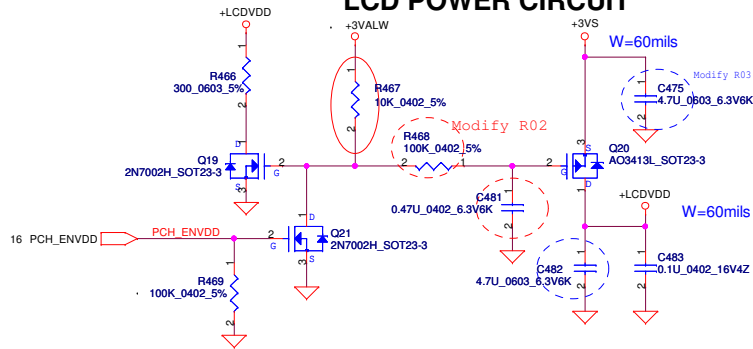
128Mx16 DDR3\*8==>2GB (GS)

64Mx16 DDR3\*8==>1GB (GS)

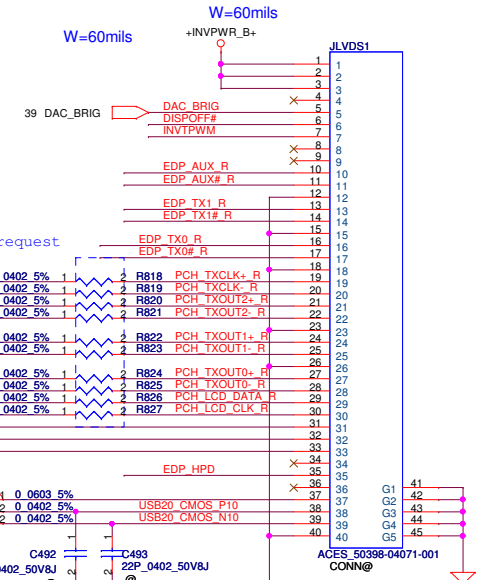
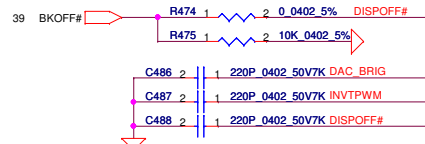
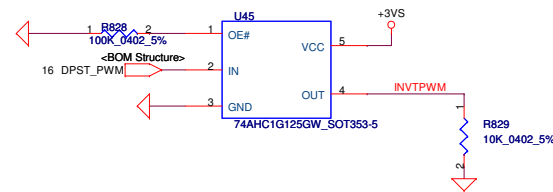
23,29 DQMC[7..0] ← DQMC[7..0]  
23,29 CMD[30..0] ← CMD[30..0]  
23,29 DQSC[7..0] ← DQSC[7..0]  
23,29 DQSC[7..0] ← DQSC[7..0]  
23,29 MDC[63..0] ← MDC[63..0]



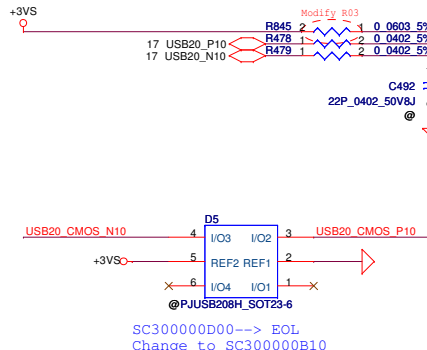
# LCD POWER CIRCUIT



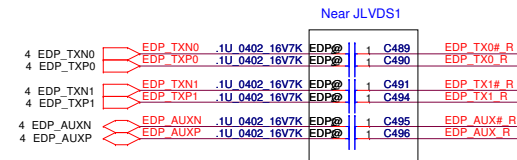
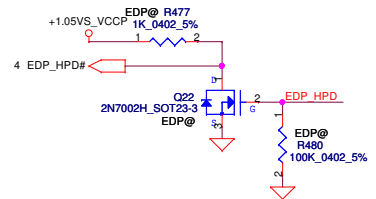
# LCD/LED PANEL Conn.



Modify R02  
PCH\_LCD\_CLK & PCH\_LCD\_DATA  
Pull high at PCH side.

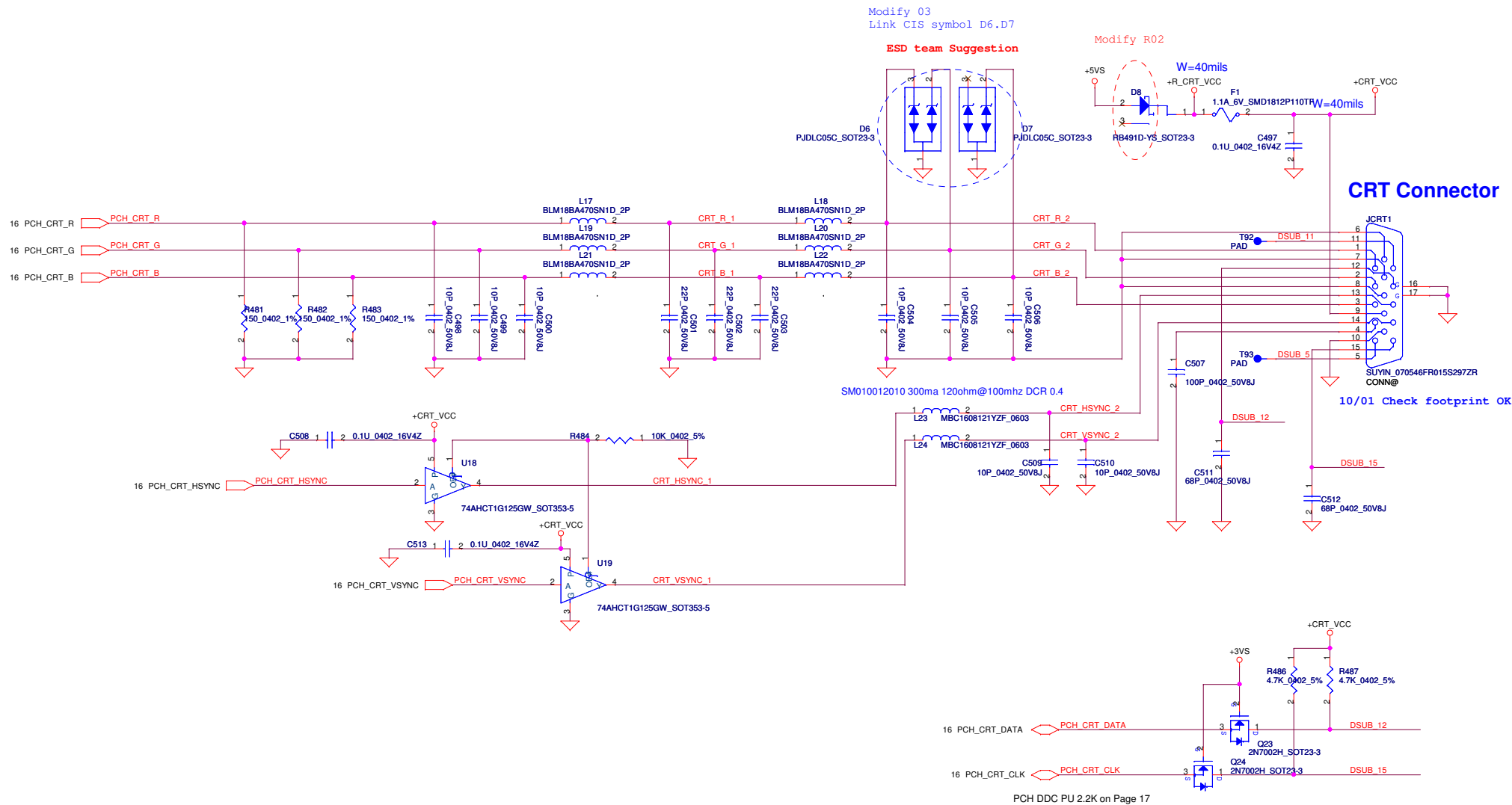


# eDP



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Date: Wednesday, February 16, 2011				Sheet 31 of 59

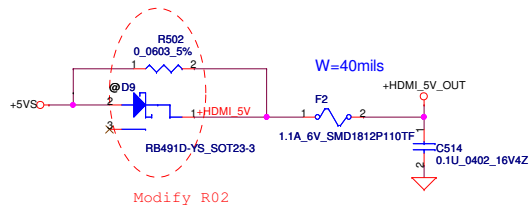




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Issued Date				2009/08/01		Deciphered Date		2010/08/01		Title	
										CRT Connector	
										Size	
										Document Number	
										LA-7221P	
										Rev	
										0.2	
										Date	
										Wednesday, February 16, 2011	
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										32 of 59	

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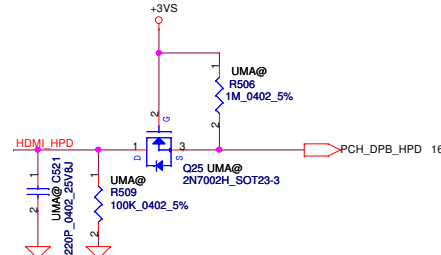
### UMA & Optimus 1.0

16 PCH_DPB_N0	C515	UMA@	2	1	1U	0402	16V7K	HDMI TX2-
16 PCH_DPB_P0	C516	UMA@	2	1	1U	0402	16V7K	HDMI TX2+
16 PCH_DPB_N1	C517	UMA@	2	1	1U	0402	16V7K	HDMI TX1-
16 PCH_DPB_P1	C518	UMA@	2	1	1U	0402	16V7K	HDMI TX1+
16 PCH_DPB_N2	C519	UMA@	2	1	1U	0402	16V7K	HDMI TX0-
16 PCH_DPB_P2	C520	UMA@	2	1	1U	0402	16V7K	HDMI TX0+
16 PCH_DPB_N3	C522	UMA@	2	1	1U	0402	16V7K	HDMI CLK-
16 PCH_DPB_P3	C523	UMA@	2	1	1U	0402	16V7K	HDMI CLK+

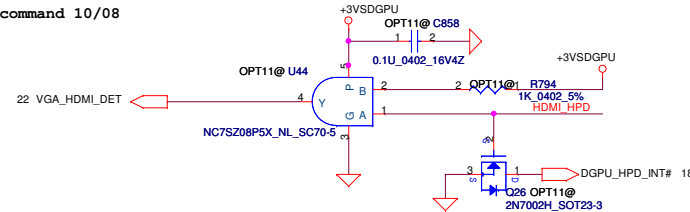
### Optimus 1.1

24 VGA_HDMI_TXD2-	C524	OPT11@	2	1	1U	0402	16V7K	HDMI TX2-
24 VGA_HDMI_TXD2+	C525	OPT11@	2	1	1U	0402	16V7K	HDMI TX2+
24 VGA_HDMI_TXD1-	C526	OPT11@	2	1	1U	0402	16V7K	HDMI TX1-
24 VGA_HDMI_TXD1+	C527	OPT11@	2	1	1U	0402	16V7K	HDMI TX1+
24 VGA_HDMI_TXD0-	C528	OPT11@	2	1	1U	0402	16V7K	HDMI TX0-
24 VGA_HDMI_TXD0+	C529	OPT11@	2	1	1U	0402	16V7K	HDMI TX0+
24 VGA_HDMI_TXC-	C530	OPT11@	2	1	1U	0402	16V7K	HDMI CLK-
24 VGA_HDMI_TXC+	C531	OPT11@	2	1	1U	0402	16V7K	HDMI CLK+

### UMA/OPT1.0

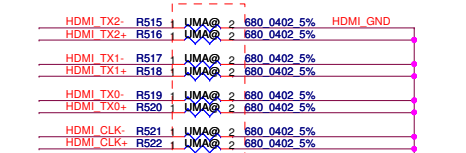
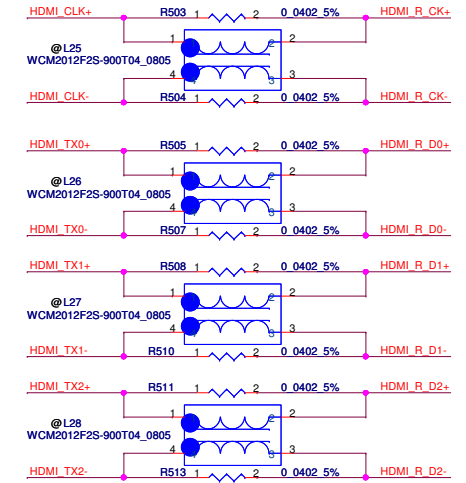


### NVIDIA Recommend 10/08 OPT1.1



Modify 03  
Link CIS symbol L25.L26.L27.L28

SM070001310 400ma 90ohm@100mhz DCR 0.3

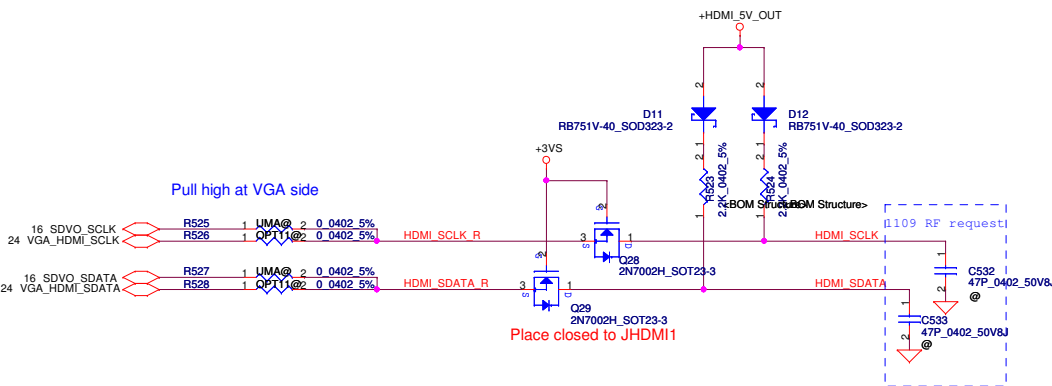


Optimus 1.0--> 680\_0402\_5%  
Optimus 1.1--> 499\_0402\_1%

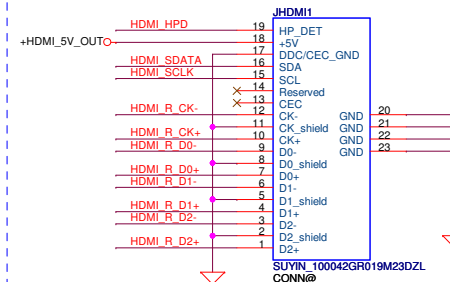
### Optimus 1.1 Option Component

R515	2	OPT11@	499	0402	1%
R516	2	OPT11@	499	0402	1%
R517	2	OPT11@	499	0402	1%
R518	2	OPT11@	499	0402	1%
R519	2	OPT11@	499	0402	1%
R520	2	OPT11@	499	0402	1%
R521	2	OPT11@	499	0402	1%
R522	2	OPT11@	499	0402	1%

Pull high at VGA side



### HDMI connector



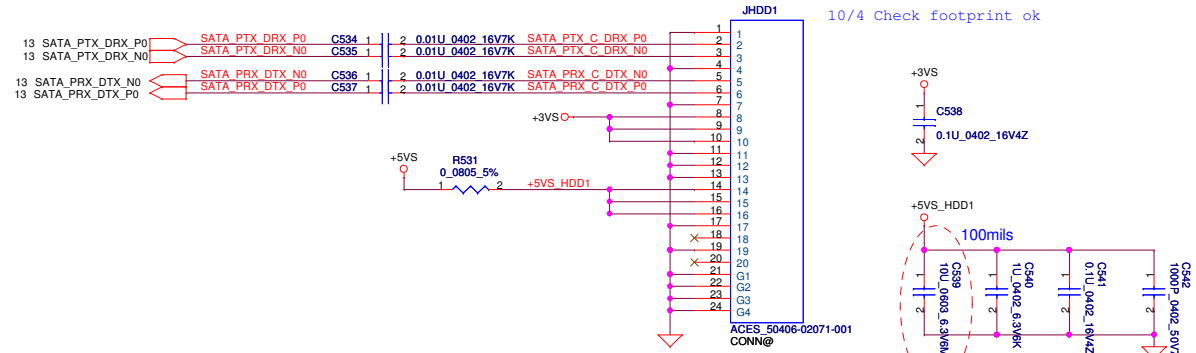
10/13 Link CIS symbol OK!

Modify R02  
SDVO\_CTRL.DATA strap pull high at PCH side

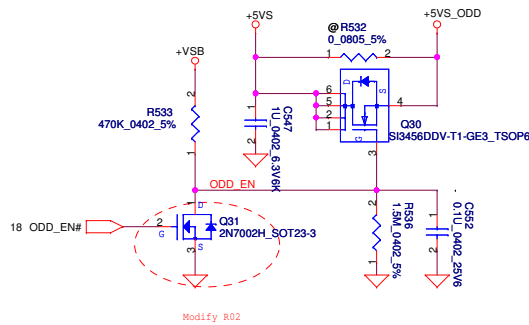
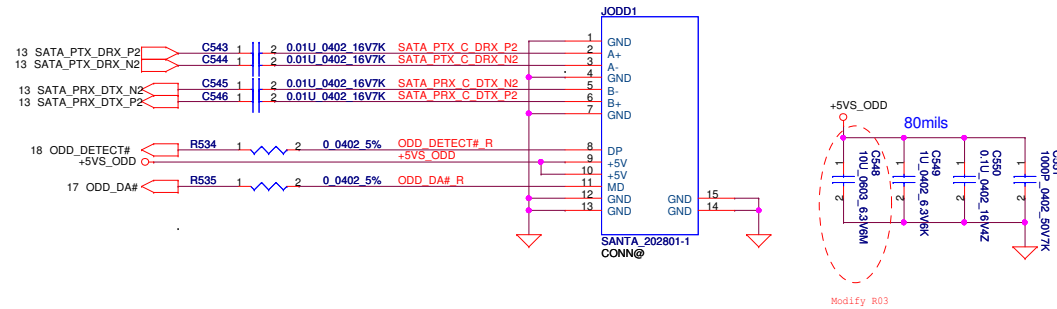
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Size	Custom	Document Number	LA-7221P	Rev
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## SATA HDD1 Conn.

CL 4.0 mm



## SATA ODD Conn.

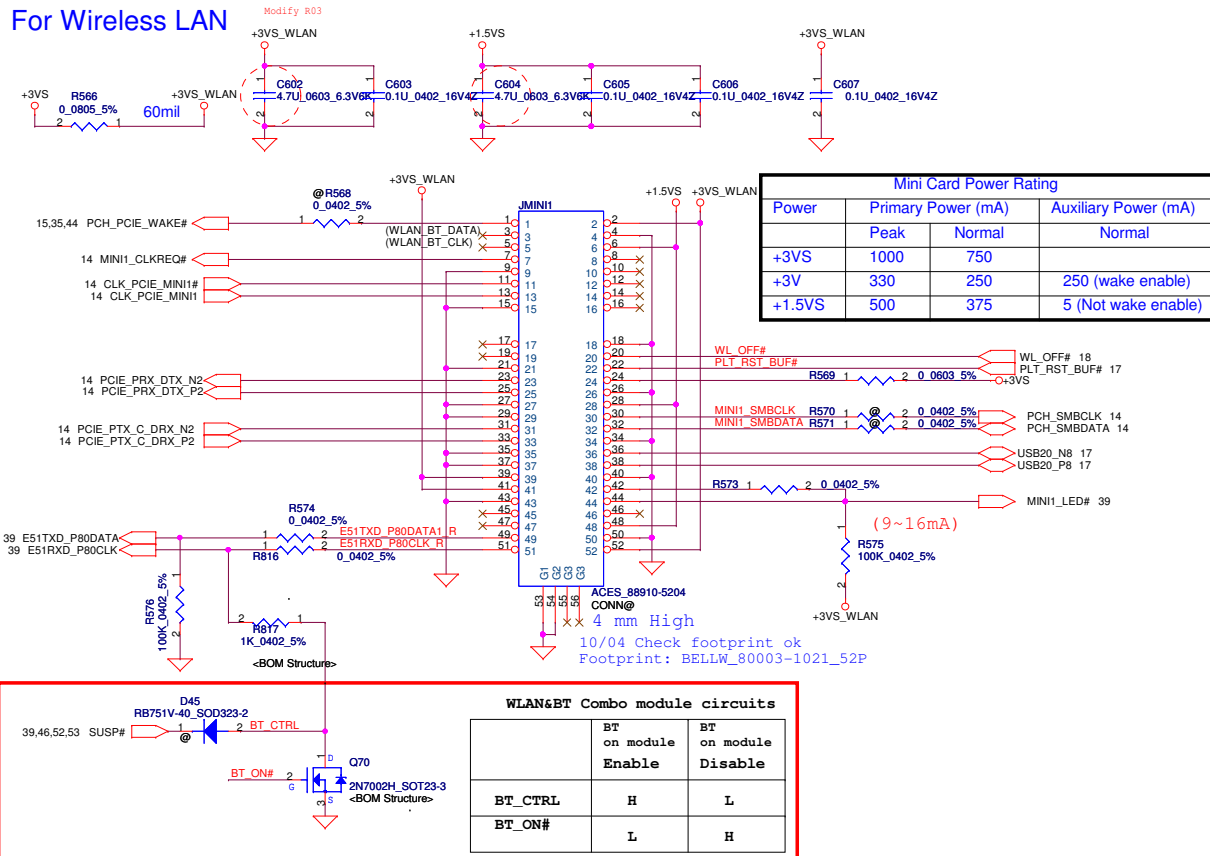


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				Size		Document Number		Rev 0.2
				Custom		LA-7221P		
				Date:		Wednesday, February 16, 2011		
				Sheet		34 of 59		

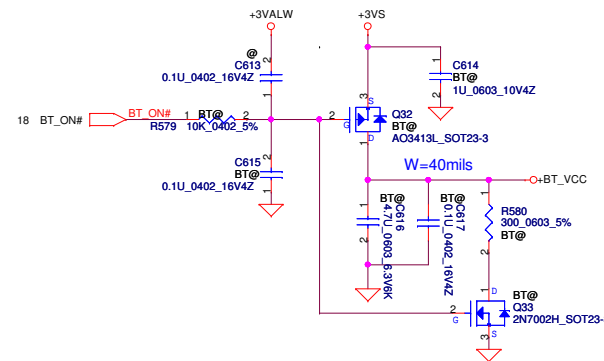
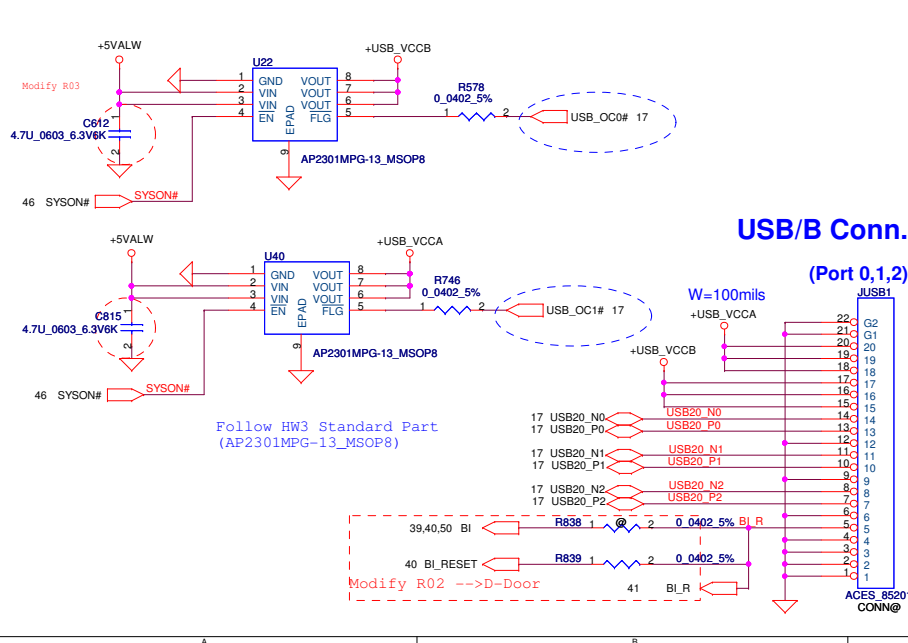
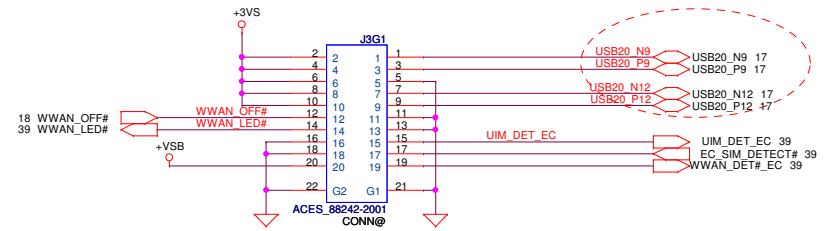
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/08/10	Deciphered Date	2010/08/01	Title	LAN Board AR8151 RevB
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				Customer	0.2
				Date: Wednesday, February 16, 2011         Sheet 35 of 59	



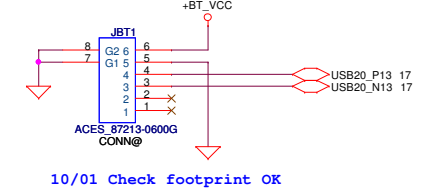
## For Wireless LAN



## For 3G / GPS To 3G Module Connect

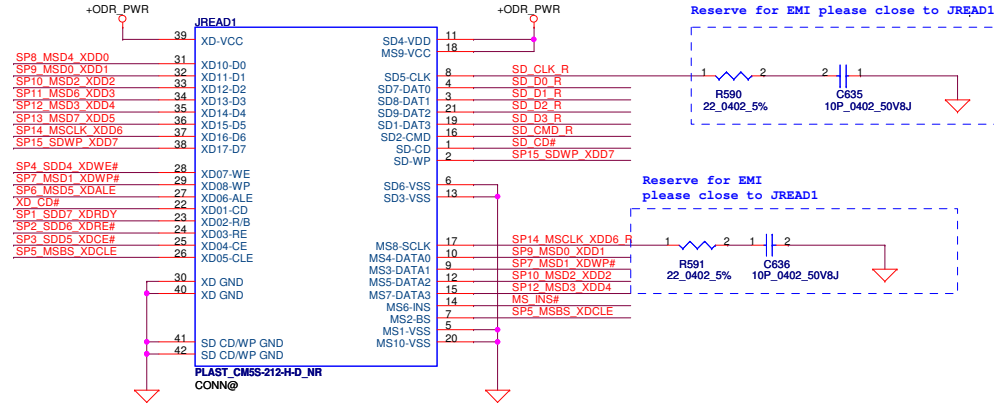
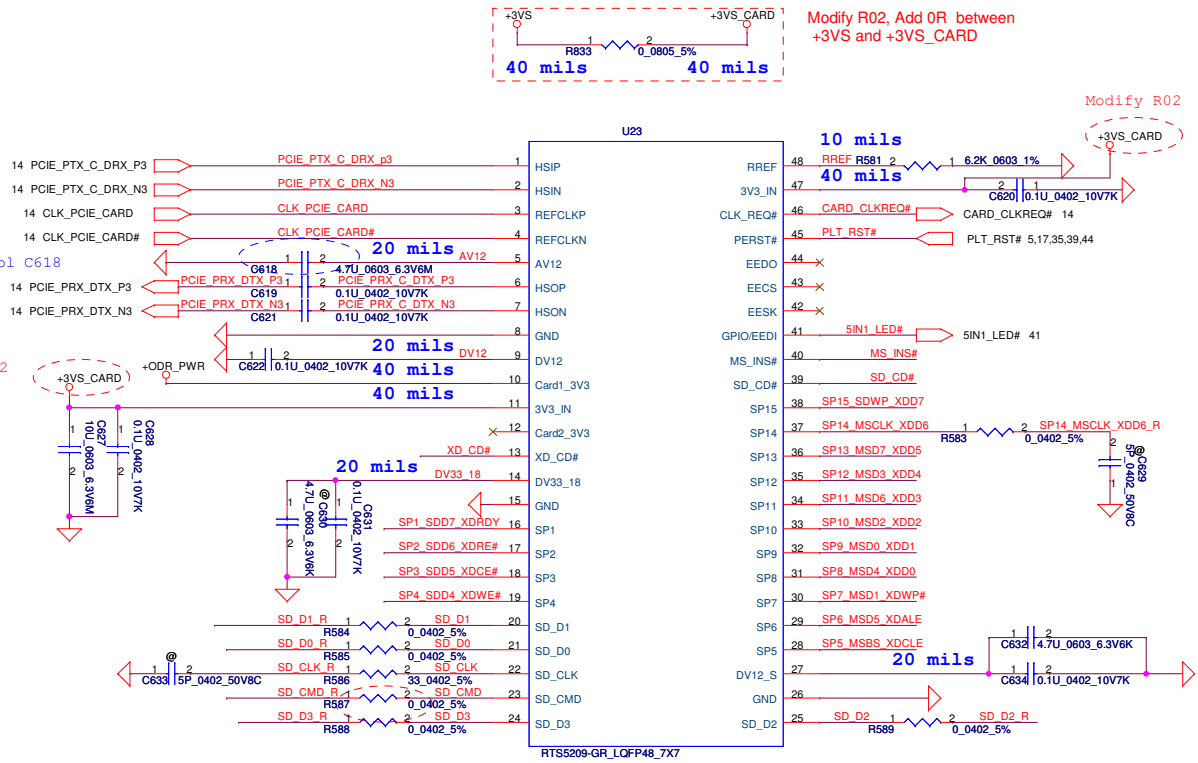
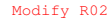
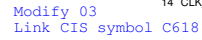
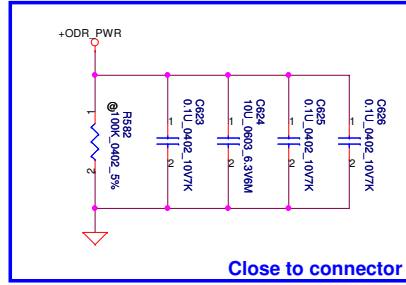


## BT Conn. (Port 13)



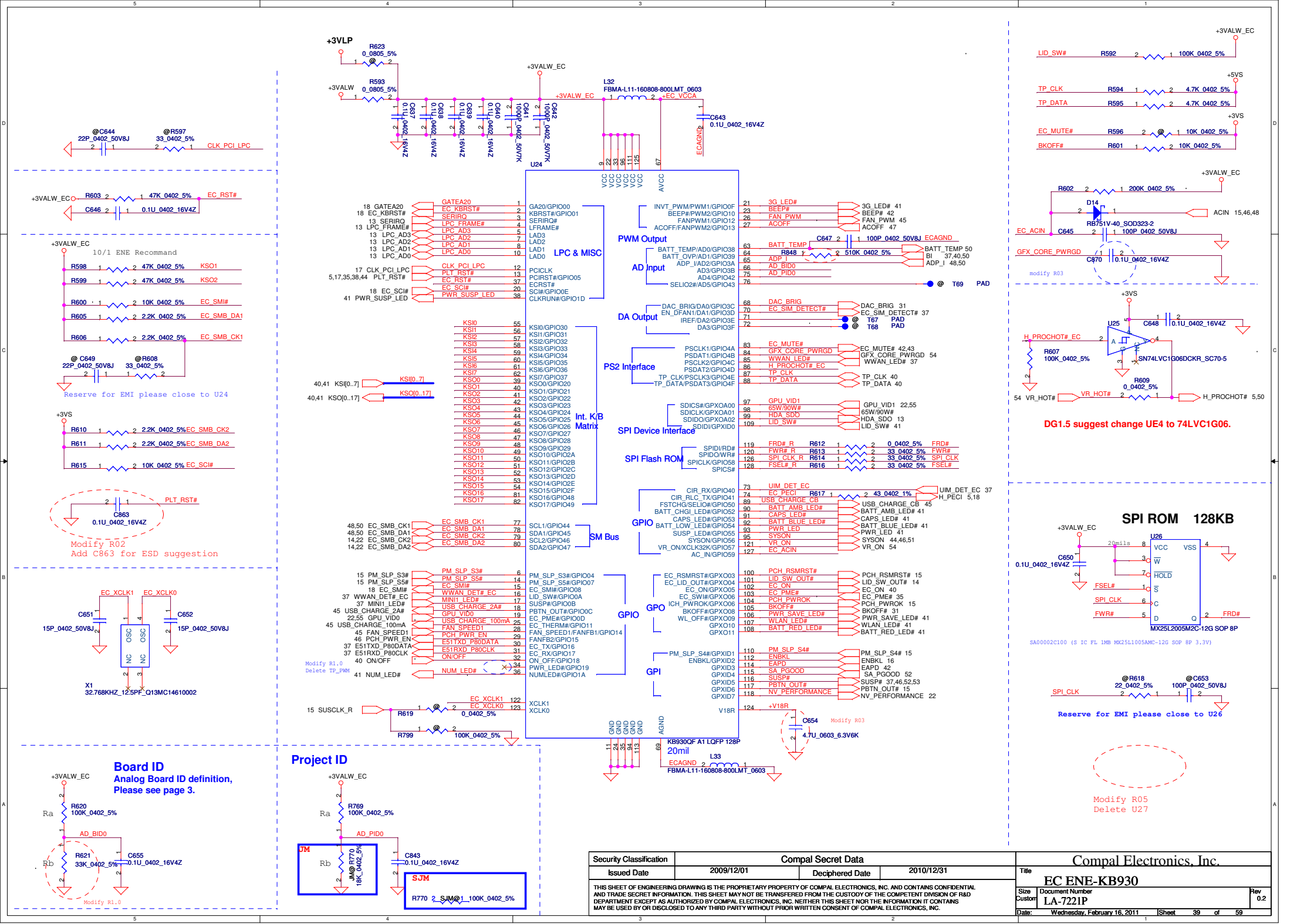
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Issued Date		2008/08/10		Deciphered Date		2010/08/01	
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				MINI CARD (WLAN & TV-Tuner)/USB/BT			
				Size		Document Number	Rev
				Customer		LA-7221P	0.2
Date:				Wednesday, February 16, 2011		Sheet 37 of 59	

## Card Reader



10/5 Update symbol

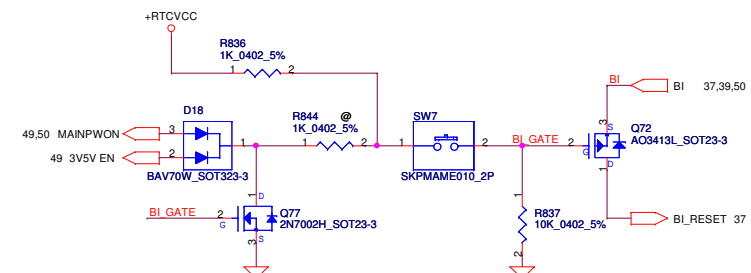
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Issued Date	2008/08/10	Deciphered Date	2010/08/01	Title Card Reader RTS5209		
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				Custom	LA-7221P	
				Date: Wednesday, February 16, 2011		Sheet



Modify R02  
KB connector use JKB2,JKB1 reserved.



10/04 Check footprint ok

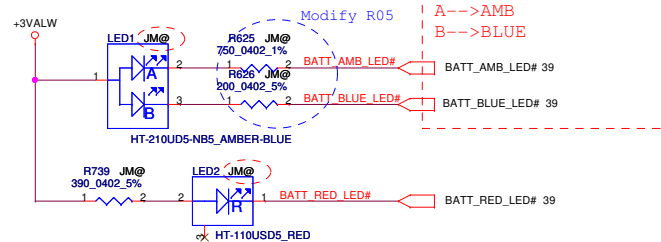


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				I/O Port & K/B Connector/PWR OK			
				Size	Document Number	Rev	
				Custom	LA-7221P	0.2	
				Date:	Wednesday, February 16, 2011	Sheet	40 of 59

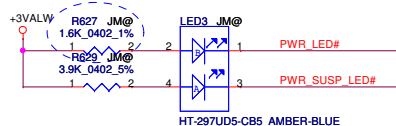


## Battery LED (JM)

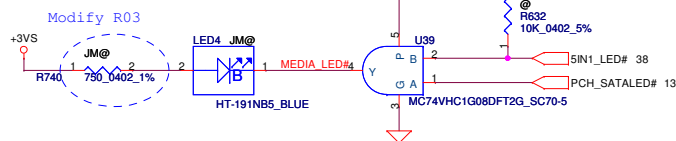
Side View LED with Blue/Amber/Red Color



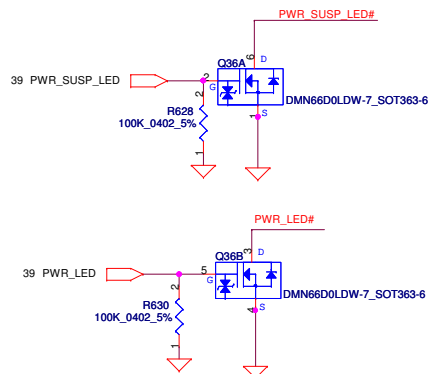
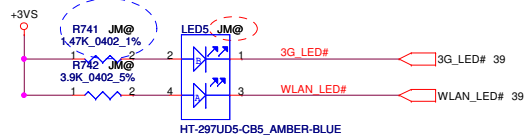
## Power LED (JM)



## HDD LED (JM)

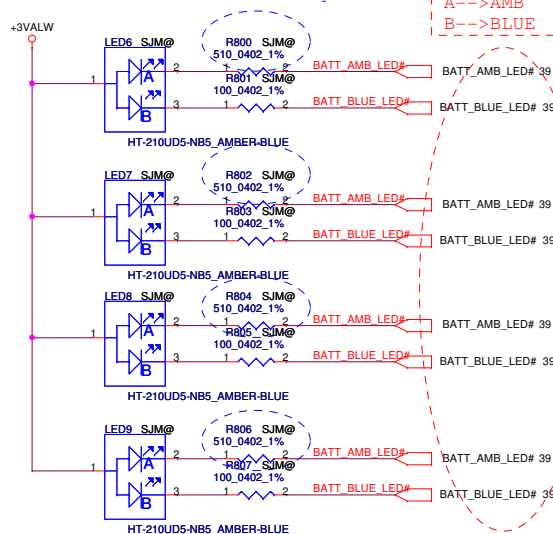


## 3G/Wireless LED (JM)

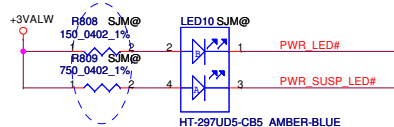


## Battery LED (SJM)

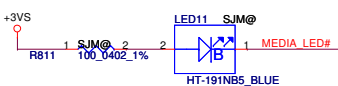
Modify R05



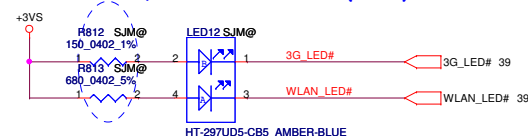
## Power LED (SJM)



## HDD LED (SJM)



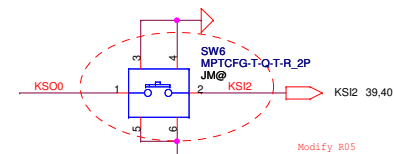
## 3G/Wireless LED (SJM)



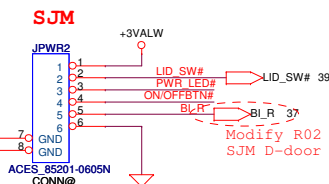
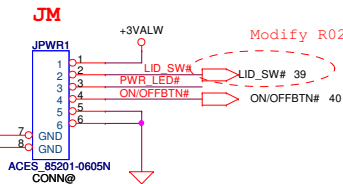
LED Status	Power/SUS		Battery		3G/WLAN		BlueTooth	ACIN
	ON	SUS	Full	Charge	3G	WLAN		
		Blue	Amber	Blue	Amber	Blue	Amber	

Modify R02  
LED\_HT-210UD5-NB5  
A-->AMB  
B-->BLUE

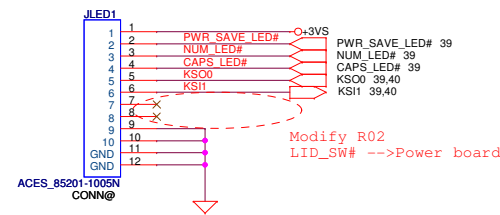
## Battery Indicator BTN (JM only)



## PWR/B

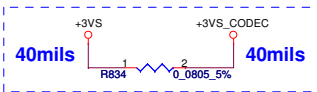
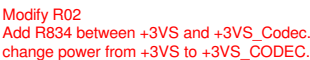


## LED Board (JM only)

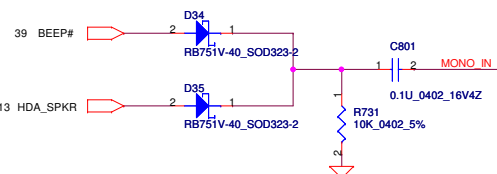


KSO0	
KSI0	Battery BTN#
KSI1	PWR SAVE BTN#

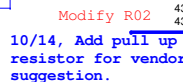
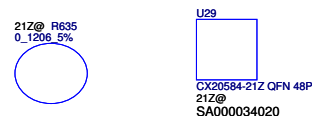
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Issued Date		2008/08/10	Deciphered Date	2010/08/01						
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						Title		LED/PWR/B		
						Size	Document Number	Rev	0.2	
						Customer	LA-7221P			
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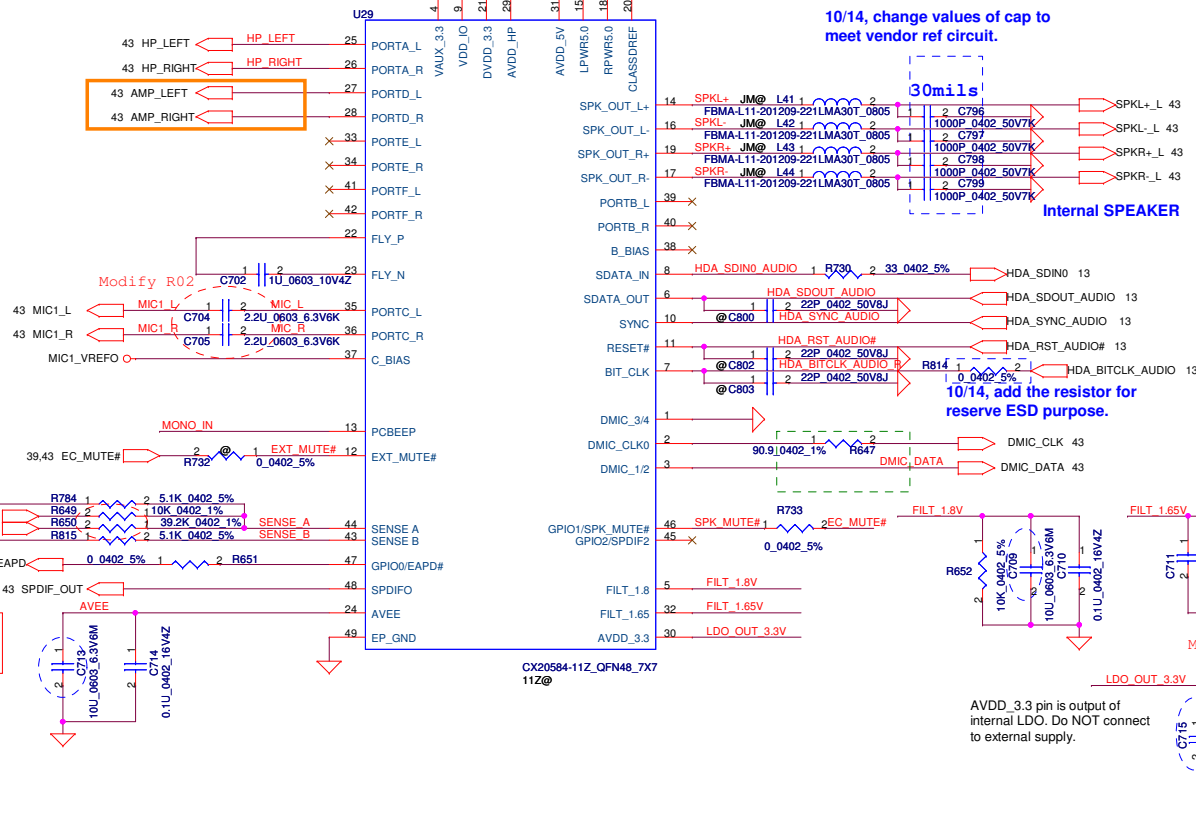
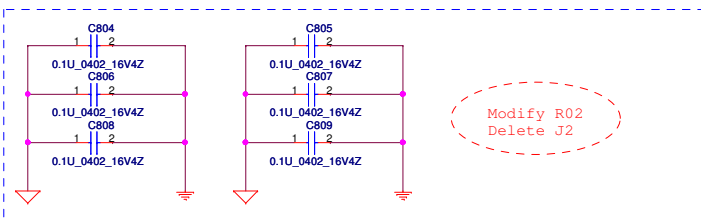
Modify R02  
Delete R638.Q39.Q38  
Add R835 between EC MUTE# and PD#.



Modify R02  
CX2058-21Z Option Component

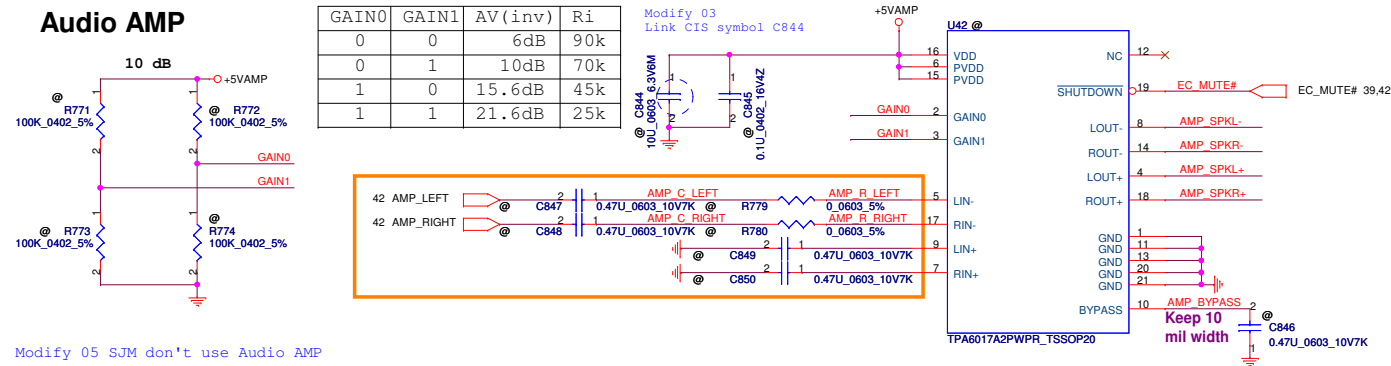


EAPD active low  
0=power down ex AMP  
1=power up ex AMP



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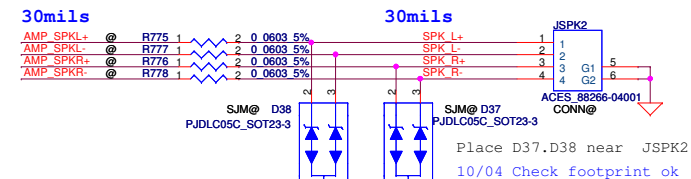
## Audio AMP



Modify 05 SJM don't use Audio AMP

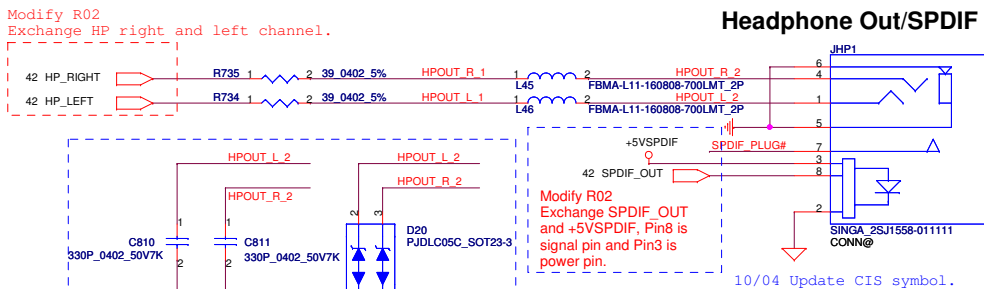
## Int. Speaker Conn.

SJM

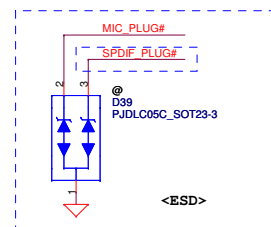


Place D37.D38 near JSPK2  
10/04 Check footprint ok

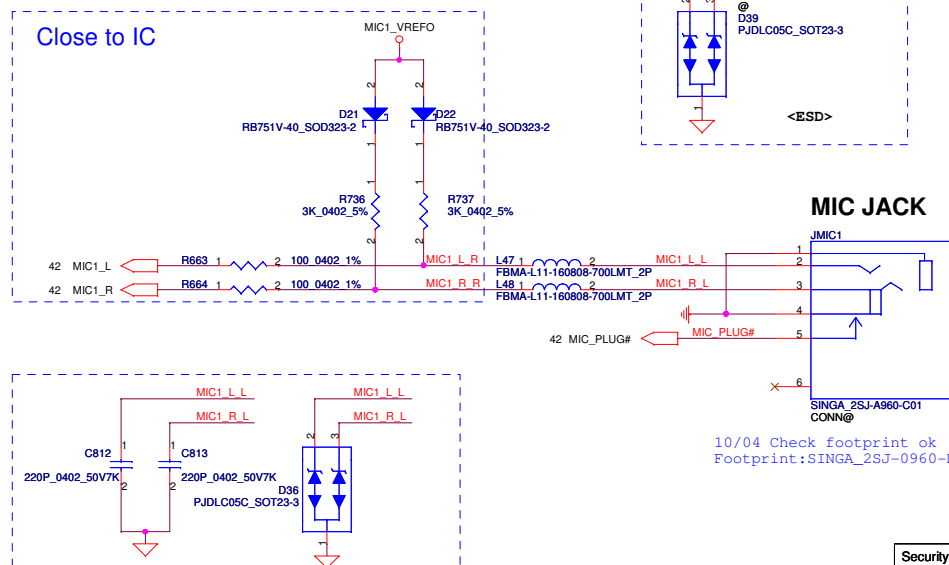
### Headphone Out/SPDIF



10/04 Update CIS symbol.

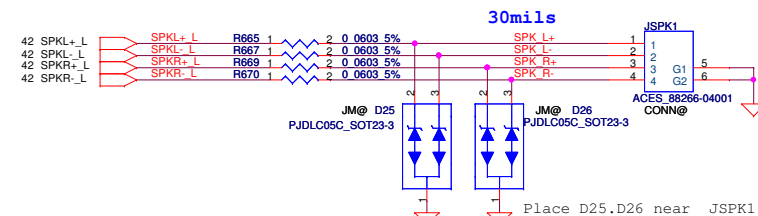


**MIC JACK**



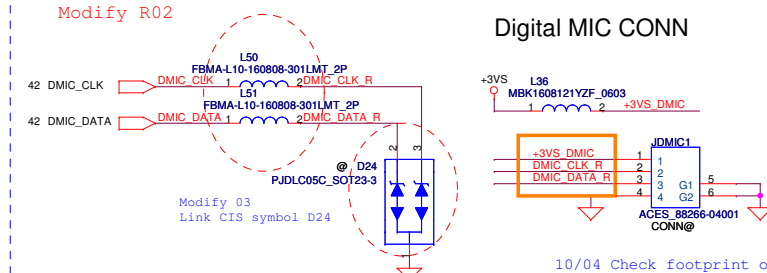
10/04 Check footprint ok  
Footprint:SINGA\_2SJ-0960-D06\_6F

Int. Speaker Conn.

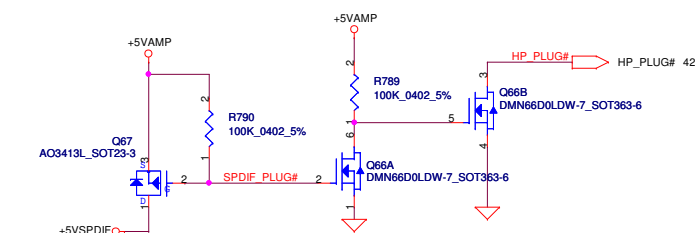
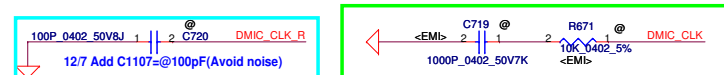


Place D25.D26 near JSPK1

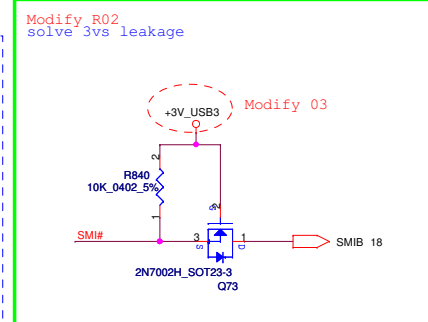
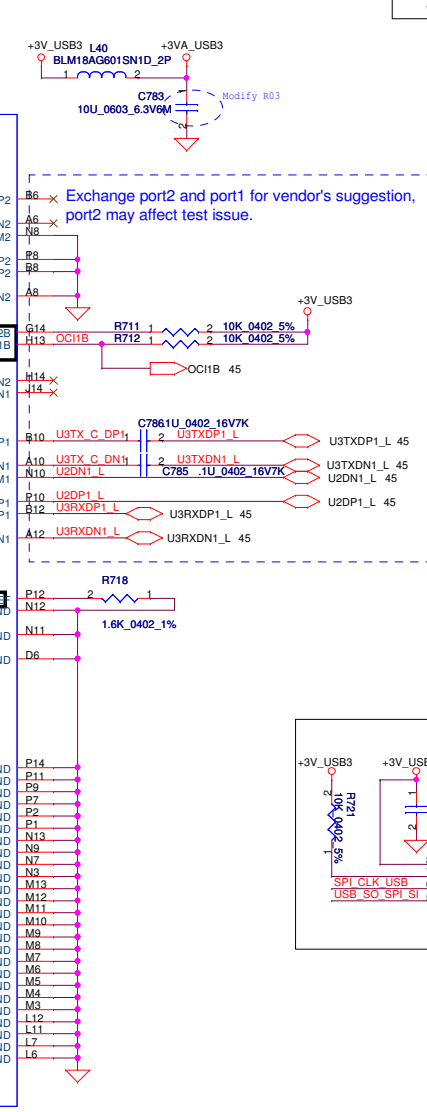
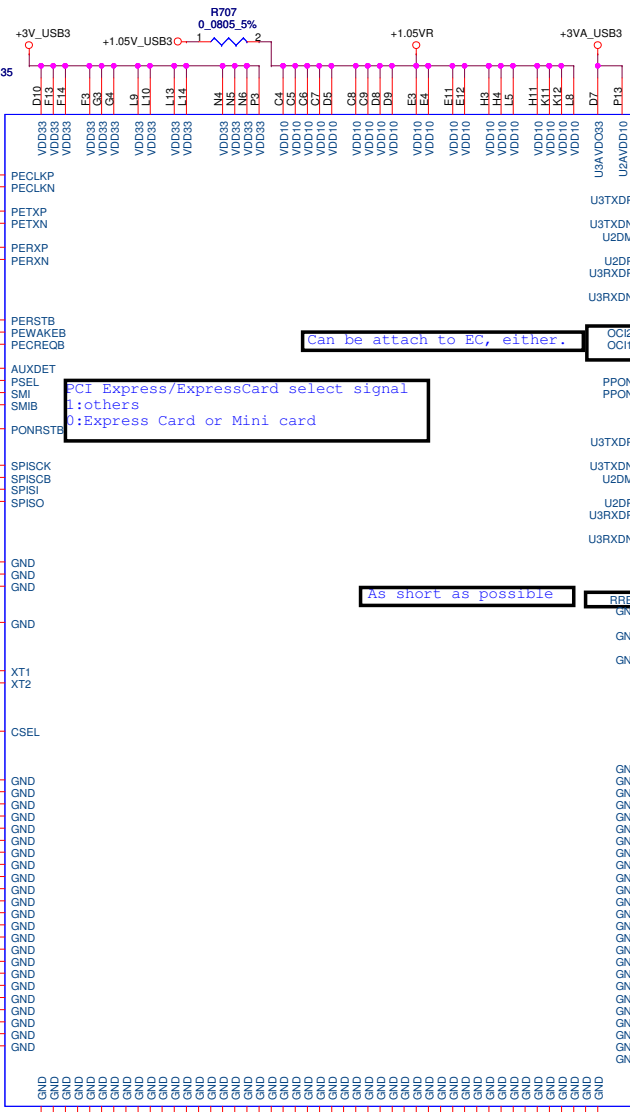
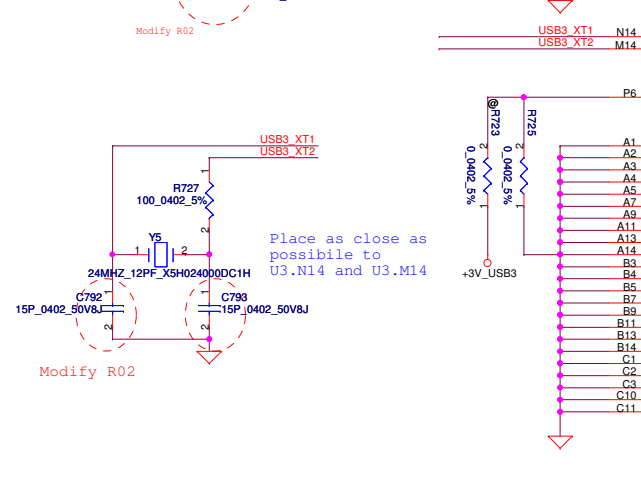
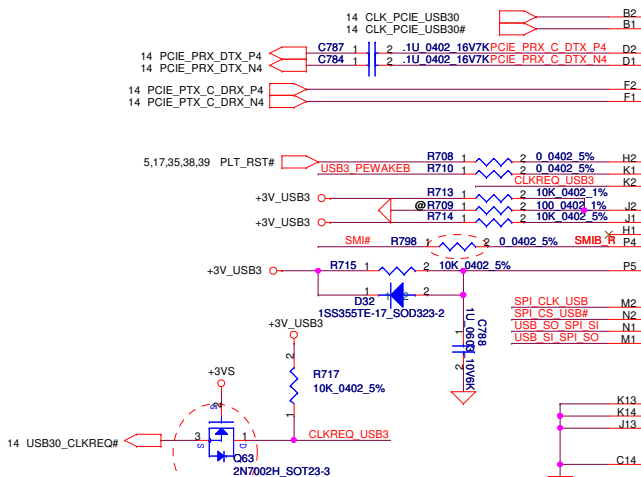
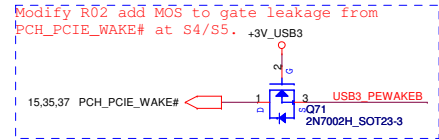
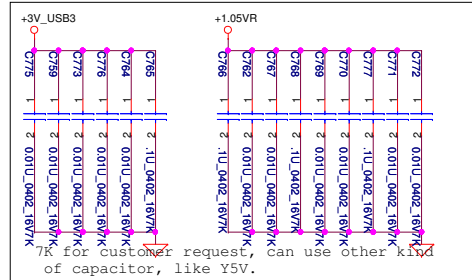
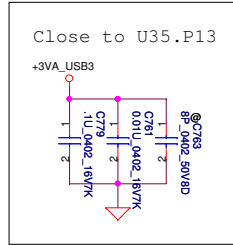
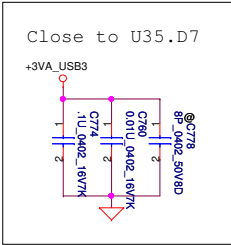
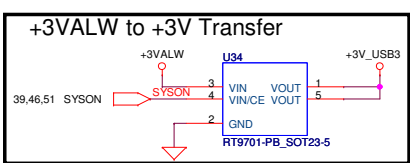
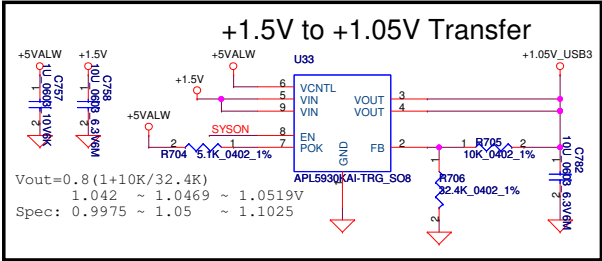
## Digital MIC CONN



10/04 Check footprint ok



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Pin compare table for support USB remote wakeup or not

	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y1,R19,C40,C41
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R22,R25

P/N: SA000048H00

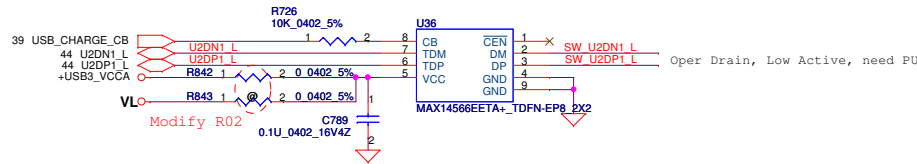
Security Classification	Deciphered Date	Deciphered Date
Issued Date	2010/09/28	2011/09/28

UPD720200AF1-DAP-A\_FPGA176

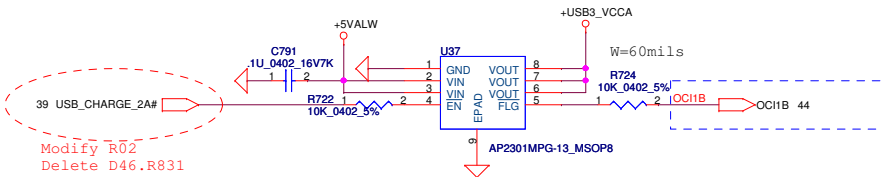
Security Classification	Deciphered Date	Deciphered Date
Issued Date	2010/09/28	2011/09/28

Title		Rev
USB3.0 PD720200A		0.2
Size	Document Number	
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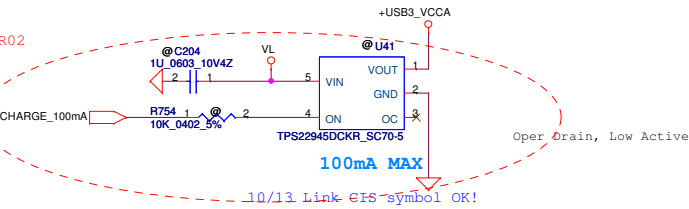
## USB Host Charger



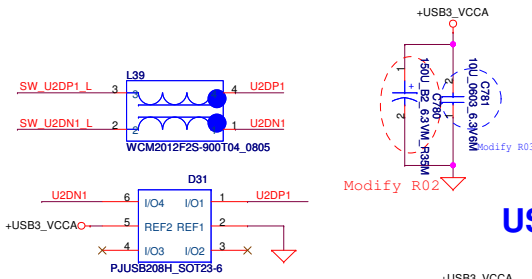
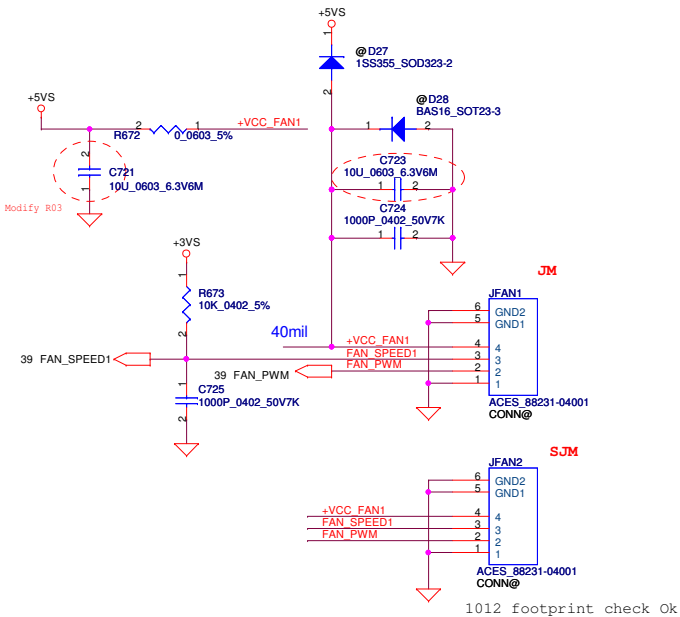
CB=0	Auto detection charger identification active
CB=1	Connect DP/DM to TDP/TDM



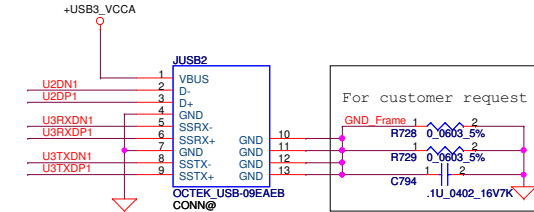
Modify R02



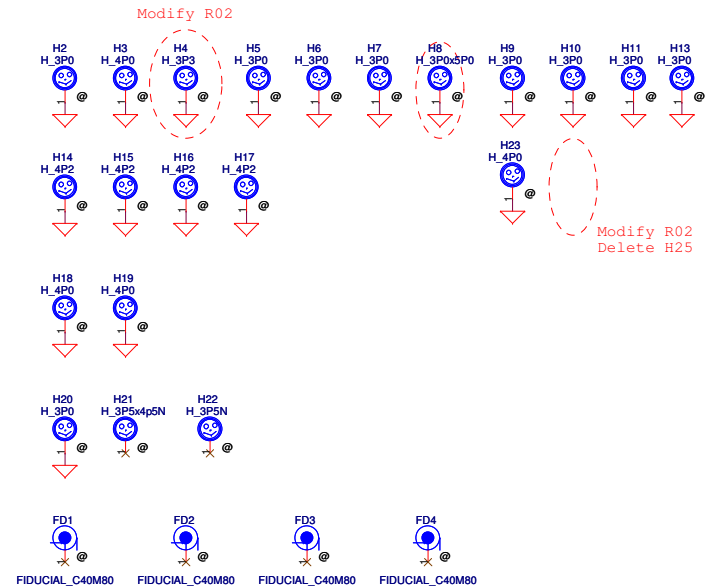
## FAN1 Conn



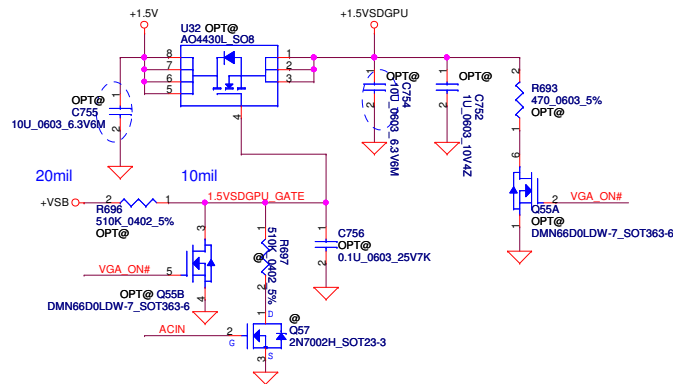
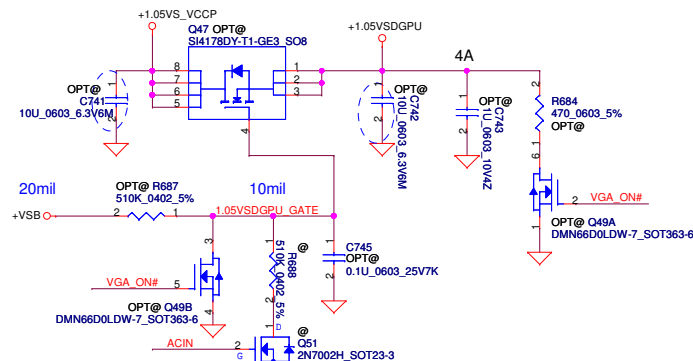
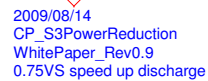
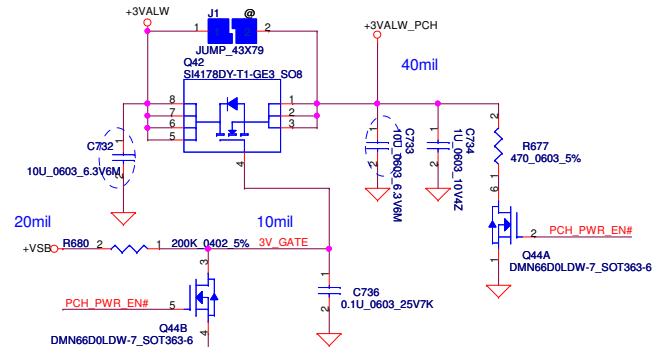
## USB3.0 Connector



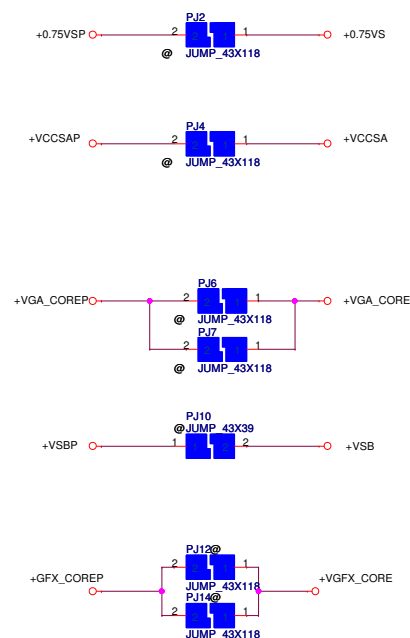
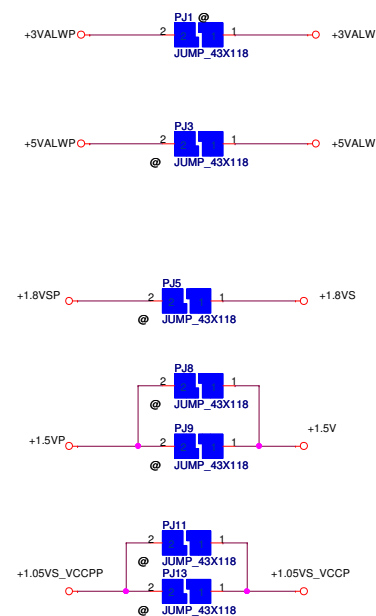
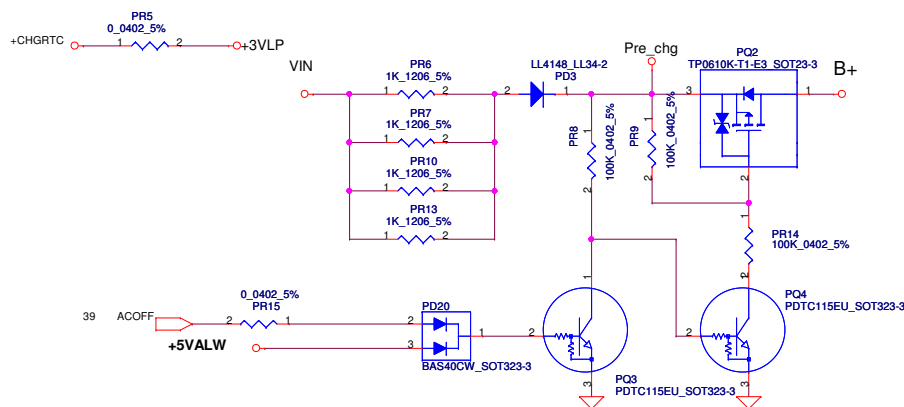
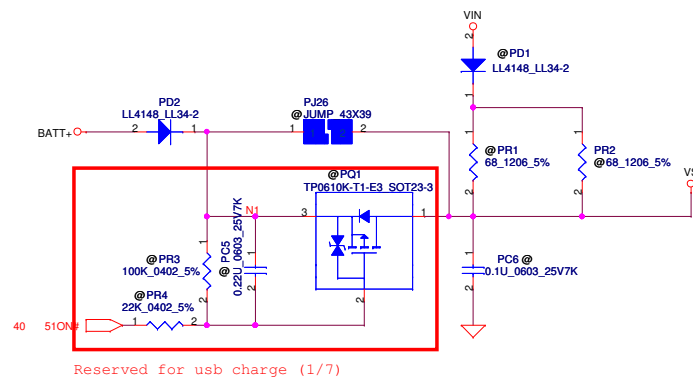
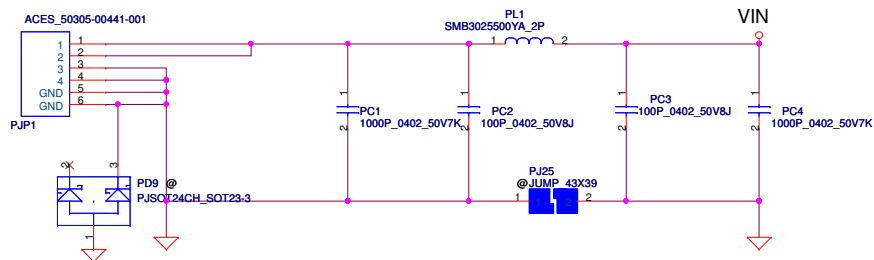
10/05 Update symbol .



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				Size	Document Number	Rev
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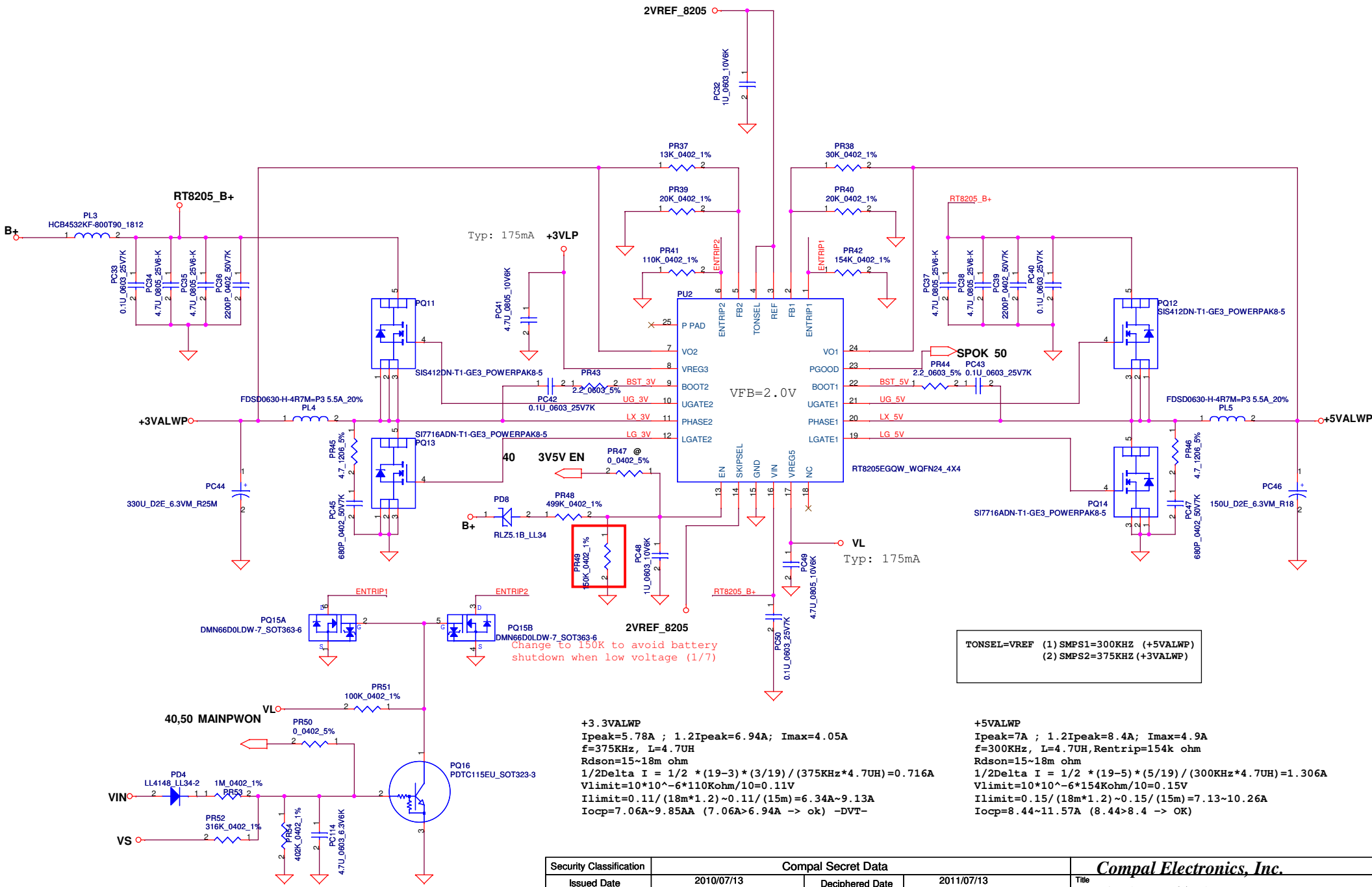
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Size	Custom	Document Number	LA-7221P	Rev	0.1
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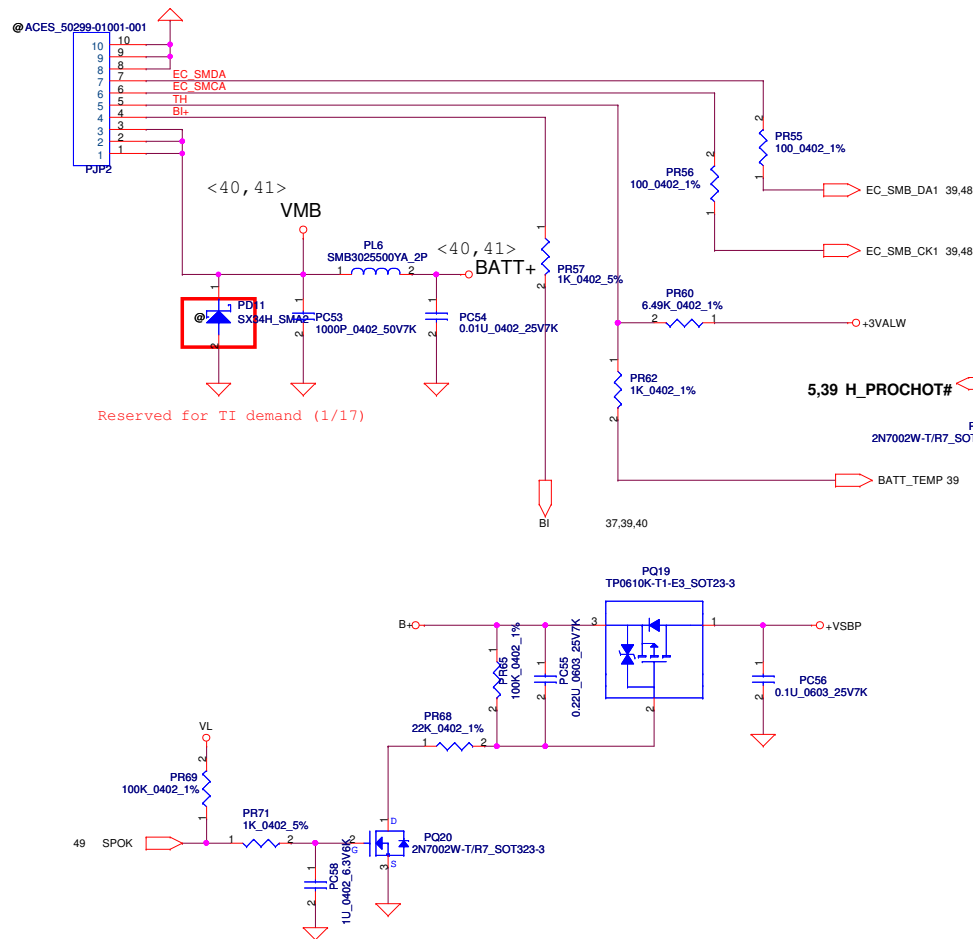
Change to 150K to avoid battery shutdown when low voltage (1/7)

TONSEL=VREF (1) SMPS1=300KHZ (+5VALWP)  
(2) SMPS2=375KHZ (+3VALWP)

**+3.3VALWP**  
 $I_{peak}=5.78A$  ;  $1.2I_{peak}=6.94A$  ;  $I_{max}=4.05A$   
 $f=375KHz$  ,  $L=4.7UH$   
 $R_{dson}=15\sim 18m\ ohm$   
 $1/2\Delta I = 1/2 * (19-3) * (3/19) / (375KHz * 4.7UH) = 0.716A$   
 $V_{limit}=10*10^{-6} * 110Kohm / 10 = 0.11V$   
 $I_{limit}=0.11 / (18m * 1.2) \sim 0.11 / (15m) = 6.34A \sim 9.13A$   
 $I_{ocp}=7.06A \sim 9.85A$  (  $7.06A > 6.94A \rightarrow ok$  ) -DVT-

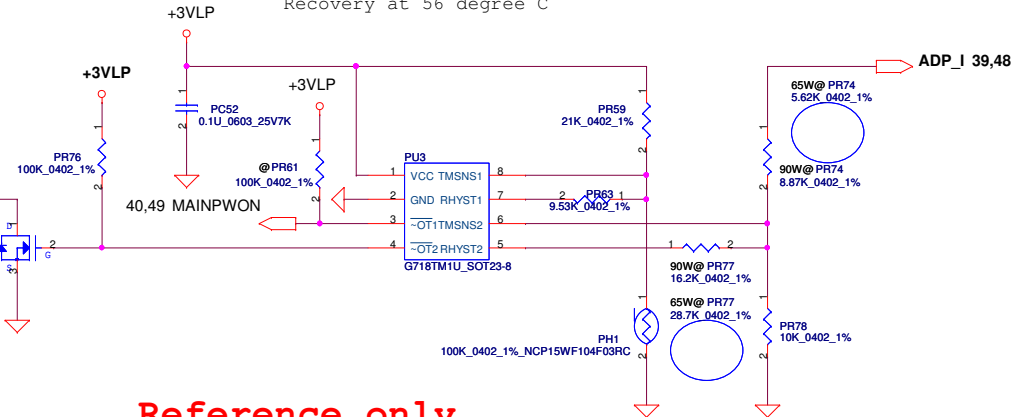
**+5VALWP**  
 $I_{peak}=7A$  ;  $1.2I_{peak}=8.4A$  ;  $I_{max}=4.9A$   
 $f=300KHz$  ,  $L=4.7UH$  ,  $R_{entrip}=154k\ ohm$   
 $R_{dson}=15\sim 18m\ ohm$   
 $1/2\Delta I = 1/2 * (19-5) * (5/19) / (300KHz * 4.7UH) = 1.306A$   
 $V_{limit}=10*10^{-6} * 154Kohm / 10 = 0.15V$   
 $I_{limit}=0.15 / (18m * 1.2) \sim 0.15 / (15m) = 7.13 \sim 10.26A$   
 $I_{ocp}=8.44 \sim 11.57A$  (  $8.44 > 8.4 \rightarrow OK$  )

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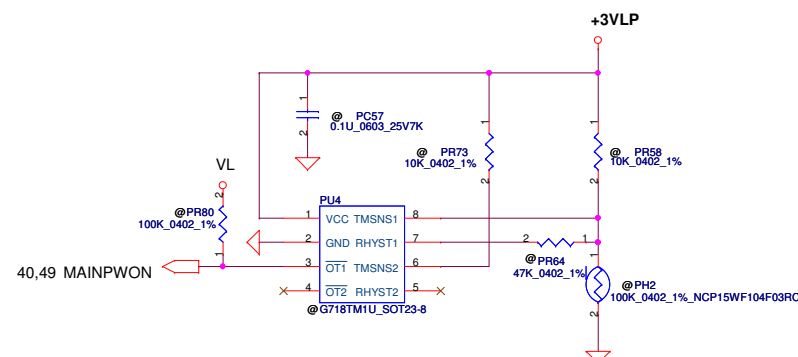


Combine protection circuit(1/7)

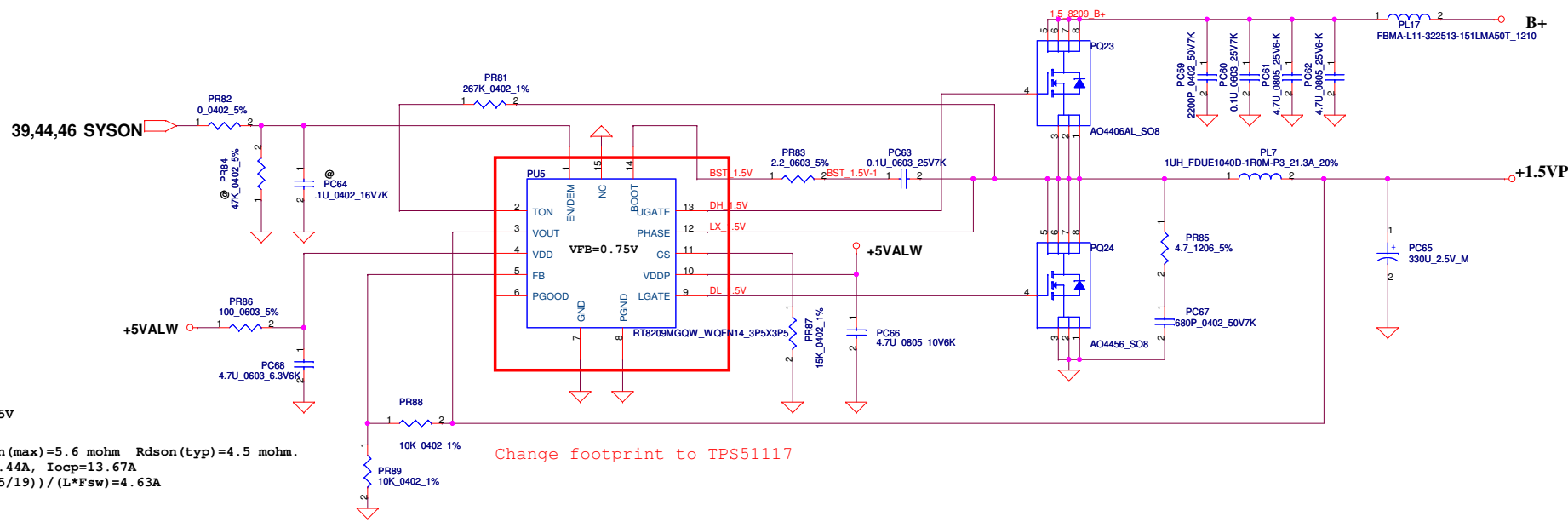
PH1 under CPU bottom side : **Reference only**  
 CPU thermal protection at 92 degree C  
 Recovery at 56 degree C



For 65W adapter==>action 70W , Recovery 54W  
 For 90W adapter==>action 97W , Recovery 75W



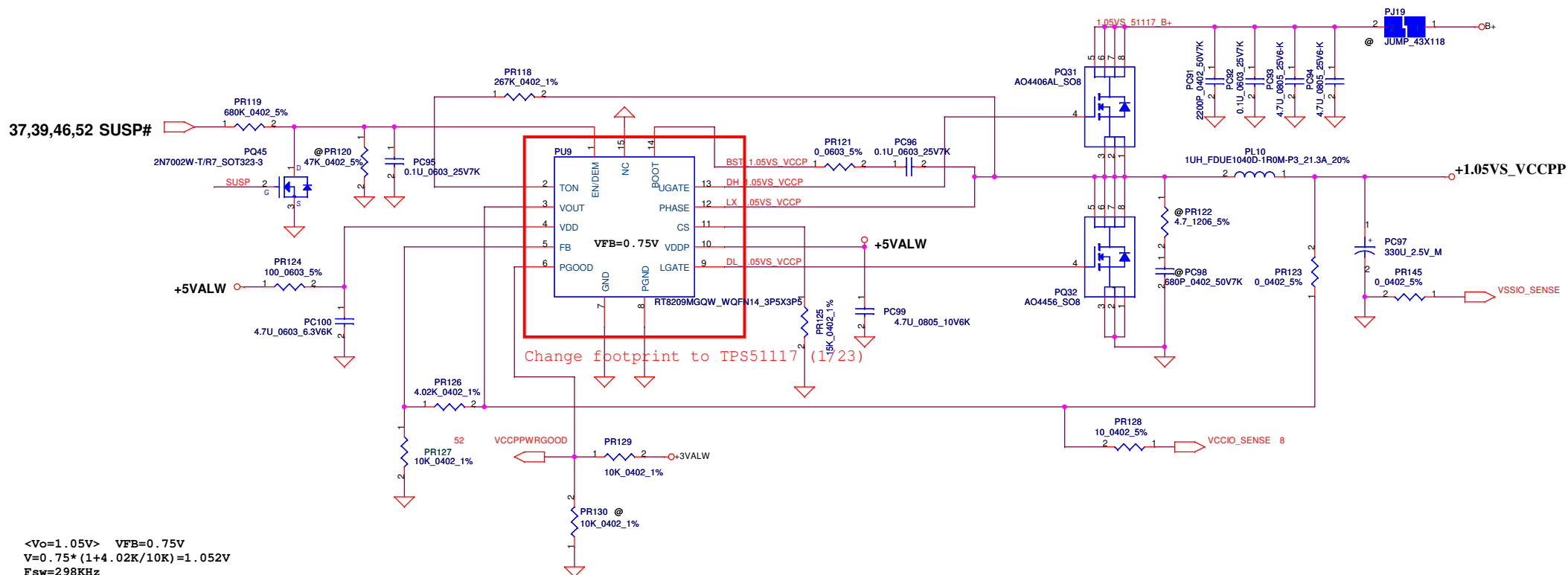
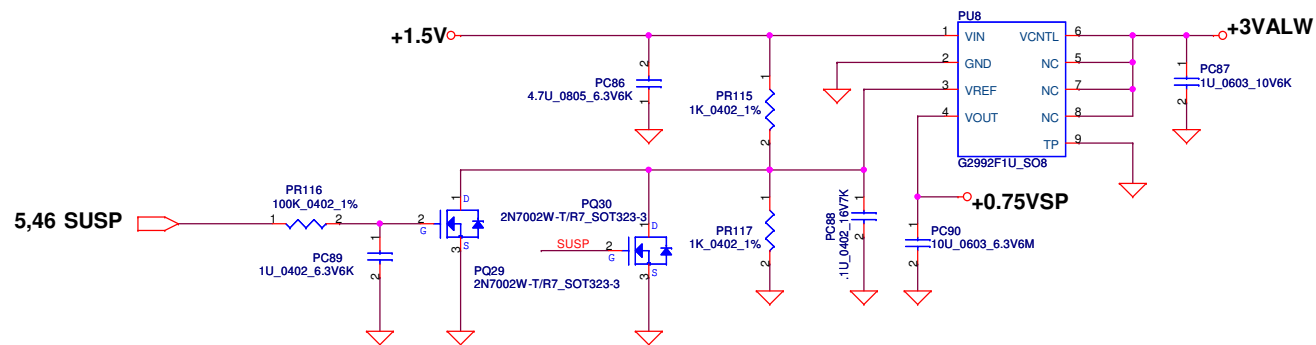
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Issued Date	2010/01/25	Deciphered Date	2010/12/31	Title	PWR-BATTERY CONN/OTP
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$V_o = 1.5V$      $V_{FB} = 0.75V$   
 $V = 0.75 * (1 + 10K / 10K) = 1.5V$   
 $F_{sw} = 298KHz$   
 $C_{out} ESR = 15m \text{ ohm}$      $R_{dson(max)} = 5.6 \text{ mohm}$      $R_{dson(typ)} = 4.5 \text{ mohm}$ .  
 $I_{peak} = 19.53A$ ,  $I_{max} = 23.44A$ ,  $I_{ocp} = 13.67A$   
 $\Delta I = ((19 - 1.5) * (1.5 / 19)) / (L * F_{sw}) = 4.63A$   
 $\Rightarrow 1/2 \Delta I$      $I = 2.315A$   
choose  $R_{cs} = 15K$   
 $I_{ocpmax} = ((15K * 11uA) / 0.0045) + 2.315A = 35.65A$   
 $I_{ocpmin} = ((15K * 9uA) / (0.0056 * 1.3)) + 2.315A = 23.06A$   
 $I_{ocp} = 23.06A \sim 35.65A$

Change footprint to TPS51117

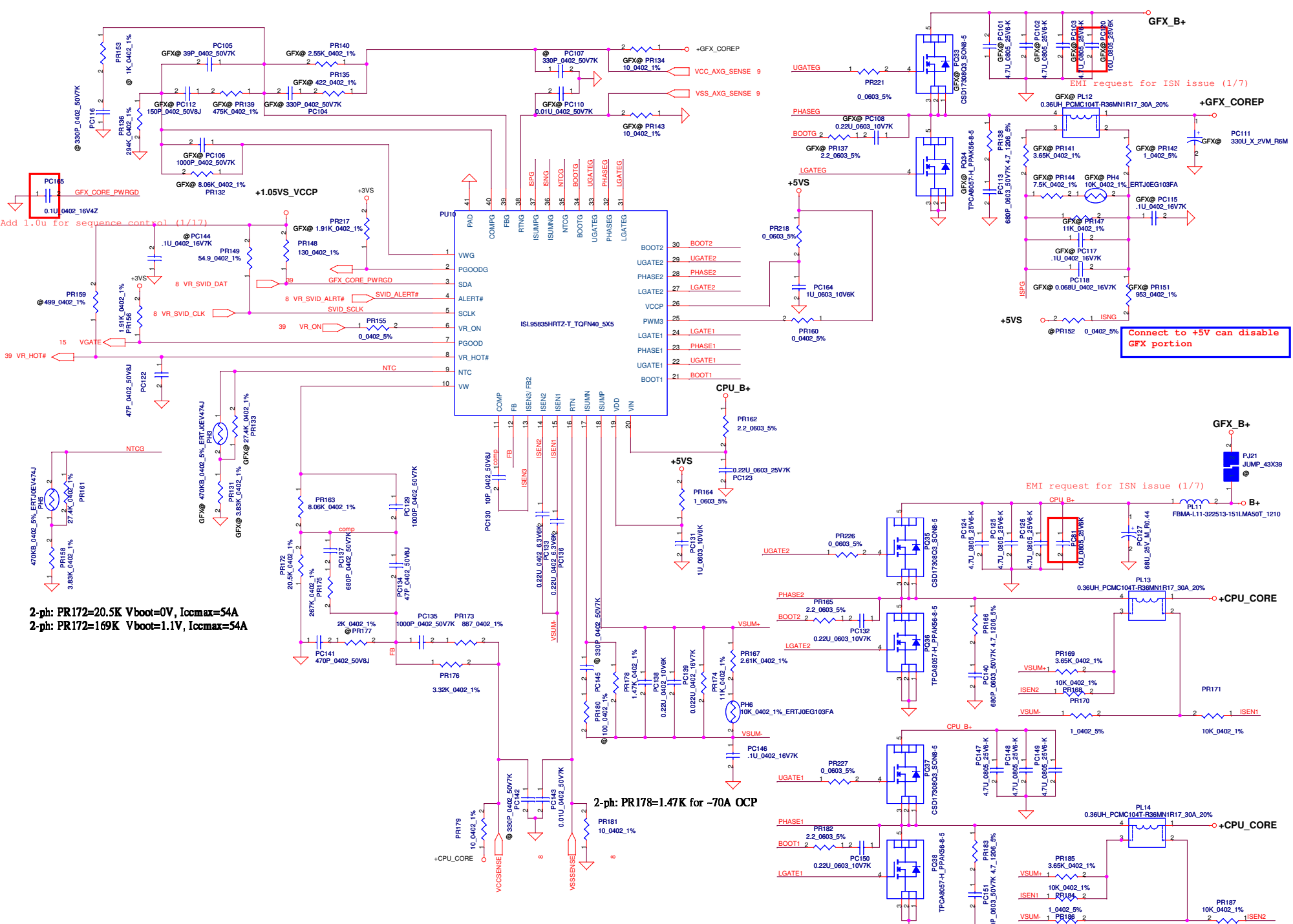




$V_o = 1.05V$      $V_{FB} = 0.75V$   
 $V = 0.75 * (1 + 4.02K/10K) = 1.052V$   
 $F_{sw} = 298KHz$

$C_{out} ESR = 15m \text{ ohm}$      $R_{dson(max)} = 5.6 \text{ mohm}$      $R_{dson(typ)} = 4.5 \text{ mohm}$   
 $I_{peak} = 12.866A$ ,  $I_{max} = 9A$ ,  $I_{ocp} = 15.439A$   
 $\Delta I = ((19 - 1.05) * (1.05/19)) / (L * F_{sw}) = 3.33A$   
 $\Rightarrow 1/2 \Delta I = 1.665A$   
choose  $R_{cs} = 15K$   
 $I_{ocpmax} = ((15K * 11uA) / 0.0045) + 1.665A = 37.62A$   
 $I_{ocpmin} = ((15K * 9uA) / (0.0056 * 1.3)) + 1.665A = 23.02A$   
 $I_{ocp} = 23.02A \sim 37.62A$

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Issued Date	2010/07/13	Deciphered Date	2011/07/13	Title	PWR +1.05VS_VCCPP/+0.75VSP
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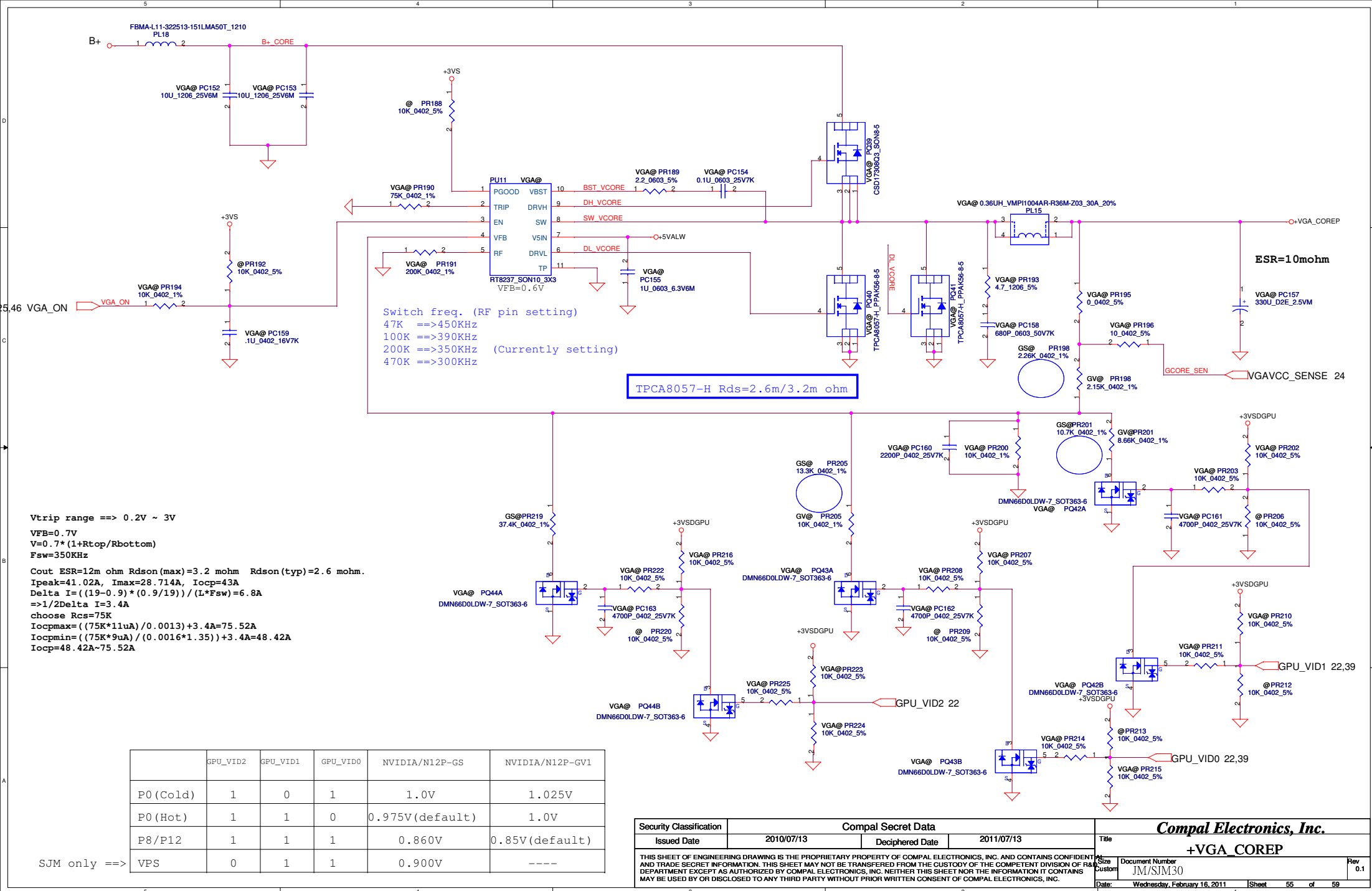
2-ph: PR172=20.5K Vboot=0V, Iccmax=54A  
2-ph: PR172=169K Vboot=1.1V, Iccmax=54A

2-ph: PR178=1.47K for -70A OCP

+CPU_CORE	+GFX_CORE
Iocp=70A, IccMAX=53A	Iocp=40A, IccMAX=24A
Load line=1.9mohm	Load line=3.9mohm
DCR=1.1mohm	DCR=1.1mohm

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	GPU_VID2	GPU_VID1	GPU_VID0	NVIDIA/N12P-GS	NVIDIA/N12P-GV1
P0(Cold)	1	0	1	1.0V	1.025V
P0(Hot)	1	1	0	0.975V(default)	1.0V
P8/P12	1	1	1	0.860V	0.85V(default)
VPS	0	1	1	0.900V	----

## Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	HW/Edward request	Meet Turn off sequence		53	Add PQ45	2010 11/24	DVT
2	HW/Edward request	Meet Turn on sequence		53	Change PR119 to 680KΩ, PC95 to 0.1uF	2010 11/27	DVT
3	HW/Edward request	Meet new VGA table		55	Change PR201, PR205, PR219	2010 12/03	DVT
4	Battery Turn on time too long	Change enable 3/5V path				2010 12/04	DVT
5	HW/Edward request	For USB 3.0 charger function		47	Add PJ26	2010 12/04	DVT
6	HW/Edward request	Don't need VGA_PW_OK net		55	Delete net	2010 12/04	DVT
7	NVedia request.	NVedia request.	0.2	55	change PR201 to SD034107280. change PR198 to SD034226180 chnage PR205 to SD034133280. Change PR219 to SD034374280	2010 12/10	DVT
8	HW request.	to adjust power sequence to modify.	0.2	52 53	Change PR92 to SD034510380, remove PR94 SD028100480 Change PR116 from SD034249280 to SD034100380.	2010 12/10	DVT
9	Sourcer request.	Change to a normal part.	0.2	54	Change PC138 from SE00000R700to SE095224K00	2010 12/10	DVT
10	EMI request	For ISN issue, add solution on charger and CORE power	0.3	48,54	Add PL16 PC19 PC109 PC80 PC51 PC120 PC81	2010 01/17	PVT
11	EMI request	For ISN issue, add solution on charger	0.3	48	Change PL2 to SH162100M10 (4.7U to 10U)	2010 01/17	PVT
12	TI concern charger IC will be lauch	Negative current reaches 110mV on low side Rdson Charger IC will be lauch	0.3	48	Change PC38 to SE026104K80 (2.2U to 0.1U)	2010 01/23	PVT
13	RT8209 footprint issue	The footprint pad is too short, It will happen SMT problem	0.3	51 53	Change PU5, PU9 footprint to TPS51117RGYR_QFN14_3P5X3P5	2010 01/23	PVT
14							
15							
16							
17							

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	41	Memo	2010/11/25	Compal	Bom structure error.	Correct LED1,LED2,LED5 bom structure to JM@	Rev02
2	27~30	Memo	2010/11/25	Compal		Change X76289BOL05(VRAM P/N) from SA00003MQ60 to SA000047Q20 Change X76289BOL06(VRAM P/N) from SA00003VS10 to SA00003YO20	Rev02
3	42	Memo	2010/11/25	Compal	New Audio Codec IC	Change U29 from SA000034010 to SA000034020 Change R635 from 0.1ohm to 0 ohm	Rev02
4	41	LED	2010/11/25	Compal	Battery LED Color mistake	SWAP LED1,LED6,LED7,LED8,LED9 Pin 2 and Pin3 (Pin2-->BATT_AMB_LED#,Pin3-->BATT_BLUE_LED#)	Rev02
5	07	EDP	2010/12/08	Compal	Bom structure error.	Correct R70 bom structure to EDP@	Rev02
6	24	Rework instruction	2010/12/08	Compal	N12P-GV Strap sets up the mistake	a. Pop R382, Depop R388 (ROM_SO: pull up 10K ohm) b. Pop R380, Change R380 from 15k to 45k. Depop R386.(STRAP2: pull up 45K ohm.) c. Pop R760, Change R760 from 10k to 5k.( STRAP3: pull down 5K ohm.) d. Pop R756. (STRAP4: pull down 10K ohm.) e. Pop R578. (STRAP_REF2, need to stuff with 40K ohm 1%.) f. Pop R757. (PGOOD (pin E7) stuff 10K ohm.)	Rev02
7	05	XDP	2010/12/08	Compal		Depop XDP component	Rev02
8	07	EDP	2010/12/08	Compal	Bom structure error.	Correct R70 bom structure to EDP@	Rev02
9	15	PCH	2010/12/08	Compal		Change R244.1 net name from PCH_RSMRST# to PCH_RSMRST#_R Pop R223,Depop U5 Delete R231(0 ohm) between SUSACK#_R and SUSWARN#_R Add T90 test point for SUSACK#	Rev02
10	17	PCH	2010/12/08	Compal		Delete VGA_ON for PD only. Change PR3.2 to PCH_GPIO53 Delete R257 Change U6,U7 to SA00000OH00	Rev02
11	18	PCH	2010/12/08	Compal	Power sequence for DGPU_PWROK after 1.5VSDGPU	Add Q75,Q74,R841	Rev02
12	22	GPU	2010/12/08	Compal		Change R342.1 from R762.2 to R762.1(NV_PERFORMANCE_R)	Rev02
13	26	GPU	2010/12/08	Compal	Bom structure error.	Correct C381 & C857 bom structure to OPT@	Rev02
14	31	LVDS	2010/12/08	Compal	For LCDVDD rise time sequence issue	Change R468 from 1k to 100k Change C481 from 0.047u to 0.47u PCH_LCD_CLK & PCH_LCD_DATA,Pull high at PCH side. Add R832 between +3VS and JLVDS1.31.	Rev02
15	32,33	CRT.HDMI	2010/12/08	Compal		D8, D9 change material to SCS00003600	Rev02
16	33	HDMI	2010/12/08	Compal		Pop R502,Depop D9 SDVO_CTRL_DATA strap pull high at PCH side	Rev02
17	34,44	ODD.USB3.0	2010/12/08	Compal		Change Q31.Q63.Q71 to SB000008J10	Rev02
18	35	LAN	2010/12/08	Compal	Auto power on issue	Change R541.2 net name from PCH_PCIE_WAKE# to LAN_WAKE#. Pop R541	Rev02
19	35	LAN	2010/12/08	Compal		Change C583 from 27 to 15P Change C582 from 27to 18P Change Y4 from CL(20P)to CL(12P) Add Q76 and Depop R555	Rev02
20	36	Transformer	2010/12/08	Compal		Change T63 from SP050003T10 to SP050003T20	Rev02

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
21	36	LAN	2010/12/08	Compal		L31 update CIS Symbol and PCB footprint	Rev02
22	37	3G	2010/12/08	Compal	3G Power noise	Delete L49.L50.R764.R765.R766.R767.U43.C852.C853.CR781.Q69.C856.C854. C855.C851.R572.R782 Change J3G1 Pin 2.4.6.8.10 to +3VS Change R572.3 to +3VS Change J3G1.30 to +VSB Change J3G1.17 to EC_SIM_DETECT#	Rev02
23	37	D_Door switch	2010/12/08	Compal		Add R838,R839 Depop R838 Pop R839	Rev02
24	38	Card Reader	2010/12/08	Compal		Change R590,R591 to 22ohm Change C635,C636 to 10P Add R833 between +3VS and +3VS_CARD	Rev02
25	39	EC	2010/12/08	Compal		Change R621 from 0ohm to 8.2k(Board ID) Add C863	Rev02
26	40	TP	2010/12/08	Compal	TP Pin define issue	Change JTP1 Pin define (Pin-->GND,Pin2-->RIGHT_BTN#,Pin3-->LEFT_BTN#,Pin4-->TP_DATA, Pin5-->TP_CLK,Pin6-->+5VS) Change JTP2 Pin define (Pin-->NC,Pin2-->GND,Pin3-->TP_CLK,Pin4-->TP_DATA,Pin5-->PWM,Pin6-->+5VS) Add C864	Rev02
27	40	Power Button	2010/12/08	Compal		Change R622.2 from +3VALW to +3VALW_EC	Rev02
28	40	Reset Button	2010/12/08	Compal	Reset system by mainpower and BI	Add R844,R836.R837.Q72.Q77 Change R836 to 1K Change R837 to 10K	Rev02
29	41	Power board	2010/12/08	Compal		Change JPWR2.5 from NC pin to BI_R (SJM D_door) Change LID_SW# from LED board(JLED1.8) to Power board(JPWR1.2)	Rev02
30	42	HD Audio Codec	2010/12/08	Compal	Fix HP/MIC Detect issue	Change R649 from 39.2k to 10k Change R650 from 10k to 39.2k	Rev02
31	42	HD Audio Codec	2010/12/08	Compal		Change C704,C705 to SE107225K80 Delete R637.R638.Q39.Q38.R634. R636.R639.R640.J2 Change power from +3VS to +3VS_CODEC. Add R834	Rev02
32	43	Headphone Out/SPDIF	2010/12/08	Compal	HP right and left channel inverse issue	Change R735.1 to HP_RIGHT Change R734.1 to HP_LEFT SWAP JHP1.3 and JHP1.8 (Pin8-->SPDIF_OUT and Pin3-->+5VSPDIF)	Rev02
33	43	Digital MIC	2010/12/08	Compal		Delete R666.R668 Add L50,L51 300ohm bead(SM010017710)	Rev02
34	44	USB3.0	2010/12/08	Compal	Modify SMI circuit for leakage issue	Delete R797,R830 Add R840,Q73.Q71	Rev02
35	44	USB3.0	2010/12/08	Compal		Change c792.c793 from 12P to 15P	Rev02
36	45	USB3.0	2010/12/08	Compal		Delete D46 Change C780 from SGA19151410(D size) to SGA00002N80(B2 size) Depop U41,C204,R754 Add R842,R843	Rev02
37	45	Screw Hole	2010/12/08	Compal		Change H4 from H_3P0 to H_3P3 Change H8 from H_3P0 to H_3P0x5P0 Delete H25	Rev02

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
38	46	DC Interface	2010/12/08	Compal		a.+5VS (Change R679 from 20K to 100K) b.+3VS (Change R685 from 47K to 200K) c. +1.5VS (Change R692 from 200K to 750K)	Rev02
39	13~21	PCH	2010/12/08	Compal		Change U3 from SA00004EE10 to SA00004EE40	Rev02
40	38	Caed Reader	2010/12/08	Compal		Change R587 from SD028330A00 to SD028330A80	Rev02
41	20.34. 35.36.42	Capacitor	2010/12/08	Compal		C226, C540, C549, C566, C573, C576, C580, C590, C712 change material to SE000000K80	Rev02
42	24	GPU	2010/12/10	Compal	Update N12P-GV QS DevID: 0x1050	1. ROM_SCLK: pull up 5K ohm. 2. STRAP2: pull down 5K ohm. 3. ROM_SO: pull up 10K ohm.	Rev02
43	44	USB3.0	2010/12/20	Compal	USB driver can't install issue	Change Q73.2 from +3V_USB3.0 to +3V_USB3 Pop R840	Rev03
44	31	CMOS Camera	2010/12/29	Compal		Add R845,Delete R832	Rev03
45	39	BI	2011/01/03	Compal	TI charger short protection prevent	Add R848	Rev03
46	40	TP	2011/01/03	Compal		Change SW2.SW3 from SN111002700 to SN100000K00	Rev03
47	41	LED	2011/01/12	Compal		Change R625 from 3.9K to 680 ohm Change R626 from 2.2K to 390 ohm Change R739 from 3.9K to 390 ohm Change R740 from 100 to 3.3K ohm	Rev03
48	46	VGA_ON	2011/01/13	Compal	Restart dGPU loss issue.	Change R703 from 22K to 100K Add R849 (10K)	Rev04
49	19	CRT	2011/01/22	Compal	water ripple issue	Change L1 from SM01000AX00 to SHI00003Y00	Rev04
50	39	EC	2011/01/25	Compal		Delete U27	Rev0.5
51	41	BTN	2011/01/25	Compal		Change SW6 from SN100001C00 to SN100001D10	Rev0.5
52	39	Board ID	2011/01/27	Compal	Board ID version	Change R621 to 33K	Rev0.5
53	5	CPU XDP	2011/01/27	Compal		Delete C34.C35.Q1.R21.R24.JXDP1.R3~R16.R18~R22.R39~R41.R43.R45~R47.R53~R60 Add T94~T98	Rev0.5
54	40	TP	2011/01/27	Compal		Delete net name TP_PWM	Rev0.5
55	18	DGPU_PWROK	2011/01/27	Compal		Pop C872	Rev0.5
56	44	USB3.0	2011/01/27	Compal	For EEPROM (EON).	Pop R720	Rev0.5

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