

Compal Confidential

JAWD0 Schematics Document

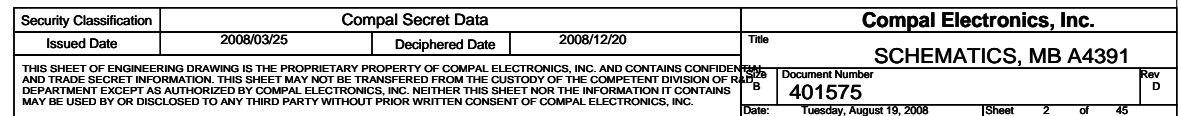
AMD Griffin Processor with RS780M+SB700

2008-07-01

REV:1.0

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/03/25	Deciphered Date	2008/12/20	Title	SCHEMATICS, MB A4391
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				Rev D	
Date: Tuesday, August 19, 2008				Sheet 1 of 45	

Model Name : JAWD0



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	X
+3V_LAN	3.3V power rail for LAN	ON	ON	X
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b		

EC SM Bus2 address

SB700
SM Bus 0 address

Device	Address
Clock Generator (ICS9LPRS365)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb
Minicard	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

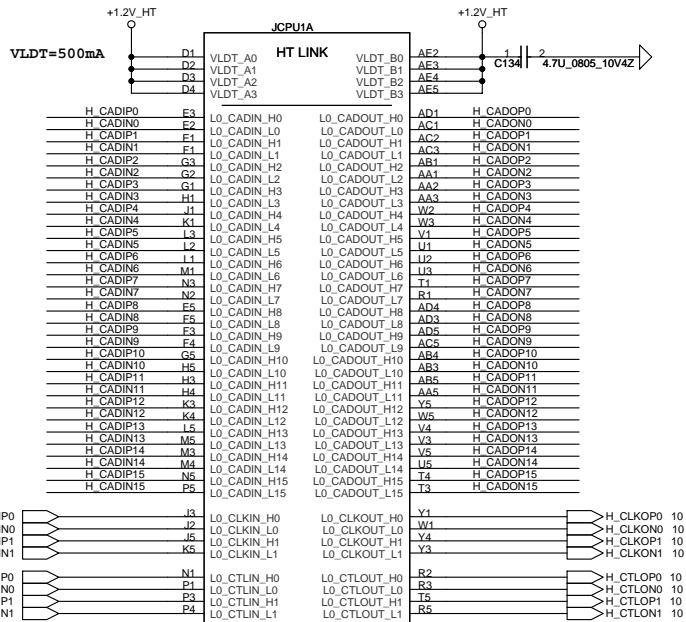
Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure

PROJECT ID Table

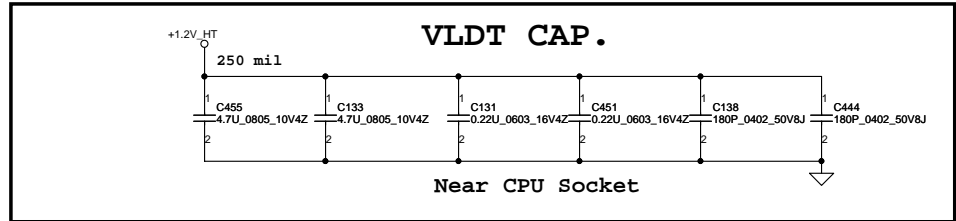
Board ID	PROJECT
0	JALB0
1	
2	
3	
4	
5	JAWD0
6	
7	JALC0



6090022100G_B

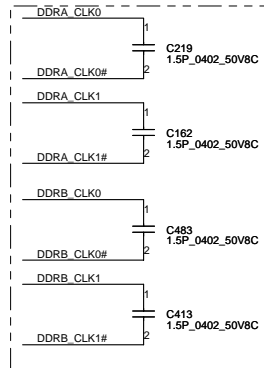
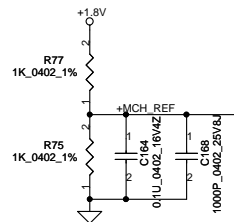
Athlon 64 S1

Processor Socket

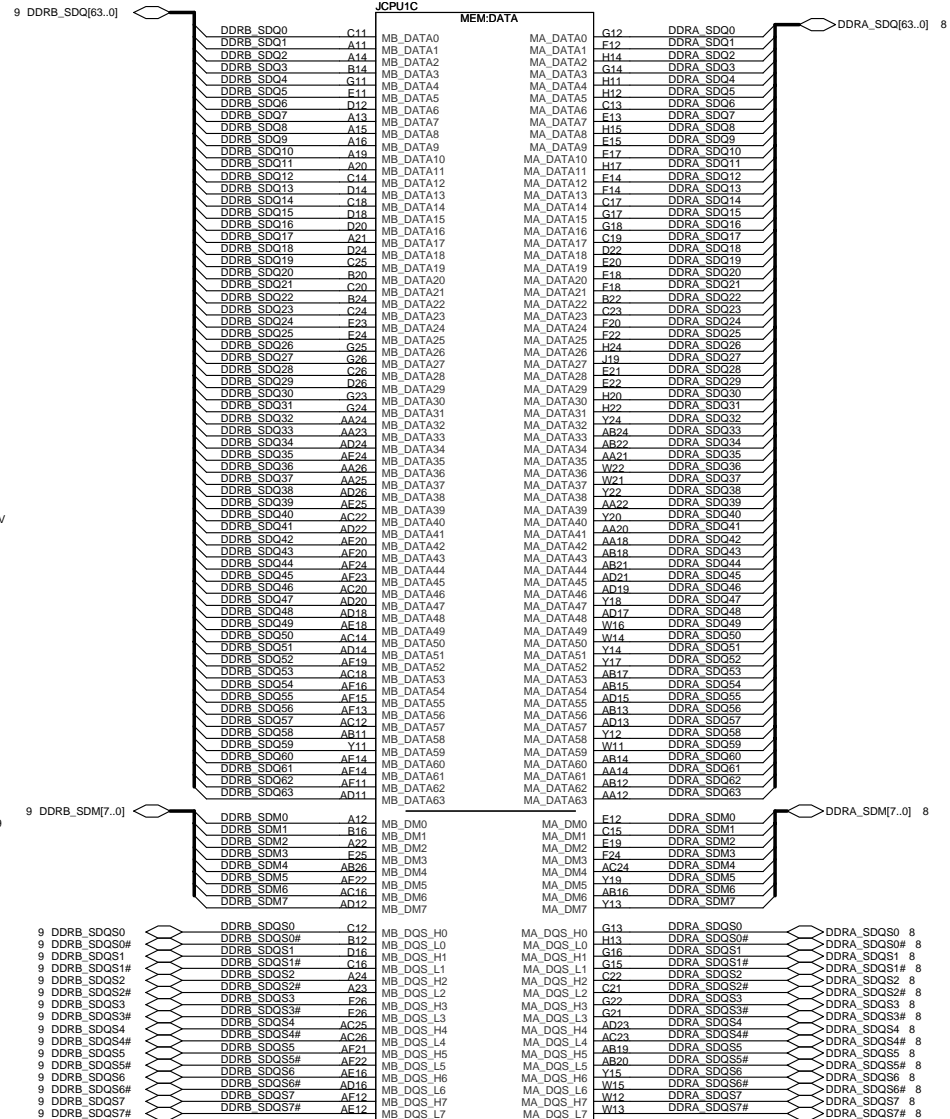


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				401575	
				Date: Tuesday, August 19, 2008	Sheet 4 of 45

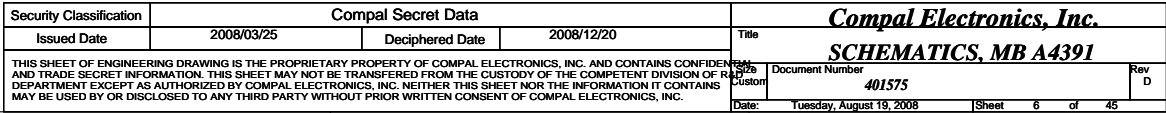
PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH



Processor DDR2 Memory Interface



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								401575			
								Tuesday, August 19, 2008			
								Sheet 5 of 45			



VDD(+CPU_CORE) decoupling.

Near CPU Socket

Diagram showing decoupling capacitors for +CPU_CORE_0 and +CPU_CORE_1 near the CPU socket.

+CPU_CORE_0: Capacitor C40 (330U_X_2VM_R6M) and C39 (330U_X_2VM_R6M) are connected to the +CPU_CORE_0 pin and ground.

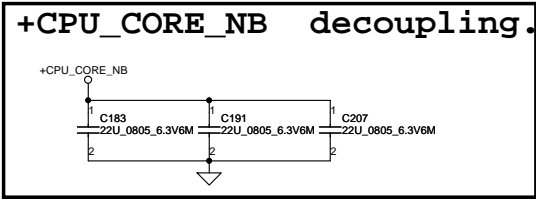
+CPU_CORE_1: Capacitor C36 (330U_X_2VM_R6M) and C37 (330U_X_2VM_R6M) are connected to the +CPU_CORE_1 pin and ground.

Under CPU Socket

Diagram showing decoupling capacitors for +CPU_CORE_0 and +CPU_CORE_1 under the CPU socket.

+CPU_CORE_0: Capacitors C184 (22U_0805_6.3V6M), C206 (22U_0805_6.3V6M), C199 (22U_0805_6.3V6M), and C205 (22U_0805_6.3V6M) are connected to the +CPU_CORE_0 pin and ground. Capacitors C198 (0.22U_0603_16V4Z), C95 (1U_0402_25V4Z), and C196 (180P_0402_50V8J) are connected to the +CPU_CORE_0 pin and ground.

+CPU_CORE_1: Capacitors C179 (22U_0805_6.3V6M), C180 (22U_0805_6.3V6M), C170 (22U_0805_6.3V6M), and C186 (22U_0805_6.3V6M) are connected to the +CPU_CORE_1 pin and ground. Capacitors C185 (0.22U_0603_16V4Z), C67 (1U_0402_25V4Z), and C163 (180P_0402_50V8J) are connected to the +CPU_CORE_1 pin and ground.



Under CPU Socket

Between CPU Socket and DIMM

180PF Qt'y follow the distance between CPU socket and DIMM0. <2.5inch>

220U_Y_4VM
NBO CAP

VTT decoupling.

change to polymer

Near Power Supply

+0.9V

C517

C510

220U_D2_4VM_R15

22U_0805_6.3V6M

+0.9V

C407

C406

C411

C412

C156

C155

C154

C157

4.7U_0805_10V4Z

4.7U_0805_10V4Z

0.22U_0603_16V4Z

0.22U_0603_16V4Z

1000P_0402_25V8J

1000P_0402_25V8J

180P_0402_50V8J

180P_0402_50V8J

Near CPU Socket Right side.

+0.9V

C499

C498

C491

C492

C478

C485

C479

C486

4.7U_0805_10V4Z

4.7U_0805_10V4Z

0.22U_0603_16V4Z

0.22U_0603_16V4Z

1000P_0402_25V8J

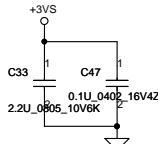
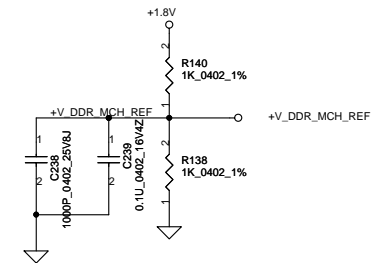
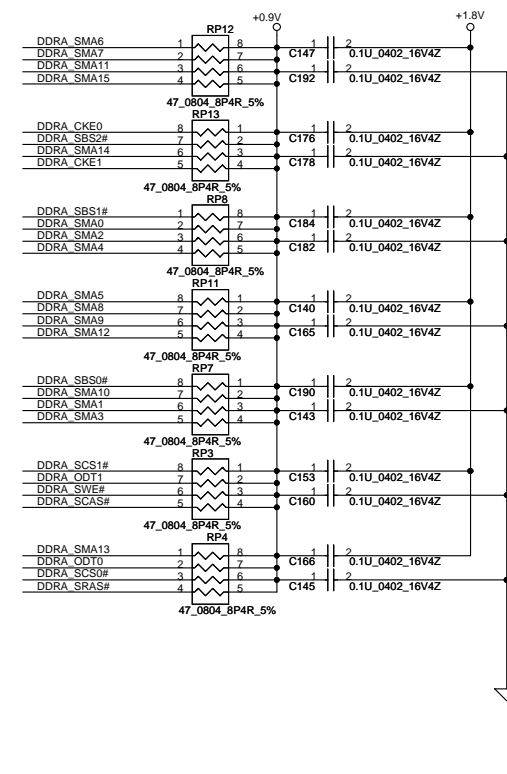
1000P_0402_25V8J

180P_0402_50V8J

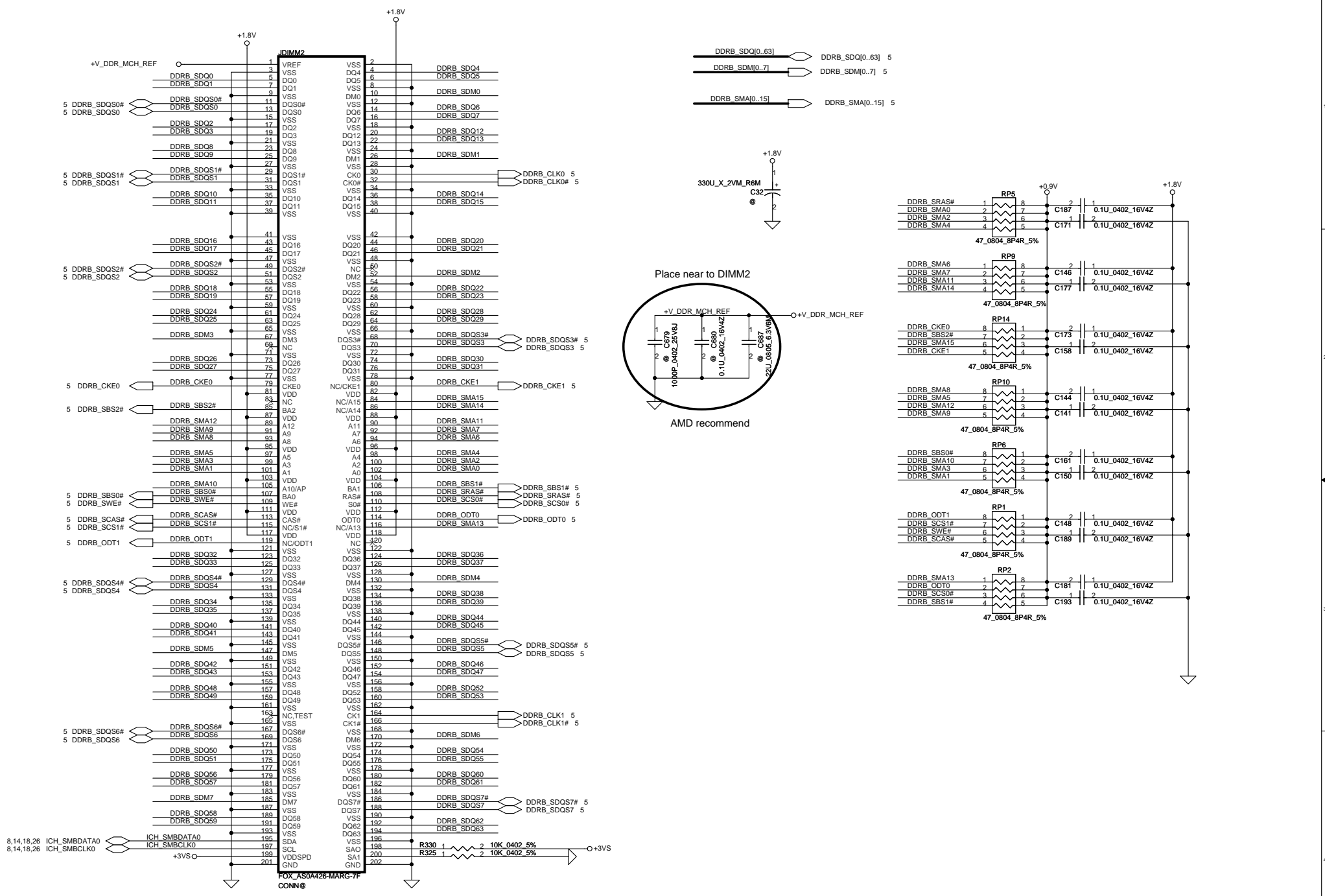
180P_0402_50V8J

Near CPU Socket Left side.

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				Doc Cust	401575	
Date:				Tuesday, August 19, 2008	Sheet	7 of 45

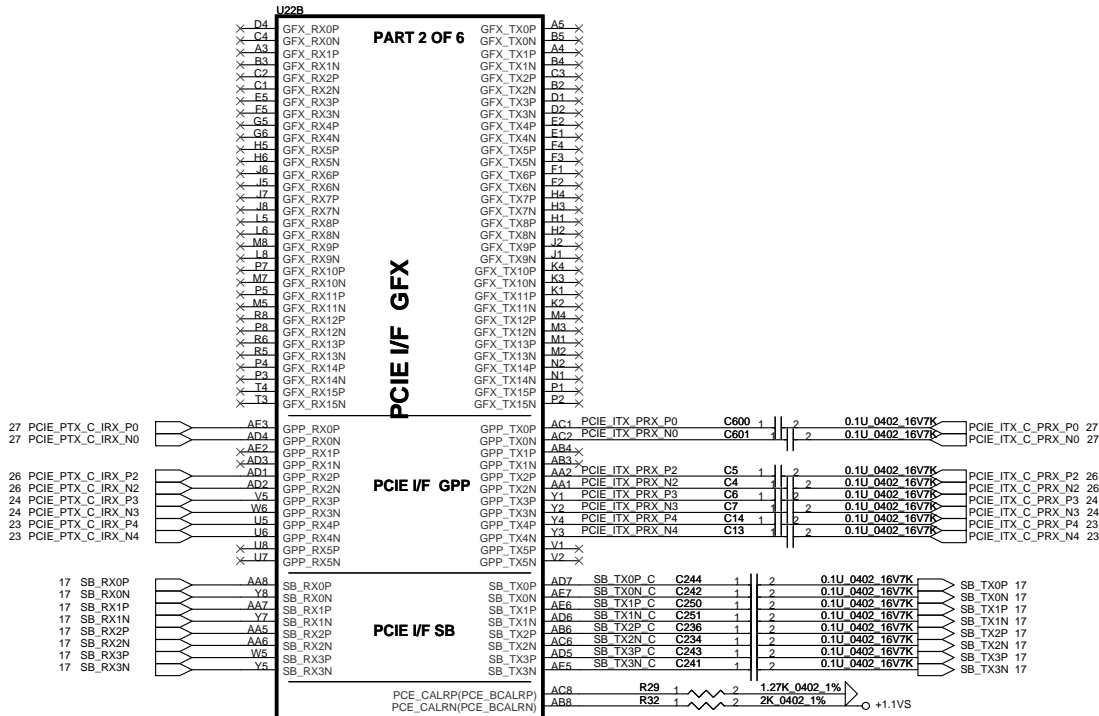


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				Customer	D	
				401575		
Date:	Tuesday, August 19, 2008	Sheet	8	of	45	



DIMM1 REV H:9.2mm (BOT)

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				401575	
				Date: Tuesday, August 19, 2008	Sheet 9 of 45



RS780M_FCBGA528

RS780MN-SA00002DR30 Ver:A13

RS780M Display Port Support (muxed on GFX)

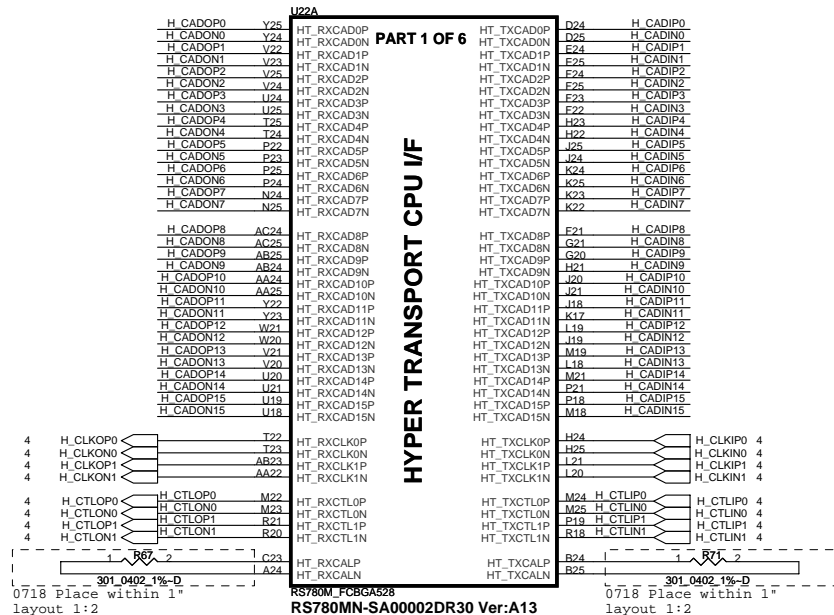
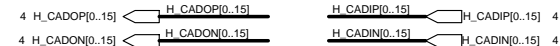
DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

New Card

Minil

GLAN

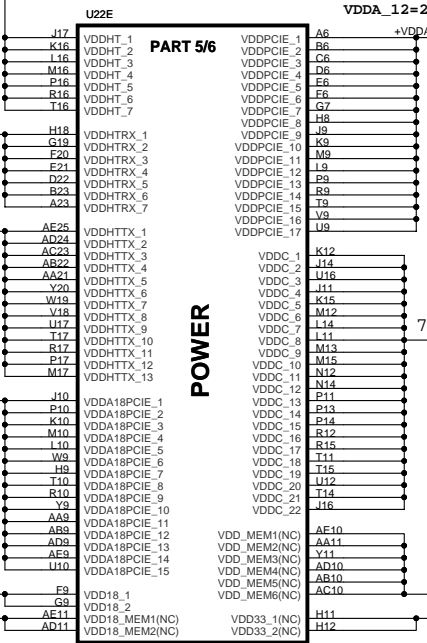
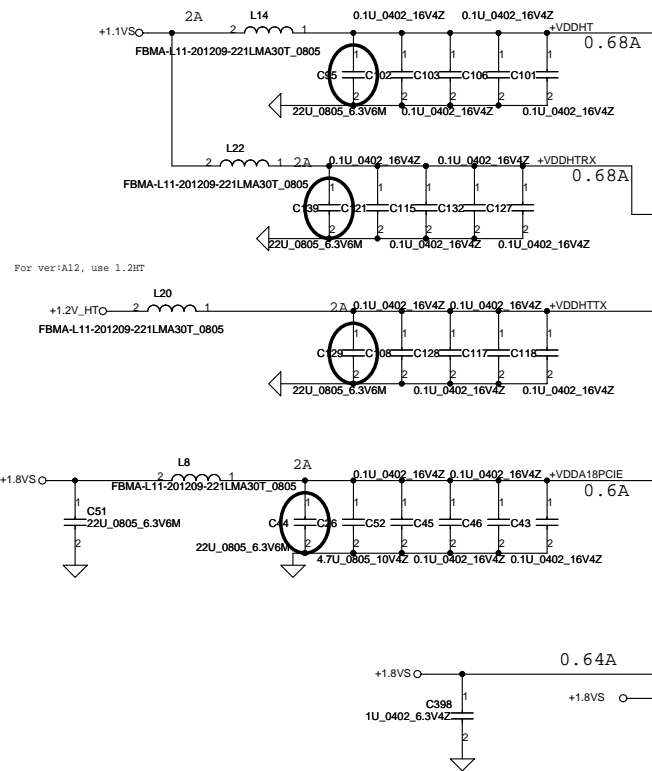
Card Reader

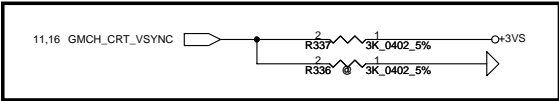


RS780M_FCBGA528

RS780MN-SA00002DR30 Ver:A13

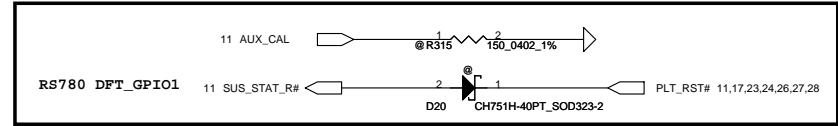
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				401575	
				Date: Tuesday, August 19, 2008	Sheet 10 of 45





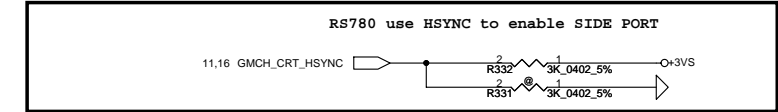
DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO. (VSYNC)
1 : Disable (RS780)
0 : Enable (Rs780)



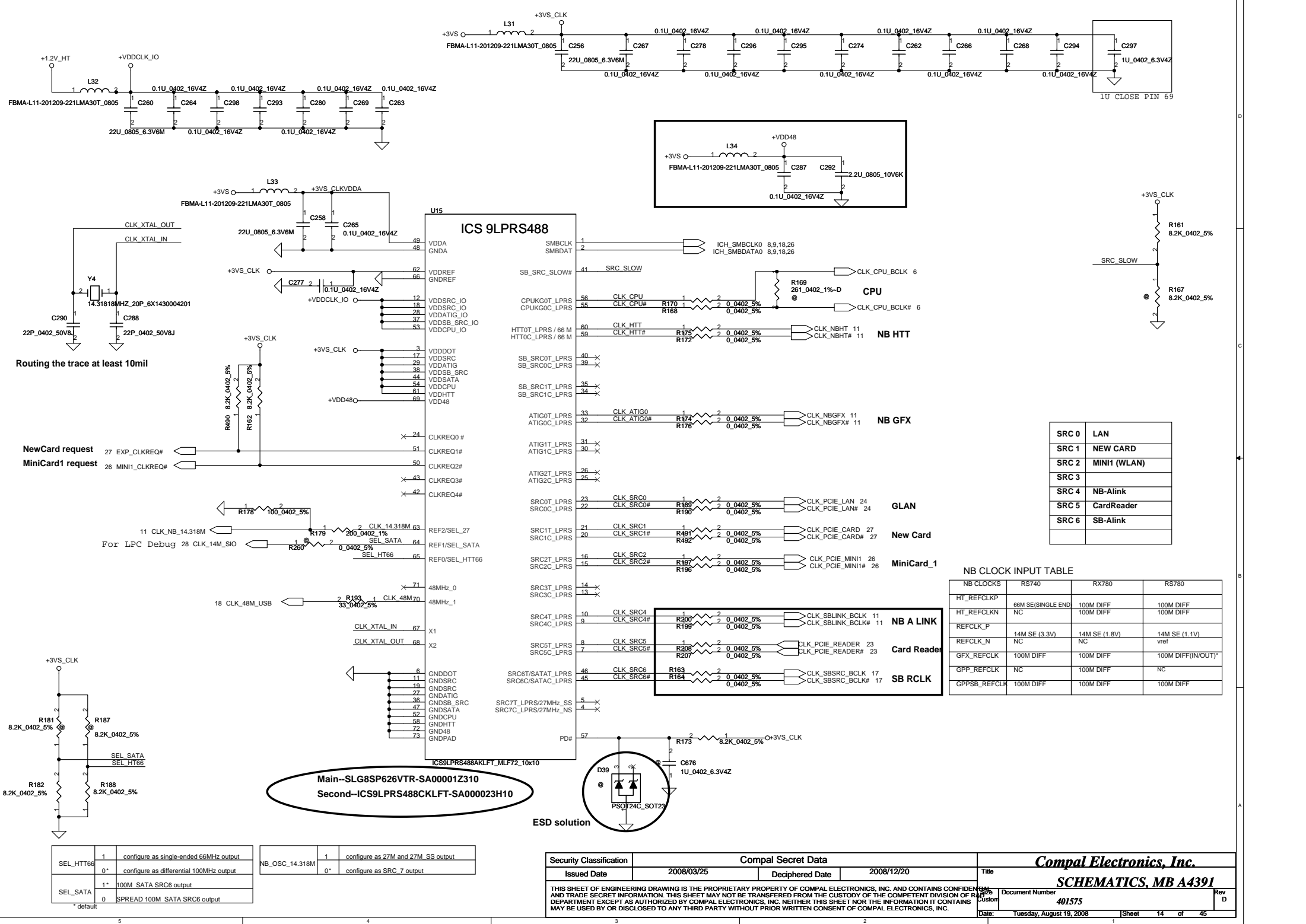
DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RS740/RX780: DFT_GPIO1 RS780:SUS_STAT



RS780 use HSYNC to enable SIDE PORT

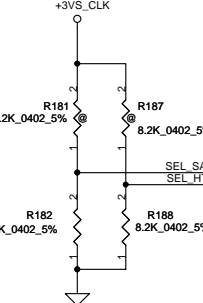
RS740/RS780: Enables Side port memory (RS780 use HSYNC#)
0. Enable (RS780)
1 : Disable(RS780)



Routing the trace at least 10mil

NewCard request
MiniCard1 request

For LPC Debug



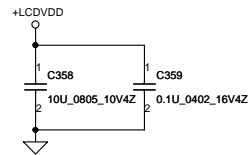
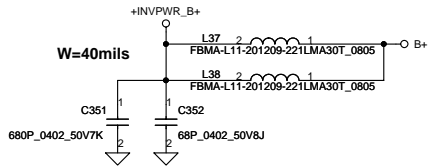
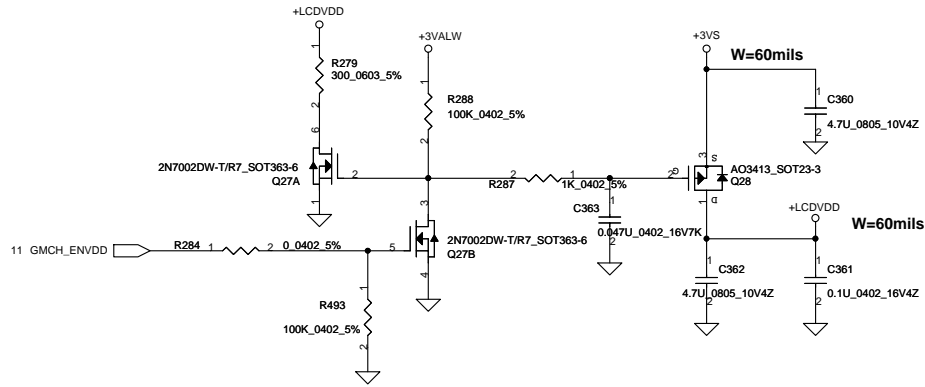
SEL_HTT66	1	configure as single-ended 66MHz output
	0*	configure as differential 100MHz output
SEL_SATA	1*	100M SATA SRC6 output
	0	SPREAD 100M SATA SRC6 output

* default

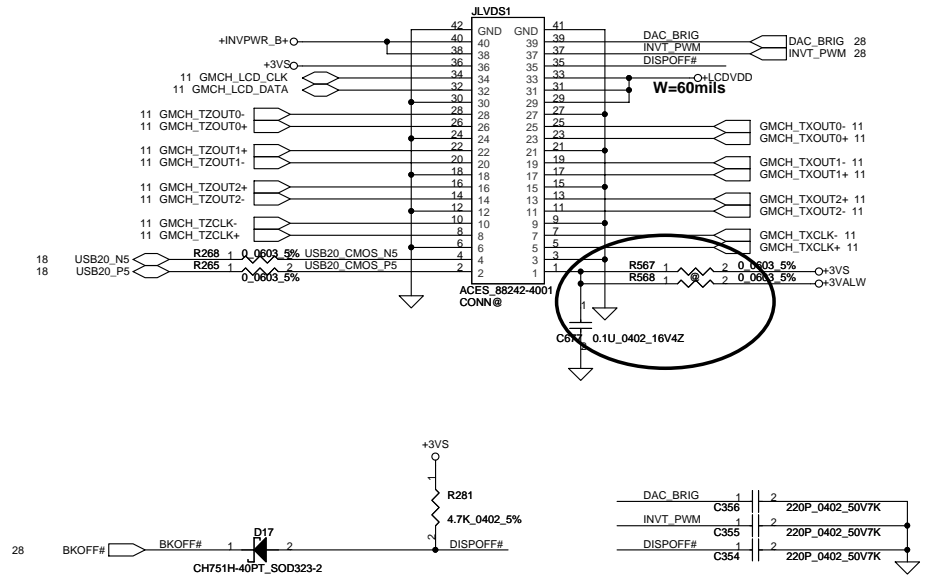
NB_OSC_14.318M	1	configure as 27M and 27M_SS output
	0*	configure as SRC_7 output

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				Date:	Tuesday, August 19, 2008	Sheet 14 of 45

LCD POWER CIRCUIT

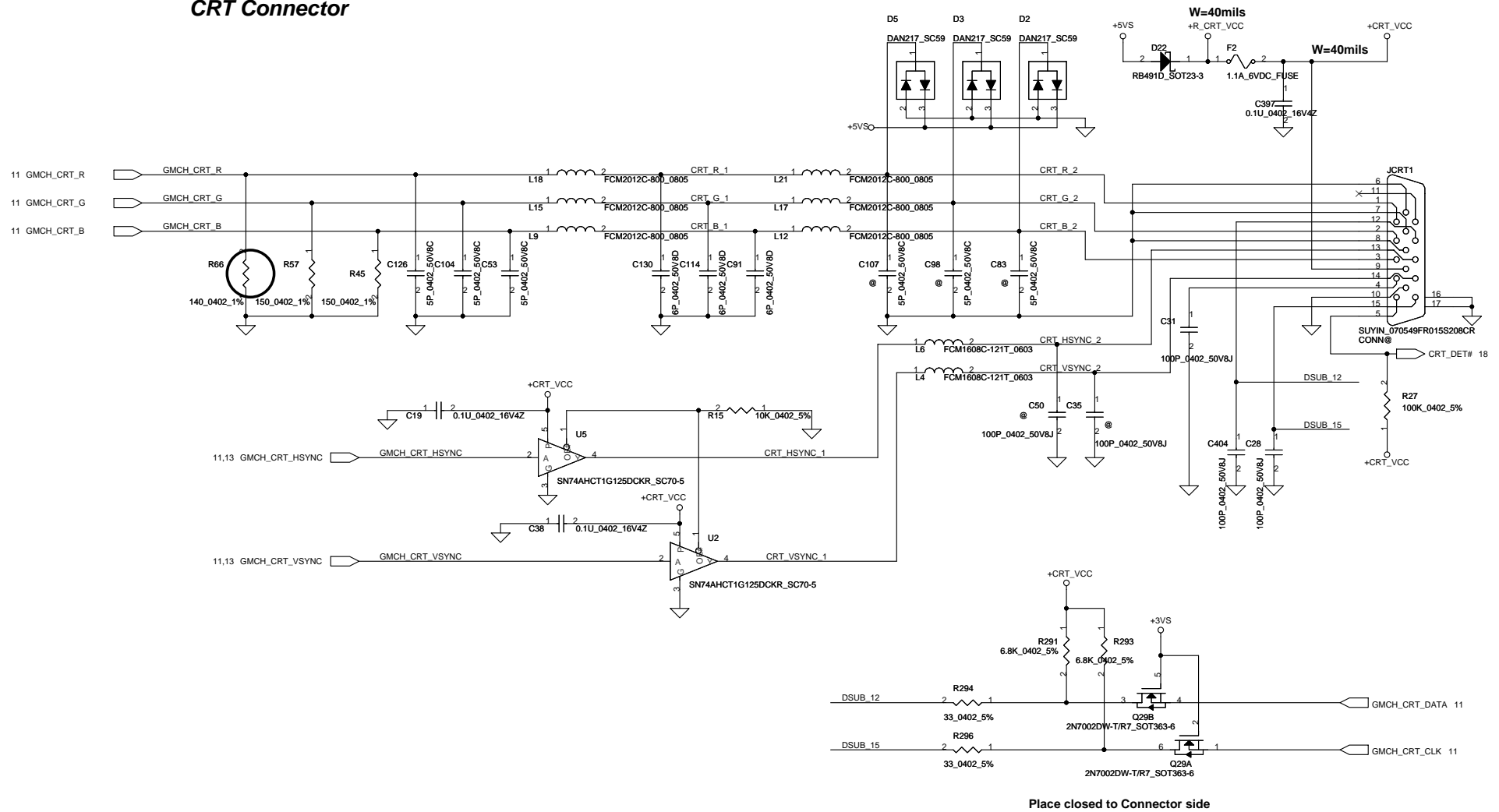


LCD/PANEL BD. Conn.

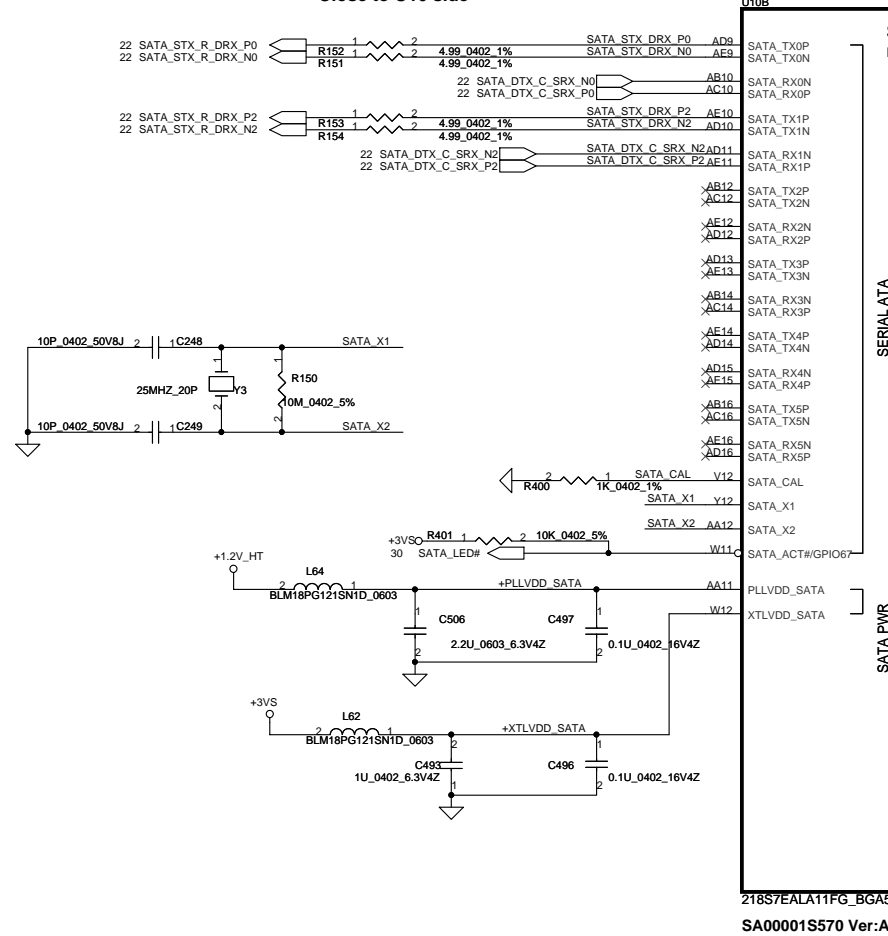
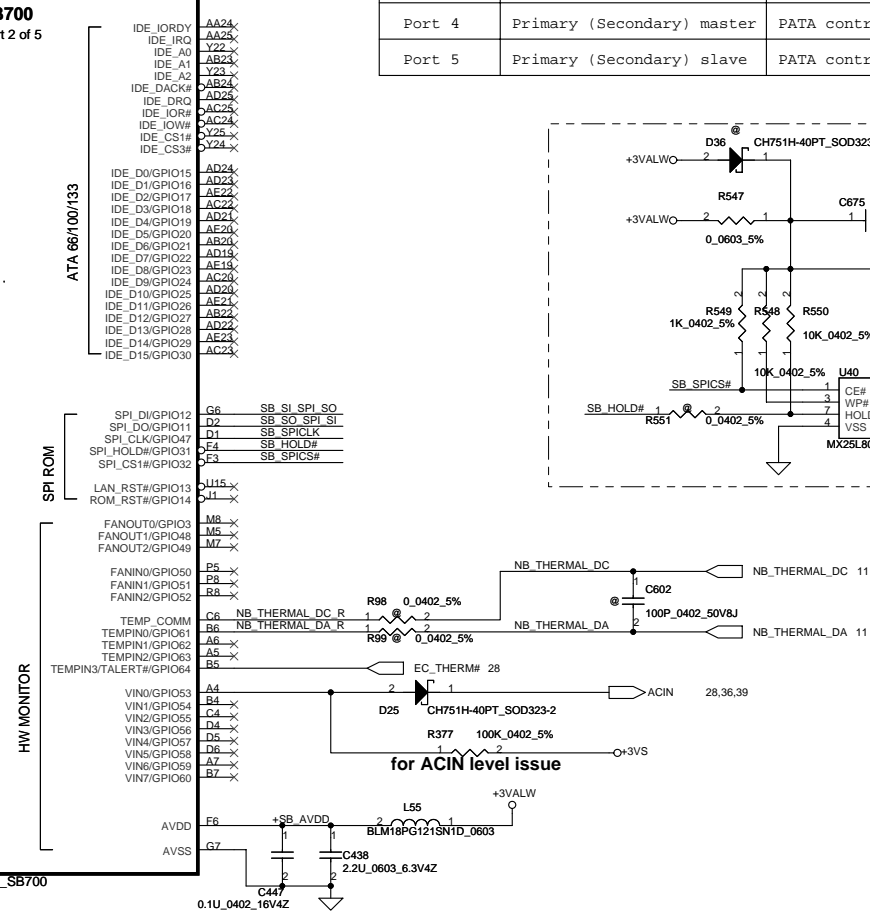


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								401575			
								Date			
								Tuesday, August 19, 2008			
								Sheet 15 of 45			

CRT Connector

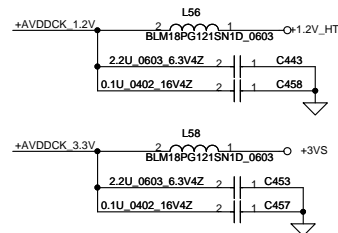
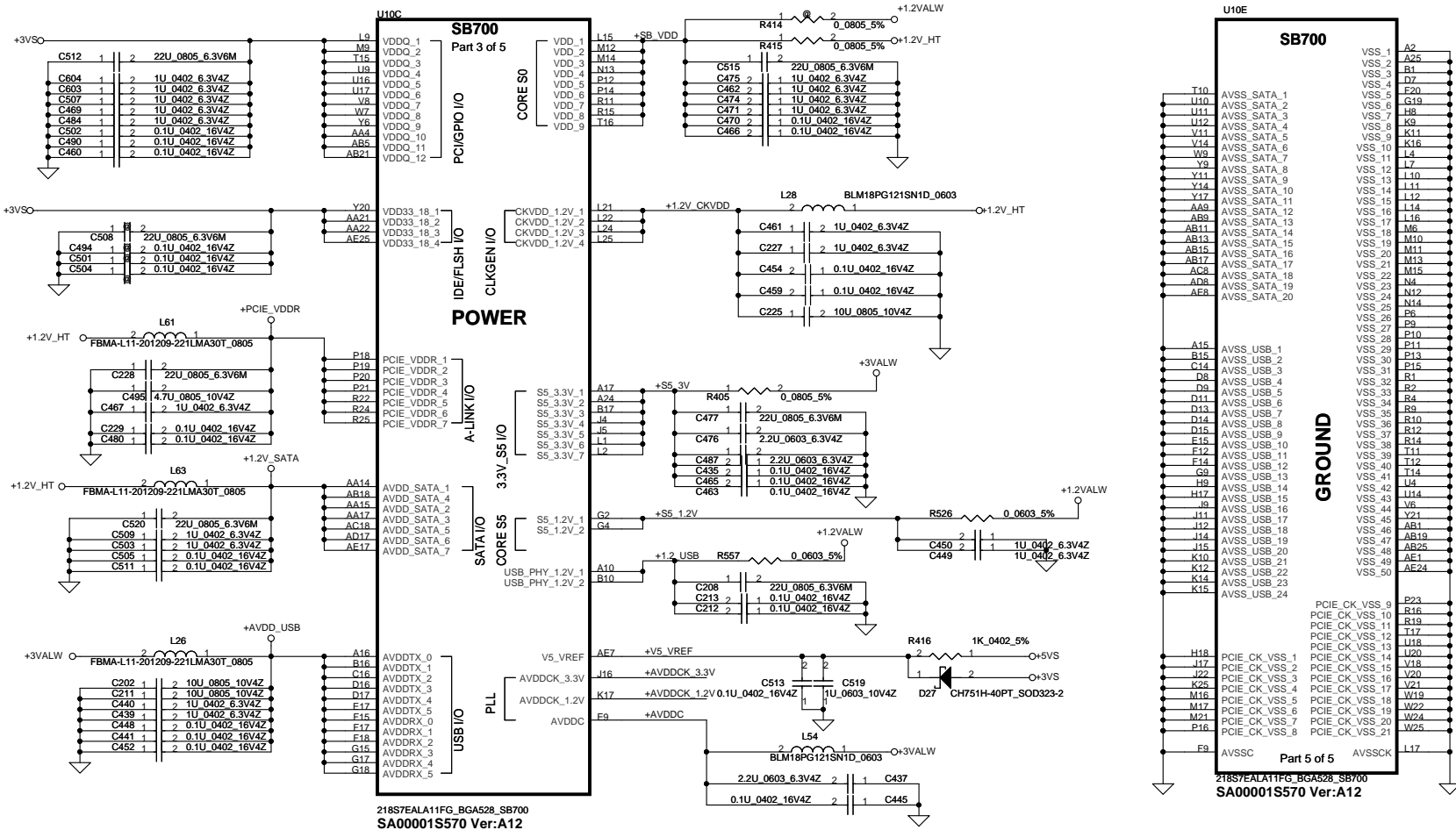


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								Document Number	
								401575	
Date		Tuesday, August 19, 2008		Sheet		16		of 45	

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				Document Number	
				401575	
Date:	Tuesday, August 19, 2008	Sheet	19	of	45

FOR Version A11 pop 1.2VALW, A12 use 1.2V_HT

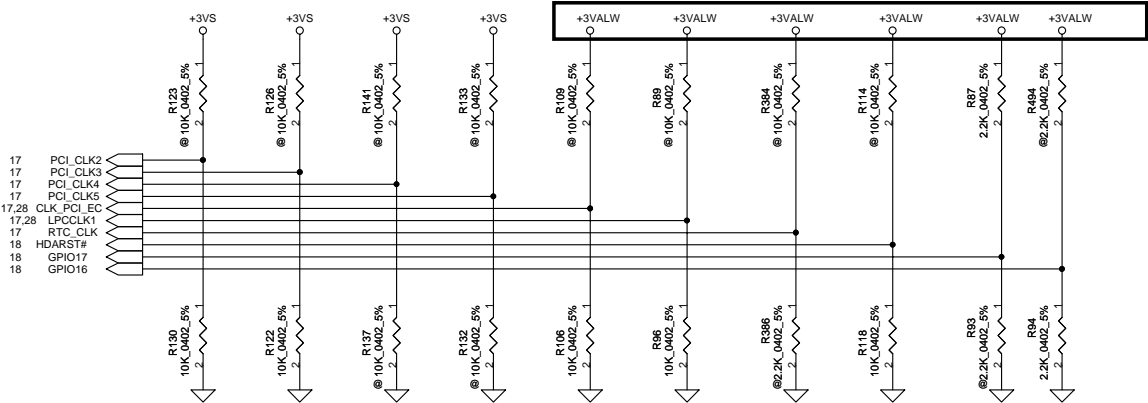


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				401575	
				Date: Tuesday, August 19, 2008	Sheet 20 of 45

REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

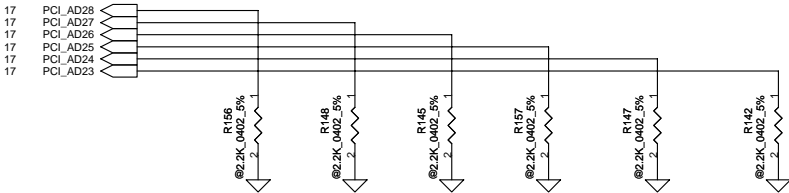
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	L,H = LPC ROM (Default L,NC) L,L = FWH ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		



DEBUG STRAPS

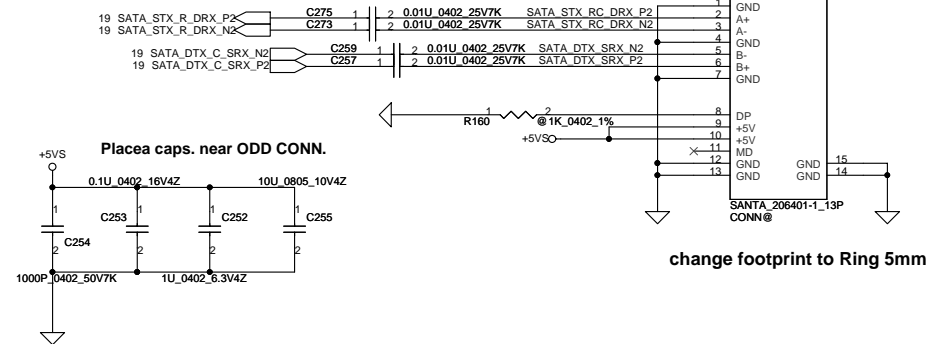
SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



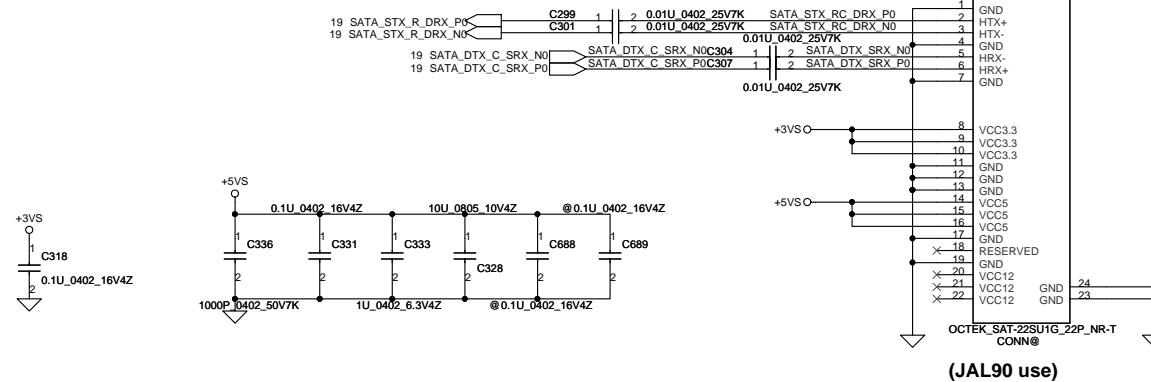
SATA ODD Conn.

Close to Conn side

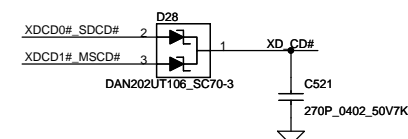
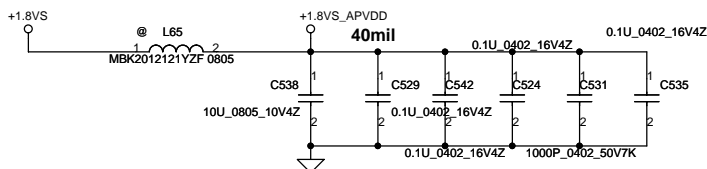


SATA HDD Conn.

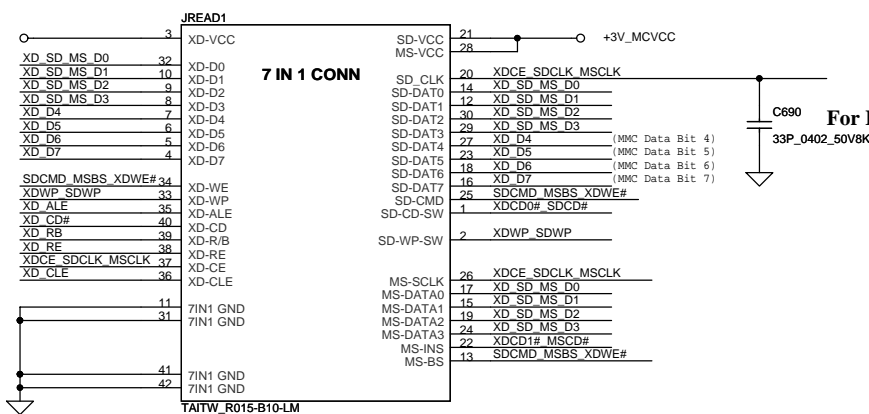
Close to Conn side



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				Date	Tuesday, August 19, 2008
				Sheet	22 of 45



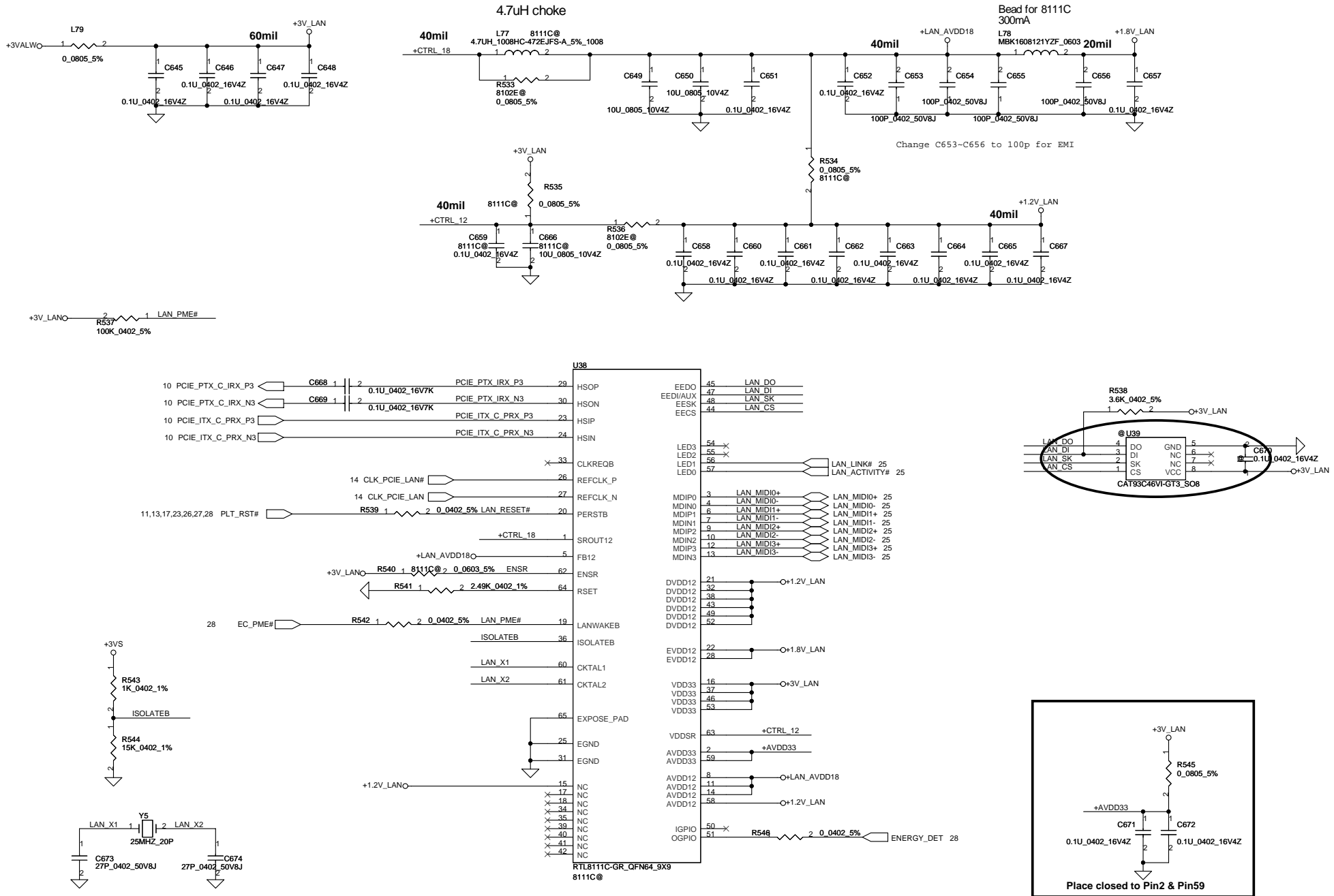
Memory Card Power Switch



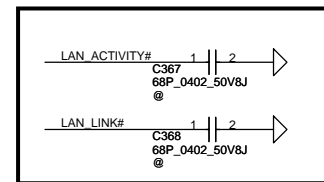
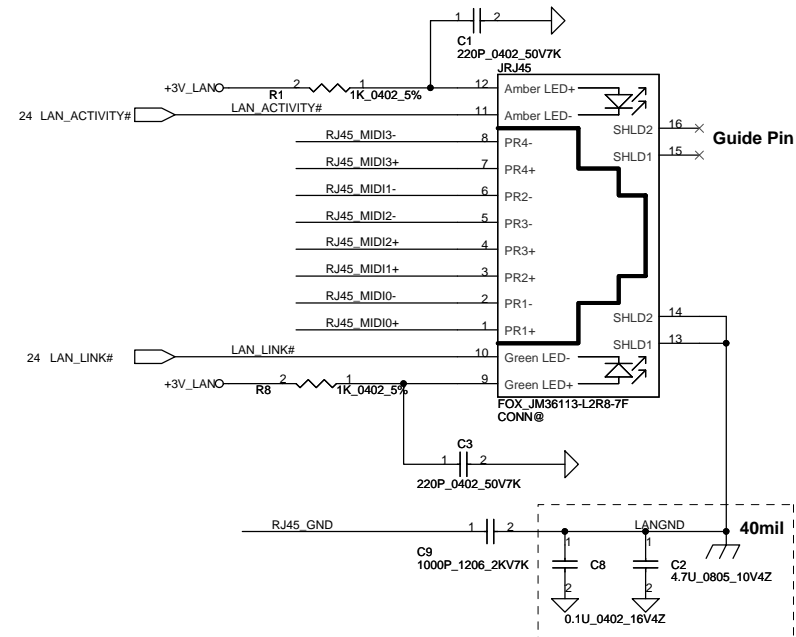
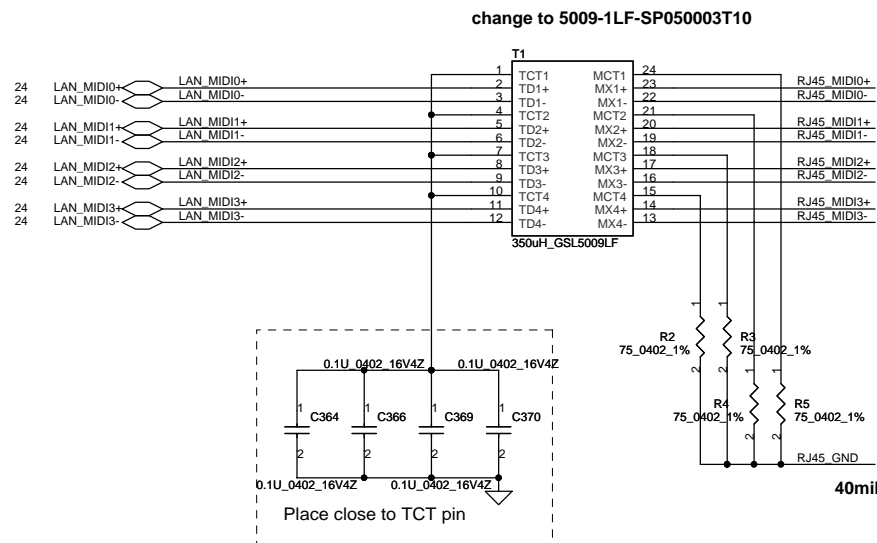
For EMI
402_50V8K

**C0/B0 both remove 2061
check Frank**

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				Customer	401575
				Date:	Tuesday, August 19, 2008
				Sheet	23 of 45

LAN RTL8111C/8102E

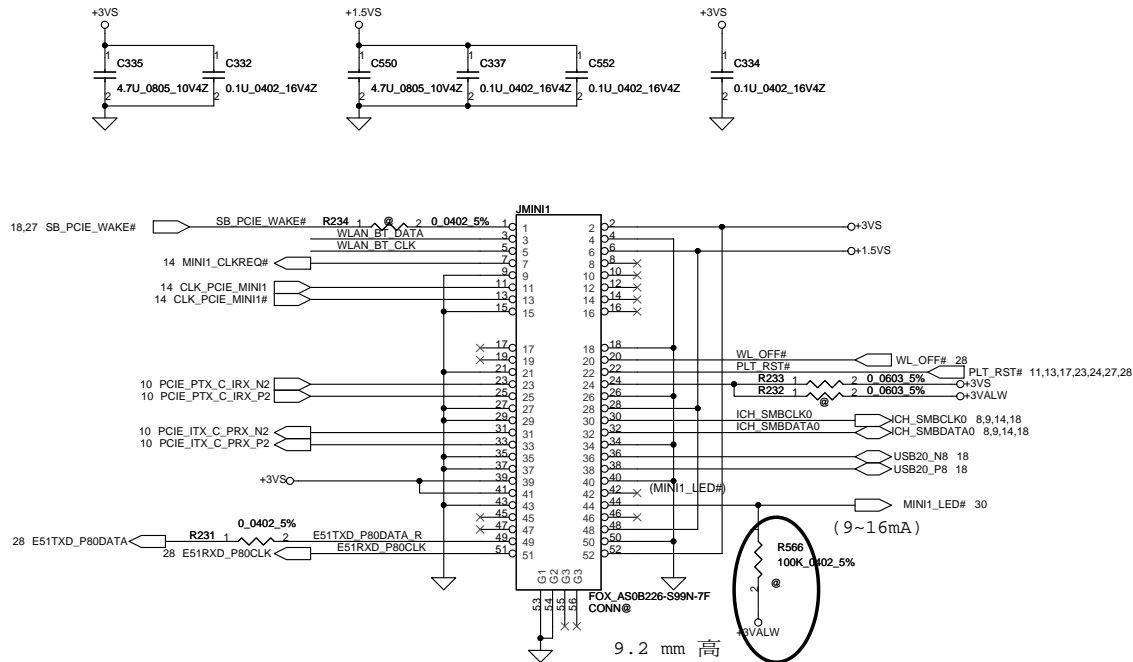
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				Customer Number 401575	
Date: Tuesday, August 19, 2008		Sheet 24 of 45			



For EMI

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				Date:	Tuesday, August 19, 2008
				Sheet	25 of 45

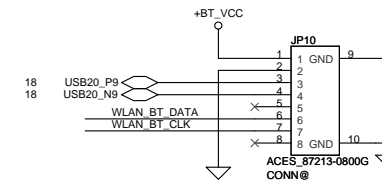
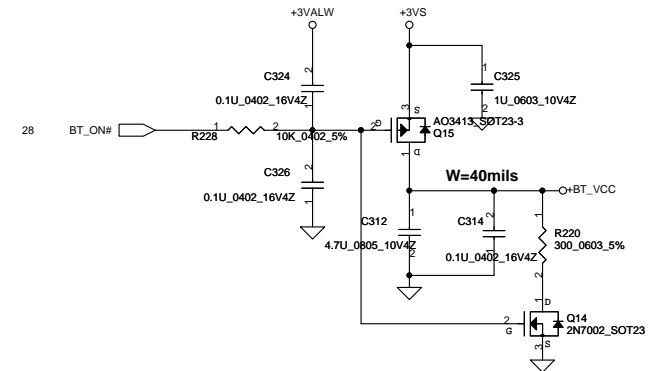
For Wireless LAN



Mini Card Power Rating

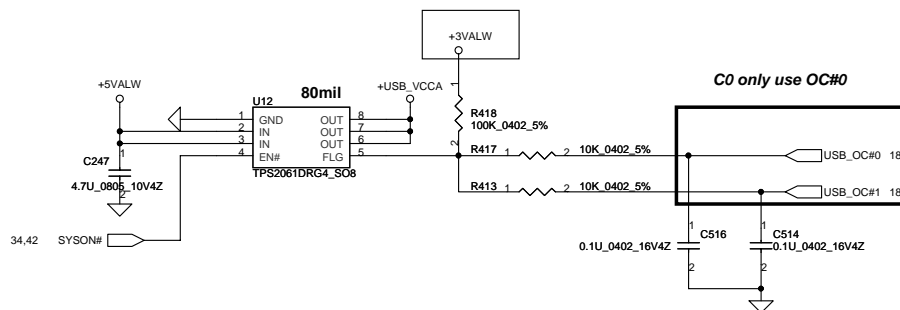
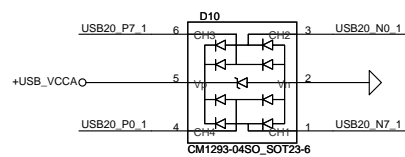
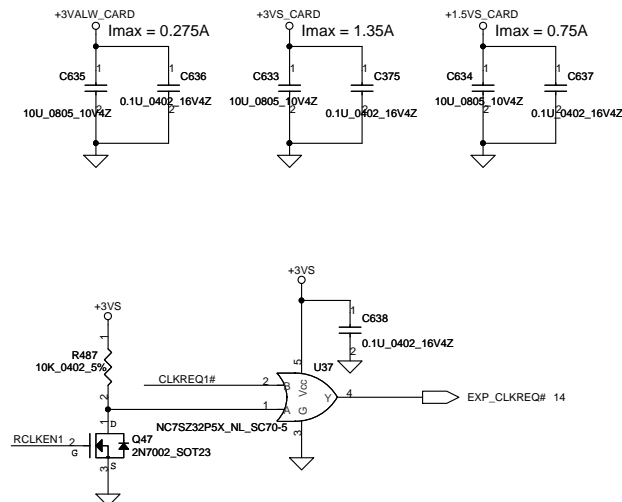
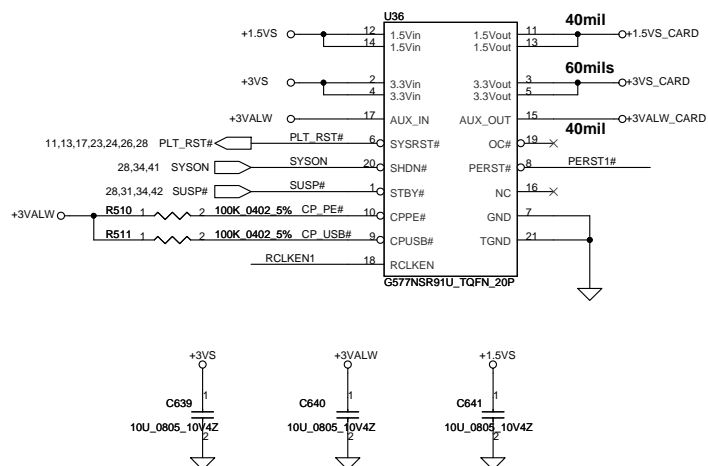
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

Bluetooth Conn.

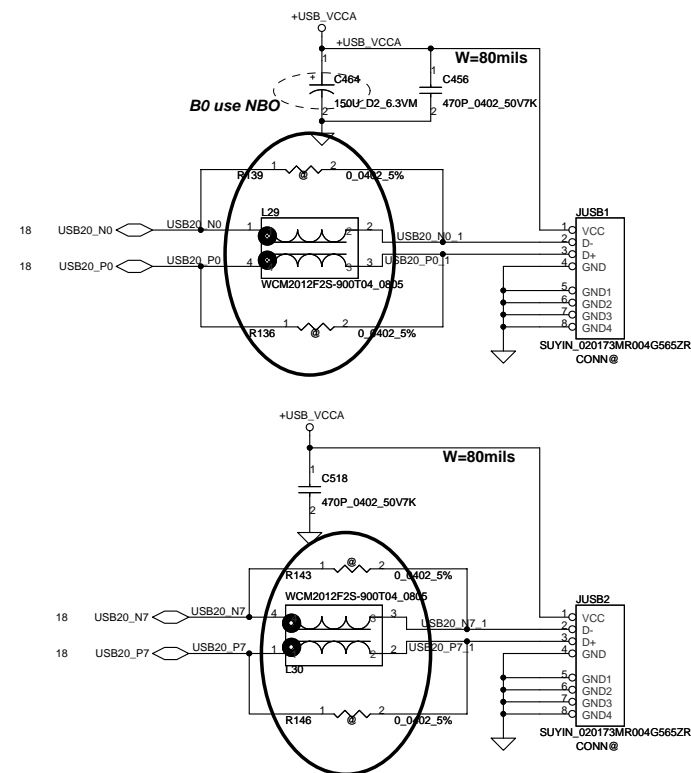
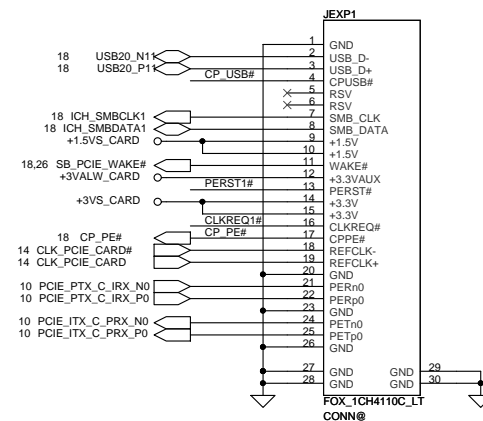


for 線材, 7, 8pin不打

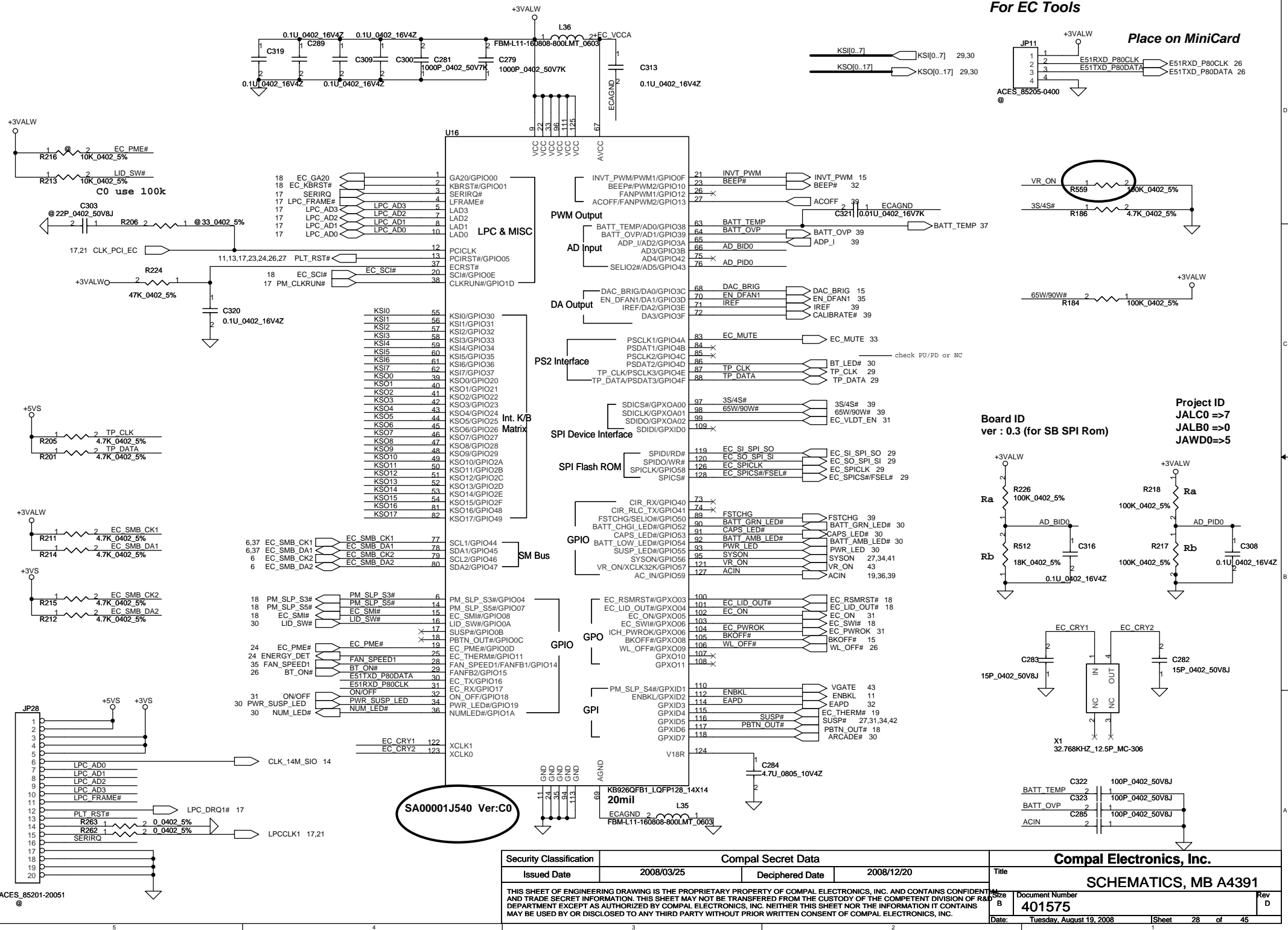
New Card Power Switch

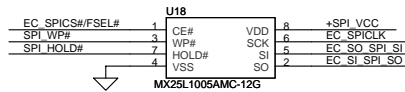
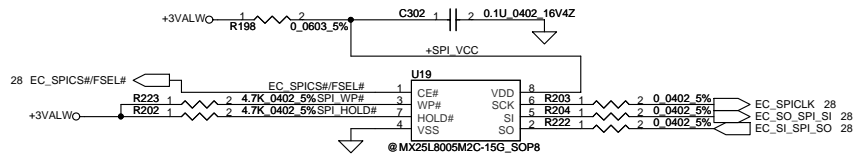


New Card Socket (Left/TOP)



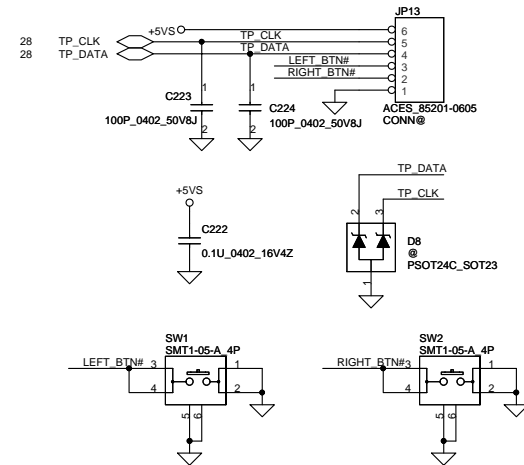
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				401575	
Date:	Tuesday, August 19, 2008	Sheet	27	of	45





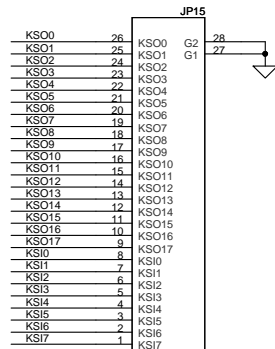
Reserved for BIOS simulator.
Footprint SO8

To TP/B Conn.



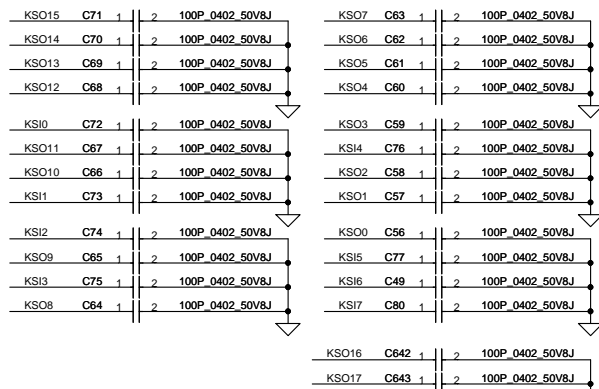
INT_KBD Conn.

(Left)

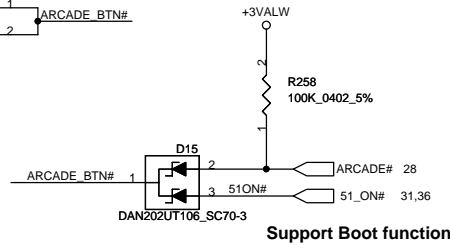
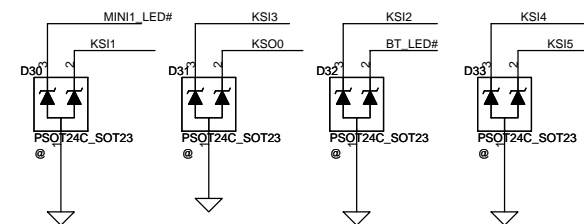
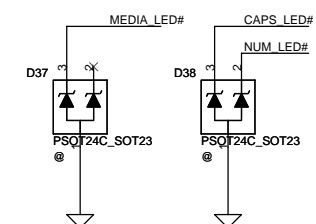
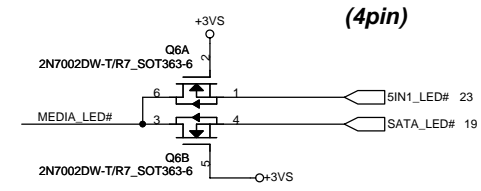
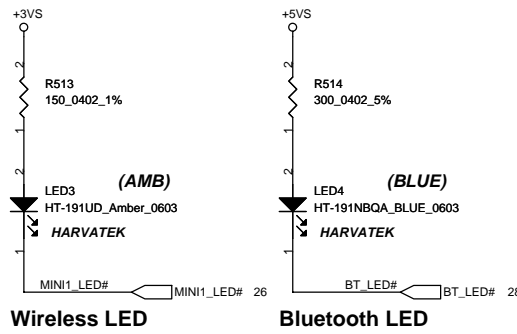
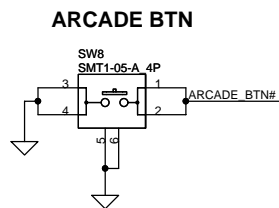
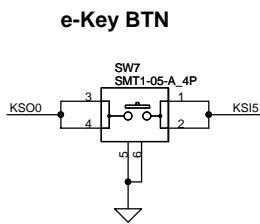
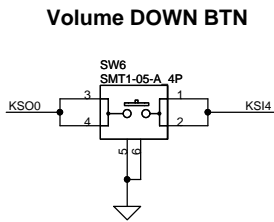
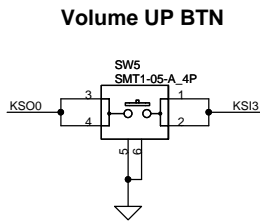
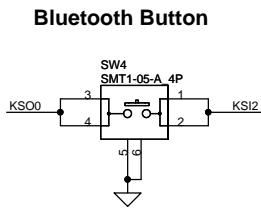
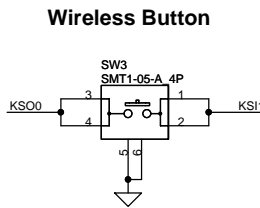
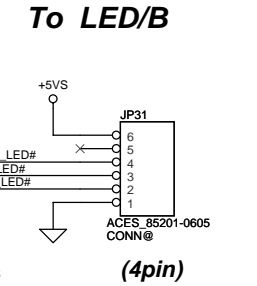
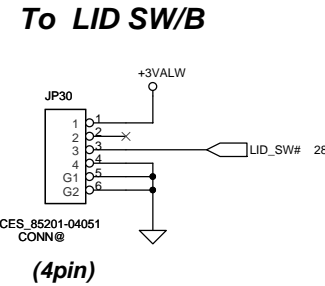
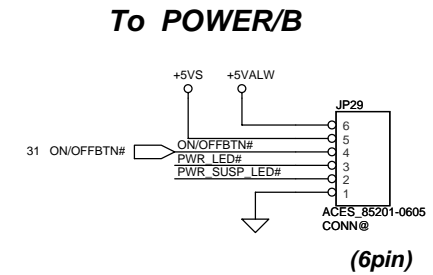
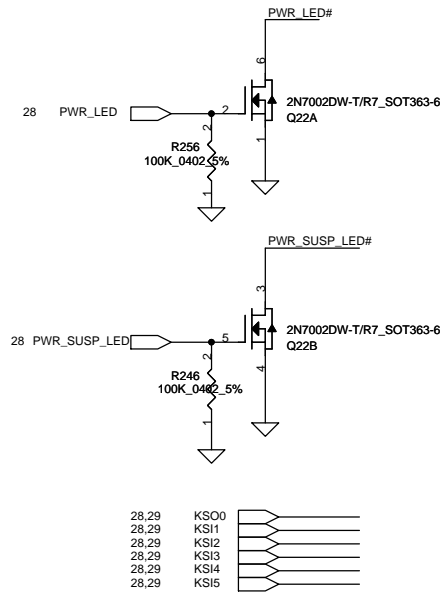
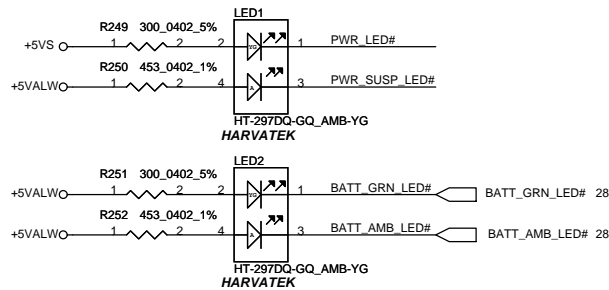


(Right)

ACES_88747-2601
CONN@



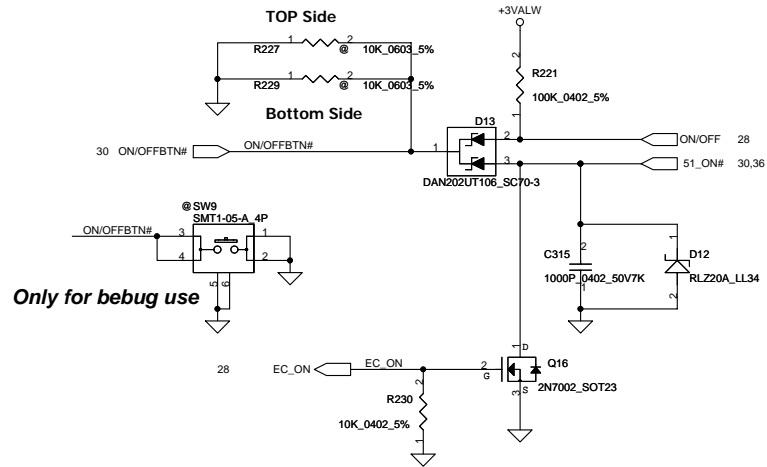
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				401575
				Rev D
				Date: Tuesday, August 19, 2008
				Sheet 29 of 45



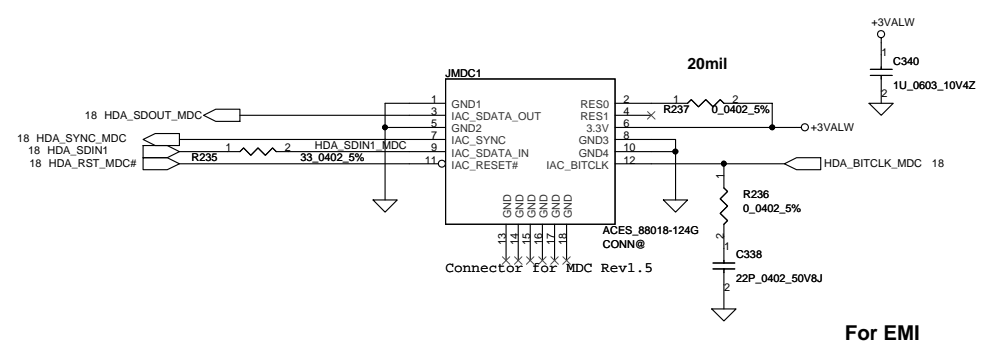
KSO0	
KSI1	Wireless BTN
KSI2	BT BTN
KSI3	Volume UP
KSI4	Volume DOWM
KSI5	e-Key BTN
KSI6	

Power Button

ON/OFF switch

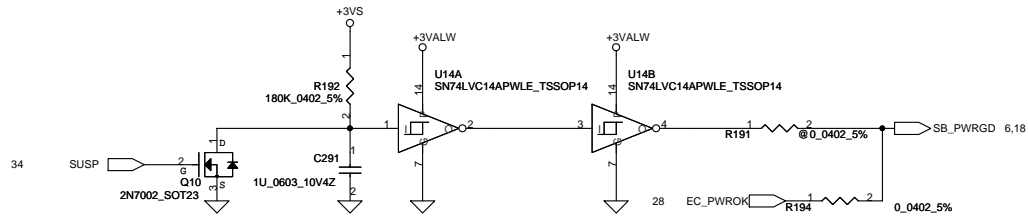


HDA MDC Conn.

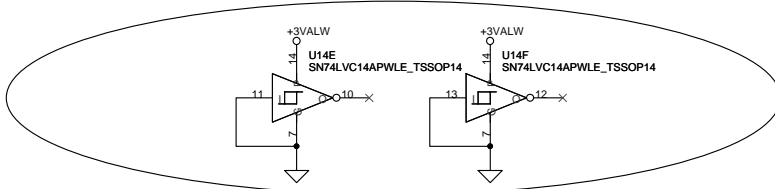
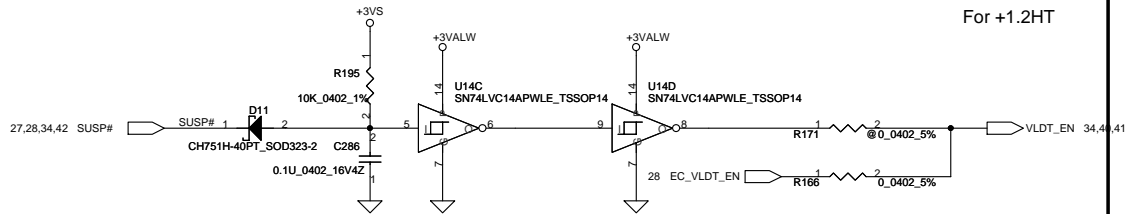


Power ON Circuit

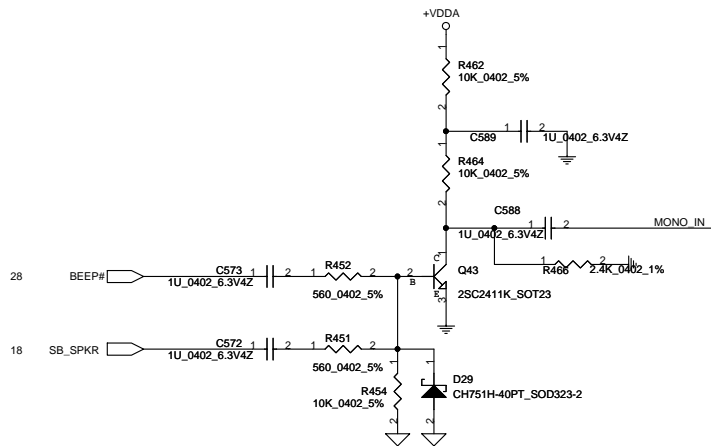
For South Bridge



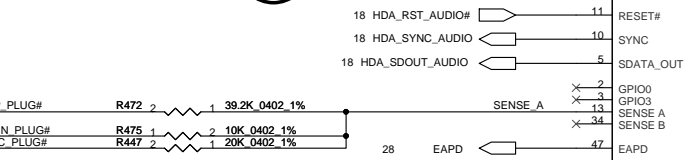
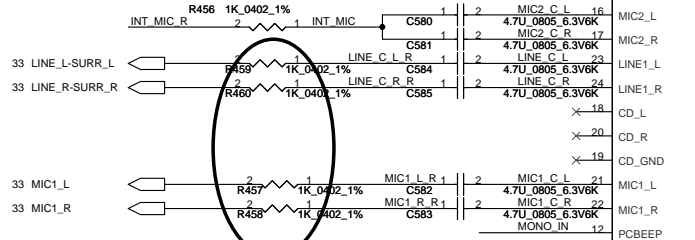
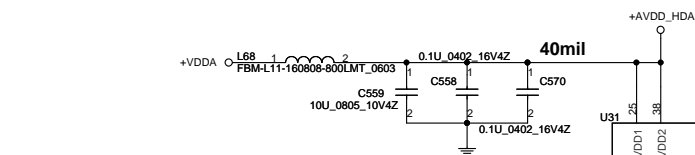
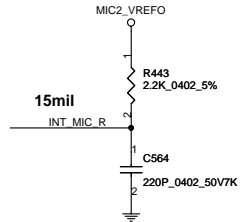
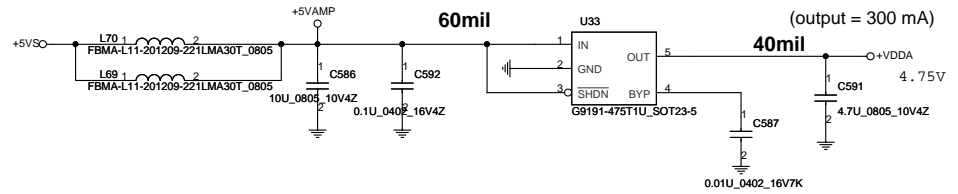
For +1.2HT



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				Date:	Tuesday, August 19, 2008
				Sheet	31 of 45



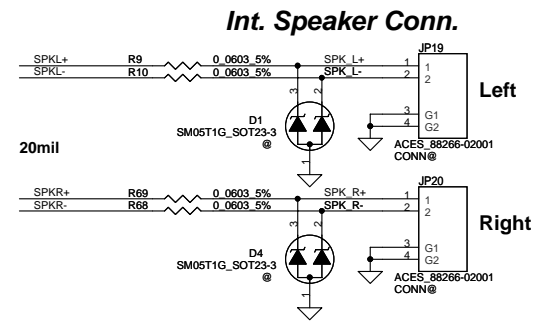
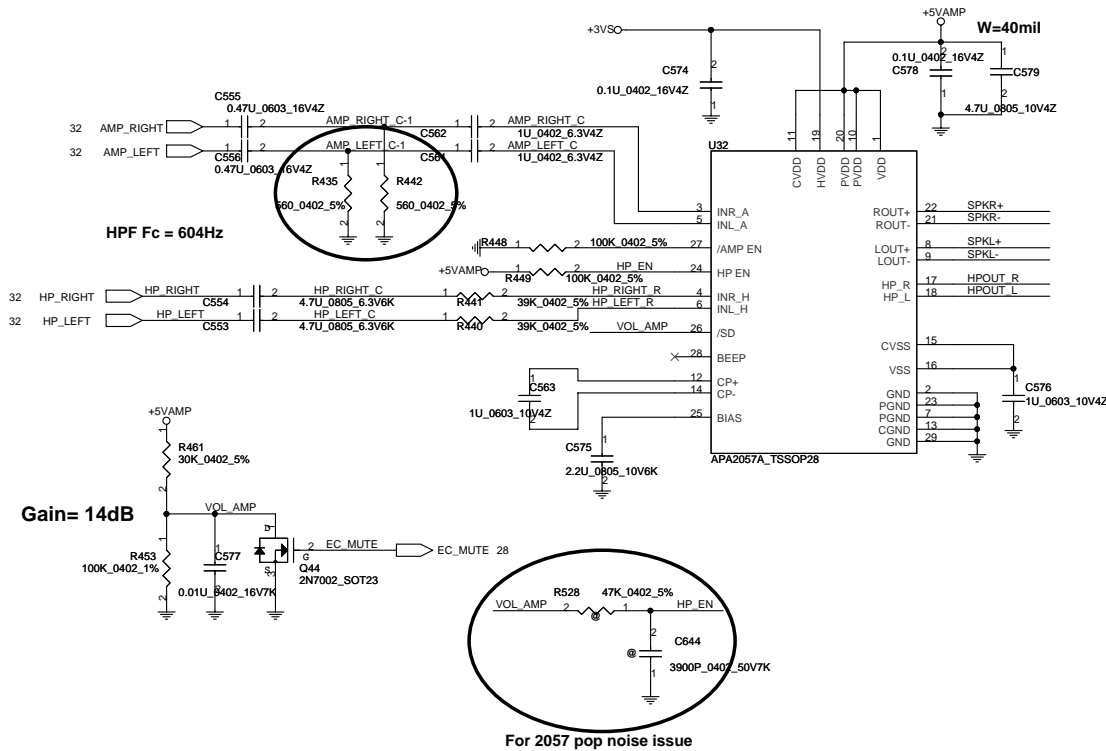
HD Audio Codec



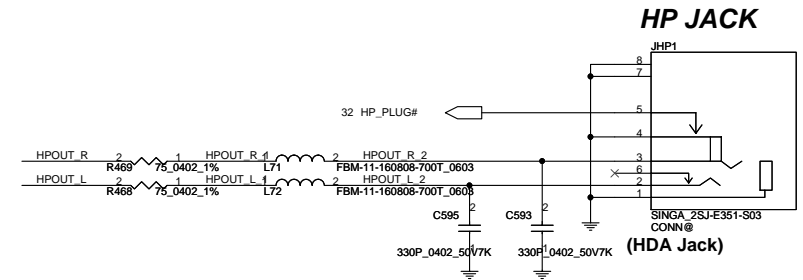
33 HP_PLUG#
33 LINEIN_PLUG#
33 MIC_PLUG#

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

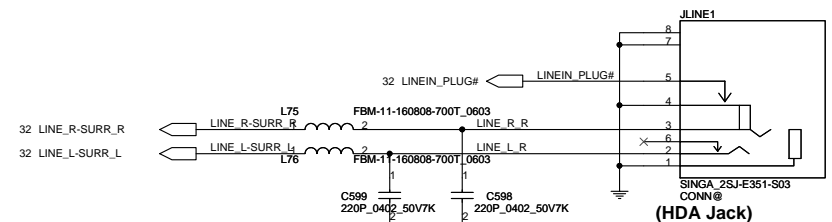
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Sheet 32 of 45				Document Number 401575				Rev D			



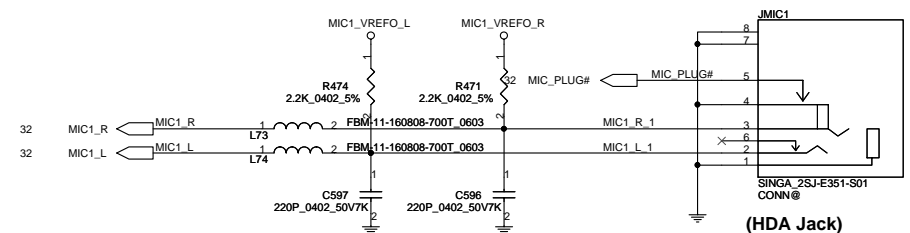
S/PDIF Out JACK LINE Out/Headphone Out



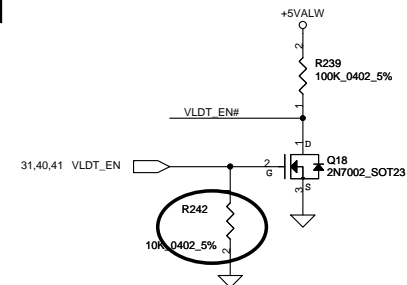
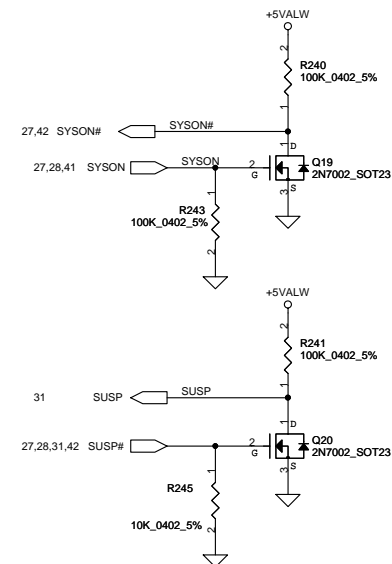
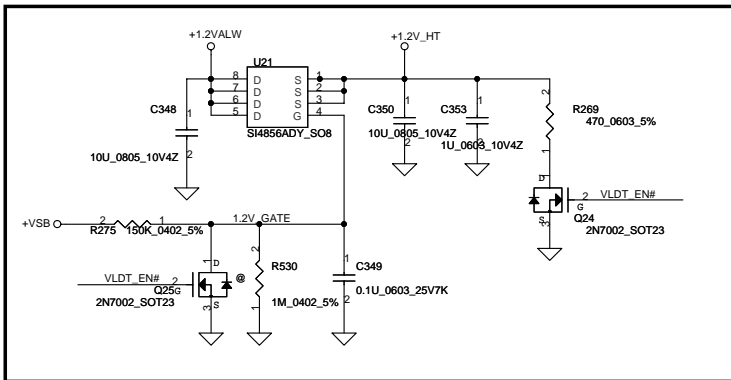
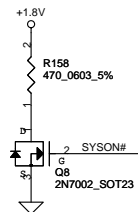
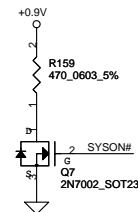
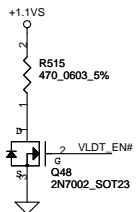
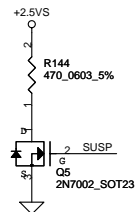
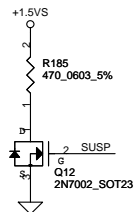
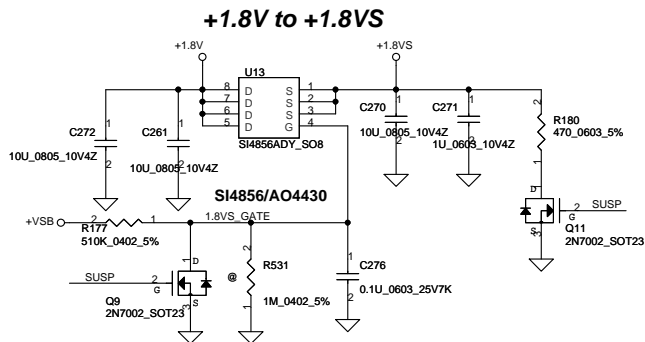
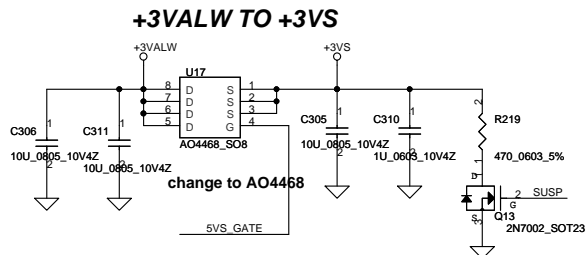
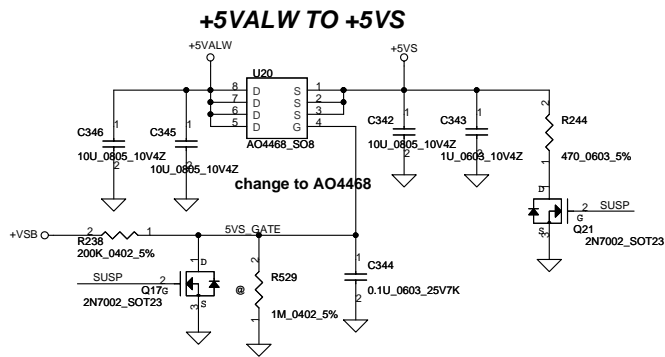
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MIC JACK

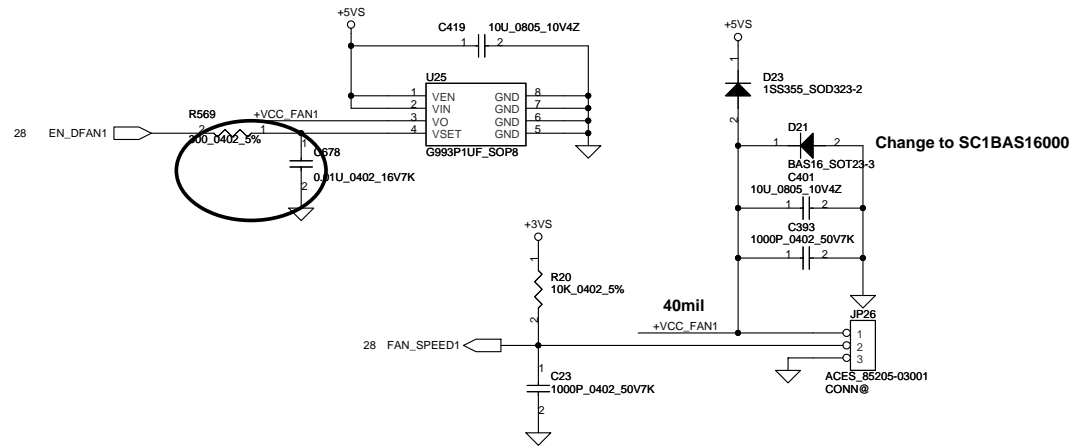


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						Document Number		Rev D	
						401575			
						Date: Tuesday, August 19, 2008		Sheet 33 of 45	

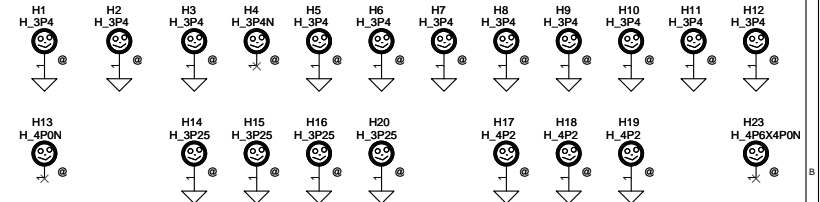
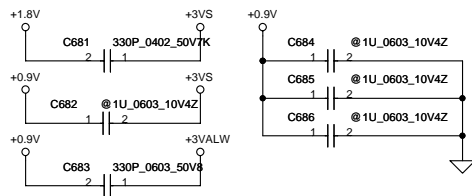


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				Date:	Tuesday, August 19, 2008	Sheet 34 of 45

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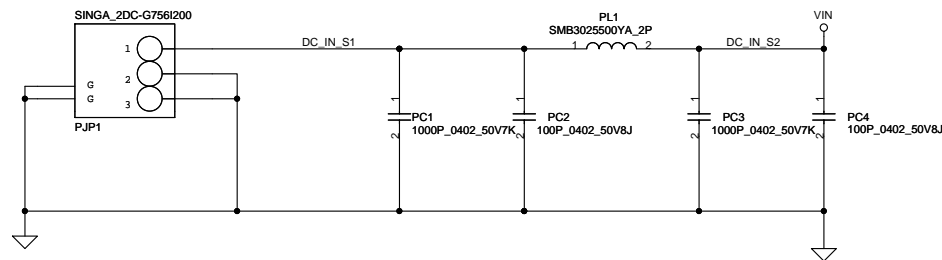


EMI solution

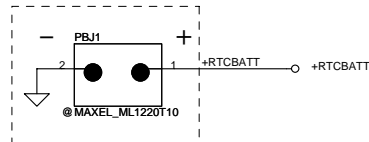


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Document Number				Rev D
401575				
Date: Tuesday, August 19, 2008				Sheet 35 of 45

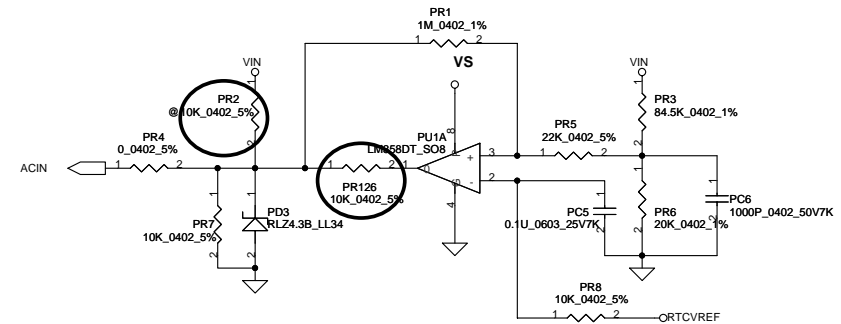
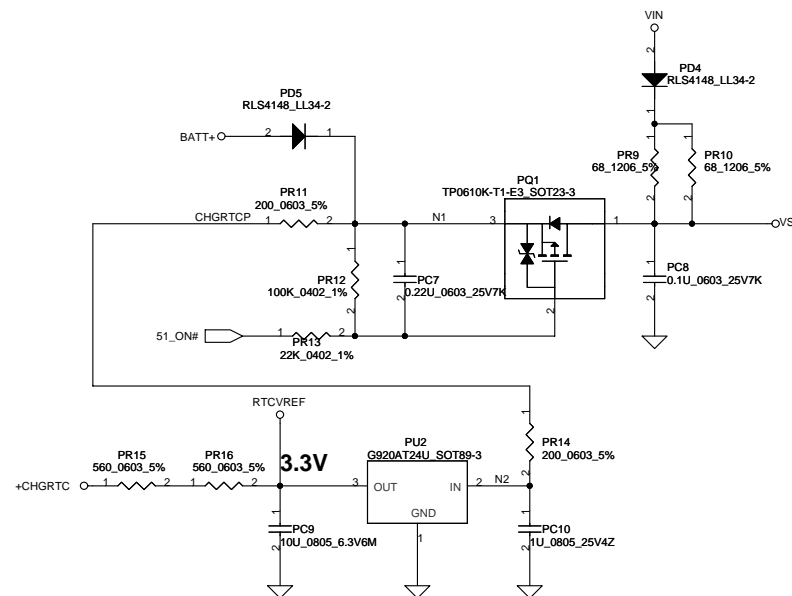
DC231000500



RTC Battery

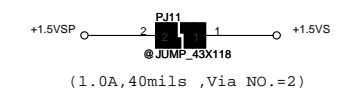
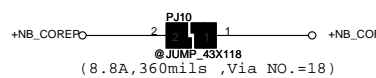
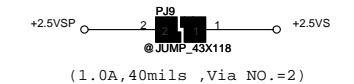
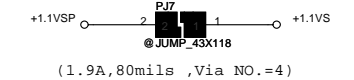
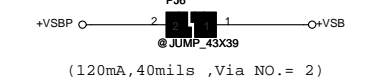
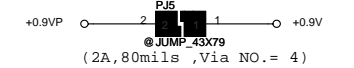
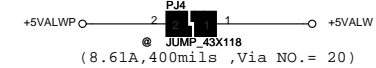
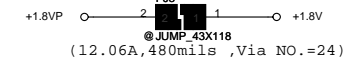
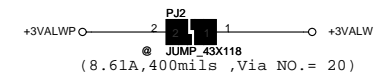


SP093MX0000



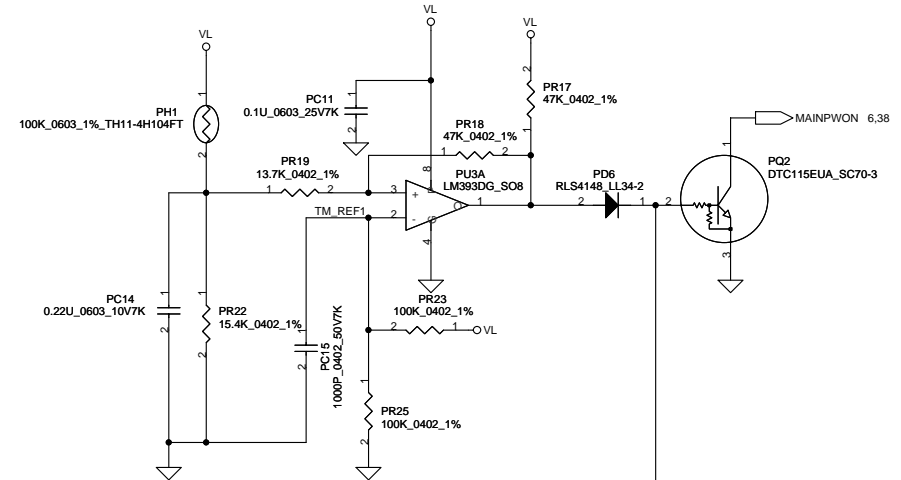
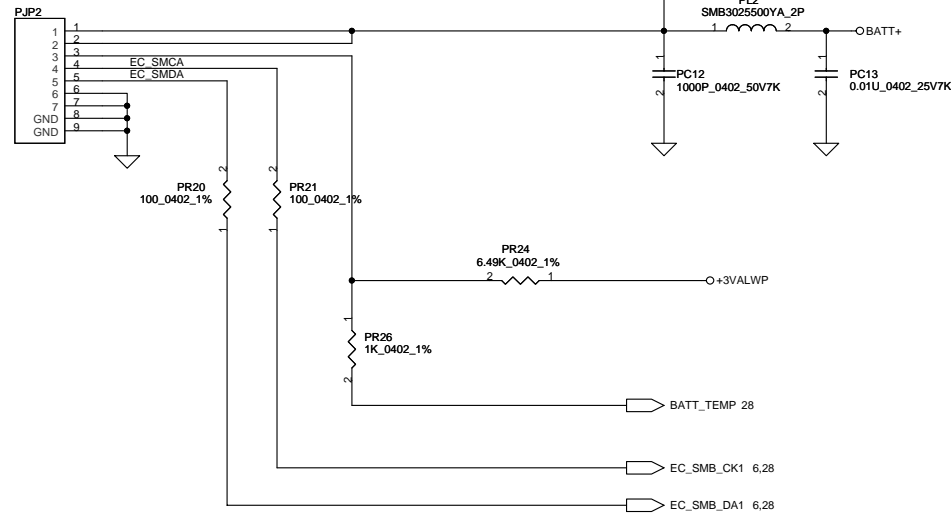
Vin Detector

	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

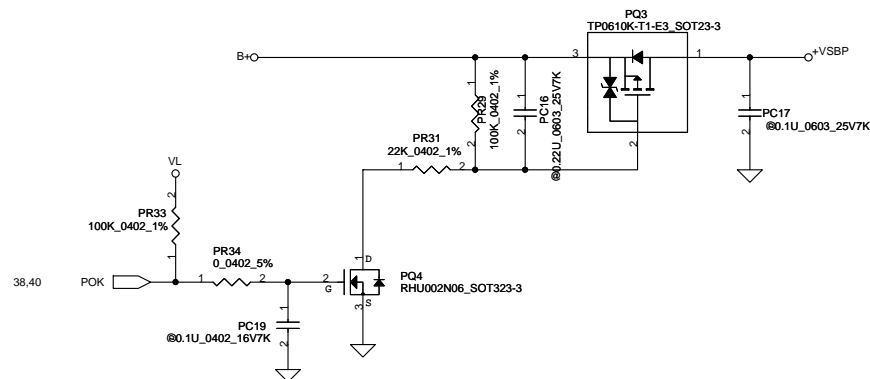
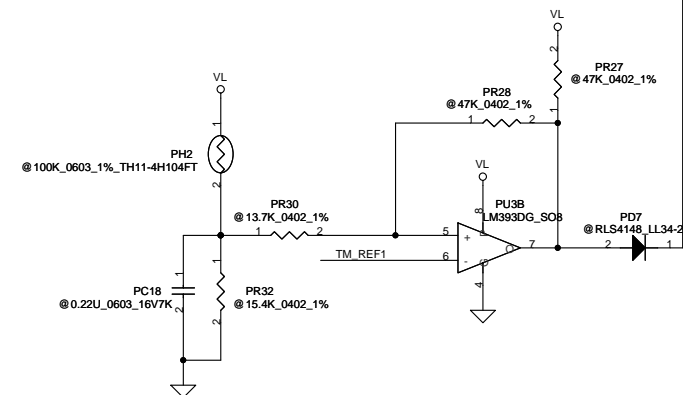


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					401575
					Rev D
					Date: Tuesday, August 19, 2008
					Sheet 36 of 45

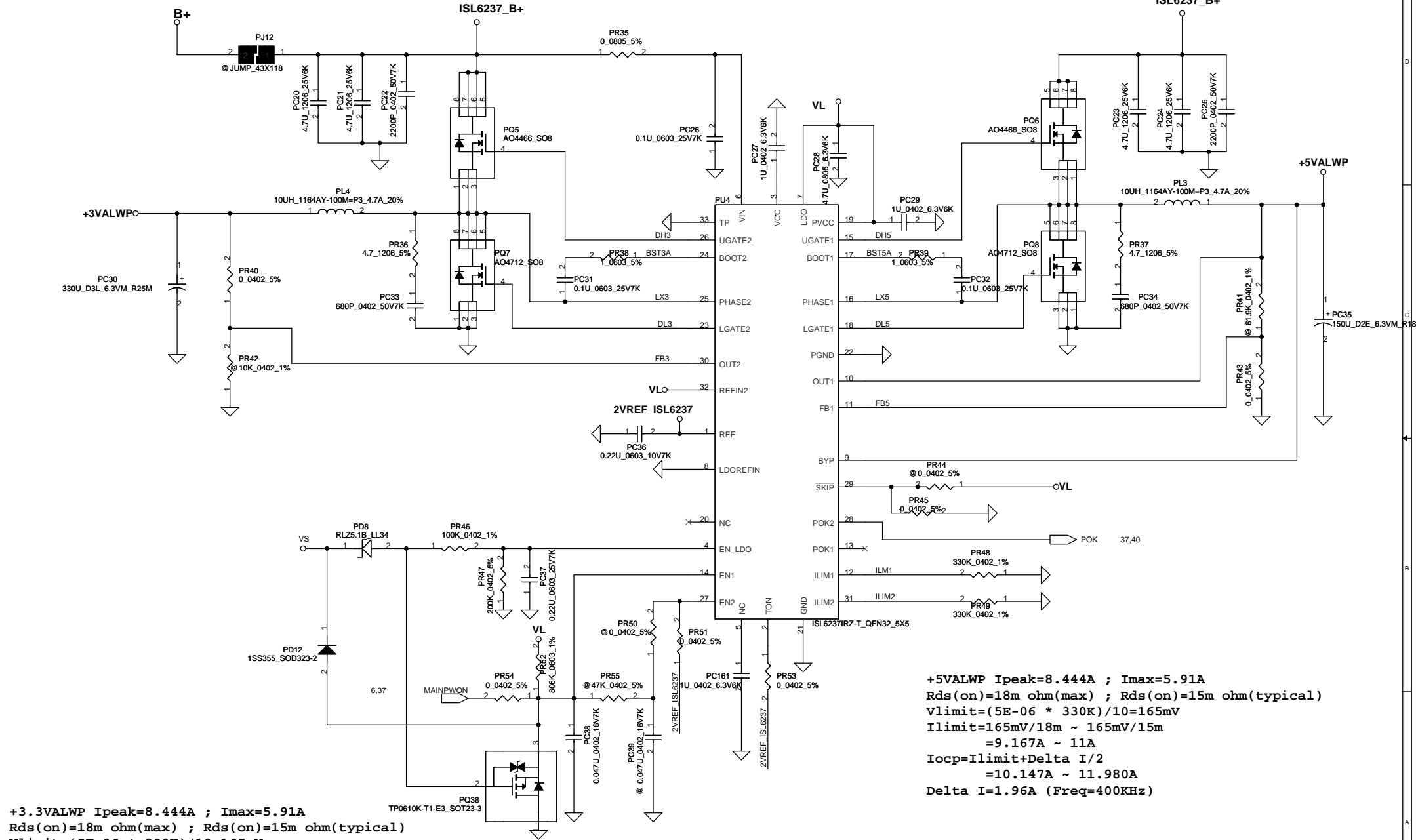
Recovery at 56 degree C



Recovery at 56 degree C



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					401575	
				Date:	Tuesday, August 19, 2008	Sheet 37 of 45



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				Date	Tuesday, August 19, 2008
				Sheet	38 of 45

1.1V Ipeak=8.9A ; Imax=6.23A
DCR=6m ohm (max)
Rocset=(Iocp*DCR)/10E-06=7.87K ohm
Iocp=10.089A(1.3*DCR)
Csen=L/(Rocset*DCR)=0.022uF

Freq=303KHz
Rfset=1/(1.5E-10 * Freq)=22K

1.2V Ipeak=3.94A ; Imax=2.758A
DCR=10m ohm (max)
Rocset=(Iocp*DCR)/10E-06=8.06K ohm
Iocp=6.716A(1.2*DCR)
Csen=L/(Rocset*DCR)=0.022uF

Freq=366KHz
Rfset=1/(1.5E-10 * Freq)=18.2K

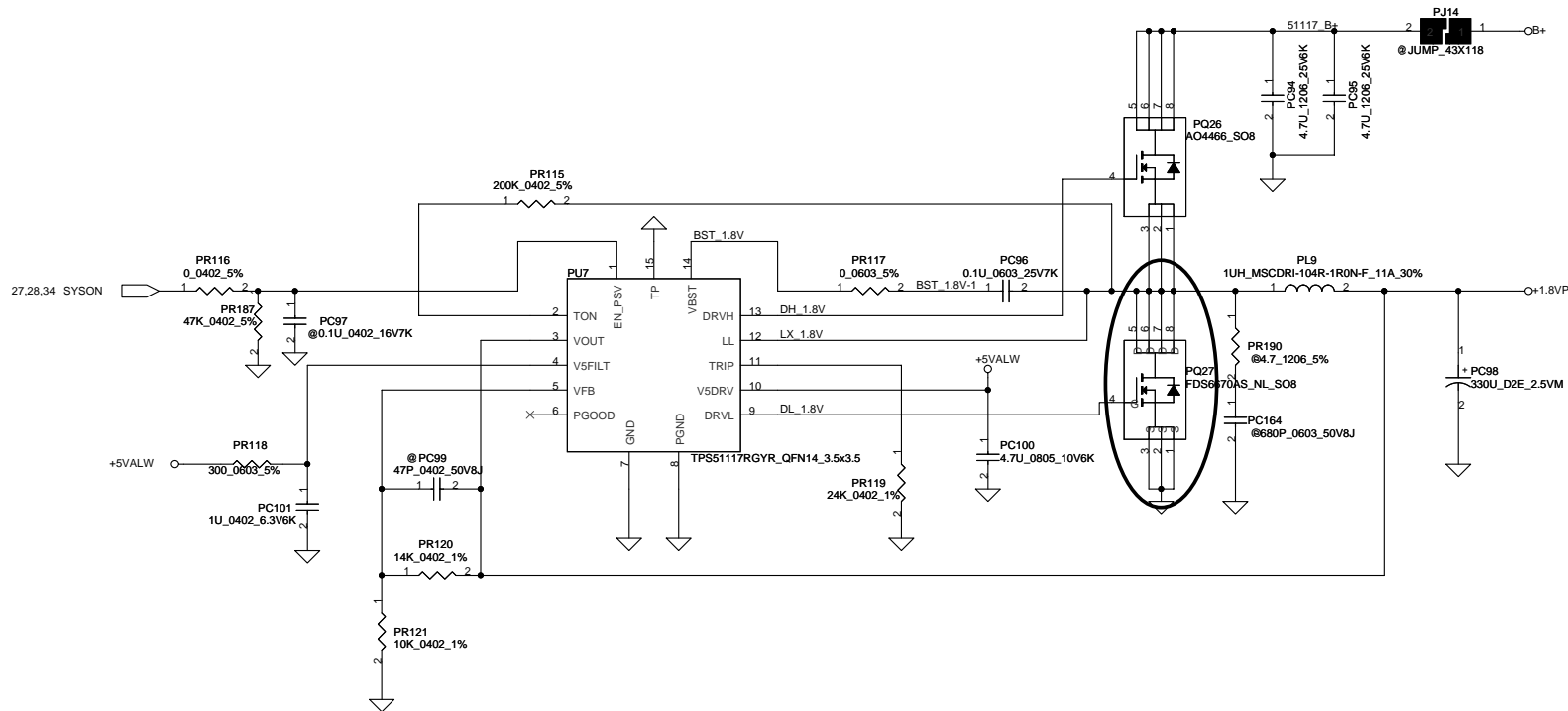
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1.2VP Ipeak=3.94A ; Imax=2.758A
DCR=10m ohm (max)
Rocset=(Iocp*DCR)/10E-06=8.06K ohm
Iocp=6.716A(1.2*DCR)
Csen=L/(Rocset*DCR)=0.022uF

Freq=366KHz
Rfset=1/(1.5E-10 * Freq)=18.2K

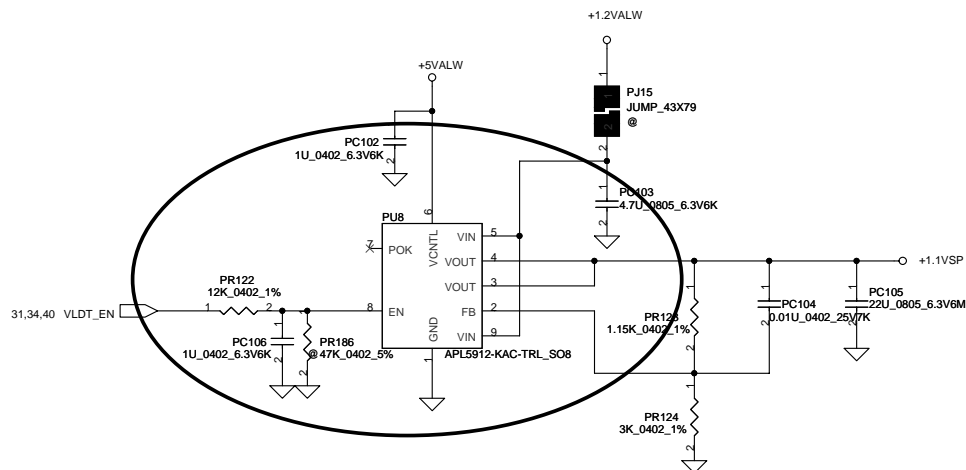
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					401575	
Date:				Tuesday, August 19, 2008	Sheet	40 of 45

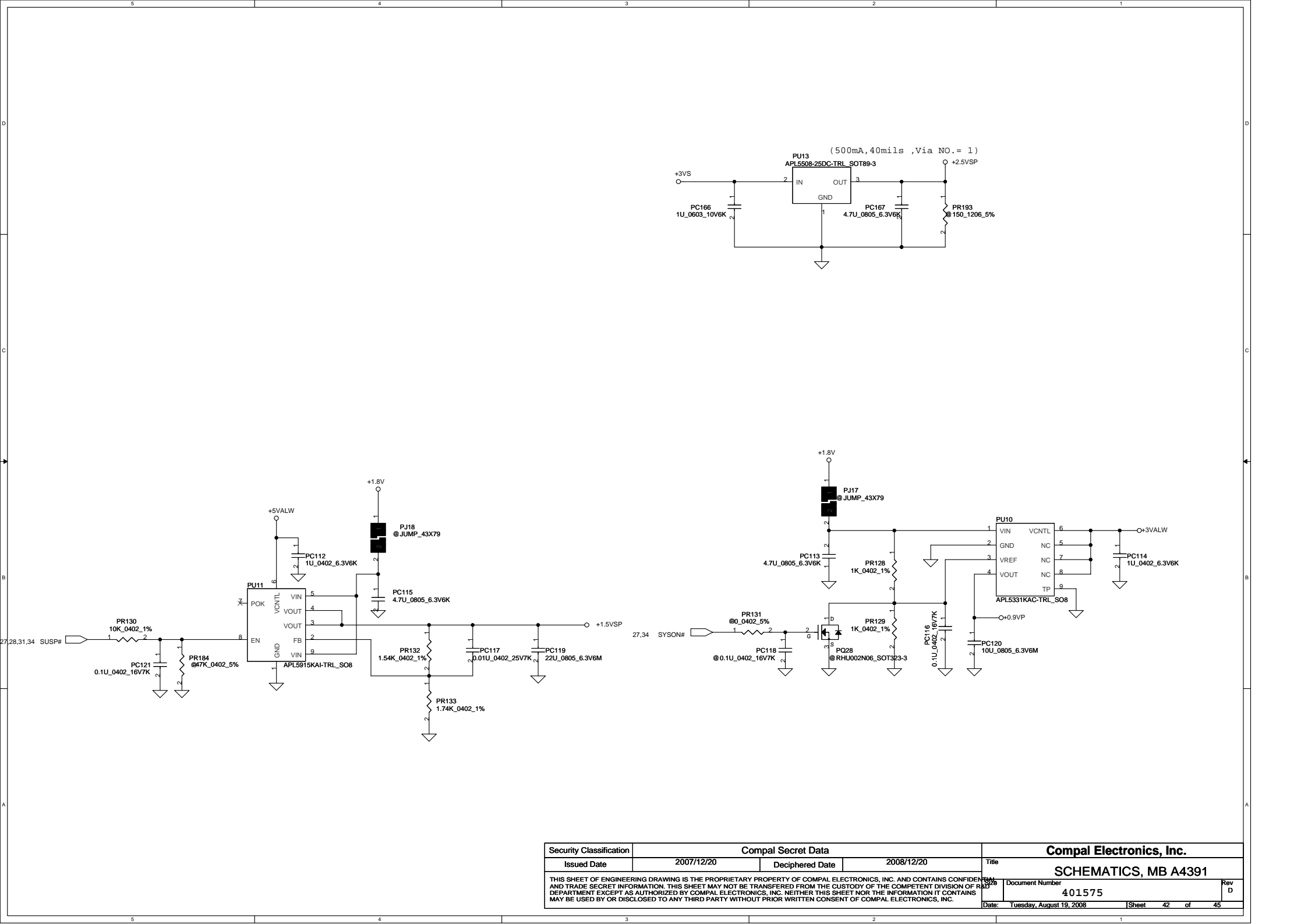


$V_{FB}=0.75V$
 $V_o=V_{FB} \cdot (1 + \frac{PR120}{PR121}) = 1.8V$
 $T_{on}=19E-12 \cdot R_{on} \cdot ((\frac{2}{3}) \cdot \frac{V_o+100mV}{V_{in}}) + 50ns = 3.1E-07$
 $Freq=305KHz$

$C_{esr}=15m \text{ ohm}$
 $I_{peak}=12.6A$ $I_{max}=8.82A$
 $\Delta I = ((19-1.8) \cdot (1.8/19)) / (L \cdot Freq) = 5.332A$
 $V_{trip}=R_{trip} \cdot I_{0uA} = 0.24V$
 $I_{ocp-min}=V_{trip}/R_{ds(on)max} \cdot 1.4 + 2.666 = 17.573A$
 $I_{ocp-max}=V_{trip}/R_{ds(on)typ} \cdot 1.2 + 2.666 = 26.908A$
 $I_{ocp}=17.573 \sim 26.908A$



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				Rev D
				401575
				Date: Tuesday, August 19, 2008
				Sheet 41 of 45



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Date: Tuesday, August 19, 2008				Sheet	42 of 45

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Add NB_CORE B+ circuit	NB_CORE B+ 加強	0.1	40	Add PL14 SM010016410 (S SUPPRE_ KC FBMA-L11-322513-151LMA50T)	20080506	PVT
2	Modify the circuit for Vin dectector	BOM modify	0.1	36	Cahnge PR122 SD028100280(S RES 1/16W 10K +-5% 0402) to PR126 SD028100280(S RES 1/16W 10K +-5% 0402)	20080506	PVT
3	1.1V circuit change	For debug	0.1	41	Add PU8 SA000015410 (S I C APL5912-KAC-TRL SO 8P LDO)	20080506	PVT
4	1.1V circuit change	For debug	0.1	41	Add PC102 SE000000K80(S CER CAP 1U 6.3V K X5R 0402)	20080506	PVT
5	1.1V circuit change	For debug	0.1	41	Add PC103 SE093475K80 (S CER CAP 4.7U 6.3V K X5R 0805 H1.25)	20080506	PVT
6	1.1V circuit change	For debug	0.1	41	Add PC104 SE075103K80 (S CER CAP .01U 25V K X7R 0402)	20080506	PVT
7	1.1V circuit change	For debug	0.1	41	Add PC105 SE000000I10 (S CER CAP 22UF 6.3V M X5R 0805 H1.25)	20080506	PVT
8	1.1V circuit change	For debug	0.1	41	Add PC106 SE000000K80 (S CER CAP 1U 6.3V K X5R 0402)	20080506	PVT
9	1.1V circuit change	For debug	0.1	41	Add PR122 SD034120280 (S RES 1/16W 12K +-1% 0402)	20080506	PVT
10	1.1V circuit change	For debug	0.1	41	Add PR123 SD034115180 (S RES 1/16W 1.15K +-1% 0402)	20080506	PVT
11	1.1V circuit change	For debug	0.1	41	Add PR124 SD034300180 (S RES 1/16W 3K +-1% 0402)	20080506	PVT
12	NB_CORE low side MOS change	BOM modify	0.1	40	Cahnge PQ24 SB00000AJ00(S TR AO4712 1N SO8) to SB000004T80(S TR FDS6670AS_NL 1N SO8)	20080506	PVT
13	1.8V low side MOS change	BOM modify	0.1	41	Cahnge PQ27 SB00000AJ00(S TR AO4712 1N SO8) to SB000004T80(S TR FDS6670AS_NL 1N SO8)	20080506	PVT
14	1.1V circuit change	BOM modify	0.1	41	Cahnge PL8 SH000009180 (S COIL 1UH +-30% MSCDRI -104RD-1R0N 11A) to SH000009180 (S COIL 1UH +-30% MSCDRI -104RD-1R0N 11A)	20080506	PVT
15	1.2V circuit change	For 0 degree not boot issue	0.1	40	Add PR185 SD013100180 (S RES 1/10W 1K +-5% 0603)	20080512	PVT
16							
17							
18							
19							
20							
21							
22							
23							
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							401575
							Rev D
							Date: Tuesday, August 19, 2008
							Sheet 44 of 45

NO	DATE	PAGE	MODIFICATION LIST	NO	DATE	PAGE	MODIFICATION LIST
3/15		P.06	Modify CPU DTS function Add R562,R565 Pop R344,R348,C410,Q32,Q33 Un-pop R560,R561,R563,R564 Change R345,R346 to 2.2K_0402	5/6			Update PW circuit
						P.06	Un-pop R344,R348,C410,Q32,Q33,R562,R565,R335 Remove R560,R563
		P.11	Change R55 to 140_0402_1% Un-pop Q2,R86,Q49,R411 Pop R85,R553			P.14	Change U15 clockgen to Silego ()
						P.24	Un-pop U39,C670 Change R532 to L79 (SM010005480)
		P.12	Change C95,C139,C129,C44 to 22u_0805 Pop L1,L2			P.35	Add R569, C678
						P.28	Change U16 to version:D1 (SA00001J550)
		P.16	Change R66 to 140_0402_1%			P.06	Add R570
		P.19	Change R550 to 4.7K_0402			P.22	Change JSATA1 footprint
		P.21	Change R87 to 2.2K_0402	5/6		P.12	Change L3 to R571, 0_0805
		P.26	Add R566	5/12			Update PW circuit
		P.32	Change R459,R460,R457,R458 to 1K_0402_1%			P.09	Add C679, C680
		P.34	Change R242 to 10K_0402	5/13		P.14	Add D39 for ESD
3/18		P.28	Pop R559			P.35	Add C681,C682,C683,C684,C685,C686 for EMI
		P.12	Change C15,C16,C17,C18 to 22u_0805			P.35	H4 become NPTH
		P.18	Pop R558			P.09	Udate PW circuit Add C687
3/19			Upgrade PW circuit	5/13		P.33	JHP1,JLINE1,JMIC1-->pin7,8 connect to AGND for ESD
		P.07	Change C195,C167 to 0402 package				
3/21		P.14	Change U15 to SA000023H10	6/02		P.22	Reserve C688,C689
		P.11	Change C29 to 22u_0805				Update PW circuit
3/24		P.18	Change BT USB from port6 to port9.	6/10		P.23	Add C690 for EMI
		P.15	Add R567,R568,C677 Remove C357			P.24	Change C653~C656 to 100p for EMI
3/25		P.27	Pop L29,L30 Un-pop R139,R136,R143,R146			P.35	Change C681 to 330p for EMI Pop C683 for EMI
		P.24	Change R542 to Bead (SM010005480)			P.19	Change R550 to 10K
3/26			Update some notice			P.12	Un-pop L1,L2
						P.28	Change U16 to version C0 (SA00001J540) Pop R226 Change R512 to 18K
						P.29	Del U19 Pop U18 (128K--SA00002C100)
				7/1		P.19	Pop SB SPI ROM (R547,C675,R549,R548,R550,U40)
						P.24	Change L79 to 0_0805_5% Resistance
						P.31	Un-pop SW9