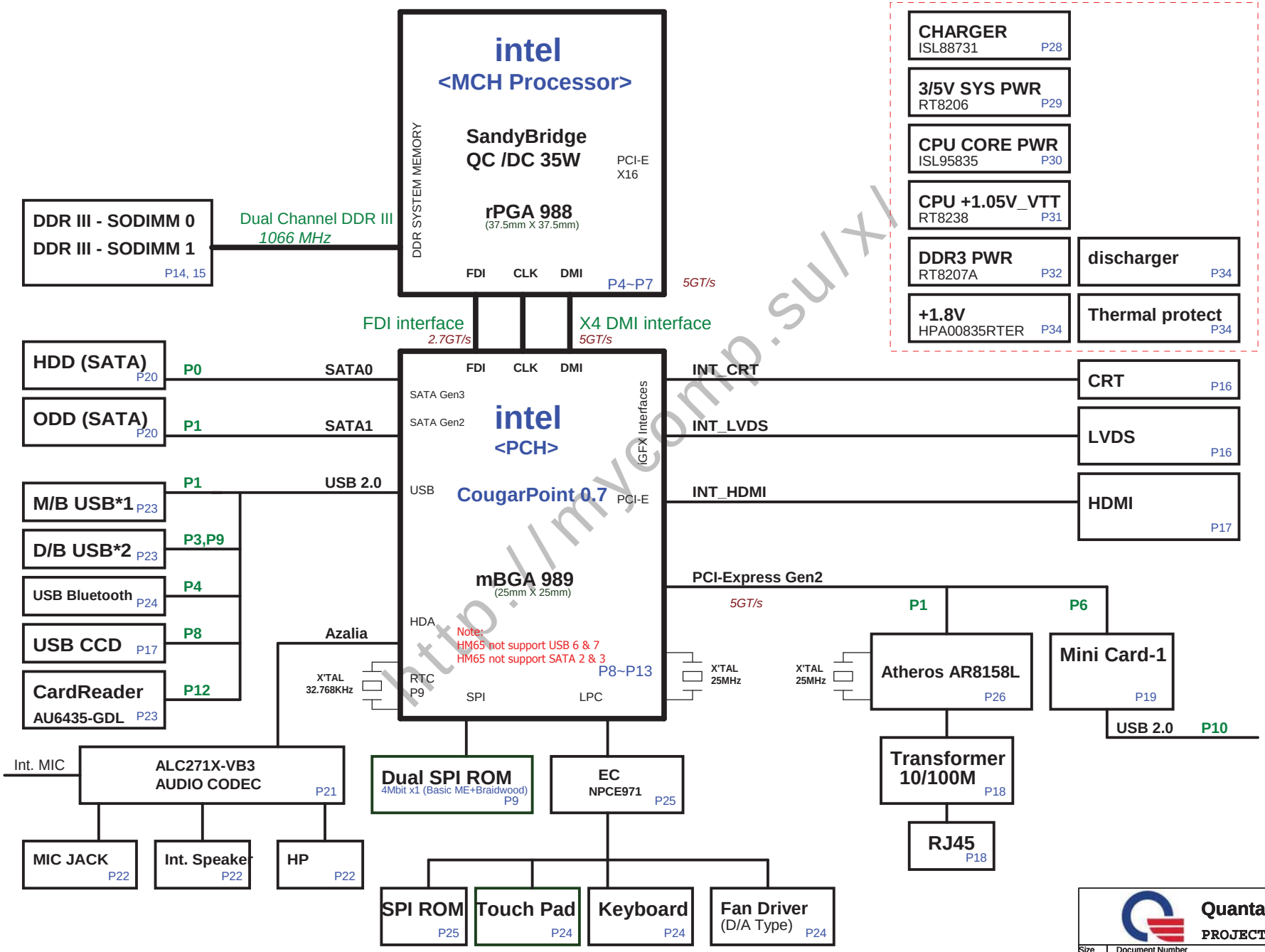
ZQR BLOCK DIAGRAM



Quanta Computer Inc.
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	Block Diagram	1A
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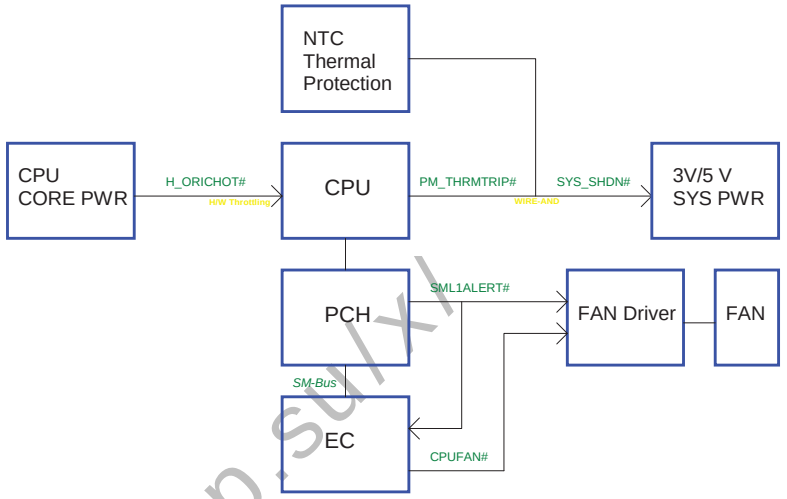
Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

Thermal Follow Chart



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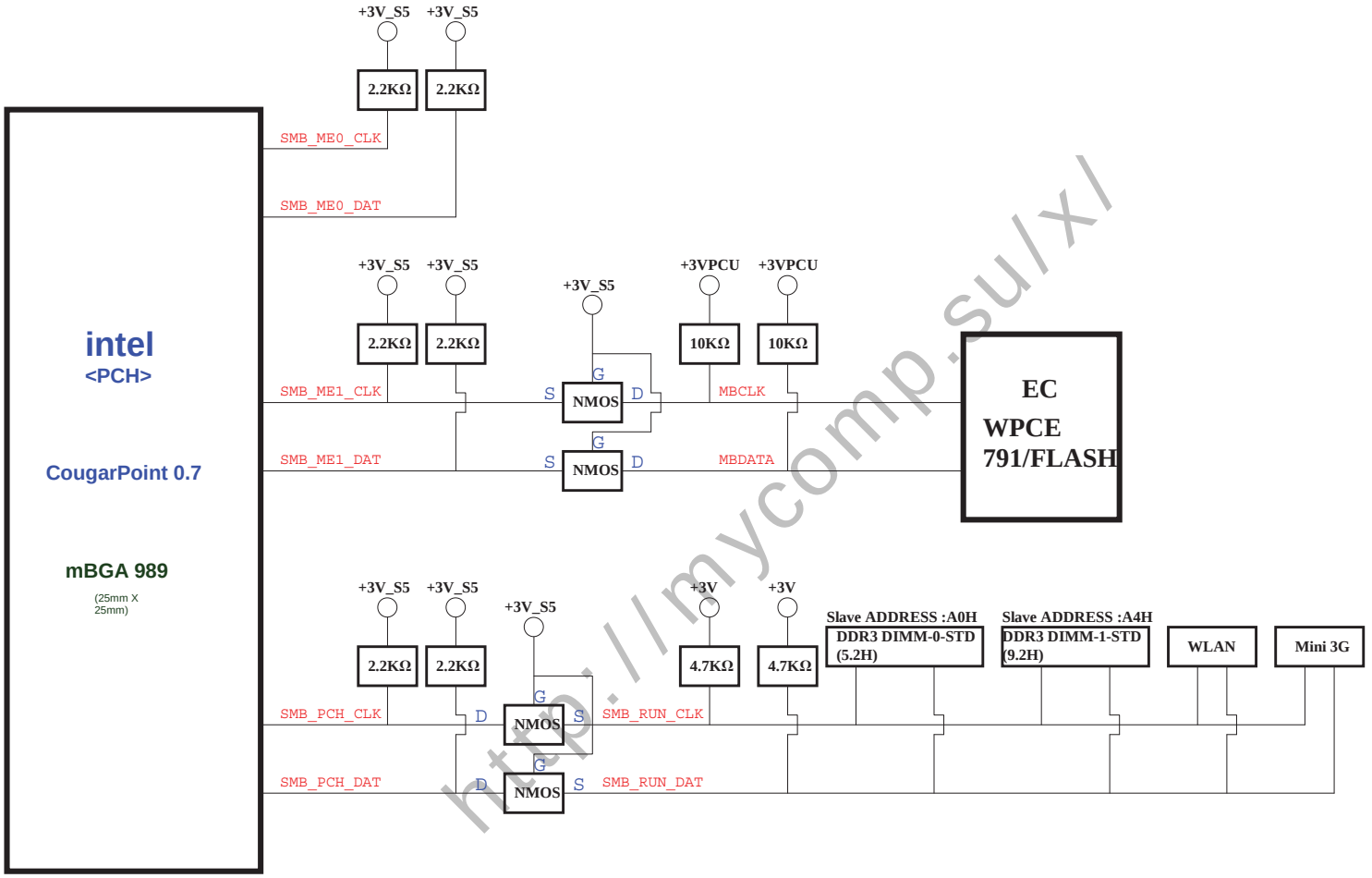

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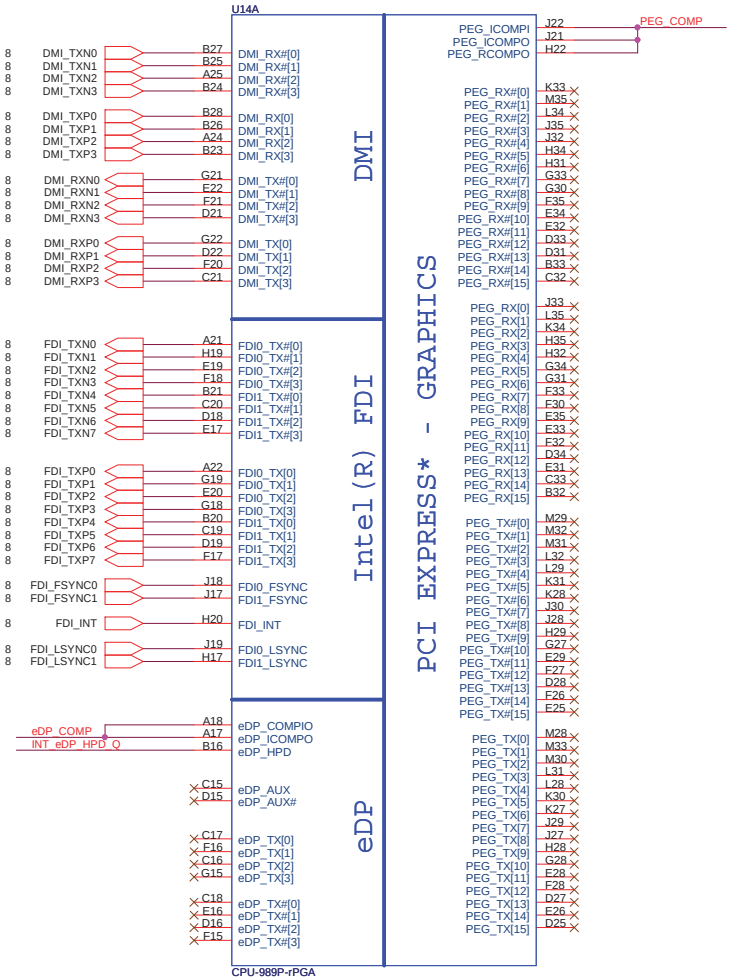
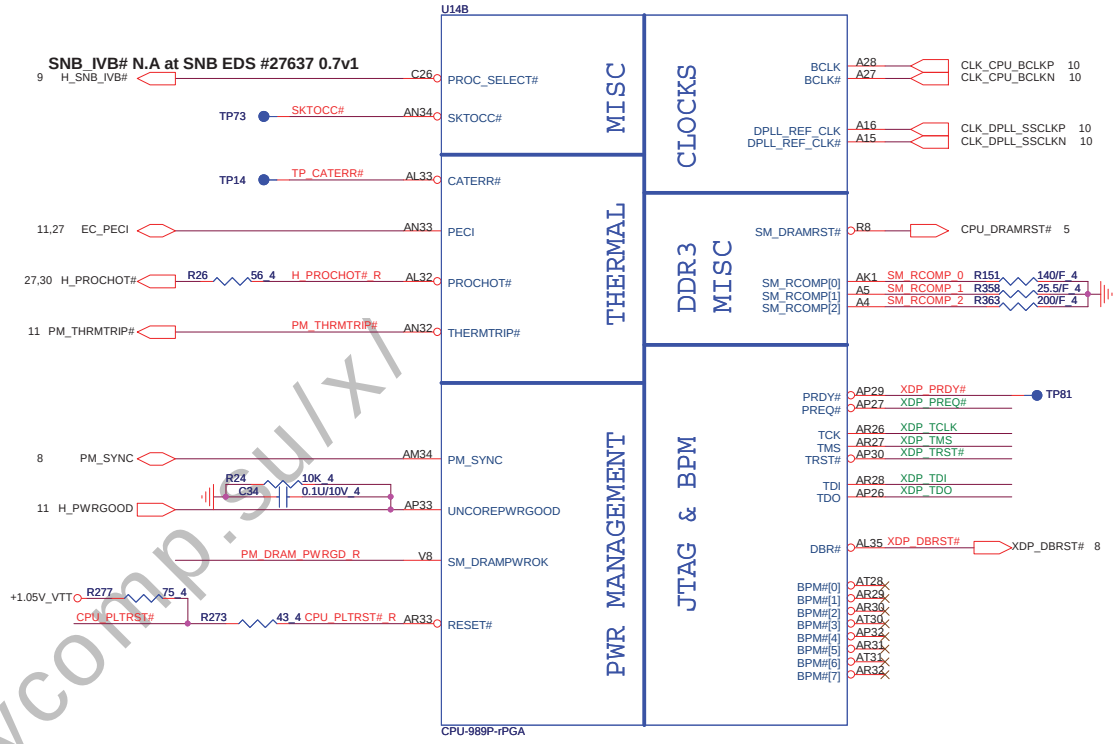
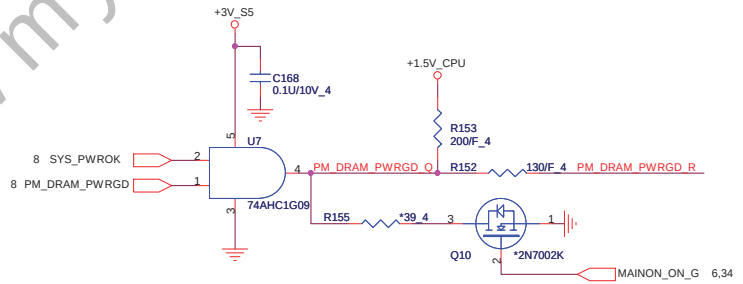
Sandy Bridge Processor (DMI,PEG,FDI)

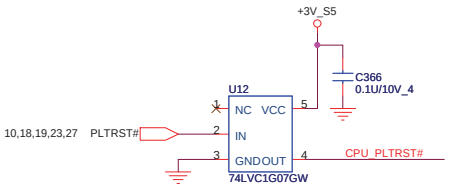
Sandy Bridge Processor (CLK,MISC,JTAG)

04

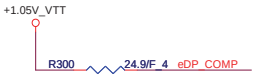




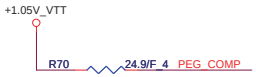




DP & PEG Compensation



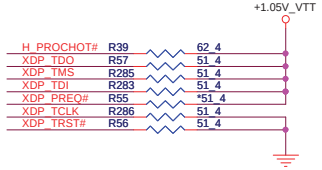
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

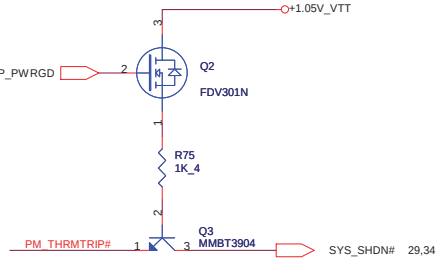


PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms

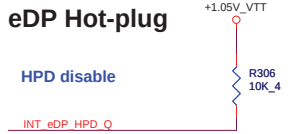
PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

Processor pull-up(CPU)





eDP Hot-plug



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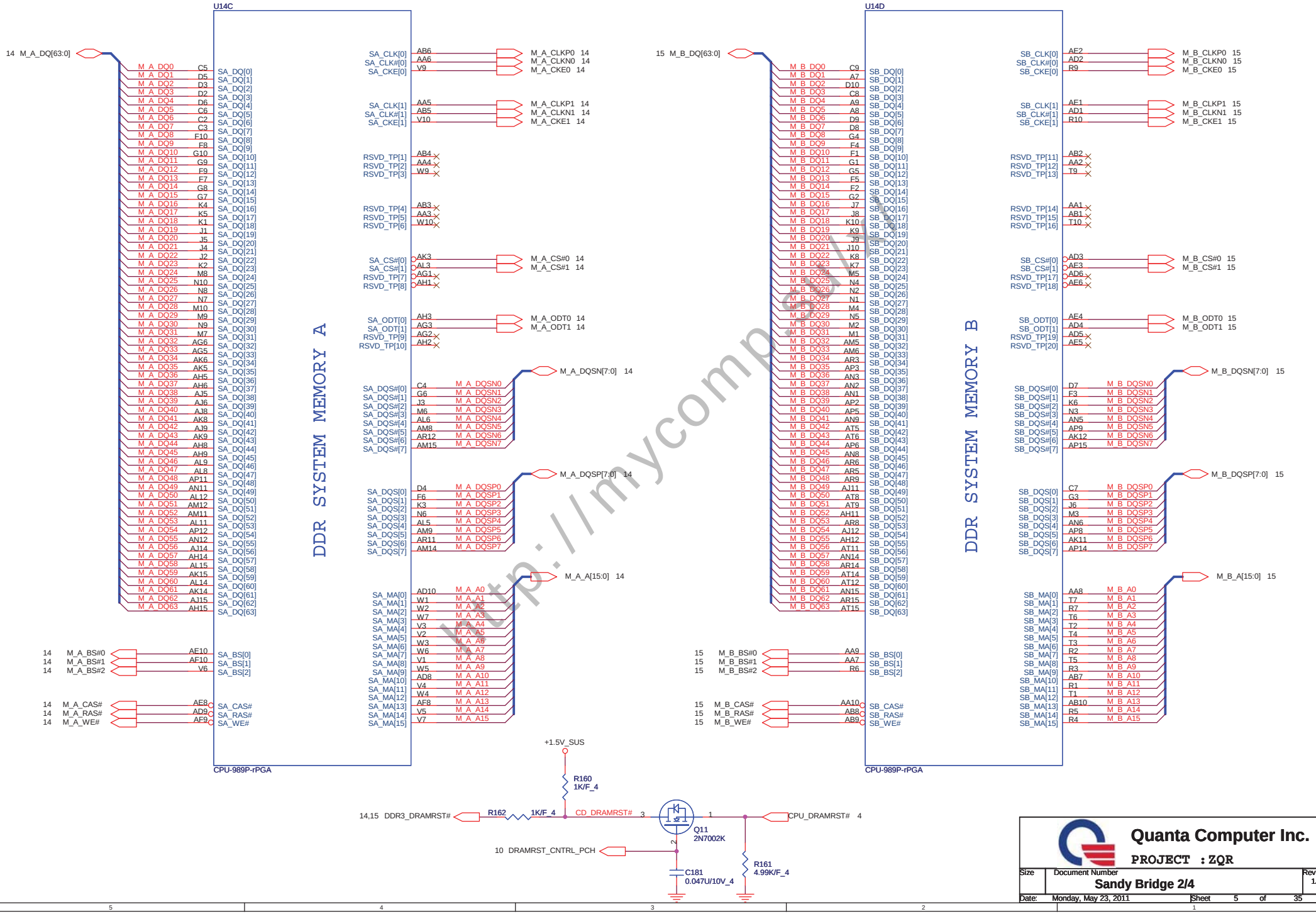
Sandy Bridge Processor (DDR3)



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Sandy Bridge Processor (POWER) CPU VTT

Sandy Bridge Processor (GRAPHIC POWER)

06

CPU Core Power
SNB 45W:52A

Spec
470uF/4mohm x 4
22uF x 16
10uF x 10

CPU VTT
SNB 45W:8.5A

Spec
330uF/6mohm x 2
22uF x 12
22uF x 7 (Non-stuff)

CPU VGT
SNB 45W:21.5A

Spec
470uF/4mohm x 2
22uF x 12

CPU VCCPL
SNB 45W:1.5A

Spec
330uF/7mohm x 1
10uF x 1
1uF x 2

CPU MCH
SNB 45W: 5A

Spec
330uF/6mohm x 1
10uF x 6

Real
10uF x 6

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

CPU SA
SNB 45W: 6A

Spec
330uF/7mohm x 1
10uF x 3

U14F — POWER — CPU-989P-rPGA
- CORE SUPPLY
- PEG AND DDR
- SVID
- SENSE LINES

U14G — POWER — CPU-989P-rPGA
- GRAPHICS
- SENSE LINES
- VREF
- DDR3 -1.5V RAILS
- SA RAIL
- 1.8V RAIL
- MISC

B23 Mount C70, C71 for +Vcc_core overshoot issue. 5/18

B45 Remove C315 for cost issue. 5/19

B54 Del C442. 5/20

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK

Place PU resistor close to CPU

SVID DATA

Place PU resistor close to CPU

SVID ALERT

4.5A

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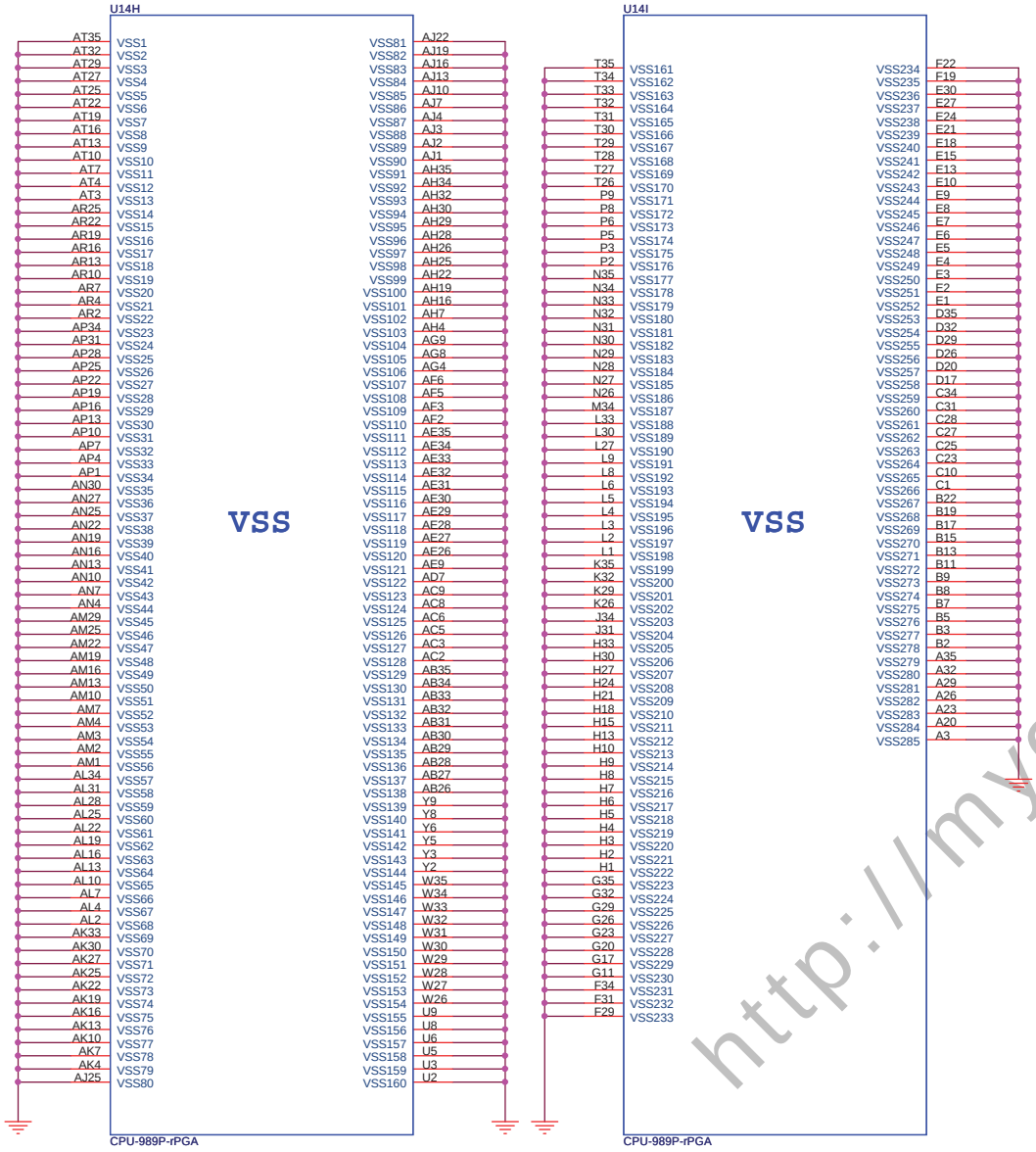
Sandy Bridge Processor (GND)



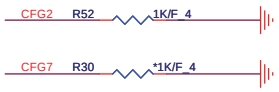
Sandy Bridge Processor (RESERVED, CFG)

07

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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Cougar Point (DMI,FDI,PM)

U13C

DMI_RXN0 BC24 DMI0RXN
DMI_RXN1 BE20 DMI1RXN
DMI_RXN2 BG18 DMI2RXN
DMI_RXN3 BG20 DMI3RXN
DMI_RXP0 BE24 DMI0RXP
DMI_RXP1 BC20 DMI1RXP
DMI_RXP2 BJ18 DMI2RXP
DMI_RXP3 BJ20 DMI3RXP
DMI_TXN0 AW24 DMI0TXN
DMI_TXN1 AW20 DMI1TXN
DMI_TXN2 BB18 DMI2TXN
DMI_TXN3 AV18 DMI3TXN
DMI_TXP0 AY24 DMI0TXP
DMI_TXP1 AY20 DMI1TXP
DMI_TXP2 AY18 DMI2TXP
DMI_TXP3 AU18 DMI3TXP

DMI

BJ24 DMI_ZCOMP
+1.05V_VTT R302 49.9/F_4 DMI_COMP BG25 DMI_IRCOMP
R307 750/F_4 DMI2RBIAS BH21 DMI2RBIAS

FDI_RXN0 BJ14 FDI_TXN0 4
FDI_RXN1 AY14 FDI_TXN1 4
FDI_RXN2 BE14 FDI_TXN2 4
FDI_RXN3 BH13 FDI_TXN3 4
FDI_RXN4 BC12 FDI_TXN4 4
FDI_RXN5 BJ12 FDI_TXN5 4
FDI_RXN6 BG10 FDI_TXN6 4
FDI_RXN7 BG9 FDI_TXN7 4
FDI_RXP0 BG14 FDI_TXP0 4
FDI_RXP1 BB14 FDI_TXP1 4
FDI_RXP2 BF14 FDI_TXP2 4
FDI_RXP3 BG13 FDI_TXP3 4
FDI_RXP4 BE12 FDI_TXP4 4
FDI_RXP5 BG12 FDI_TXP5 4
FDI_RXP6 BJ10 FDI_TXP6 4
FDI_RXP7 BH9 FDI_TXP7 4

FDI

FDI_INT AW16 FDI_INT 4
FDI_FSYNC0 AV12 FDI_FSYNC0 4
FDI_FSYNC1 BC10 FDI_FSYNC1 4
FDI_LSYNC0 AV14 FDI_LSYNC0 4
FDI_LSYNC1 BB10 FDI_LSYNC1 4

System Power Management

DSWVRMEN A18 DSWVREN
SUS_PWR_ACK C12 SUSACK#
DPWROK E22 ICH_RSMRST#
4 XDP_DBRST# XDP_DBRST# K3 SYS_RESET# WAKE# B9 PCIE_WAKE# PCIE_WAKE# 18,19
SYS_PWROK P12 SYS_PWROK CLKRUN# / GPIO32 N3 CLKRUN# CLKRUN# 27
27 PWROK_EC PWROK_EC L22 PWROK +3V_S5 SUS_STAT# / GPIO61 G8 SUS_STAT# TP43
L10 APWROK +3V_S5 SUSCLK / GPIO62 N14 PCH_SUSCLK 27
4 PM_DRAM_PWRGD PM_DRAM_PWRGD B13 DRAMPWROK +3V_S5 SLP_S5# / GPIO63 D10 TP34
27 ICH_RSMRST# ICH_RSMRST# C21 RSMRST# SLP_S4# H4 SUSC# 27
SUS_PWR_ACK K16 SUSWARN#/SUSPWRDNACK/GPIO30 +3V_S5 SLP_S3# F4 SUSB# 27
27 DNBSWON# E20 PWRBTN# SLP_A# G10 TP38
AC_PRESENT H20 ACPRESENT / GPIO31 DSW SLP_SUS# G16 TP33
PM_BATLOW# E10 BATLOW# / GPIO72 +3V_S5 PMSYNCH AP14 PM_SYNC 4
PM_RI# A10 RI# +3V_S5 SLP_LAN# / GPIO29 K14 SLP_LAN#

CougarPoint_R1P0

+3V
R10 2.2K_4 INT_LVDS_EDIDCLK
R12 2.2K_4 INT_LVDS_EDIDDATA

Cougar Point (LVDS,DDI)

U13D

16 INT_LVDS_BLON J47 L_BKLTEN
16 INT_LVDS_DIGON M45 L_VDD_EN
16 INT_LVDS_BRIGHT P45 L_BKLTCTL
16 INT_LVDS_EDIDCLK INT_LVDS_EDIDCLK T40 L_DDC_CLK
16 INT_LVDS_EDIDDATA INT_LVDS_EDIDDATA K47 L_DDC_DATA
+3V R33 2.2K_4 T45 L_CTRL_CLK
R32 2.2K_4 P39 L_CTRL_DATA
R51 2.37K/F_4 AE37 LVD_IBG
TP20 AF36 LVD_VBG
AE48 LVD_VREFH
AE47 LVD_VREFL

LVDS

16 INT_TXLCLKOUTN INT_TXLCLKOUTN AK39 LVDSA_CLK#
16 INT_TXLCLKOUTP INT_TXLCLKOUTP AK40 LVDSA_CLK
16 INT_TXLOUTN0 INT_TXLOUTN0 AN48 LVDSA_DATA#0
16 INT_TXLOUTN1 INT_TXLOUTN1 AM47 LVDSA_DATA#1
16 INT_TXLOUTN2 INT_TXLOUTN2 AK47 LVDSA_DATA#2
AJ48 LVDSA_DATA#3
16 INT_TXLOUTP0 INT_TXLOUTP0 AN47 LVDSA_DATA0
16 INT_TXLOUTP1 INT_TXLOUTP1 AM49 LVDSA_DATA1
16 INT_TXLOUTP2 INT_TXLOUTP2 AK49 LVDSA_DATA2
AJ47 LVDSA_DATA3

R place close to PCH
R259 150/F_4 INT_CRT_BLU
R258 150/F_4 INT_CRT_GRE
R257 150/F_4 INT_CRT_RED

AF40 LVDSB_CLK#
AF39 LVDSB_CLK
AH45 LVDSB_DATA#0
AH47 LVDSB_DATA#1
AF49 LVDSB_DATA#2
AF45 LVDSB_DATA#3
AH43 LVDSB_DATA0
AH49 LVDSB_DATA1
AF47 LVDSB_DATA2
AF43 LVDSB_DATA3

+3V
R34 2.7K_4 INT_CRT_DDCCLK
R35 2.7K_4 INT_CRT_DDCDAT

16 INT_CRT_BLU INT_CRT_BLU N48 CRT_BLUE
16 INT_CRT_GRE INT_CRT_GRE P49 CRT_GREEN
16 INT_CRT_RED INT_CRT_RED T49 CRT_RED
16 INT_CRT_DDCCLK INT_CRT_DDCCLK T39 CRT_DDC_CLK
16 INT_CRT_DDCDAT INT_CRT_DDCDAT M40 CRT_DDC_DATA

CRT

16 INT_CRT_HSYNC R261 33_4 INT_CRT_HSYNC_R M47 CRT_HSYNC
16 INT_CRT_VSYNC R260 33_4 INT_CRT_VSYNC_R M49 CRT_VSYNC
DAC_IREF T43 DAC_IREF
T42 CRT_IRTN
R53 1K/F_4

Digital Display Interface

SDVO_TVCLKINN AP43
SDVO_TVCLKINP AP45
SDVO_STALLN AM42
SDVO_STALLP AM40
SDVO_INTN AP39
SDVO_INTP AP40
SDVO_CTRLCLK P38 INT_HDMI_SCL 17
SDVO_CTRLDATA M39 INT_HDMI_SDA 17

INT. HDMI

DDPB_AUXN AT49
DDPB_AUXP AT47
DDPB_HPD AT40 INT_HDMI_HPD 17
DDPB_0N AV42 INT_HDMI_TXDN2 17
DDPB_0P AV40 INT_HDMI_TXDP2 17
DDPB_1N AV45 INT_HDMI_TXDN1 17
DDPB_1P AV46 INT_HDMI_TXDP1 17
DDPB_2N AU48 INT_HDMI_TXDN0 17
DDPB_2P AU47 INT_HDMI_TXDP0 17
DDPB_3N AV47 INT_HDMI_TXCN 17
DDPB_3P AV49 INT_HDMI_TXCP 17

DDPC_CTRLCLK P46
DDPC_CTRLDATA P42

INT. DP

DDPC_AUXN AP47
DDPC_AUXP AP49
DDPC_HPD AT38 DDPC_HPD_PU
DDPC_0N AY47
DDPC_0P AY49
DDPC_1N AY43
DDPC_1P AY45
DDPC_2N BA47
DDPC_2P BA49
DDPC_3N BB47
DDPC_3P BB49

DDPD_CTRLCLK M43
DDPD_CTRLDATA M36
DDPD_AUXN AT45
DDPD_AUXP AT43
DDPD_HPD BH41 DDPD_HPD_PU
DDPD_0N BB43
DDPD_0P BB45
DDPD_1N BF44
DDPD_1P BE44
DDPD_2N BF43
DDPD_2P BE42
DDPD_3N BJ42
DDPD_3P BG42

CougarPoint_R1P0

+3V
DDPC_HPD_PU R48 10K_4
DDPD_HPD_PU R287 10K_4

Follow PDG eDP disable guide

SYNC RS
33ohm for Direct Connect
20ohm for Dock Support
20ohm for Switchable Graphics Device Down Topology
10ohm for Switchable Graphics Dock Support

PCH Pull-high/low(CLG)

+3V
CLKRUN# R350 8.2K_4
XDP_DBRST# R353 10K_4
R337 *1K_4
ICH_RSMRST# R303 10K_4
SYS_PWROK R111 10K_4

+3V_S5
PM_RI# R326 10K_4
PM_BATLOW# R105 8.2K_4
PCIE_WAKE# R329 10K_4
SLP_LAN# R91 *10K_4
SUS_PWR_ACK R324 10K_4
AC_PRESENT R83 10K_4
PM_DRAM_PWRGD R319 200/F_4

System PWR_OK(CLG)

+3V_S5
C150 *0.1U/10V_4
U6 TC7SH08
4 SYS_PWROK SYS_PWROK 4
IMVP_PWRGD_R
PWROK_EC
R145 100K_4

R409 0_4
C142 *2.2U/6.3V_4
U5 *TC7SH08
IMVP_PWRGD 4,30
CFX_PWRGD 30

B05 Use R409 to exchange U5, C142 for saving cost 05/17

+3V_RTC
R309 330K_4
DSWVREN
R310 *330K_4

On Die DSW VR Enable
High = Enable (Default)
Low = Disable

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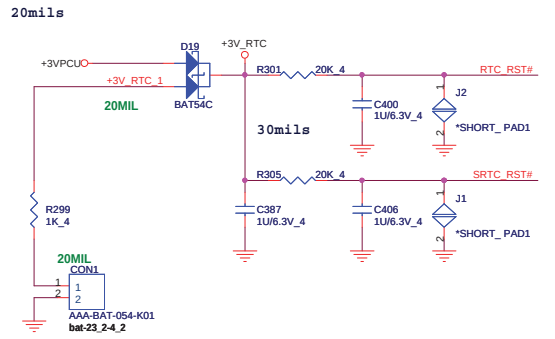
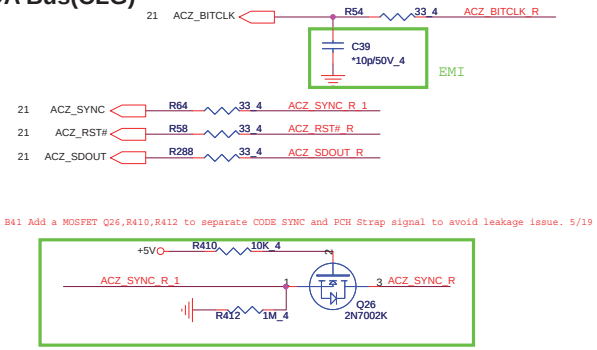
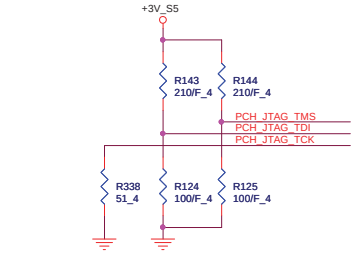
RTC Circuitry(RTC)



HDA Bus(CLG)

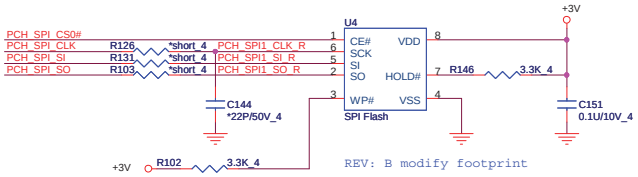


PCH JTAG Debug (CLG)



PCH Dual SPI (CLG)

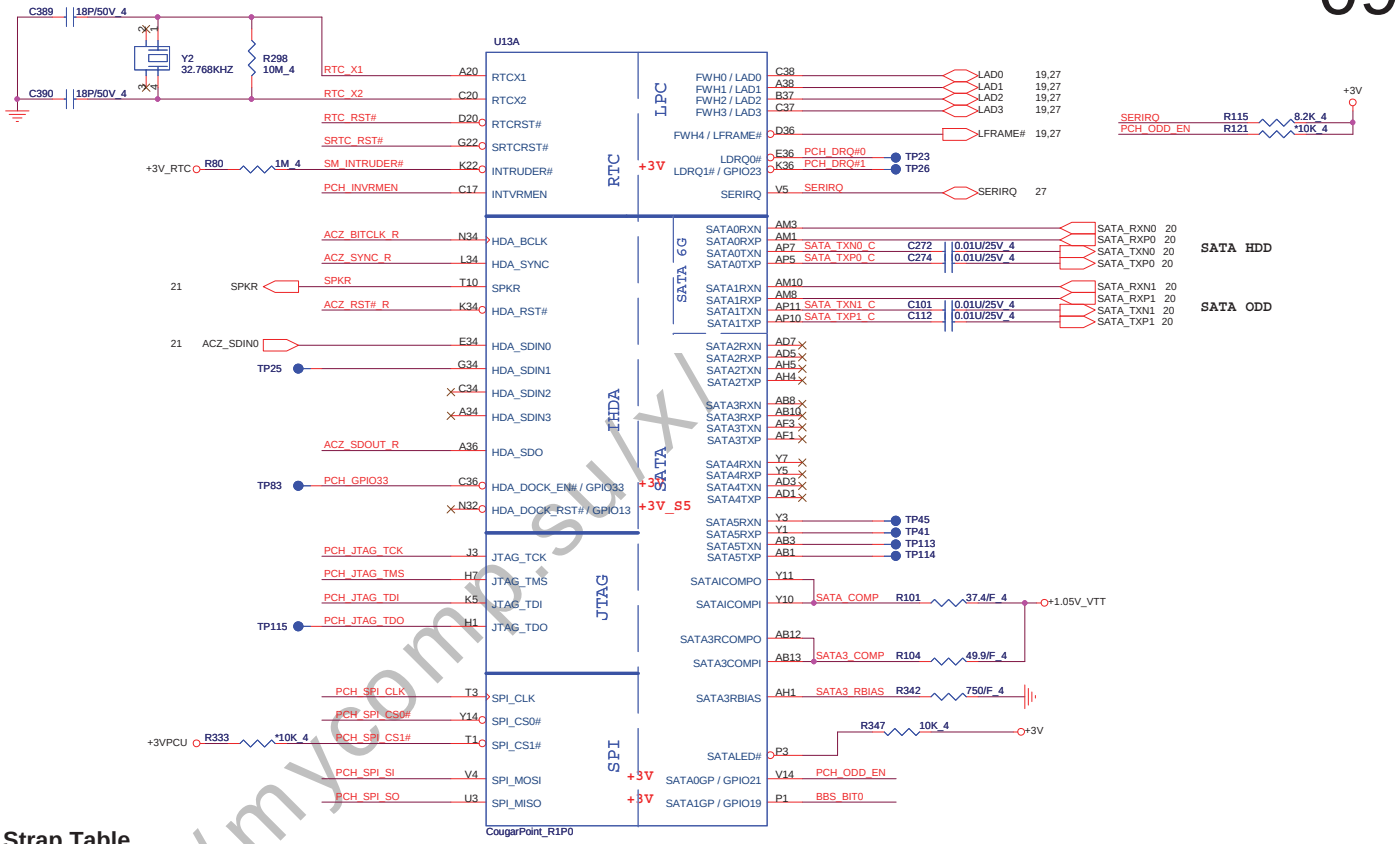
MX25L3205DM2I-12G: AKE39FP0Z00
W25X32VSSIG: AKE39ZP0N00



PCH2 (CLG)

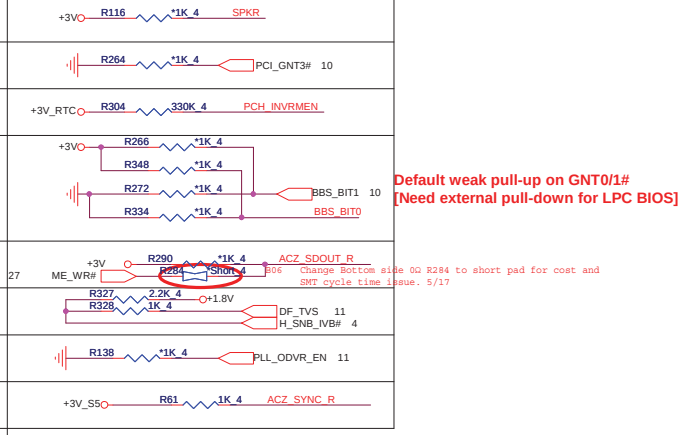
Cougar Point (HDA,JTAG,SATA)

09



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location 1 / 1 / SPI * 0 / 0 / LPC
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)



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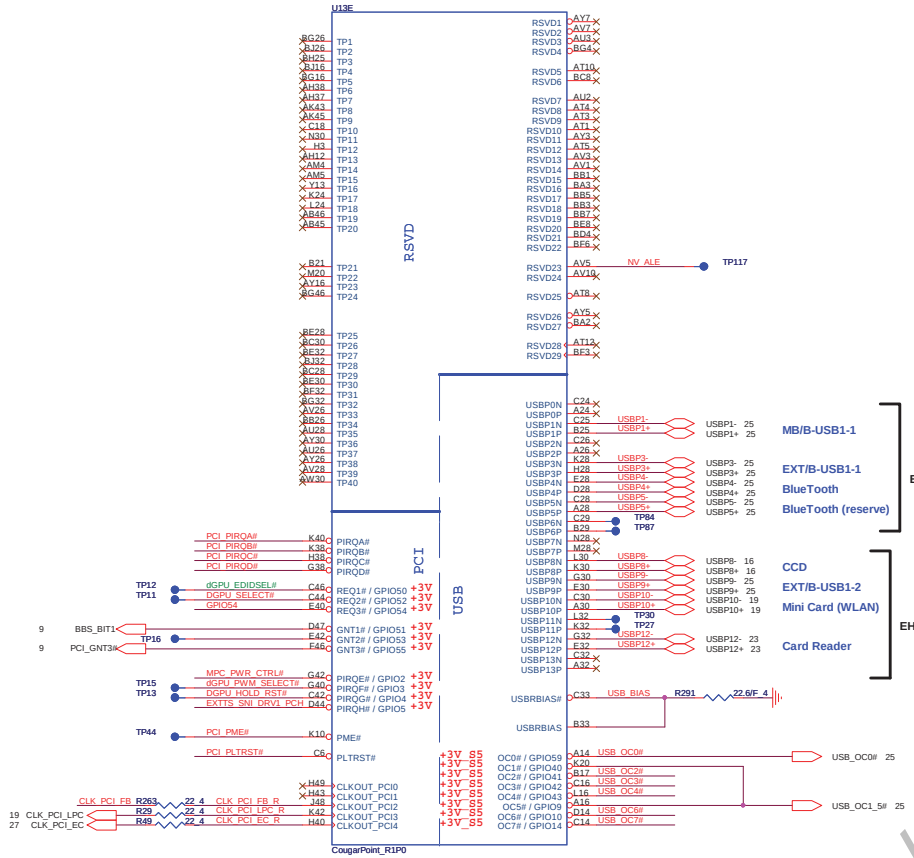
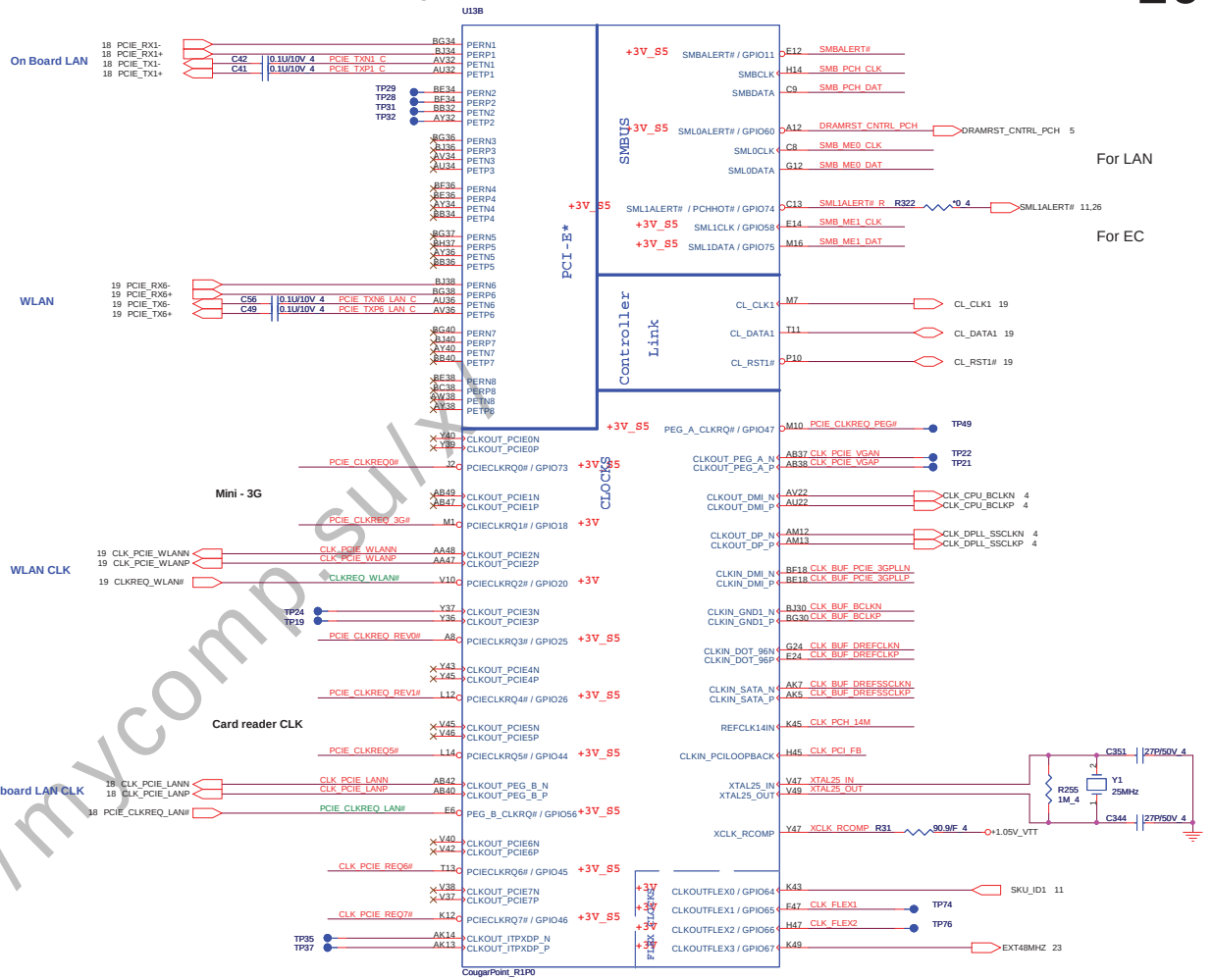
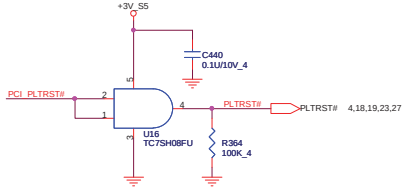
Cougar Point-M (PCI,USB,NVRAM)



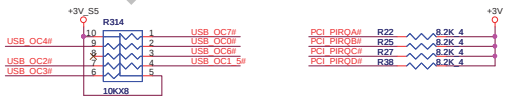
Cougar Point-M (PCI-E,SMBUS,CLK)

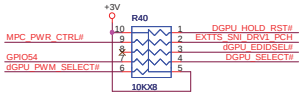


PLTRST#(CLG)



PCI/USBOC# Pull-up(CLG)

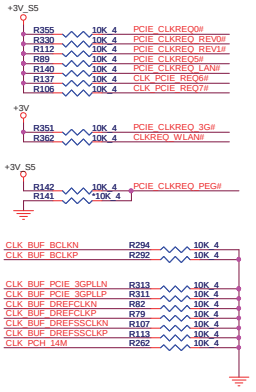




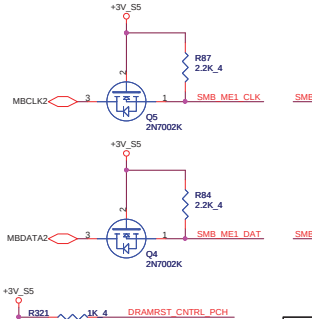
MPC Switch Control	
MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

MPC_PWR_CTRL# R50 *1K_4

CLK_REQ/Strap Pin(CLG)



SMBus/Pull-up(CLG)



SMBus(PCH)

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Cougar Point (GPIO,VSS_NCTF,RSVD)

U13F

GPIO

S_GPIO	T7	BMBUSY# / GPIO0	+3V	+3V	TACH4 / GPIO68	C40	DGPU_PRSNT#
27 EC_EXT_SMI#	EC_EXT_SMI#	A42	TACH1 / GPIO1	+3V	+3V	TACH5 / GPIO69	B41 R280 1.5K/F_4
	BOARD_ID1	H36	TACH2 / GPIO6	+3V	+3V	TACH6 / GPIO70	C41 R276 1.5K/F_4 +3V
27 EC_EXT_SCI#	EC_EXT_SCI#	E38	TACH3 / GPIO7	+3V	+3V	TACH7 / GPIO71	A40 R279 1.5K/F_4
TP111		C10	GPIO8	+3V_S5			
	SMIB#	C4	LAN_PHY_PWR_CTRL / GPIO12		+3V_S5		
	PCH_GPIO15	G2	GPIO15	+3V_S5			
check VR_ON GPIO	SKU_ID0	U2	SATA4GP / GPIO16	+3V			
TP10	dGPU_PWROK	D40	TACH0 / GPIO17	+3V			
	BIOS_REC	T5	SCLOCK / GPIO22	+3V			
	CR_WAKER#	E8	GPIO24 / MEM_LED	+3V_S5			
	GPIO27	E16	GPIO27	DSW			
9 PLL_ODVR_EN	PLL_ODVR_EN	P8	GPIO28	+3V_S5			
Need Check	STP_PCI#	K1	STP_PCI# / GPIO34	+3V			
TP40	dGPU_VRON	K4	GPIO35	+3V			
TP42	DMI_OVRVLTG	V8	SATA2GP / GPIO36	+3V			
	FDI_OVRVLTG	M5	SATA3GP / GPIO37	+3V			
	MFG_MODE	N2	SLOAD / GPIO38	+3V			
	BOARD_ID0	M3	SDATAOUT0 / GPIO39	+3V			
	TEST_SET_UP	V13	SDATAOUT1 / GPIO48	+3V			
10,26 SML1ALERT#	R148 *short_4 CRIT_TEMP_REP#	V3	SATA5GP / GPIO49	+3V			
	BOARD_ID2	D6	GPIO57	+3V_S5			

CPU/MISC

A20GATE	P4	EC_A20GATE	EC_A20GATE 27
PECI	AU16	R325 *0_4	EC_PECI 4,27
RCIN#	P5	EC_RCIN#	EC_RCIN# 27
PROCPWRGD	AY11	TP36	H_PWRGOOD 4
THRMTRIP#	AY10	PCH_THRMTRIP# R323 390_4	PM_THRMTRIP# 4
INIT3_3V#	T14		
DF_TVS	AY1		DF_TVS 9
TS_VSS1	AH8		
TS_VSS2	AK11		
TS_VSS3	AH10		
TS_VSS4	AK10		
NC_1	P37		

NCTF

VSS_NCTF_1	A4	VSS_NCTF_15	BG2
VSS_NCTF_2	A44	VSS_NCTF_16	BG48
VSS_NCTF_3	A45	VSS_NCTF_17	BH3
VSS_NCTF_4	A46	VSS_NCTF_18	BH47
VSS_NCTF_5	A5	VSS_NCTF_19	BJ4
VSS_NCTF_6	A6	VSS_NCTF_20	BJ44
VSS_NCTF_7	B3	VSS_NCTF_21	BJ45
VSS_NCTF_8	B47	VSS_NCTF_22	BJ46
VSS_NCTF_9	BD1	VSS_NCTF_23	BJ5
VSS_NCTF_10	BD49	VSS_NCTF_24	BJ6
VSS_NCTF_11	BE1	VSS_NCTF_25	C2
VSS_NCTF_12	BE49	VSS_NCTF_26	C48
VSS_NCTF_13	BF1	VSS_NCTF_27	D1
VSS_NCTF_14	BF49	VSS_NCTF_28	D49
		VSS_NCTF_29	E1
		VSS_NCTF_30	E49
		VSS_NCTF_31	F1
		VSS_NCTF_32	F49

CougarPoint_R1P0

R353??

GPIO27:
Un-multiplexed. Can be configured as wake input to allow wakes from Deep Sleep.
If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.

	DGPU_PRSNT# (GPIO68)	SKU_ID1 (GPIO64)	SKU_ID0 (GPIO16)	VGA H/W Signal	Setup Menu	
UMA Only	1	0	0	UMA	Hidden	UMA boot

SV_SET_UP

High = Strong (Default)

TEST_SET_UP R136 10K_4 R120 *0_4 +3V

SGPIO

S_GPIO R135 1K/F_4 R118 *100_4 +3V

PCH_GPIO15 R356 1K_4 +3V_S5

Intel ME Crypto Transport Layer Security (TLS) cipher suite

Low = Disable (Default)

High = Enable

MFG-TEST

MFG_MODE R349 10K_4 R335 *0_4 +3V

GPIO Pull-up/Pull-down(CLG)

+3V_S5

CR_WAKER#	R108	10K/F_4
SMIB#	R341	10K_4
PLL_ODVR_EN	R139	*10K_4

+3V

EC_EXT_SMI#	R278	10K_4
EC_EXT_SCI#	R41	10K_4
STP_PCI#	R354	*10K_4
EC_A20GATE	R119	10K_4
EC_RCIN#	R123	10K_4
CRIT_TEMP_REP#	R147	10K_4
dGPU_PWROK	R23	*10K_4
GPIO27	R86	*10K_4

+3V

R281 IV@10K_4 R282 *EV@100K_4 DGPU_PRSNT#

+3V

R37 *EV@10K_4 R36 IV@10K_4 SKU_ID1 10

+3V

R345 *10K_4 R332 IV@10K_4 SKU_ID0

+3V

R336 10K_4 BOARD_ID0 R352 *10K_4

R45 10K_4 BOARD_ID1 R46 *10K_4

+3V_S5

R339 100K_4 BOARD_ID2 R340 *10K_4

FDI_OVRVLTG R122 *10K/F_4 +3V

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

DMI_OVRVLTG R128 *200K/F_4 +3V

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

BIOS_REC R134 10K_4 R117 *0_4 +3V

BIOS RECOVERY	High = Disable (Default) Low = Enable

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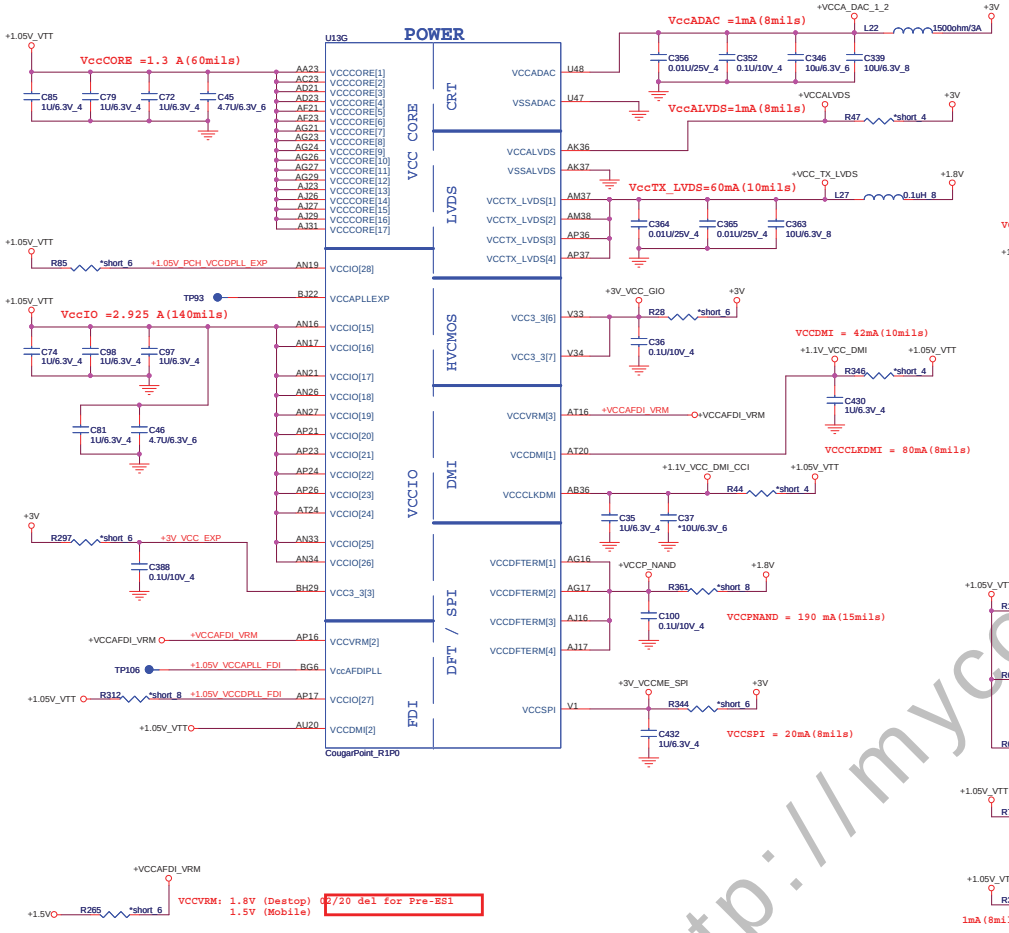
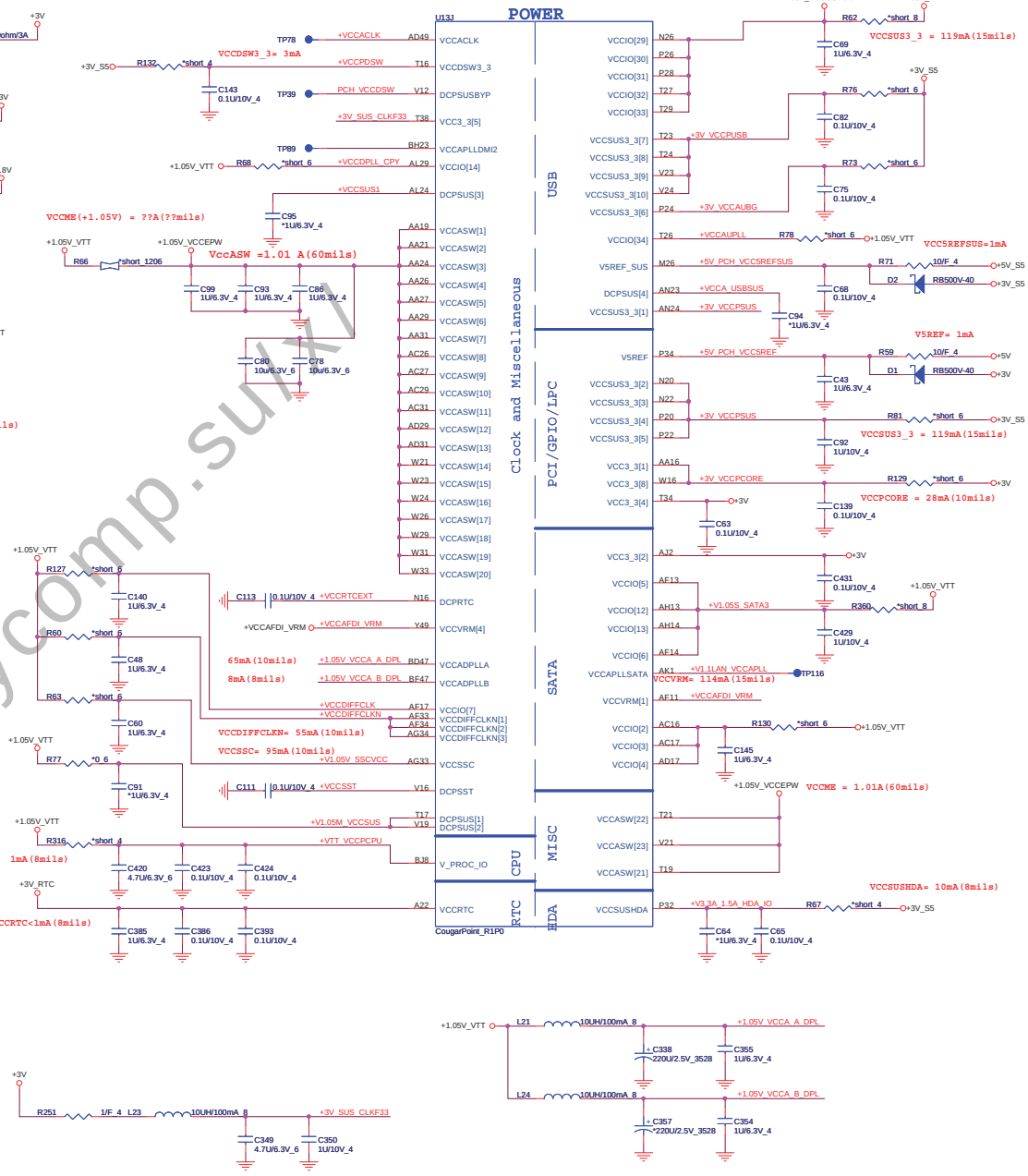
COUGAR POINT (POWER)



Cougar Point-M (POWER)



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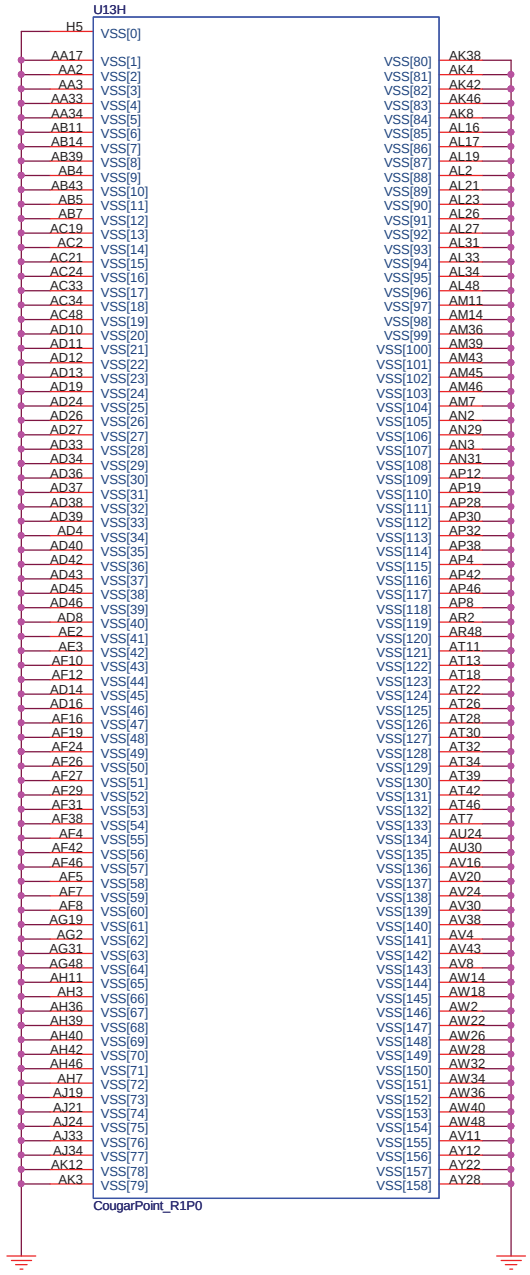
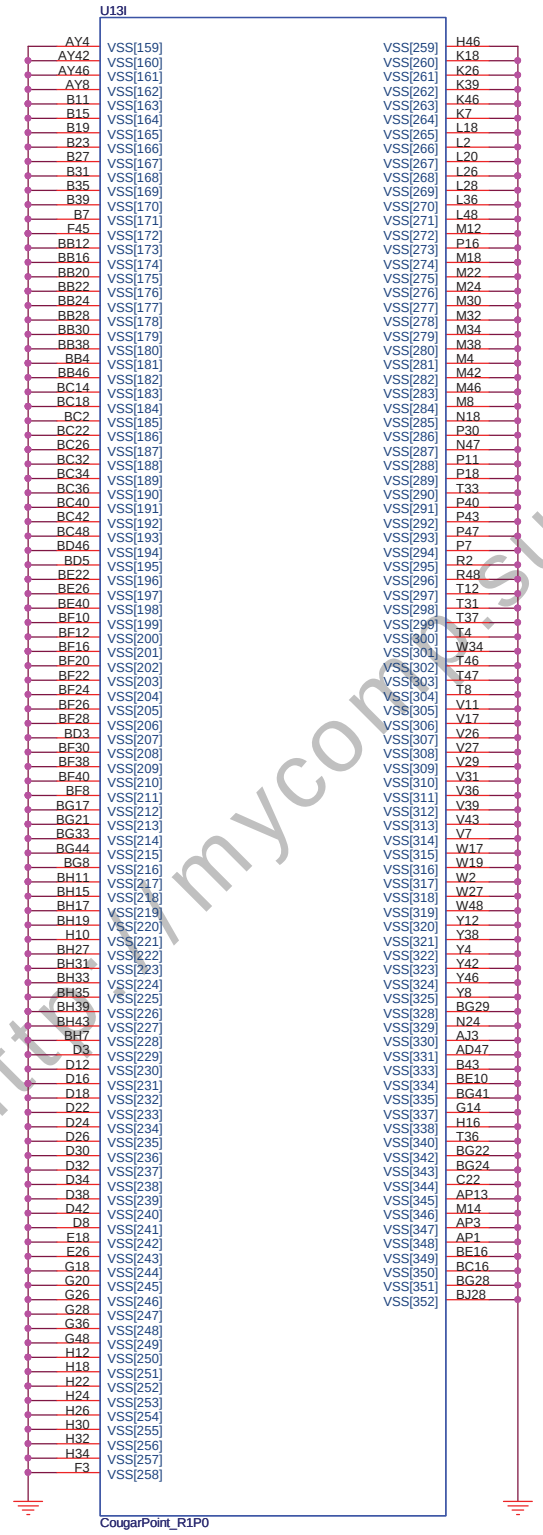
PCH6 (CLG)

13

IBEX PEAK-M (GND)





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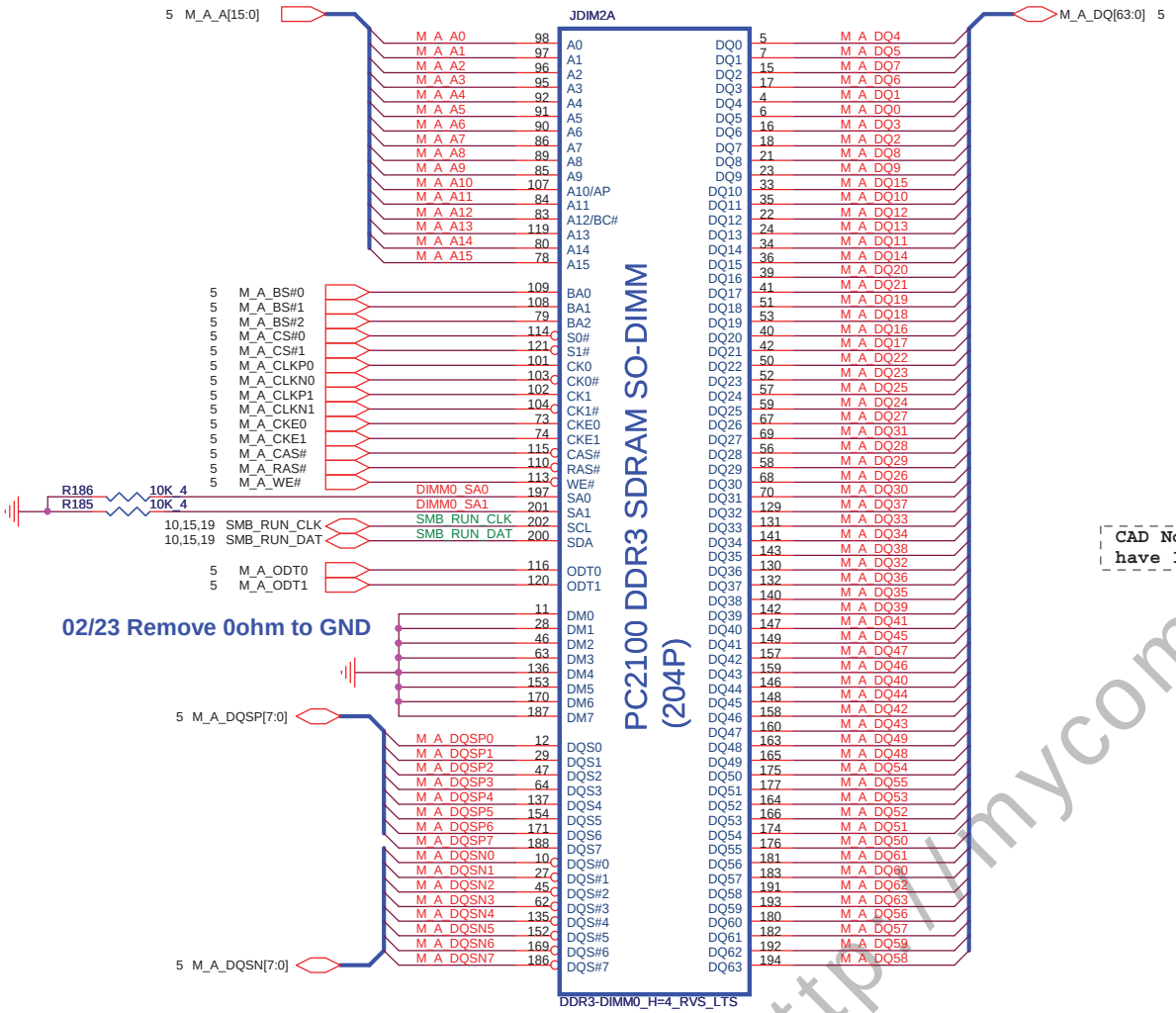
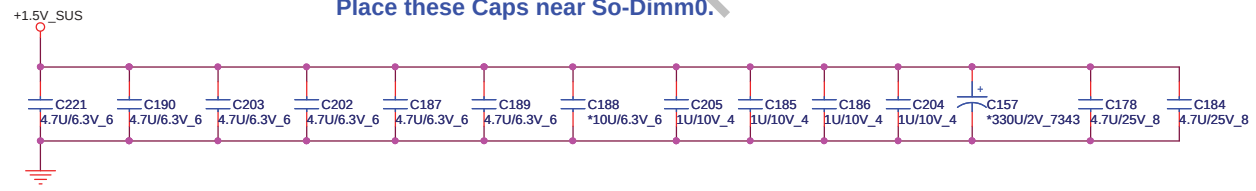
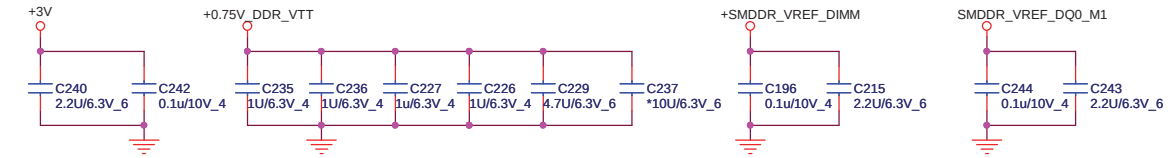
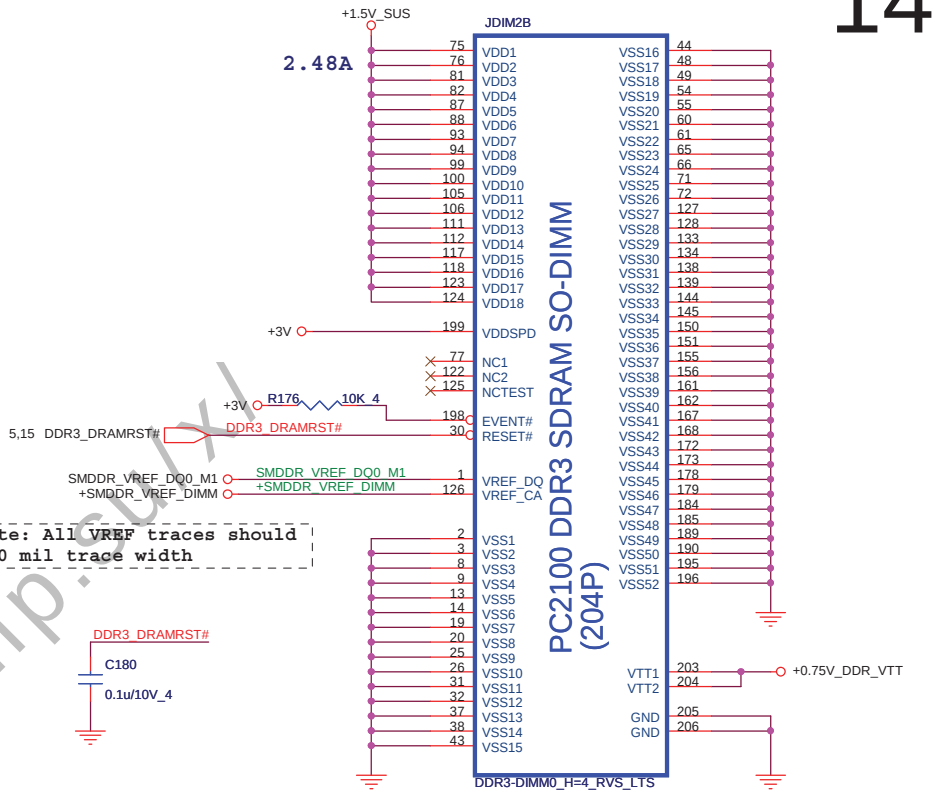
DDR RVS 4H

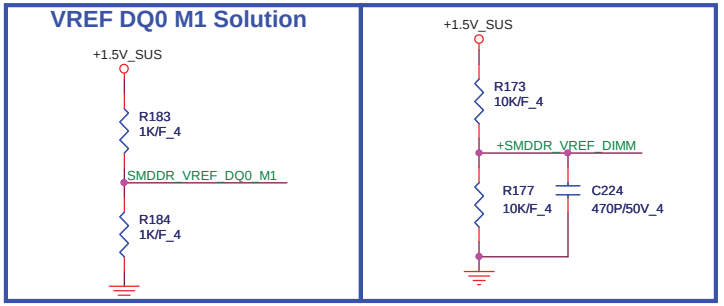


02/23 Remove 0ohm to GND









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	DDRIII SO-DIMM-0	1A

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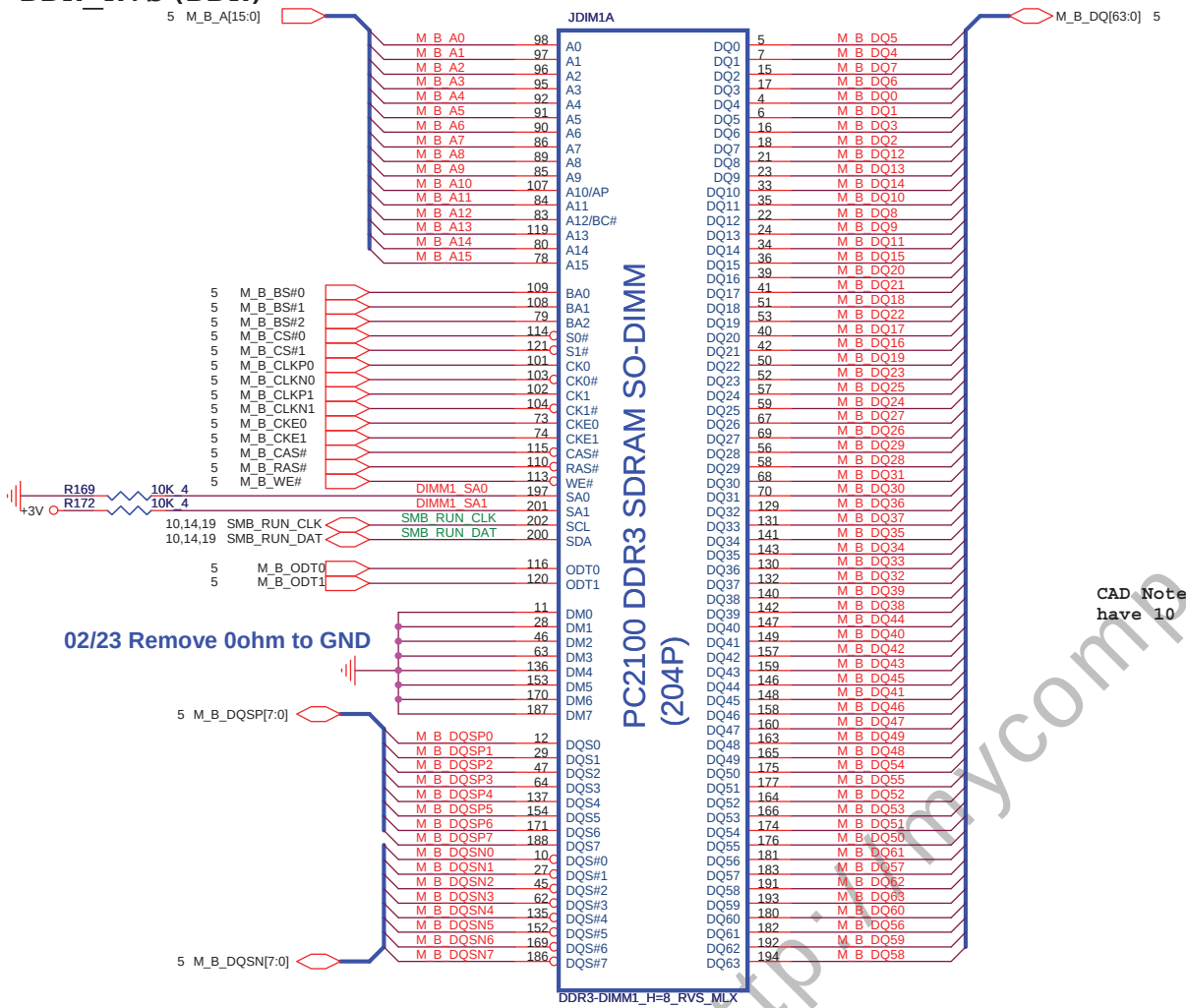
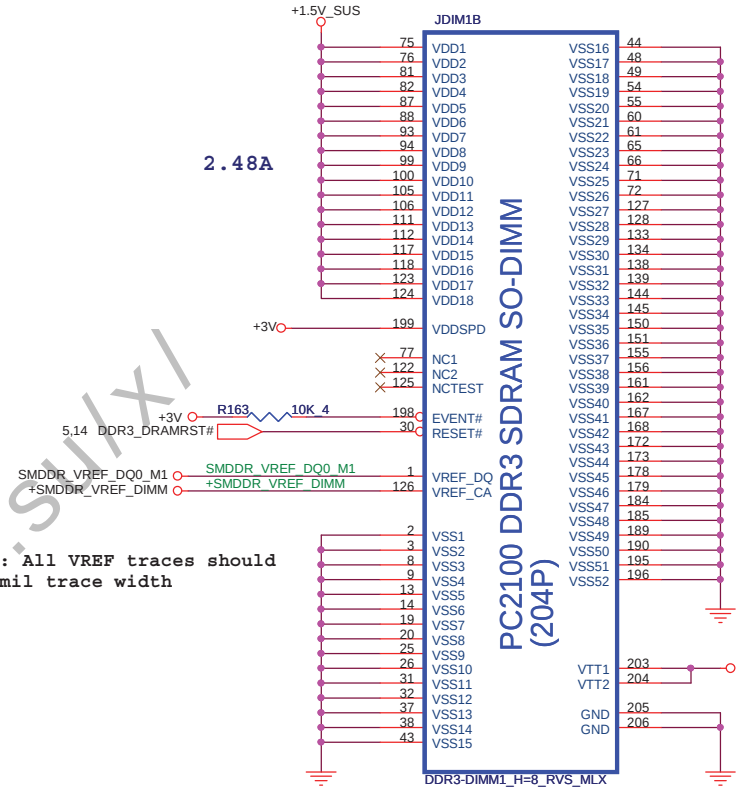
DDR_RVS(DDR)

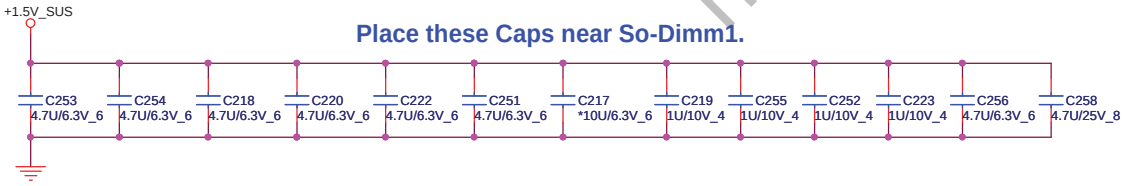


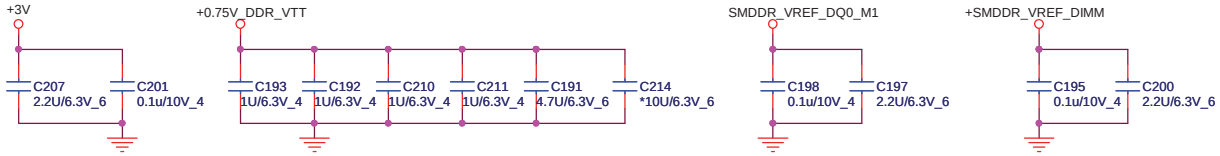
02/23 Remove 0ohm to GND



CAD Note: All VREF traces should have 10 mil trace width

Place these Caps near So-Dimm1.





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CRT Switch

0_ohm Resistor place close to Joint-Point

8 INT_CRT_RED — INT_CRT_RED
8 INT_CRT_GRE — INT_CRT_GRE
8 INT_CRT_BLU — INT_CRT_BLU

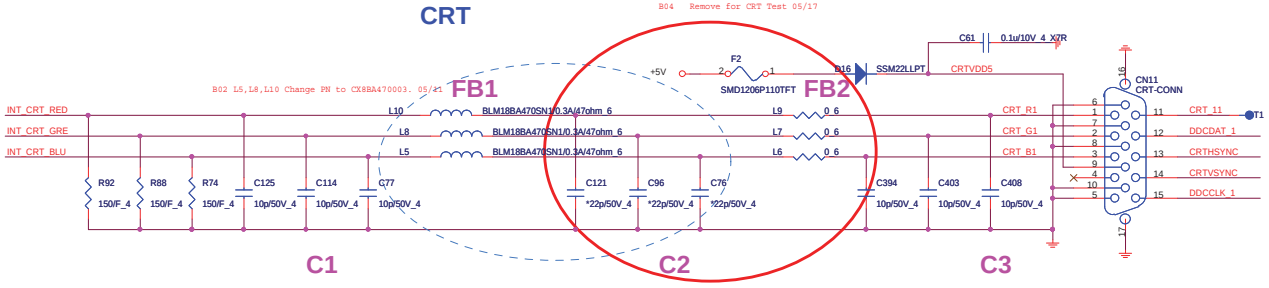
8 INT_CRT_VSYNC — INT_CRT_VSYNC
8 INT_CRT_HSYNC — INT_CRT_HSYNC

8 INT_CRT_DDCDAT — INT_CRT_DDCDAT
8 INT_CRT_DDCCLK — INT_CRT_DDCCLK

CRT

B04 Remove for CRT Test 05/17

B02 L5,L8,L10 Change PN to CX8BA470003. 05/17

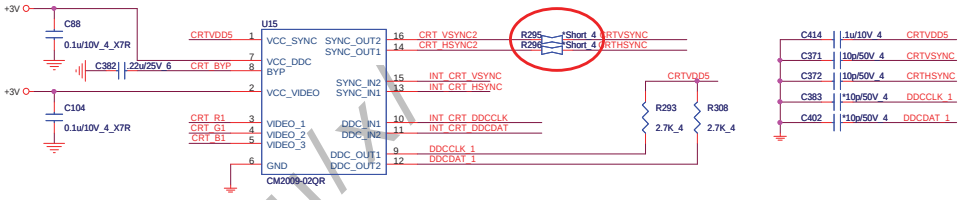


Note:this video filter is a 2-pole,low-pass filter configuration with a target design cutoff frequency of ~200MHZ

C1: 10pF ,C2 : 22pF , C3 :10pF,

FB1:47ohm@100MHZ , FB2:47ohm@100MHZ

B06 Change R295,R296 to short pad. 5/17



LVDS

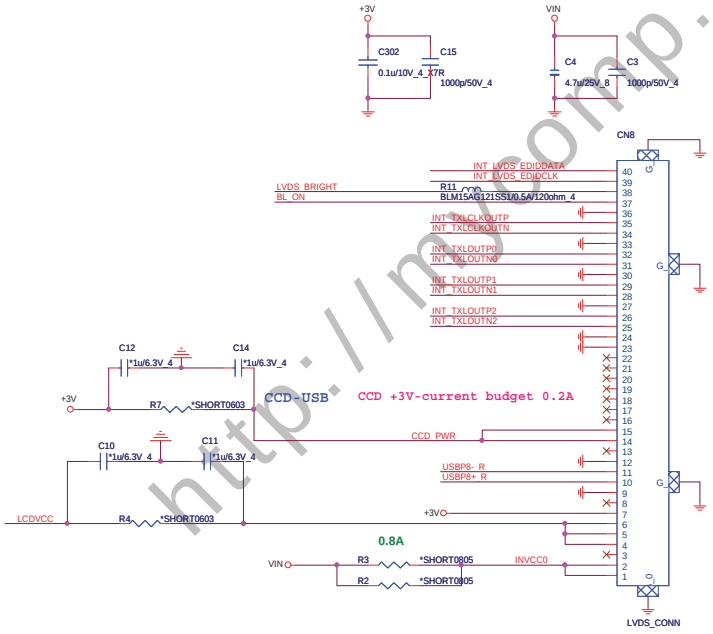
0_ohm Resistor place close to Joint-Point

8 INT_LVDS_EDIDCLK — INT_LVDS_EDIDCLK
8 INT_LVDS_EDIDDATA — INT_LVDS_EDIDDATA
C18 2200p/50V_4
C17 2200p/50V_4
EMI

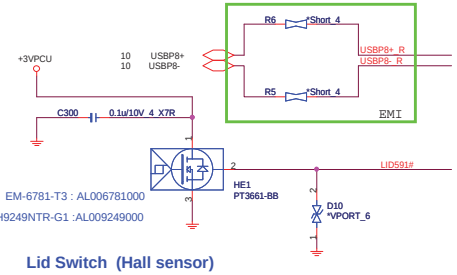
8 INT_LVDS_DIGON — INT_LVDS_DIGON
8 INT_LVDS_BLON — INT_LVDS_BLON

8 INT_TXLCLKOUTP — INT_TXLCLKOUTP
8 INT_TXLCLKOUTN — INT_TXLCLKOUTN
8 INT_TXLOUTP0 — INT_TXLOUTP0
8 INT_TXLOUTN0 — INT_TXLOUTN0
8 INT_TXLOUTP1 — INT_TXLOUTP1
8 INT_TXLOUTN1 — INT_TXLOUTN1
8 INT_TXLOUTP2 — INT_TXLOUTP2
8 INT_TXLOUTN2 — INT_TXLOUTN2

27 CONTRAST — R8 *0_4 — LVDS_BRIGHT
8 INT_LVDS_BRIGHT — R9 0_4

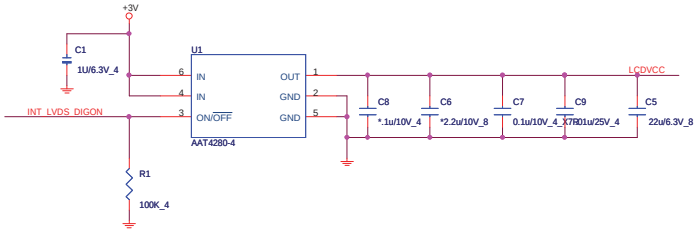


B43 Change 0Ω R5,R6 to short pad, remove CMC L1. 5/19

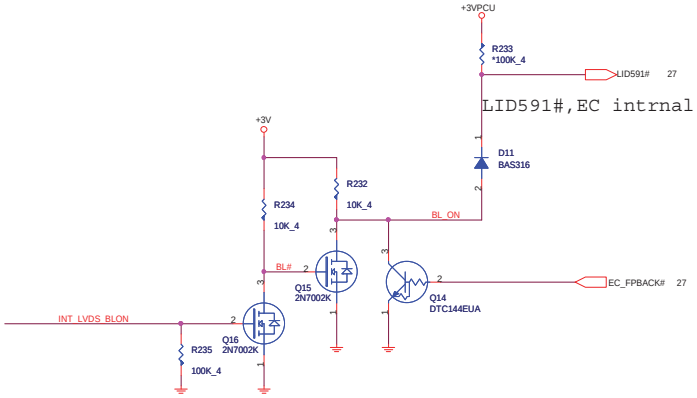


Lid Switch (Hall sensor)

LCD Power



Backlight Control



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	CRT/LVDS/CAMERA/LID	1A

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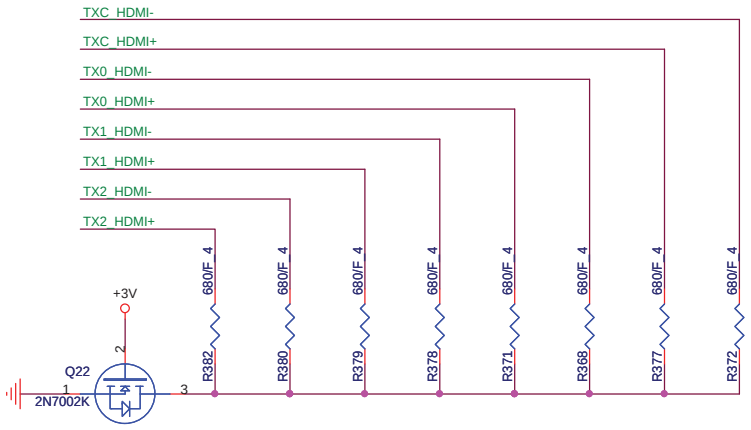
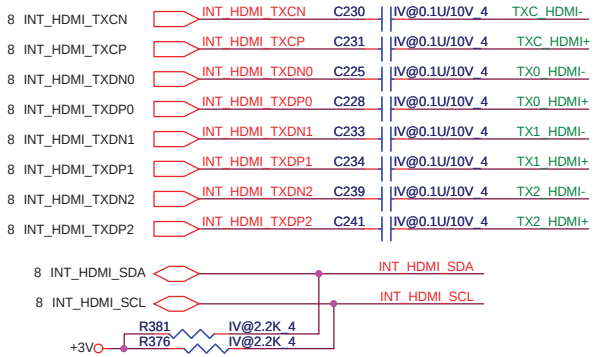


	EV@	IV@
SP@	500 ohm	680 ohm

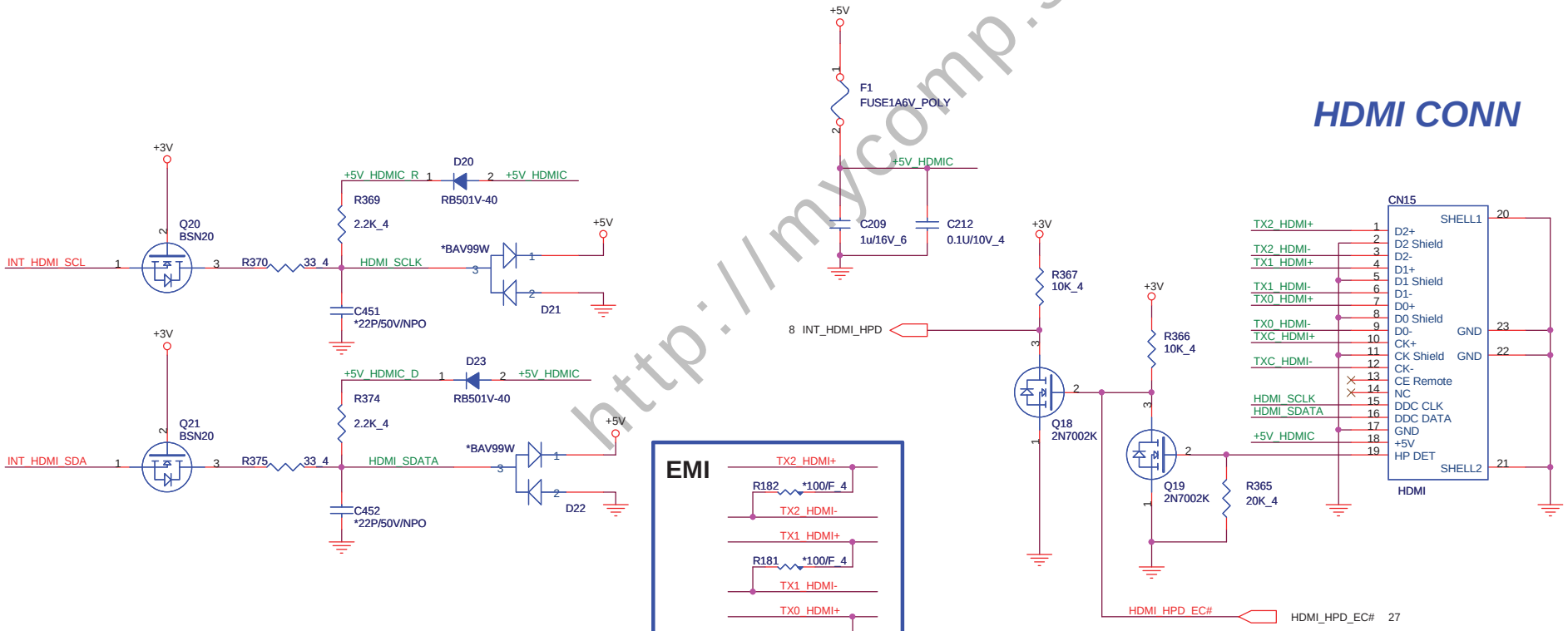
PLACE PULL DOWN RESISTORS CLOSE TO DIFFERENTIAL PAIRS CONNECTED TO SOLID GROUND FLOOD WHICH IS CONTROLLED BY THE FET
AVOID STUBS TO ALL DIFFERENTIAL TRACES

INT-HDMI

PLACE AC CAP CLOSE TO CONNECTOR



HDMI CONN



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LAN (LAN)

<BOM note>
If center tap power come from internal switch regulator
=>Stuff 52SWR@ (Default)
If center tap power come from internal LDO
=>Stuff 52LDO@

* Why does Pin17 CLKREQn connect to Pin16(LED2) and Pin30(DVDDL)?

Power Sequence:
VDD33 to PERSTn >= 100ms

PU in CLK Gen.

<Layout note>
Close to Pin1

L28 4.7uH/1A DCR:0.15ohm LX
C419 0.1U/16V_4
C415 10U/10V_8
VDDCT

C426 33P/50V_4 XTLO_LAN
Y3 25MHz-LAN
C428 33P/50V_4 XTLI_LAN

76.1mA ; 30mil <Layout note> Close to Pin2
+3V_S5 +3V_LAN
R318 2.2_6
C421 10U/10V_8
C133 1U/10V_4
C134 0.1U/16V_4
Int. PU in SB

U3 AR8158 4X4mm 32Pin QFN
AR8158-BL1A-RL

1	LX	CLKREQn	17
2	VDD33	SMCLK	18
3	PERSTn	SMDATA	19
4	WAKEn	TESTMODE	20
5	VDDCT_REG	NC	21
6	VDDCT	TX_N	22
7	AVDDL_REG	TX_P	23
8	XTLO	AVDDL	24
9	XTLI	REFCLK_N	25
10	AVDDH_REG	REFCLK_P	26
11	RBIAS	AVDDL	27
12	TRXP0	RX_P	28
13	TRXN0	RX_N	29
14	TRXP1	DVDDL_REG	30
15	TRXN1	LED[0]	31
16	LED[2]	LED[1]	32
		GND1	33

TP92 TP109 TP112 TP48 TP47 TP46
4,10,19,23,27 PLTRST#
8,19 PCIE_WAKE#
B47 Del short pad R114, connect to PCIE_CLKREQ_LAN# 5/20
PCIE_CLKREQ_LAN# 10
SMBUS for debug only

VDDCT_REG 20mil
VDDCT
AVDDL 20mil
AVDDH 20mil
C425 0.1U/16V_4
C137 0.1U/16V_4
C141 1U/10V_4
C427 0.1U/16V_4
C147 1U/10V_4
C146 0.1U/16V_4
R343 2.37K/F_4 RBIAS

PCIE_RXN1_LAN C138 .1U/10V_4 PCIE_RX1- 10
PCIE_RXP1_LAN C136 .1U/10V_4 PCIE_RX1+ 10
C135 0.1U/16V_4
C132 0.1U/16V_4
CLK_PCIE_LANN 10
CLK_PCIE_LANP 10
PCIE_TX1+ 10
PCIE_TX1- 10
DVDDL 20mil
C130 *0.1U/16V_4
C129 1U/10V_4
C131 0.1U/16V_4
LAN_ACTLED
LAN_LINKLED#

TX0P C170 6.8PF/50V_4
TX0N C172 6.8PF/50V_4
TX1P C173 6.8PF/50V_4
TX1N C176 6.8PF/50V_4

<Layout note>
Close to LAN Chip
1nF reserved for EMI
1/7 swap the pin define for layout

RN1 49.9/F_4P2R
RN2 49.9/F_4P2R
C434 0.1U/16V_4 C433 *1000P/50V_4
C435 0.1U/16V_4 C436 *1000P/50V_4

1/7 change solution for surge

U17 U18 UCLAMP2512T.TCT
X-TX1N X-TX1P X-TX0N X-TX0P
TX1N TX1P TX0N TX0P

+3V_S5 2
+1.1V analog power 24/27
+1.7V analog power 6

ATHEROS AR8158

VDD33	AVDDL_REG	7
AVDDL	AVDDH_REG	10
	DVDDL_REG	30
	VDDCT_REG	5
VDDCT	LX	1

+1.1V regulator output (For all the analog 1.1V supply pins)
+2.7V regulator output
+1.1V regulator output (For all the digital 1.1V supply pins)
+1.8V regulator output (For VDDCT when LDO mode)
+1.7V Switching regulator (For VDDCT when switching mode)

TRANSFORMER (LAN)

EMI
X-TX1N C183 *6.8PF/50V_4
X-TX1P C179 *6.8PF/50V_4
X-TX0N C167 *6.8PF/50V_4
X-TX0P C163 *6.8PF/50V_4

B27 L11 change from 0 Ω to short pad. 5/18
VDDCT L11 *Short_6 AVDD_CEN
CX8EG601000 0.5A/600OHM_6
C158 *1U/6.3V_4
C174 0.1U/16V_4
C177 *1000P/50V_4
C162 0.1U/16V_4
C169 *1000P/50V_4

U19 NS0014 LF_Bothhand
TD- TD+ CT NC NC CT RD- RD+
TX- TX+ CT NC NC CT RX- RX+
TX1N TX1P TX0N TX0P
X-TX1N X-TX1P TERM0 TERM1 X-TX0N X-TX0P

R154 75/F_8 R159 75/F_8
TERM9
R164 1M_8
D3 B88069X9231T203
C447 220P/3KV_1808

D3: CY003100Z06 (2nd) / CY231T20Z00 (1st & non prefer)
U17,U18: BC02512TZ00 (2nd) / BC02512TZ00 (1st)

RJ45 Connector (LAN)

R149 5.1K/J_8
C152 *0.1U/50V_8 LAN_ACTLED
Active LED Pin:
Non-overclocking=>active high

R165 *5.1K/J_8
C194 *0.1U/50V_8 LAN_LINKLED#
LINK LED Pin:
SWR mode=>active low
LDO mode=>active high

B53 Del short pad R133,R168, connect to GND.
LAN_ACTLED R150 510/J_6 N27354430
LAN_LINKLED# R170 510/J_6
+3V_S5 R171 *SHORT0805

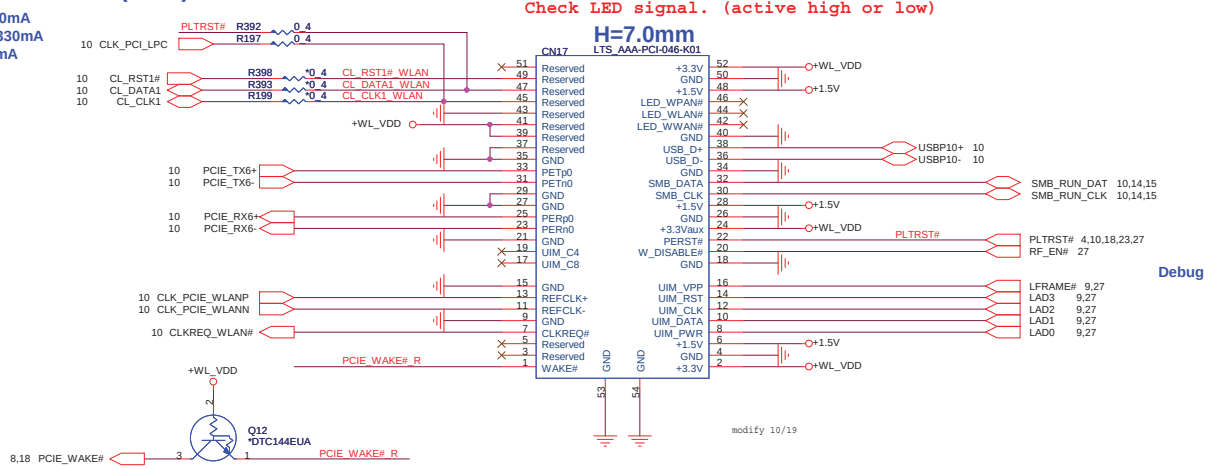
CN13 RJ45
YELLOW_N YELLOW_P GREEN_N GREEN_P GND2 GND1
X-TX0P X-TX0N X-TX1P X-TX1N TERM9 TERM9
0+ 0- 1+ 2+ 2- 1- 3+ 3-

Quanta Computer Inc.			
PROJECT : ZQR			
Size	Document Number		Rev
	LAN AR8158L		1A
Date: Monday, May 23, 2011		Sheet 18 of 35	

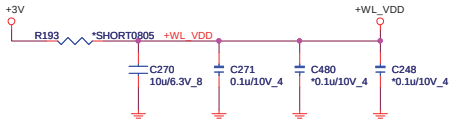
MINI-CARD WLAN(MPC)

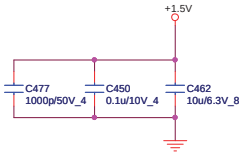
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

Check LED signal. (active high or low)



Debug



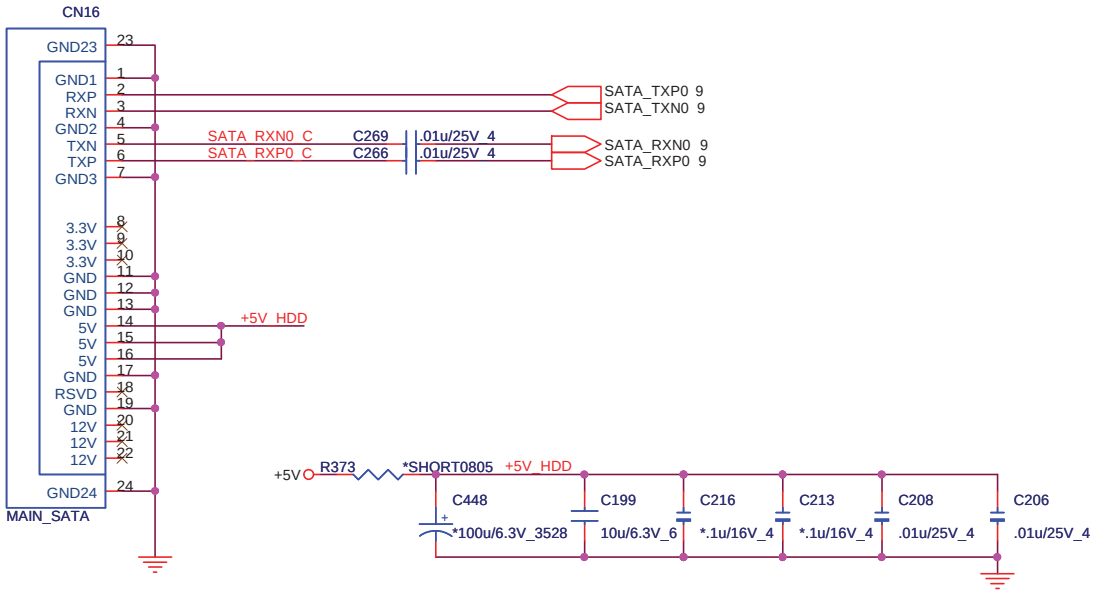


Quanta Computer Inc.
PROJECT : ZQR

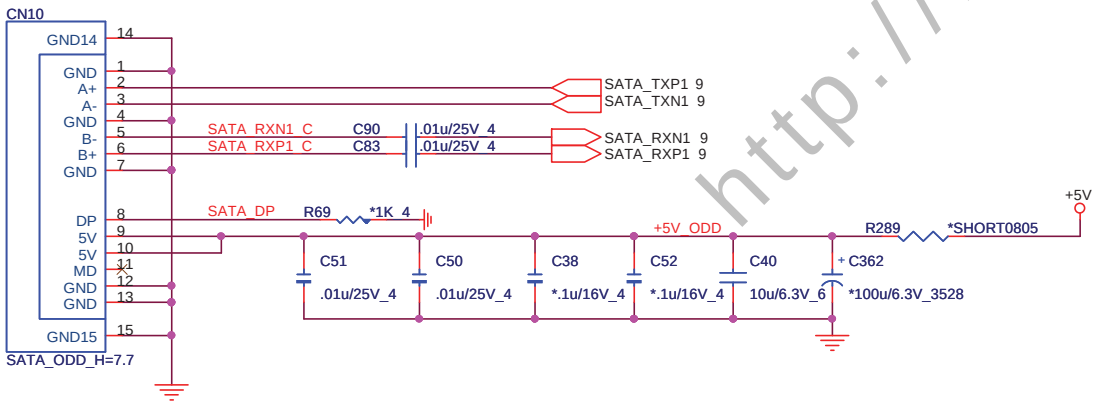
Size	Document Number	Rev
	MINI PCI-E card/TV	1A

Date: Monday, May 23, 2011 Sheet 19 of 35

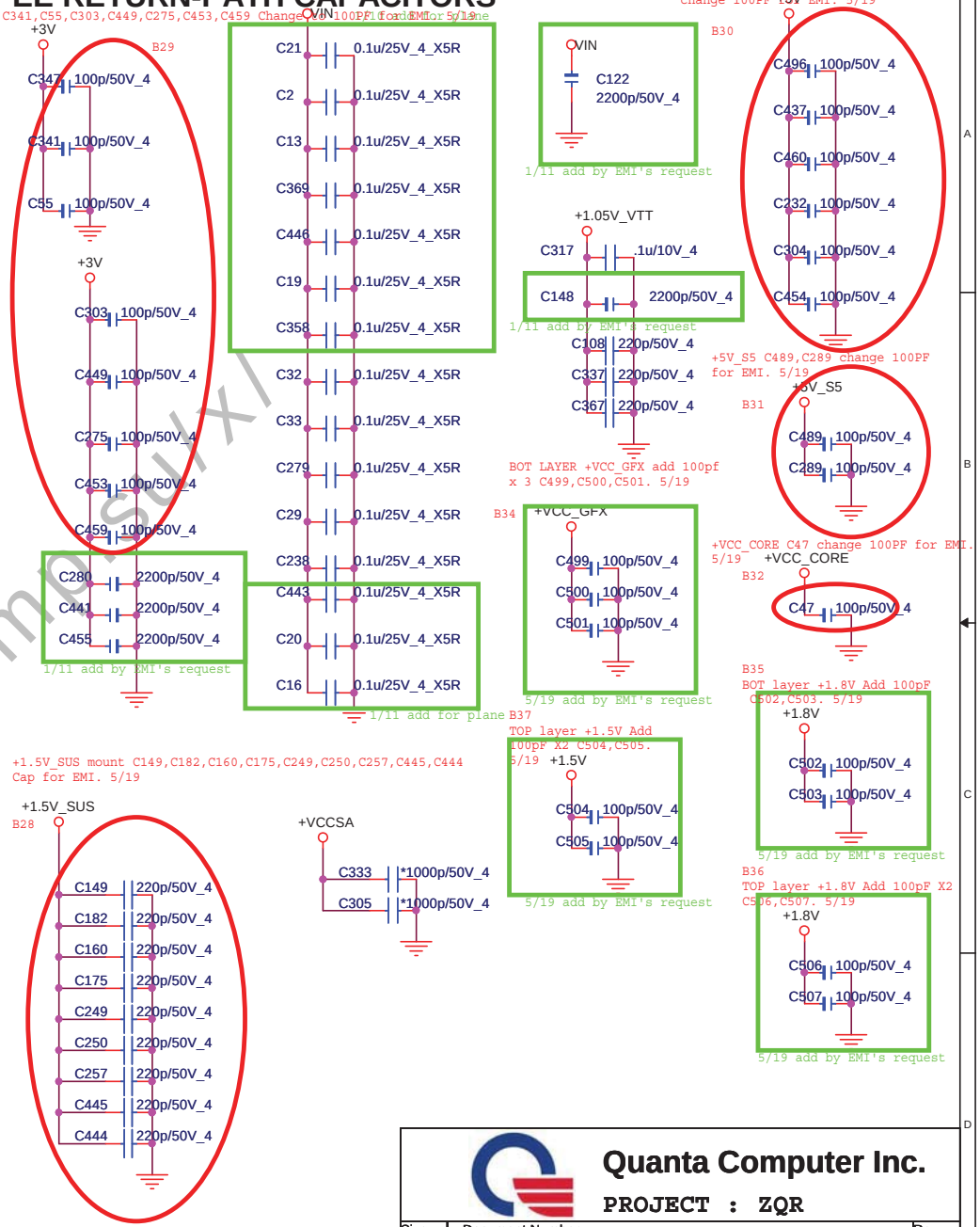
MAIN SATA HDD



ODD (SATA)



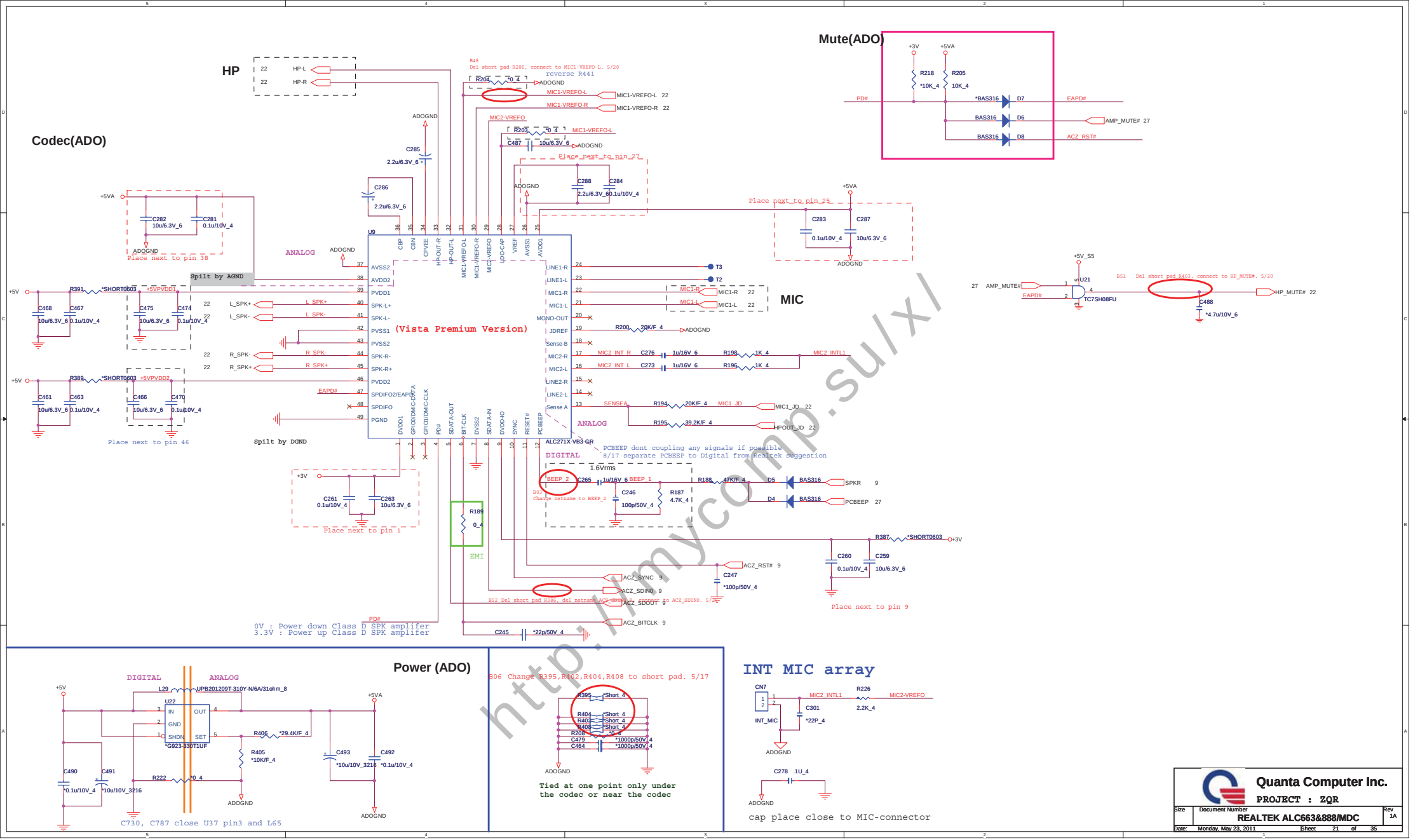
EE RETURN-PATH CAPACITORS



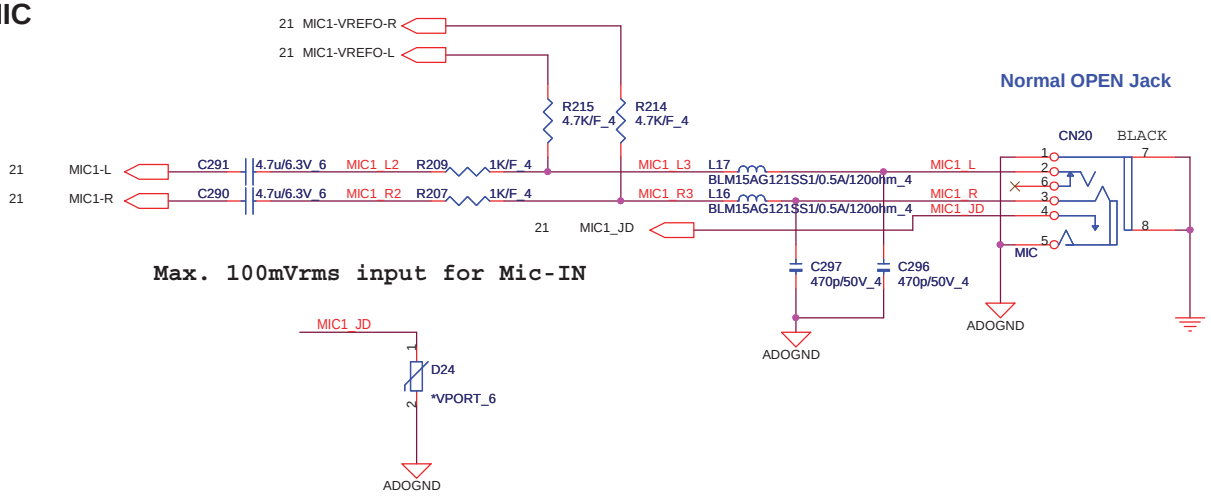
Quanta Computer Inc.

PROJECT : ZQR

Size	Document Number	Rev
	SATA-HDD/ODD	1A
Date: Monday, May 23, 2011	Sheet 20 of 35	

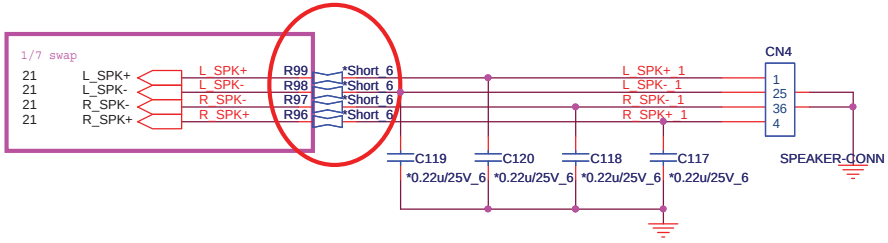


MIC

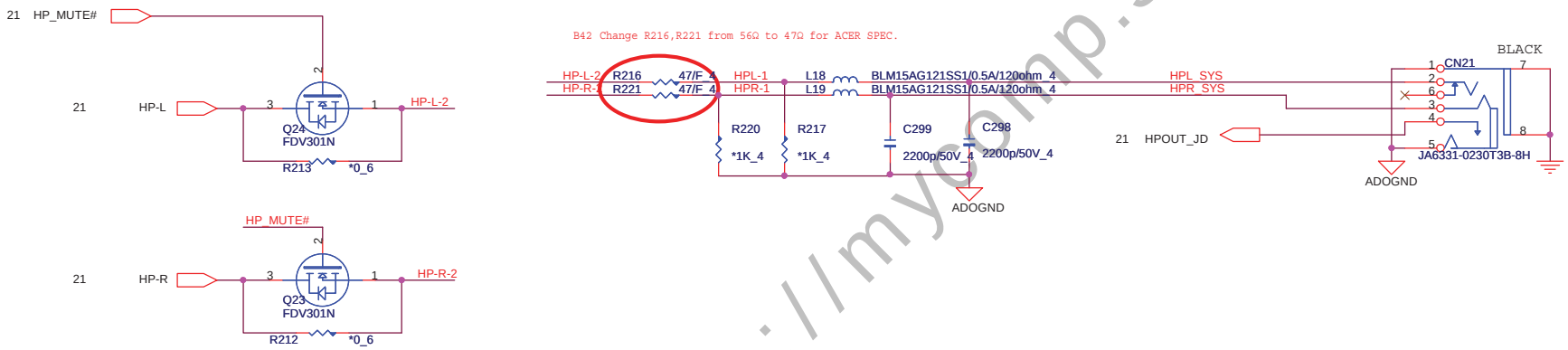


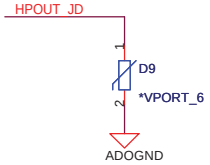
Internal Speaker

B27 R96,R97,R98,R99 change from 0 Ω to short pad. 5/18



HP/SPDIF





Quanta Computer Inc.

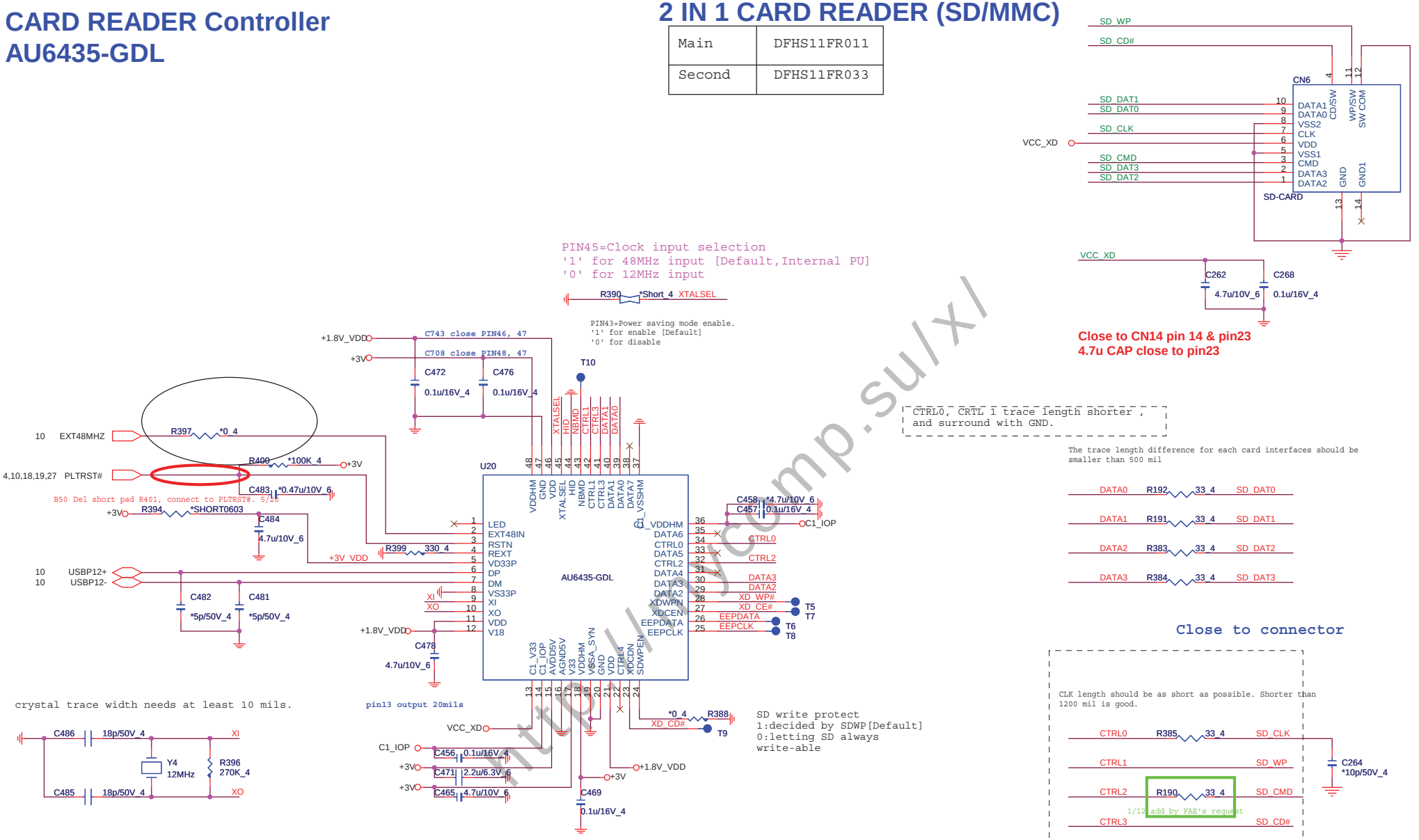
PROJECT : ZQR

Size	Document Number	Rev
	AMP /AUDIO JACK CONN	1A
Date: Monday, May 23, 2011	Sheet 22 of 35	

CARD READER Controller
AU6435-GDL

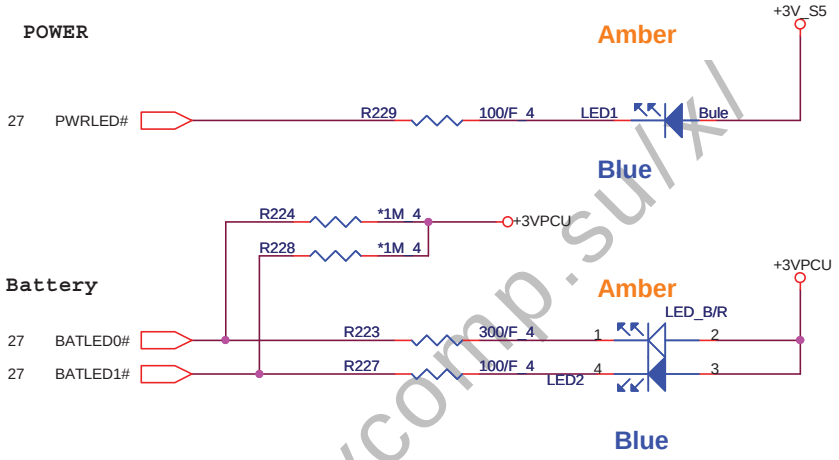
2 IN 1 CARD READER (SD/MMC)

Main	DFHS11FR011
Second	DFHS11FR033



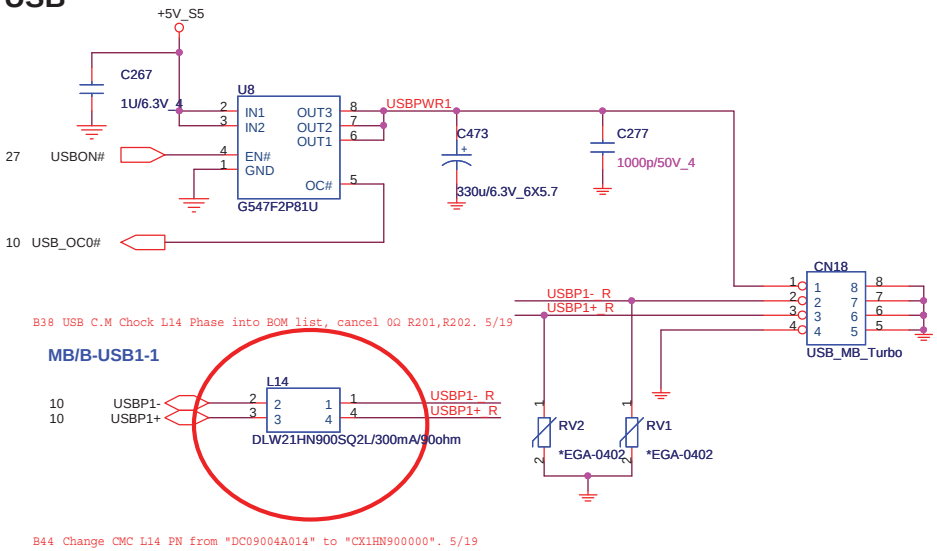
PROJECT : ZQ5 Quanta Computer Inc.			
Size	Document Number AU6433 CardReader		Rev 1A
Date:	Monday, May 23, 2011	Sheet 23 of	43

LED

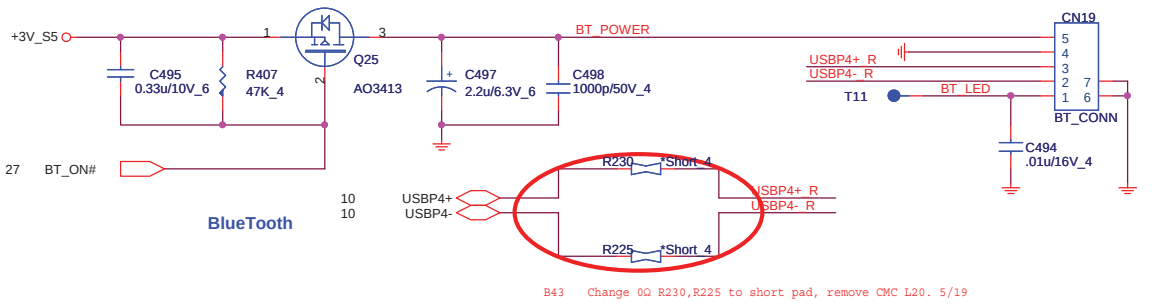


Quanta Computer Inc.		
PROJECT : ZQR		
Size	Document Number: POWER/MMB/LAUNCH/LED	Rev: 1A
Date: Monday, May 23, 2011	Sheet 24 of 35	

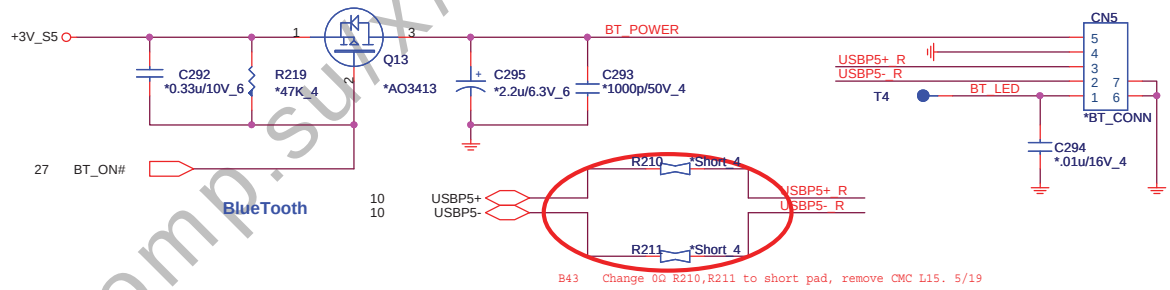
USB



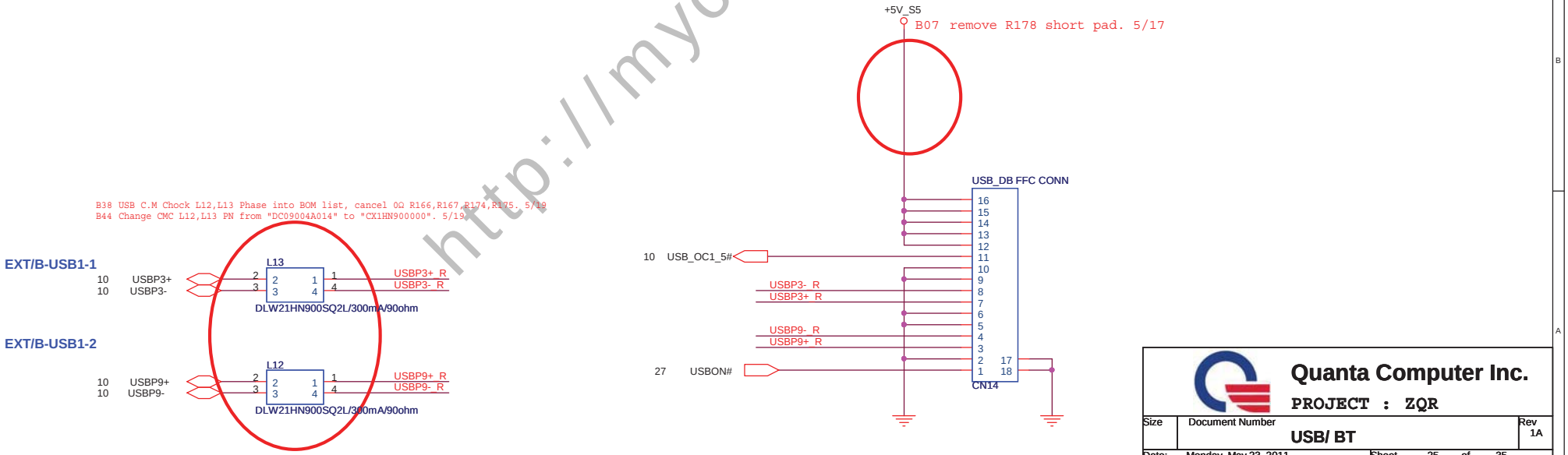
BLUETOOTH CONNECTOR for 3.0



Reserve



USB/B



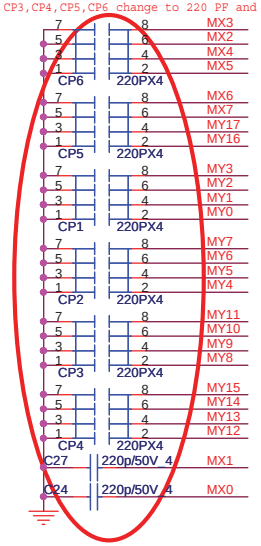
Quanta Computer Inc.

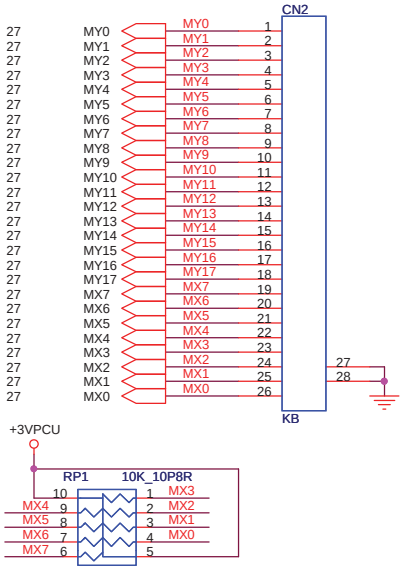
PROJECT : ZQR

Size	Document Number	Rev
	USB/ BT	1A
Date: Monday, May 23, 2011	Sheet 25 of 35	

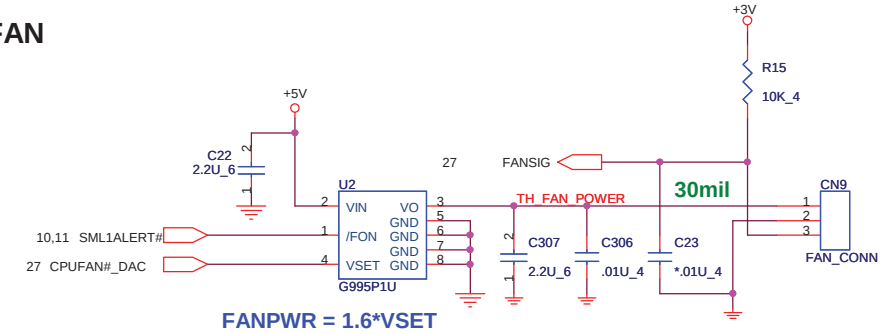
K/B

KB Cap CP1,CP2,CP3,CP4,CP5,CP6 change to 220 PF and phase into BOM list. 5/19 B33



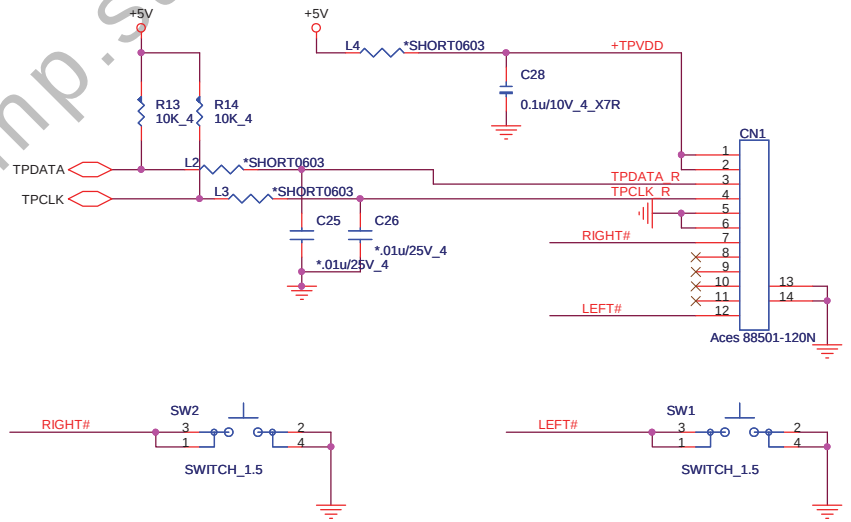


CPU FAN

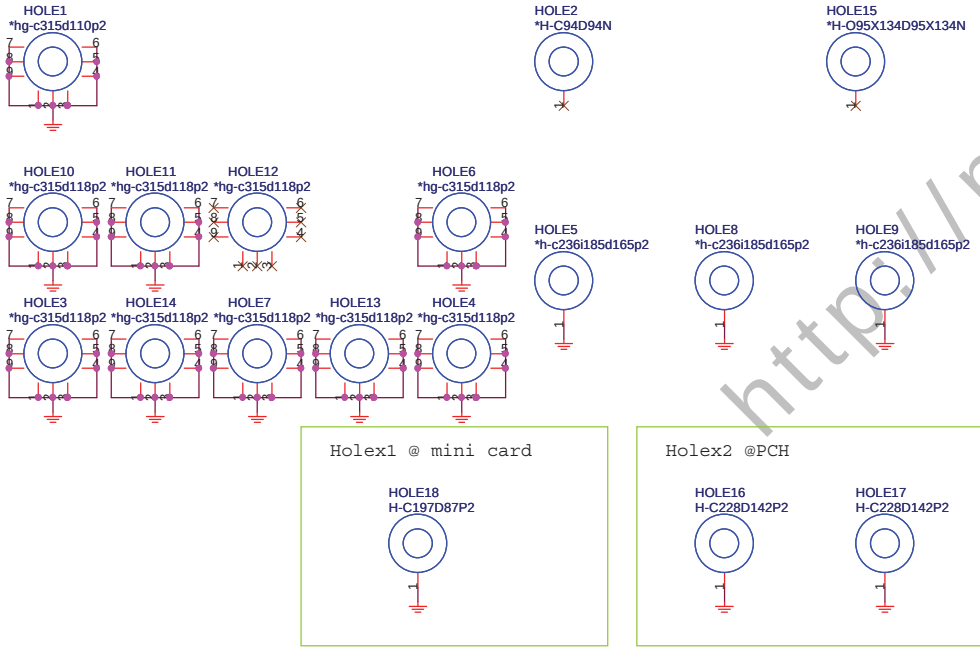


FANPWR = 1.6*VSET

TOUCHPAD & Switch CONN.



HOLE



Holex1 @ mini card

HOLE18 H-C197D87P2

Holex2 @PCH

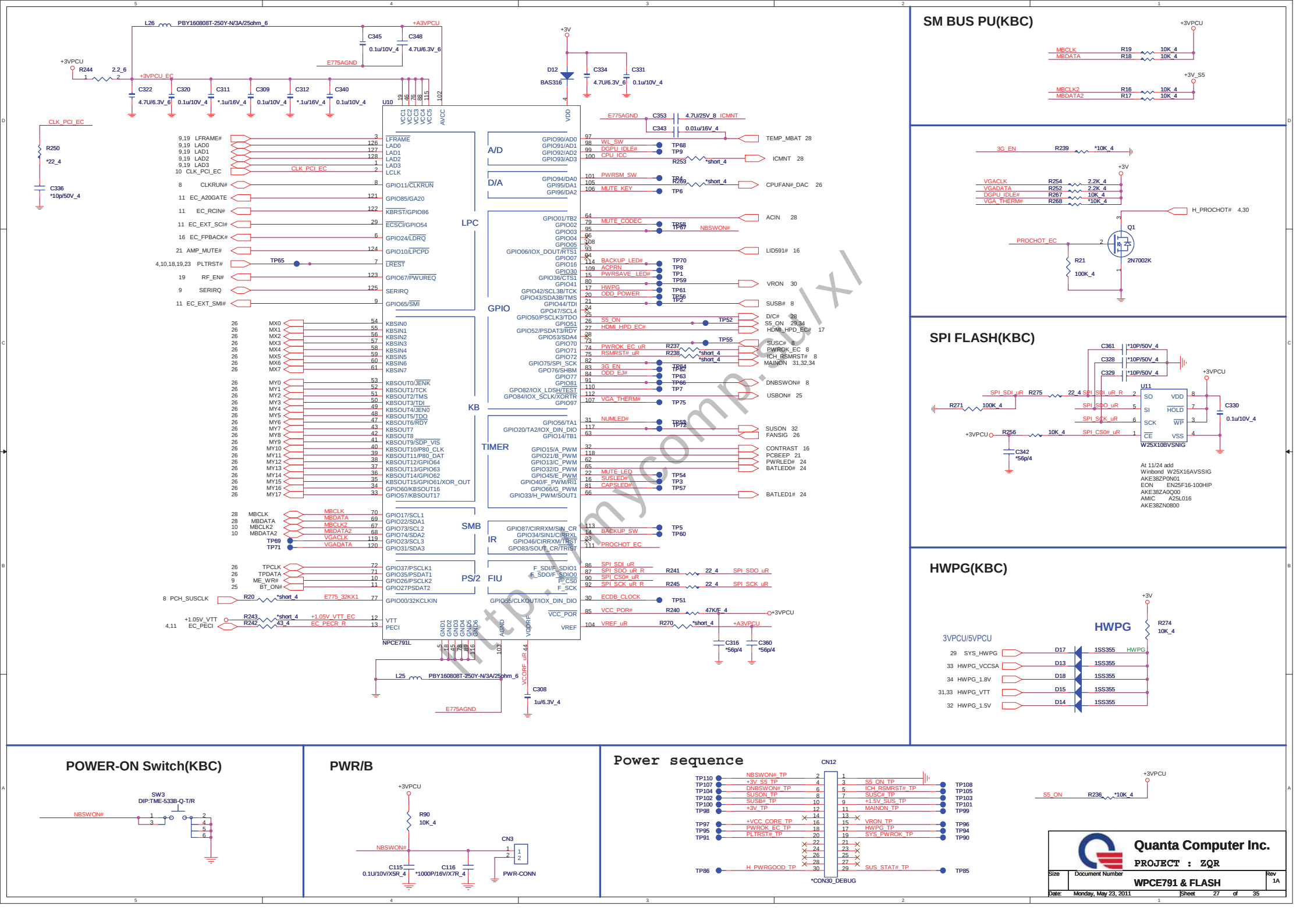
HOLE16 H-C228D142P2

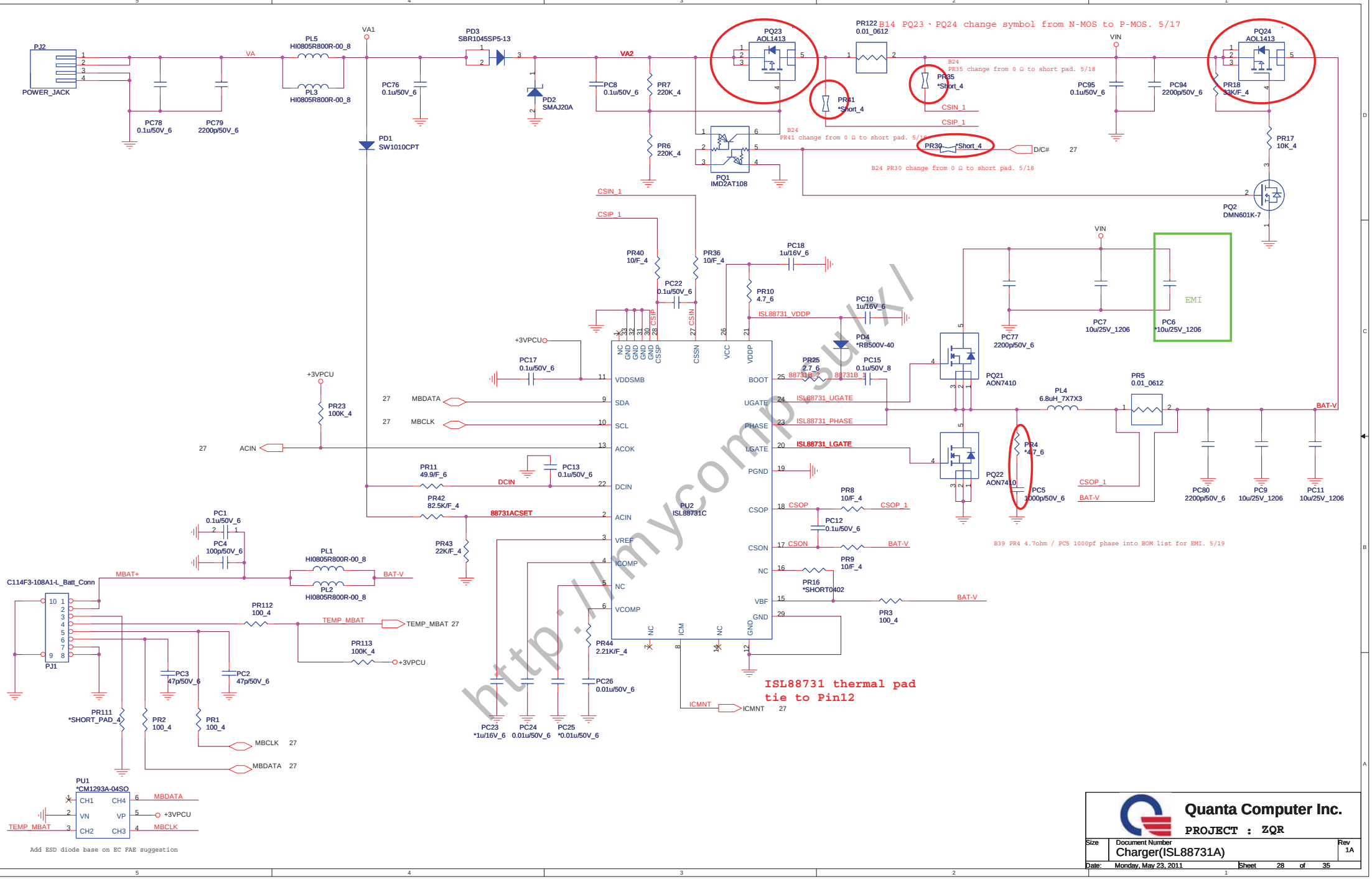
HOLE17 H-C228D142P2

Quanta Computer Inc.

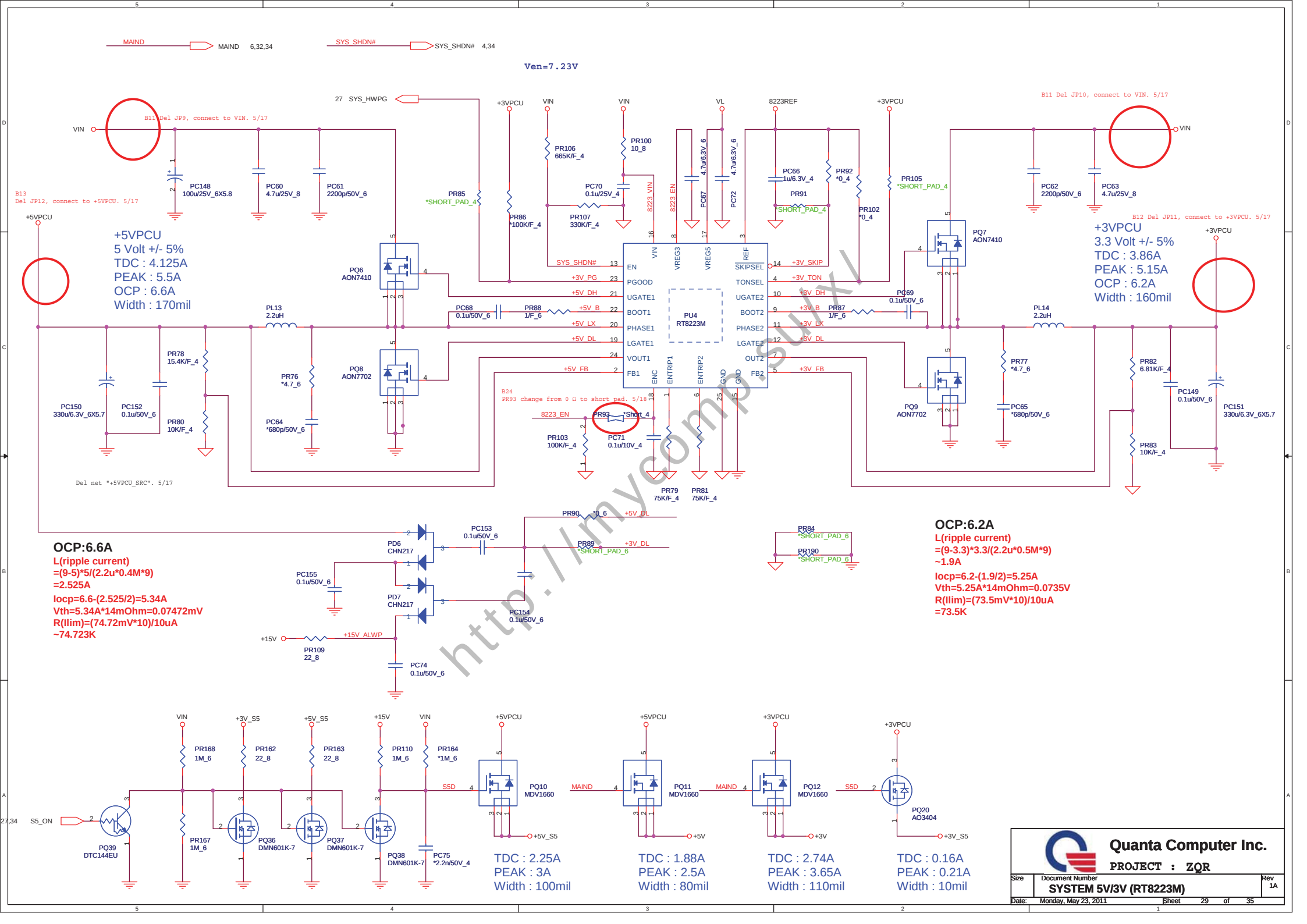
PROJECT : ZQR

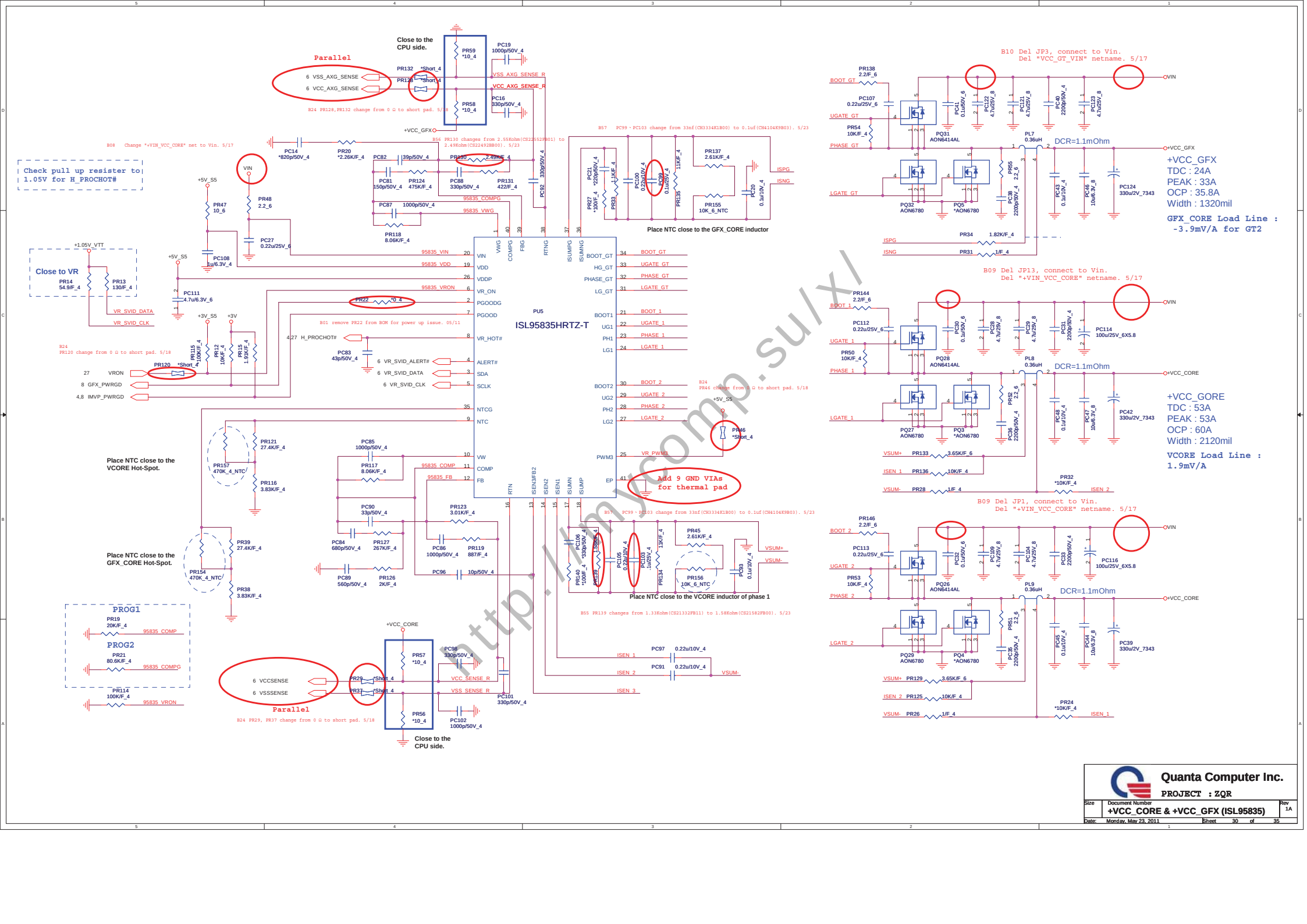
Size	Document Number	Rev
	KB/FAN/TP+FP	1A
Date: Monday, May 23, 2011	Sheet 26 of 35	


SM BUS PU(KBC)
SPI FLASH(KBC)
HWPG(KBC)
POWER-ON Switch(KBC)
PWR/B
Power sequence
NPCE791L
LPC
A/D
D/A
GPIO
KB
SMB
PS/2
TIMER
IR
FIU
Quanta Computer Inc.
PROJECT : ZQR
WPCE791 & FLASH
Rev 1A
Size
Document Number
Date: Monday, May 23, 2011
Sheet 27 of 35
http://mycomp.cc/xl

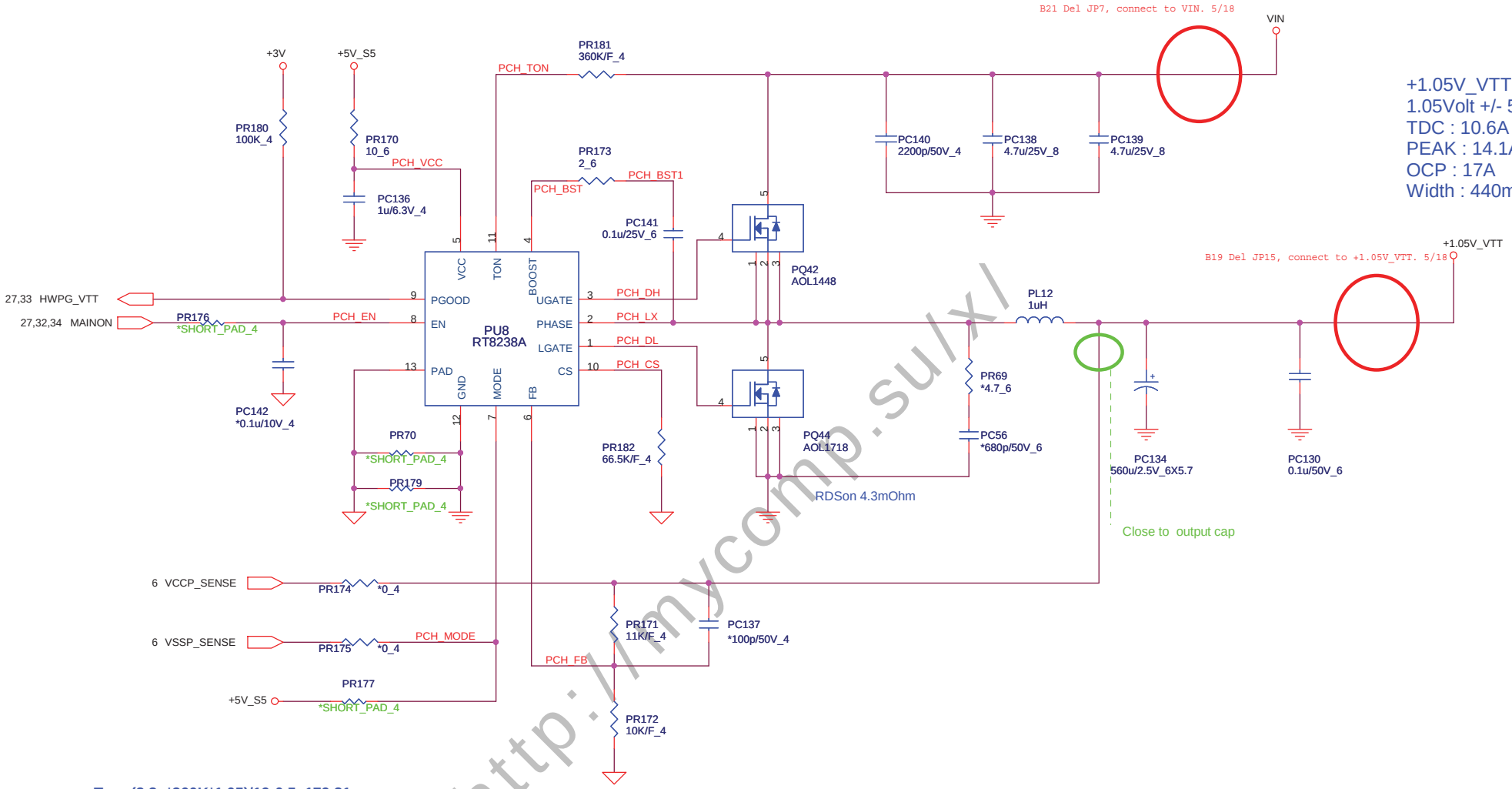


Quanta Computer Inc.			
PROJECT : ZQR			
Size	Document Number: Charger(ISL88731A)		Rev: 1A
Date: Monday, May 23, 2011		Sheet 28 of 35	


MAIND
MAIND 6,32,34
SYS_SHDN#
SYS_SHDN# 4,34
Ven=7.23V
27 SYS_HWPG
B11 Del JP9, connect to VIN. 5/17
B11 Del JP10, connect to VIN. 5/17
B13
Del JP12, connect to +5VPCU. 5/17
B12 Del JP11, connect to +3VPCU. 5/17
+5VPCU
5 Volt +/- 5%
TDC : 4.125A
PEAK : 5.5A
OCP : 6.6A
Width : 170mil
+3VPCU
3.3 Volt +/- 5%
TDC : 3.86A
PEAK : 5.15A
OCP : 6.2A
Width : 160mil
PU4
RT8223M
B24
PR93 change from 0 Ω to short pad. 5/16
Del net "+5VPCU_SRC". 5/17
OCP:6.6A
L(ripple current)
=(9-5)*5/(2.2u*0.4M*9)
=2.525A
Iocp=6.6-(2.525/2)=5.34A
Vth=5.34A*14mOhm=0.07472mV
R(Ilim)=(74.72mV*10)/10uA
~74.723K
OCP:6.2A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.5M*9)
~1.9A
Iocp=6.2-(1.9/2)=5.25A
Vth=5.25A*14mOhm=0.0735V
R(Ilim)=(73.5mV*10)/10uA
=73.5K
TDC : 2.25A
PEAK : 3A
Width : 100mil
TDC : 1.88A
PEAK : 2.5A
Width : 80mil
TDC : 2.74A
PEAK : 3.65A
Width : 110mil
TDC : 0.16A
PEAK : 0.21A
Width : 10mil
http://mycomp.sytx/
Quanta Computer Inc.
PROJECT : ZQR
SYSTEM 5V/3V (RT8223M)
Size
Document Number
Rev 1A
Date: Monday, May 23, 2011
Sheet 29 of 35



Quanta Computer Inc.		
PROJECT : ZQR		
Size	Document Number: +VCC_CORE & +VCC_GFX (ISL95835)	Rev: 1A
Date: Monday, May 23, 2011	Sheet 30 of 35	



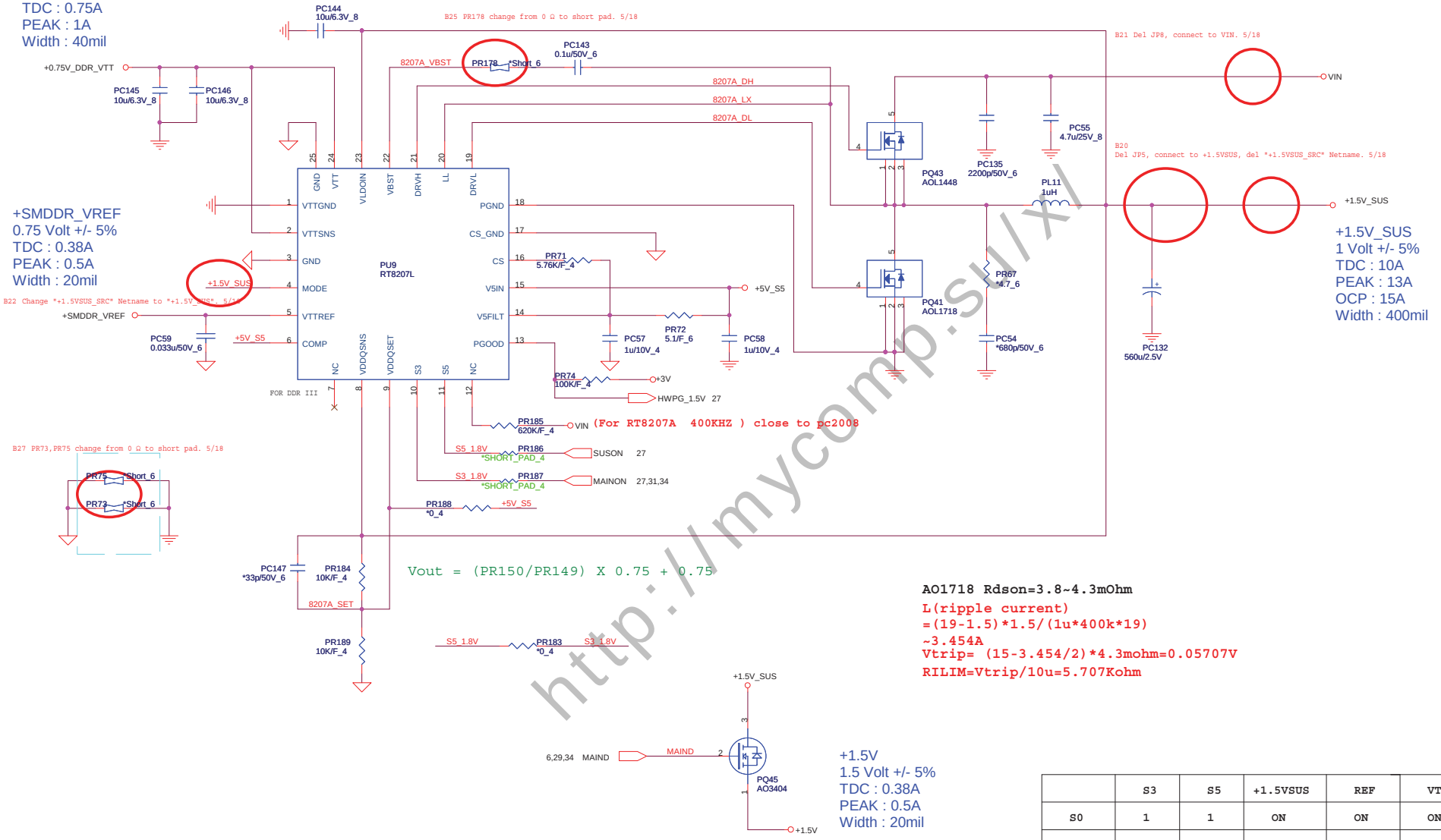
Ton=(8.8p*360K*1.05)/19-0.5=179.81ns
Lcurrent=(19-1.05)*179ns/1uH=3.228A
Iocp=17-3.228/2=15.386A
Vcs=15.386*4.3mohm=0.06616V
Rcs=0.06616/1u=66.16Kohm

VOUT=(1+R1/R2)*0.5

Quanta Computer Inc.		
PROJECT : ZQR		
Size	Document Number: +PCH&VTT (RT8238A)	Rev: 1A
Date: Monday, May 23, 2011	Sheet 31 of 35	

+0.75V_DDR_VTT
0.75 Volt +/- 5%
TDC : 0.75A
PEAK : 1A
Width : 40mil

+SMDDR_VREF
0.75 Volt +/- 5%
TDC : 0.38A
PEAK : 0.5A
Width : 20mil



+1.5V_SUS
1 Volt +/- 5%
TDC : 10A
PEAK : 13A
OCP : 15A
Width : 400mil

AO1718 Rdson=3.8~4.3mOhm
L(ripple current)
=(19-1.5)*1.5/(1u*400k*19)
~3.454A
Vtrip= (15-3.454/2)*4.3mohm=0.05707V
RILIM=Vtrip/10u=5.707Kohm

+1.5V
1.5 Volt +/- 5%
TDC : 0.38A
PEAK : 0.5A
Width : 20mil

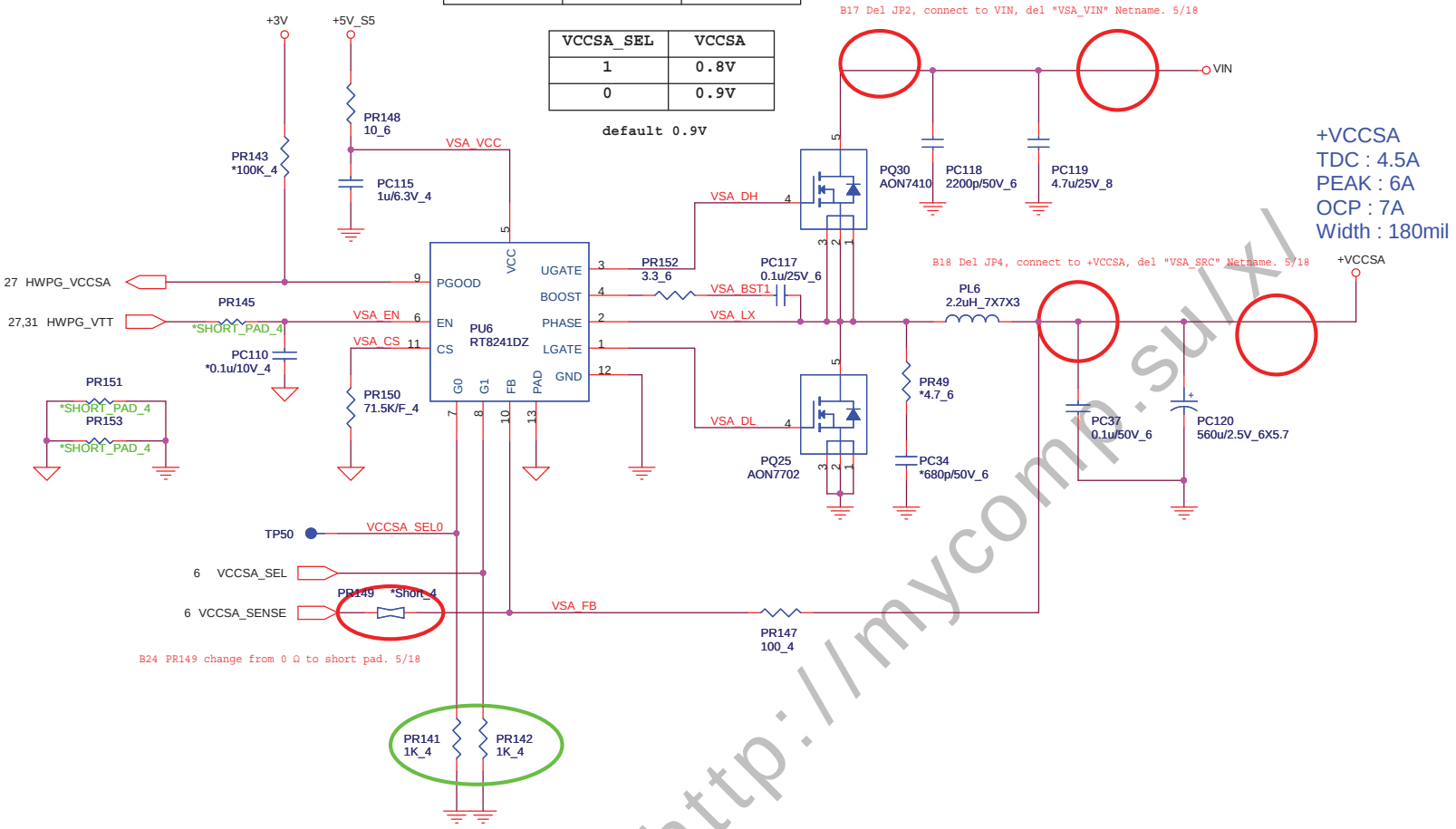
	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.
PROJECT : ZQR
Size | Document Number: DDR 1.5V(RT8207A) | Rev 1A
Date: Monday, May 23, 2011 | Sheet 32 of 35

G0	G1	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

VCCSA_SEL	VCCSA
1	0.8V
0	0.9V

default 0.9V

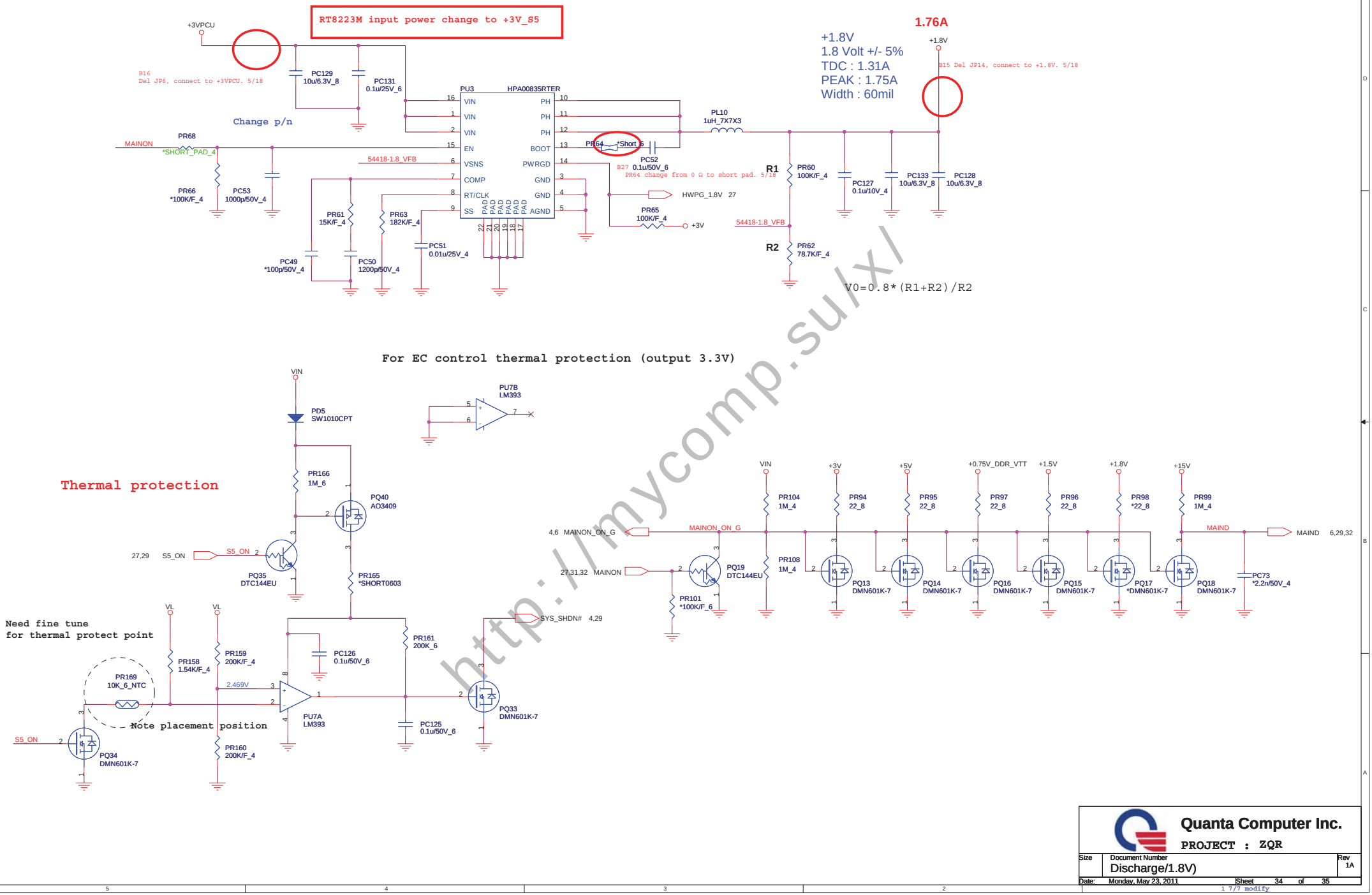


+VCCSA
TDC : 4.5A
PEAK : 6A
OCP : 7A
Width : 180mil

OCP=7A
Iripple=(19-0.9)*0.9/(2.2u*300K*19)
=1.299A
Rth=14mohm*8*(7-0.65)/10uA
=71.125K
Ipeak=8.299A

Quanta Computer Inc.
PROJECT : ZQR

Size	Document Number	Rev
	+VCCSA(RT8241A)	1A
Date: Monday, May 23, 2011	Sheet 33 of 35	



Quanta Computer Inc.

PROJECT : ZQR

Size	Document Number	Rev
	Discharge/1.8V)	1A

Date: Monday, May 23, 2011 Sheet 34 of 35

1 7/7 modify

Model

ZQR MB

REV	CHANGE LIST
B	2011/05/11 B01 remove PR22 from BOM for power up issue. B02 L5,L8,L10 Change PN to CX8BA470003. 2011/05/16 B03 Change net closed to Audio Codec PCBEEP netname to BEEP_2 2011/05/17 B04 Change L6,L7,L9 to 0Ω, remove C76,C96,C121 for CRT Test. B05 Add R409, remove U5, C142 for saving cost. B06 Change Bottom side 0Ω to short pad for cost and SMT cycle time issue; R284,R295,R296,R392,R395,R401,R402,R403,R404,R408. B07 Remove R178 short pad, connect to +5V_S5. B08 Change "+VIN_VCC_CORE" net to Vin. B09 Del JP1,JP13, connect to Vin, del "+VIN_VCC_CORE" netname. B10 Del JP3, connect to Vin. Del "VCC_GT_VIN" netname. B11 Del JP9,JP10 connect to Vin. B12 Del JP11, connect to +3VPCU. B13 Del JP12, connect to +5VPCU. B14 PQ23、PQ24 change symbol from N-MOS to P-MOS 2011/05/18 B15 Del JP14, connect to +1.8V. B16 Del JP6, connect to +3VPCU. B17 Del JP2, connect to VIN, del "VSA_VIN" Netname. B18 Del JP4, connect to +VCCSA, del "VSA_SRC" Netname. B19 Del JP15, connect to +1.05V_VTT. B20 Del JP5, connect to +1.5VSUS, del "+1.5VSUS_SRC" Netname. B21 Del JP7,JP8 connect to VIN. B22 Change "+1.5VSUS_SRC" Netname to "+1.5V_SUS". B23 Mount C70, C71 for +Vcc_core overshoot issue. B24 PR29,PR30,PR35,PR37,PR41,PR46,PR93,PR120,PR128,PR132,PR149(0_4) change from 0ohm to short-pad. B25 PR178(0_6) change from 0ohm to short-pad. B26 R114,R187,R206(0_4) change from 0ohm to short-pad. B27 L11,PR64,PR73,PR75,R96,R97,R98,R99,R132,R168(0_6) change from 0ohm to short-pad. 2011/05/19 B28 Page 20 +1.5V_SUS mount C149,C182,C160,C175,C249,C250,C257,C445,C444 Cap for EMI B29 Page 20 +3V C347,C341,C55,C303,C449,C275,C453,C459 Change to 100PF for EMI. B30 Page 20 +5V C496,C437,C460,C232,C304,C454 change 100PF for EMI. B31 Page 20 +5V_S5 C489,C289 change 100PF for EMI. B32 Page 20 +VCC_CORE C47 change 100PF for EMI. B33 KB Cap CP1,CP2,CP3,CP4,CP5,CP6 change to 220 PF and phase into BOM list for EMI. B34 BOT layer +VCC_GFX add 100pf x 3 C499,C500,C501 for EMI. B35 BOT layer +1.8V Add 100pF X2 C502,C503 for EMI. B36 TOP layer +1.8V Add 100pF X2 C506,C507 for EMI. B37 TOP layer +1.5V Add 100pF X2 C504,C505 for EMI. B38 USB C.M Chock L12,L13,L14 Phase into BOM list, cancel 0Ω R166,R167,R174,R175,R201,R202 for EMI. B39 PR4 4.7ohm / PC5 1000pf phase into BOM list for EMI. B40 Change R386 from 22Ω to short pad. B41 Add a MOSFET Q26,R410,R412 to separate CODE SYNC and PCH Strap signal to avoid leakage issue. B42 Change R216,R221 from 56Ω to 47Ω for ACER SPEC. B43 Change 0Ω R5,R6,R210,R211,R225,R230 to short pad, remove CMC L1,L15,L20 for SMT. B44 Change CMC L12,L13,L14 PN from "DC09004A014" to "CX1HN900000". B45 Remove C315 for cost issue. 2011/05/20 B46 R192,R187 change from short pad to 0Ω. B47 Del short pad R114, connect to PCIE_CLKREQ_LAN#. B48 Del short pad R206, connect to MIC1-VREFO-L. B49 Del short pad R284, connect to ME_WR#. B50 Del short pad R401, connect to PLTRST#. B51 Del short pad R403, connect to HP_MUTE#. B52 Del short pad R386, del netname ACZ_SDIN0_R, connect to ACZ_SDIN0. B53 Del short pad R133,R168, connect to GND. B54 Del C442. 2011/05/23 B55 PR139 changes from 1.33Kohm(CS21332FB11) to 1.58Kohm(CS21582FB00). B56 PR130 changes from 2.55Kohm(CS22552FB01) to 2.49Kohm(CS22492BB00). B57 PC99、PC103 change from 33nf(CH3334K1B00) to 0.1uf(CH4104K9B03).
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