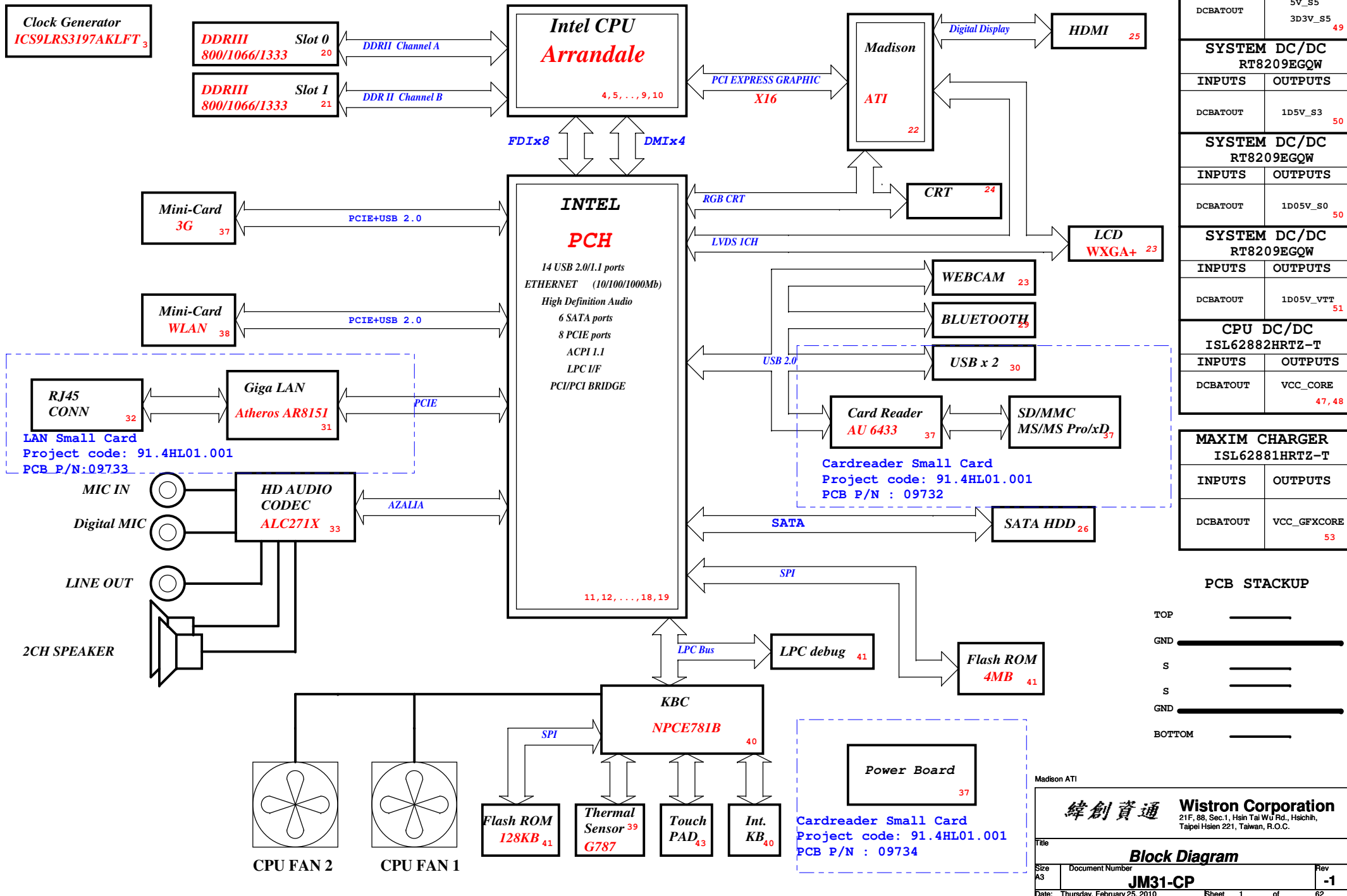


JM31-CP Block Diagram

Project code: 91.4HL01.001

PCB P/N : 48.4HL01.031

REVISION : 09921-3



A B

PCH Strapping

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	Default - Internal pull-up. Low (0) = Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN#/GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIE Routing

LANE1	LAN
LANE2	MiniCard1
LANE3	MiniCard2

USB Table

Pair	Device
0	USB1
1	USB2
2	USB4
3	MINICARD2
4	WECAM
5	Blue Tooth
6	MINIC1
7	Cardreader
8	NC
9	NC
10	NC
11	NC
12	NC
13	NC

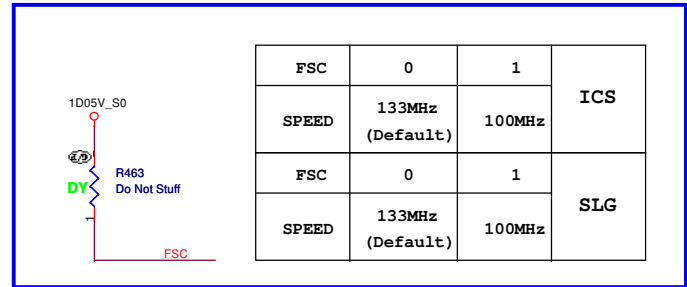
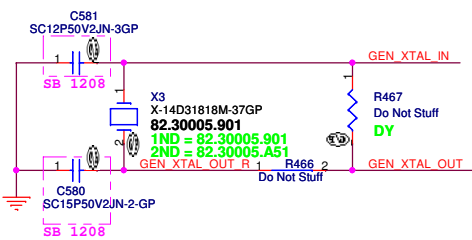
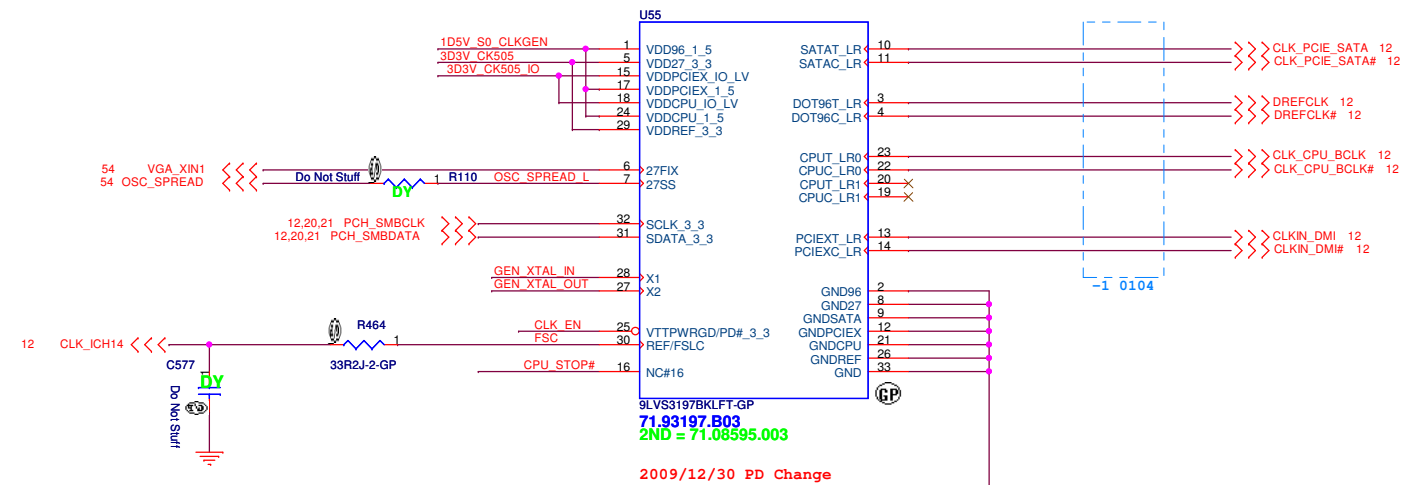
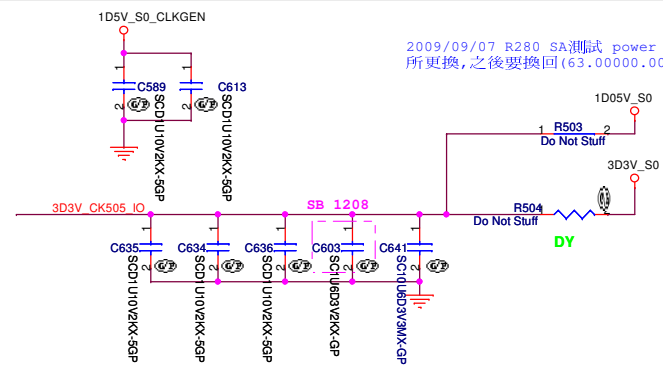
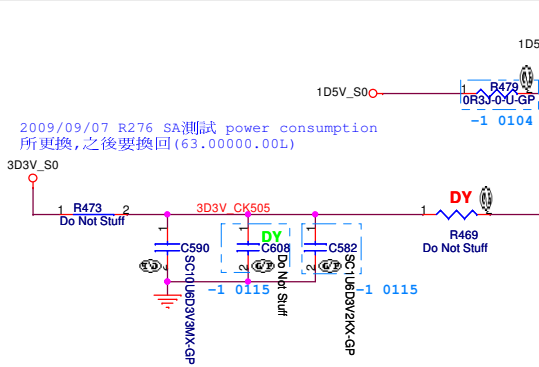
C D E

Processor Strapping

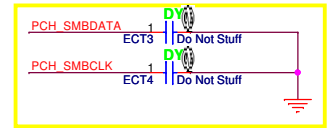
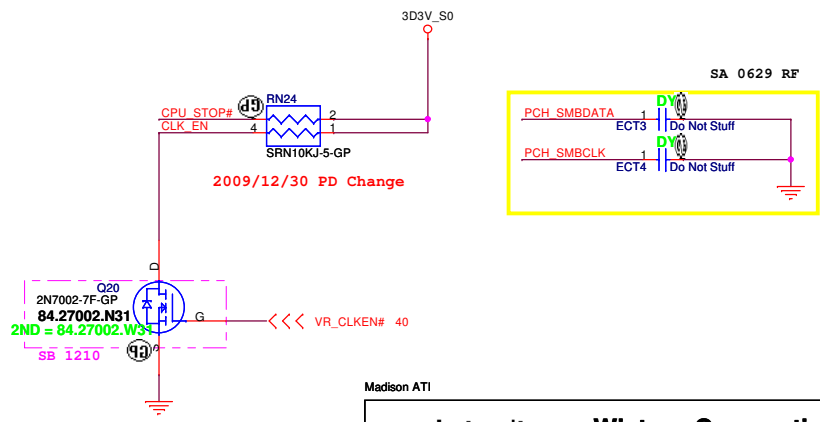
Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

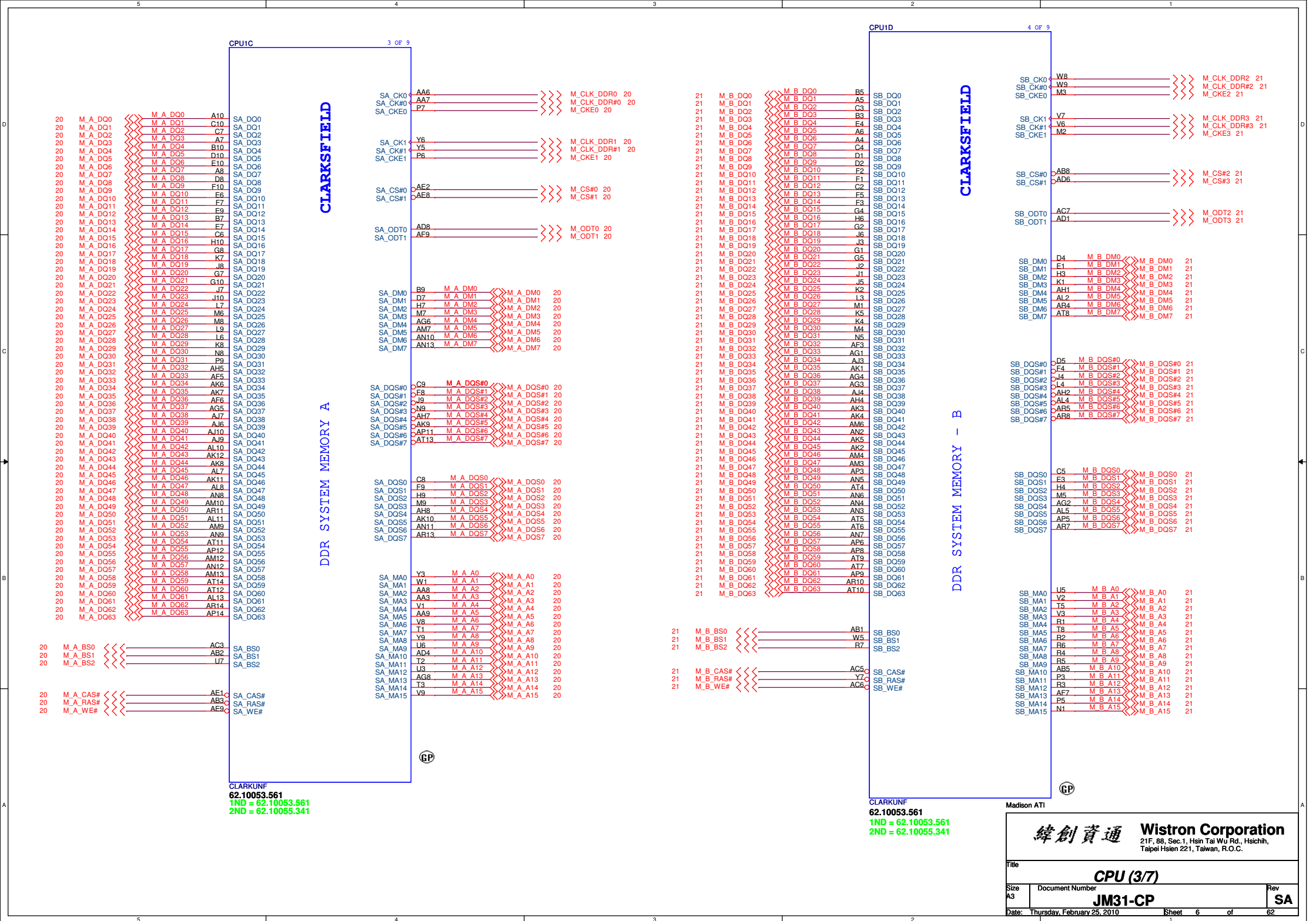
Madison ATI

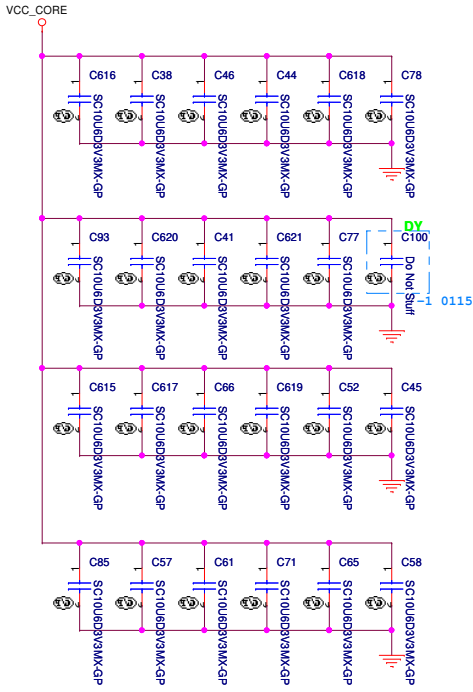
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Table of Content			
Size A3	Document Number	Rev	
JM31-CP		SA	
Date:	Thursday, February 25, 2010	Sheet	2 of 62



FSC	0	1	ICS
SPEED	133MHz (Default)	100MHz	
FSC	0	1	SLG
SPEED	133MHz (Default)	100MHz	







PROCESSOR CORE POWER

48A

VCC_CORE

- AG35 VCC
- AG34 VCC
- AG33 VCC
- AG32 VCC
- AG31 VCC
- AG30 VCC
- AG29 VCC
- AG28 VCC
- AG27 VCC
- AG26 VCC
- AF35 VCC
- AF34 VCC
- AF33 VCC
- AF32 VCC
- AF31 VCC
- AF30 VCC
- AF29 VCC
- AF28 VCC
- AF27 VCC
- AD35 VCC
- AD34 VCC
- AD33 VCC
- AD32 VCC
- AD31 VCC
- AD30 VCC
- AD29 VCC
- AD28 VCC
- AD27 VCC
- AD26 VCC
- AC35 VCC
- AC34 VCC
- AC33 VCC
- AC32 VCC
- AC31 VCC
- AC30 VCC
- AC29 VCC
- AC28 VCC
- AC27 VCC
- AC26 VCC
- AA35 VCC
- AA34 VCC
- AA33 VCC
- AA32 VCC
- AA31 VCC
- AA30 VCC
- AA29 VCC
- AA28 VCC
- AA27 VCC
- AA26 VCC
- Y35 VCC
- Y34 VCC
- Y33 VCC
- Y32 VCC
- Y31 VCC
- Y30 VCC
- Y29 VCC
- Y28 VCC
- Y27 VCC
- Y26 VCC
- V35 VCC
- V34 VCC
- V33 VCC
- V32 VCC
- V31 VCC
- V30 VCC
- V29 VCC
- V28 VCC
- V27 VCC
- V26 VCC
- U35 VCC
- U34 VCC
- U33 VCC
- U32 VCC
- U31 VCC
- U30 VCC
- U29 VCC
- U28 VCC
- U27 VCC
- U26 VCC
- R35 VCC
- R34 VCC
- R33 VCC
- R32 VCC
- R31 VCC
- R30 VCC
- P29 VCC
- P28 VCC
- P27 VCC
- P26 VCC

CLARKSFIELD

1.1V RAIL POWER

CPU CORE SUPPLY

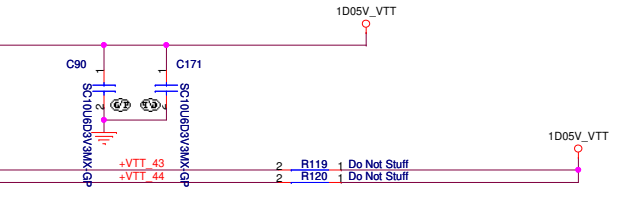
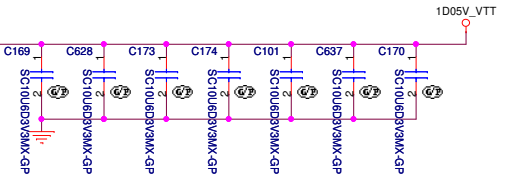
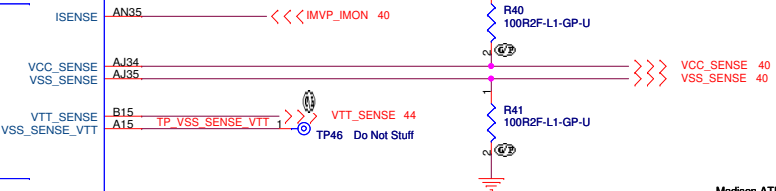
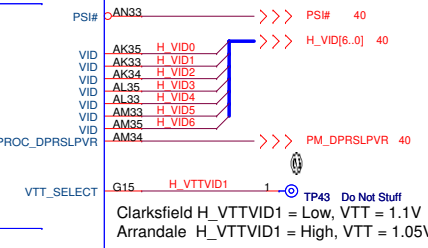
POWER

CPD VIDS

SENSE SENSE

- VTT0 AH14
- VTT0 AH12
- VTT0 AH11
- VTT0 AH10
- VTT0 J14
- VTT0 H14
- VTT0 H12
- VTT0 G14
- VTT0 G13
- VTT0 G11
- VTT0 F14
- VTT0 F13
- VTT0 F12
- VTT0 E11
- VTT0 E12
- VTT0 D14
- VTT0 D12
- VTT0 D11
- VTT0 C14
- VTT0 C13
- VTT0 C12
- VTT0 C11
- VTT0 B14
- VTT0 B12
- VTT0 A14
- VTT0 A13
- VTT0 A12
- VTT0 A11

- VTT0 AF10
- VTT0 AE10
- VTT0 AC10
- VTT0 AB10
- VTT0 Y10
- VTT0 W10
- VTT0 U10
- VTT0 T10
- VTT0 J12
- VTT0 J11
- VTT0 J16
- VTT0 J15



The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarkfield VTT=1.1V

CLARKUNF
62.10053.561
1ND = 62.10053.561
2ND = 62.10055.341

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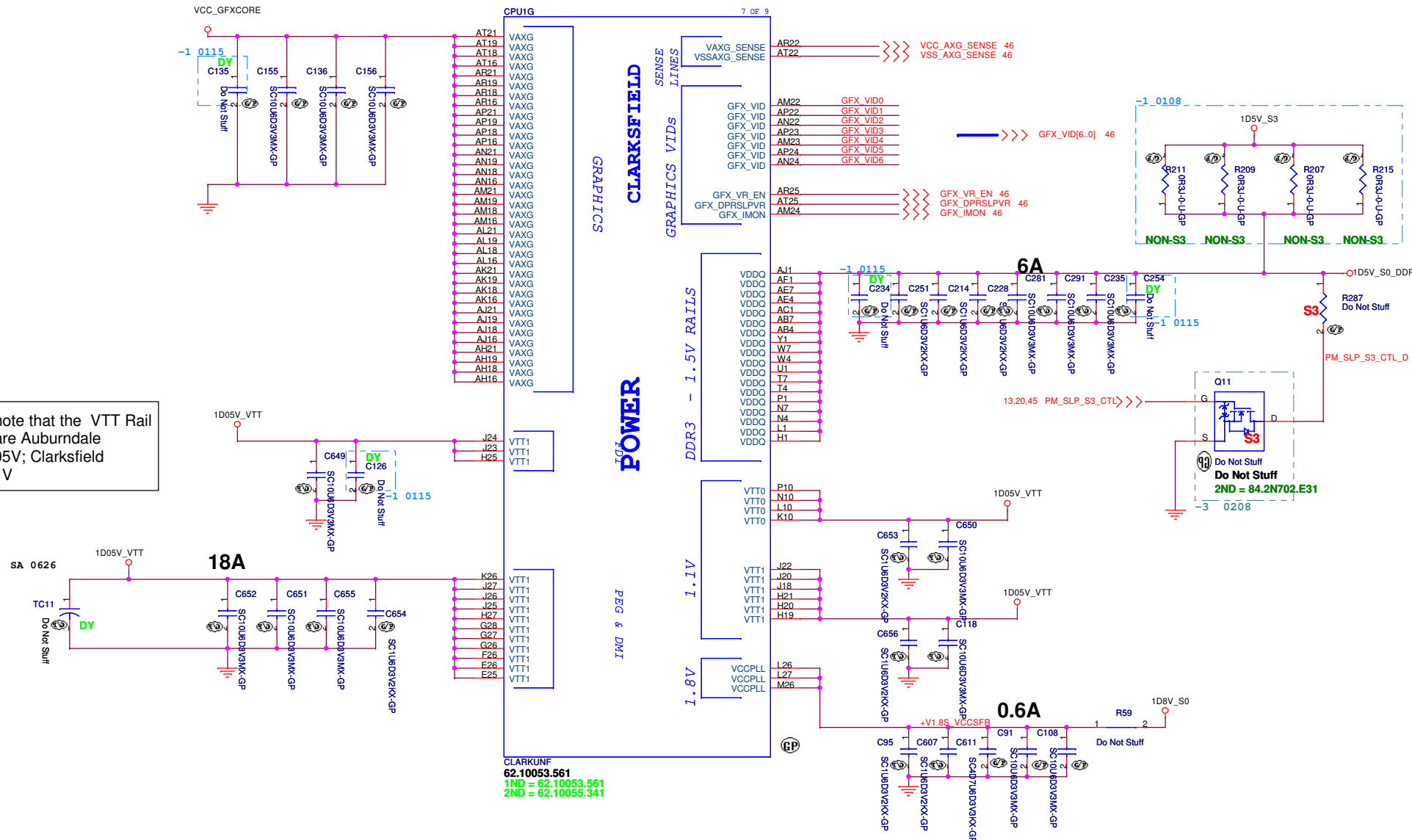
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Title: **CPU (4/7)**

Size: Document Number **JM31-CP** Rev: **SA**

Date: Thursday, February 25, 2010 Sheet 7 of 62

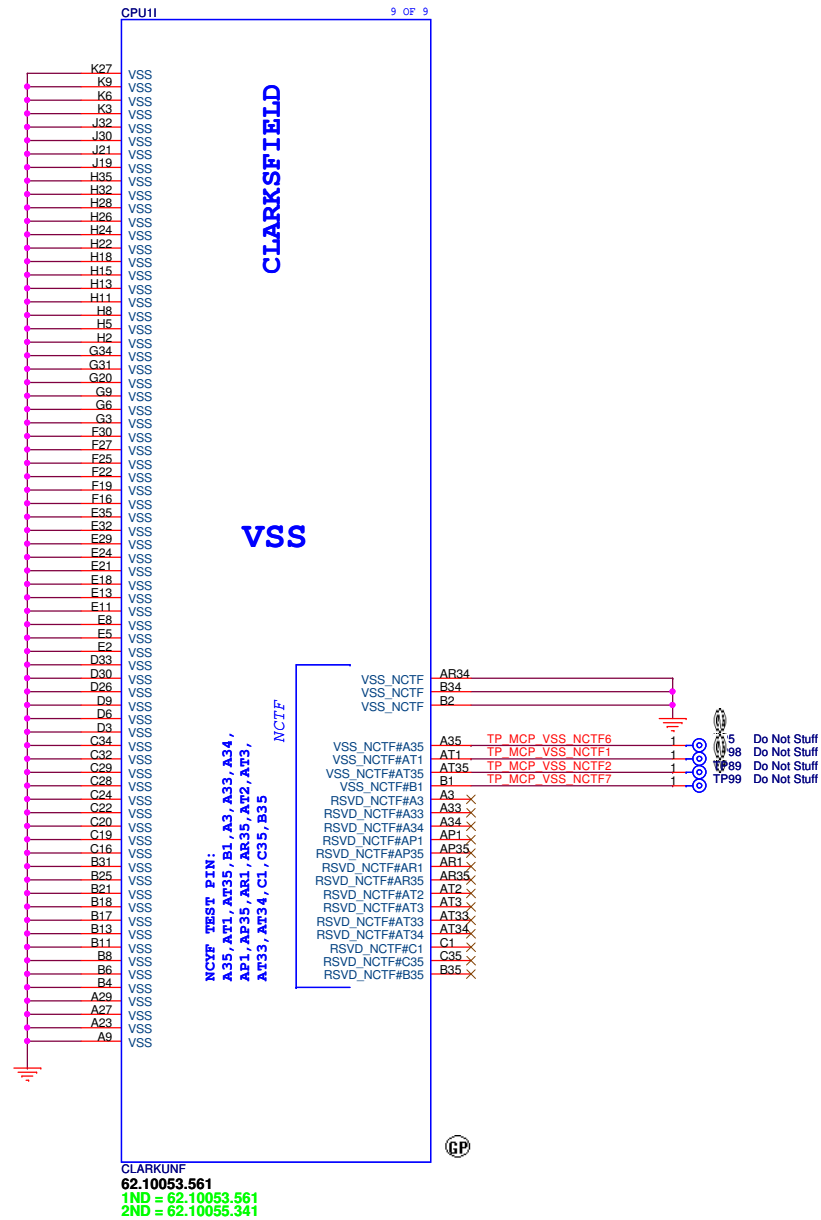
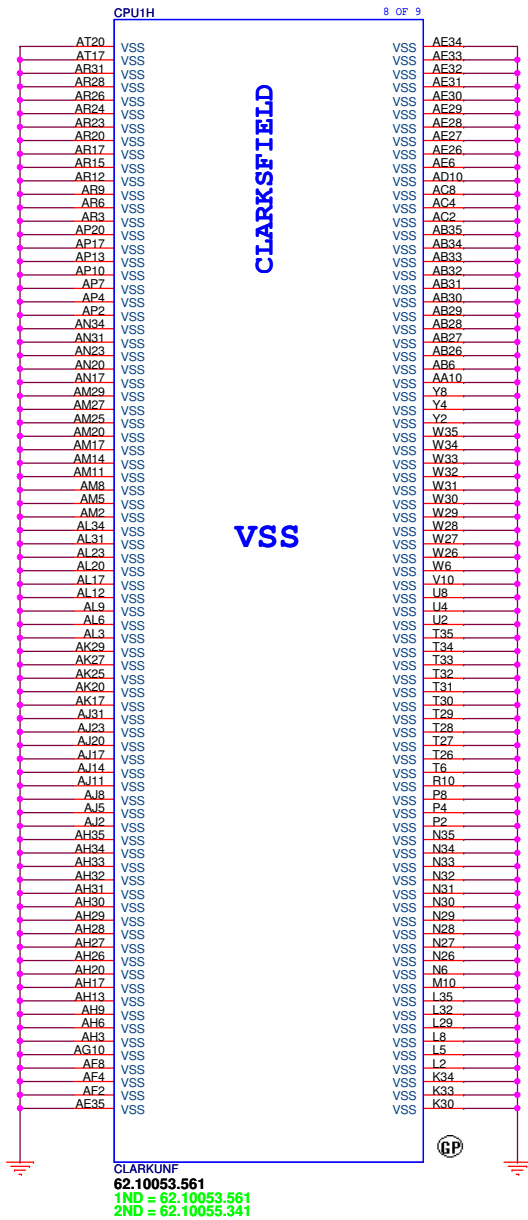
Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V



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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

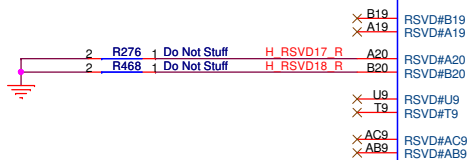
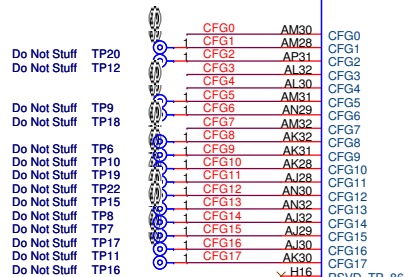
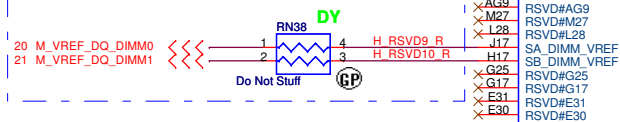
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Size	Document Number	Rev	
A3	JM31-CP	-3	
Date:	Thursday, February 25, 2010	Sheet	8 of 62



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Title			
CPU (6/7)			
Size	Document Number	Rev	
A3	JM31-CP	SA	
Date:	Thursday, February 25, 2010	Sheet	9 of 62

SO-DIMM VREFDQ (M3) Circuit for Clarkfield Processor



CPU1E

CLARKFIELD

RESERVED

CLARKUNF

62.10053.561
1ND = 62.10053.561
2ND = 62.10055.341

RSVD#AJ13
RSVD#AJ12

RSVD#AH25
RSVD#AK26
RSVD#AL26
RSVD_NCTF_37
RSVD#AJ26
RSVD#AJ27

RSVD#AL28
RSVD#AL29
RSVD#AP30
RSVD#AP32
RSVD#AL27
RSVD#AT31
RSVD#AT32
RSVD#AP33
RSVD#AR33

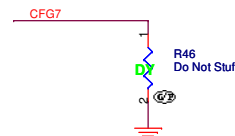
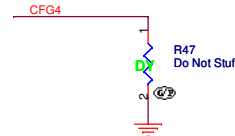
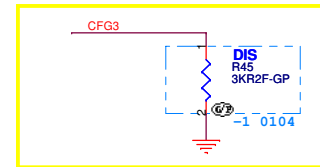
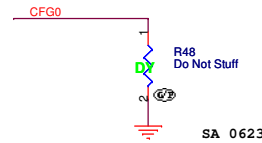
RSVD#AR32
RSVD_TP#E15
RSVD_TP#F15
KEY
RSVD#D15
RSVD#C15
RSVD#AJ15
RSVD#AH15

SA_CK2
SA_CK#2
SA_CKE2
SA_CS#2
SA_ODT2
SA_CK3
SA_CK#3
SA_CKE3
SA_CS#3
SA_ODT3

SB_CK2
SB_CK#2
SB_CKE2
SB_CS#2
SB_ODT2
SB_CK3
SB_CK#3
SB_CKE3
SB_CS#3
SB_ODT3

VSS AP34 RSVD VSS 2 R39 1 Do Not Stuff

VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.



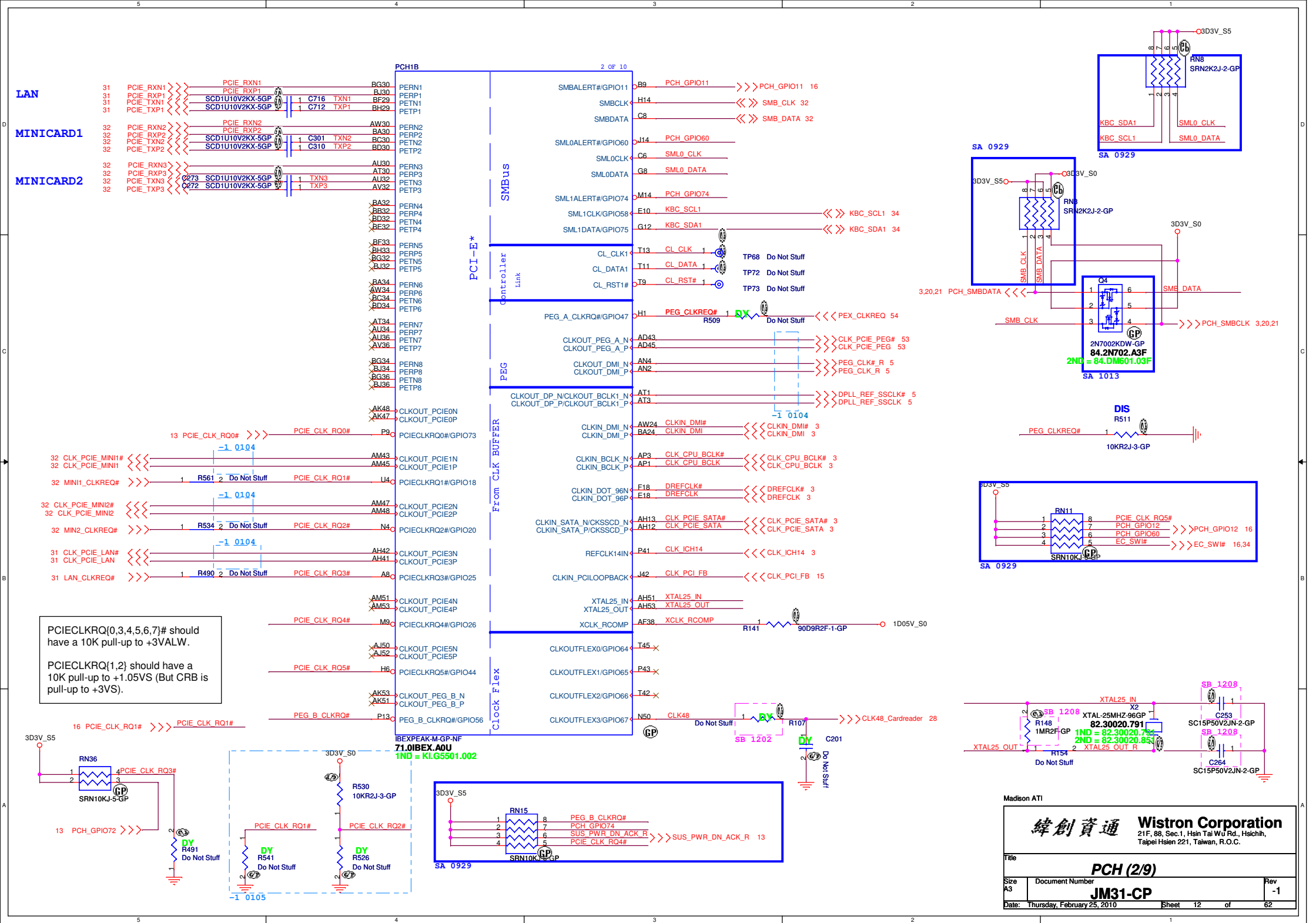
PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

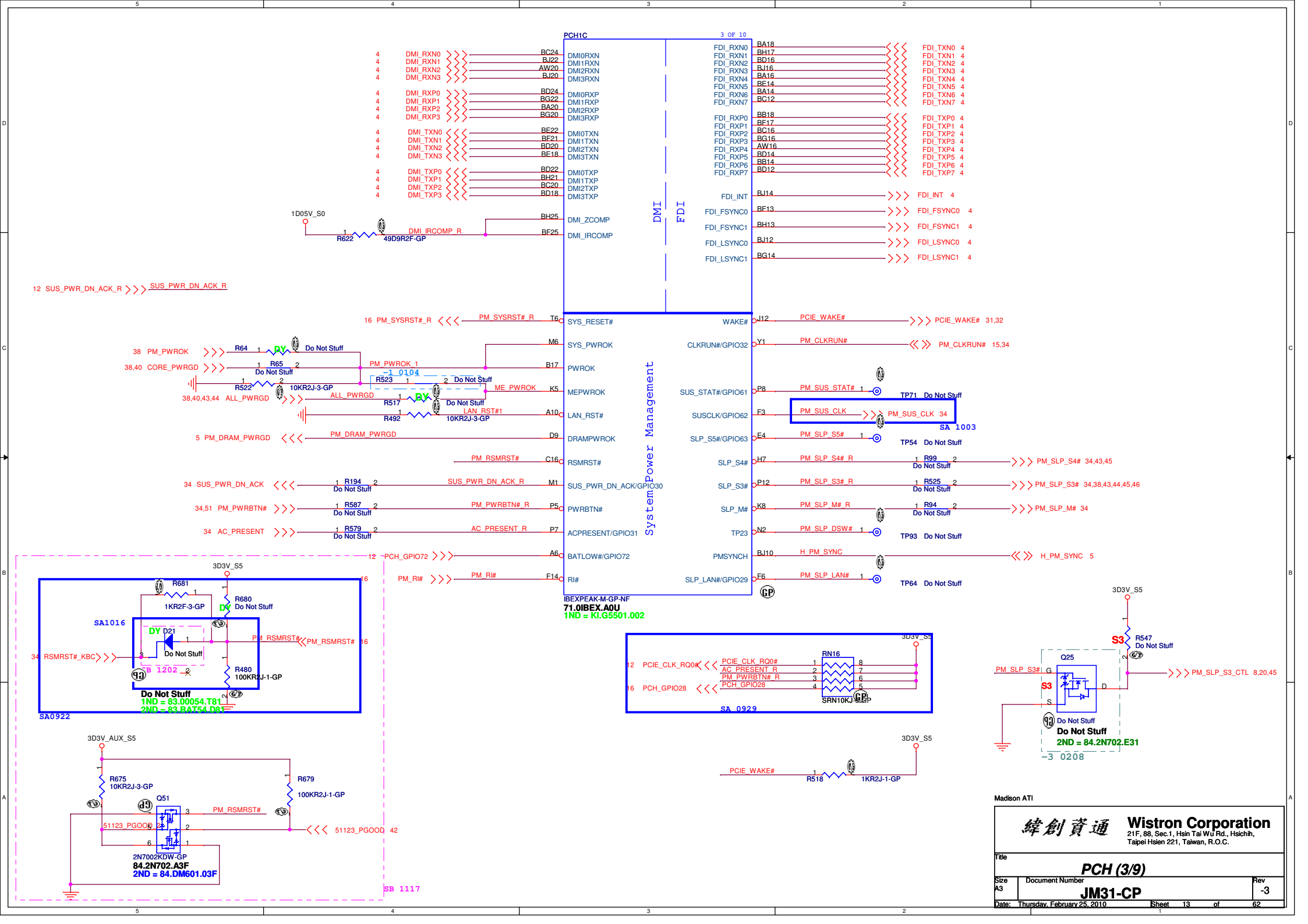
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

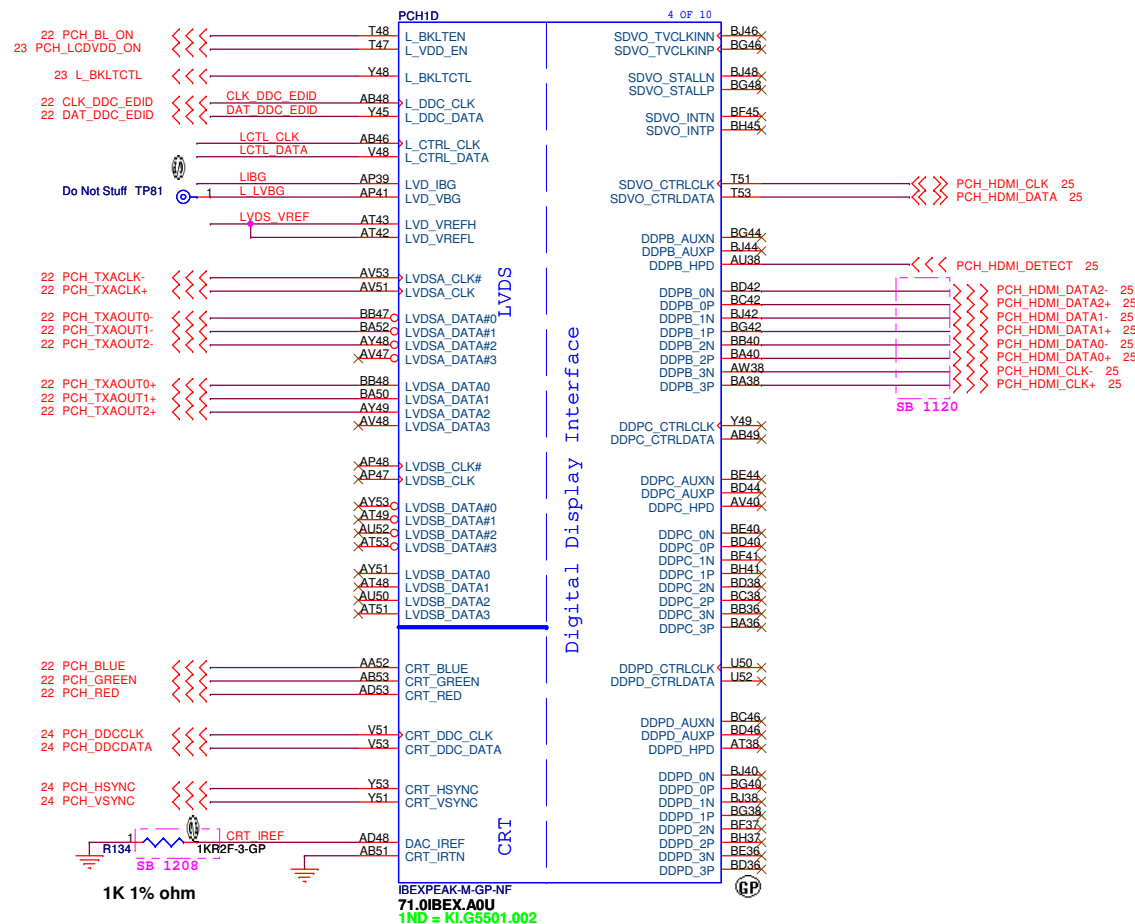
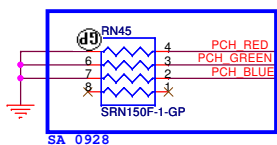
CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarkfield samples.	
CFG7	Clarkfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.

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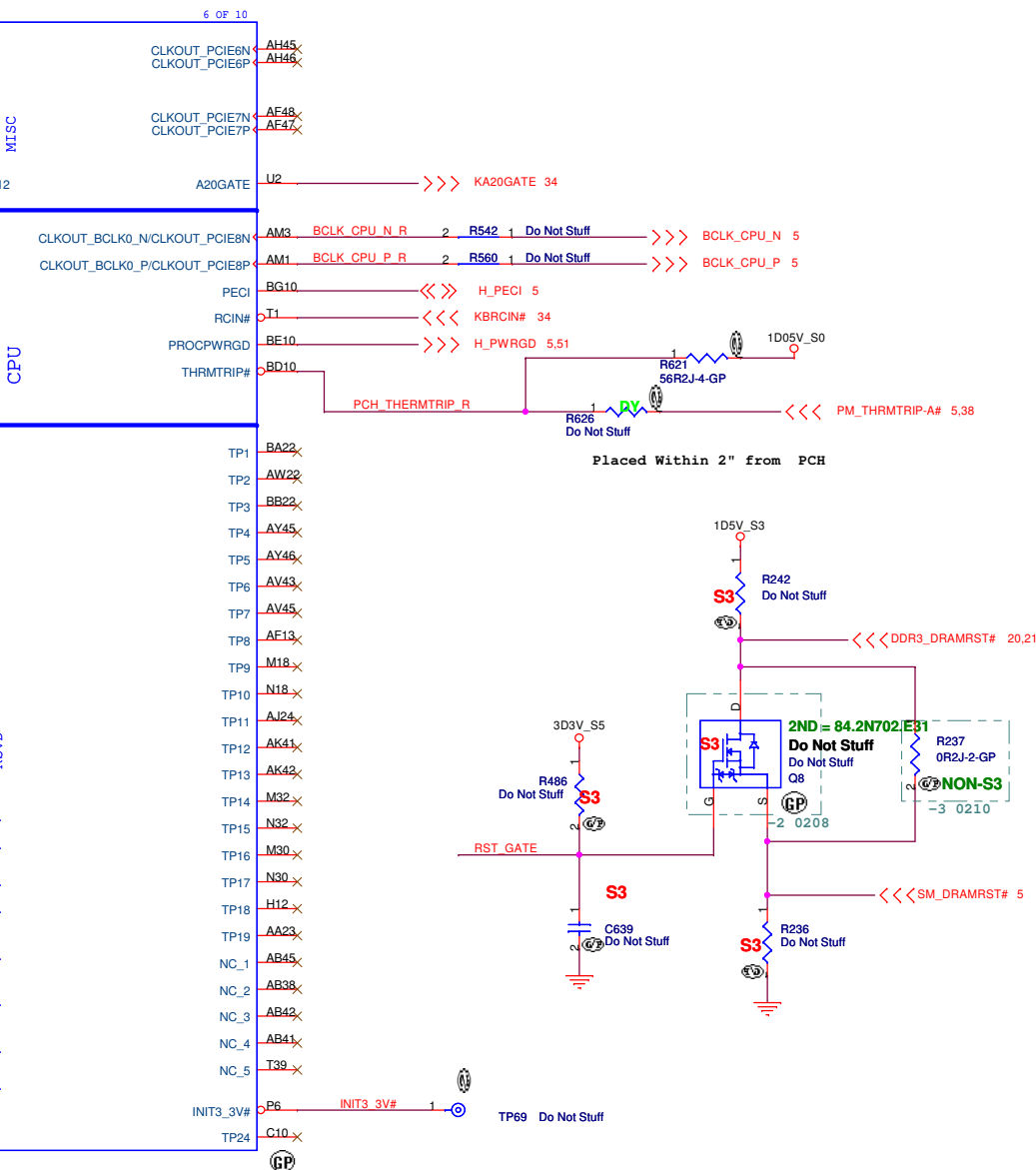
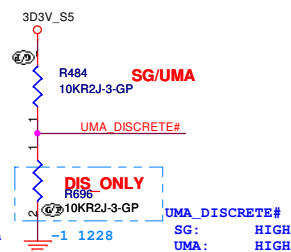
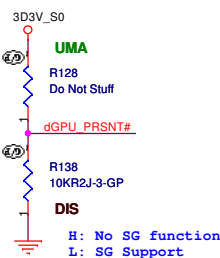
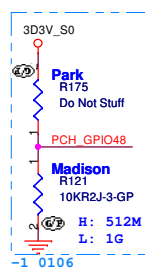


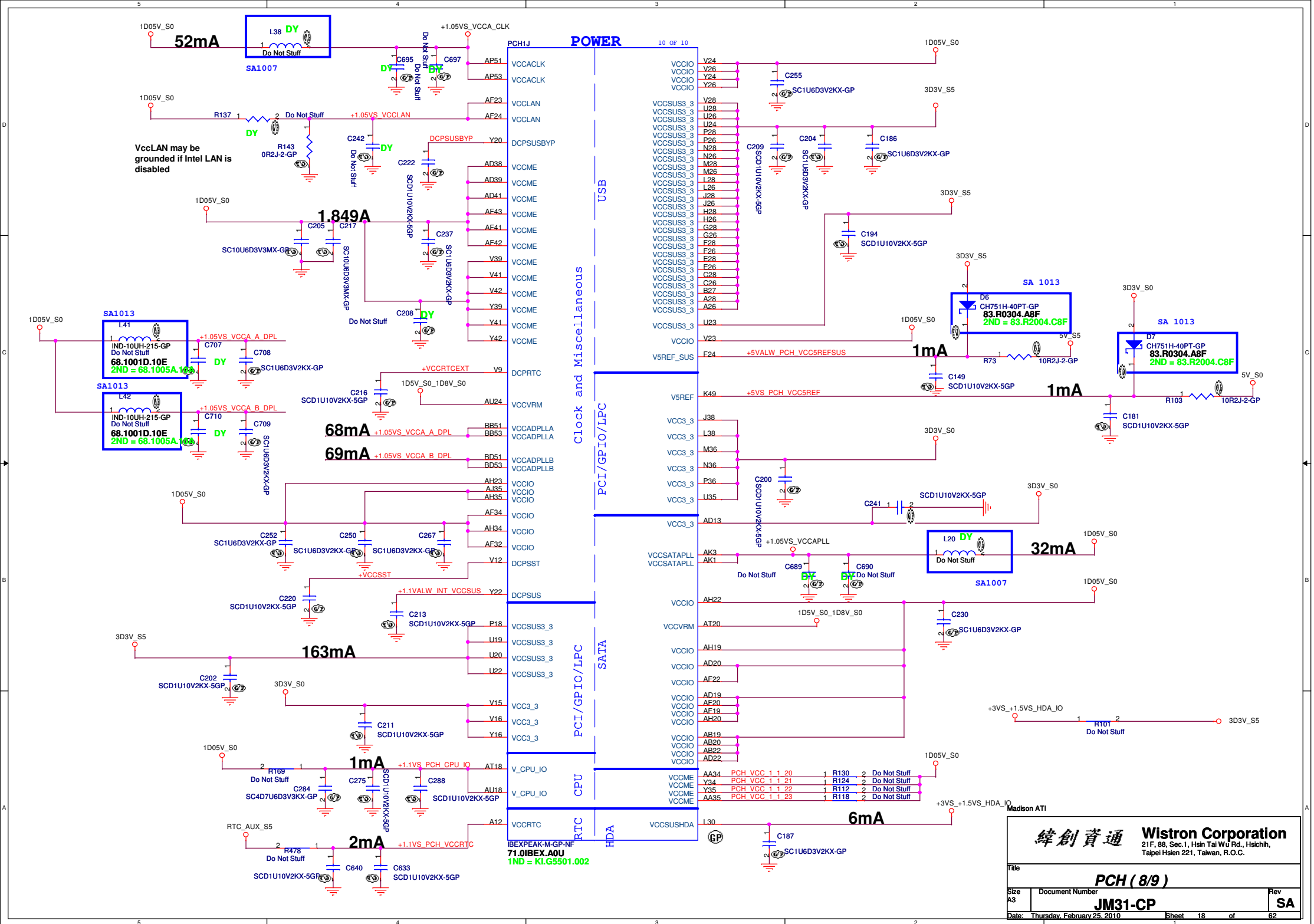


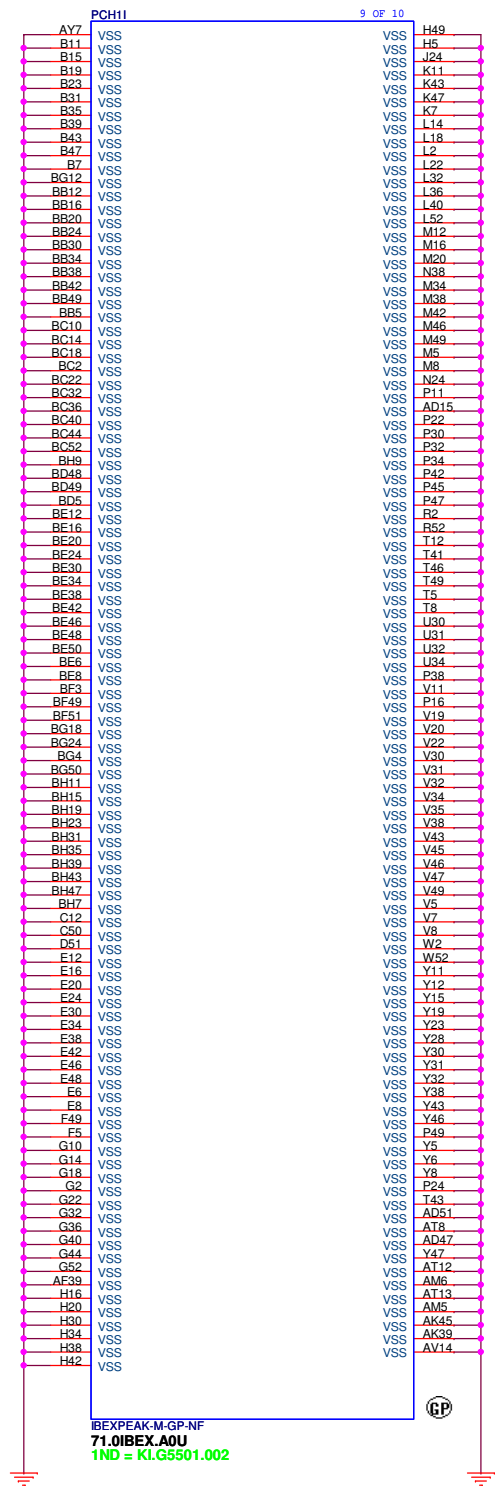
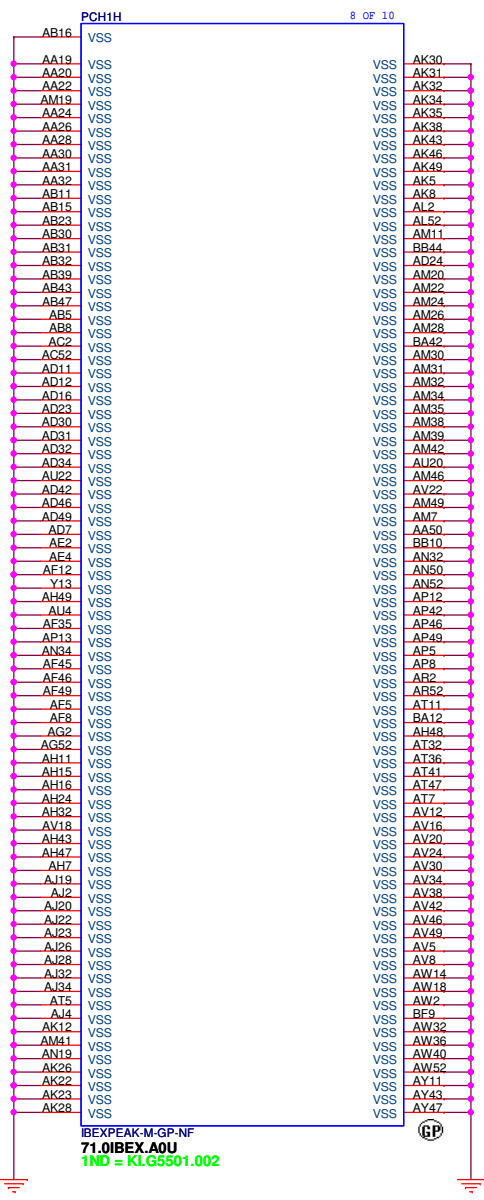


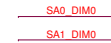
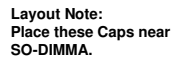
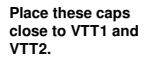
62

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regulator,
should not place external pull down.



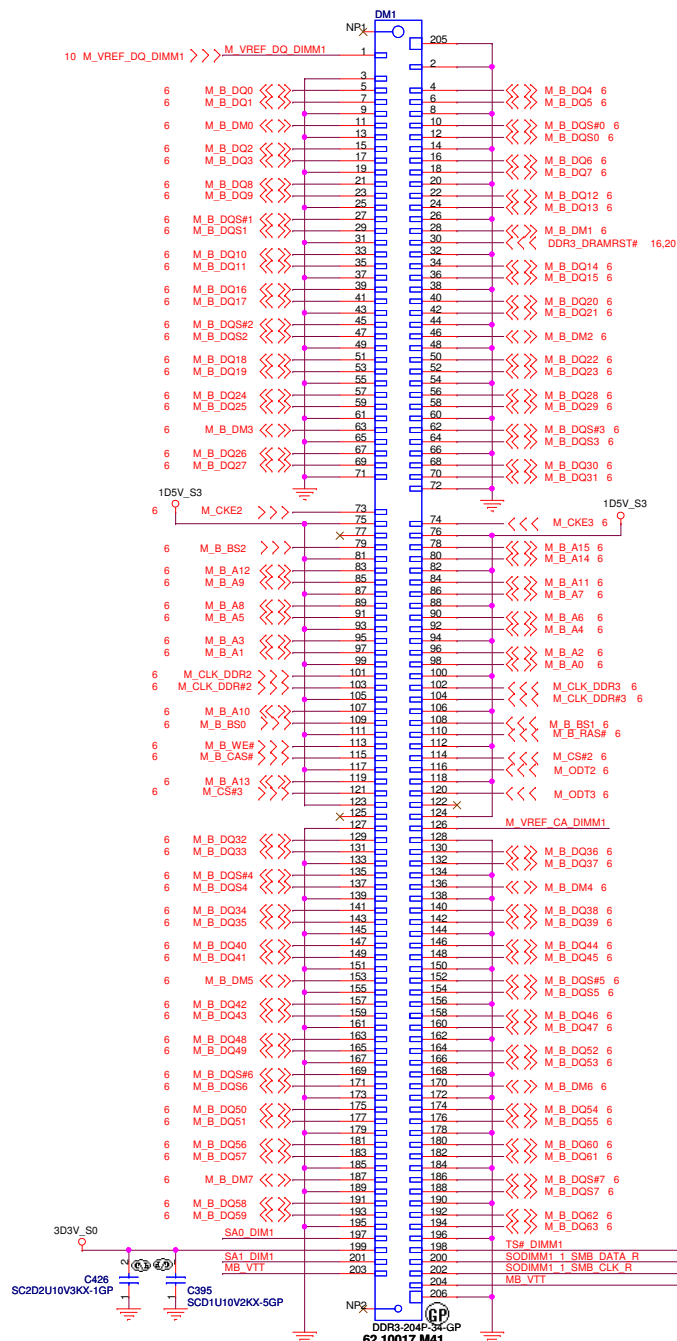
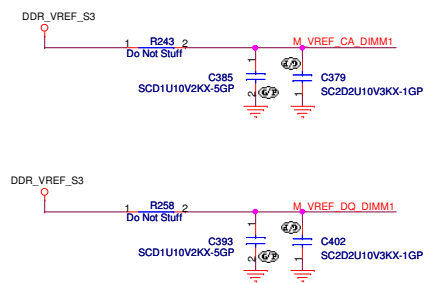






If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA SPD Address is 0xA2

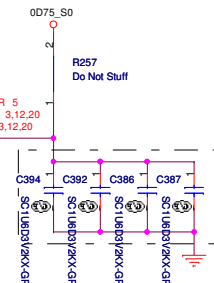
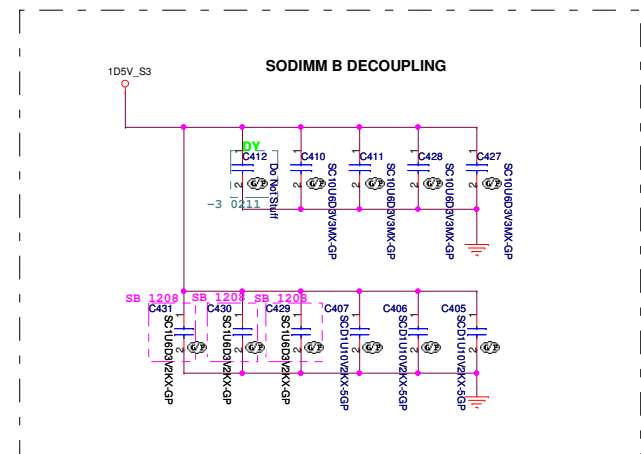
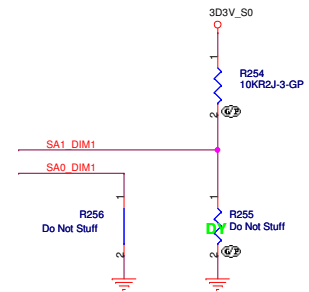


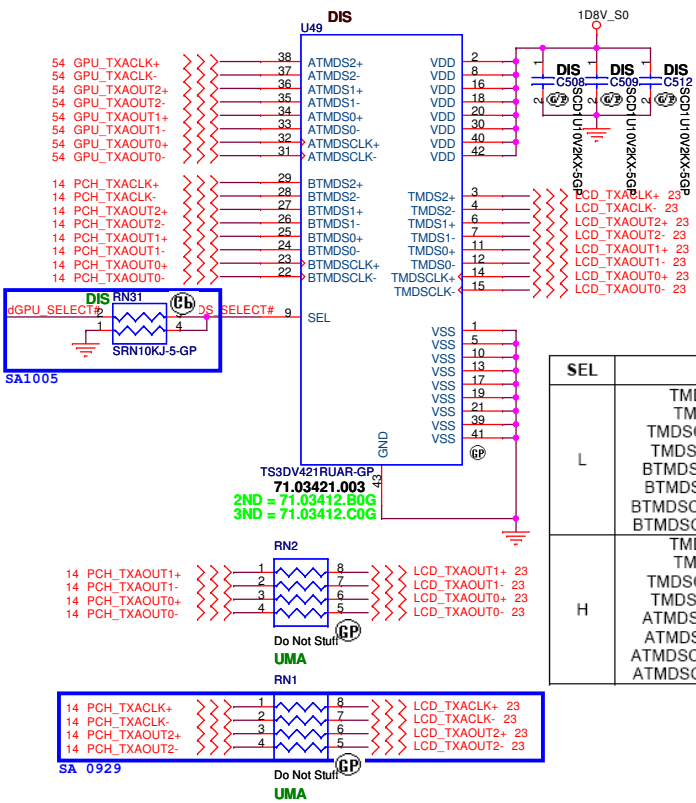


Note:
SO-DIMMB SPD Address is 0xA
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

Place these caps close to VTT1 and VTT2.





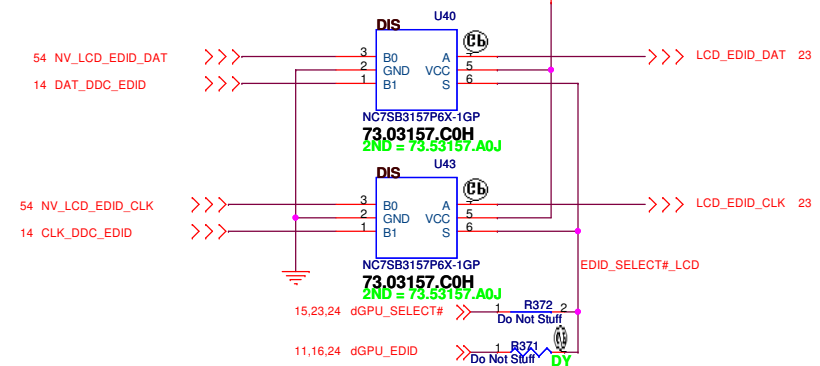
FUNCTION TABLE

SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDCLK+ = ATMDCLK+ TMDCLK- = ATMDCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDCLK+ = High Impedance BTMDCLK- = High Impedance	TMDSn+ TMDSn- TMDCLK+ TMDCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDCLK+ = BTMDCLK+ TMDCLK- = BTMDCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDCLK+ = High Impedance ATMDCLK- = High Impedance	TMDSn+ TMDSn- TMDCLK+ TMDCLK-

Function Table

Input (S)	Function
L	B ₀ Connected to A
H	B ₁ Connected to A

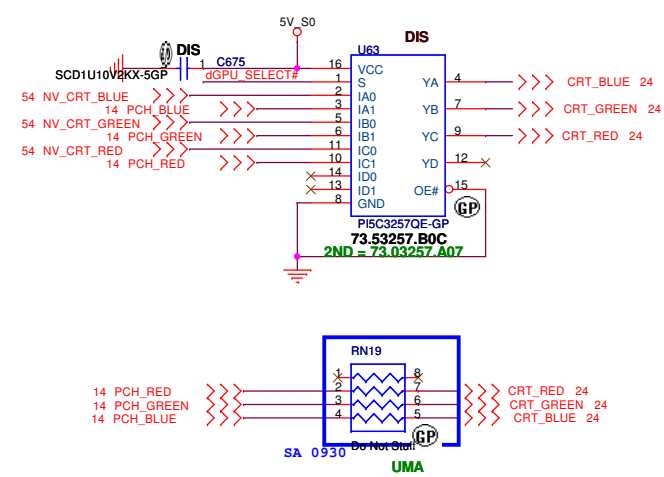
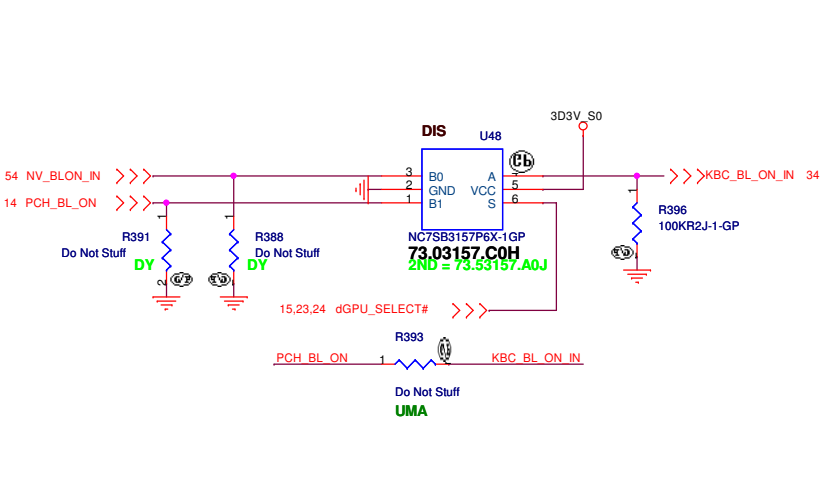
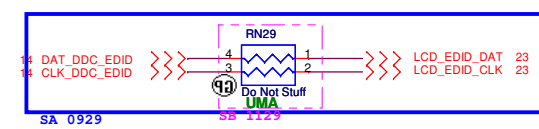
H = HIGH Logic Level L = LOW Logic Level



Function Table

Input (S)	Function
L	B ₀ Connected to A
H	B ₁ Connected to A

H = HIGH Logic Level L = LOW Logic Level



\bar{E}	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

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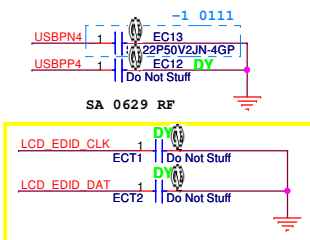
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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **PX SWITCH**

Size: A3 Document Number: **JM31-CP** Rev: **SB**

Date: Thursday, February 25, 2010 Sheet: 22 of 62

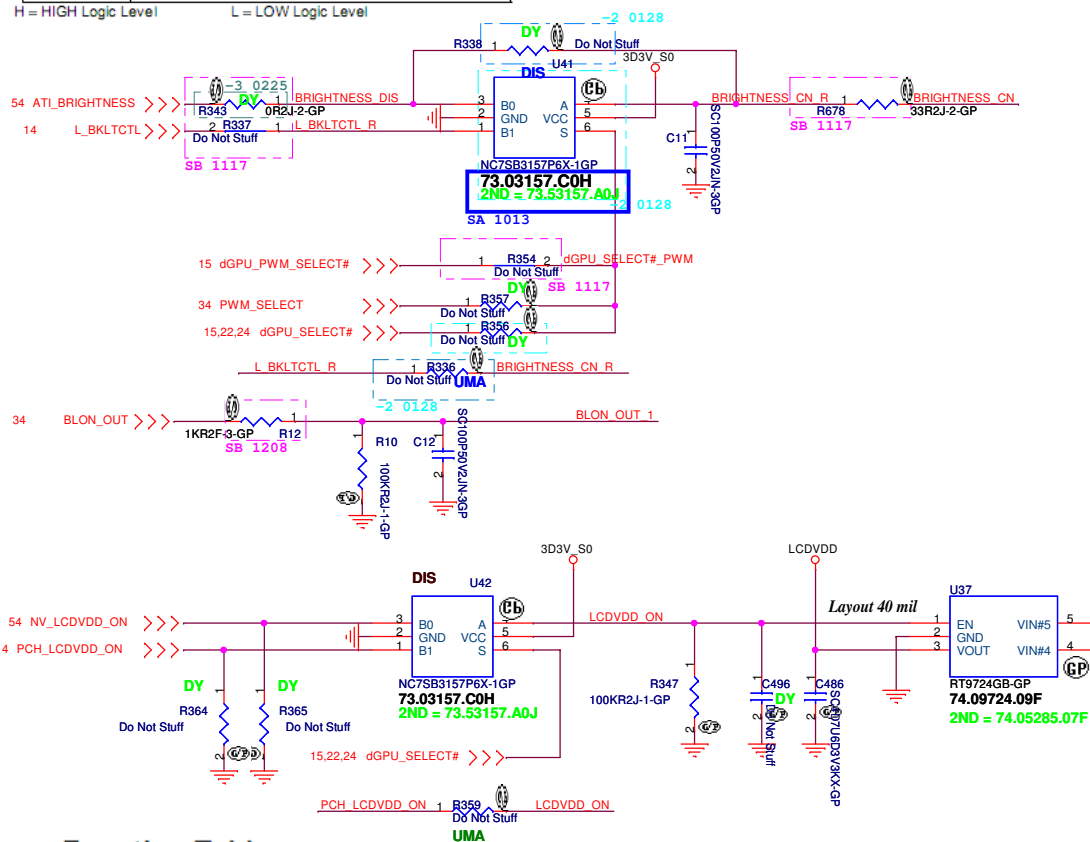
LCD/INVERTER/CCD CONN



Function Table

Input (S)	Function
L	B ₀ Connected to A
H	B ₁ Connected to A

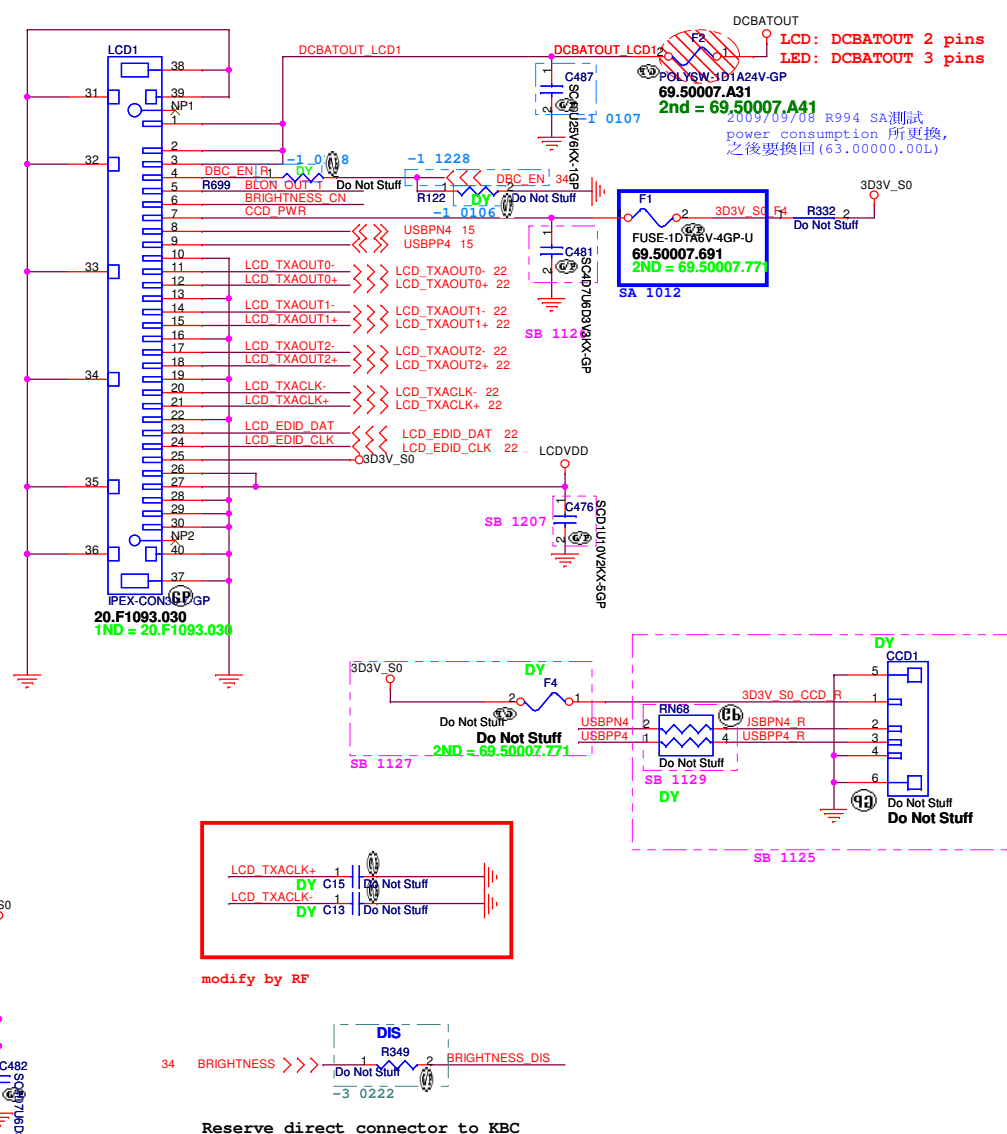
H = HIGH Logic Level L = LOW Logic Level



Function Table

Input (S)	Function
L	B ₀ Connected to A
H	B ₁ Connected to A

H = HIGH Logic Level L = LOW Logic Level

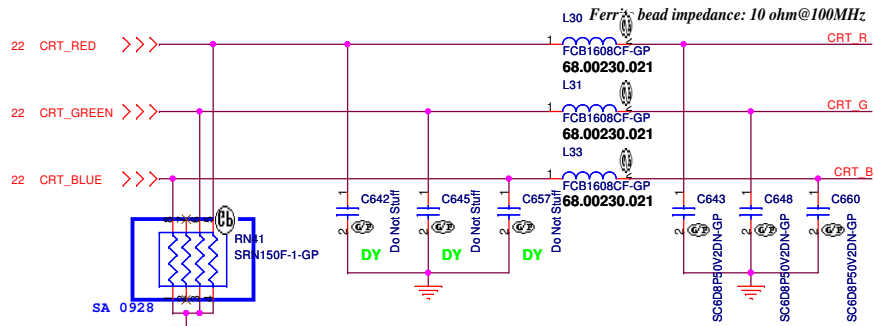


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LCD CONN		
Size A3	Document Number	Rev -1
JM31-CP		
Date: Thursday, February 25, 2010	Sheet 23	of 62

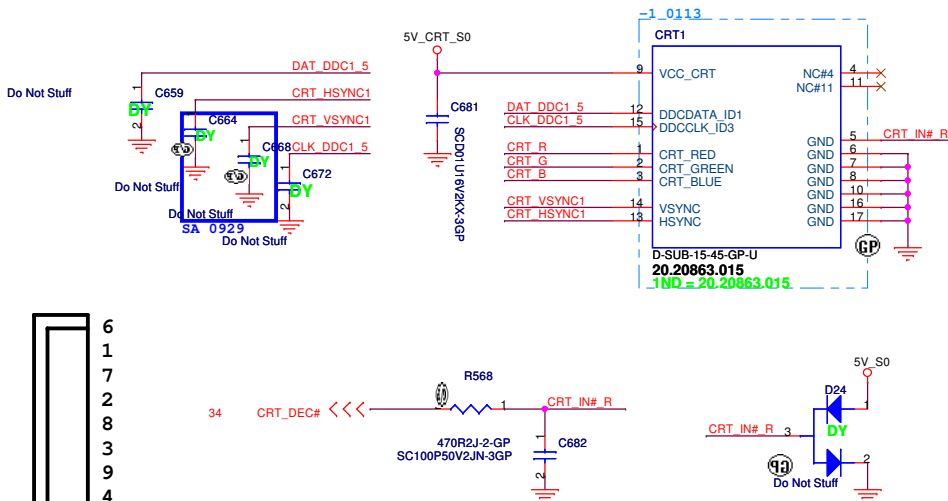
Layout Notes:
Place these resistors
close to the CRT-out
connector



Layout Note:

* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

CRT I/F & CONNECTOR



L=>B0 -DIS
H=>B1 -UMA

15,22,23 dGPU_SELECT#

For DIS CRT

54,57 NV_CRT_HSYNC

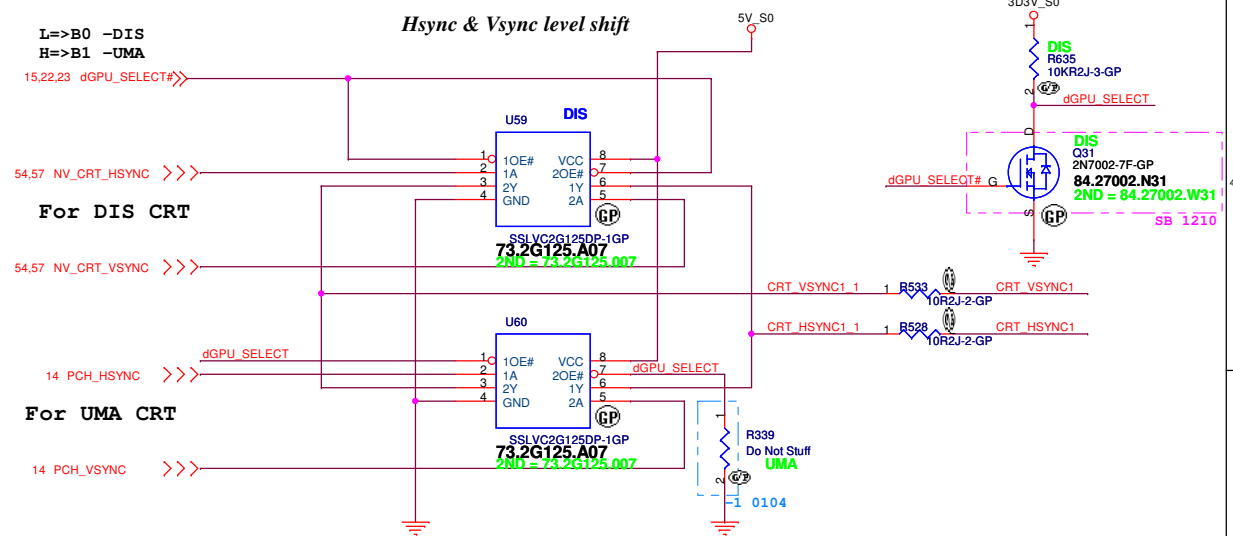
54,57 NV_CRT_VSYNC

For UMA CRT

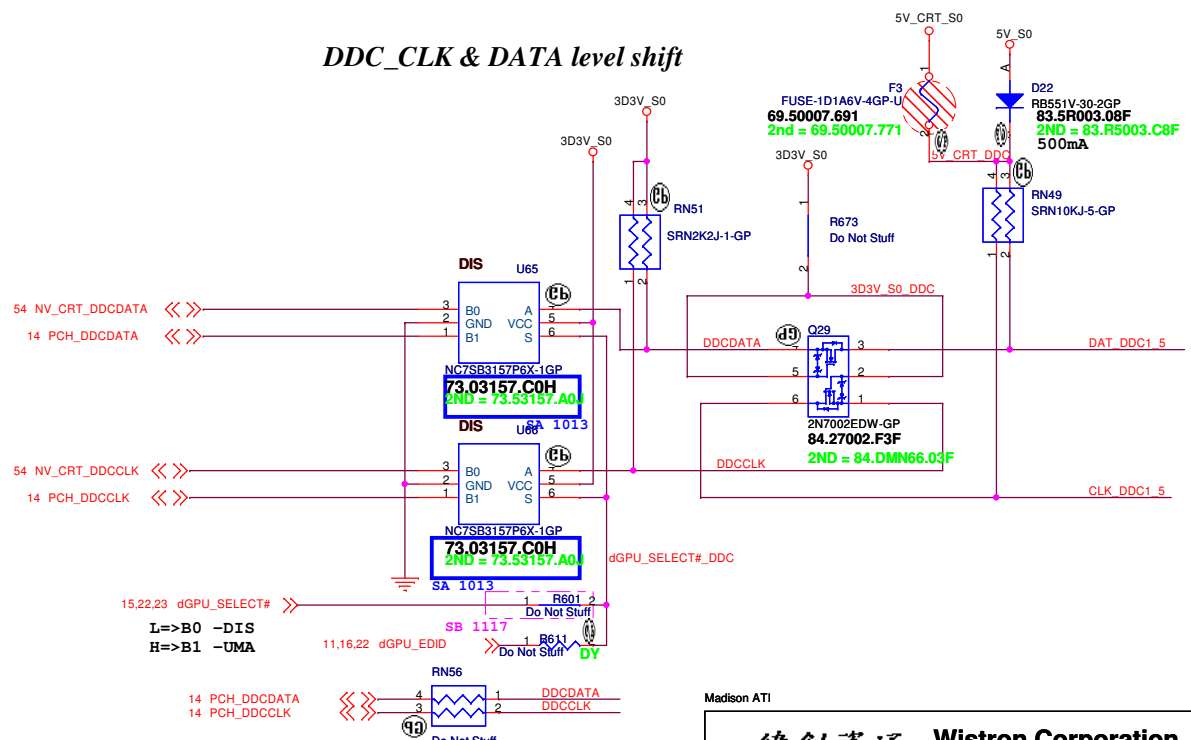
14 PCH_HSYNC

14 PCH_VSYNC

Hsync & Vsync level shift



DDC_CLK & DATA level shift



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Title

CRT CONN

Size

Document Number

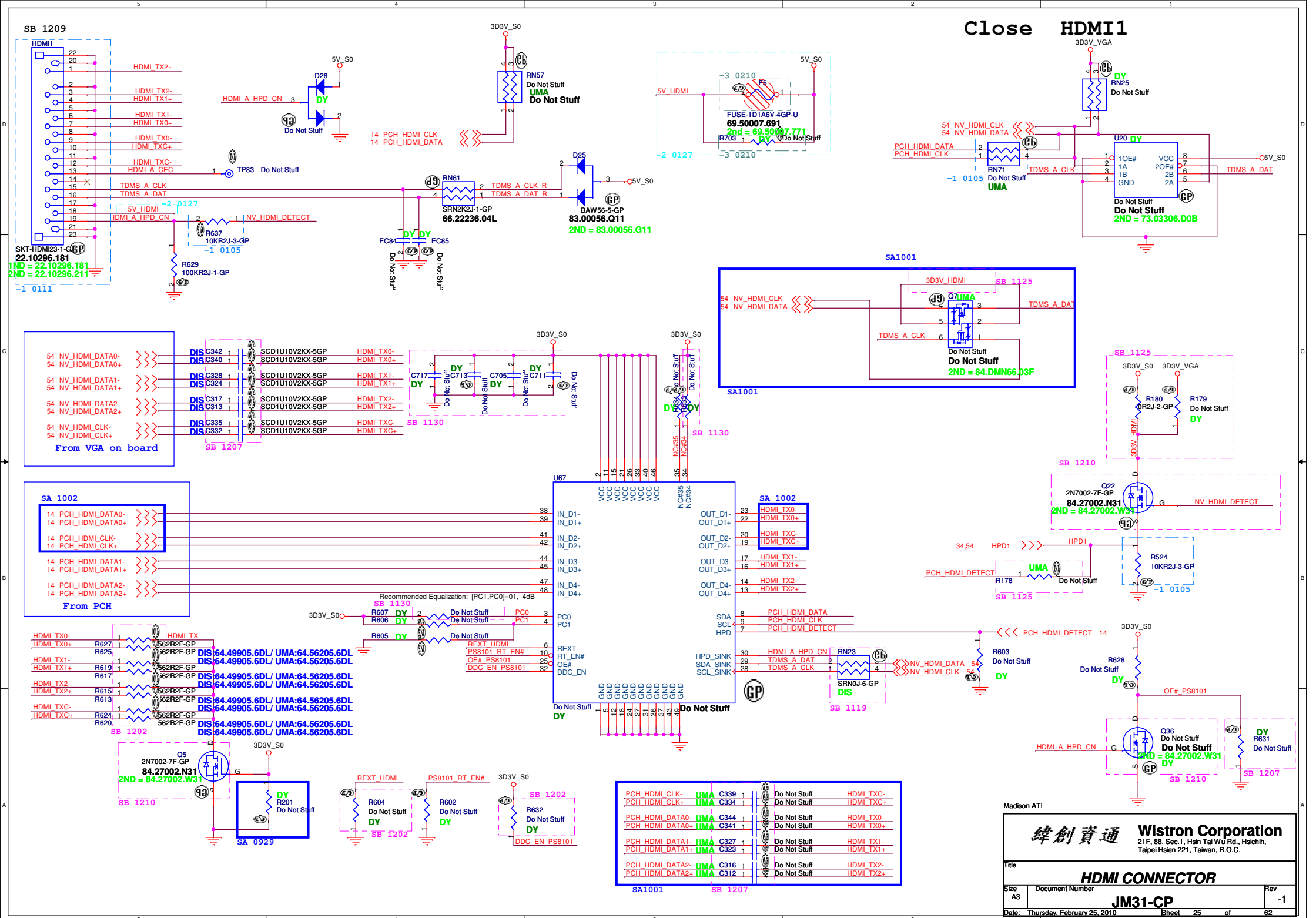
JM31-CP

Rev

SB

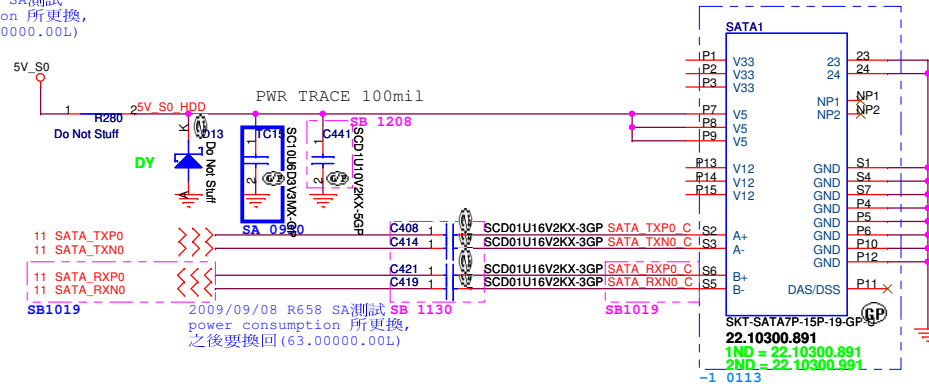
Date: Thursday, February 25, 2010

Sheet 24 of 62



SATA Connector

2009/09/08 R658 SA測試
power consumption 所更換,
之後要換回(63.00000.00L)



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Title	Author	Year	Journal	Volume	Page
...

HDD CONNSize
A3

Document Number

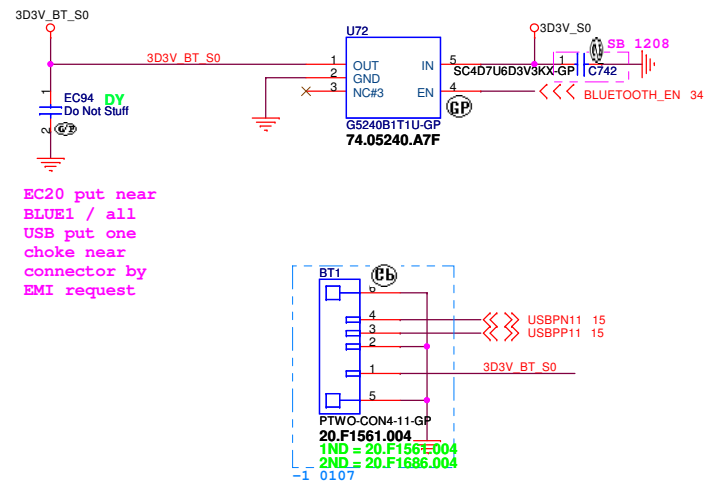
JM31-CP

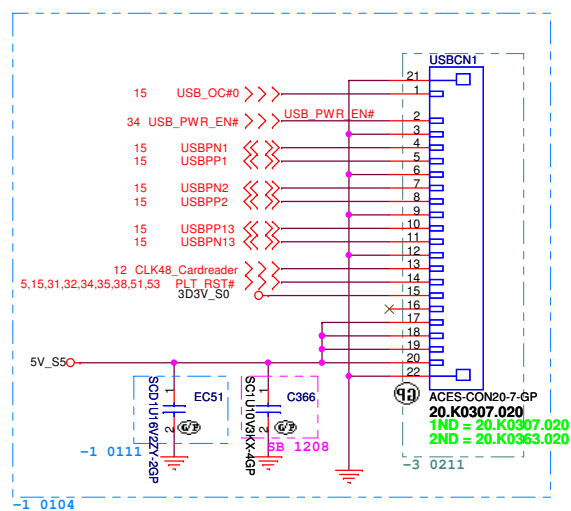
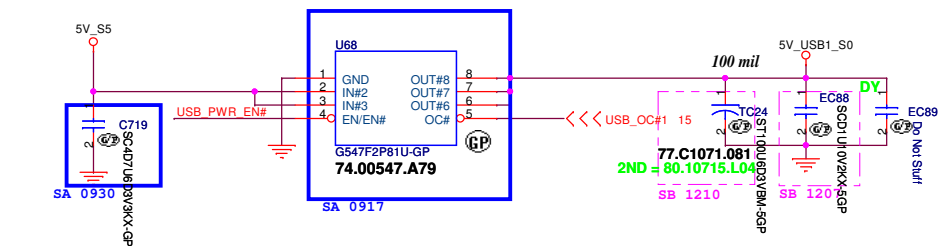
Rev	-1
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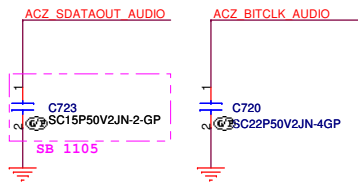
Date: Thursday, February 25, 2010

Sheet 26 of 62

BLUETOOTH MODULE

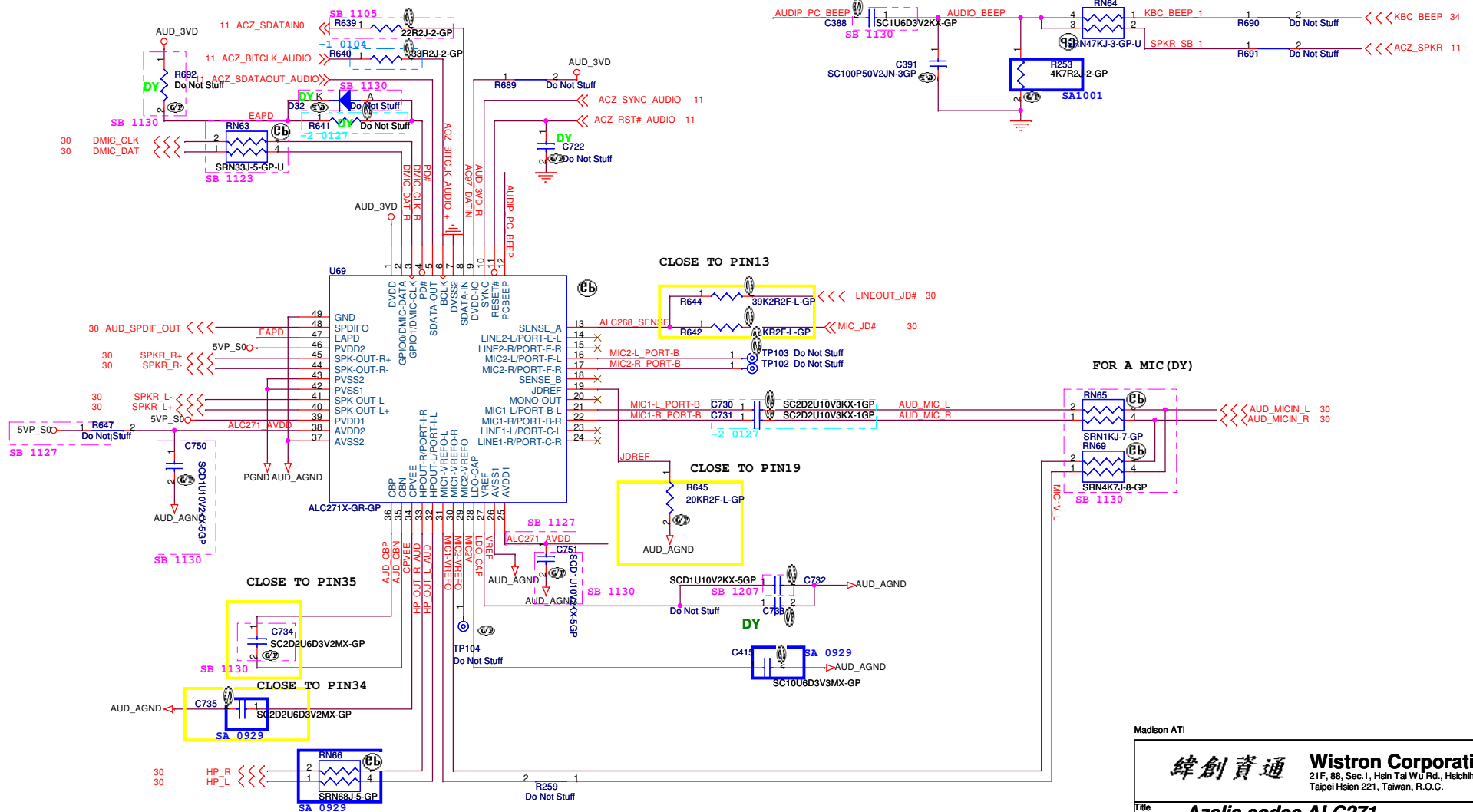
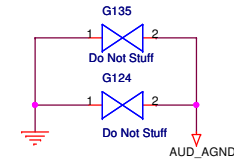
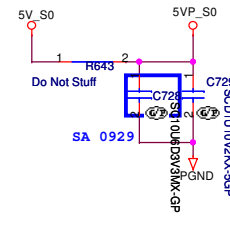
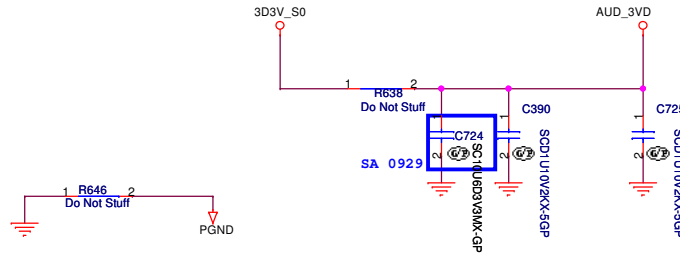






2009/09/14 R296 SA測試 power consumption
所更換,之後要換回(63.00000.00L)

2009/09/16 R296 SA測試 power consumption
所更換,之後要換回(63.00000.00L)



Madison ATI

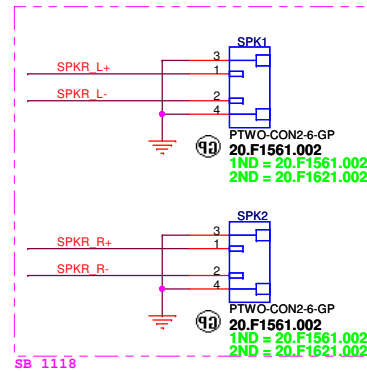
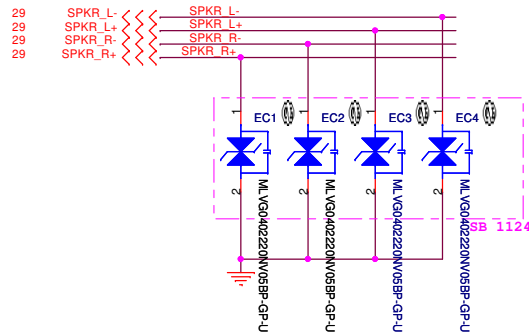
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Taipei Hsien 221, Taiwan, R.O.C.

Title Azalia codec ALC271

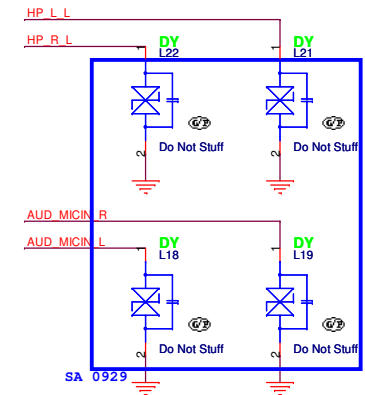
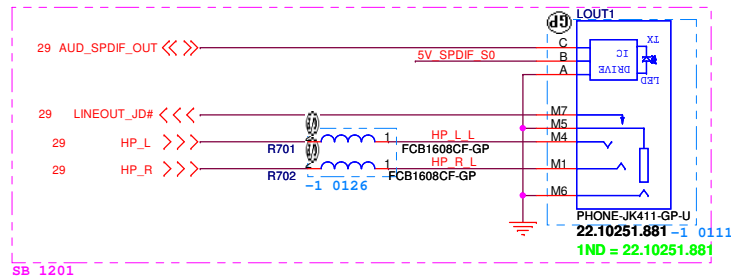
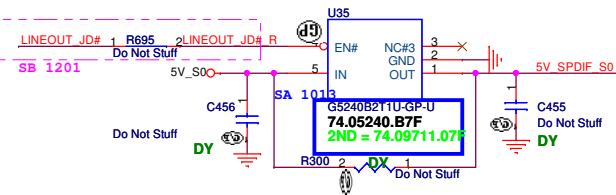
Size A3 Document Number JM31-CP Rev SB

Date: Thursday, February 25, 2010 Sheet 29 of 62

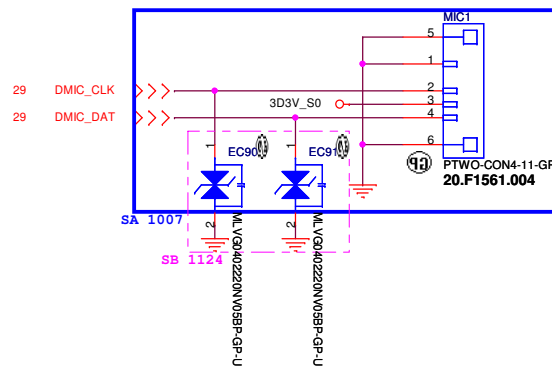
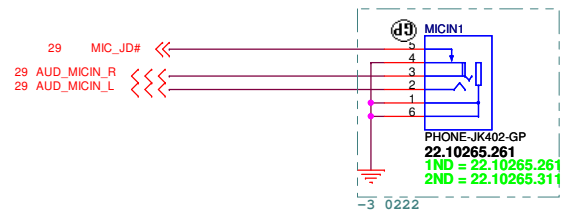
Internal Speaker



LINE OUT



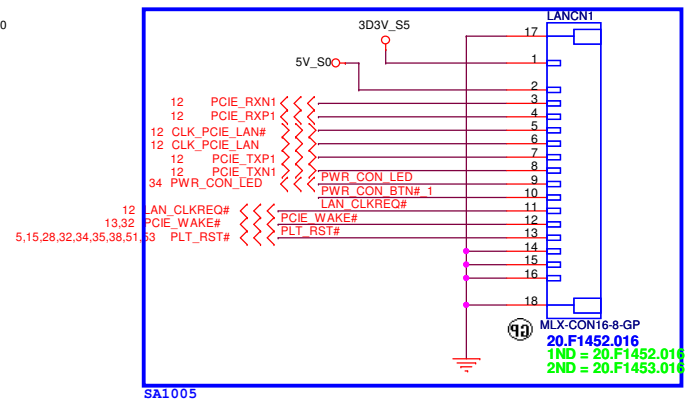
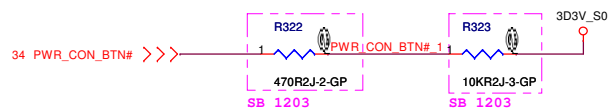
MIC IN



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Title		
AUDIO jack		
Size	Document Number	Rev
A3	JM31-CP	-1
Date:	Thursday, February 25, 2010	Sheet 30 of 62



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Title

LAN CONN

Size
A3

Document Number

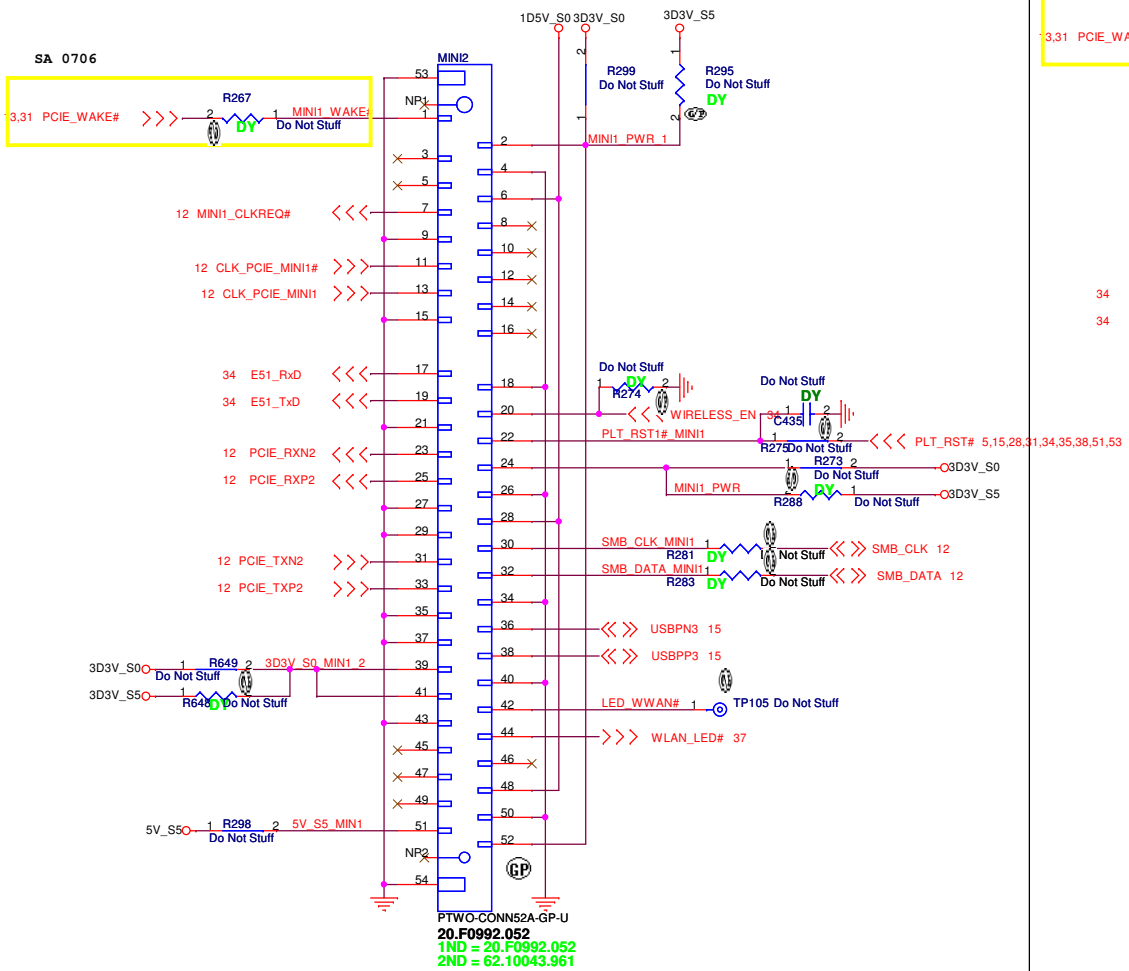
JM31-CP

Rev
SB

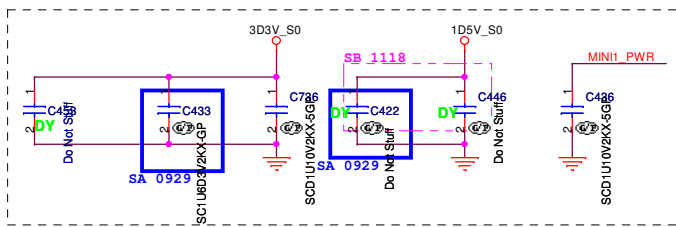
Date: Thursday, February 25, 2010

Sheet 31 of 62

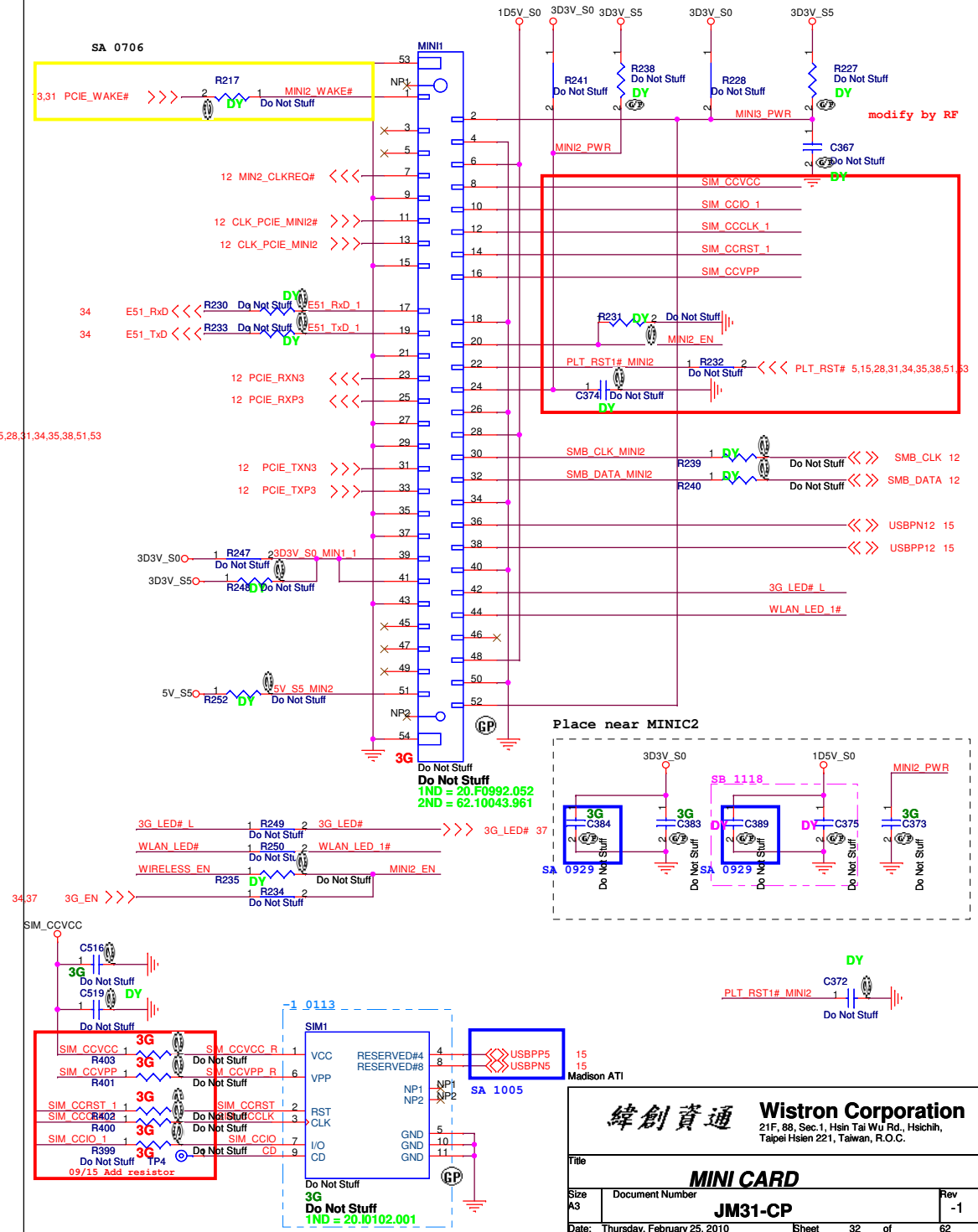
Mini Card Connector(WLAN) Support debug-card

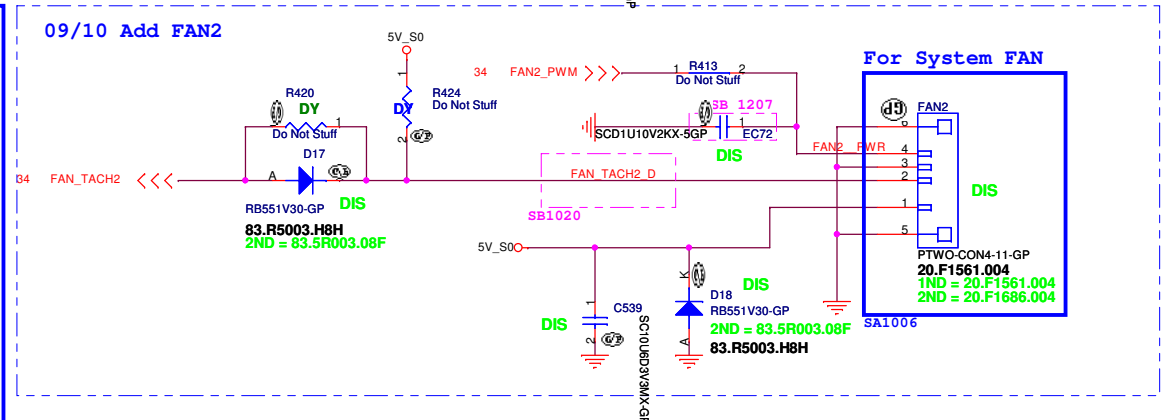
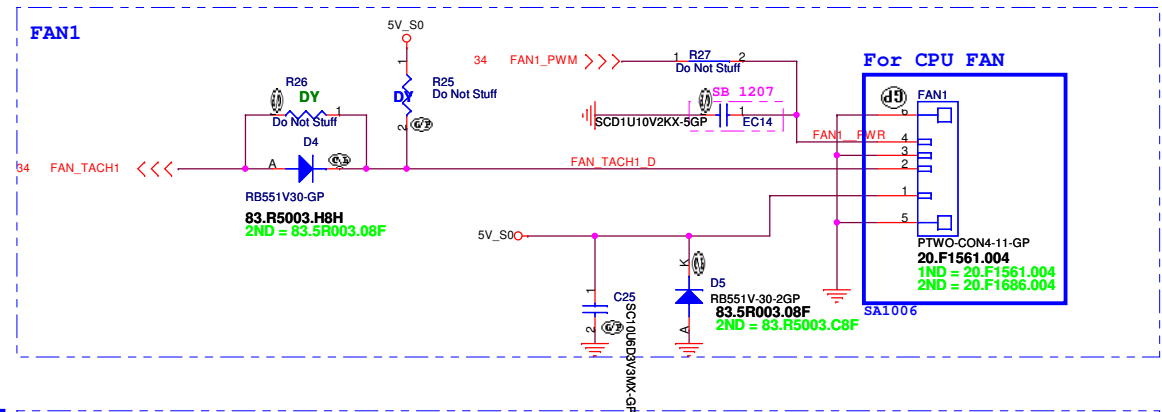
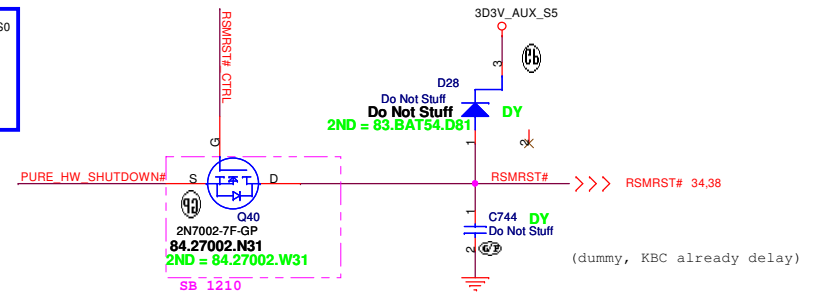
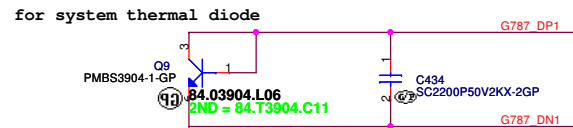


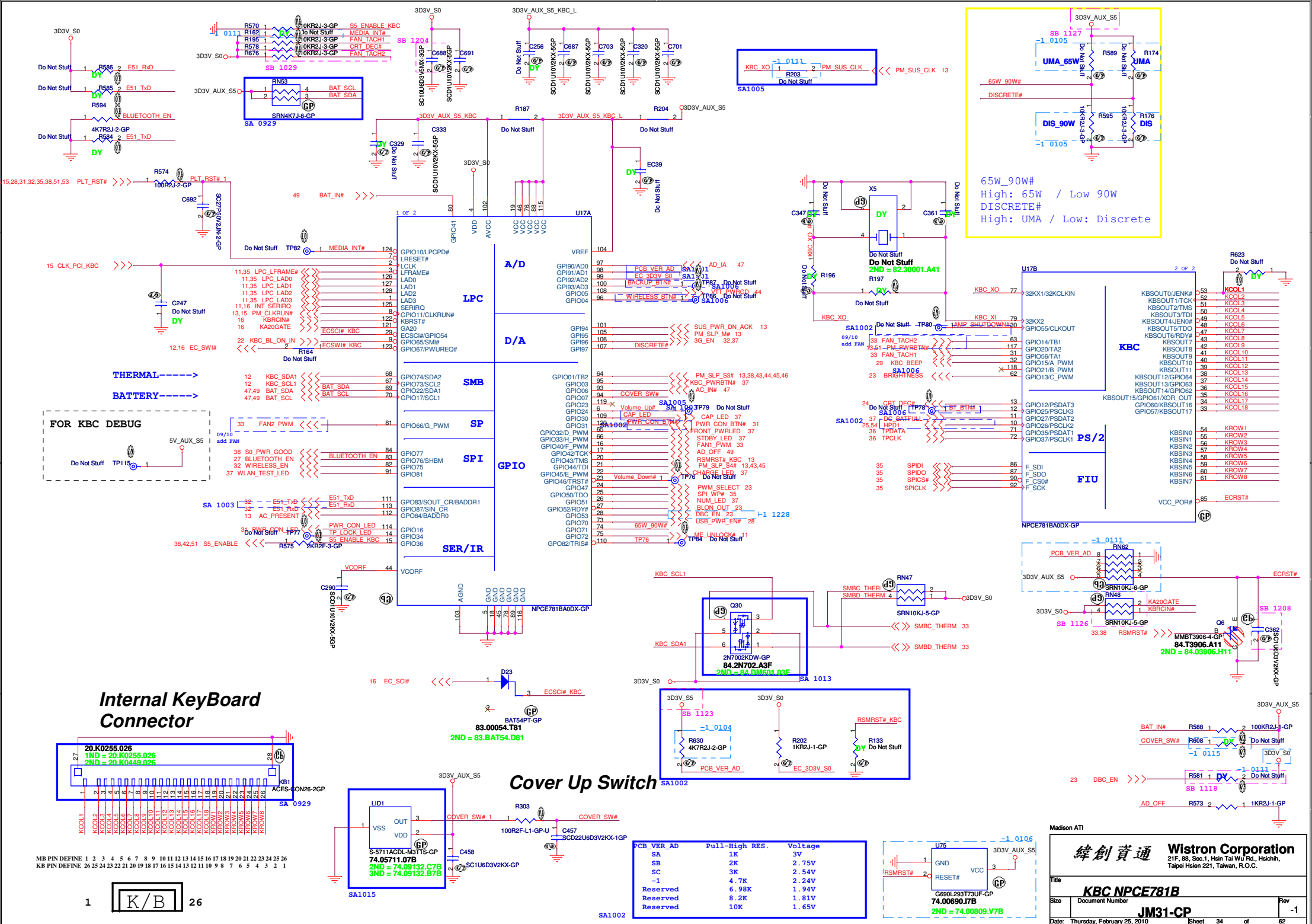
Place near MINI1

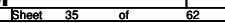


Mini Card Connector(Robson2 and 3G)

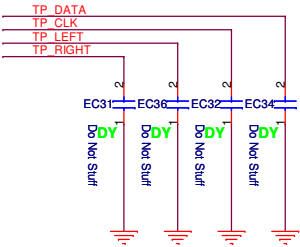
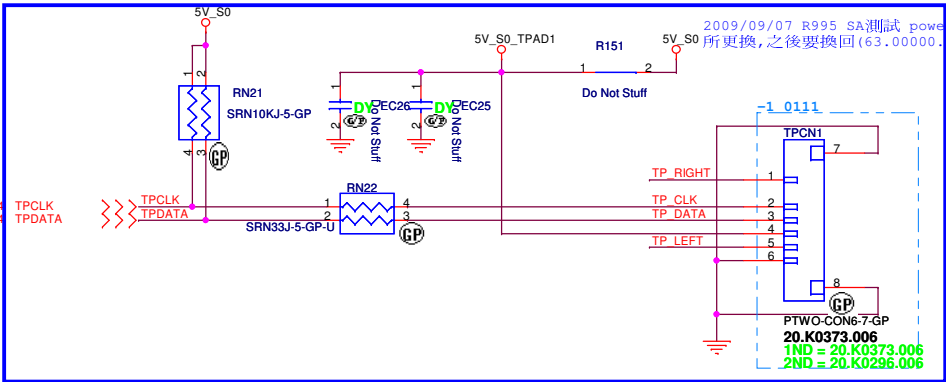
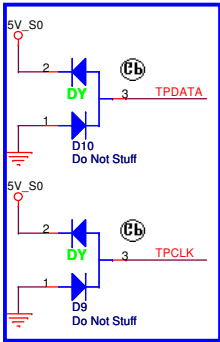




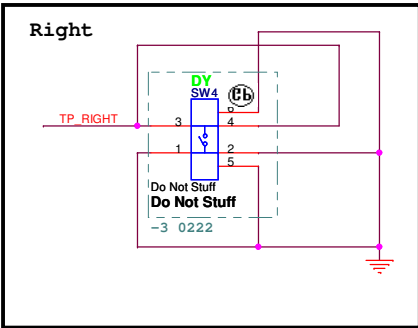
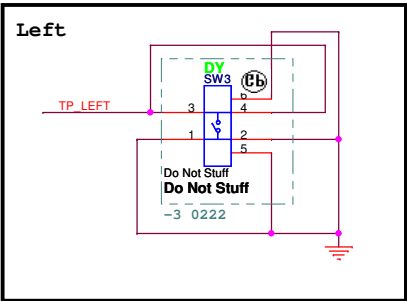
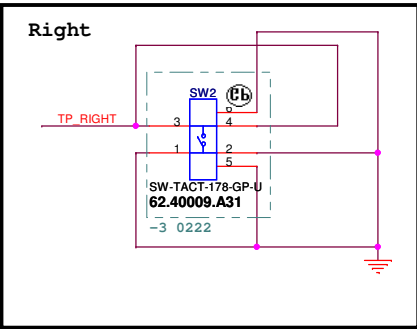
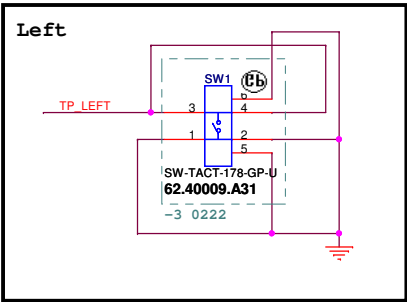


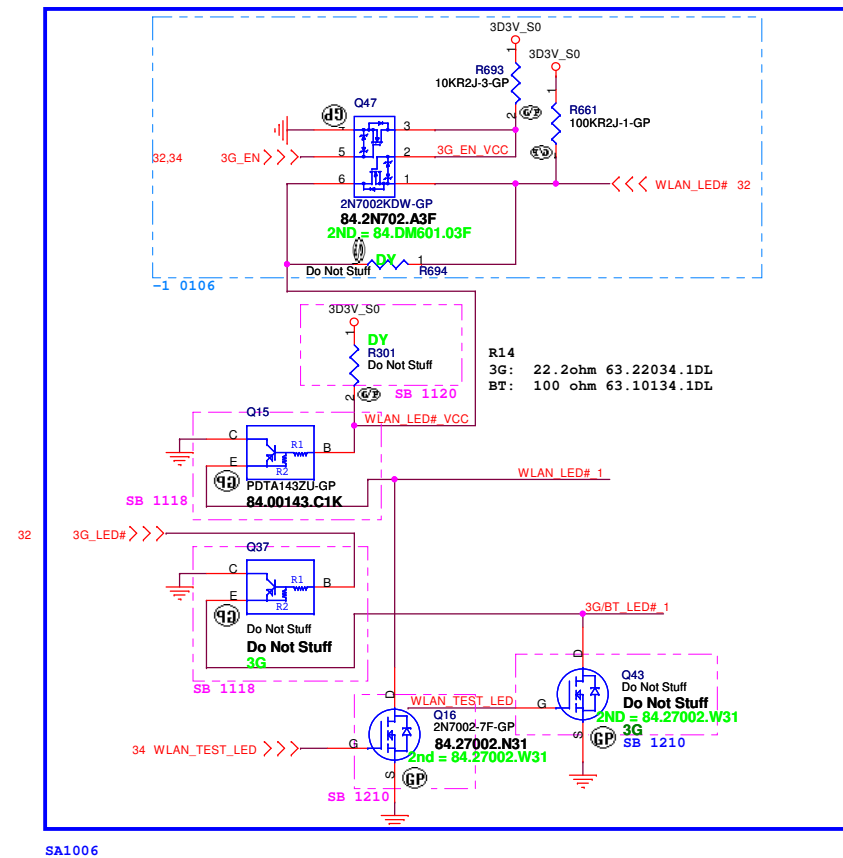
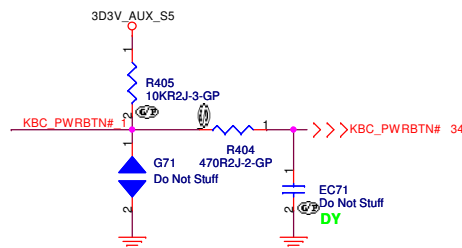
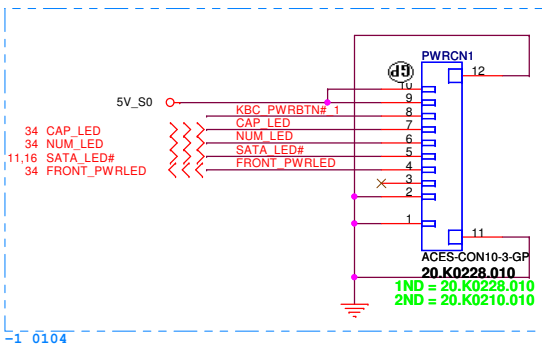
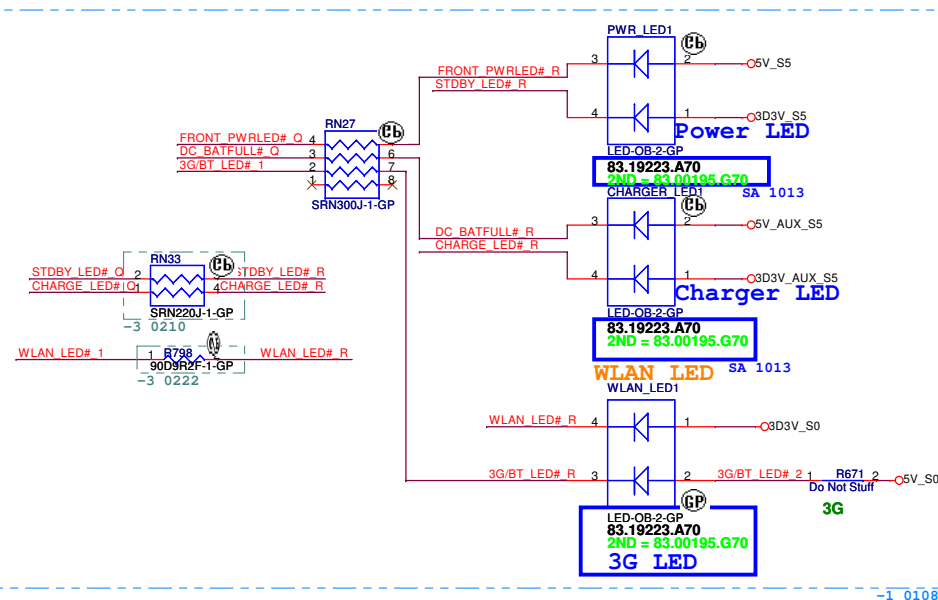
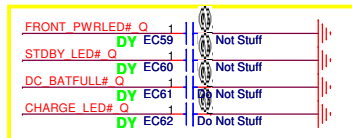
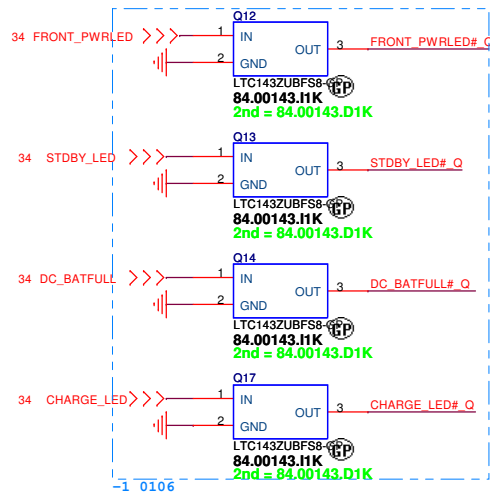
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TOUCH PAD



1 12
T/P

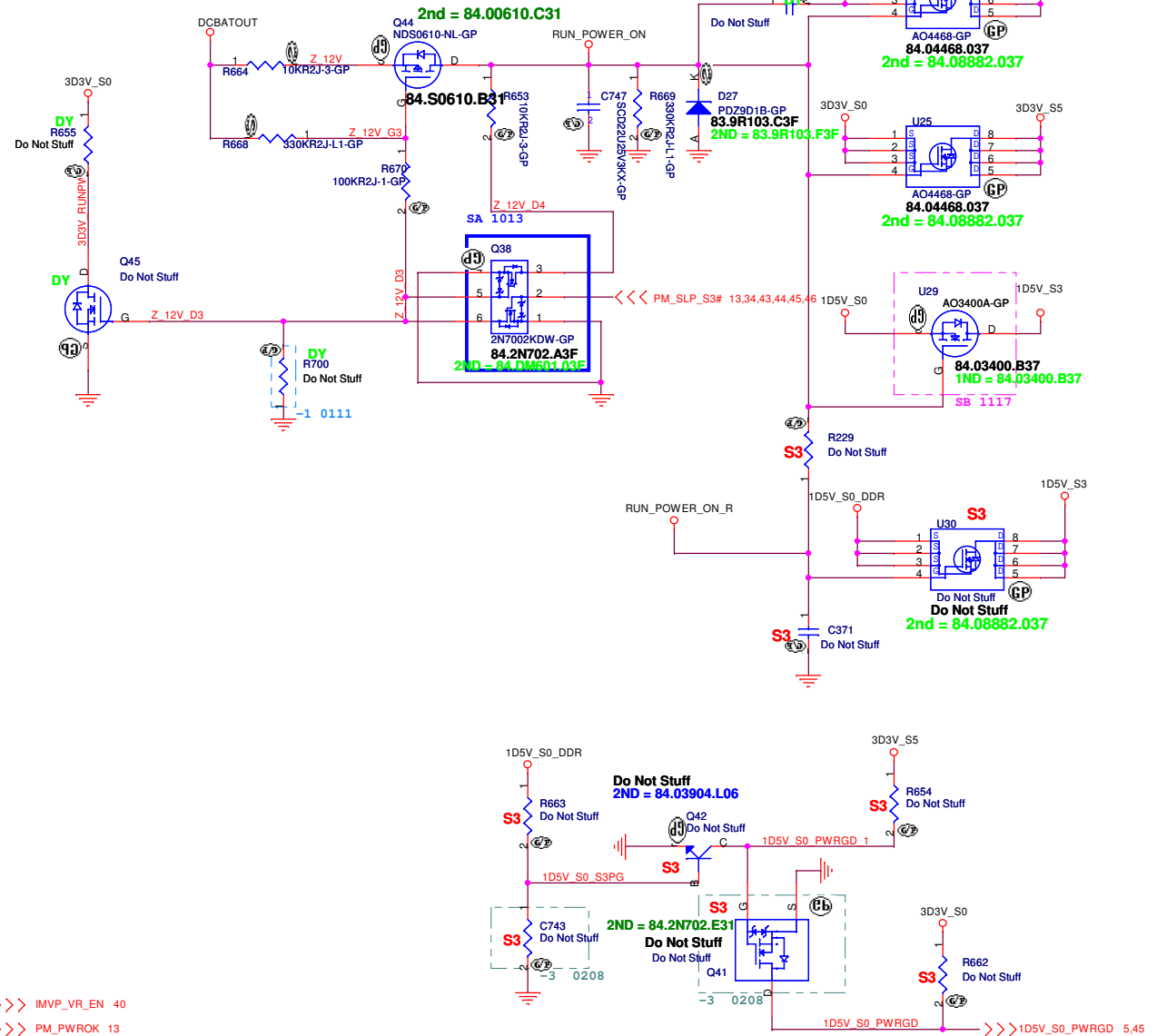
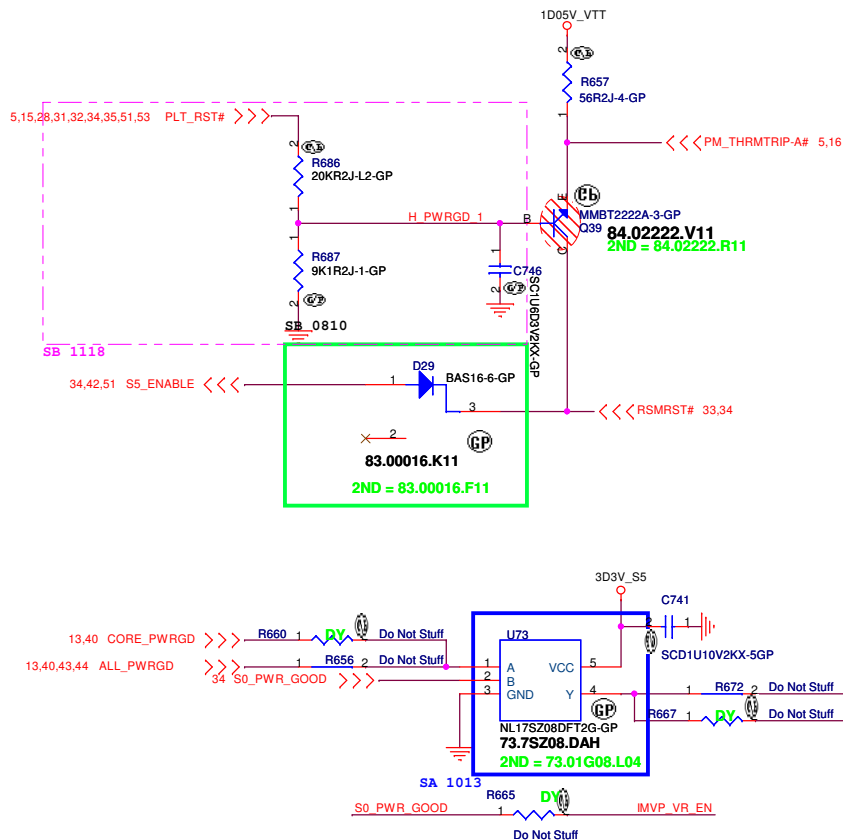
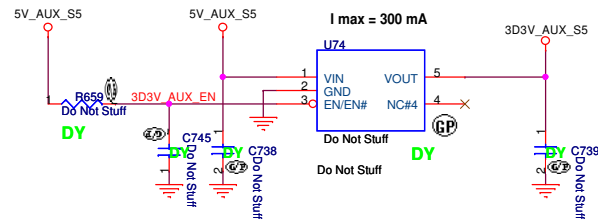




Run Power

Aux Power

3D3V_AUX_S5



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Title

RUN POWER and 3D3V AUX S5

Size

Document Number

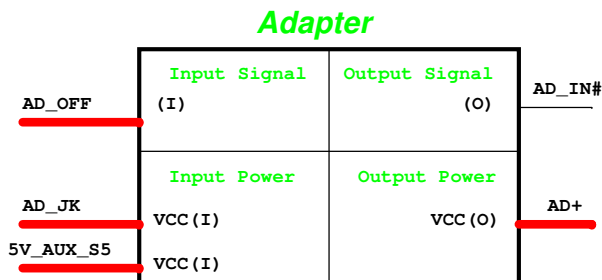
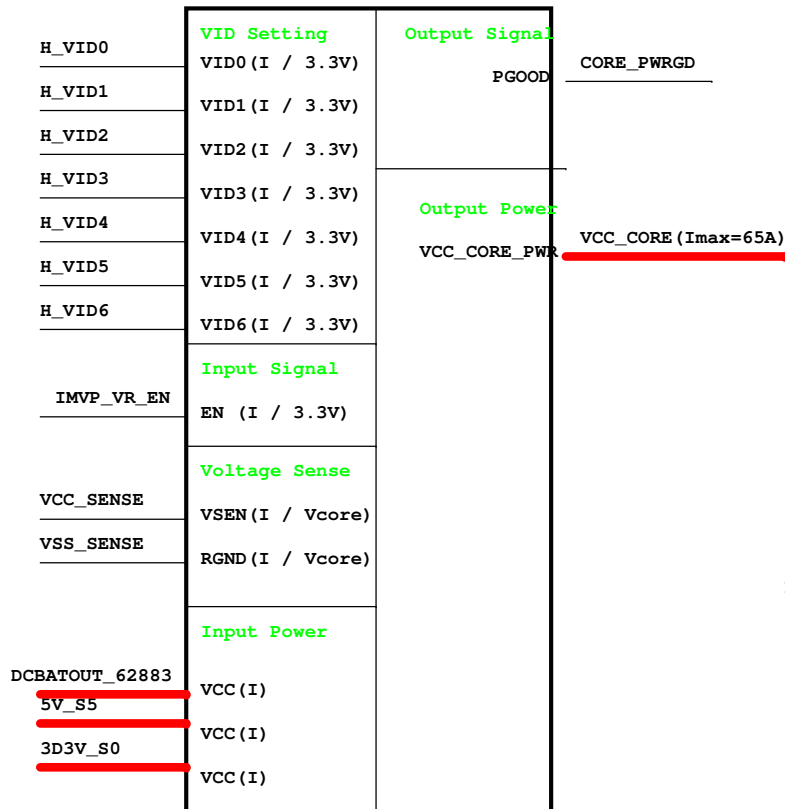
JM31-CP

-3

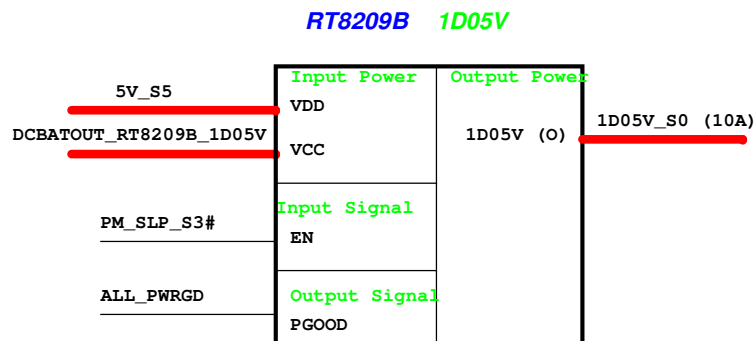
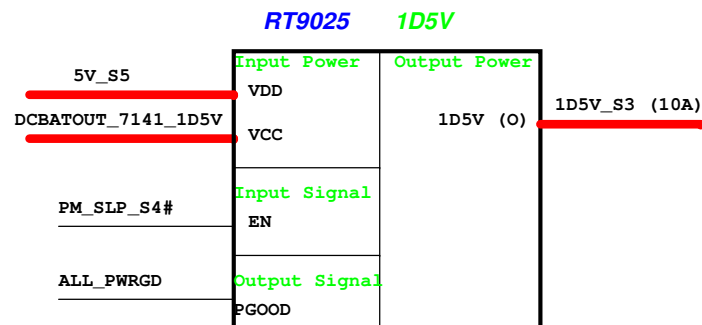
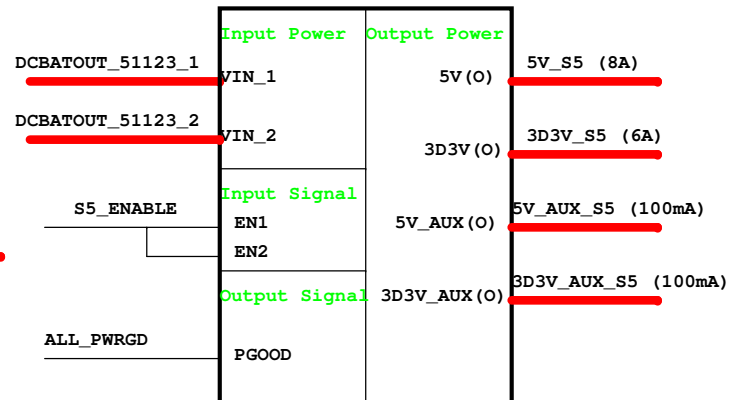
Date: Thursday, February 25, 2010

Sheet 38 of 62

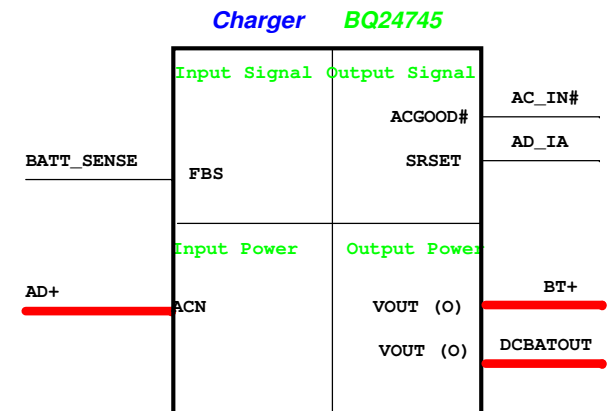
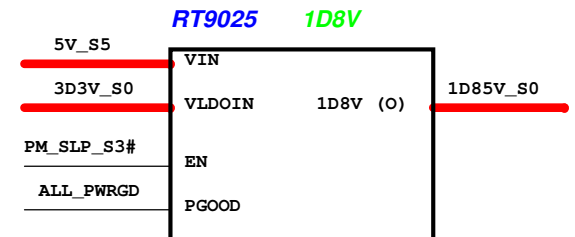
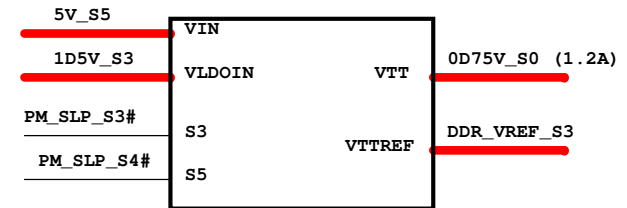
ISL62883 VCC_CORE



TPS51123 5V/3D3V



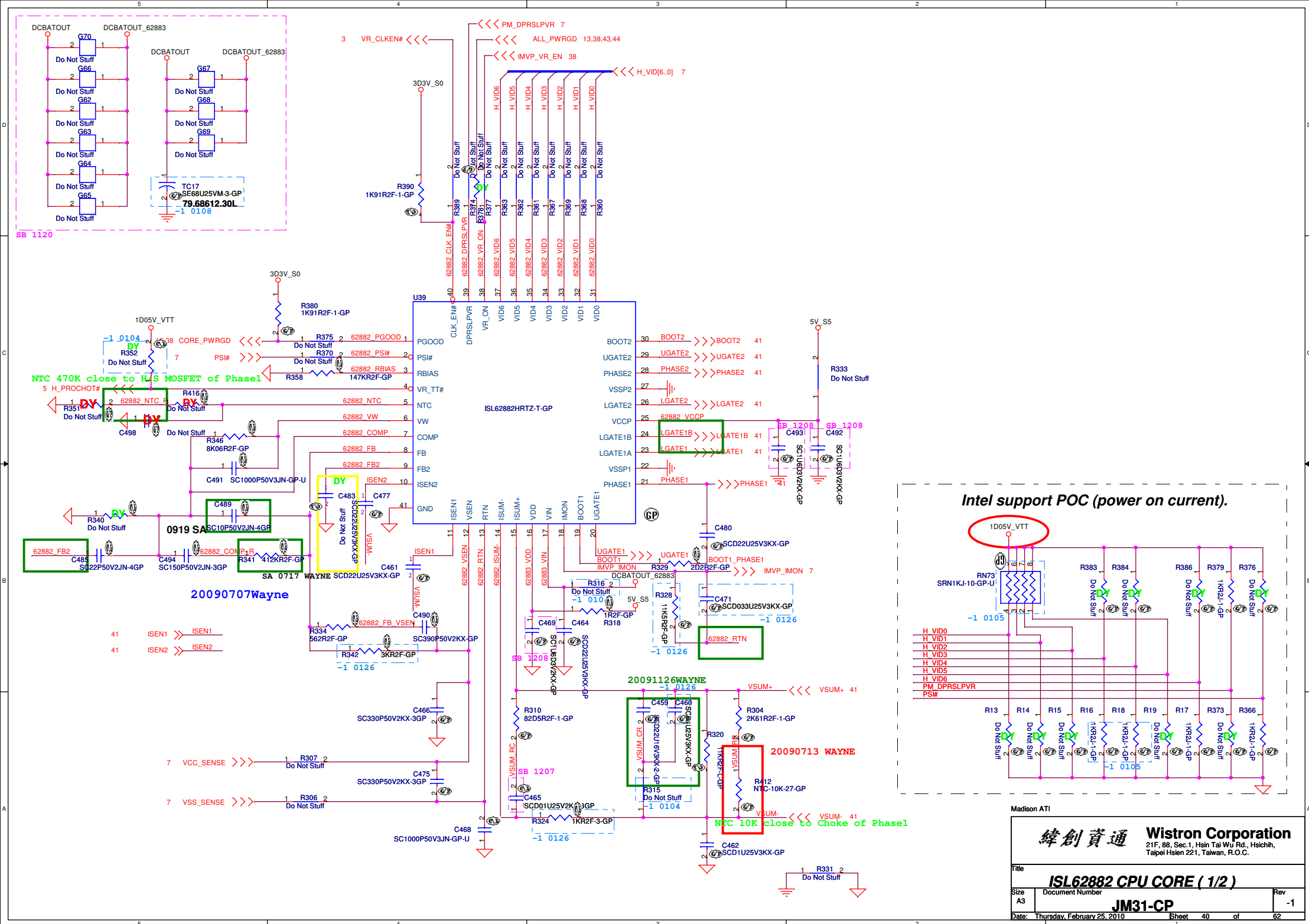
RT9026 0D75V_S0

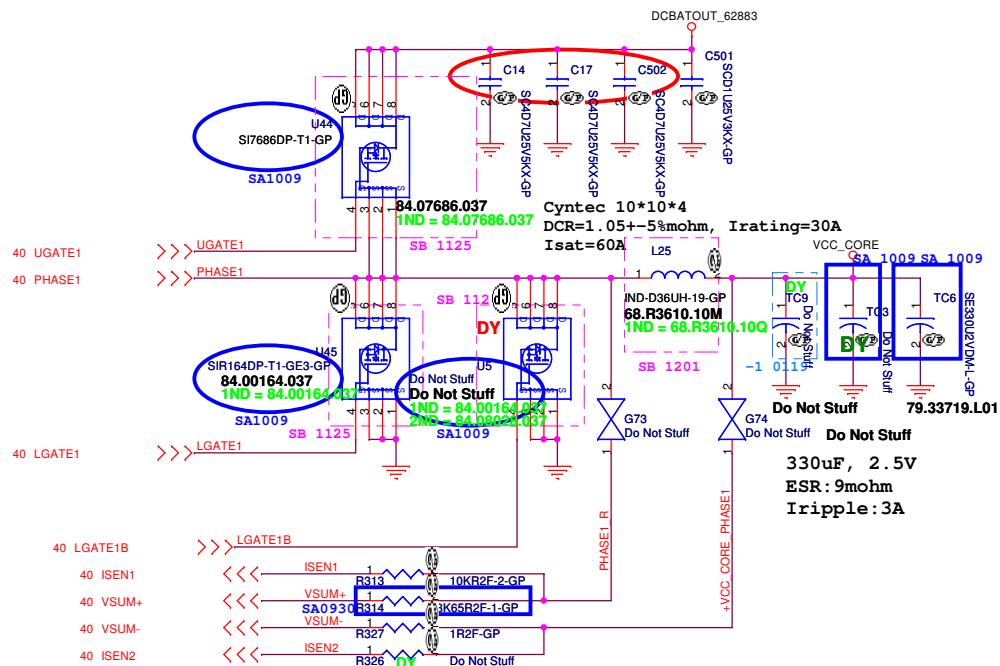
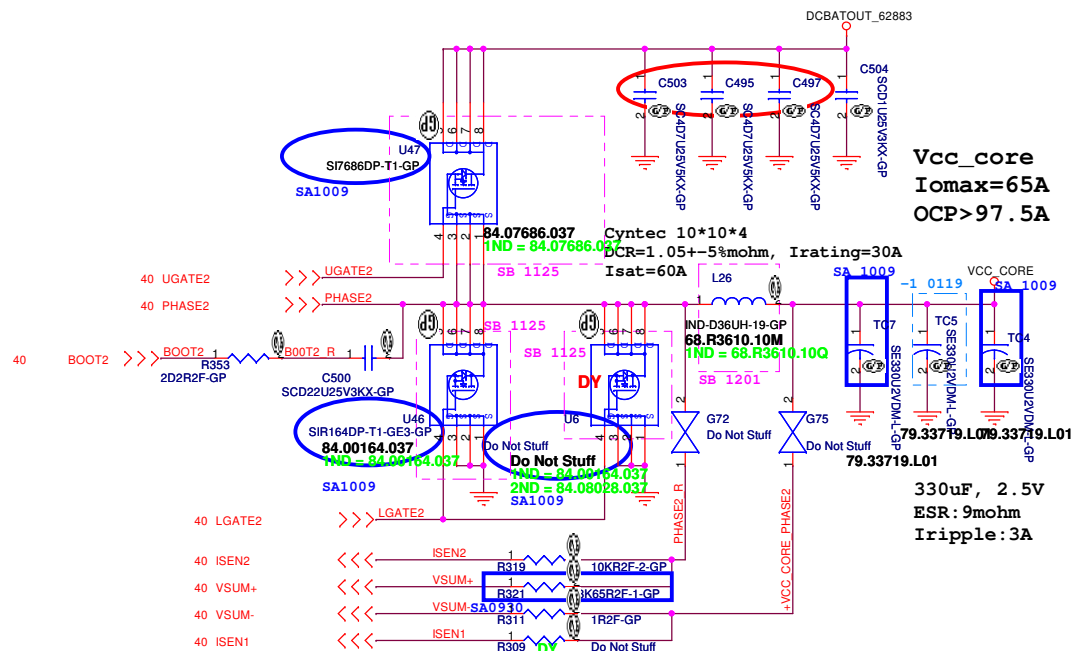


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Title		
Power Block Diagram		
Size	Document Number	Rev
	JM31-CP	SA
Date: Thursday, February 25, 2010	Sheet 39	of 62

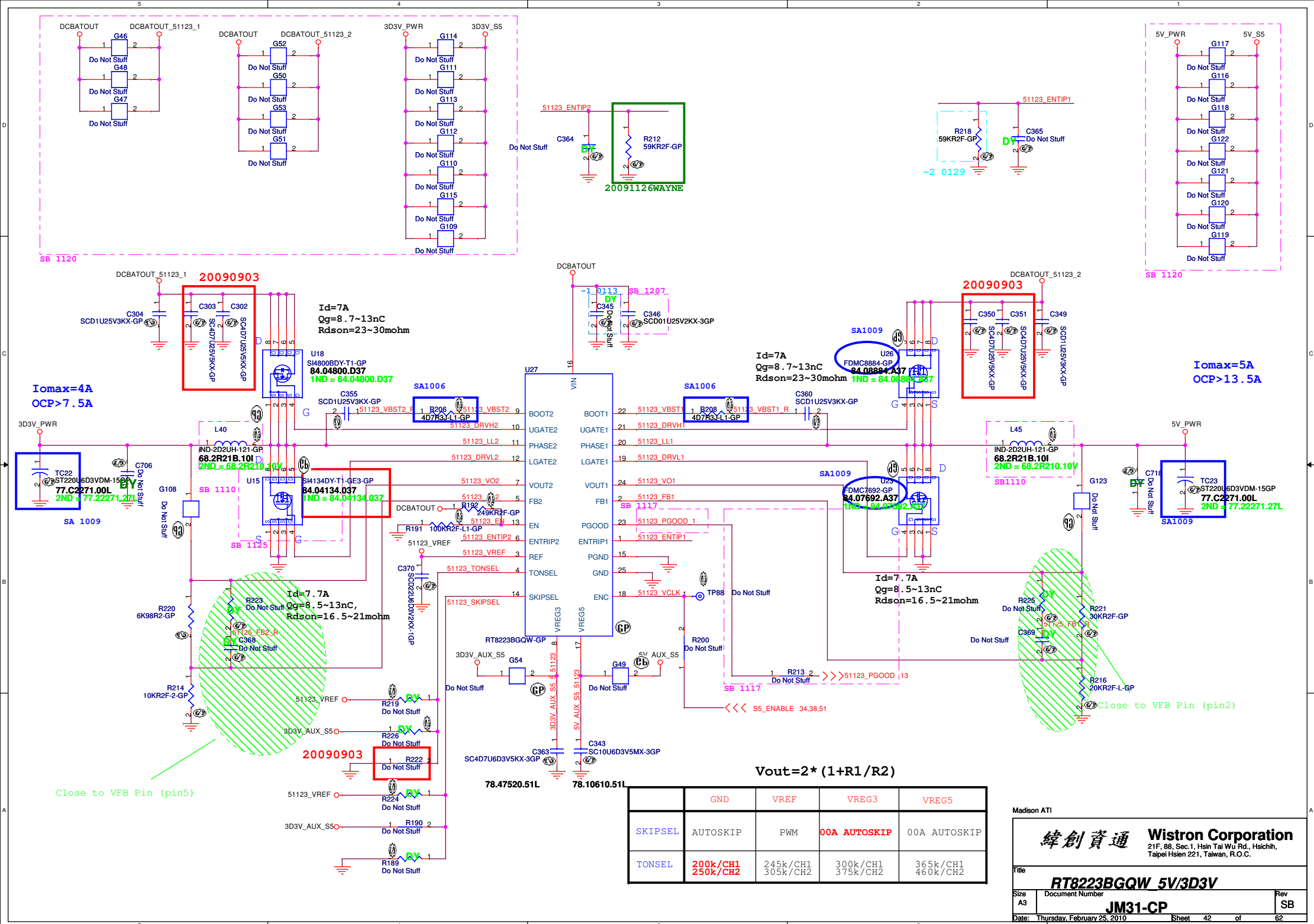




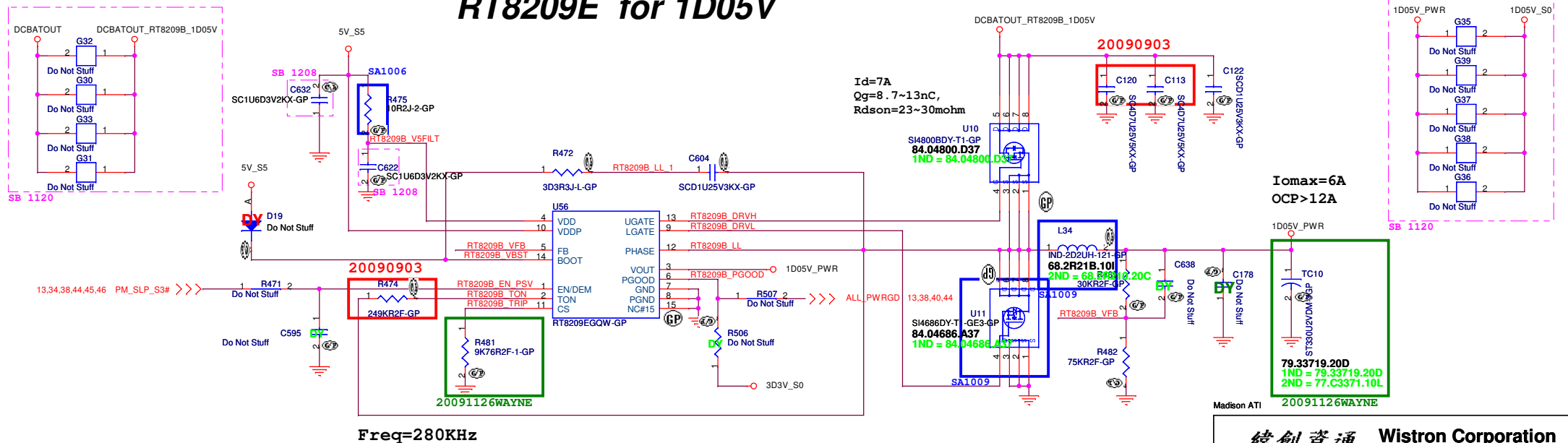
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Taipei Hsien 221, Taiwan, R.O.C.

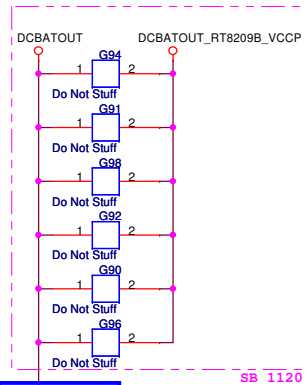
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Size	Document Number	Rev	
A3	JM31-CP	SB	
Date:	Thursday, February 25, 2010	Sheet	41 of 62



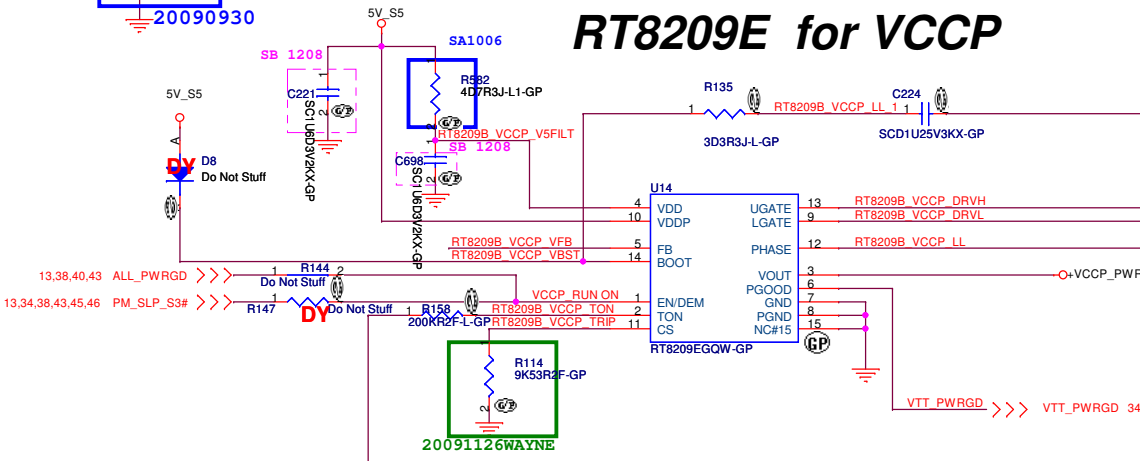
RT8209E for 1D05V



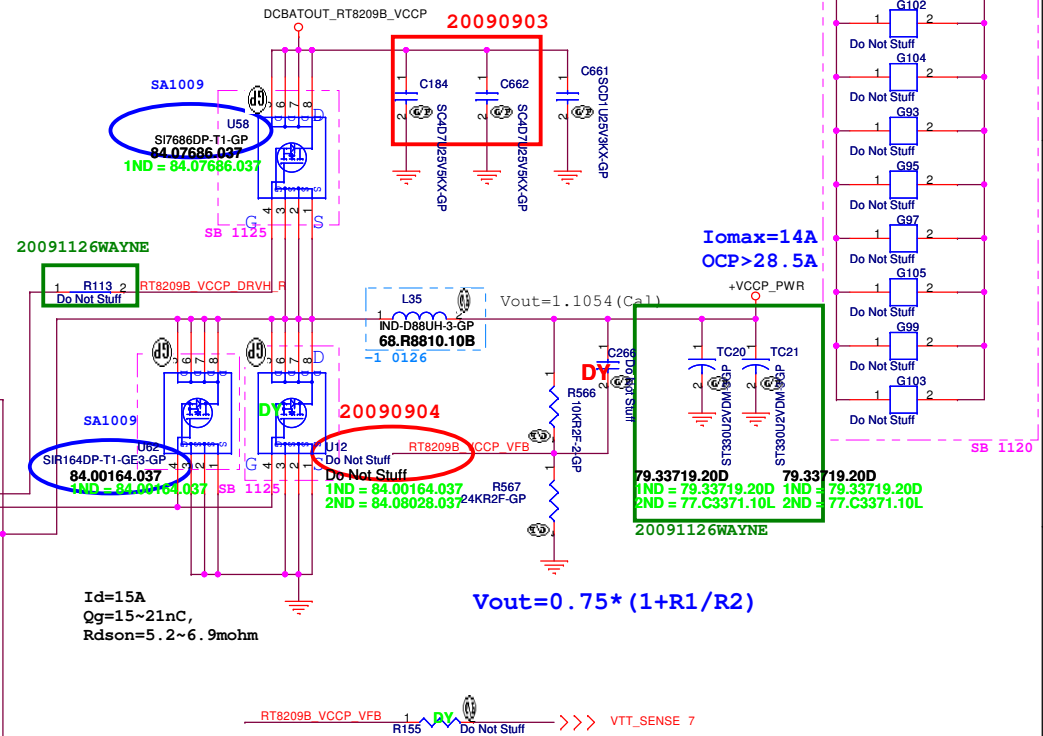
Title			
RT8209E 1D5V / RT8209E 1D05V			
Size	Document Number		Rev
A3	JM31-CP		SB
Date:	Thursday, February 25, 2010	Sheet 43 of 62	



RT8209E for VCCP

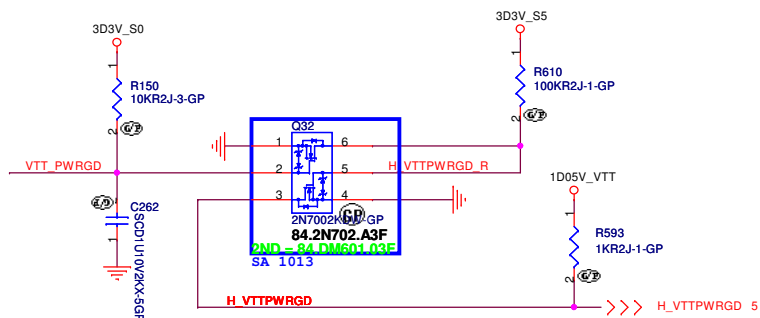


Freq=360KHz



$$V_{out} = 0.75 * (1 + R1/R2)$$

$I_d = 15A$
 $Q_g = 15 \sim 21nC$
 $R_{dson} = 5.2 \sim 6.9m\Omega$

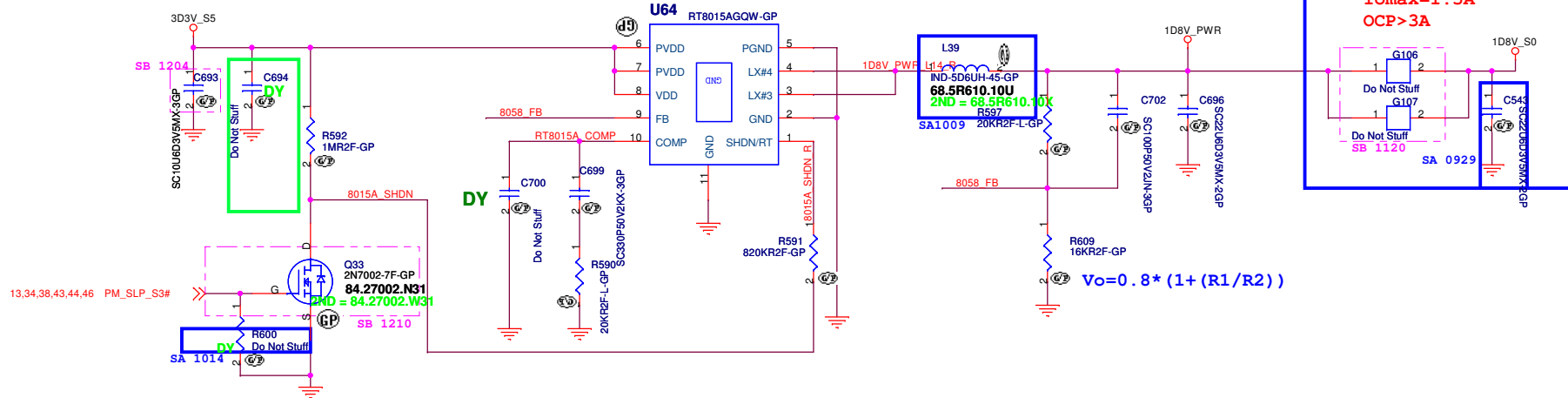


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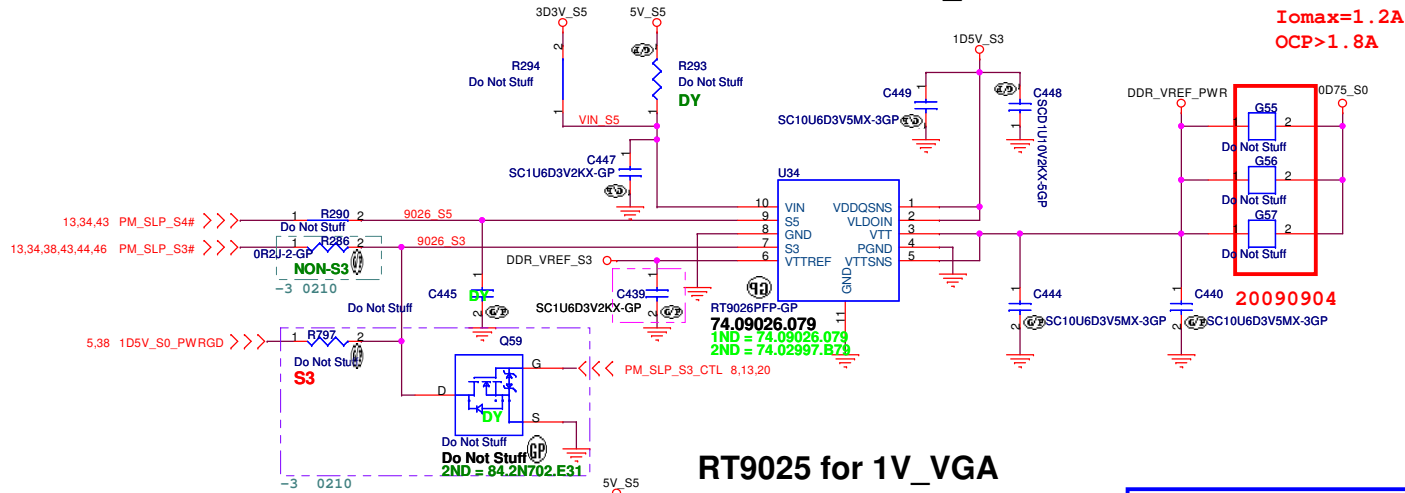
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RT8209E +VCCP				
Size	Document Number			Rev
A3	JM31-CP			SB
Date:	Thursday, February 25, 2010		Sheet 44 of	62

RT8015A for 1D8V_S0

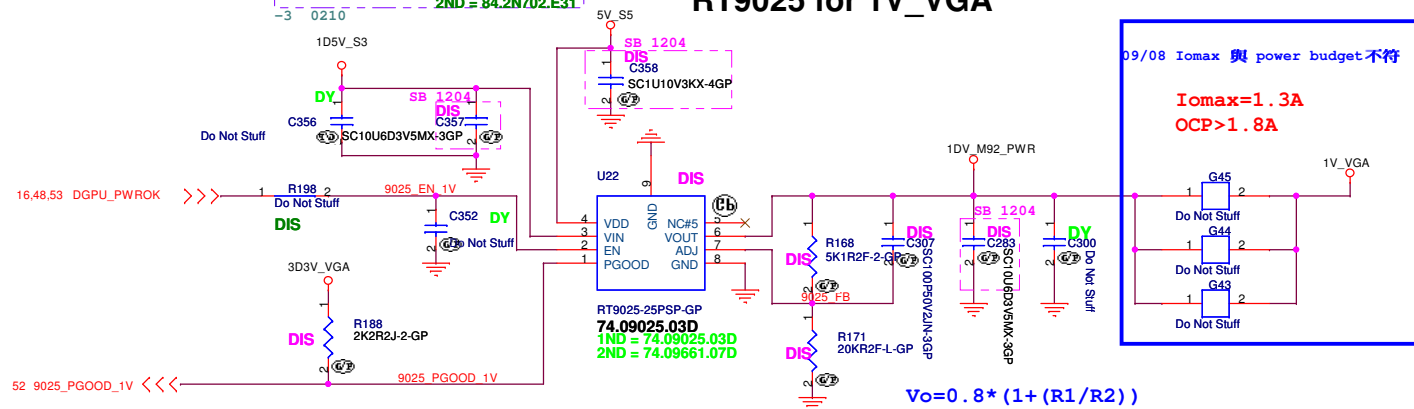


09/08 add 3D3V_S5, R837, R836

RT9026 for 0D75V_S3



RT9025 for 1V_VGA



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Title

RT9025 1D8V 1V/RT9026 0D75

Size

Document Number

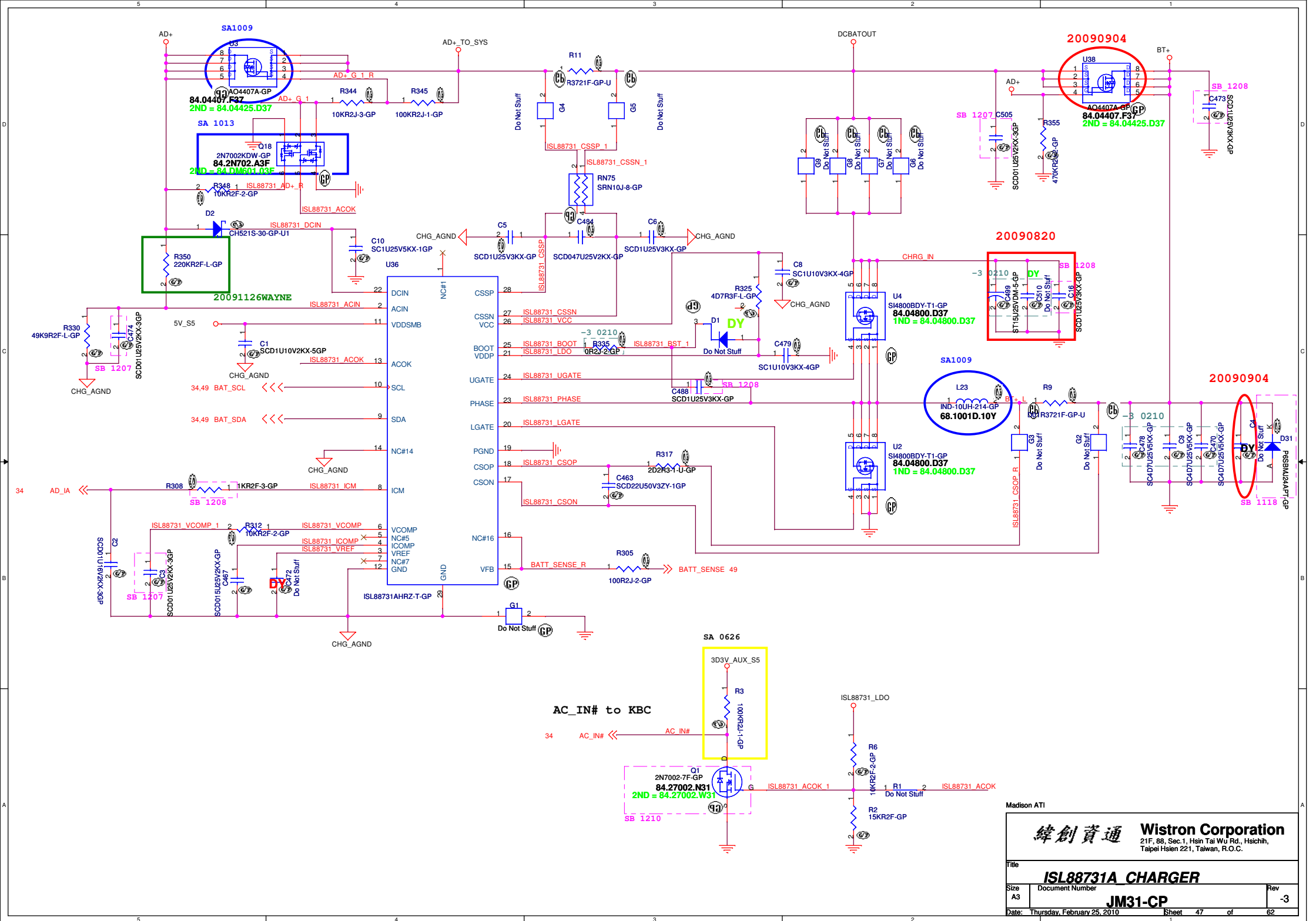
JM31-CP

Rev

-3

Date: Thursday, February 25, 2010

Sheet 45 of 62



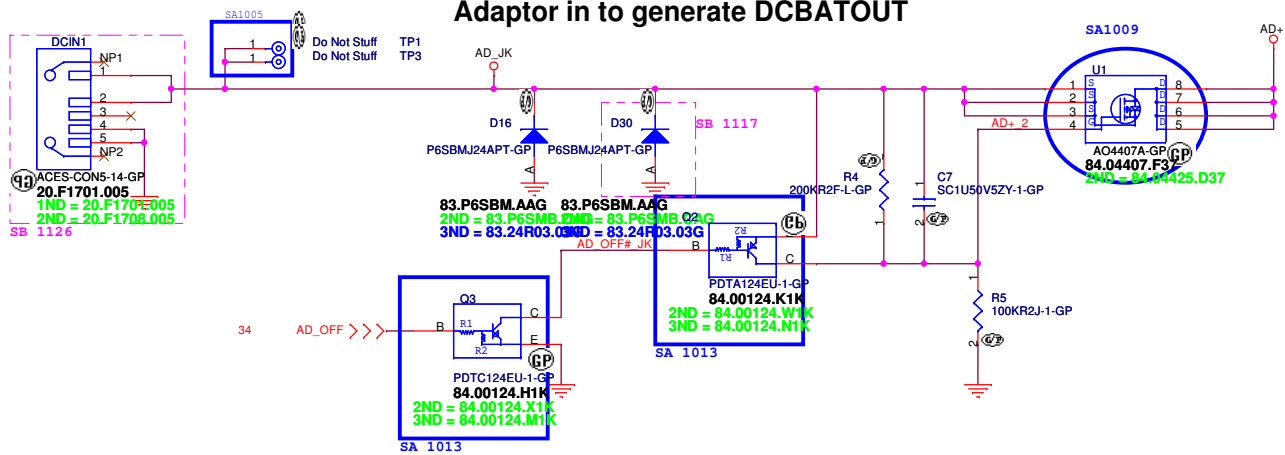
2009/06/19 WAYNE



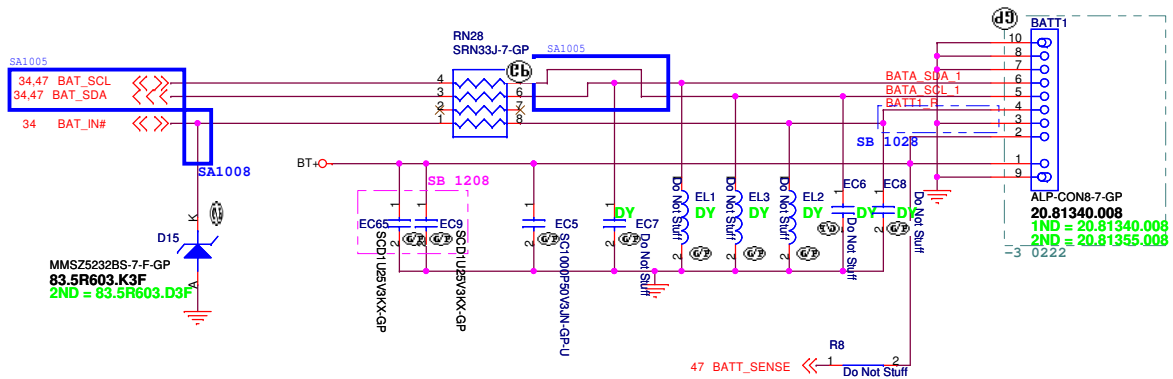
GPIO15/VID0	VGA_CORE
0	0.90V
1	1.12V

GPIO15/VID0	VGA_CORE
0	0.90V
1	1.02V

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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[illegible]

AD/BATT CONN

Size
A3

Document Number

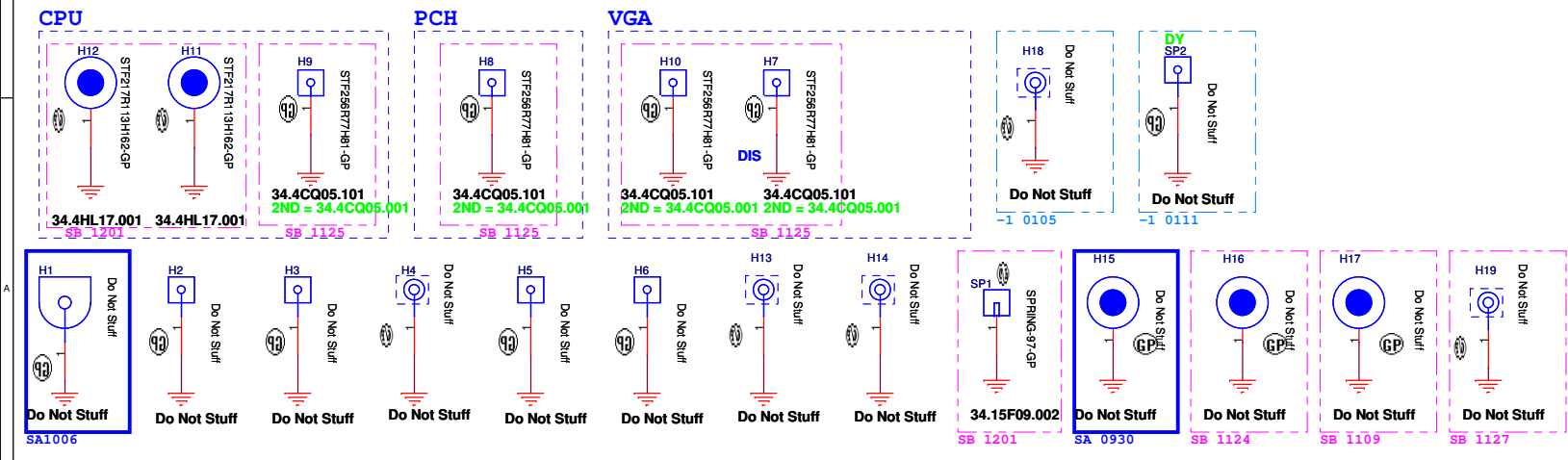
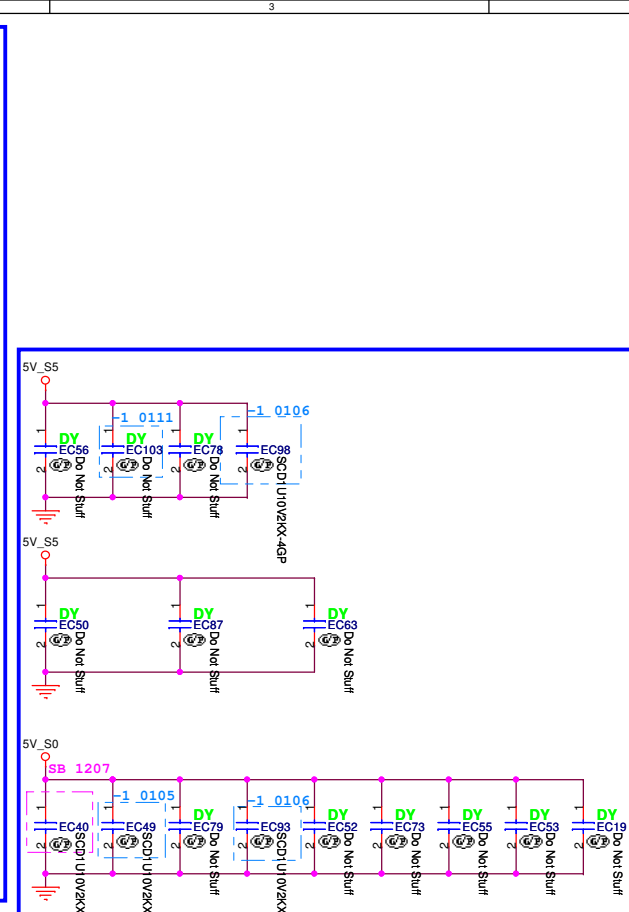
JM31-CP

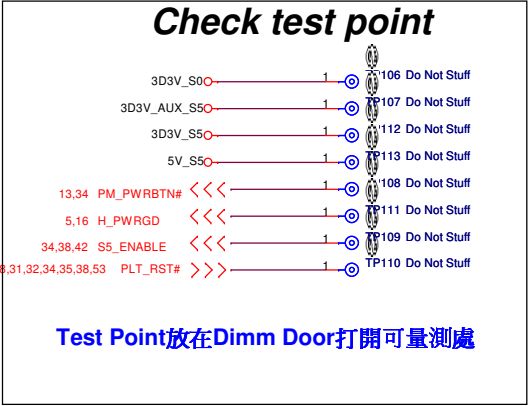
Rev	SE
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Date: Thursday, February 25, 2010

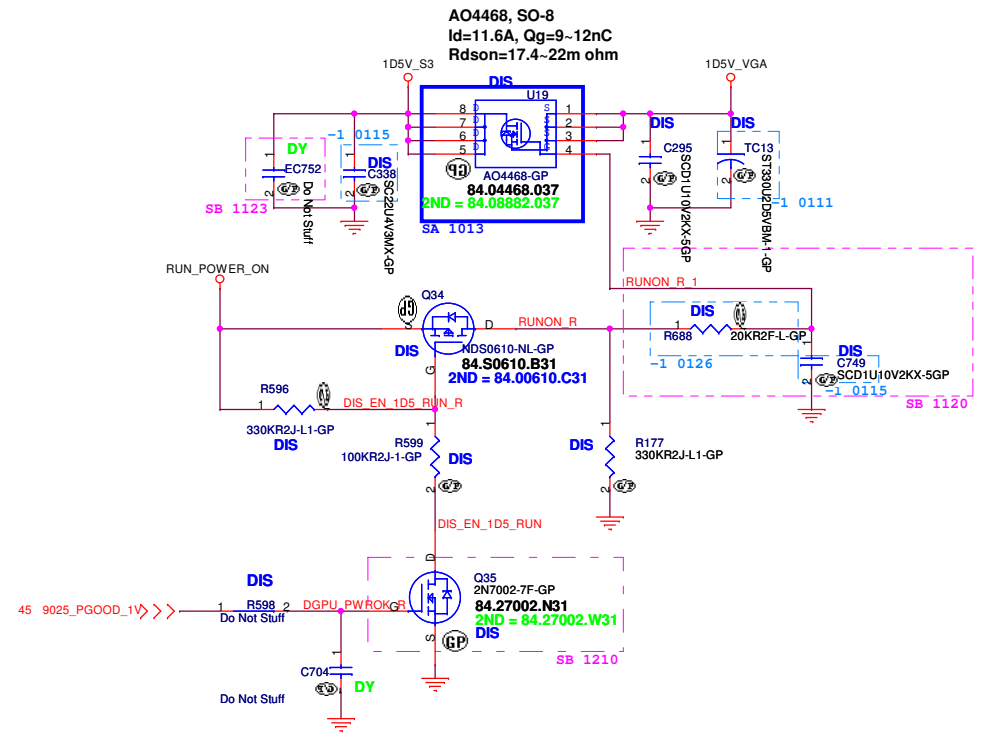
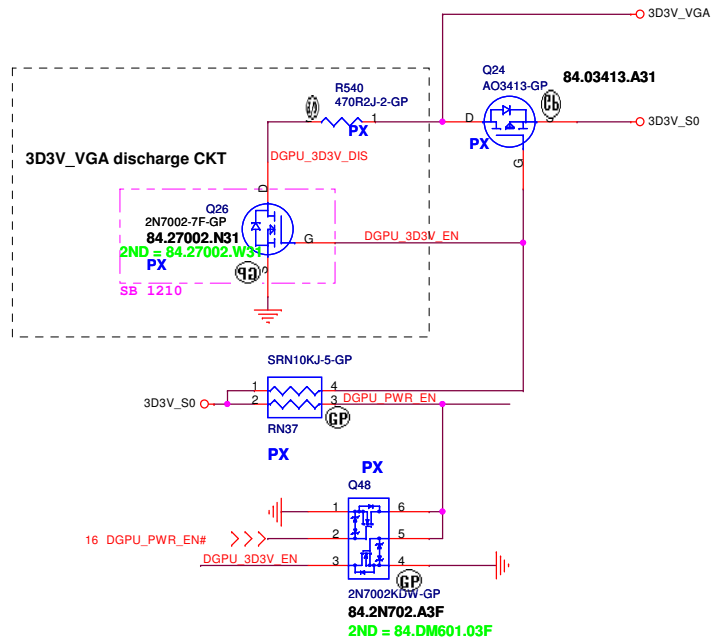
Sheet 4

62

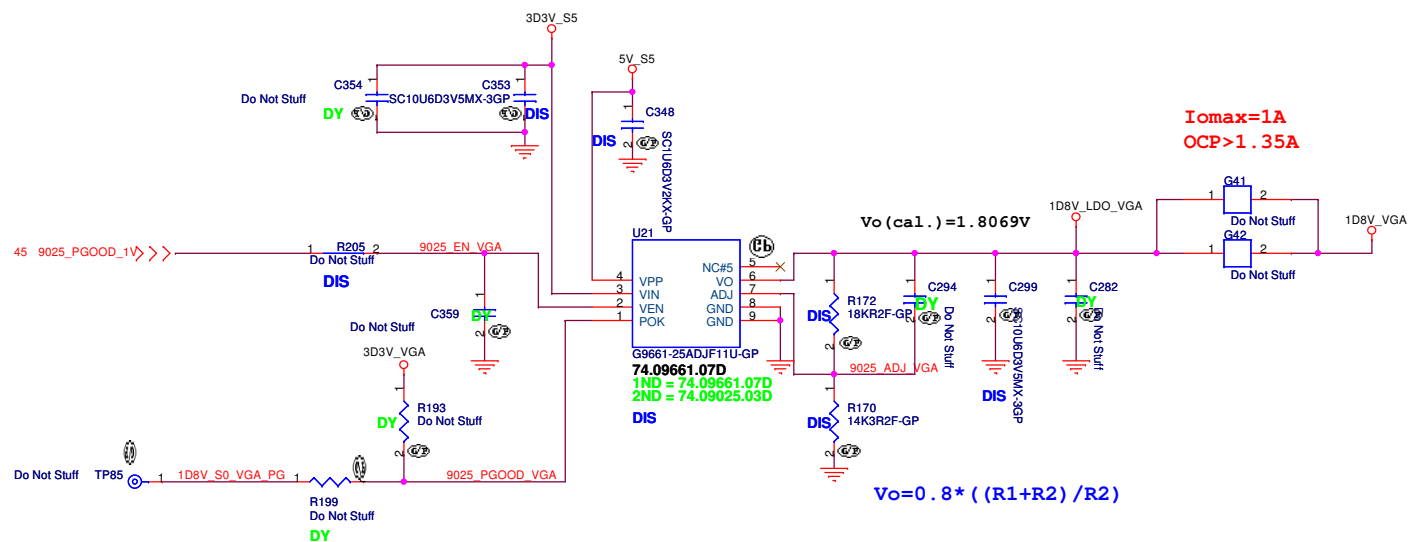




+3VS to 3.3V_DELAY Transfer



G9661 for 1D8V_VGA



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ATI POWER

Size
A3

Document Number

JM31-CP

Rev
-1

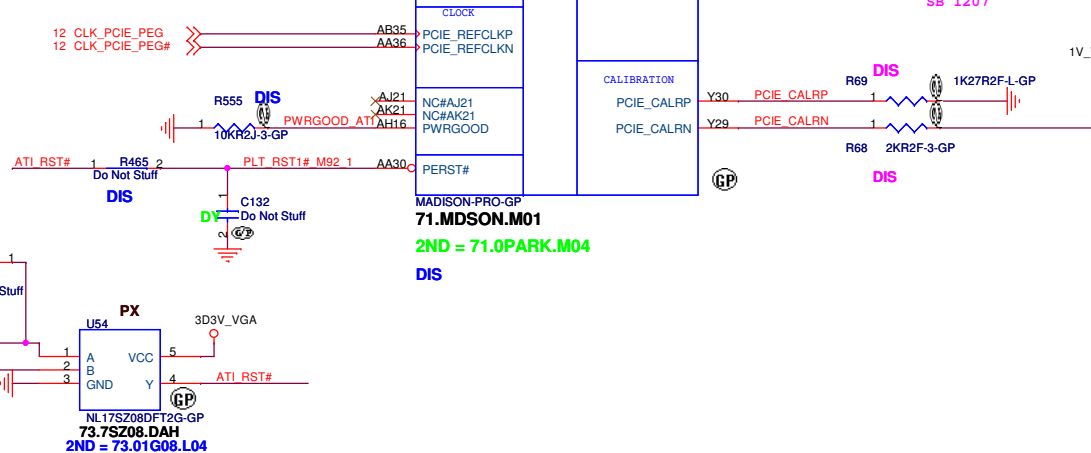
Date: Thursday, February 25, 2010

Sheet 52 of 62

4 PEG_TXP[15..0] << PEG_TXP[15..0]
4 PEG_TXN[15..0] << PEG_TXN[15..0]

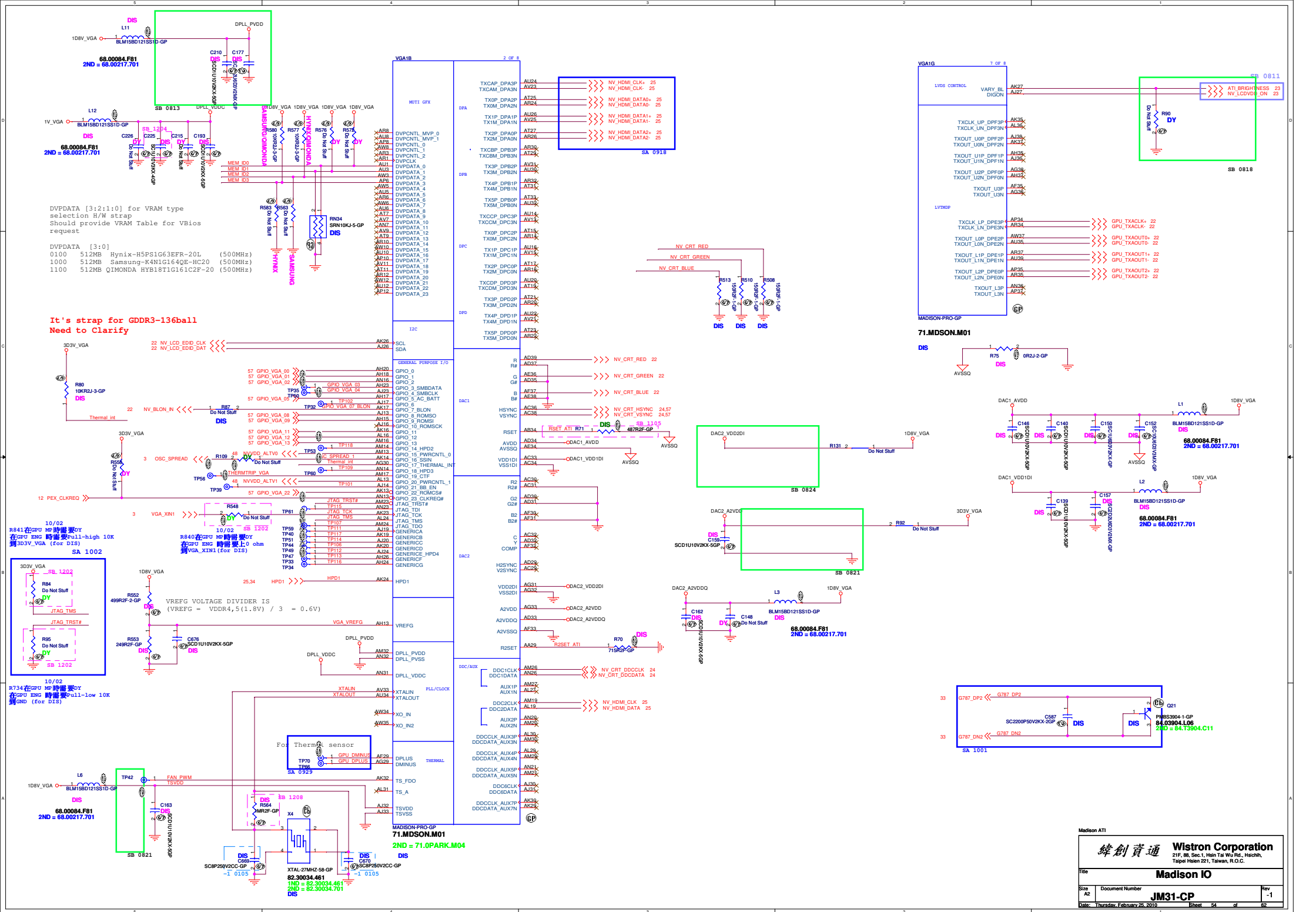


4 PEG_RXP[15..0] << PEG_RXP[15..0]
4 PEG_RXN[15..0] << PEG_RXN[15..0]



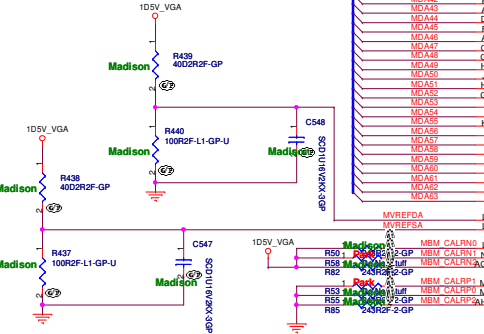
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Title Madison PCIE	
Size A3	Document Number JM31-CP
Date: Thursday, February 25, 2010	Sheet 53 of 62



For SSTL-1.8/SSTL-2/DDR1/GDDR1: 0.5 * VDDR1.
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 * VDDR1.

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R



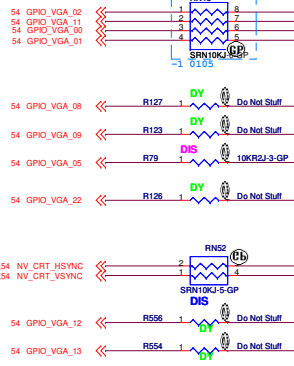
Madison: MEM_CALRP[0,2] signals are used.
Park: MEM_CALRP1 and MEM_CALRN1 are used.

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS
TX_PWRS_ENB (Internal PD)	GPI00	PCIe FULL TX OUTPUT SWING Transmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	X
TX_DEEMPH_EN (Internal PD)	GPI01	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	X
RESERVED	GPI08	RESERVED	0
BIF_VGA_DIS	GPI09	VGA ENABLED	0
RESERVED	GPI021	RESERVED	0
BIOS_ROM_EN	GPI022_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GPI0[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1, then Config[3:0] defines the ROM type if BIOS_ROM_EN=0, then Config[3:0] defines the primary memory aperture size	X X X
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	X X

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADDS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1	
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number
128MB	x000	ST	M25P05A
256MB	x001	Microelectronics	M25P10A
64MB	x010		M25P20
32MB	x		M25P40
512MB	x		M25P80
1GB	x	Chingiss (formerly PMC)	Pm25LV512A
2GB	x		Pm25LV010A
4GB	x		



Designator	For M97-M2	For Mannheim
R_MEM_1	10K	10K
R_MEM_2	40R/Short	680R
R_MEM_3	DY	DY
C_MEM	2.2nF	68pF

Madison AT1

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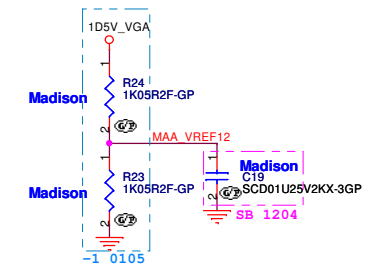
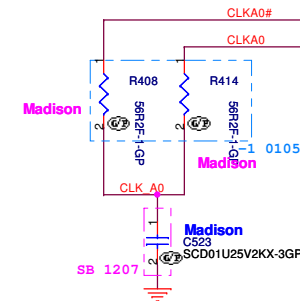
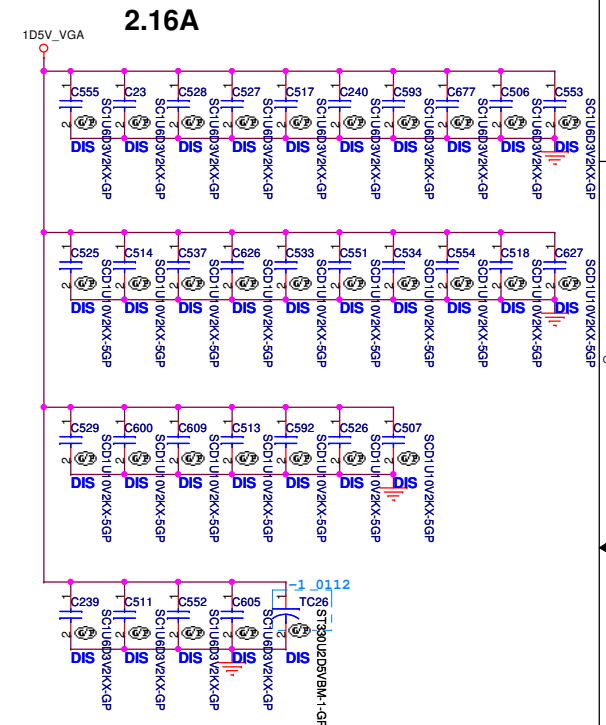
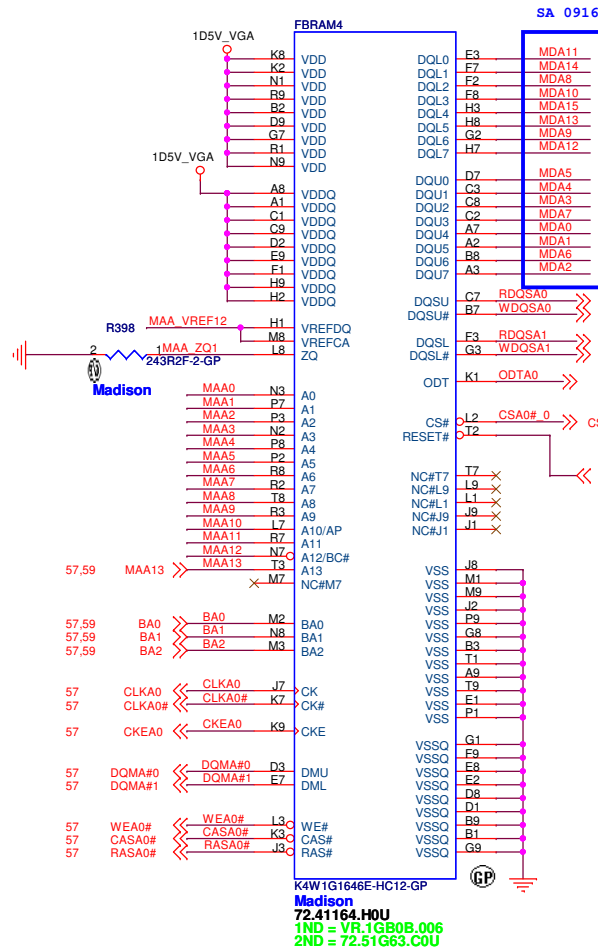
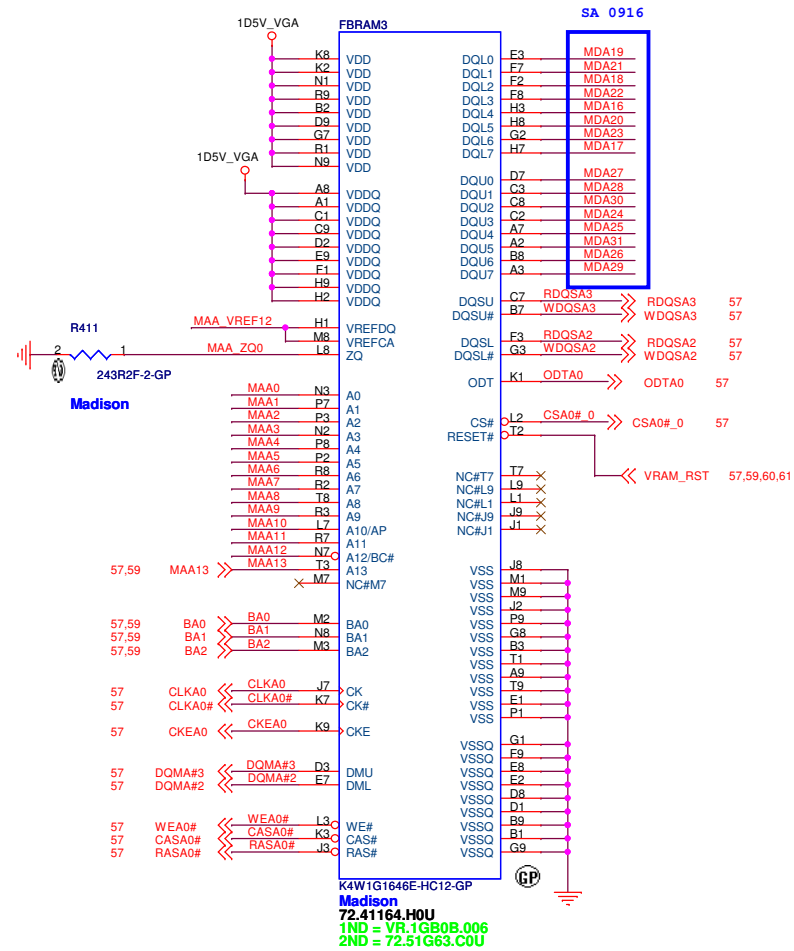
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File **Madison Memory / Straps**

Size A2 Document Number **JM31-CP** Rev SB

Date: Thursday, February 26, 2010 Sheet 57 of 62

DDR3

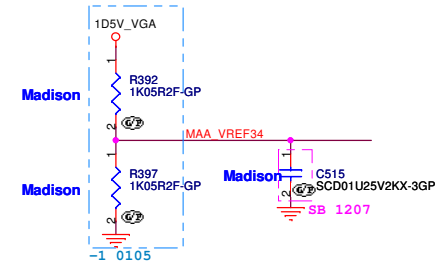
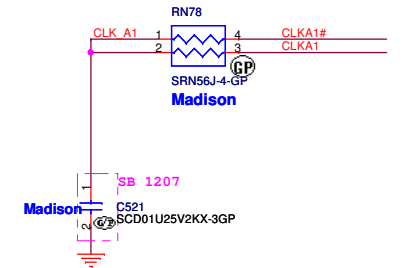
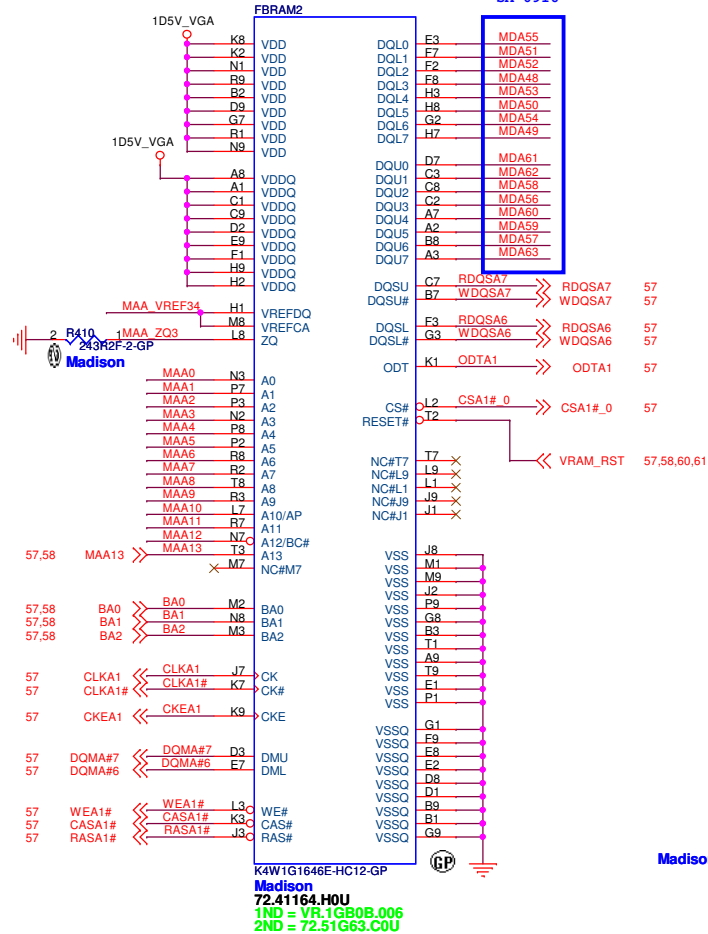
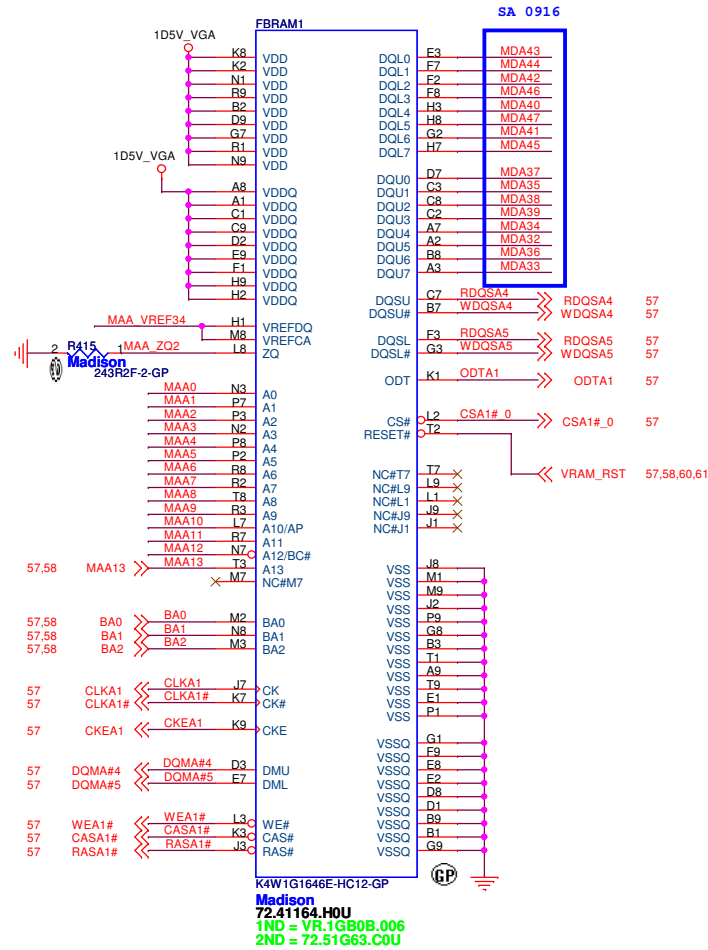


SAMSUNG: 72.41164.H0U (VR.1GB0B.006)
HYNIX: 72.51G63.C0U (VR.1GB0G.004)

Timing diagram showing the relationship between the MAA and MDA registers and the DQMA, RDQSA, and WDQSA signals. The diagram illustrates the timing of read and write operations for these registers.

- 57,59 DQMA[0..7]**: Read operation (red arrow).
- 57,59 RDQSA[0..7]**: Read operation (red arrow).
- 57,59 WDQSA[0..7]**: Read operation (red arrow).
- 57,59 MAA[0..12]**: Read operation (red arrow).
- 57,59 MDA[0..63]**: Read operation (red arrow).

DDR3



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Title		
VRAM(2/4)		
Size	Document Number	Rev
A3	JM31-CP	-1
Date:	Thursday, February 25, 2010	Sheet 59 of 62

SAMSUNG: 72.41164.H0U (VR.1GB0B.006)
HYNIX: 72.51G63.C0U (VR.1GB0G.004)

57,58 DQMA[0..7] <<>>

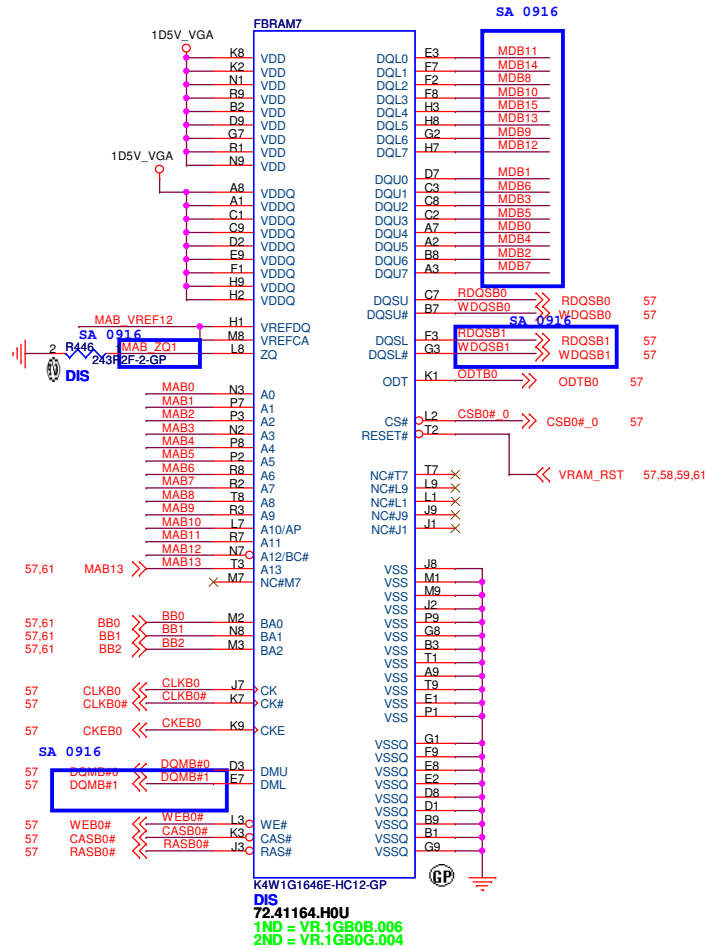
57,58 RDQSA[0..7] <<>>

57,58 WDQSA[0..7] <<>>

57,58 MAA[0..12] <<>>

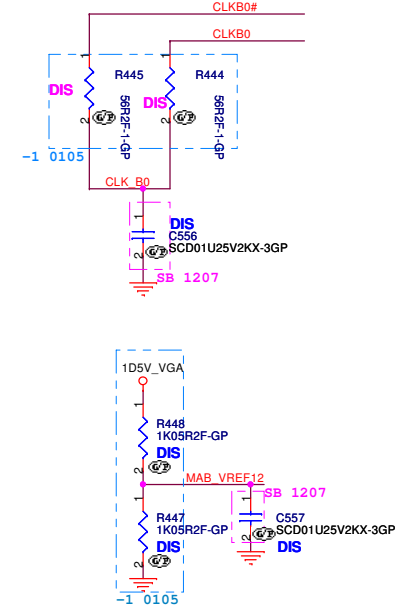
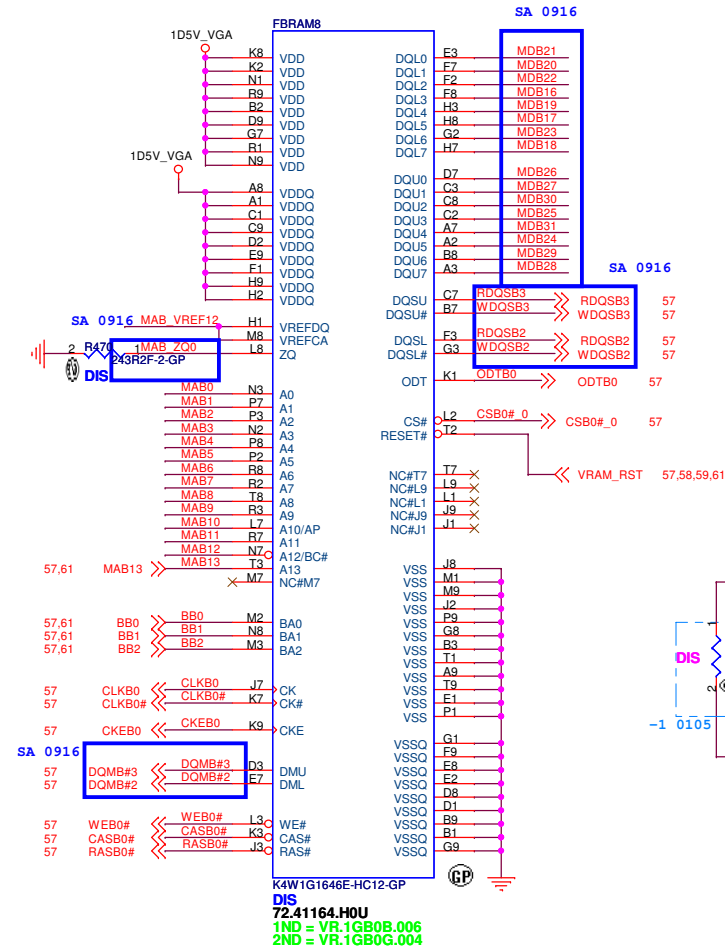
57,58 MDA[0..63] <<>>

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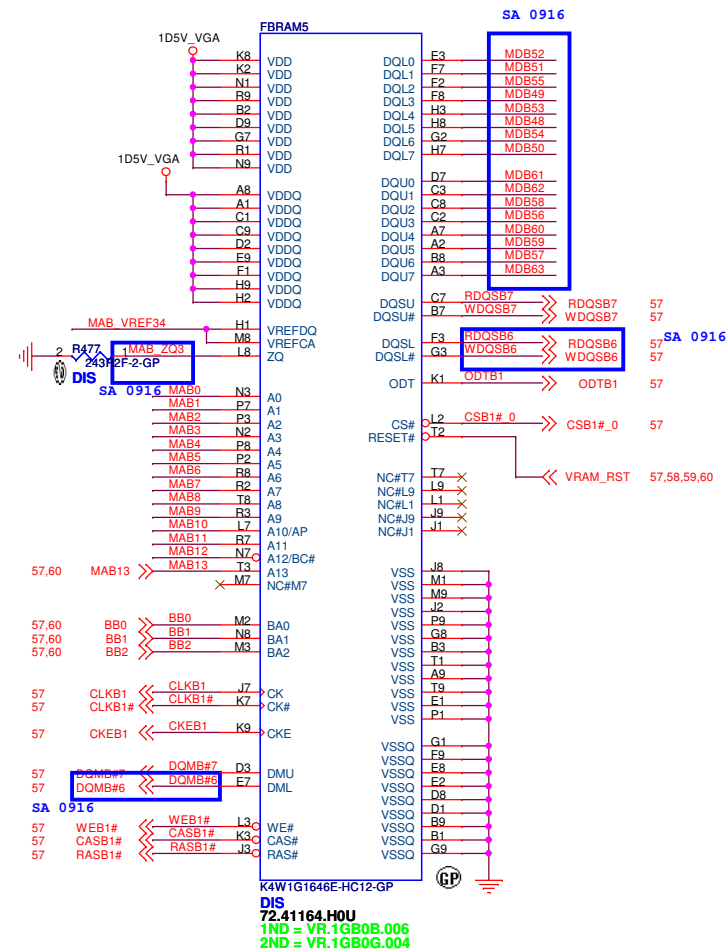


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Title			
VRAM(3/4)			
Size A3	Document Number		Rev -1
JM31-CP			
Date: Thursday, February 25, 2010	Sheet	60 of	62

DDR3



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