

Compal Schematic

HCL51 Schematics Document

Intel Yonah Processor with ATIRC410MD/E + DDRII + SB460M

www.RanAsiaLaptop.com

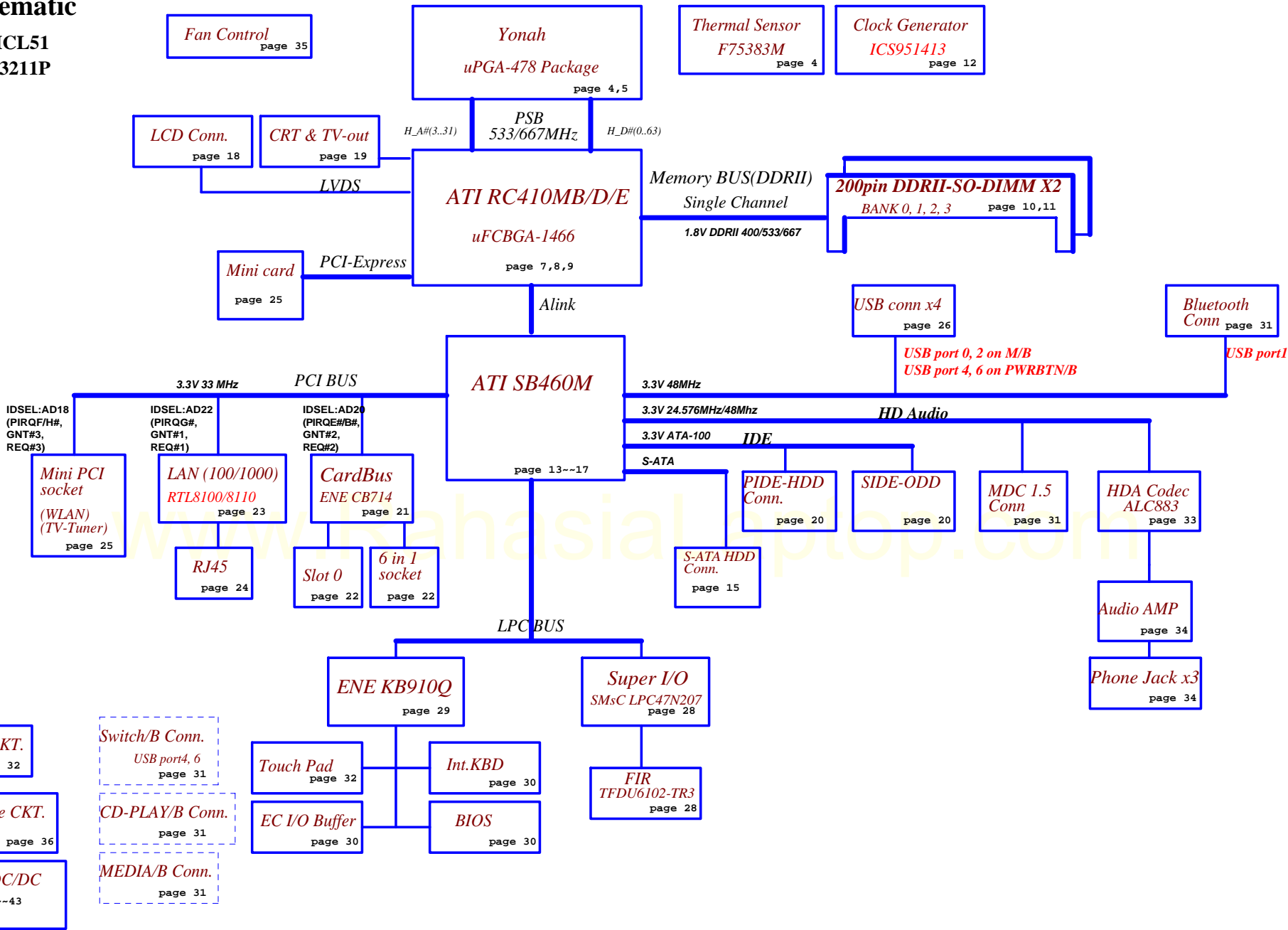
2006-04-05

REV: 1

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Compal Schematic

Model Name : HCL51
File Name : LA-3211P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQE/PIRQH
1394	AD16	0	PIROA
LAN(10/100)	AD22	1	PIRQG
Mini-PCI(WLAN/TV-Tuner)	AD18	3	PIRQF/PORQH

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Fintek F75383M	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

EC SM Bus2 address

SB460M SM Bus address

Device	Address
Clock Generator (ICS951413)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	0.2
2	0.2
3	
4	
5	
6	
7	

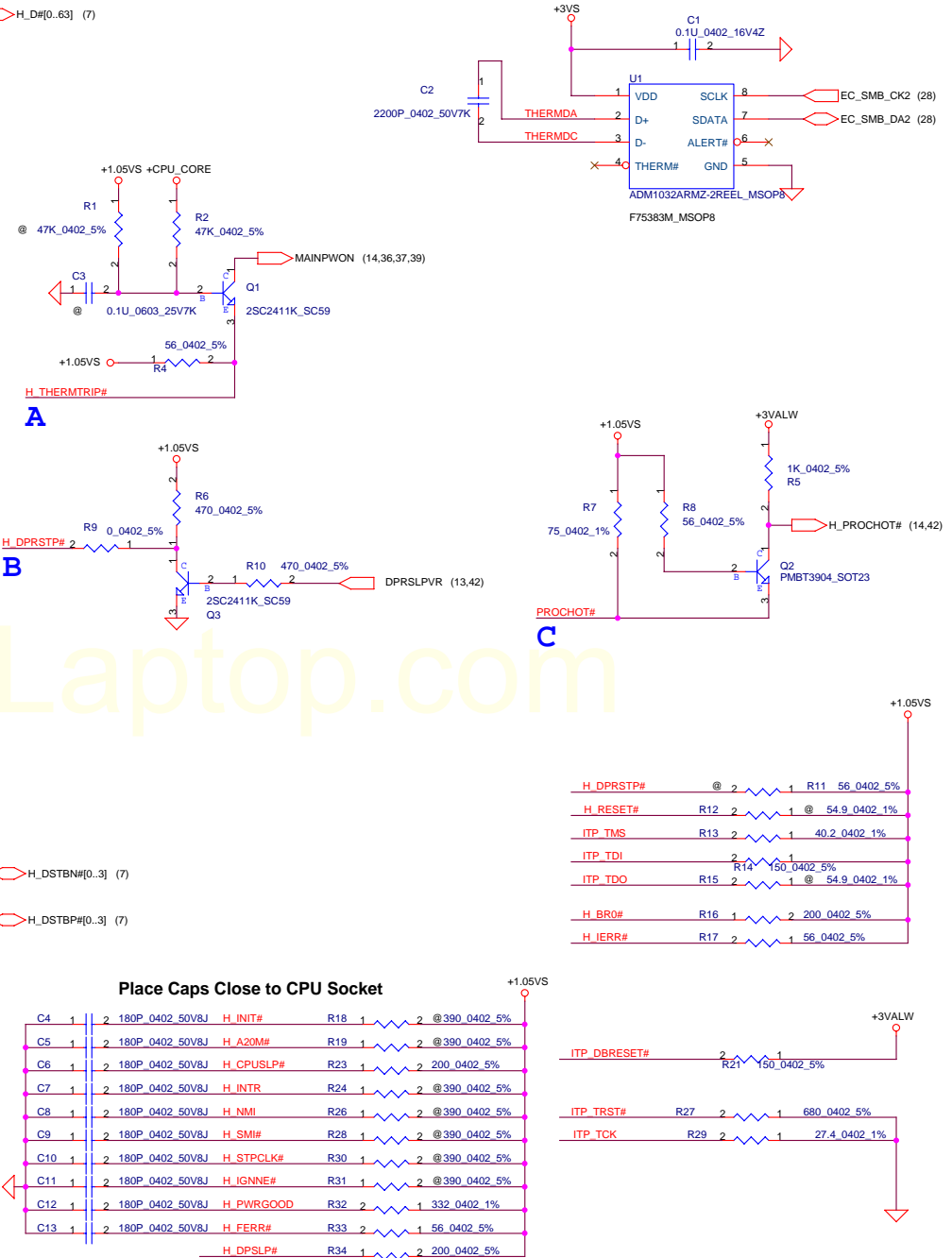
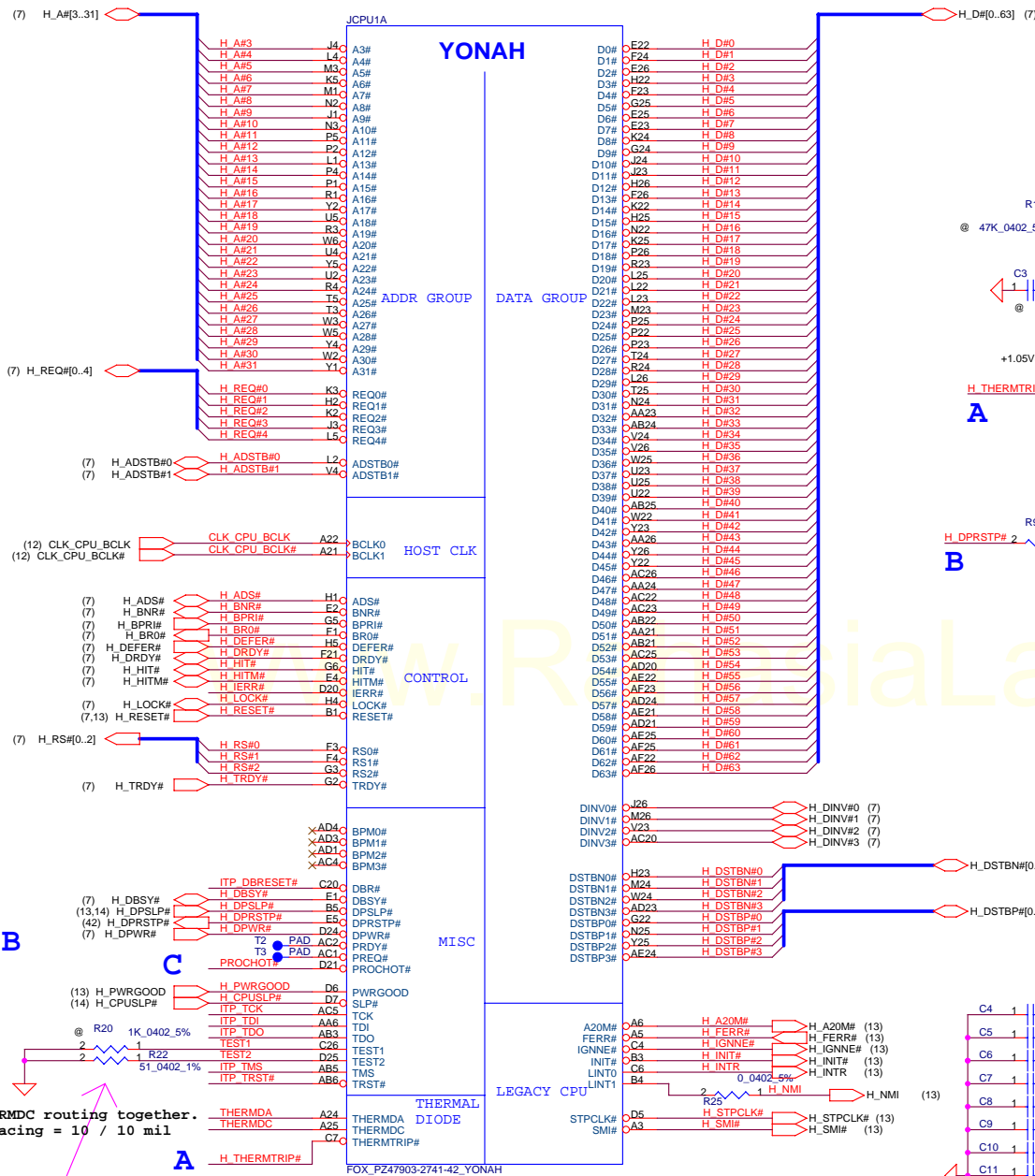
BTO Option Table

BTO Item	BOM Structure
LAN(10/100)	8100C@
LAN(GIGA)	8110S@
FIR	FIR@
MINI_CARD1	MINI1@
SATA HDD	SATA@
CardReader	4IN1@

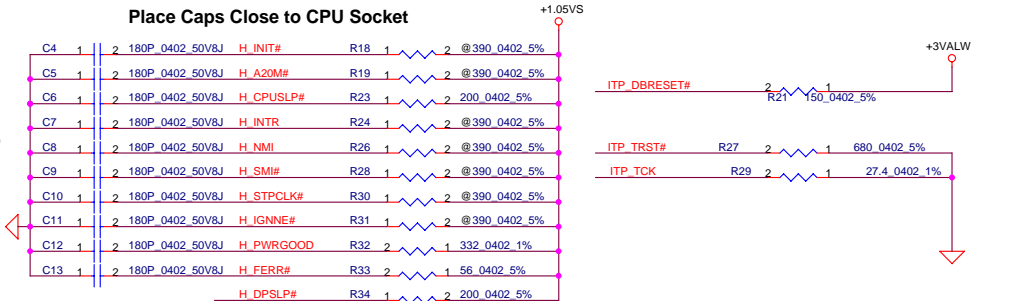
SKU ID Table

SKU ID	SKU
0	
1	
2	
3	
4	
5	
6	
7	

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Place Caps Close to CPU Socket

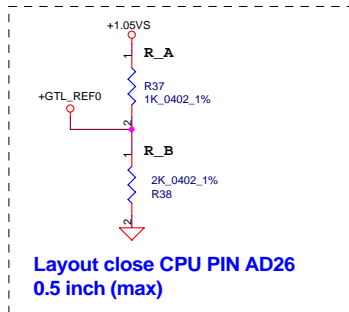


H_THERMDA, H_THERMDC routing together.
Trace width / Spacing = 10 / 10 mil

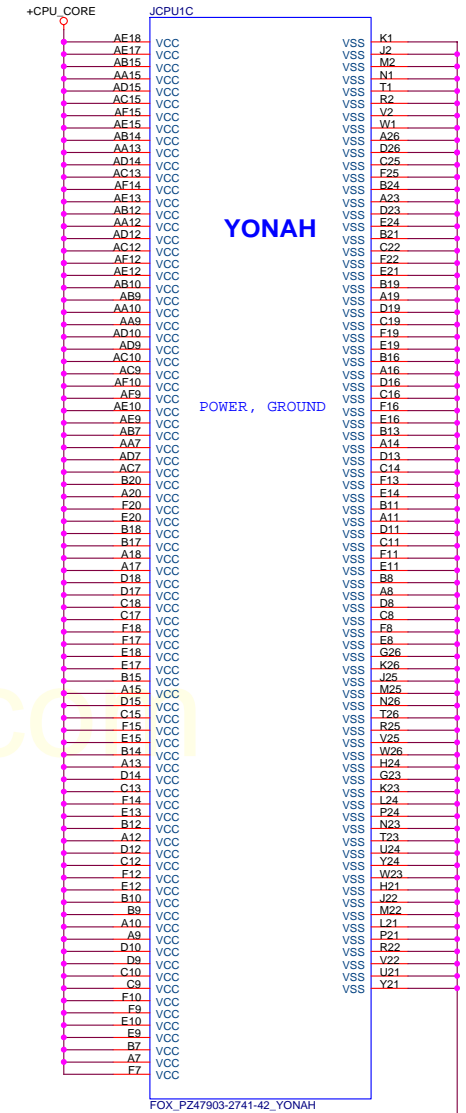
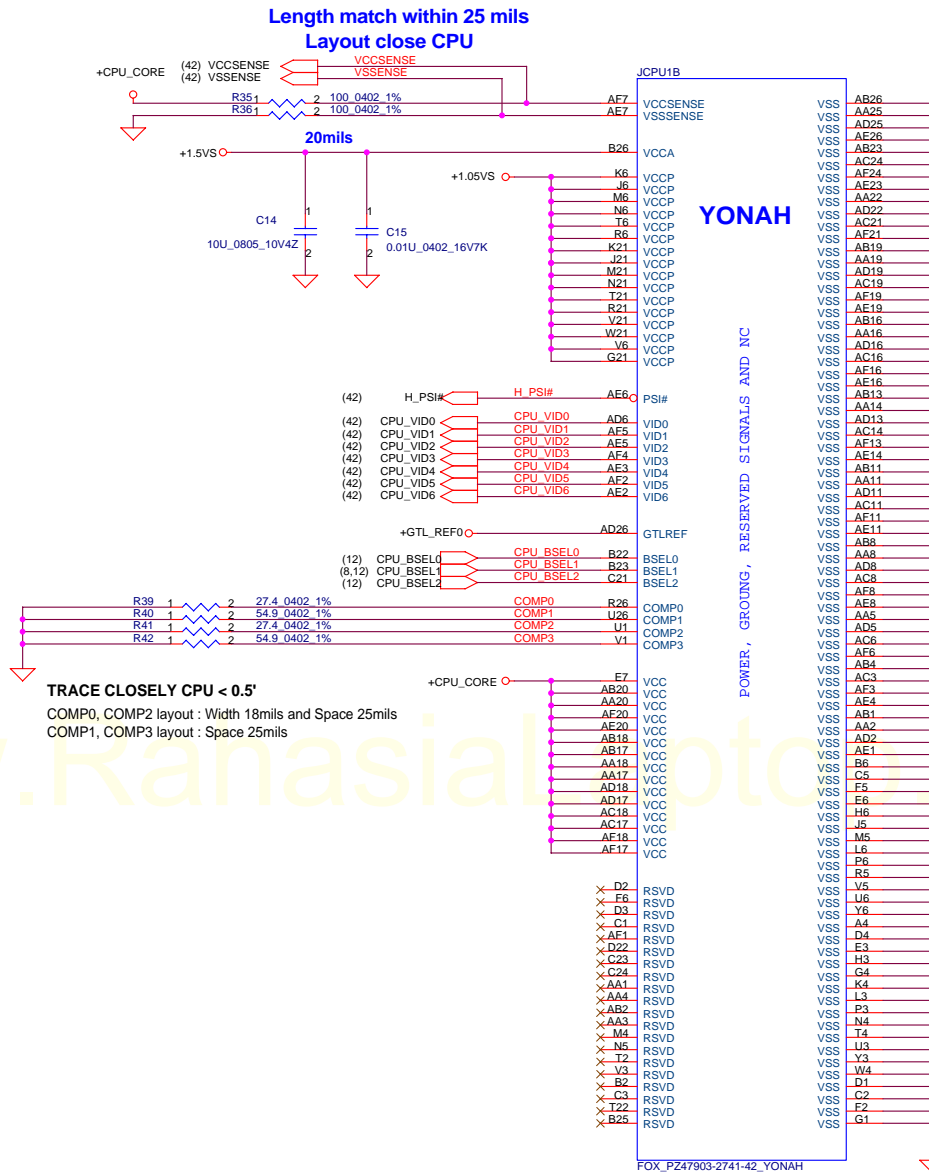
A H_THERMTRIP#

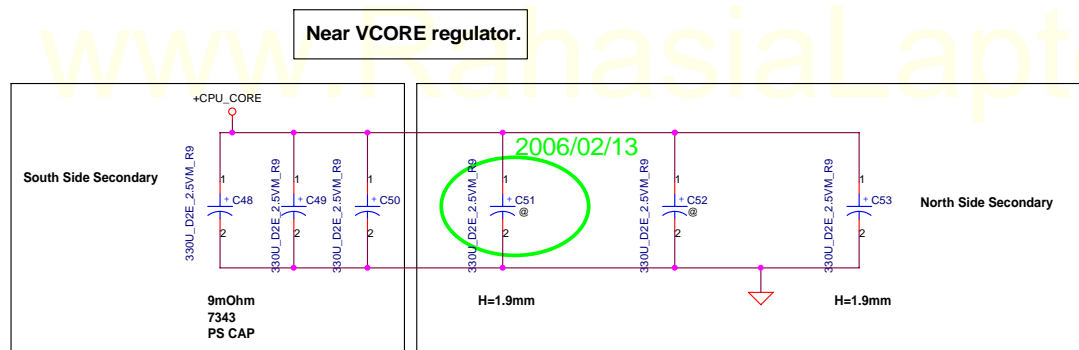
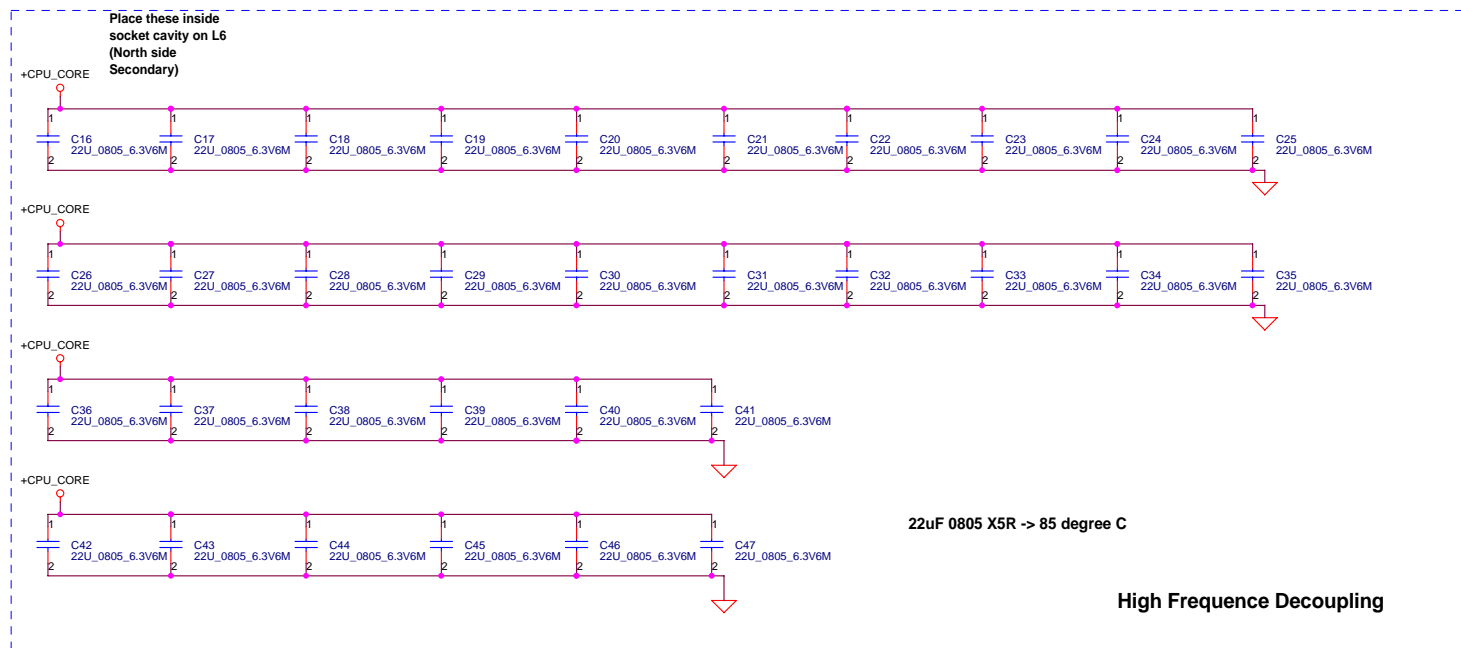
For B-0 stepping engineering samples (ES) of Celeron M processor need to pop this 51 ohm resistor.

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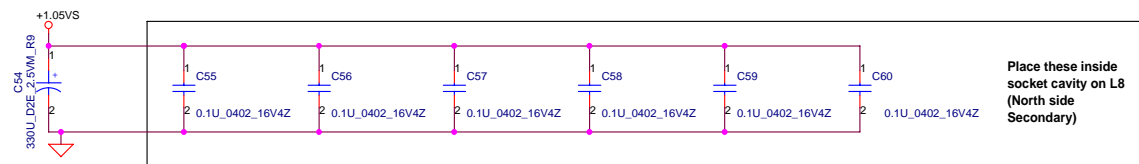


CPU_BSEL	CPU_BSEL0	CPU_BSEL1	CPU_BSEL2
133	0	0	1
166	0	1	1

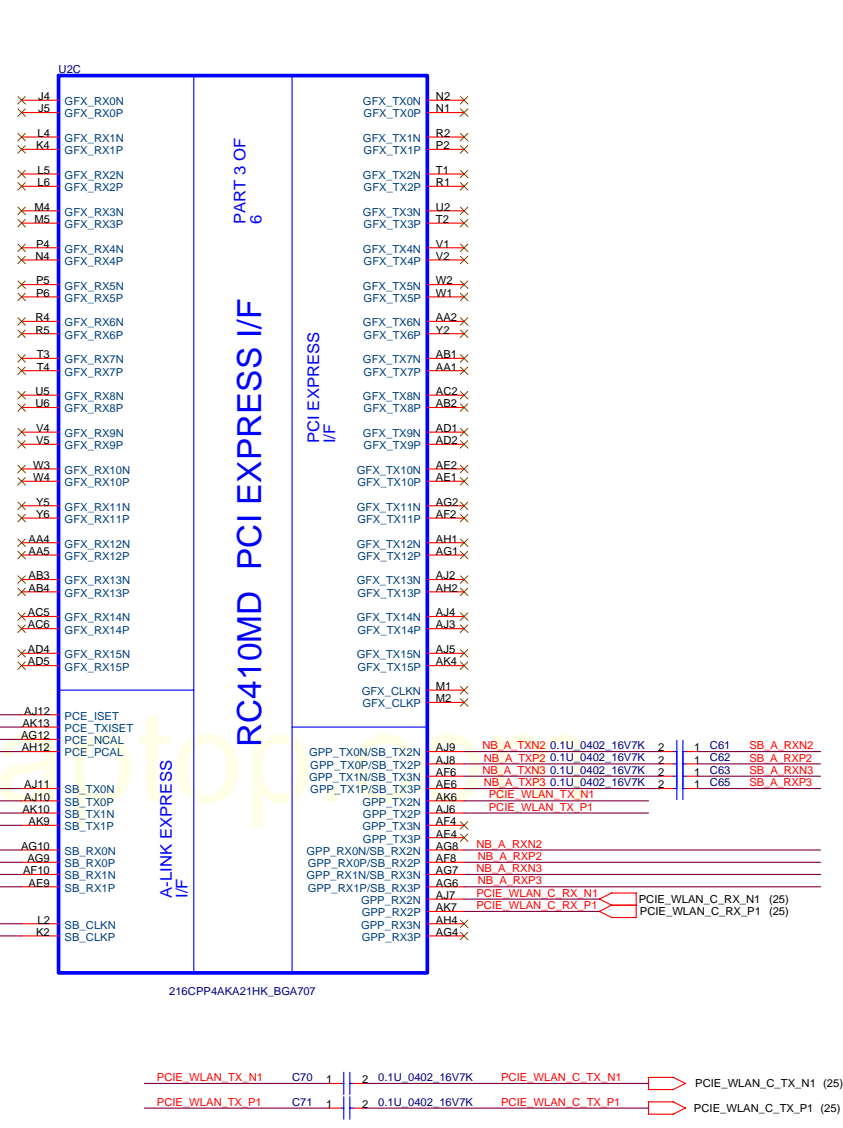
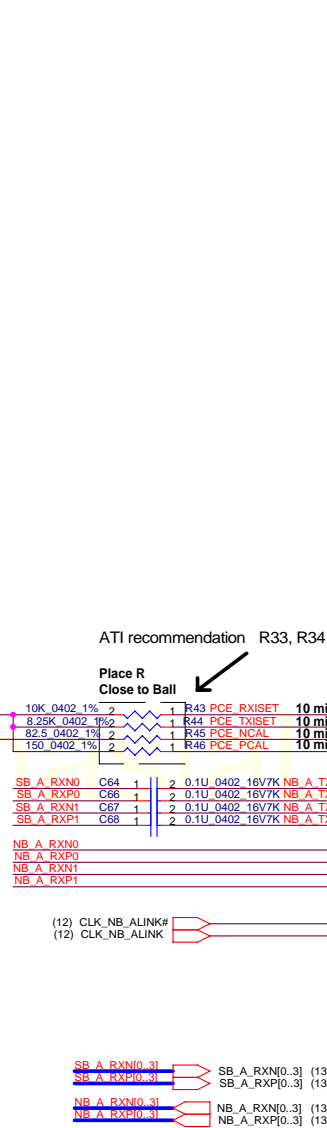
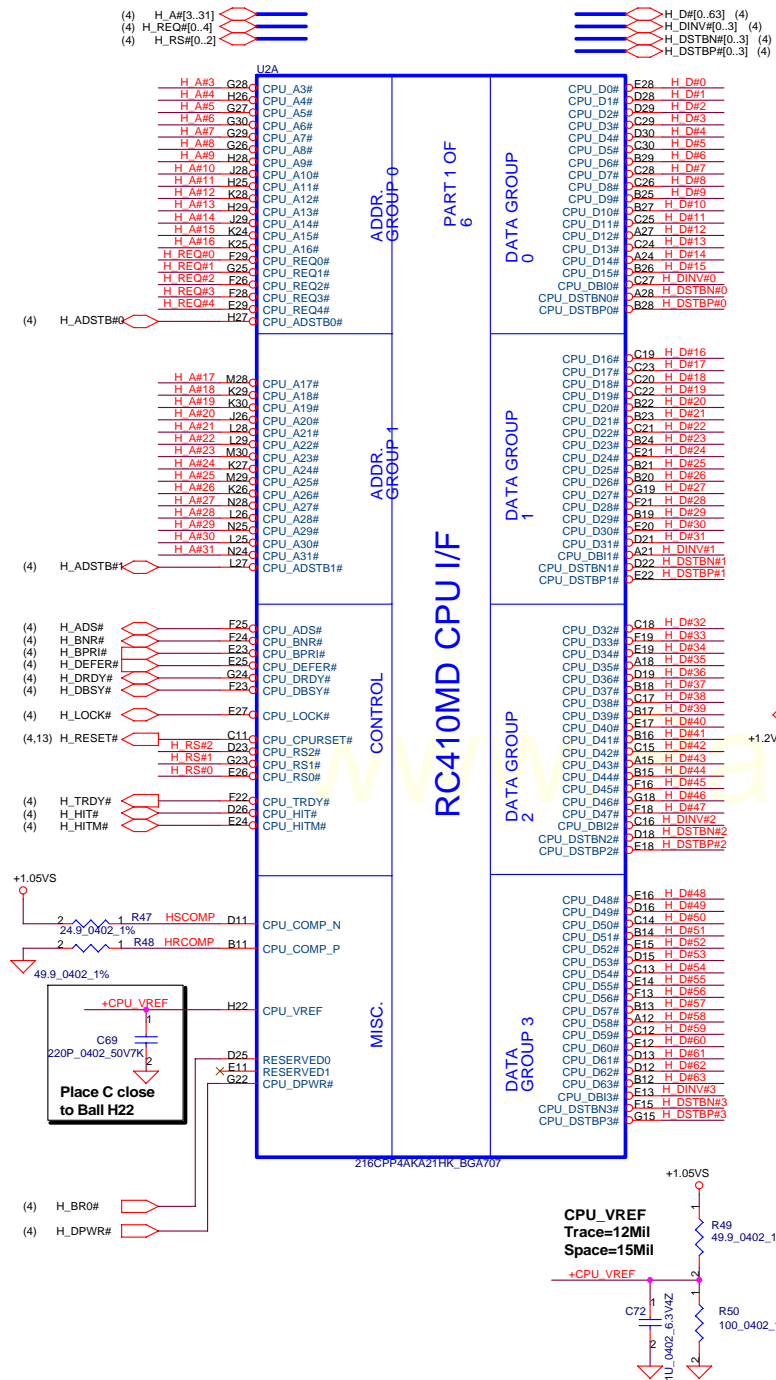




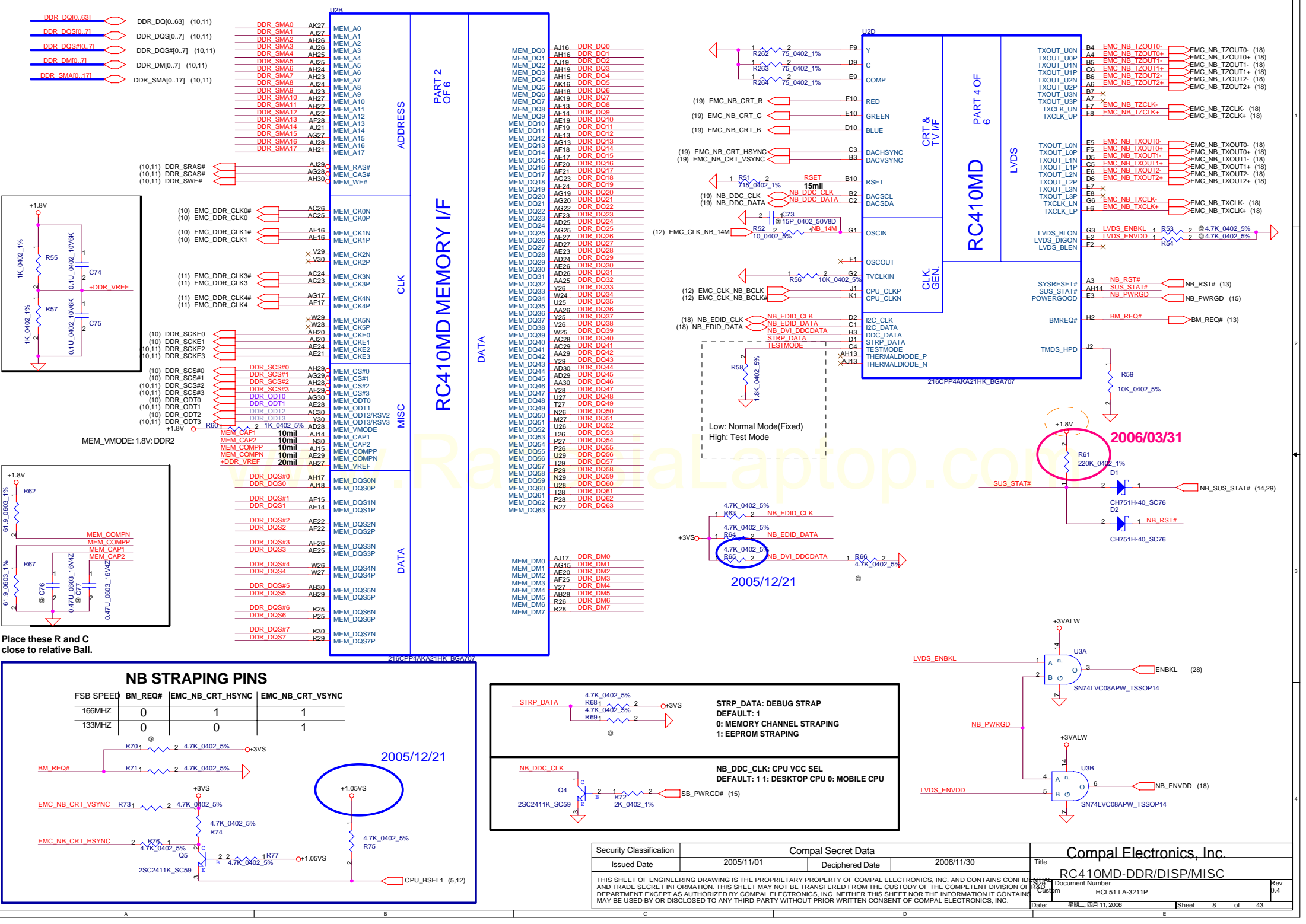
ESR <= 1.5m ohm
Capacitor > 1980uF

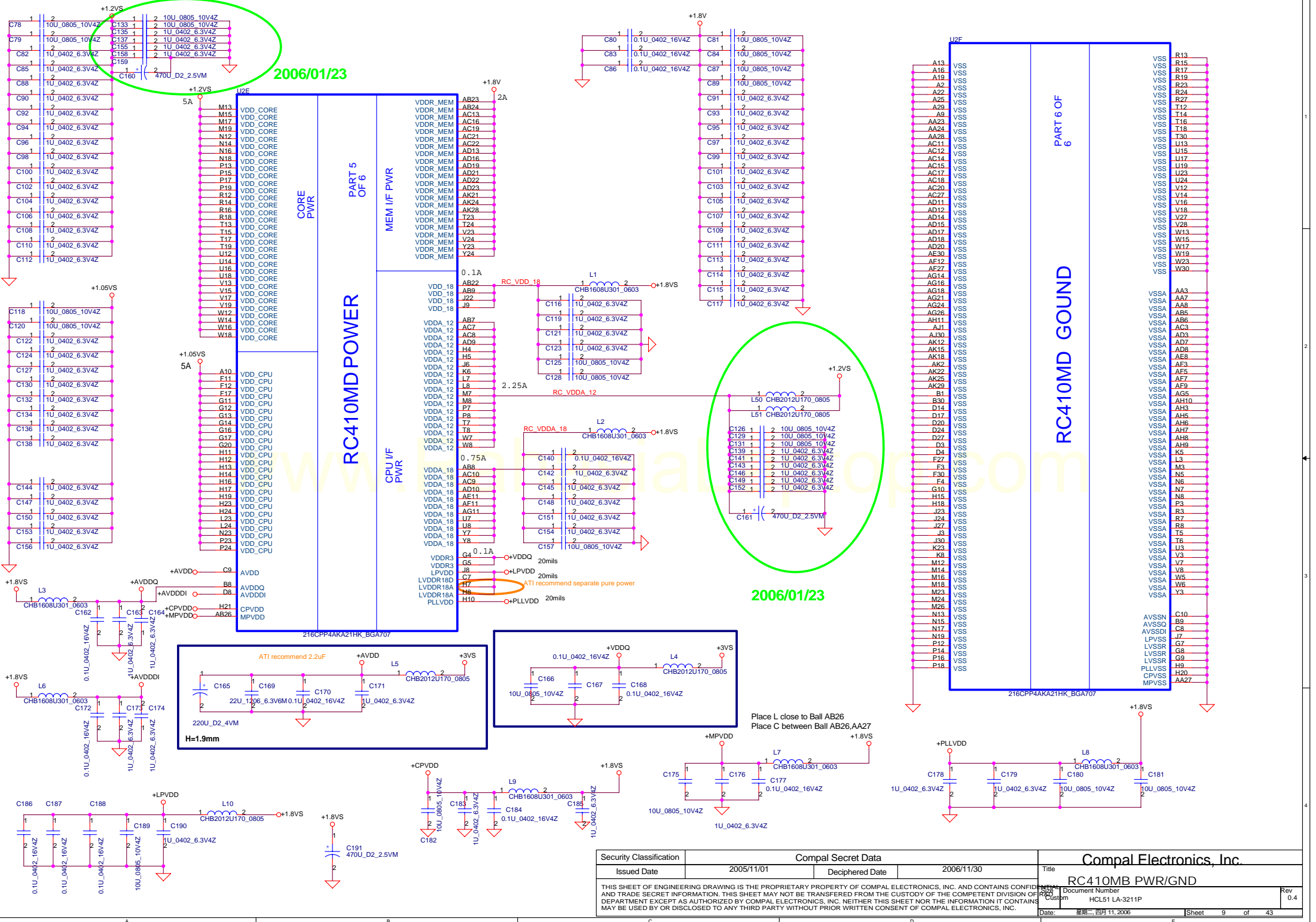


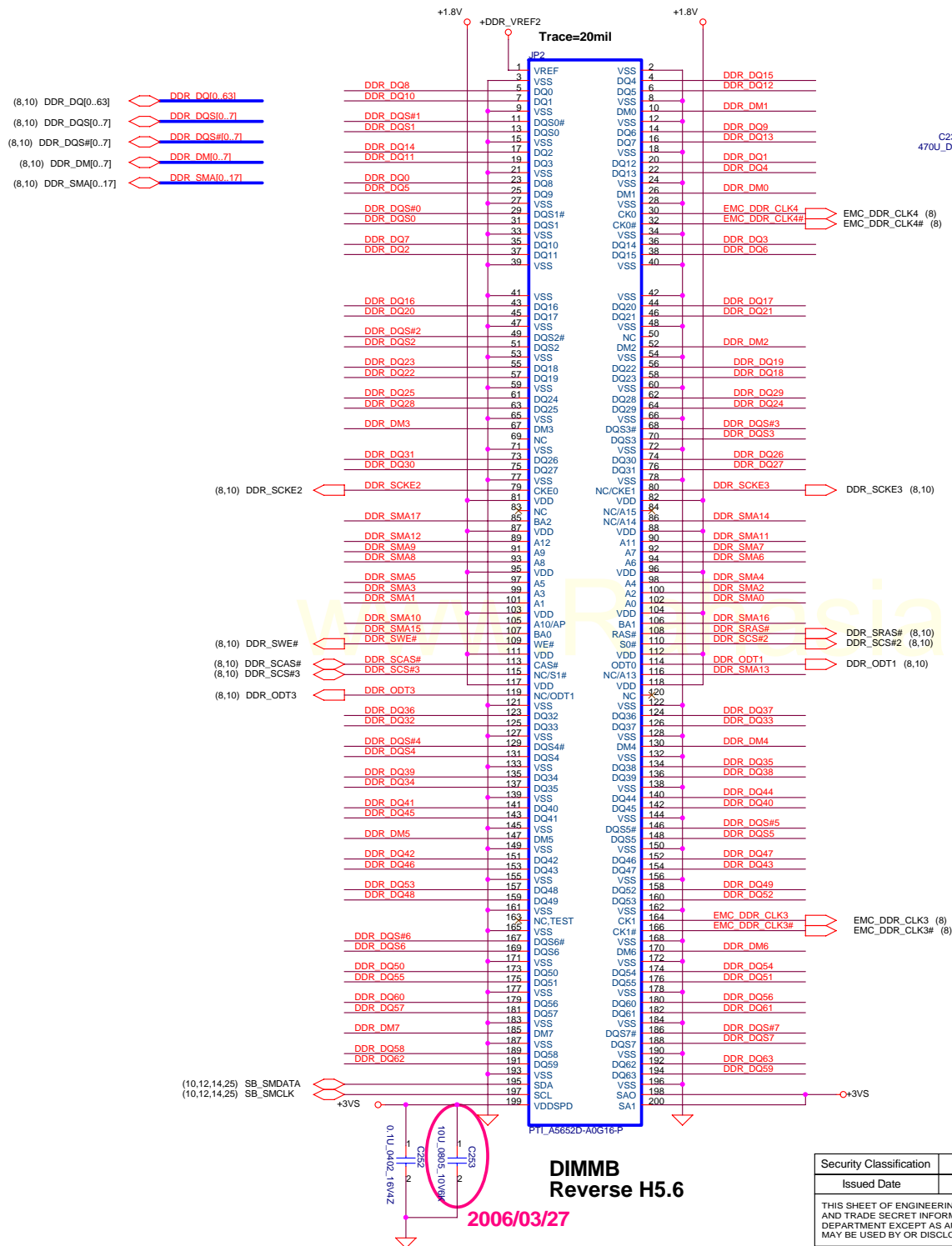
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To SB A-PCIE Link



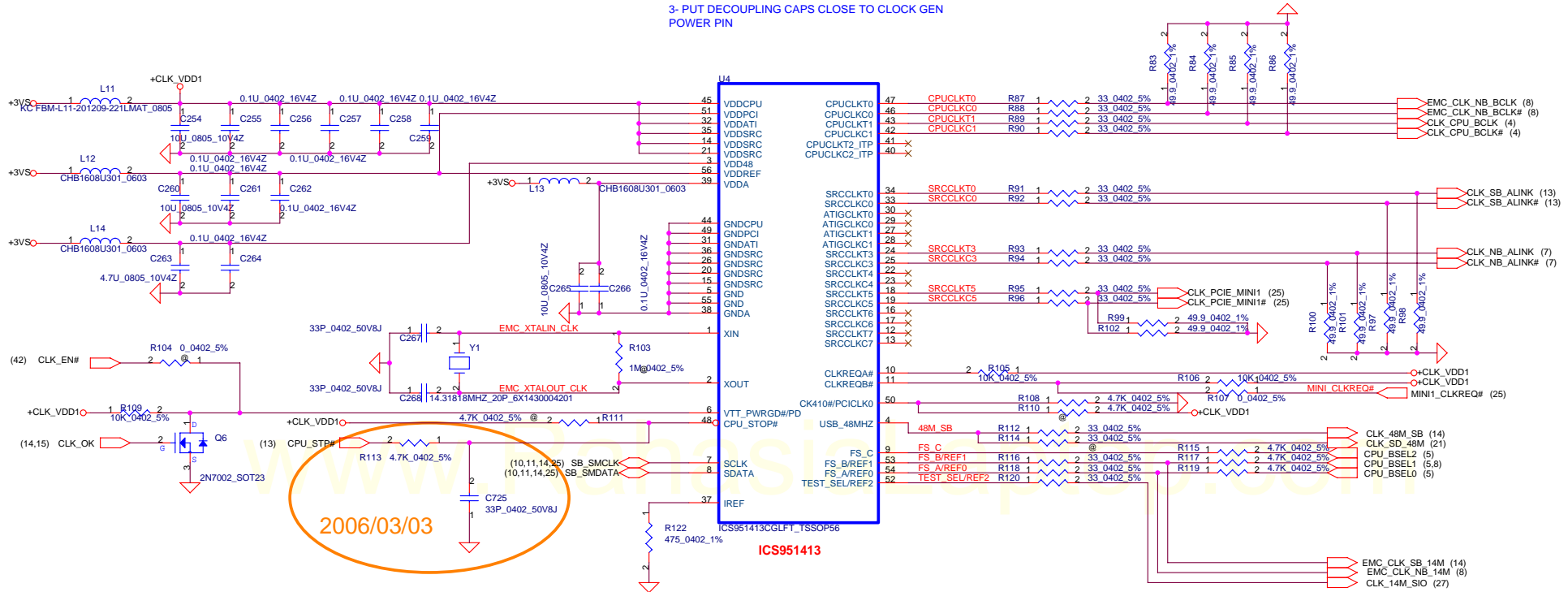




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Clock Generator

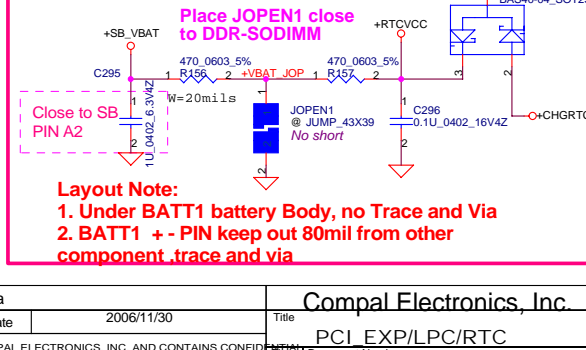
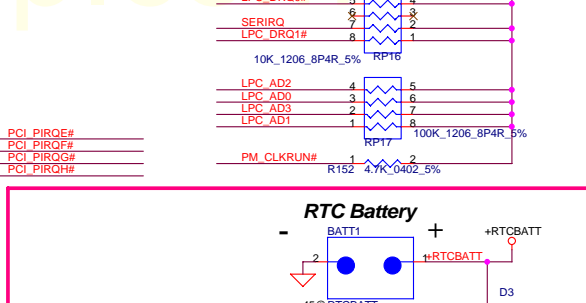
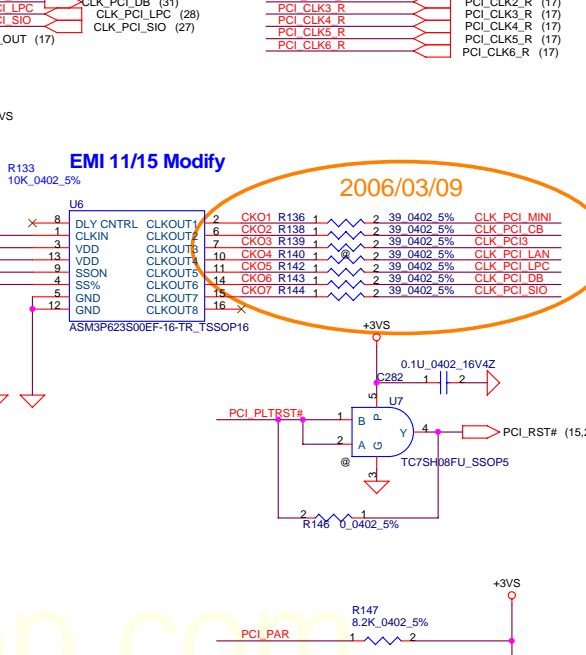
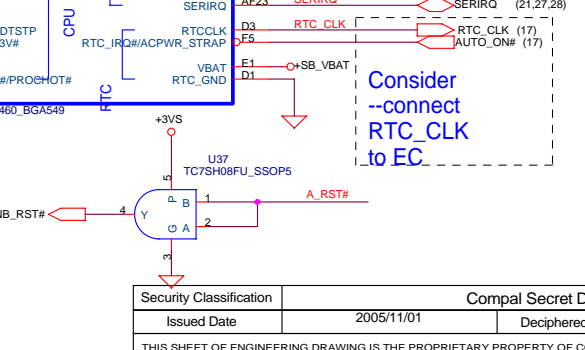
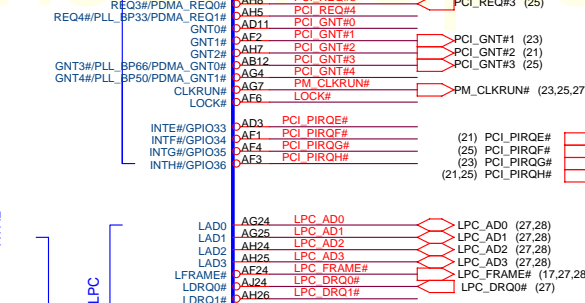
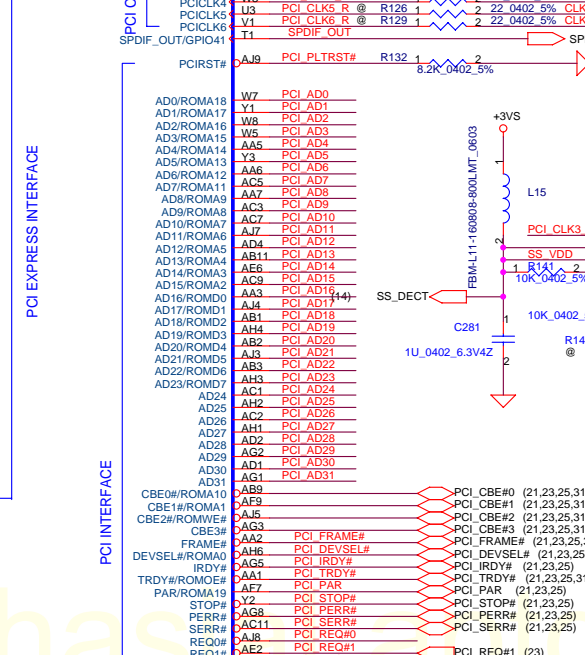
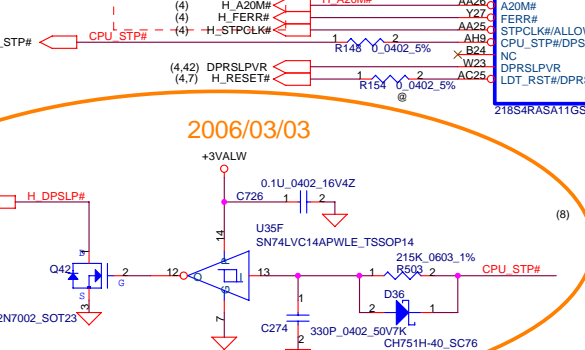
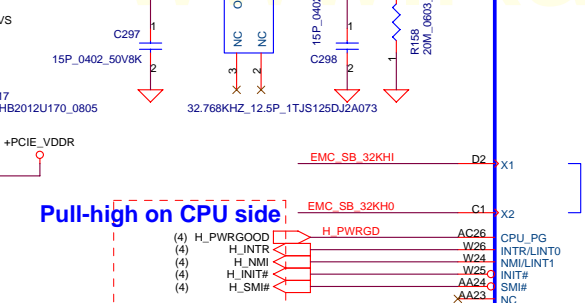
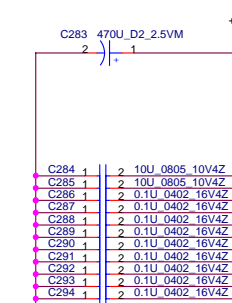
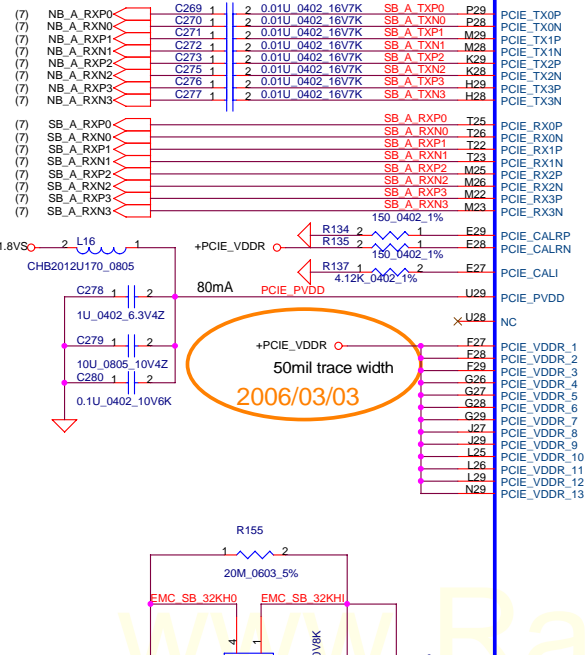
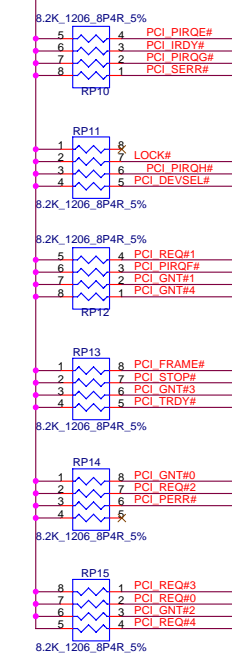
- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO CLOCK GEN AS POSSIBLE
- 2- ROUTE ALL CPUCCLK#, NBCLK#, ITPCLK# AND SRCCLK#, AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO CLOCK GEN POWER PIN



2006/03/03

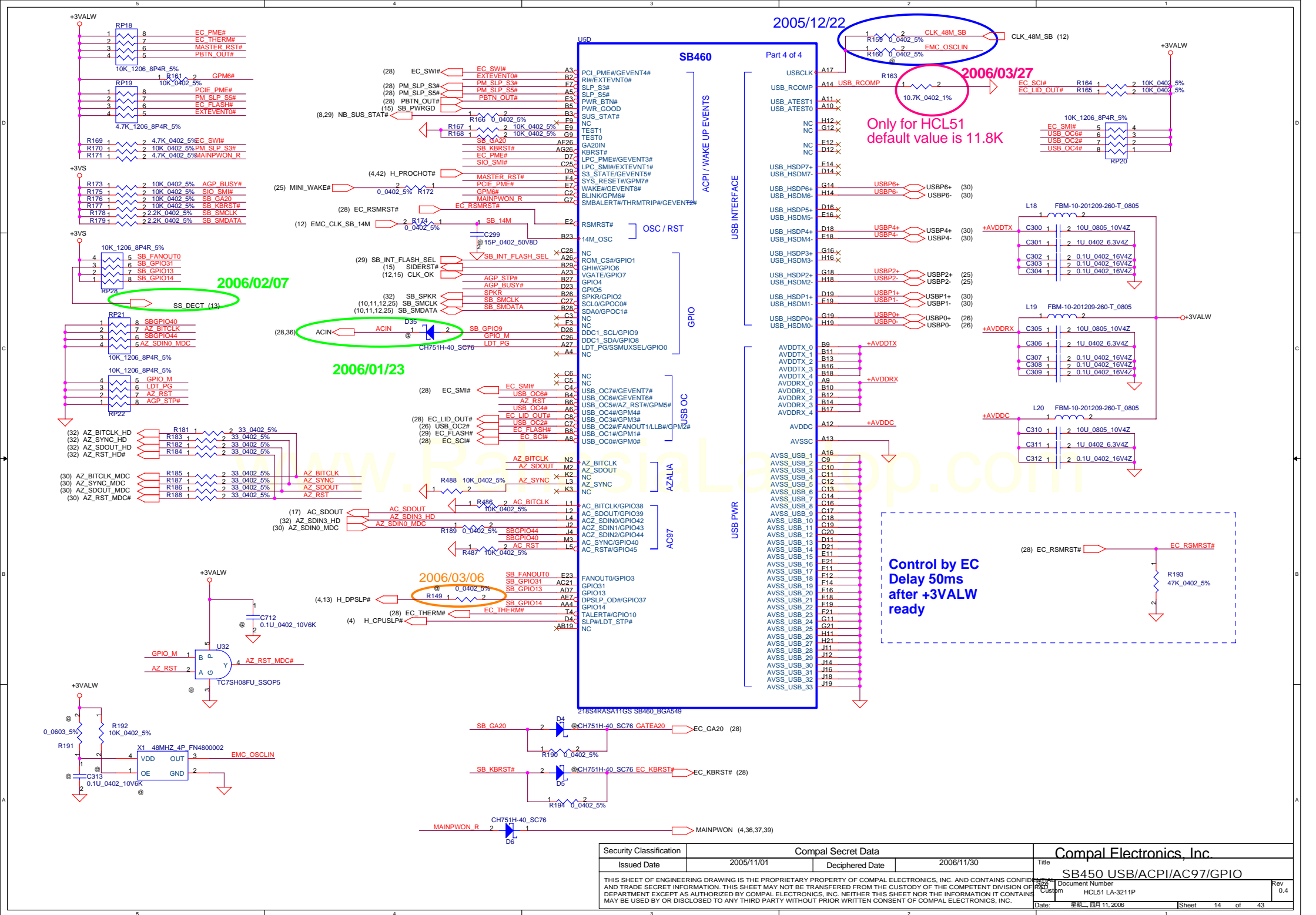
FS_C	FS_B	FS_A	CPU	SRC	PCI	REF	USB
1	0	1	100.00	100.00	33.33	14.318	48.000
0	0	1	133.33	100.00	33.33	14.318	48.000
0	1	1	166.66	100.00	33.33	14.318	48.000

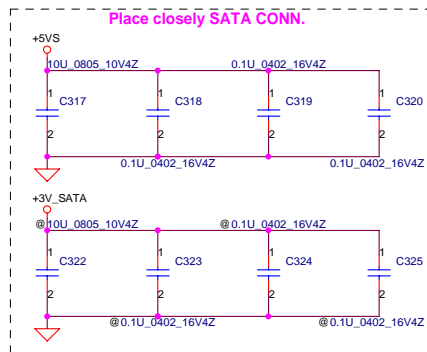
1219 DEL



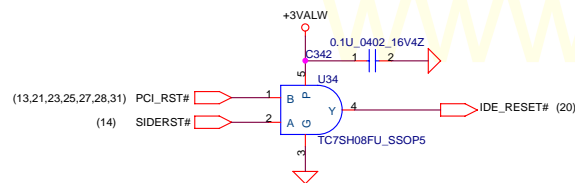
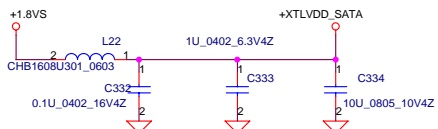
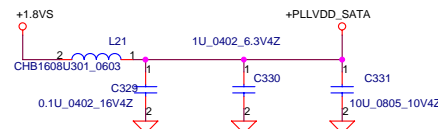
Layout Note:
 1. Under BATT1 battery Body, no Trace and Via
 2. BATT1 +- PIN keep out 80mil from other component, trace and via

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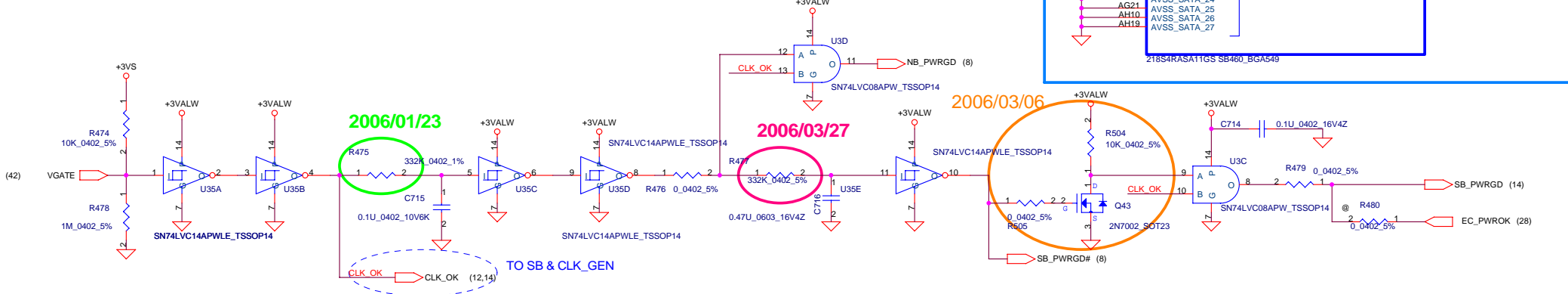




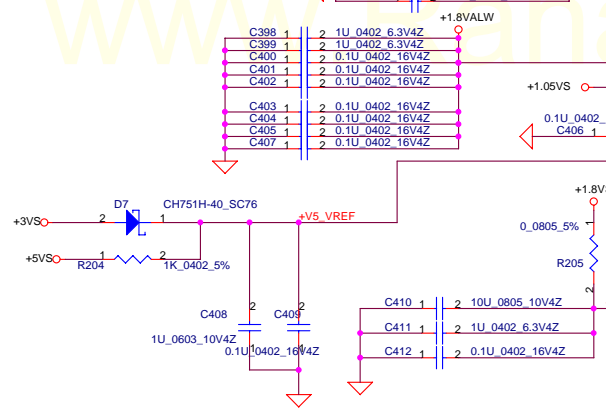
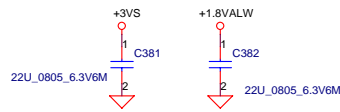
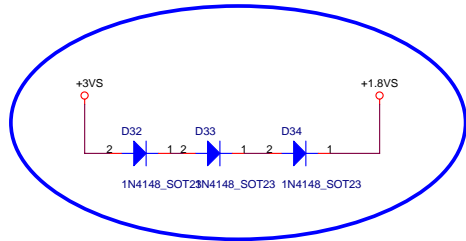
SATA HDD CONNECTOR



NB & SB POWER GOOD

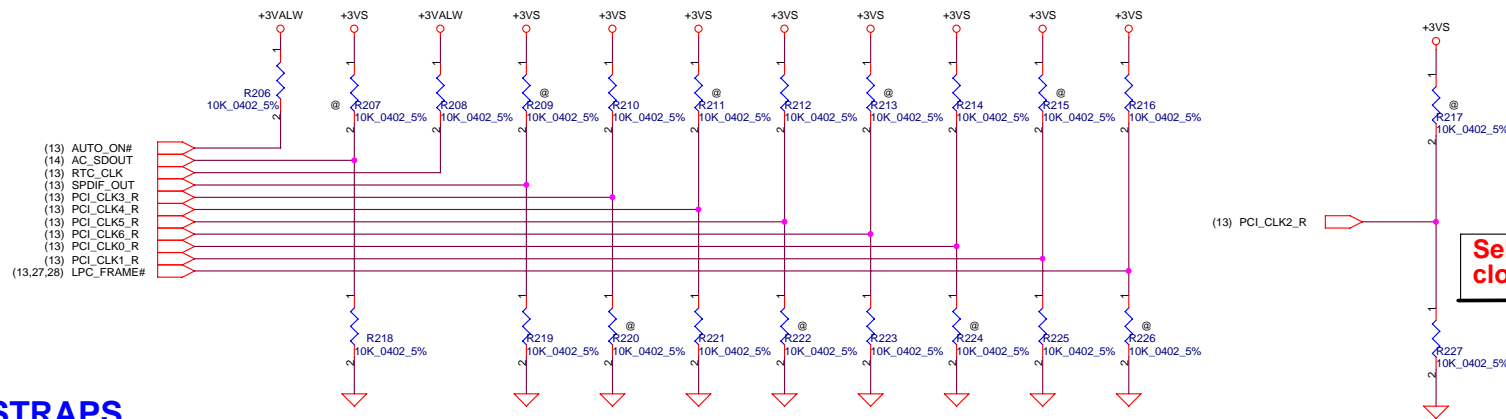


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+V5_VREF (20mils)
+AVDD_CK(40mils)

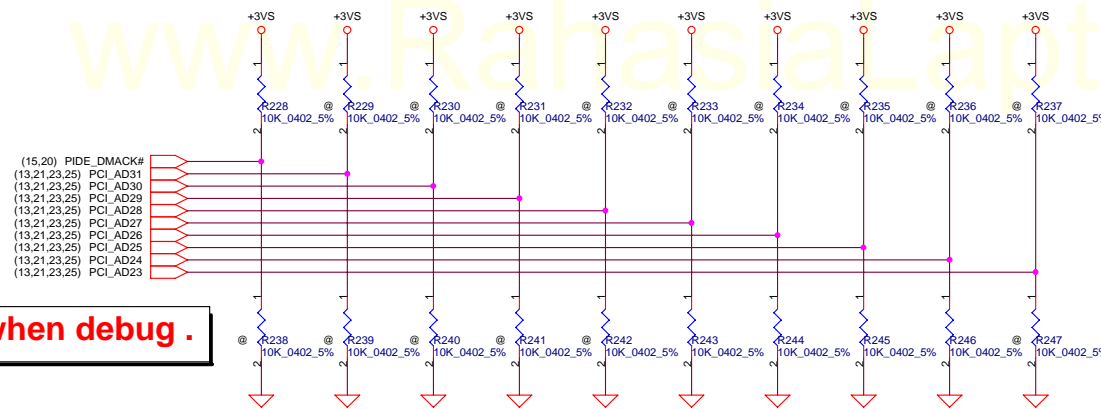
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REQUIRED STRAPS



	AUTO_ON#	AC97_SDO	RTC_CLK	SPDIF_OUT	CLK_PCI3	CLK_PCI4	CLK_PCI5	PCI_CLK6	PCI_CLK0	PCI_CLK1	LFRAME#	CLK_PCI2
PULL HIGH	MANUAL PWR ON	USE DEBUG STRAPS	INTERNAL RTC	PU for 48Mhz XTAL mode	USB PHY PWRDOWN DISABLE	Internal PLL	PCIE AUTO detect	CPU I/F = K8	ROM TYPE H,H = PCI ROM	H,L = LPC ROM I L,L = FWH ROM	THERMTRIP# ENABLE	Crystal Pad
	DEFAULT		DEFAULT		DEFAULT		DEFAULT		DEFAULT			
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	48M OSC mode DEFAULT	USB PHY PWRDOWN ENABLE	External Clock DEFAULT	Forcing PCIE to 2 lanes (debug only)	CPU I/F = P4 DEFAULT			THERMTRIP# DISABLE	Clock input buffer DEFAULT

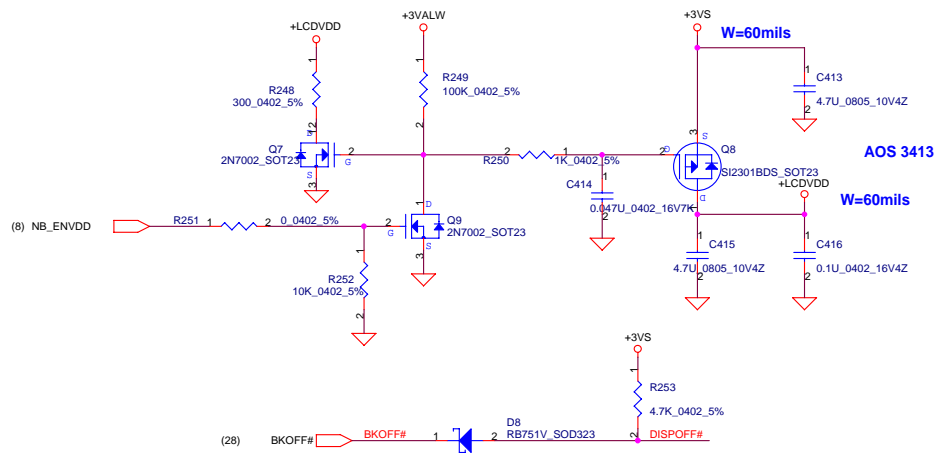


Pop R634 when debug .

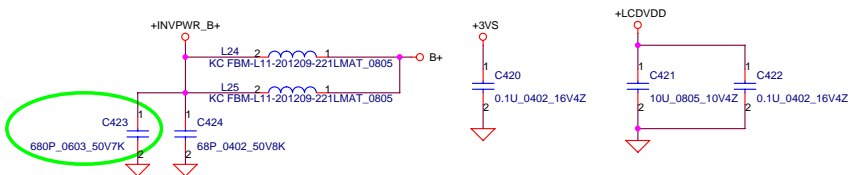
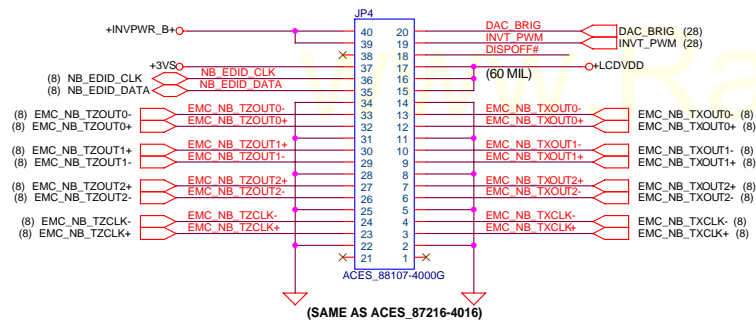
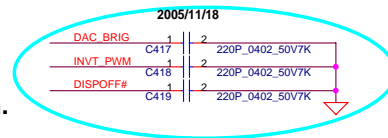
DEBUG STRAPS

	PIDE_DMACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Reserved	Reserved	Reserved	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
PULL LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS	

LCD POWER CIRCUIT

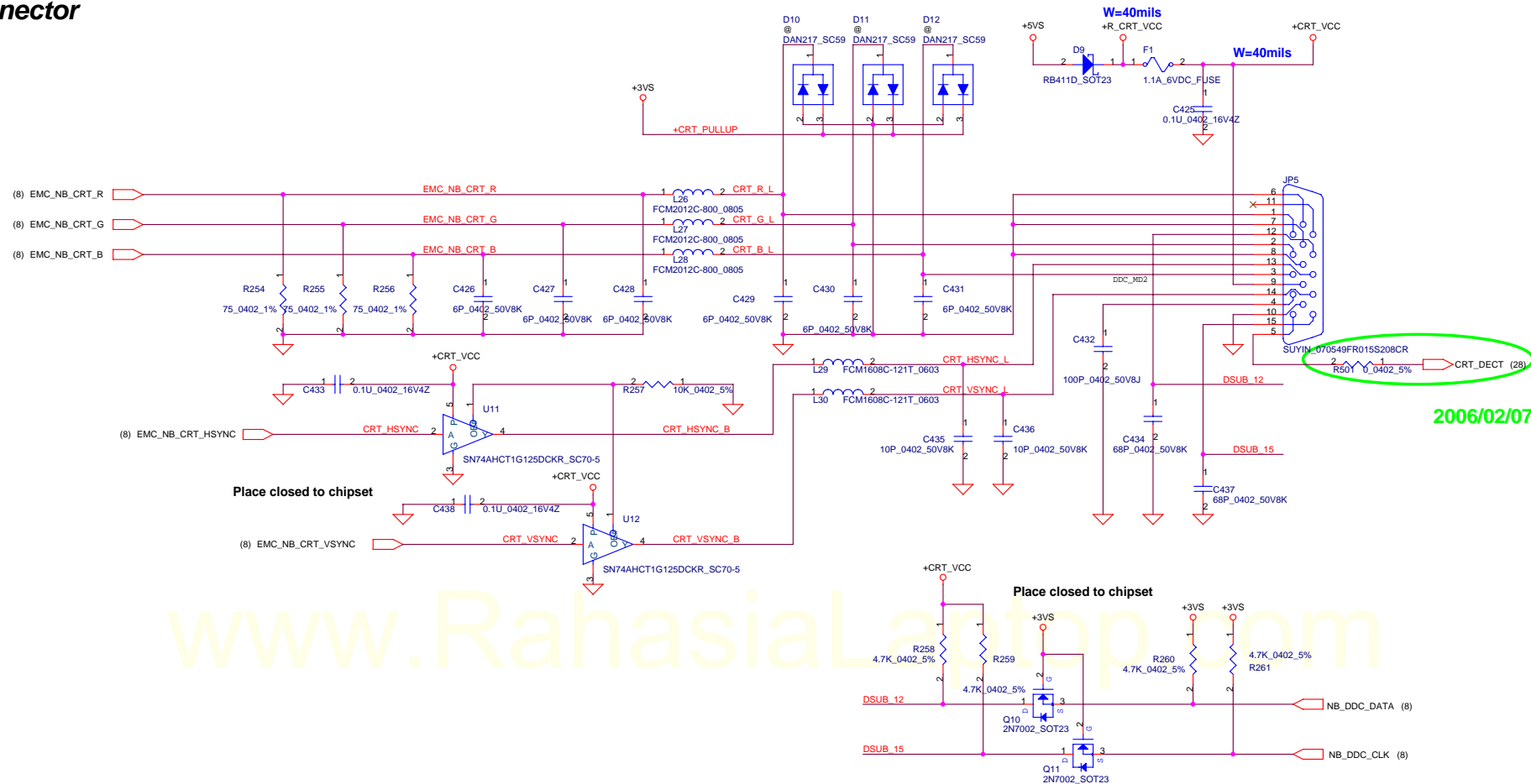


LCD/PANEL BD. Conn.

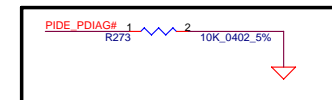
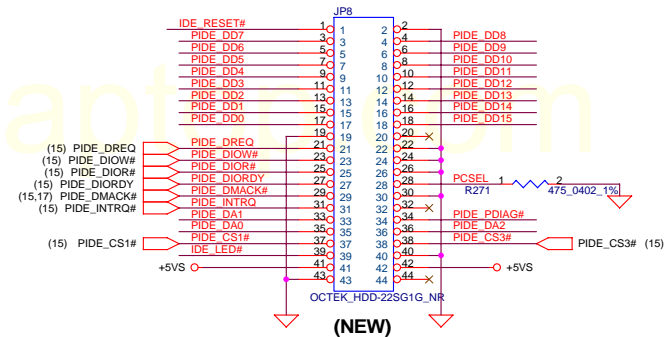
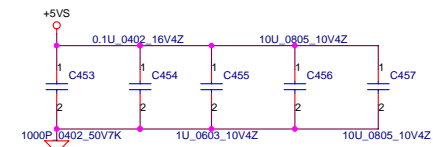


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			Document Number	
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			Date: 星期二 四月 11, 2006	Sheet 18 of 43

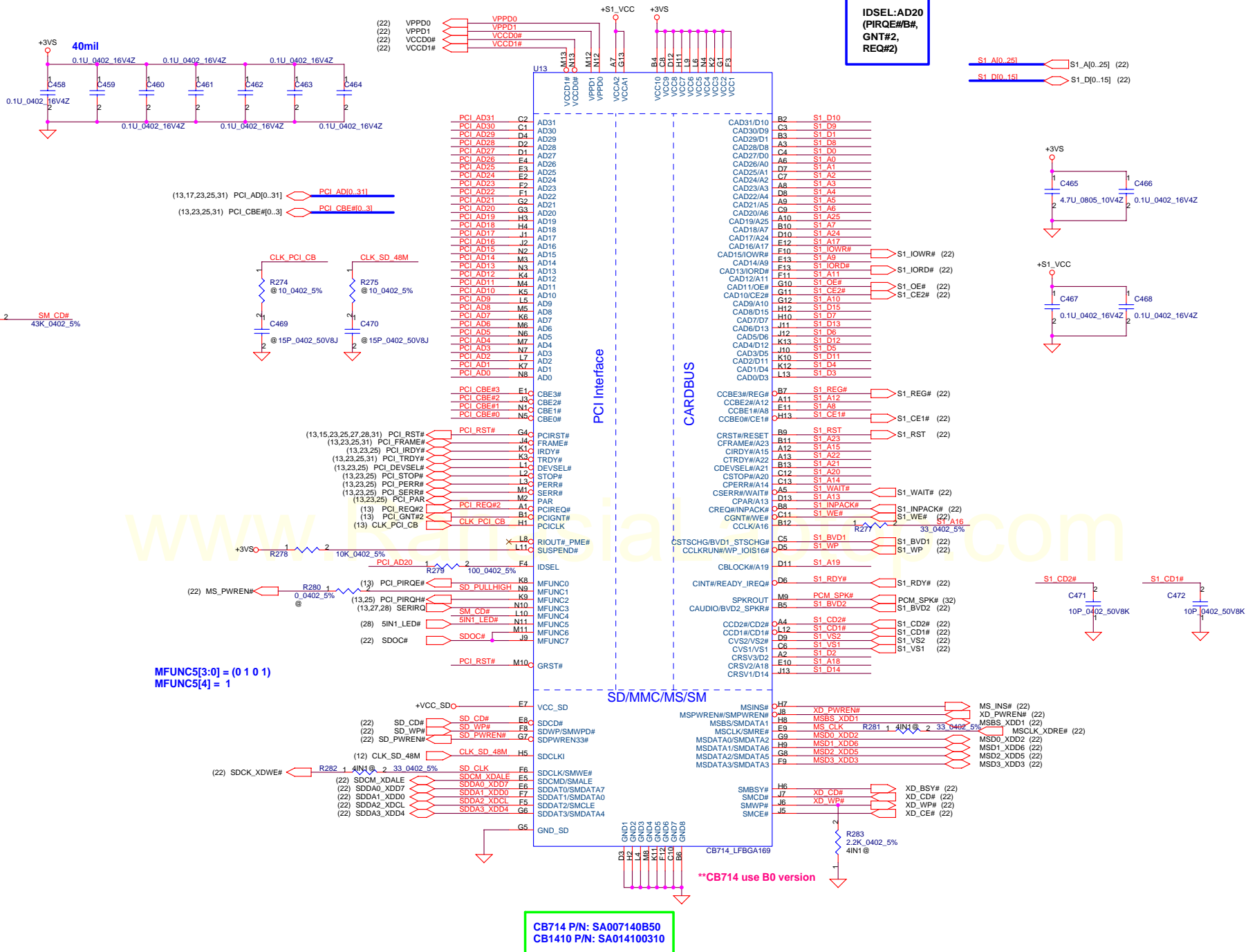
CRT Connector



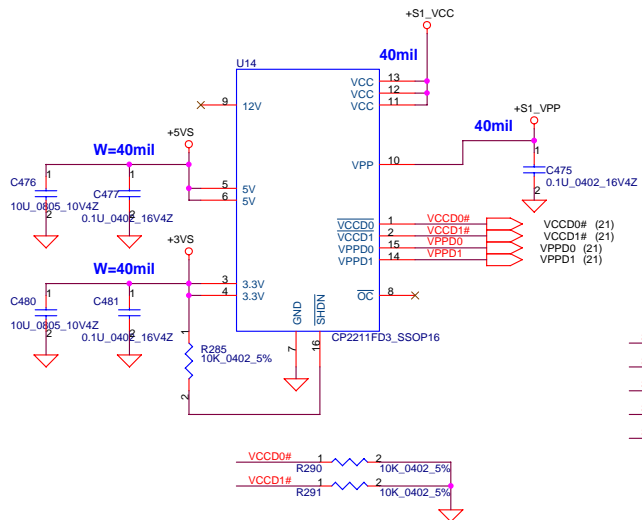
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2005/06/20	Deciphered Date	2006/06/20	
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			CRT & TV-OUT Connector	HCL51 LA-3211P
			Date: 星期二, 四月 11, 2006	Rev 0.4
			Sheet 19	of 43



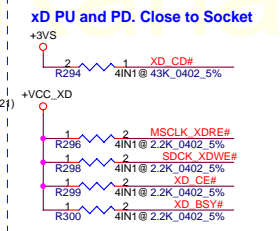
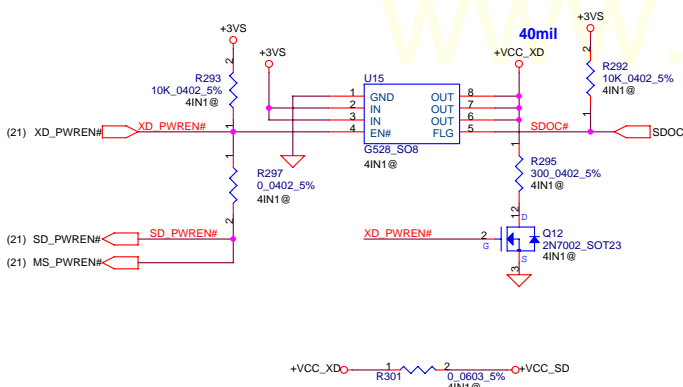
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date		2005/06/20	Deciphered Date	2006/06/20	Title	
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					Document Number	
					HCL51 LA-3211P	
Date: 星期二, 四月 11, 2006					Sheet 20 of 43	
					Rev 0.4	



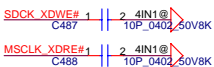
PCMCIA Power Control



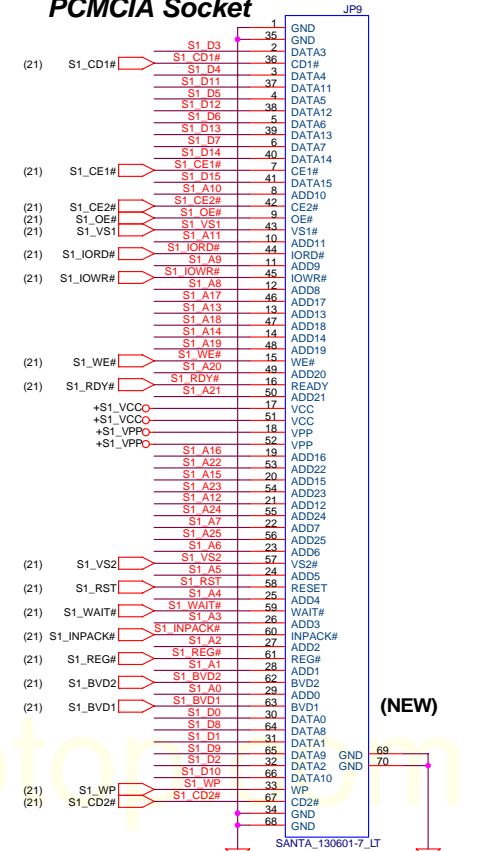
SD/MS Power Control
XD Power Control



Reserve for SD,M
Close to Socket

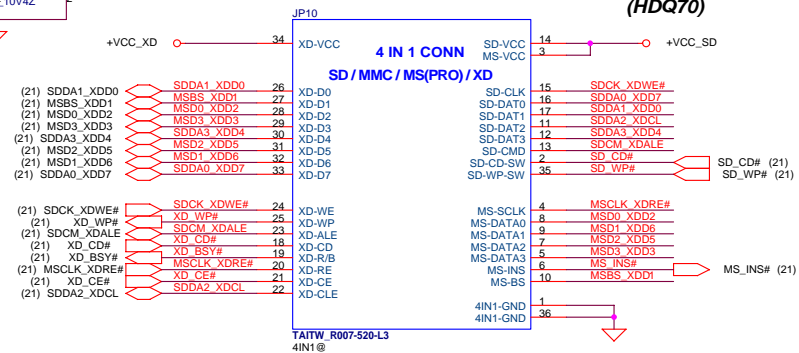


PCMCIA Socket



(NEW)

4 IN 1 Socket
(HDQ70)

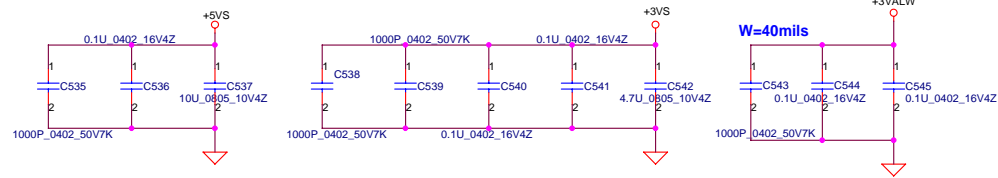


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2005/06/20	Deciphered Date	2006/06/20	Title	PCMCIA Socket
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				HCL51 LA-3211P	0.4
Date: 星期二, 四月 11, 2006		Sheet		22	of 43

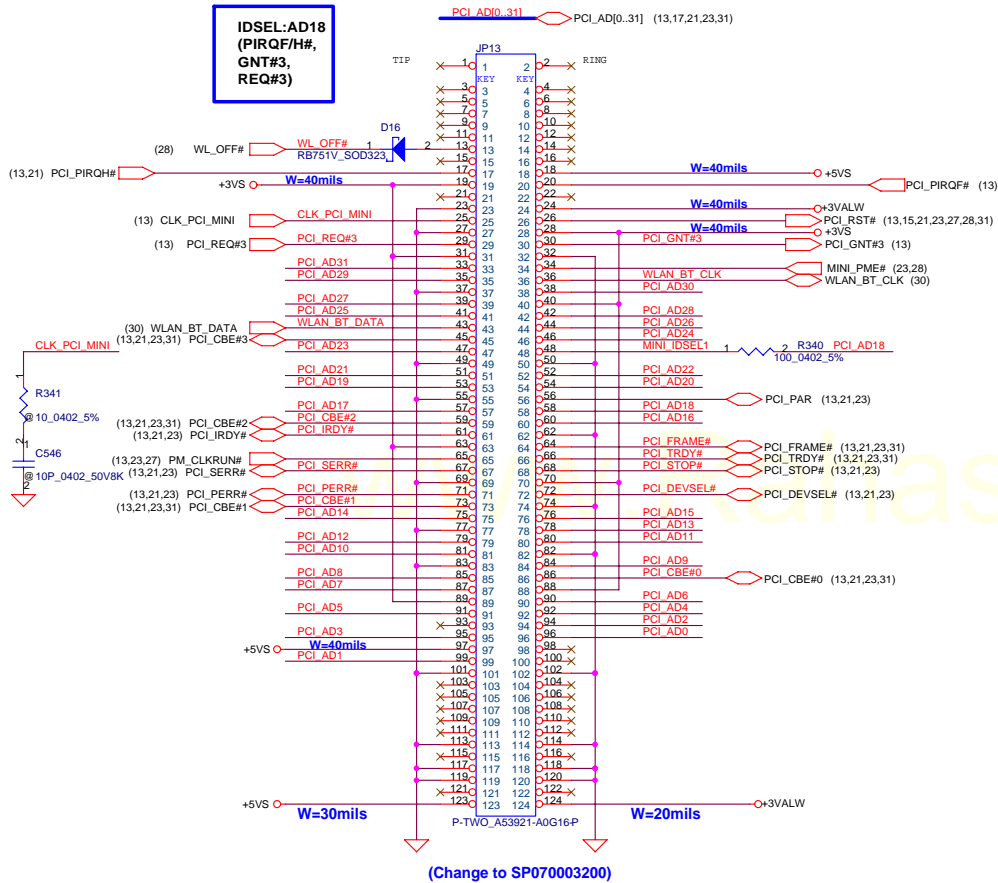
www.RahasiaLaptop.co



Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date		2005/07/29	Deciphered Date	2006/07/29	Title	LAN Magnetic & RJ45/RJ11	
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						HCL51 LA-3211P	0.4
					Date:	星期二, 四月 11, 2006	
					Sheet	24	of 43

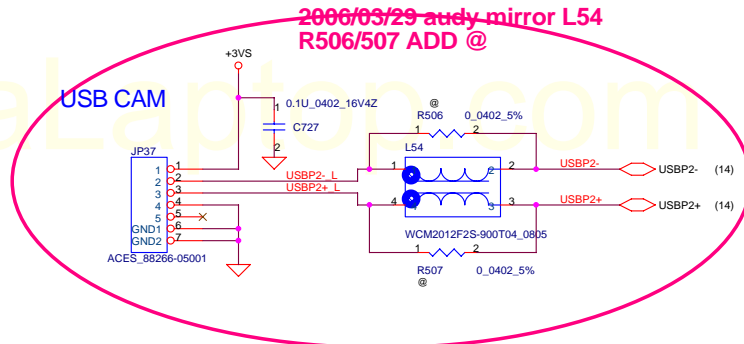
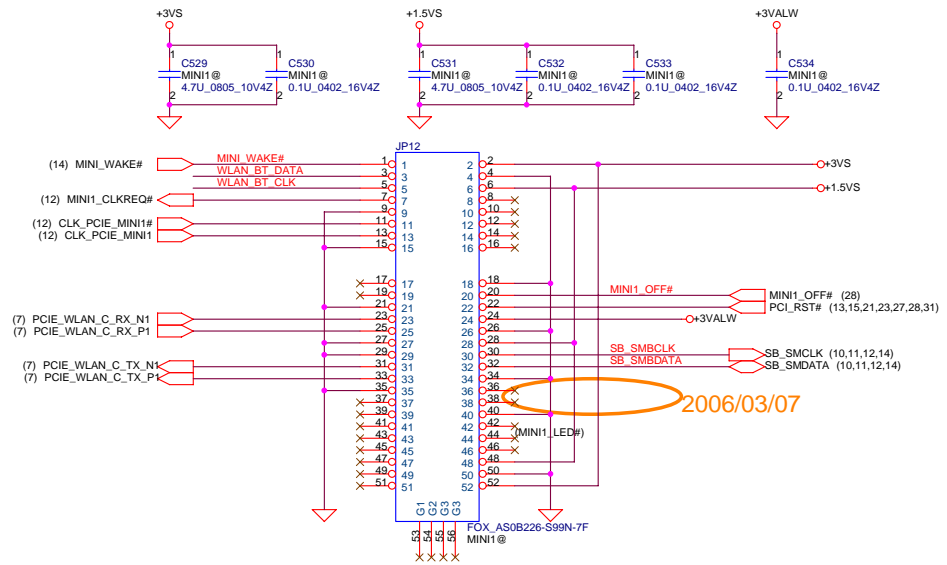


**IDSEL:AD18
(PIRQF/H#,
GNT#3,
REQ#3)**

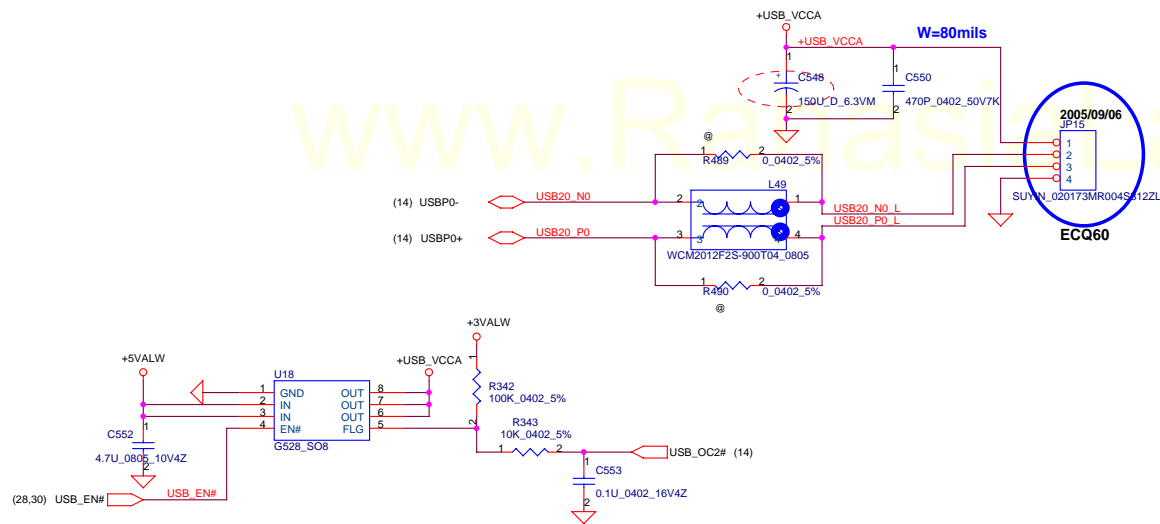


(Change to SP070003200)

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



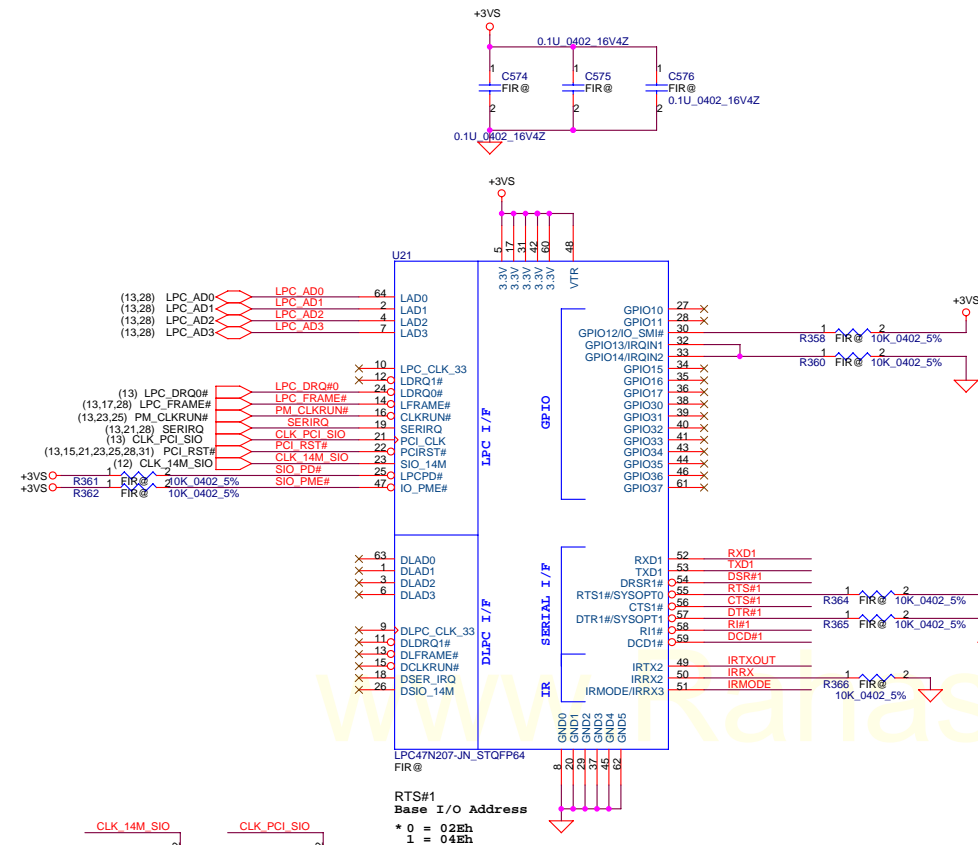
USB CONN. 1 & 2



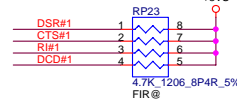
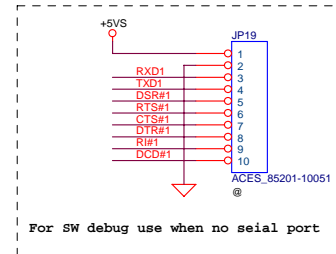
1207 DEL

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Issued Date	2005/06/20	Deciphered Date	2006/06/20	Title	NEW CARD SOCKET
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				Date	2006/04/11
				Sheet	26 of 43
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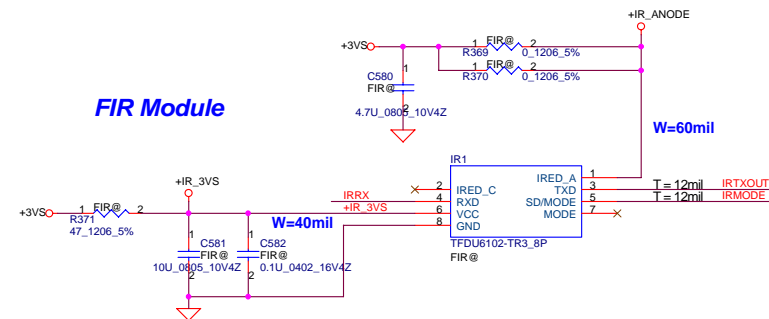
SUPER I/O SMsC LPC47N207



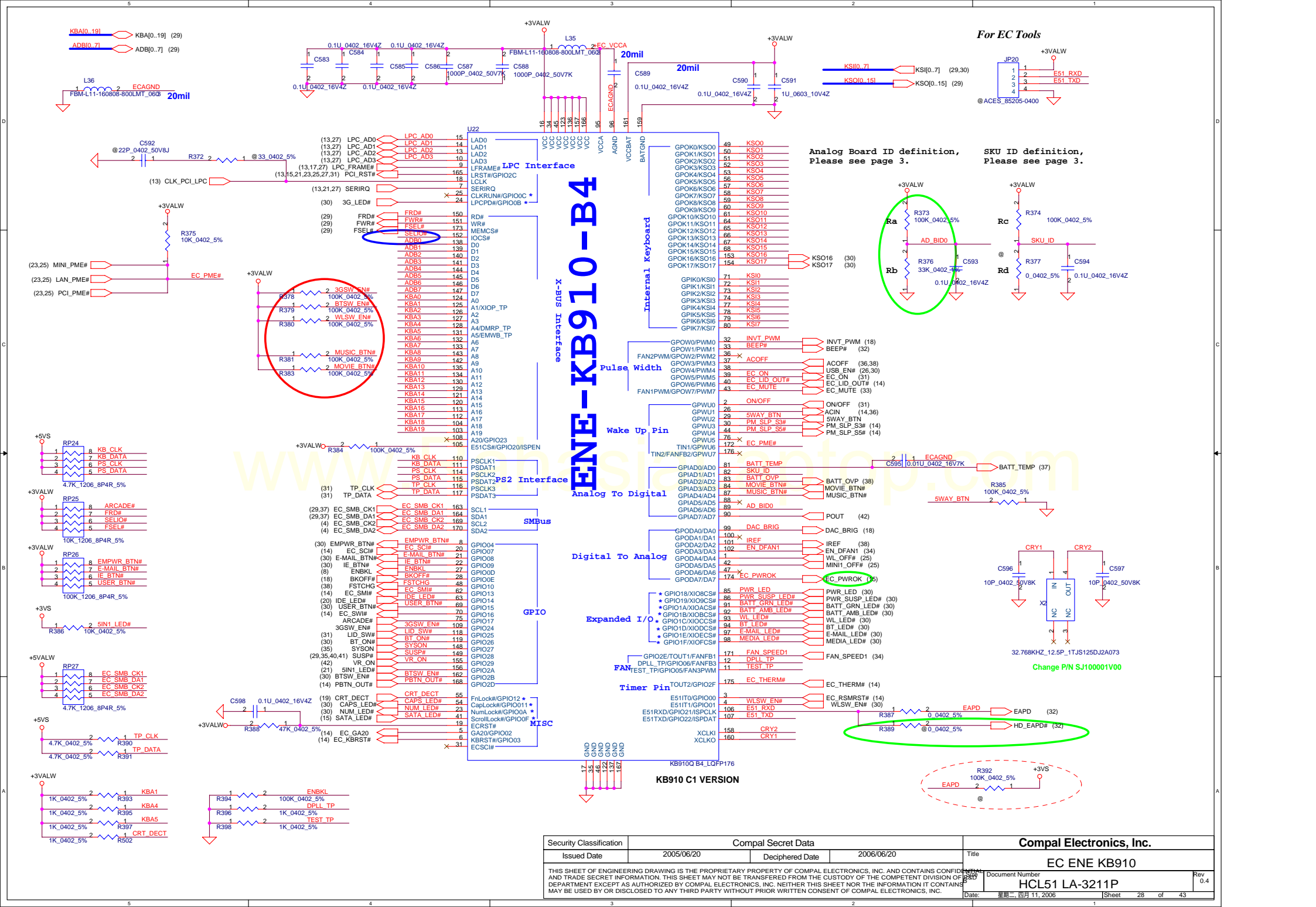
Place on the BOT side(near MINIPCI conn.)

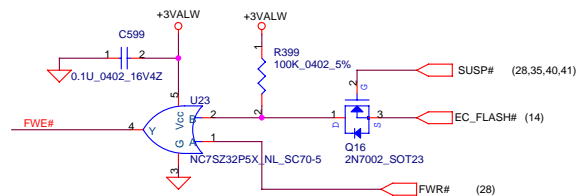


FIR Module

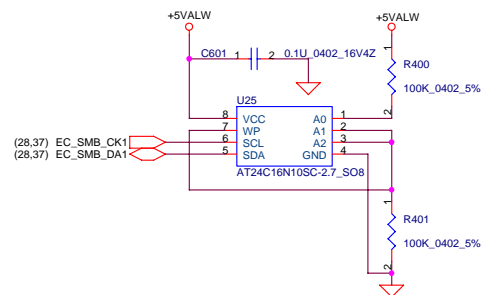


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Issued Date	2005/06/20	Deciphered Date	2006/06/20	Title	SIO1036 & FIR
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				HCL51 LA-3211P	0.4
Date:	日期	2006 四月 11	Sheet	27	of 43

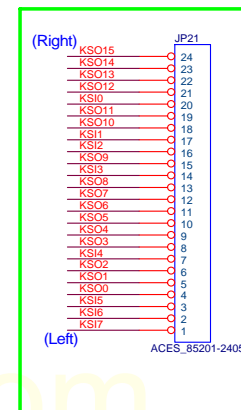




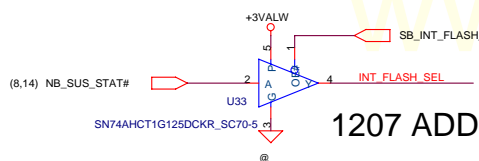
Check PCB Footprint



INT_KBD Conn.



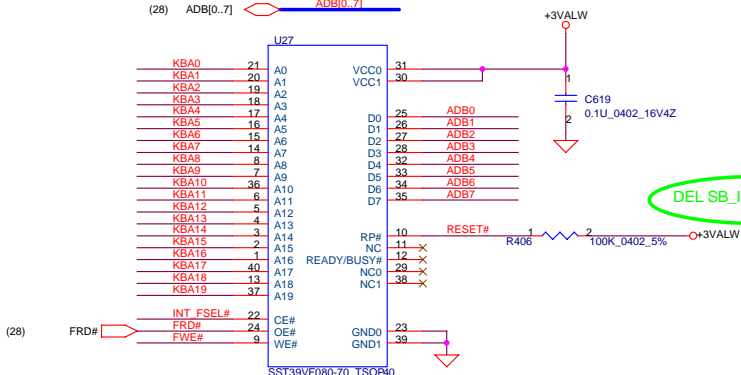
FOR DEBUG ONLY



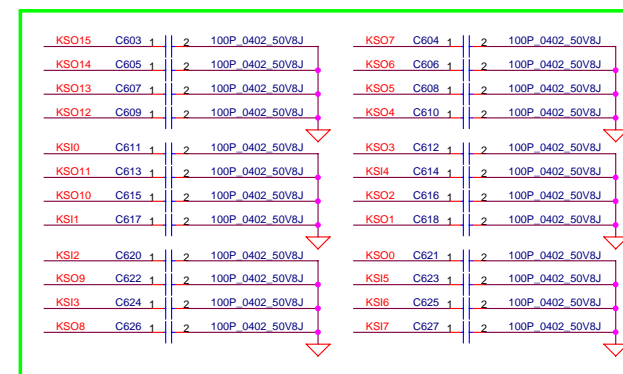
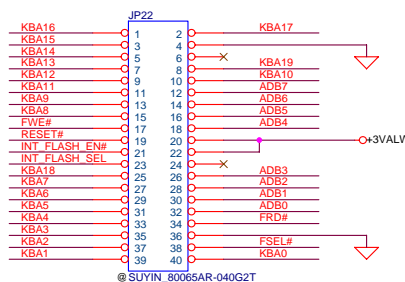
1207 ADD

1MB Flash ROM

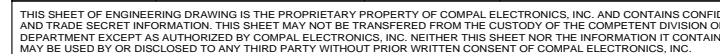
(28) KBA[0..19] KBA[0..19]
(28) ADB[0..7] ADB[0..7]



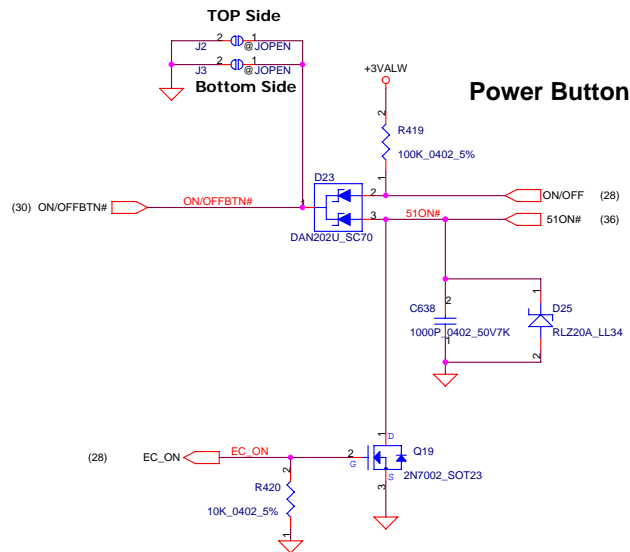
1MB ROM Socket



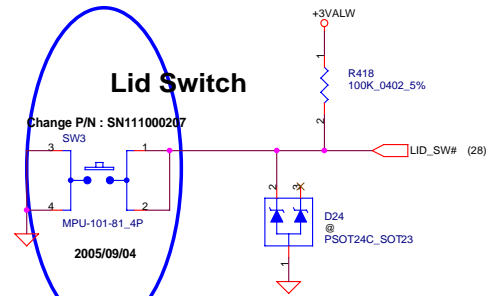
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				Date: 星期二, 四月 11, 2006	Sheet 29 of 43



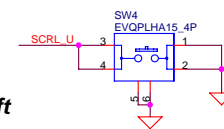
ON/OFF switch



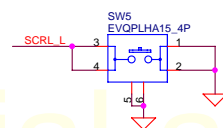
Lid Switch



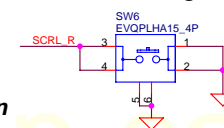
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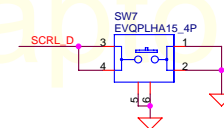
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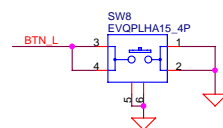
Scroll Right



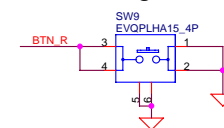
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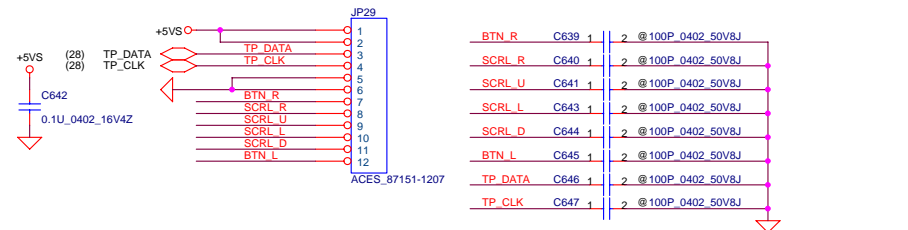
Left



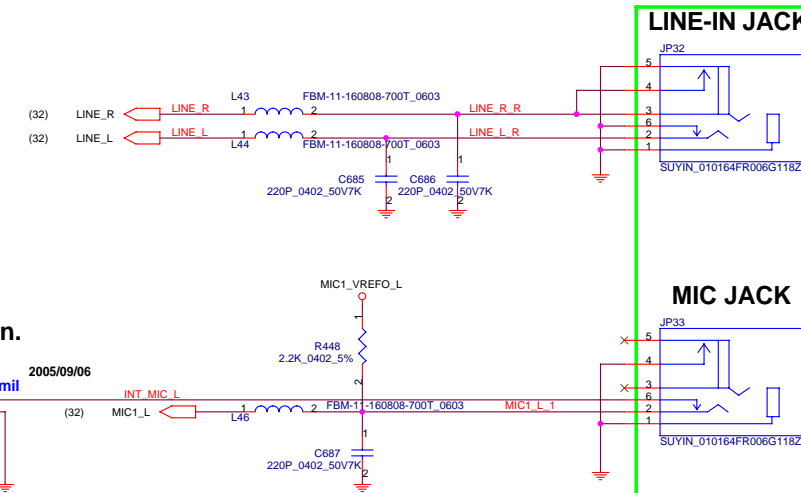
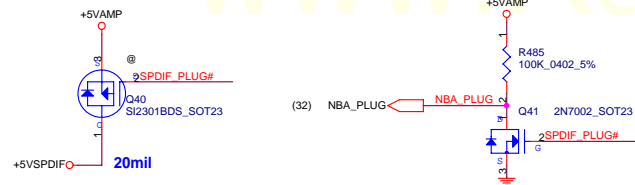
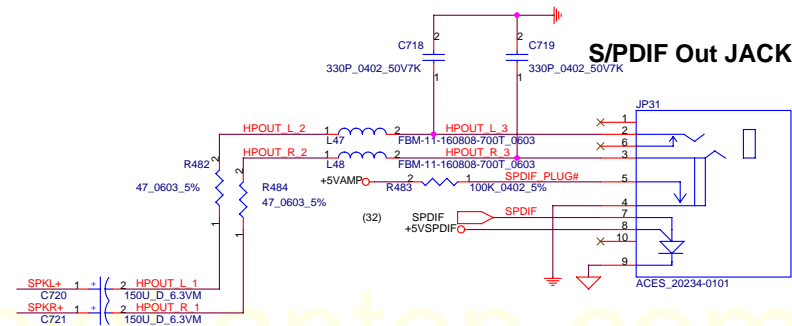
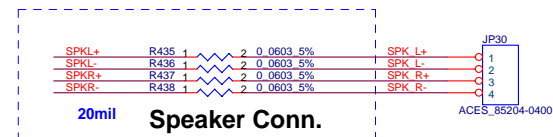
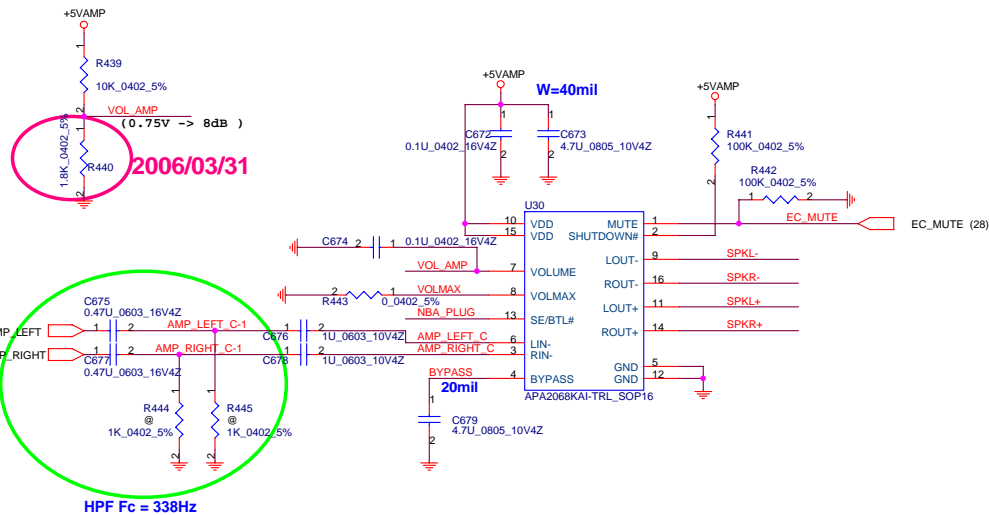
Right



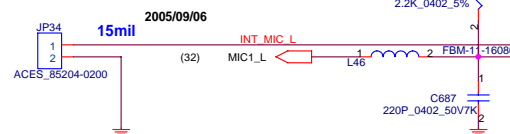
To TP/B Conn.



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				HCL51 LA-3211P
				Rev 0.4
				Date: 星期二, 四月 11, 2006
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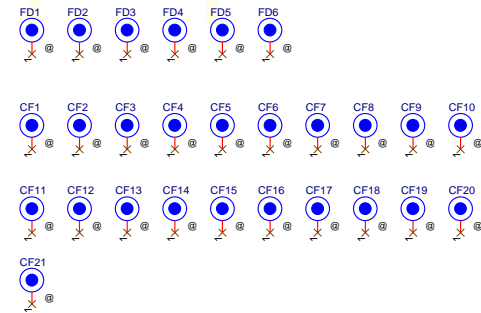
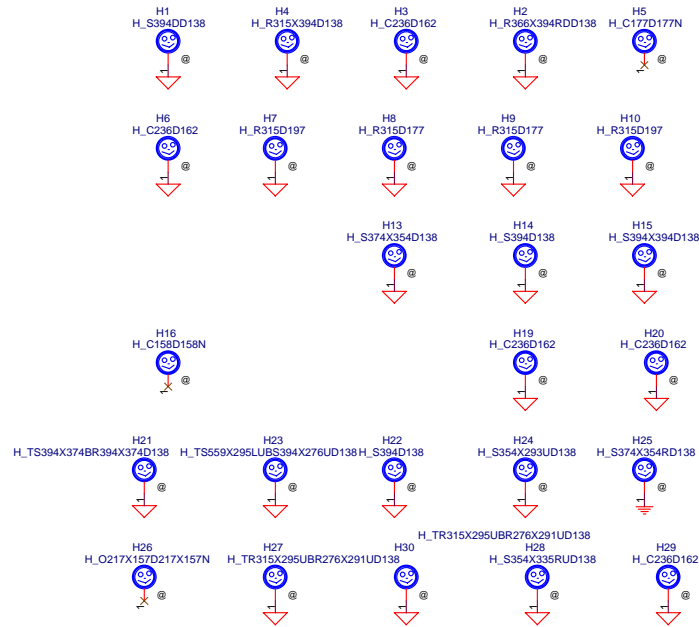
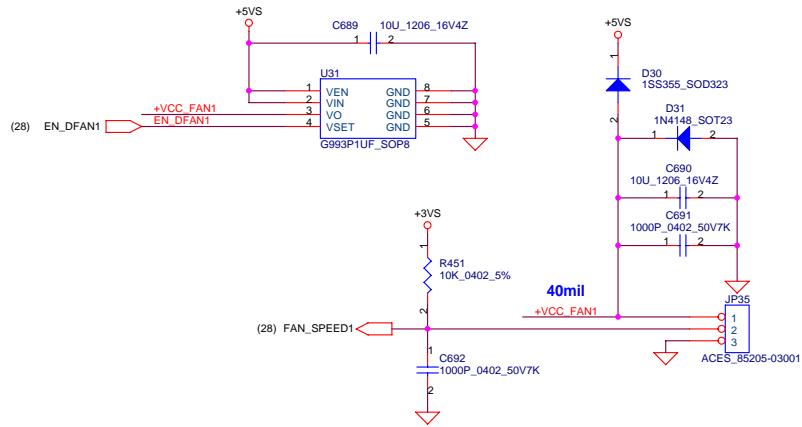


Int MIC Conn.



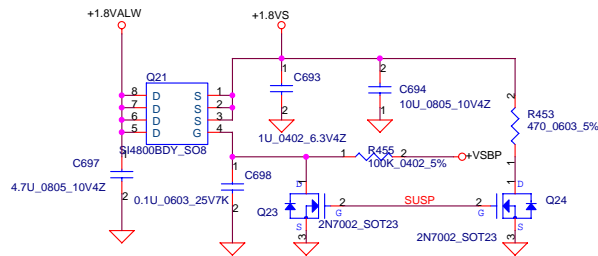
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				HCL51 LA-3211P
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				Date: 星期二, 四月 11, 2006
				Sheet 33 of 43

FAN1 Conn

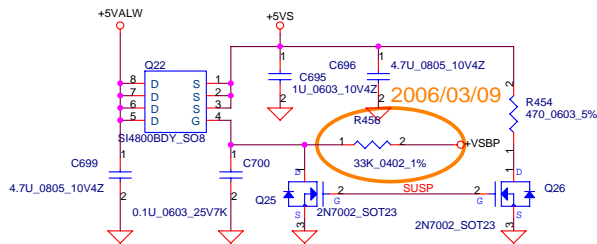


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+1.8VALW TO +1.8VS

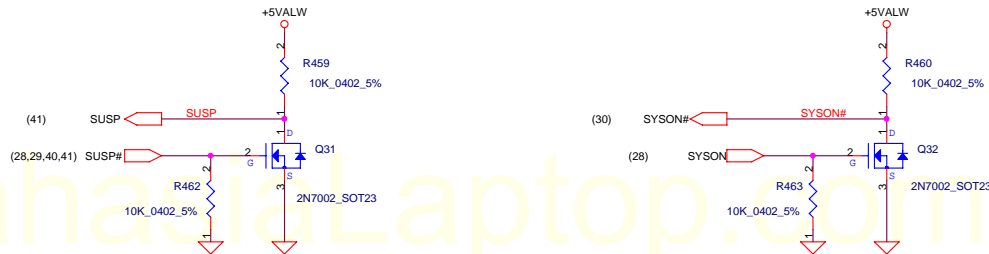
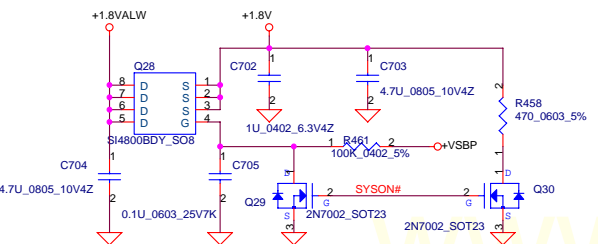


+5VALW TO +5VS

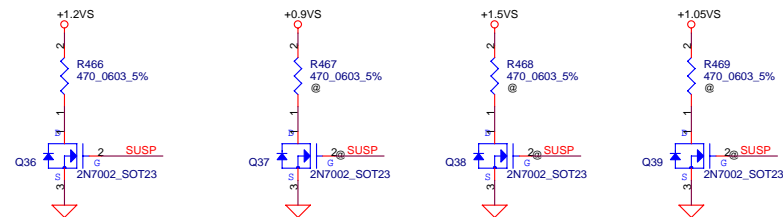
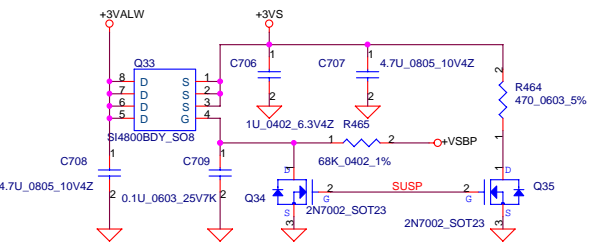


1207 DEL

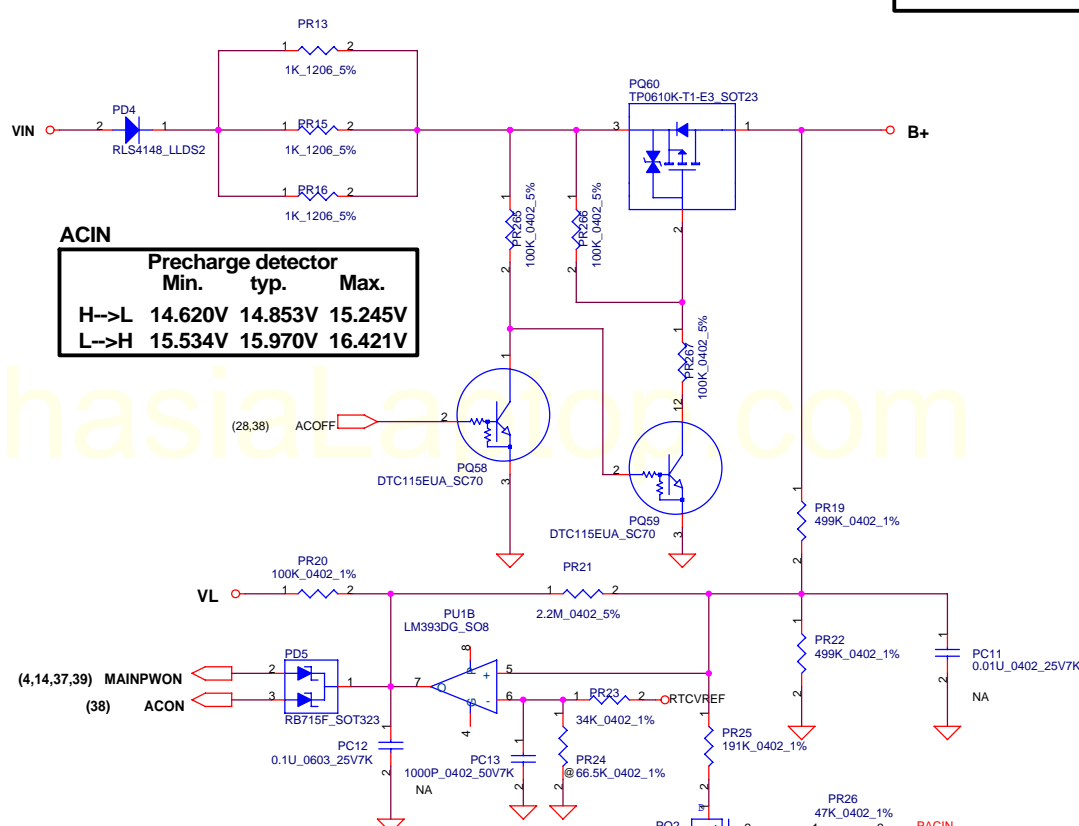
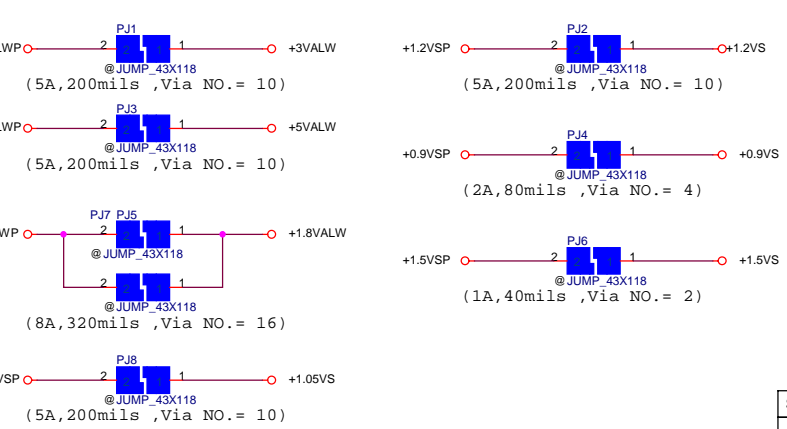
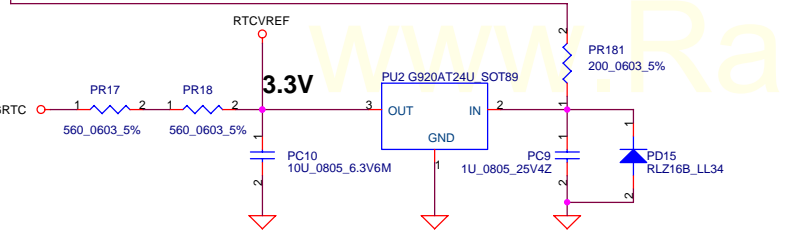
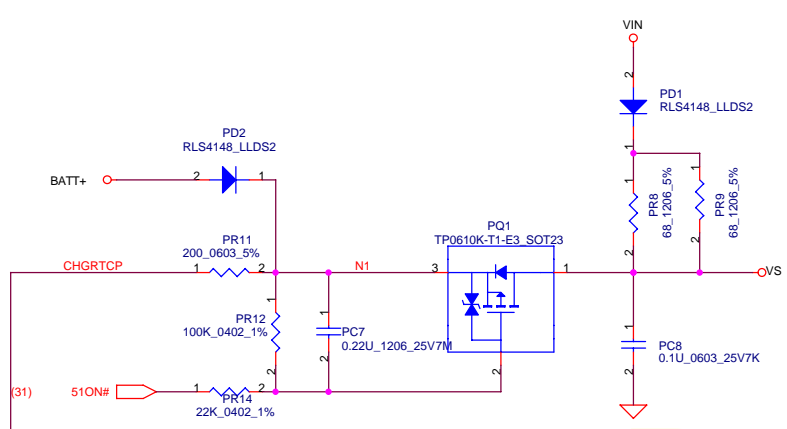
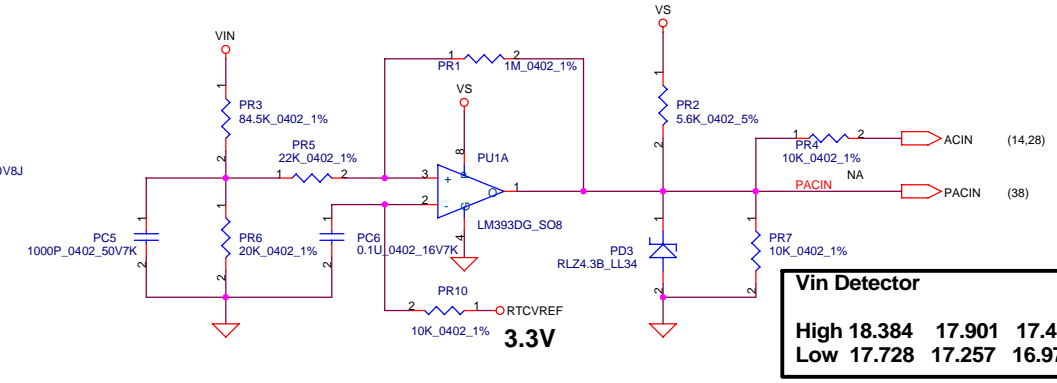
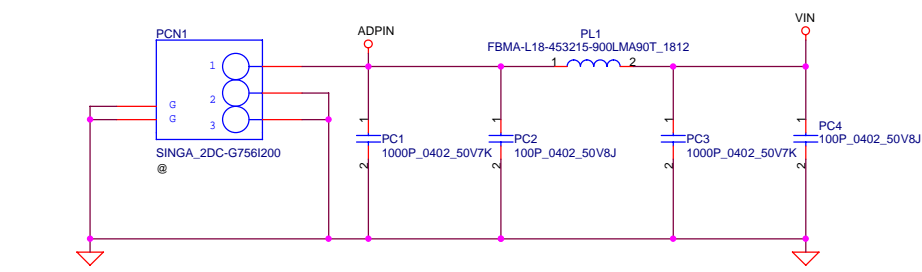
+1.8VALW TO +1.8V



+3VALW TO +3VS



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Issued Date	2005/11/01	Deciphered Date	2006/11/30	Title	DC-DC INTERFACE
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				HCL51 LA-3211P	0.4
Date: 星期二, 四月 11, 2006				Sheet	35 of 43



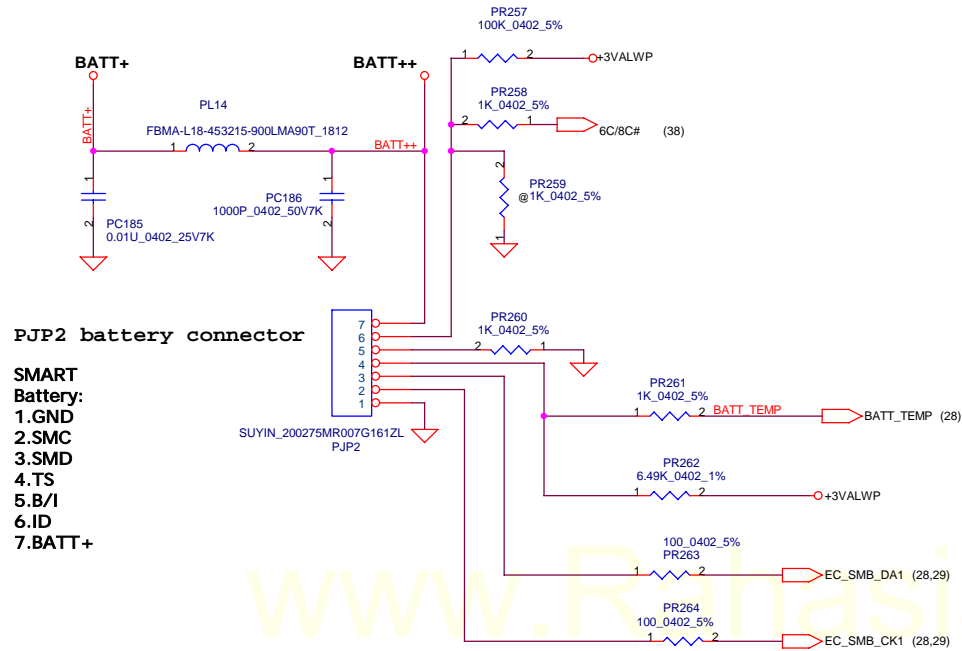
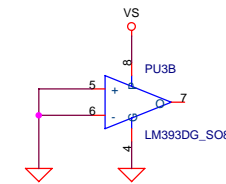
ACIN

	Precharge detector	Min.	typ.	Max.
H-->L	14.620V	14.853V	15.245V	
L-->H	15.534V	15.970V	16.421V	

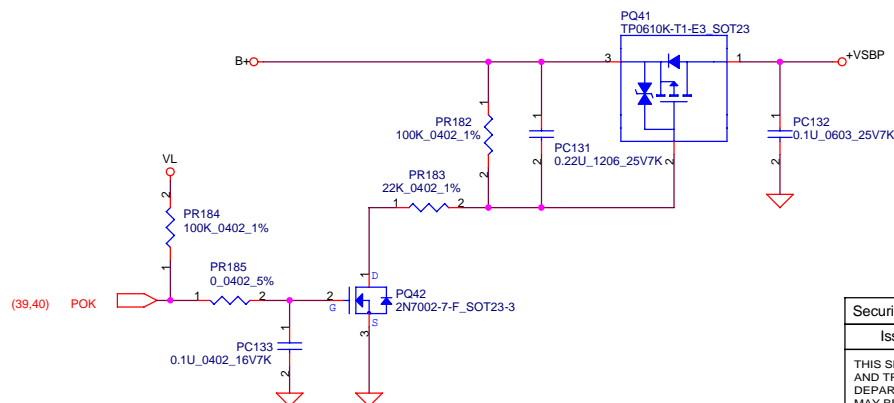
BATT ONLY

	Precharge detector	Min.	typ.	Max.
H-->L	6.169V	6.231V	6.361V	
L-->H	7.168V	7.349V	7.537V	

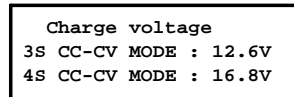
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Issued Date	2005/11/01	Deciphered Date	2006/11/30	Title
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**SMART
Battery:**
1.GND
2.SMC
3.SMD
4.TS
5.B/I
6.ID
7.BATT+



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LI-4S :17.8V---BATT-OVP=1.98V
BATT-OVP=0.111*BATT+
LI-3S :13.35V---BATT-OVP=1.98V
BATT-OVP=0.111*BATT+
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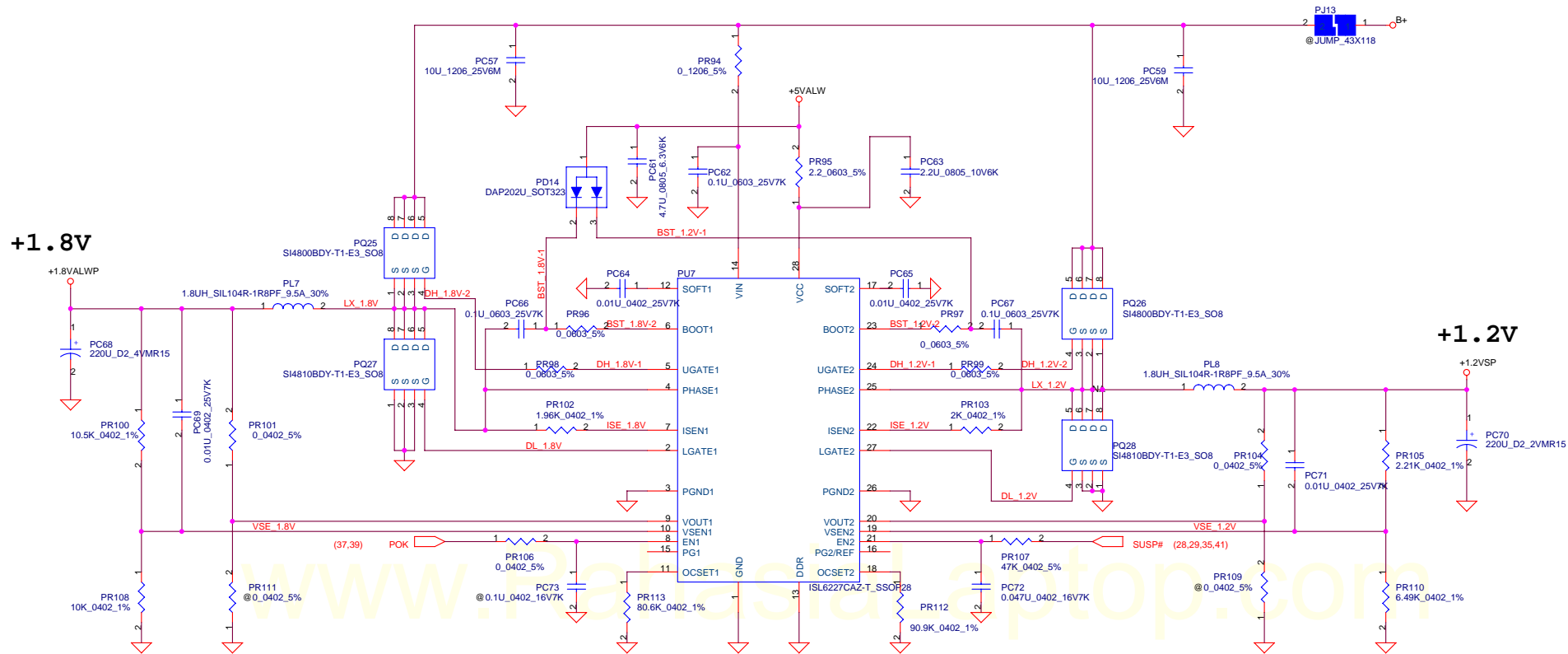
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+3.3VALWP/+5VALWP

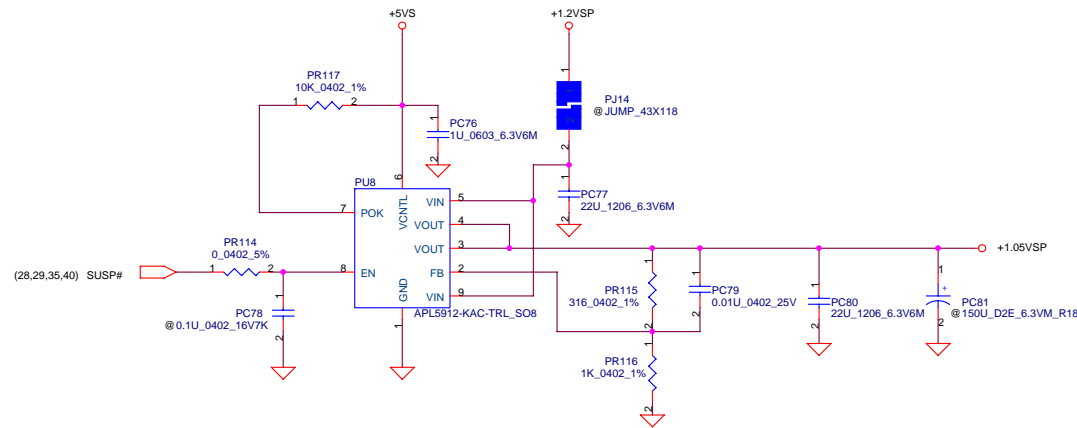
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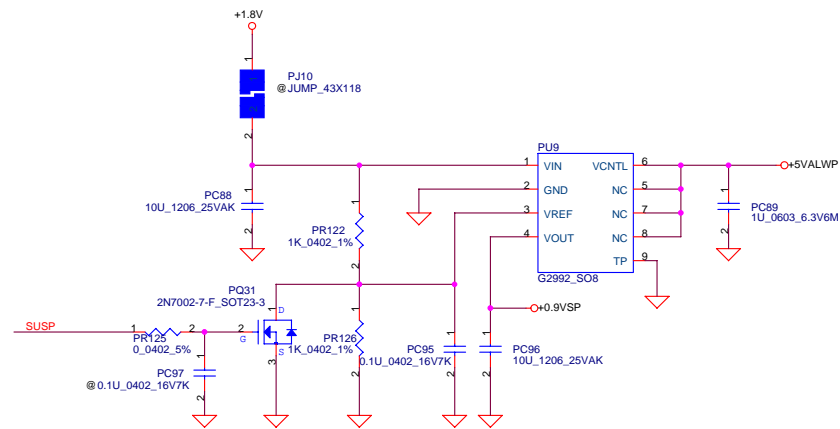
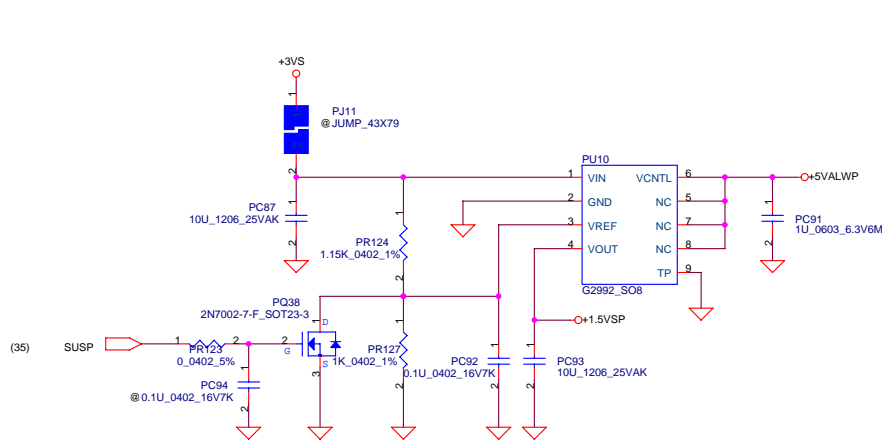
+1.2VP O.C.P= 8.67A~14.09A



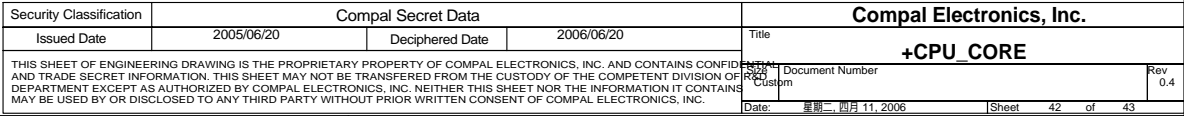
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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1		For EMI require CPU core change from 0 to 2.2		42	MODIFY PR268/PR269 FROM 0 TO 2.2		DVT
2		modify 1.2V sequence(HW require)		40	change PR107 from 0 to 1k ;add PC72: :0.01uF		DVT
3		modify 1.2V sequence(HW require)		40	change PR107 from 1K to 47K ;change PC72: : from 0.01uF to 0.047uF		PVT
4							
5							
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PIR (PWR)			
Size	Document Number		Rev
			0.4
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