

BOM MARK	
E@ EXT VGA 要打	
I@ INTVGA 要打	
SA@ SATA 要打	
F@ FIXED ODD 要打	
SW@ SWAPPABLE ODD 要打	
3@ 3in1 要打	
N@ NEW CARD 要打	
4@ 4401 要打	
5@ 5788M 要打	
D@ DOCKING 要打	

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LVDS	Page:16
TV-OUT	Page:16

DOCKING/DVI	Page: 33
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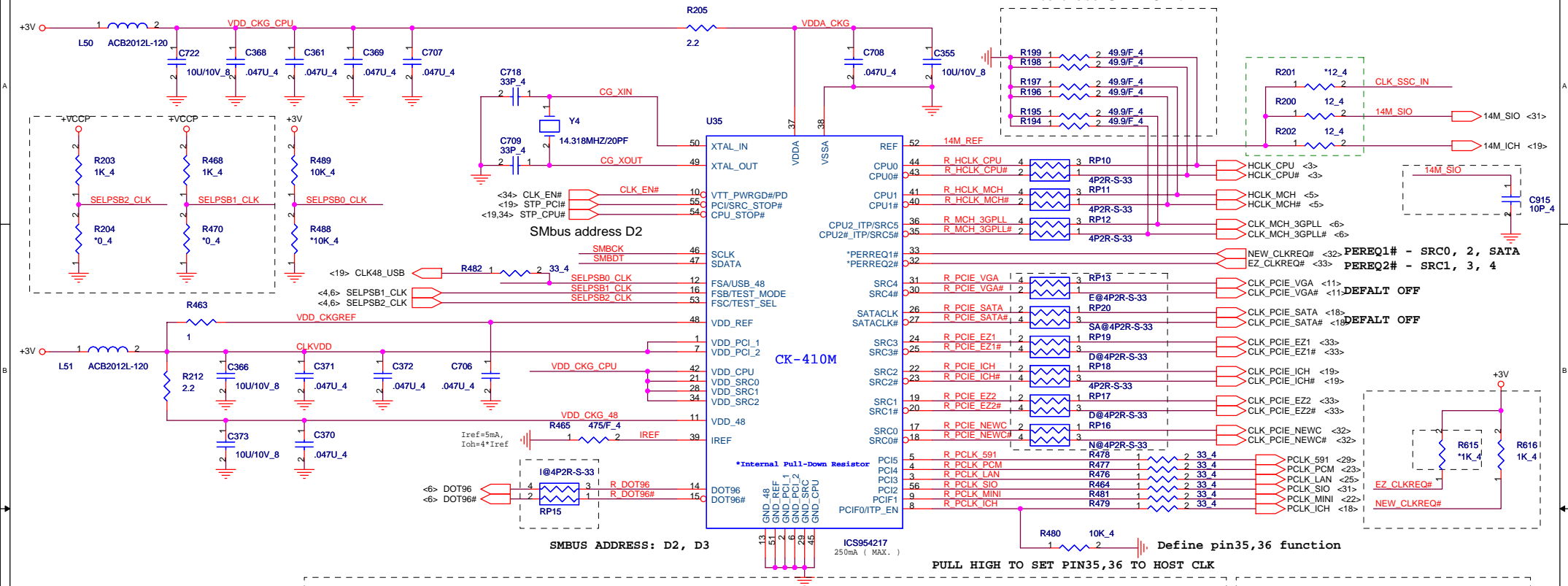
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RJ45	Page:26
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PCI ROUTING TABLE	IDSEL	INTERRUPT	DEVICE
REQ0# / GNT0#	AD24	INTA#	BROADCOM LAN
REQ2# / GNT2#	AD19	INTB# , INTD#	MINI-PCI
REQ1# / GNT1#	AD17	INTC#, INTD#, INTA#	TI 7411

Place these termination  
to close CK410M.



SMBUS ADDRESS: D2, D3

PULL HIGH TO SET PIN35,36 TO HOST CLK

SMBUS ADDRESS: D4, D5

DOTHAN-A 400

DOTHAN-A 533

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

Place these termination  
to close CK410M.



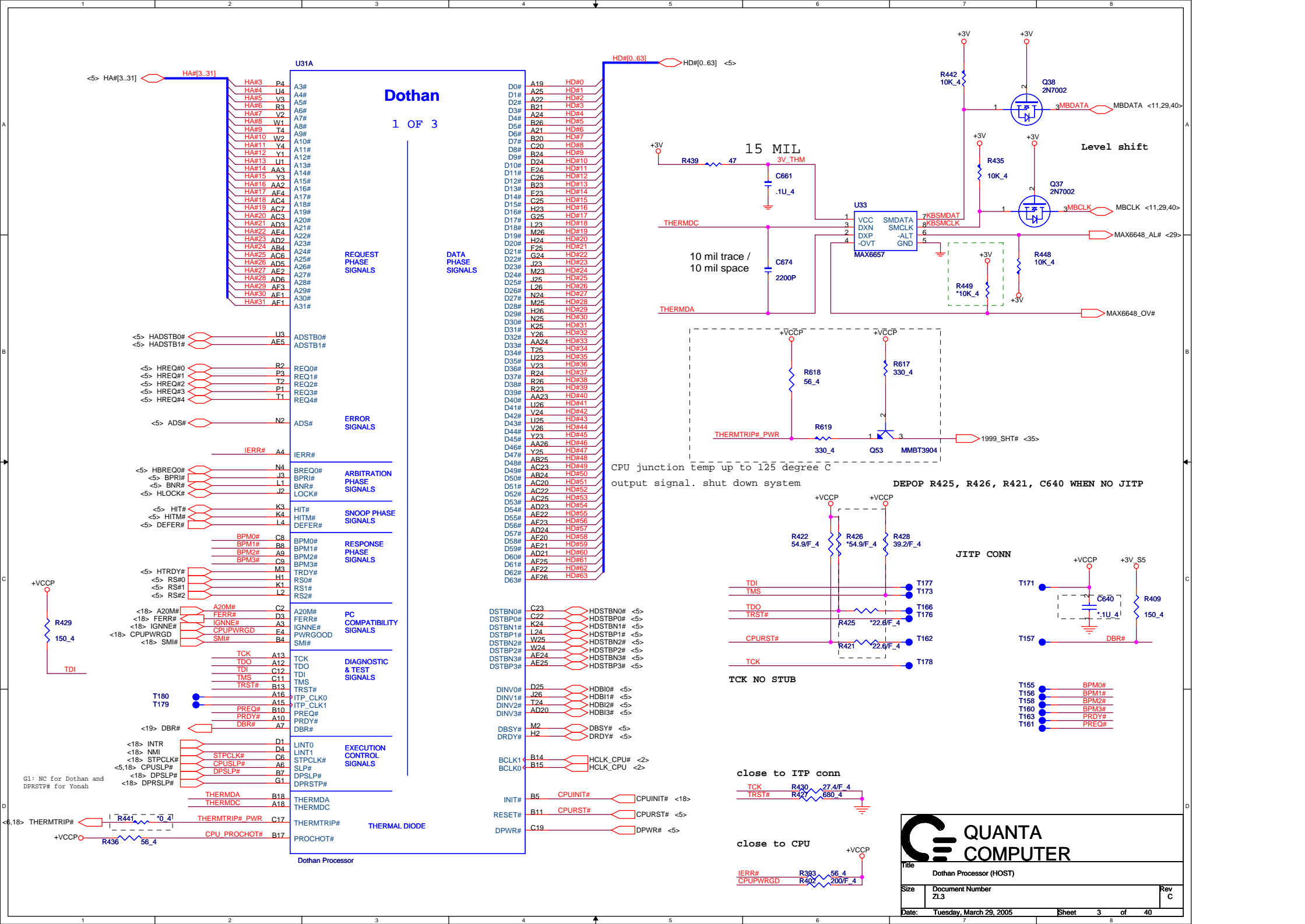
CLOCK GENERATOR

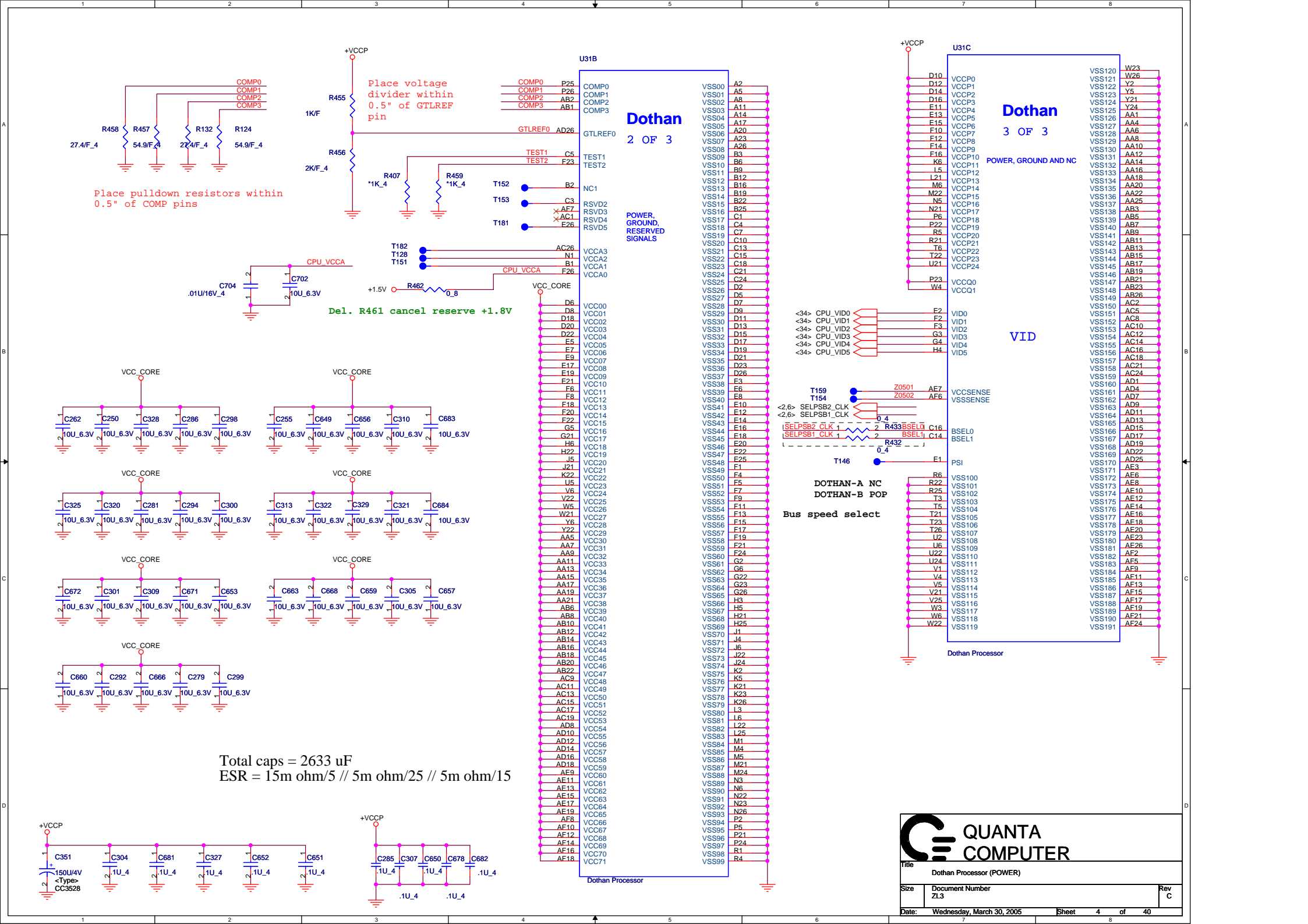
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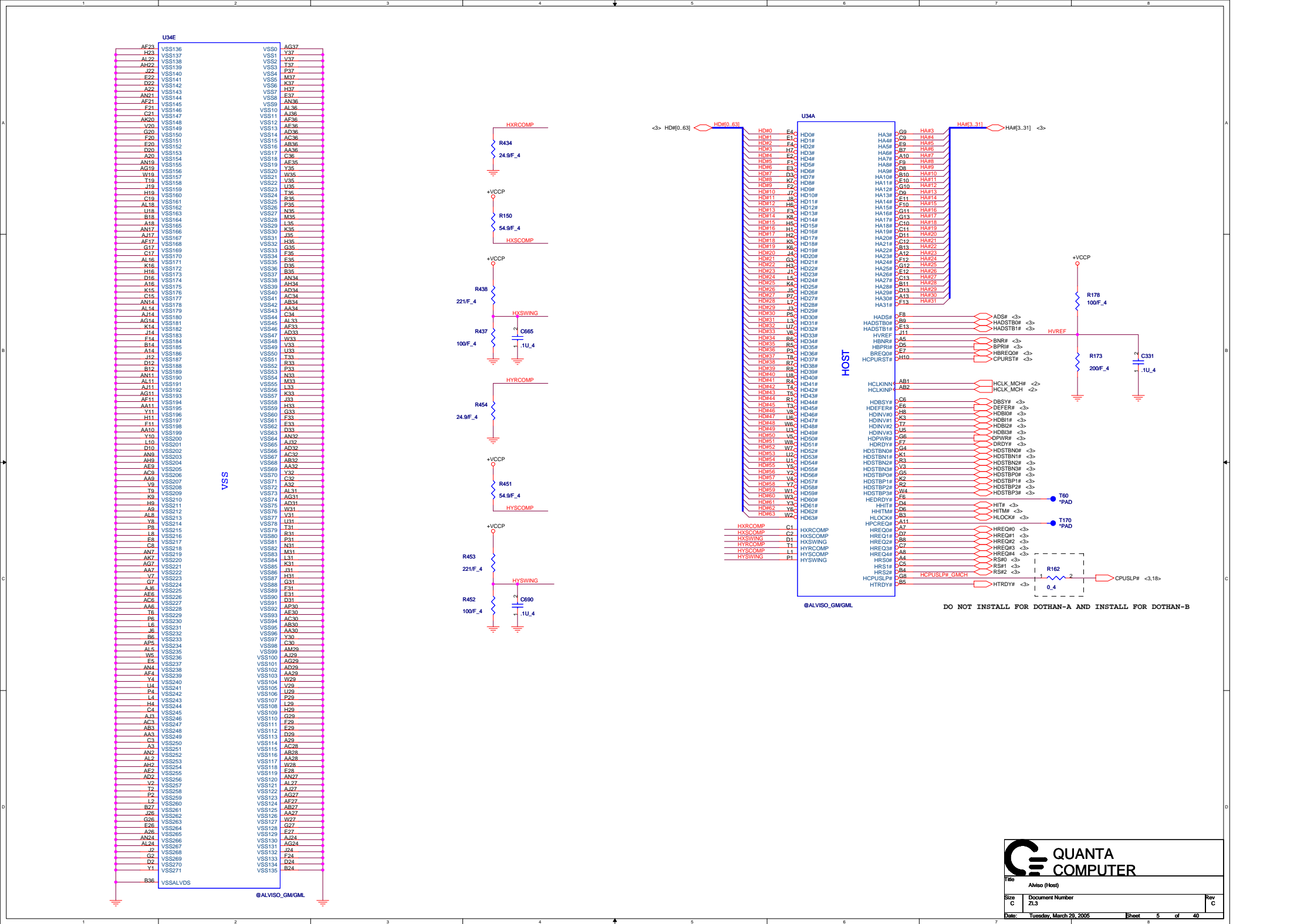
Date: Tuesday, March 29, 2005

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Rev C









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CFG[0:2]=101 FOR FSB 400

CFG3 R168 1K\_4  
FOR DDR533

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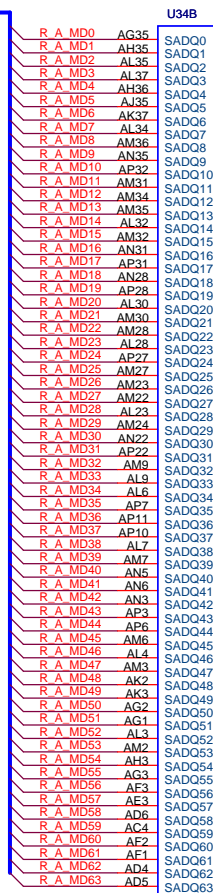
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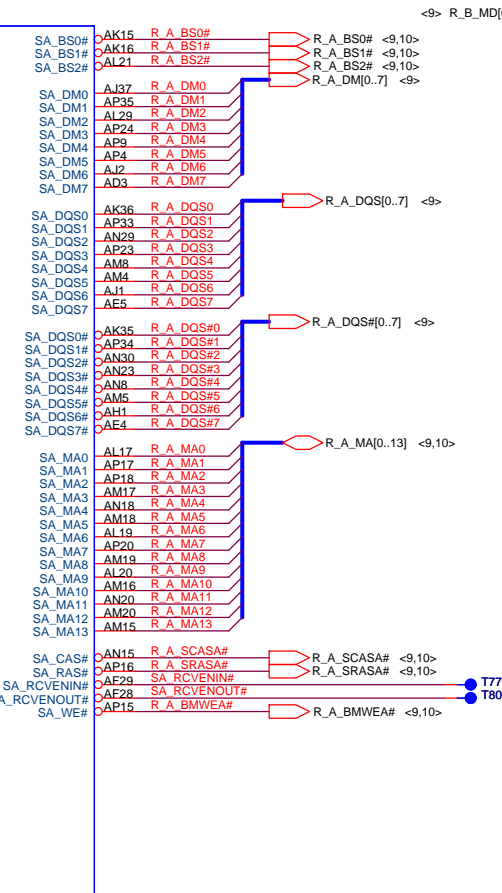
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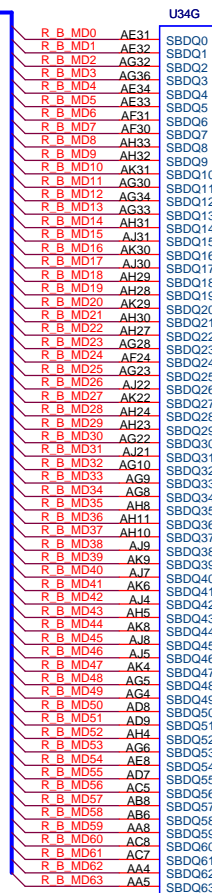


DDR SYSTEM MEMORY A

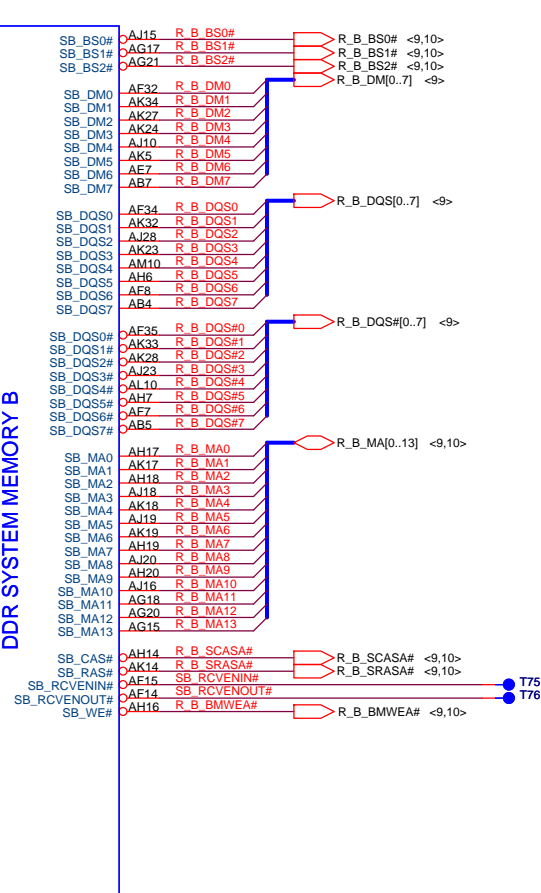


@ALVISO\_GM/GML

<9> R\_B\_MD[0..63]



DDR SYSTEM MEMORY B



@ALVISO\_GM/GML



Alviso (DDR)

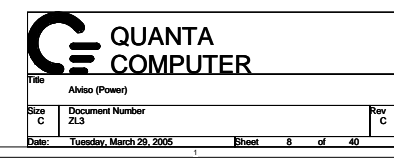
Size Document Number

CustomZL3

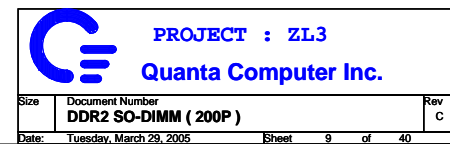
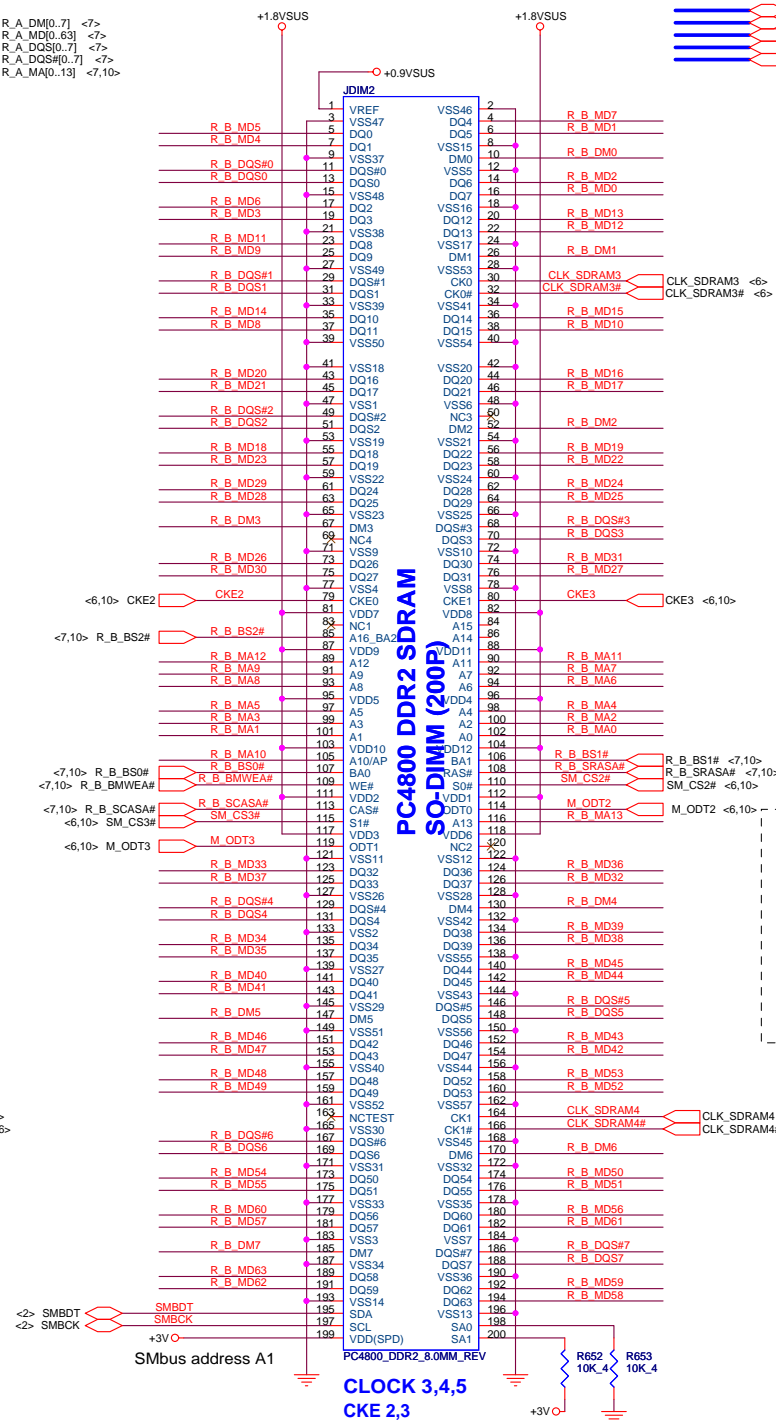
Date: Tuesday, March 29, 2005

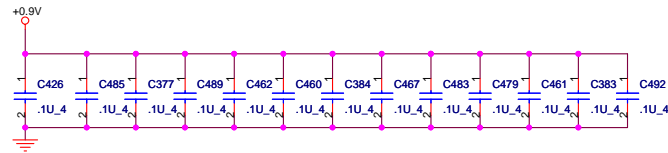
Sheet 7 of 40

Rev C

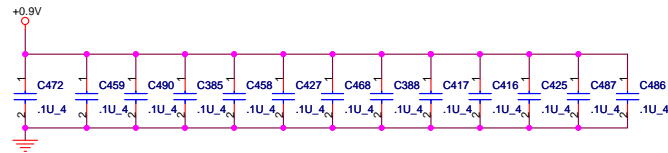




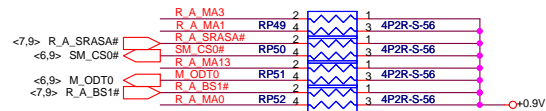
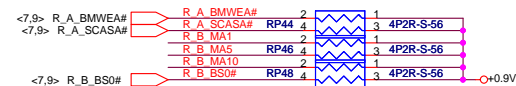
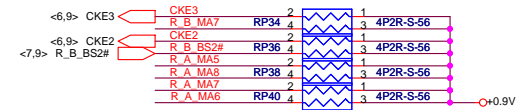
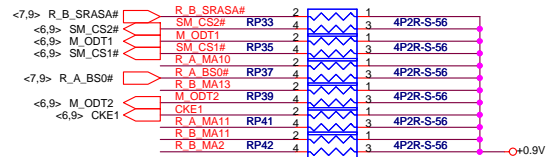
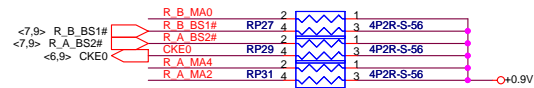


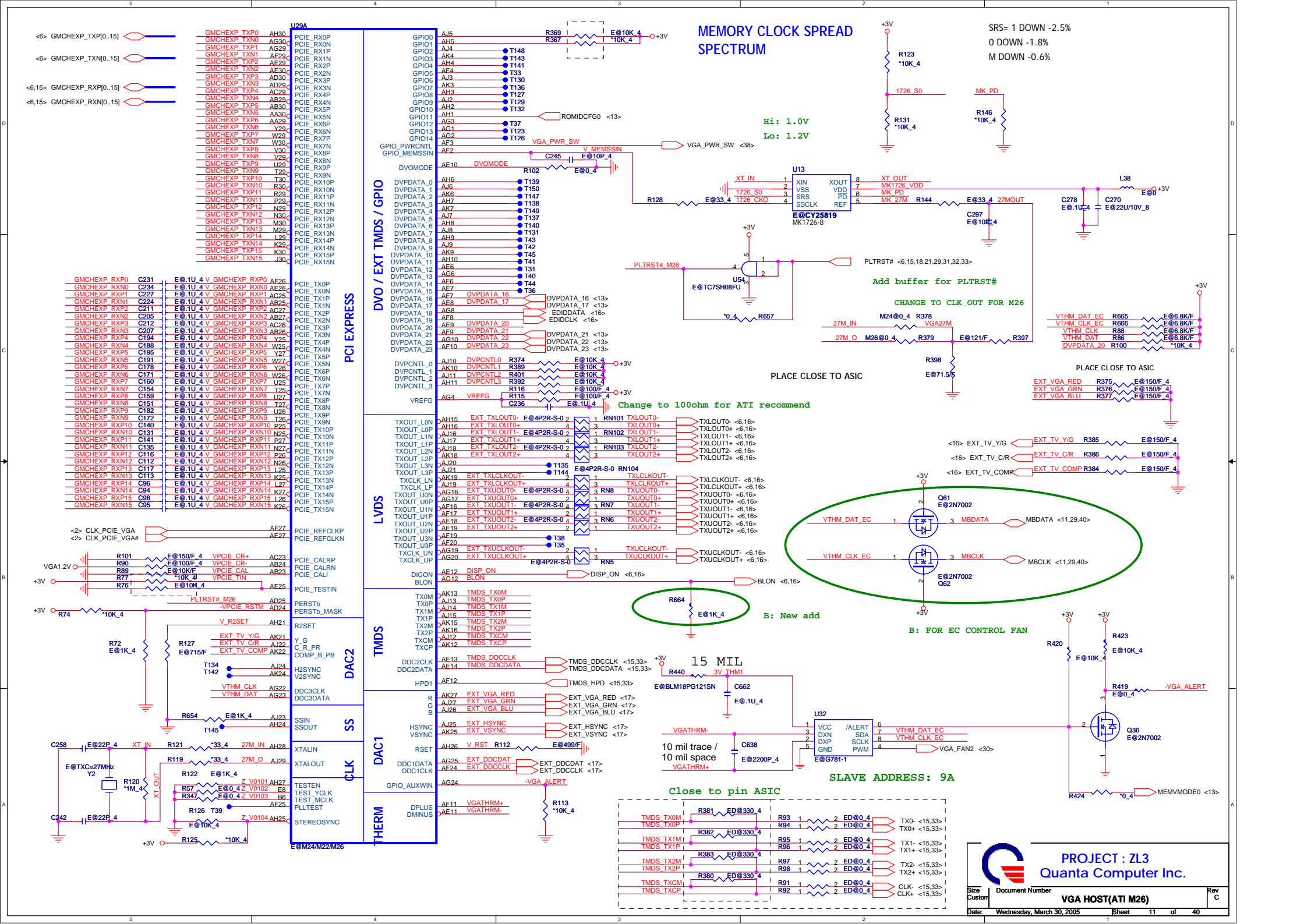


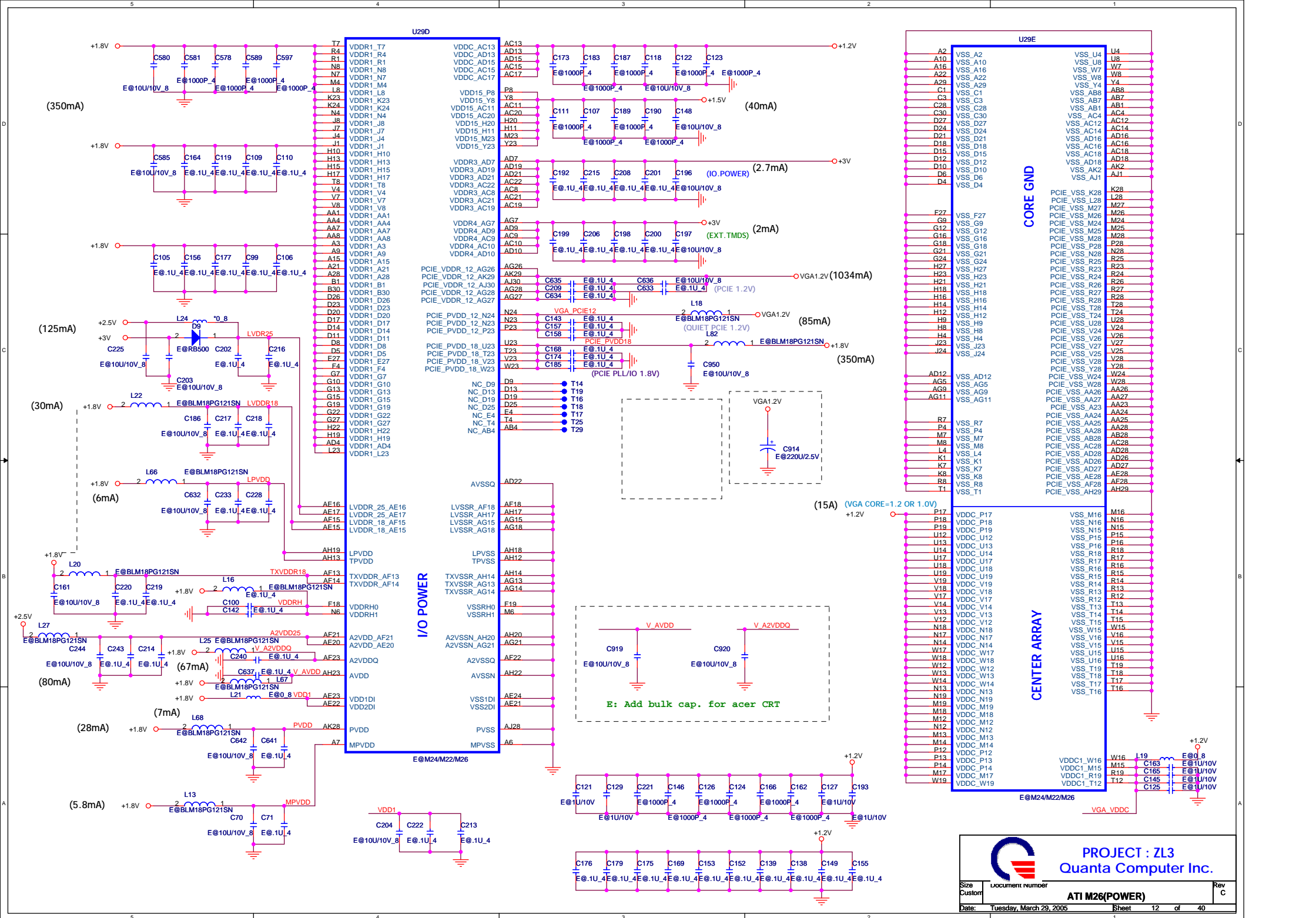
Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9V

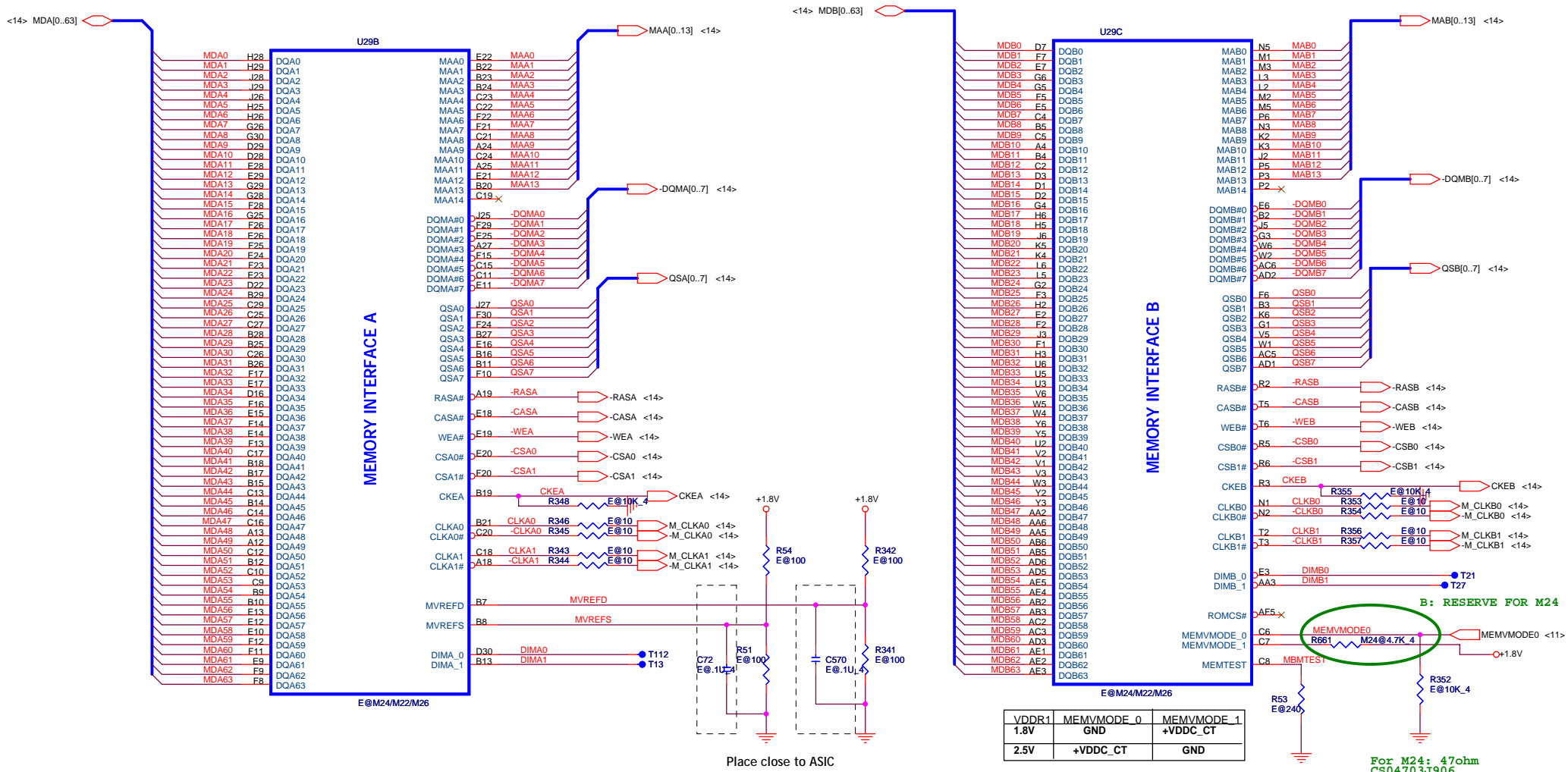


Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9V









STRAPS PIN	
GPIO_0	PCI-Express Current Calibration Bandgap Backup 0: use reference voltage from Bandgap 1: use reference voltage from resistor divider
GPIO_1	PCI-Express PLL Calibration force enable 0: Disable PLL force calibration 1: Enable PLL force calibration
GPIO_(3,2)	00: PCI Express 1.0 mode 01: RESERVED 10: PCI Express 1.0 mode 11: RESERVED
GPIO_4	Turn off PCI-Express impedance / strength calibration 0: enable 1: disable
GPIO_5	Bypass PCI-Express PLL

STRAPS PIN	
GPIO_6	PCI-Express transmitter current compensation 0: Normal 1: Inject extra current for output buffer switching
GPIO_8	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible
GPIO(9,13:11) INT P/D	ROMIDCFG 0x0x: No ROM, CHG_ID=0 0x1x: No Rom, CHG_ID=1 1000: Parallel ROM, Chip ID'S from ROM 1000: Parallel ROM, Chip ID'S from ROM
DVPDATA_21-23	MEM TYPE DVPDATA_21: 0=4Mx32 1=8Mx32 DVPDATA_22: 0=128M 1=64M DVPDATA_23: 0=Hynix 1=Samsung

ROMIDCFG0

R107 \*10K\_4

R105 E@10K\_4

R406 E@10K\_4

R410 \*10K\_4

R390 \*10K\_4

R399 E@10K\_4

R391 E@10K\_4

R400 \*10K\_4

R372 \*10K\_4

R373 \*10K\_4

R387 E@10K\_4

R388 E@10K\_4

DVPDATA\_16

DVPDATA\_17

DVPDATA\_21

DVPDATA\_22

DVPDATA\_23

For M26P ONLY  
0: 128M  
1: 256M

C: FOR HYNIX MEMORY

PROJECT :ZL3  
Quanta Computer Inc.

ATI M26 MEM/STRAPS PIN

Size Custom

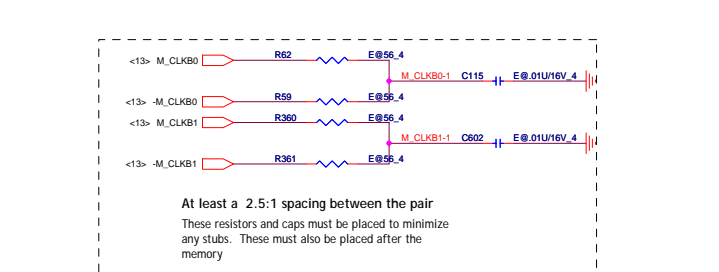
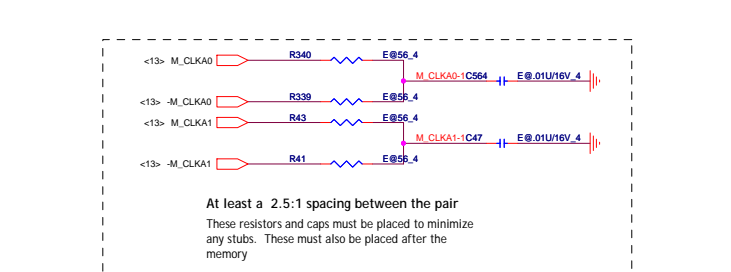
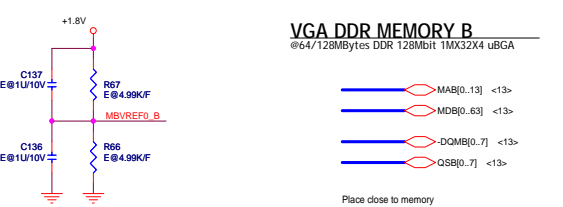
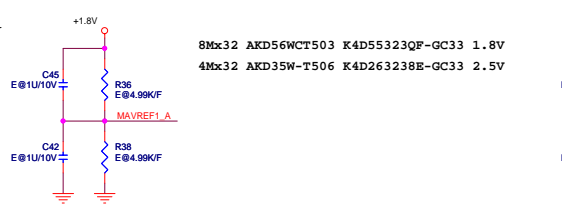
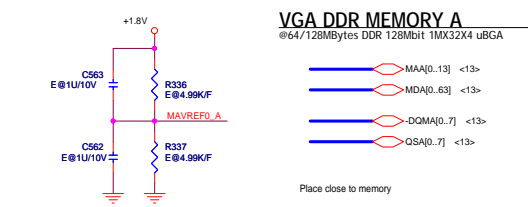
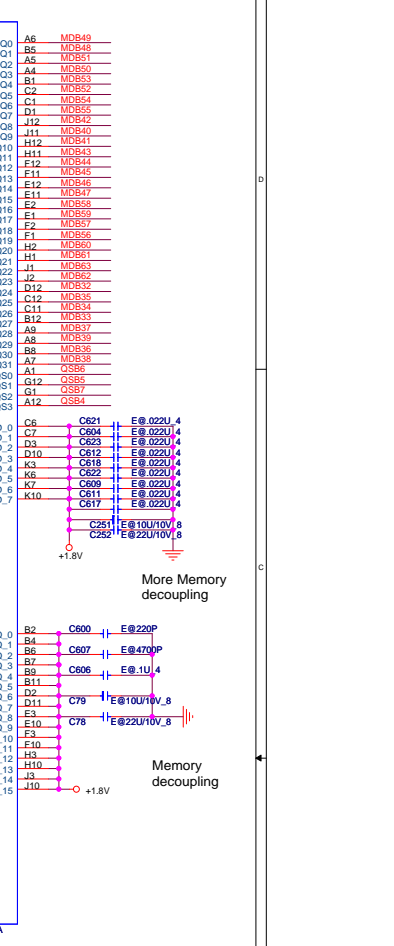
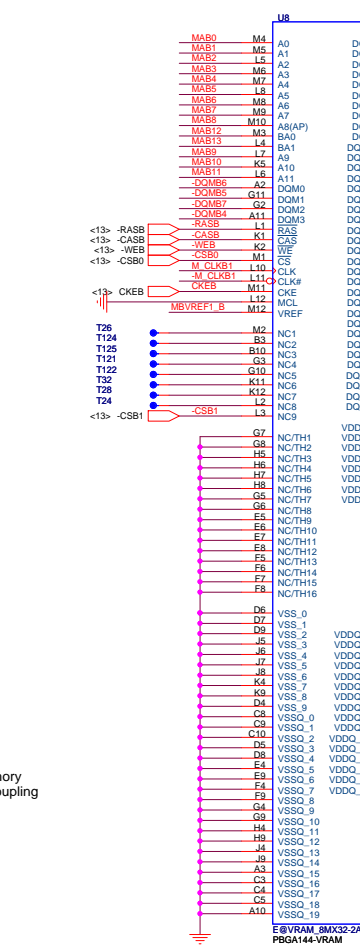
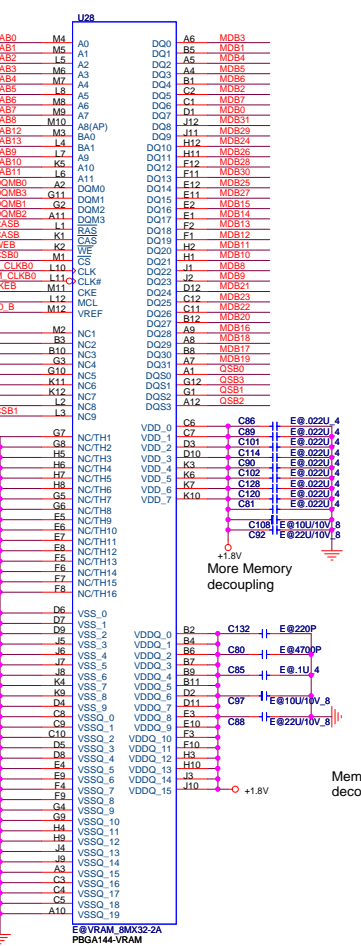
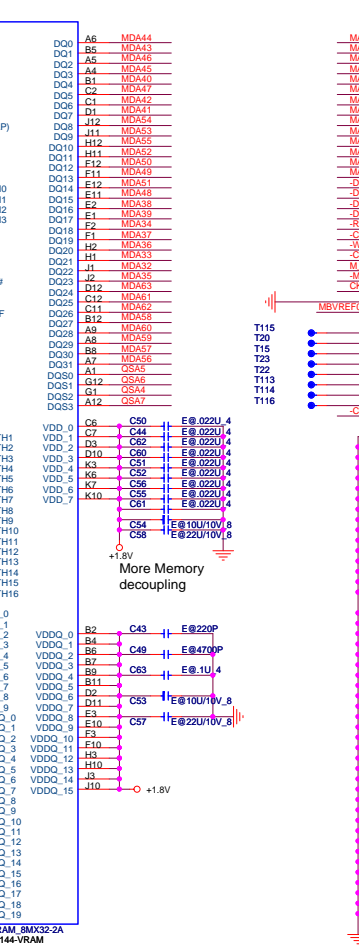
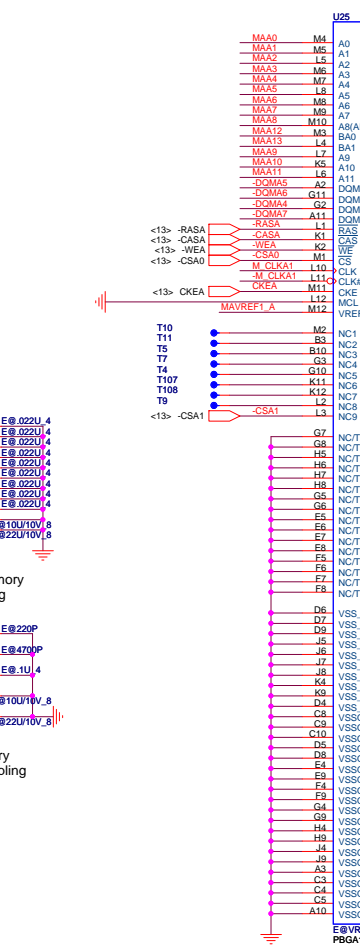
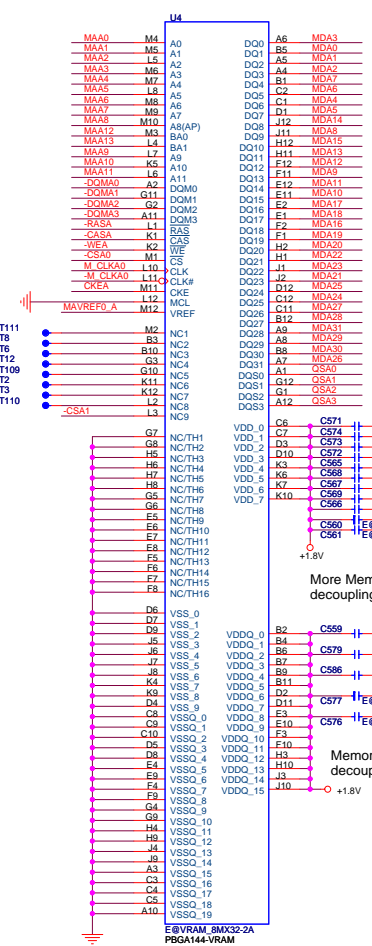
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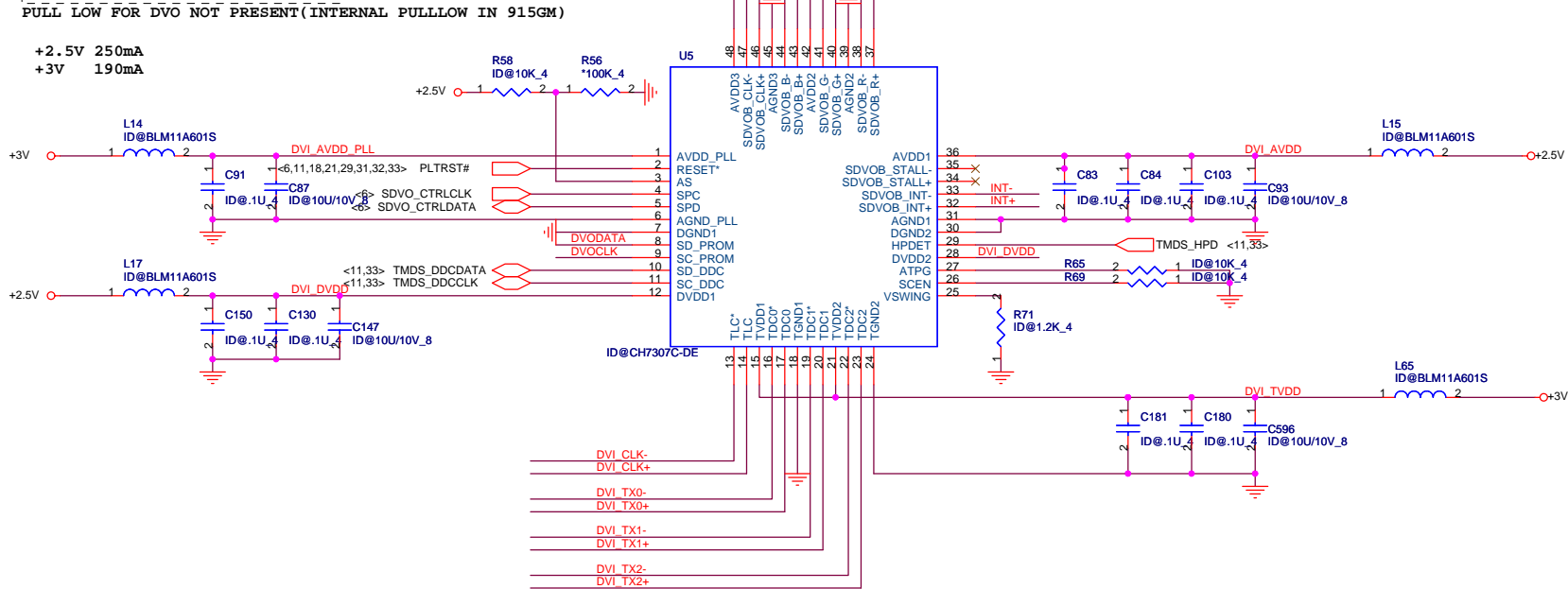
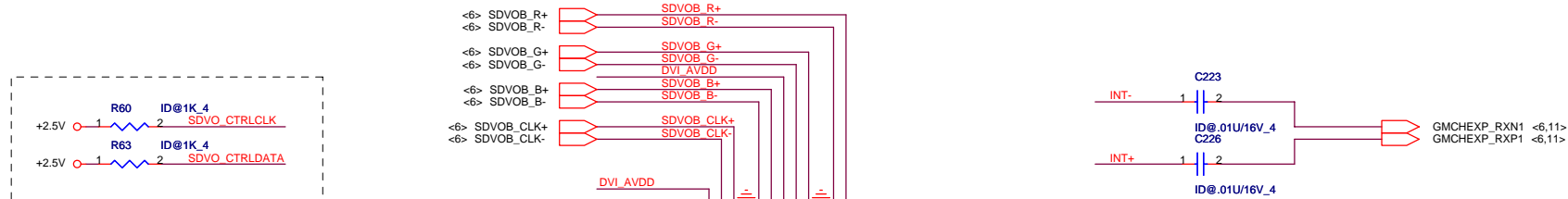
Date: Tuesday, March 29, 2005

Sheet 13 of 40

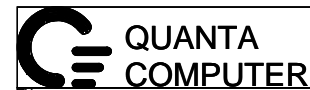
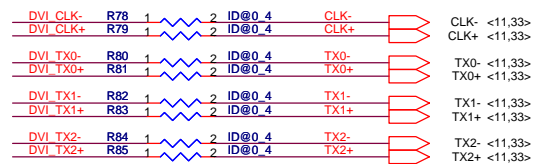
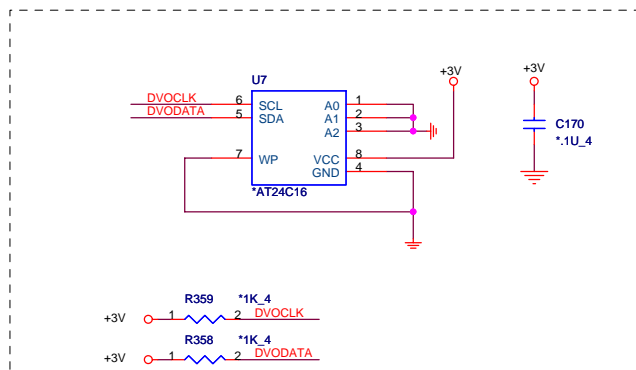
Rev C

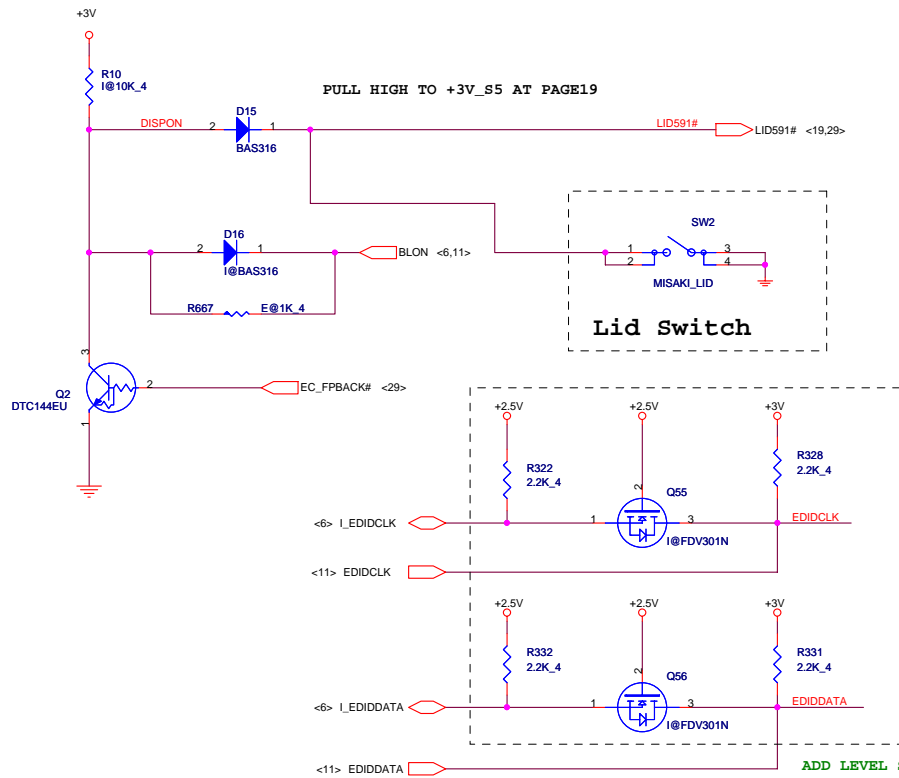




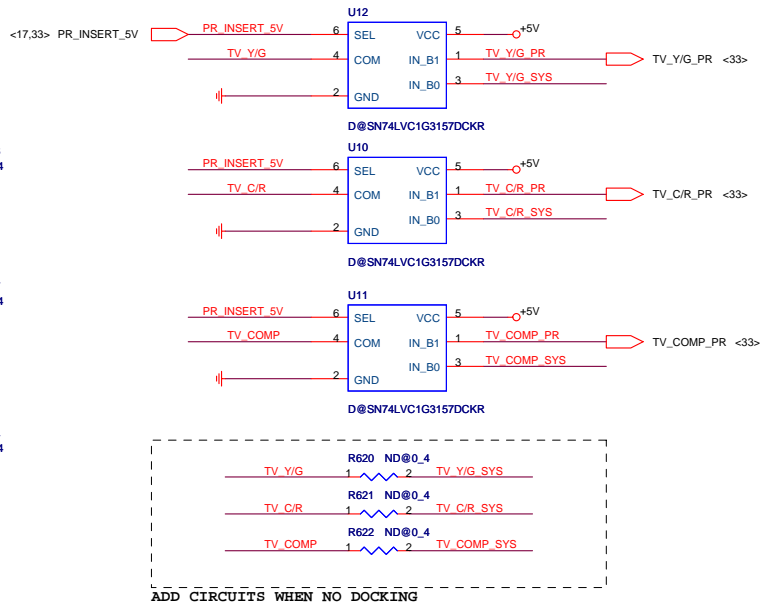


ALWAYS NOT ON, TEST ONLY

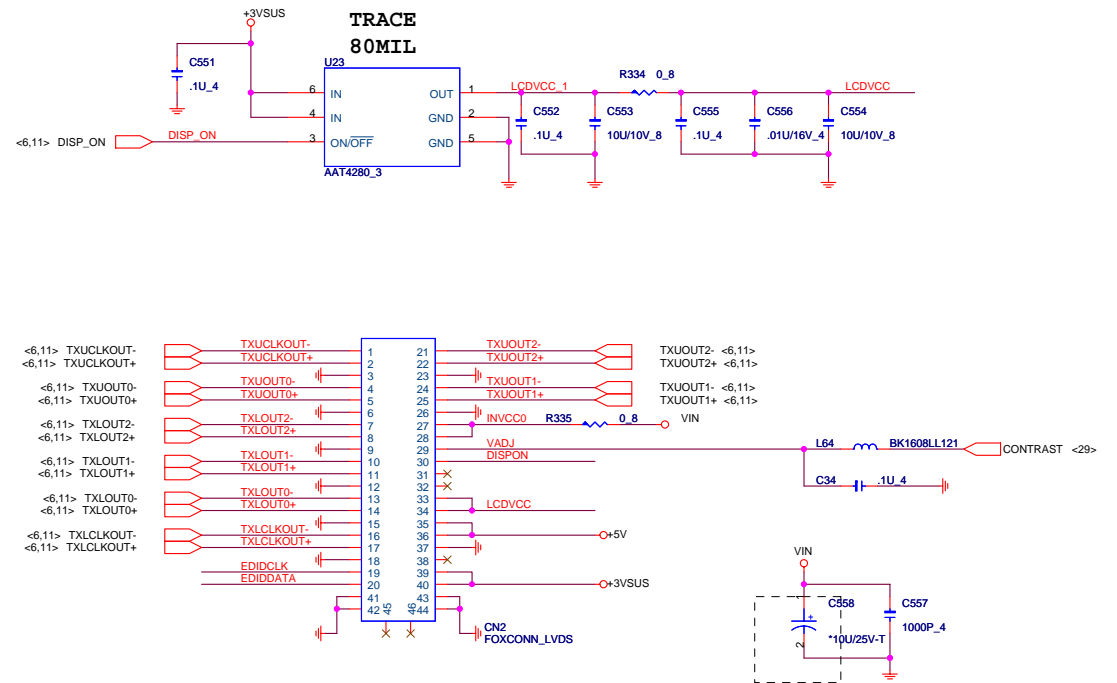
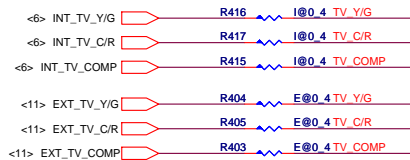


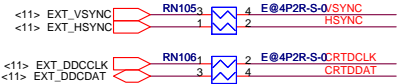
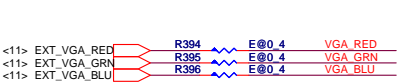
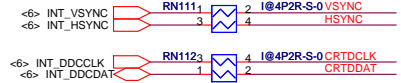


ADD LEVEL SHIFT FOR EDID  
C: Change to FDV301 for Vgs issue

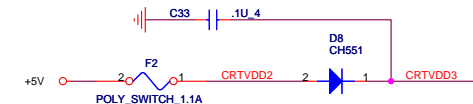
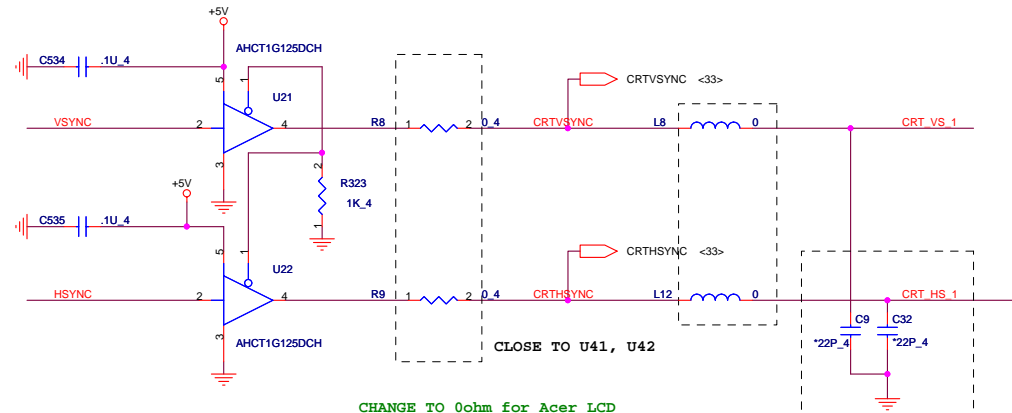
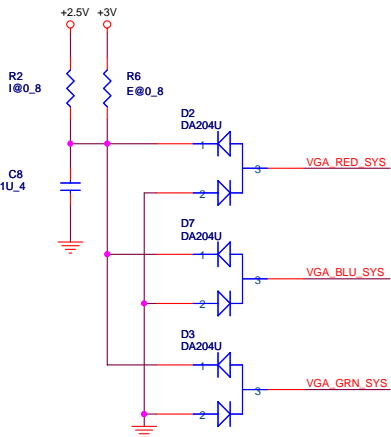
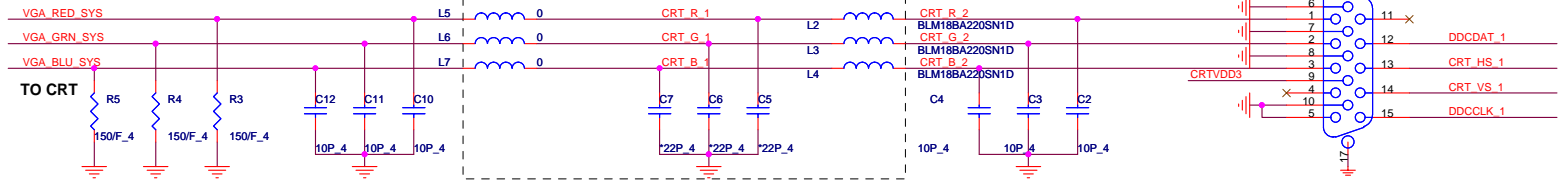
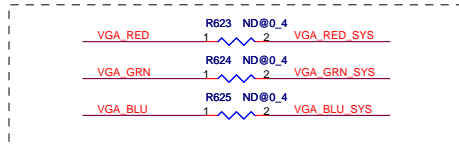
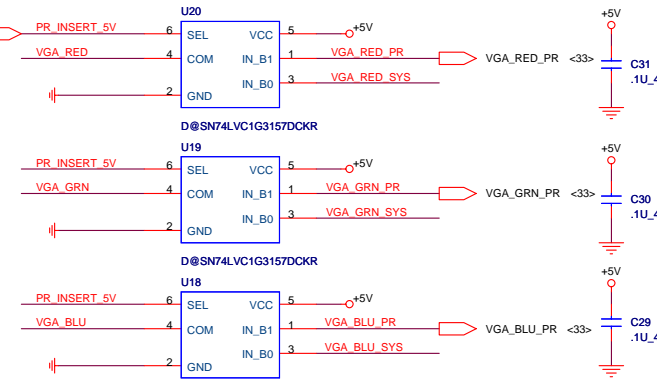


S-VIDEO



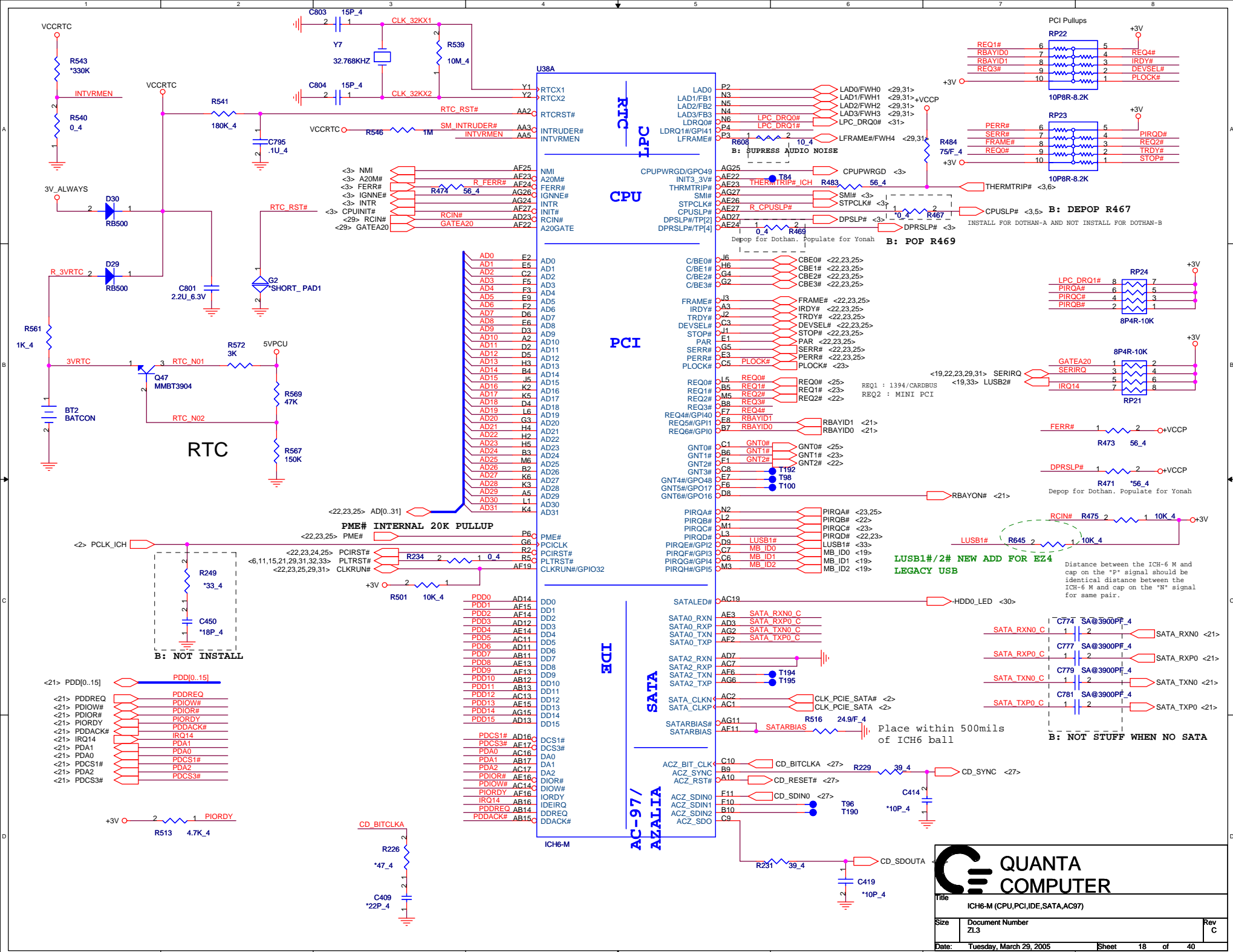


SEL	FUNCTION
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HIGH	IN_B1

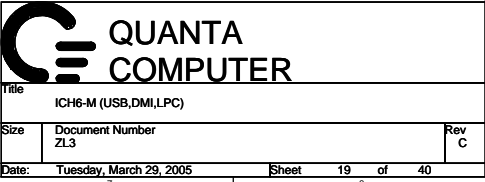


C: Change to FDV301N for Vgs issue.

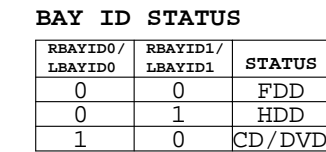
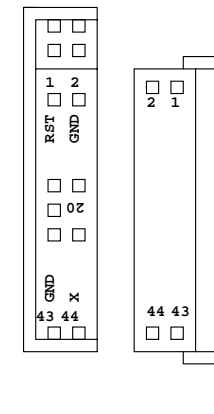
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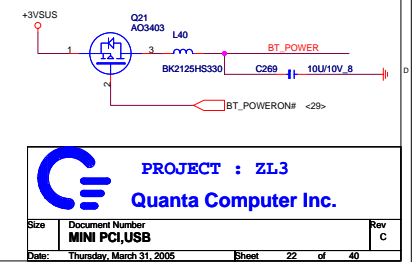






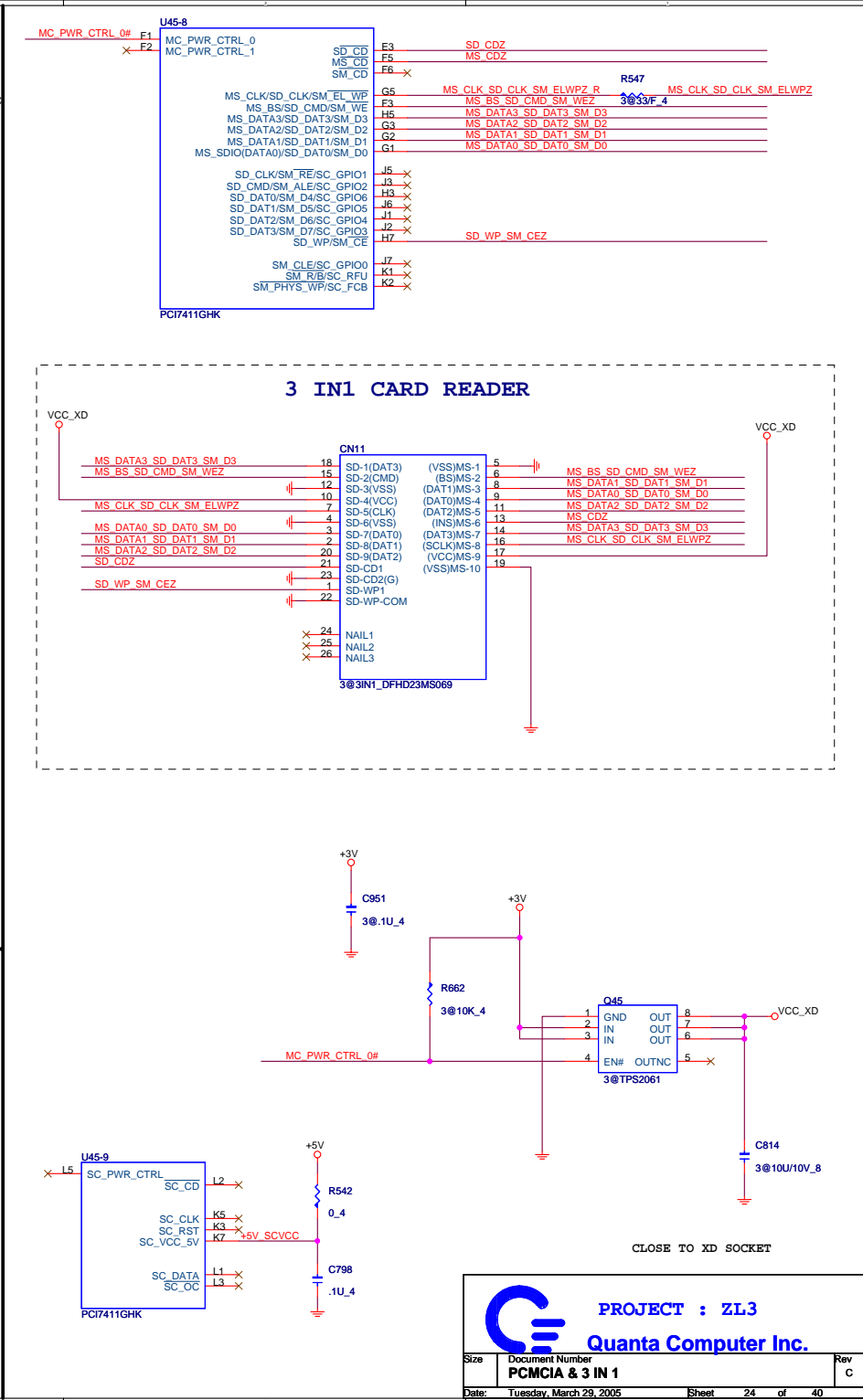
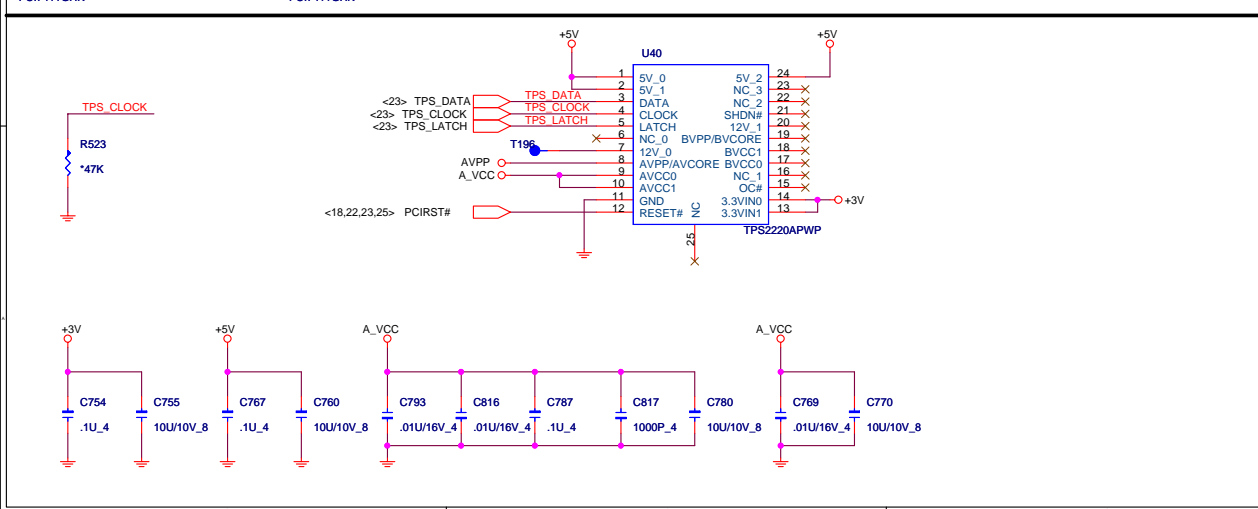
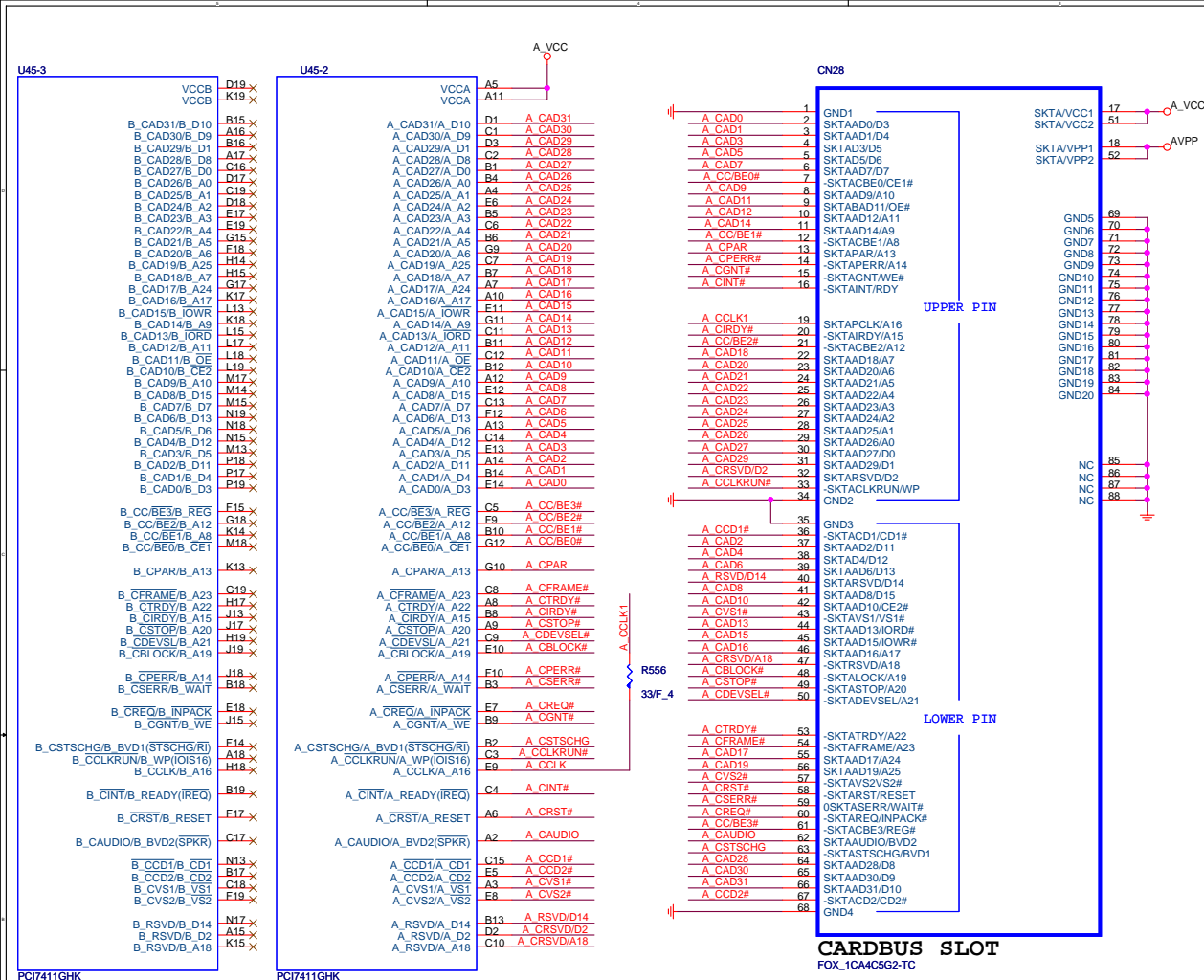


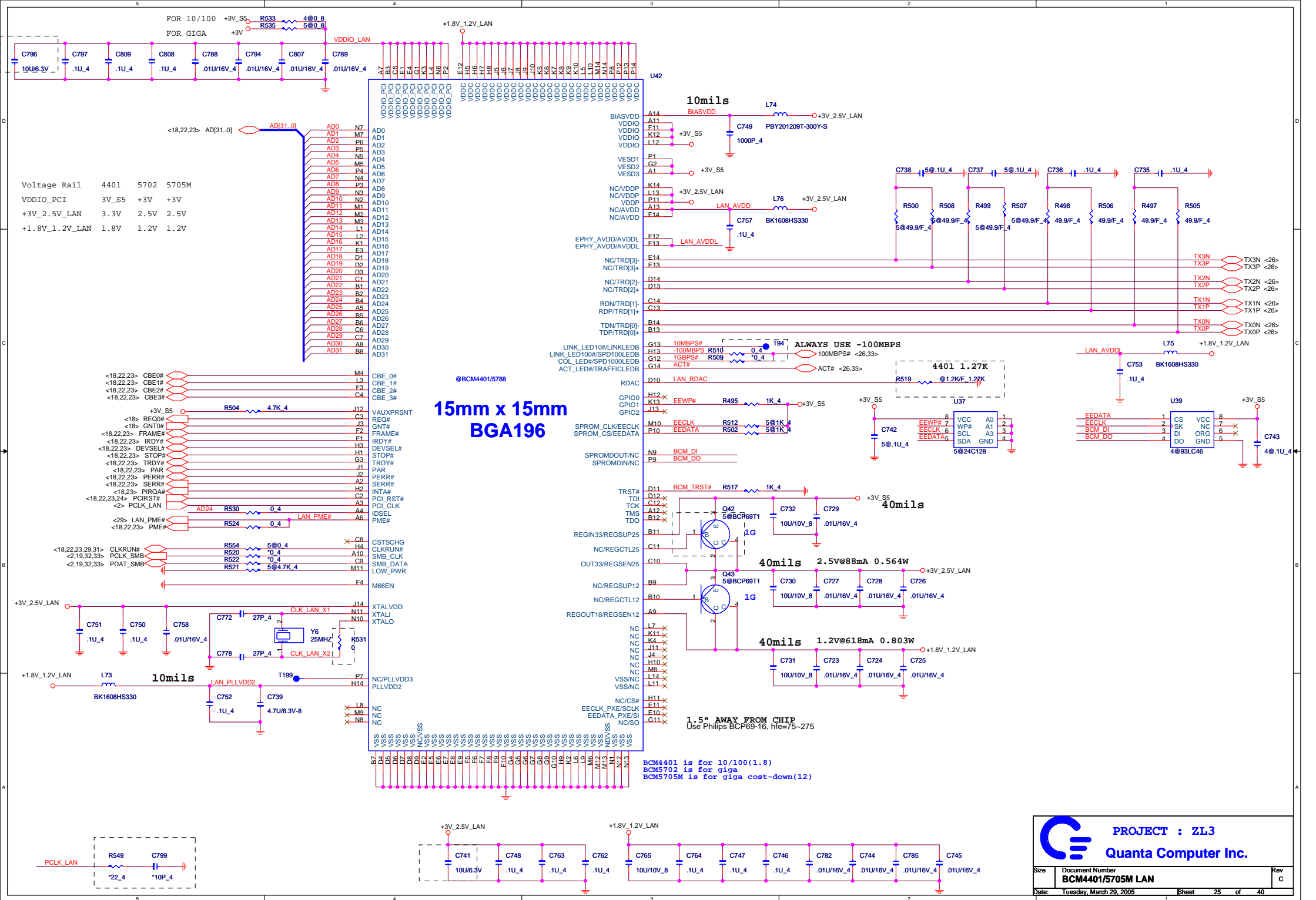


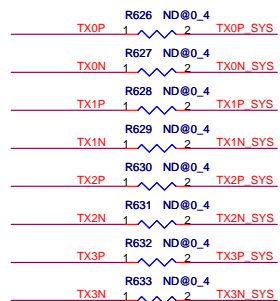
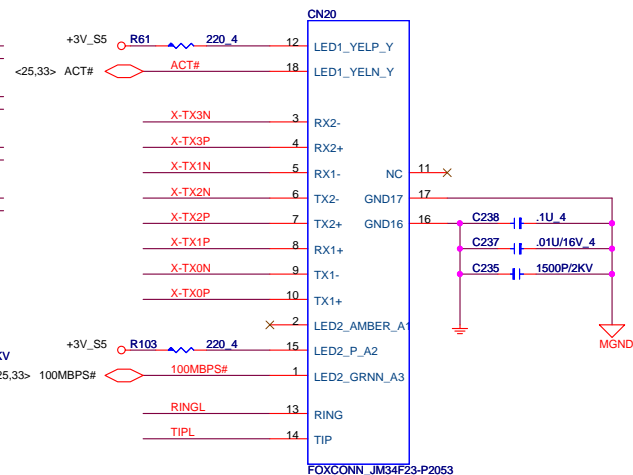
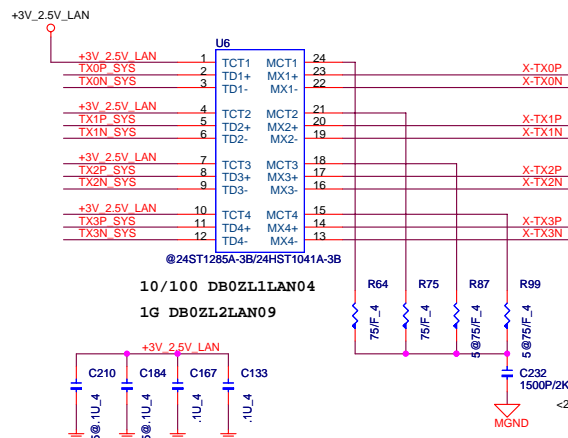
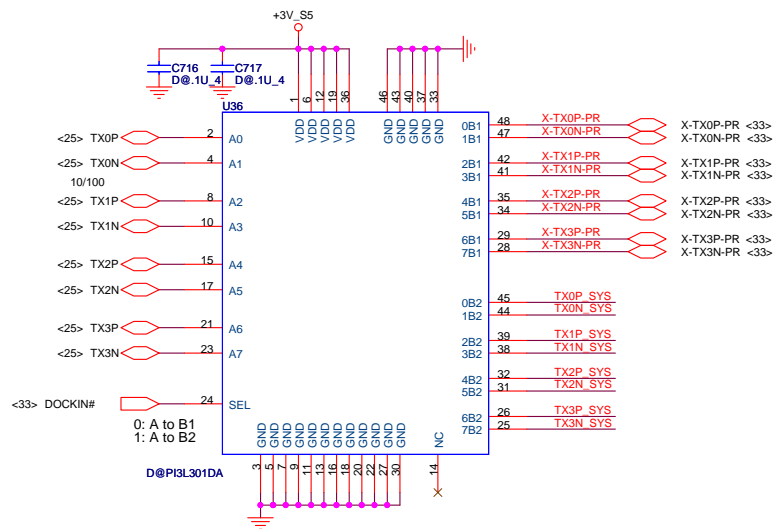
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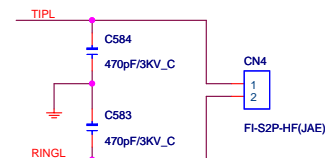






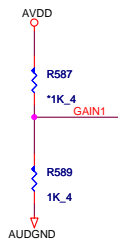


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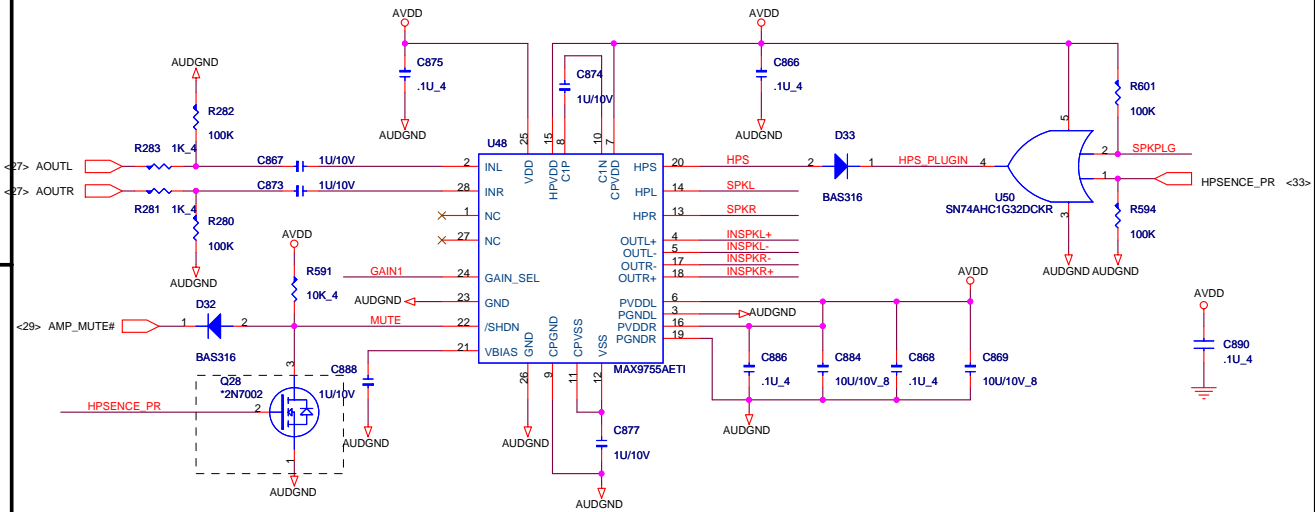
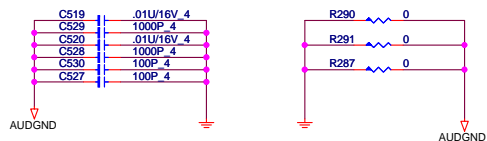
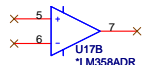
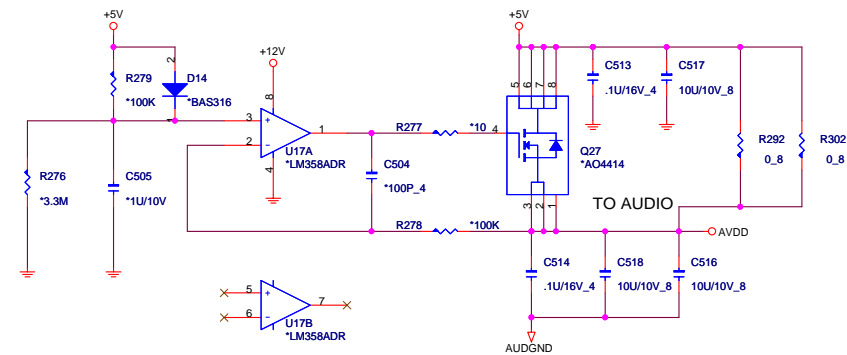




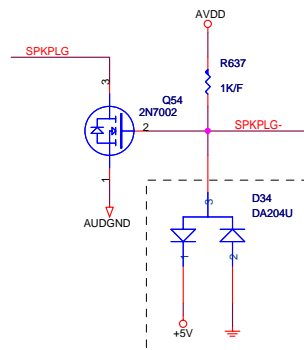
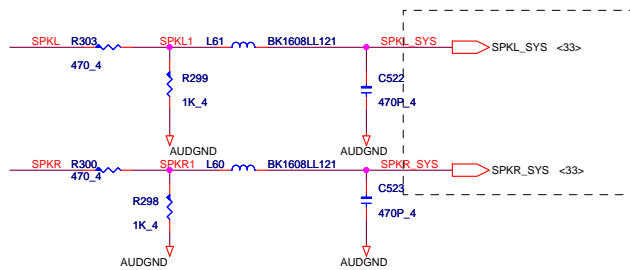
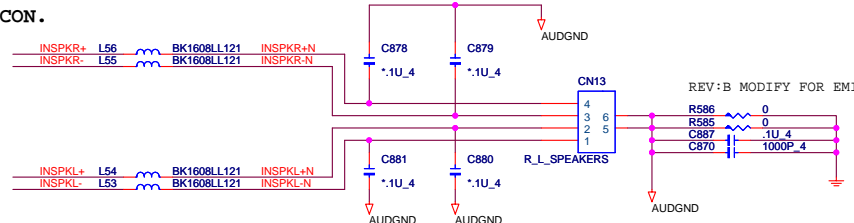
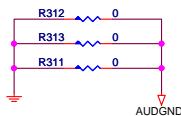
GAIN1	SPKR MODE	HP MODE
0	10.5	3
1	9	0



# AMP POWER

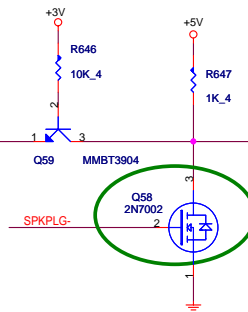
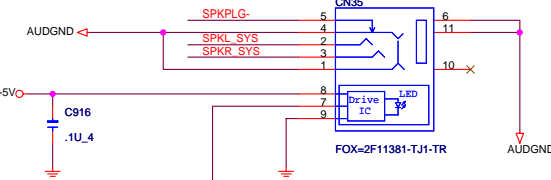


# SPEAKER CON.



F: NEW ADD FOR ESD  
CLOSE TO CN35

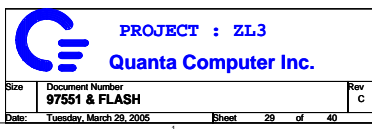
# LINE OUT&SPDIF

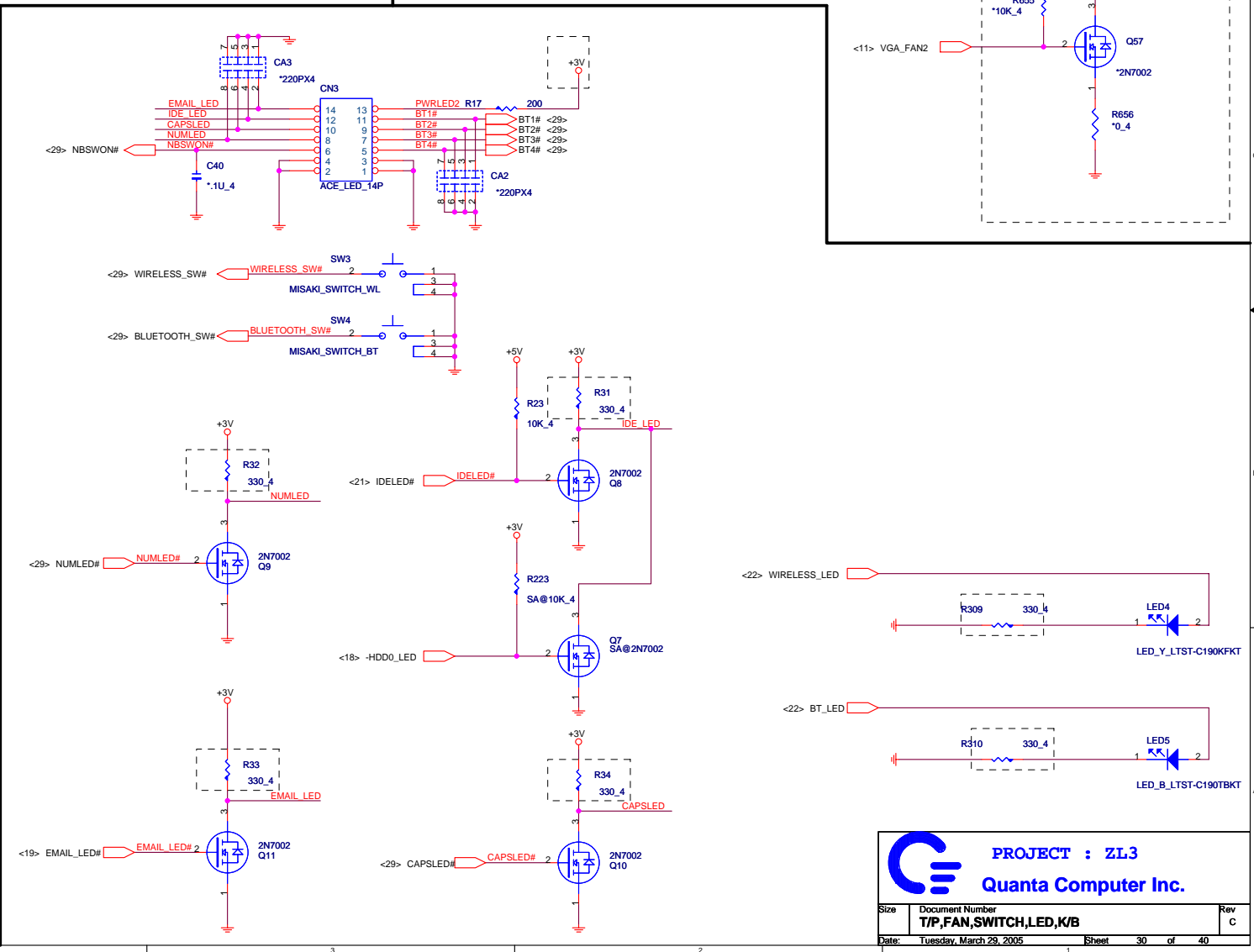
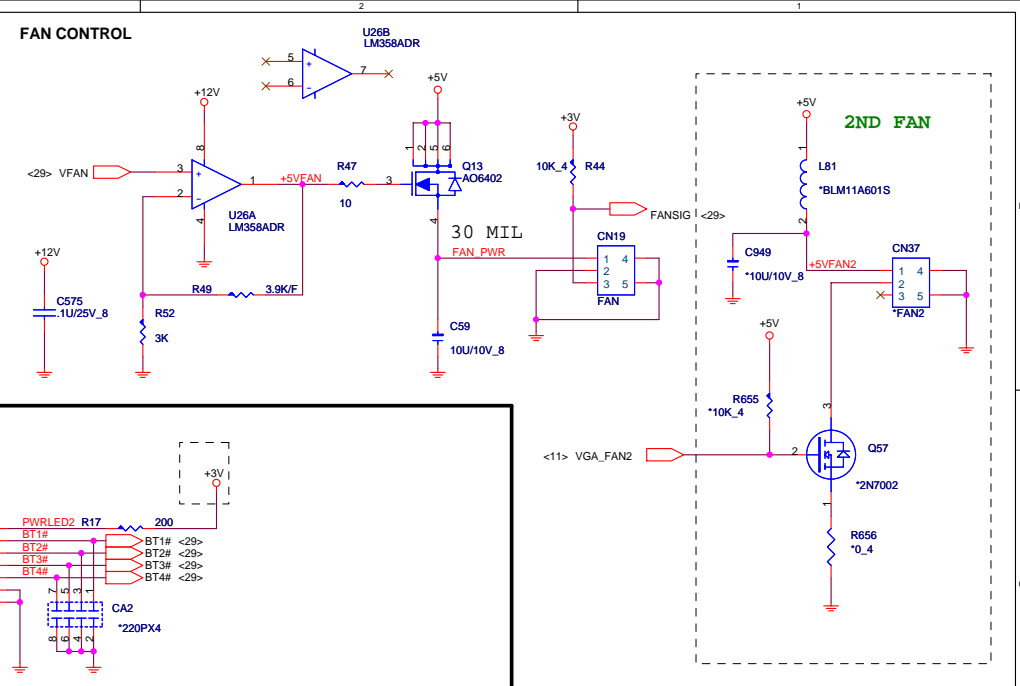


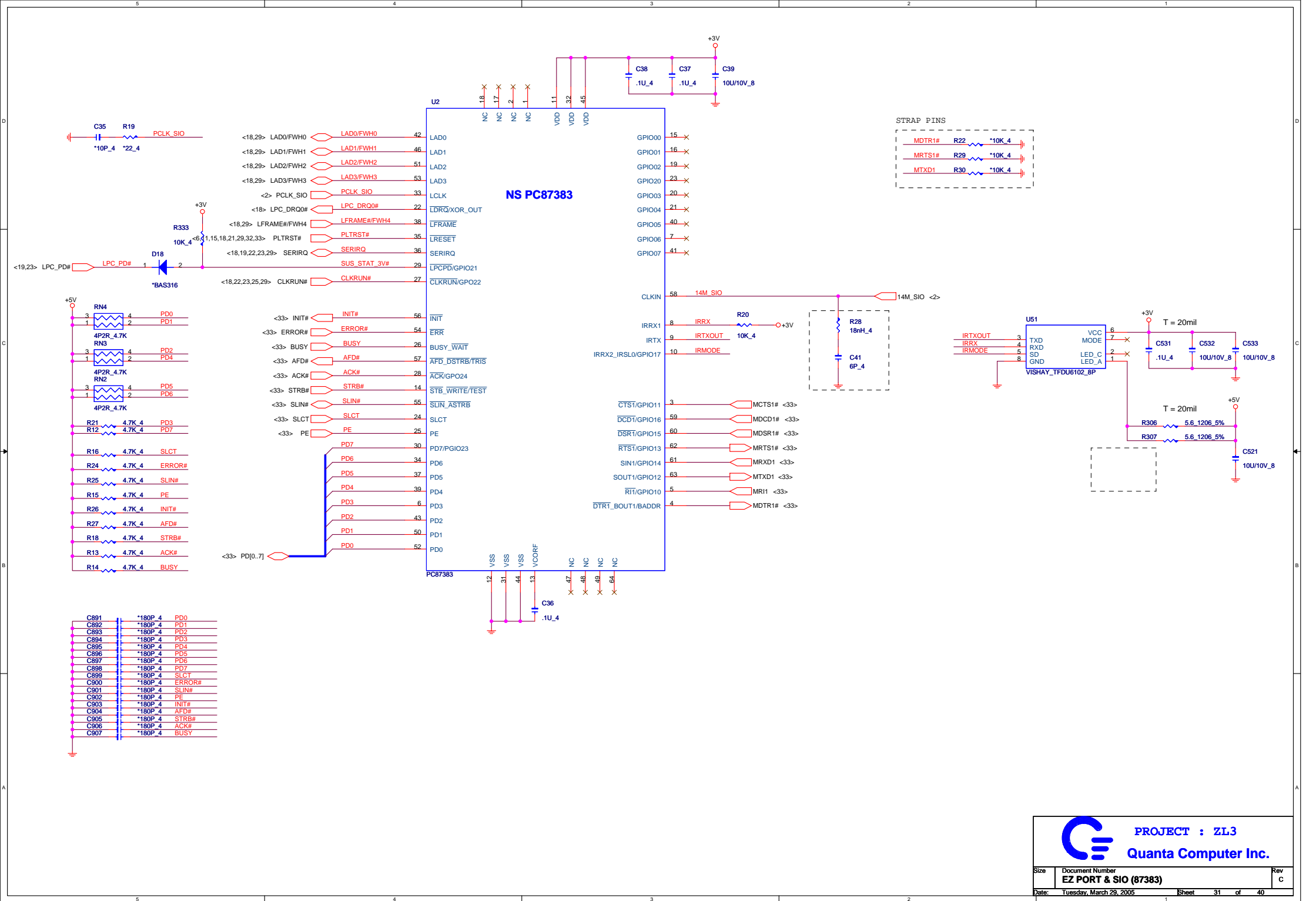
C: Change to 2N7002

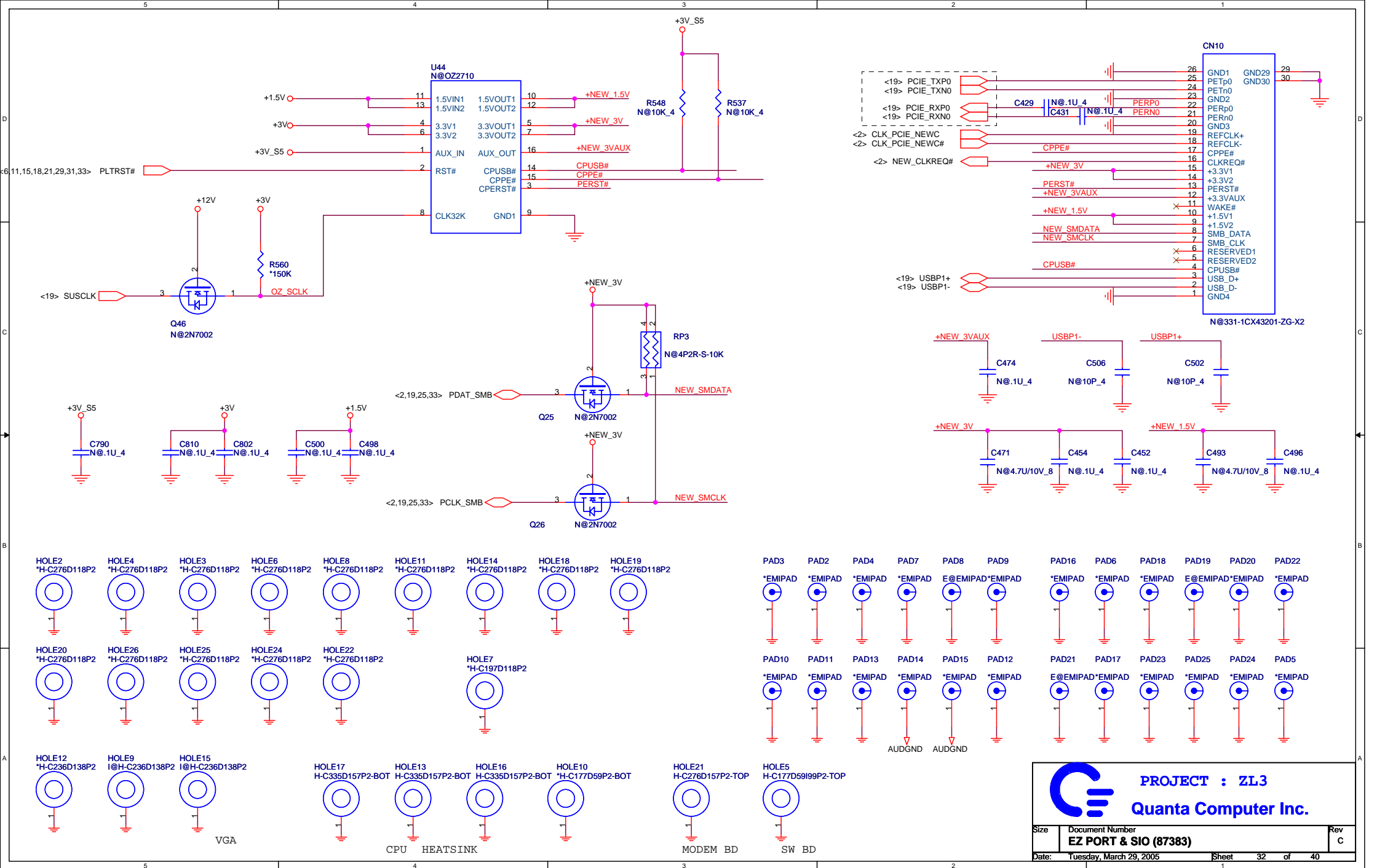
PROJECT : ZL3  
Quanta Computer Inc.



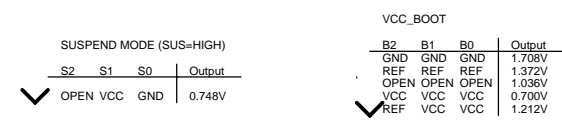









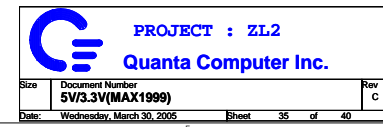




D5	D4	D3	D2	D1	D0	Output	D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	1.1986	0	0	0	0	0	0	1.7089
1	0	0	0	0	1	1.1907	0	0	0	0	0	1	1.6924
1	0	0	0	1	0	1.1644	0	0	0	0	0	0	1.6765
1	0	0	0	1	1	1.1489	0	0	0	0	0	1	1.6600
1	0	0	1	0	0	1.1329	0	0	0	0	1	0	1.6444
1	0	0	1	0	1	1.1169	0	0	0	0	1	0	1.6289
1	0	0	1	1	0	1.1009	0	0	0	0	1	1	1.6129
1	0	1	0	0	1	1.0844	0	0	0	0	1	1	1.5969
1	0	1	0	0	0	1.0689	0	0	0	1	0	0	1.5809
1	0	1	0	0	1	1.0529	0	0	0	1	0	1	1.5644
1	0	1	0	1	0	1.0369	0	0	0	0	1	0	1.5489
1	0	1	0	1	1	1.0209	0	0	0	0	1	1	1.5329
1	0	1	1	0	0	1.0044	0	0	0	0	1	0	1.5169
1	0	1	1	0	1	0.9889	0	0	0	1	0	1	1.5009
1	0	1	1	1	0	0.9729	0	0	0	1	1	0	1.4844
1	0	1	1	1	1	0.9569	0	0	0	1	1	1	1.4689
1	1	0	0	0	0	0.9409	0	1	0	0	0	0	1.4529
1	1	0	0	0	1	0.9244	0	1	0	0	0	1	1.4369
1	1	0	0	1	0	0.9089	0	1	0	0	0	1	1.4209
1	1	0	0	1	1	0.8929	0	1	0	0	1	1	1.4044
1	1	0	1	0	0	0.8769	0	1	0	0	0	0	1.3889
1	1	0	1	0	1	0.8609	0	1	0	0	1	0	1.3729
1	1	0	1	1	0	0.8444	0	1	0	0	1	1	1.3569
1	1	0	1	1	1	0.8289	0	1	0	0	1	1	1.3409
1	1	1	0	0	0	0.8129	0	1	0	1	0	0	1.3244
1	1	1	0	0	1	0.7969	0	1	0	1	0	1	1.3089
1	1	1	0	1	0	0.7809	0	1	0	1	0	1	1.2929
1	1	1	0	1	1	0.7644	0	1	0	1	0	1	1.2769
1	1	1	1	0	0	0.7489	0	1	0	1	0	1	1.2609
1	1	1	1	0	1	0.7329	0	1	0	1	1	0	1.2444
1	1	1	1	1	0	0.7169	0	1	1	0	1	0	1.2289
1	1	1	1	1	1	0.7009	0	1	1	1	0	1	1.2129

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	Quanta Computer Inc.	
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	CPU CORE (MAX1907)	C
Date:	Wednesday, March 30, 2005	
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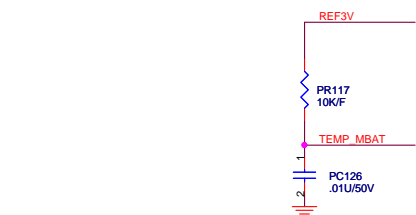
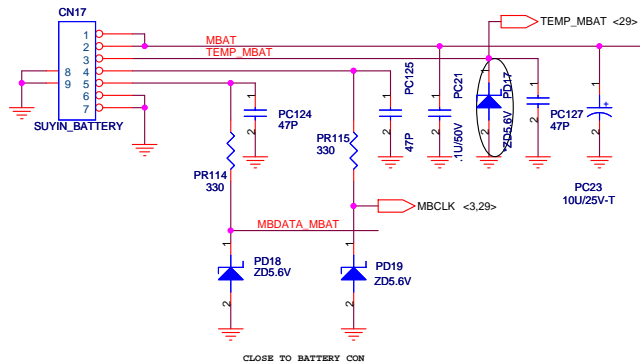




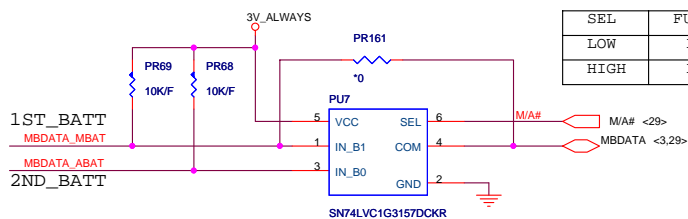
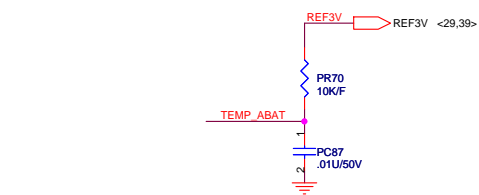
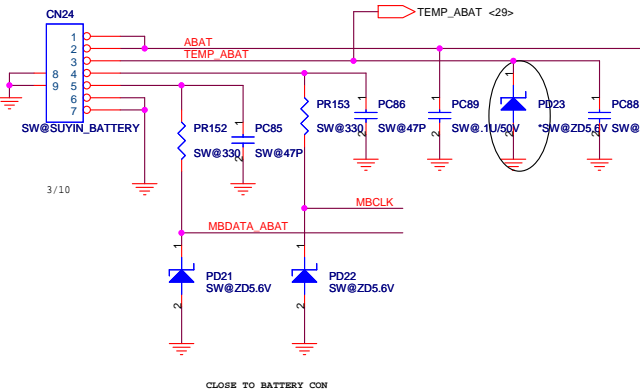




# 1ST\_BATT\_CONN



# 2ND\_BATT\_CONN



SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1

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Quanta Computer Inc.

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	<b>BATTERY SELECT</b>	C
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