

REVISION HISTORY

PCI RESOURCE TABLE

SA-2:

- 1.GPIO 16,pull-high take it away, (DUMMY R537)
- 2.CODEC,S/PDIF,10K PULL DOWN (ADD R539)
- 3.PANEL ID FROM SIO
- 4.LCDPOWER_S0 FUSE/1A (RAYCHEM)
- 5.USB .fuse-->RAYCHEM
- 6.RTL8100.PIN80-->1K-->3D3V
- 7.FDD POWER RAIL-->1A FUSE
- 8.CODECP/N UPDATE:71.09766.A0G
- 9.DB1,DB3,DB4 CHANGE SOURCE

NOTE:
1.F2 : NOT RAYCHEM

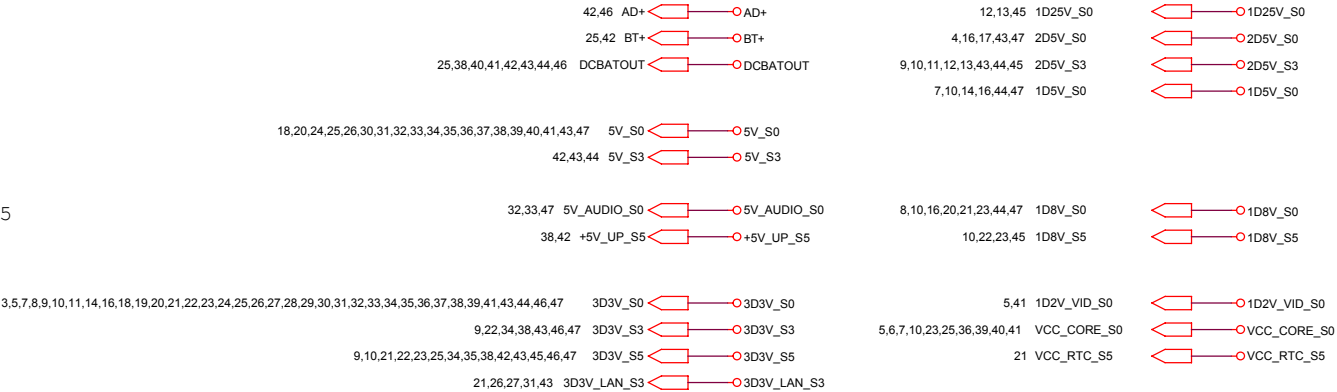
SB:

- 1. REPLACE F5 with type of F1 (ok)
- 2. U35,pin4 MUST PH 47K(R280)? (No)
- 3. PUT R537 BACK? (no)
- 4. audio:short BC617,BC584?(no)
- 5. audio:remove BC583,R139,R138,BC135(no)
- 5. audio:remove BC618,R180,R181,BC164(no)
- 7. audio:modify BC584 and BC617 to 33nF(no)
- 8. CPU ripple issue:capacitor-->77.22271.071(ok)
- 9. BC8,BC21-->DUMMY
- 10. EMI:L5,L8,L11,L14,L15,L33,L40,L41,L42,L43(68.00082.321)-->0805 00hm
EMI:L1(68.00089.081)-->delete
EMI:L30(63.R0003.161)-->0805 00hm
EMI:L31(68.4R72B.1F1)-->0805 00hm
- 11.USB,l fuse for l port
- 12. 2*4P 14.318MHz
- 13 DB10
- 14 MIC C42
- 15 BL3
- 16 WOL
- 17 text on Page21
- 18 TC11 shift lmm
- 19 CLK33_PCM

SC

- 1.Board revision ID
- 2.USB controller change;replace USB port3 with port5
- 3.KBC-P60-->EN_MINI_PCI
- 4.VGA floating input-->PD "SSIN","SSOUT",HPD"
- 5.

DEVICE	IDSEL	PCI IRQ	REQ#/GNT#
INTERNAL_LAN	AD13	INTC#/INTG#	
EXTERNAL_LAN	AD18	INTD#	REQ4#/GNT4#
Mini-PCI	AD21	INTC#	REQ3#/GNT3#
IEEE 1394	AD13		
USB 2.0 USB 1.1	AD14		
	AD14	INTD#/INTE# INTD#/INTH#	
CARDBUS	AD20	INTA#	REQ1#/GNT1#
LPC	AD13		
AC97	AD13	INTC#/INTF#	
IDE	AD13	INTH#	



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Title

REVISION HISTORY

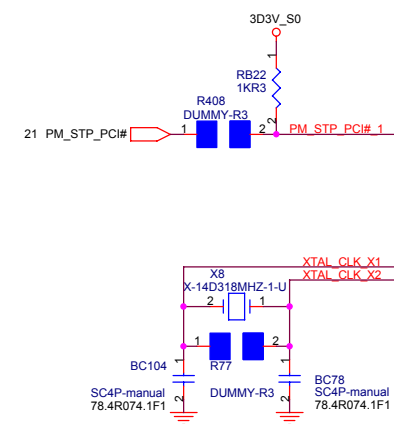
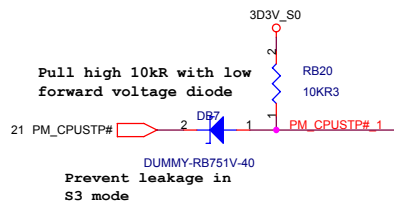
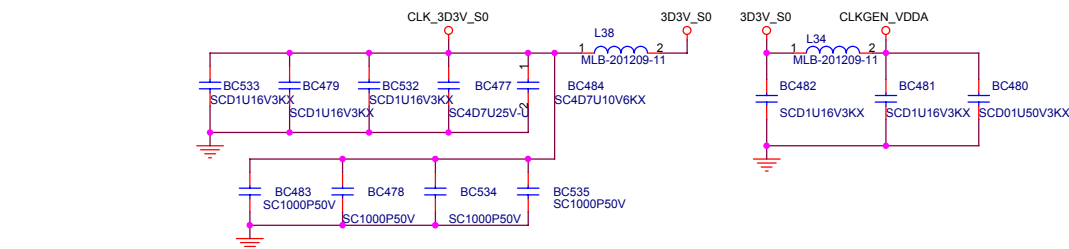
Size
A3

Document Number
TOUCAN2

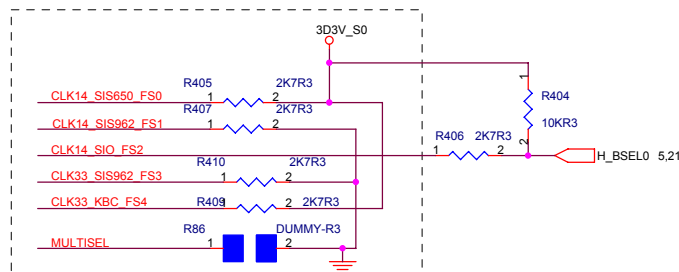
Rev
1

Date: Wednesday, December 18, 2002

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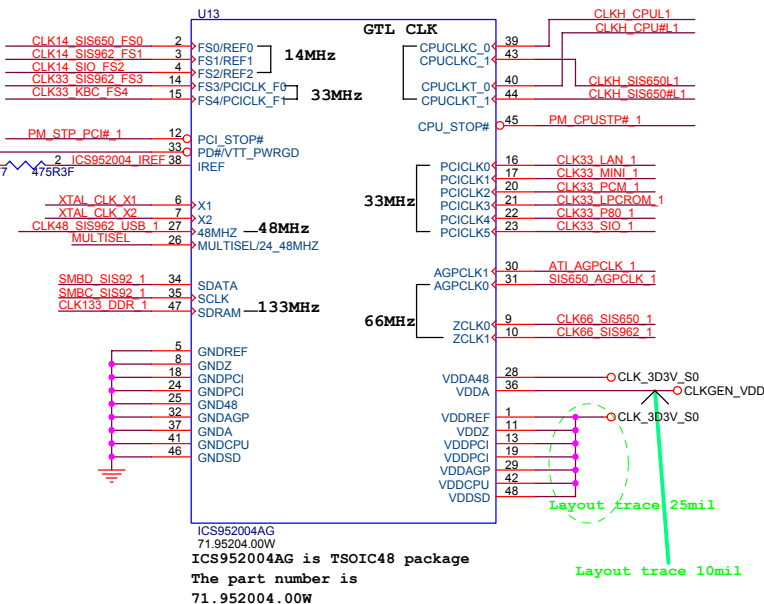


The frequency can be program by software



FREQUENCY TABLE									
FS4	FS3	FS2	FS1	FS0	CPU	DDRRAM	ZCLK	AGPCLK	PCI
0	0	0	0	0	66.67	66.67	66.67	66.67	33.33
0	0	0	0	1	100.00	100.00	66.67	66.67	33.33
0	0	0	1	1	100.00	133.33	66.67	66.67	33.33
1	0	0	0	1	100.90	100.90	67.27	67.27	33.63
1	0	1	0	1	133.33	100.00	66.67	66.67	33.33

Default Setting



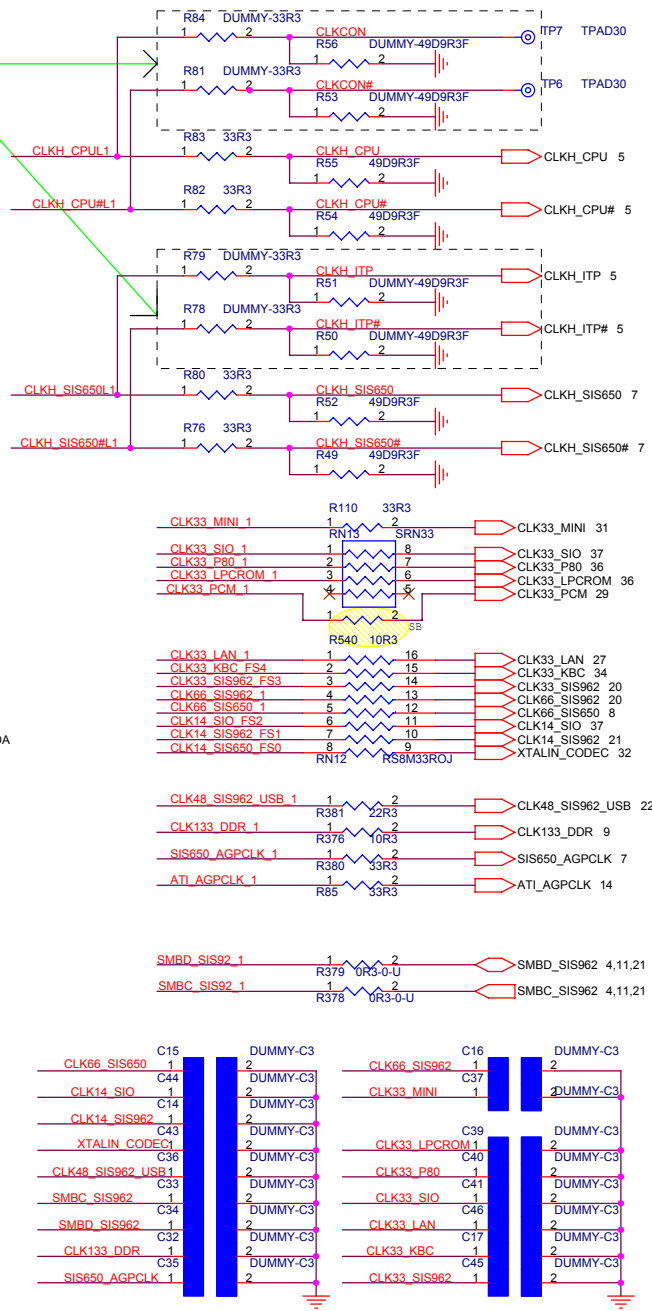
CLOCK GROUP	JITTER	SKEW	NOTE
HOST: CPUCLK0/#, CPUCLK1/#	<0.25ns	<0.4ns	1, 2
HOST Bus To Memory Bus: CPUCLK1/#, SDCLK	<0.25ns	<0.4ns	
MuTIO: ZCLK0, ZCLK1	<0.25ns	<0.325ns	
AGP: ACLK0, ACLK1	<0.25ns	<0.325ns	
PCI Bus: PCICLK_F[0:1], PCICLK[0:5]	<0.5ns	<0.65ns	

Note:

- These skews are all calculated at the receiver's clock pin, including clock driver pin to pin skew and PCB clock routing skew.
- All skews are reference to the crossing point for differential clock signals and 1.5V rising edge for 3.3V clock signals.

R1,R3,R9,R11 please as possible closed to trace's branch node.

Layout trace 25mil
Layout trace 10mil



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CLOCK GENERATOR

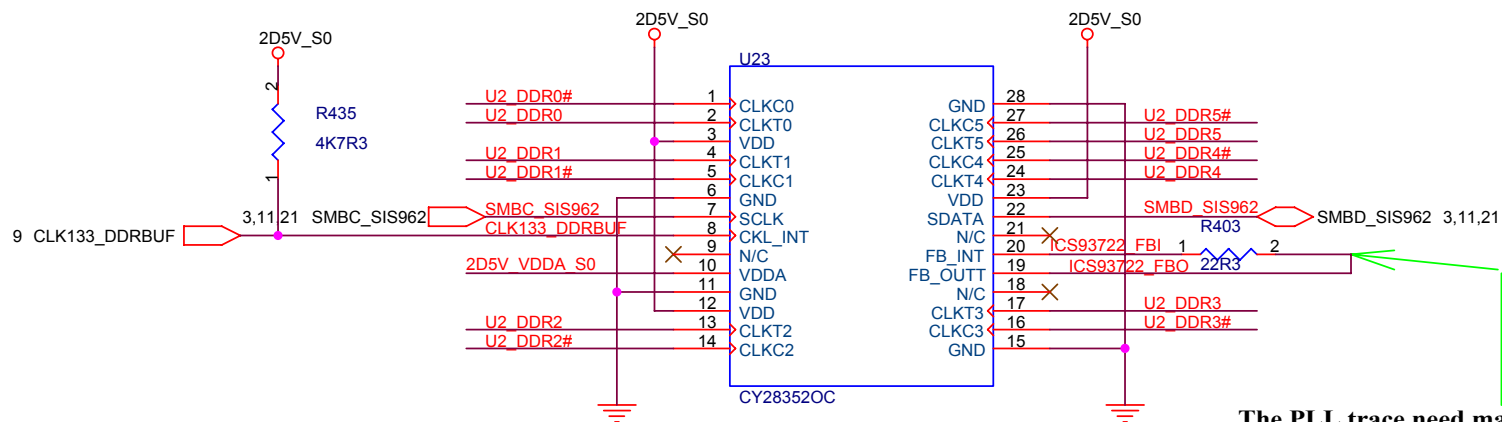
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TOUCAN2

Date: Wednesday, December 18, 2002

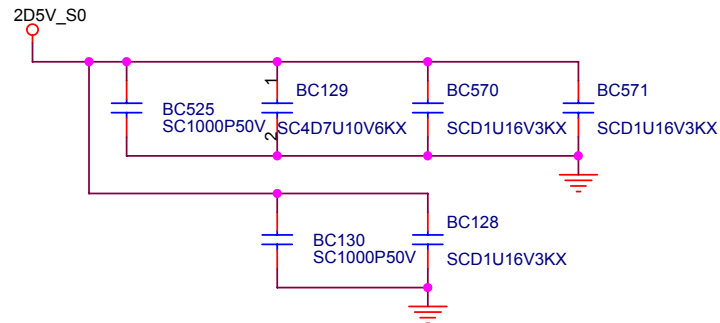
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Rev 1

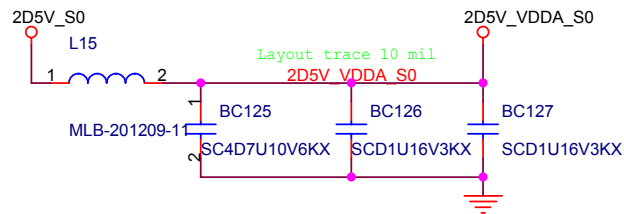


H2U
P/N: 71.93732.00I

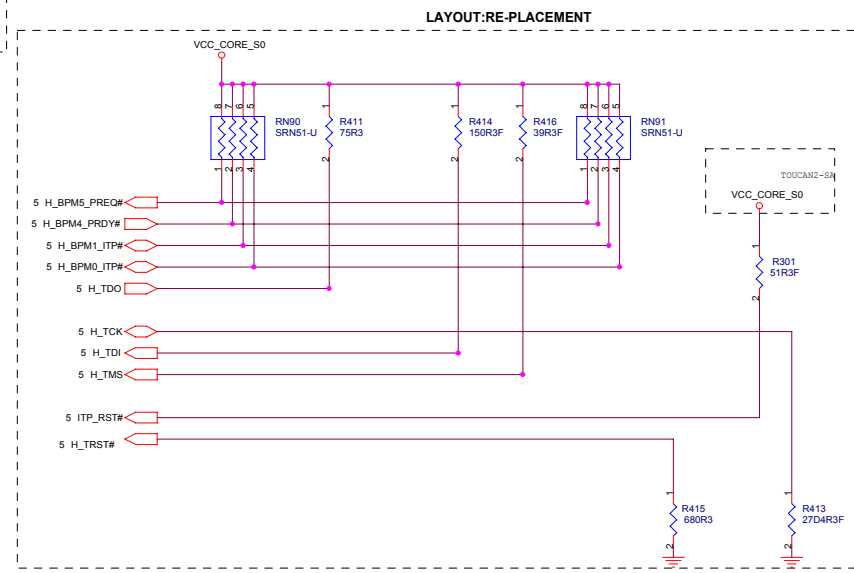
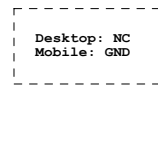
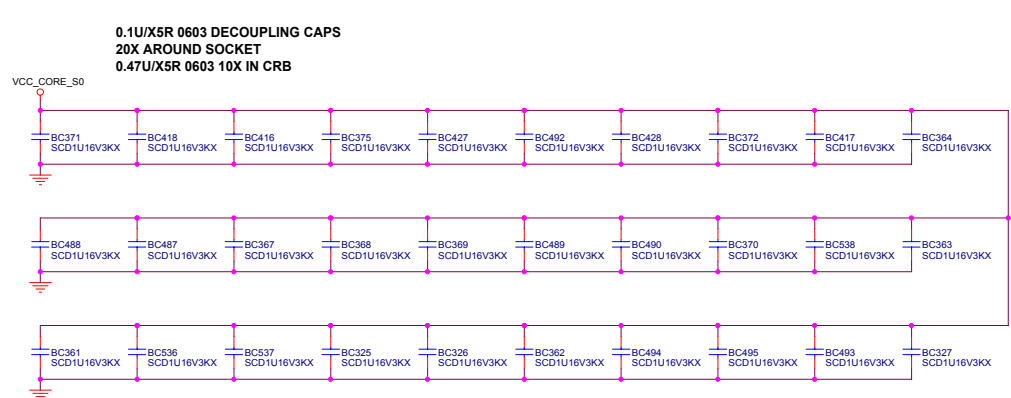
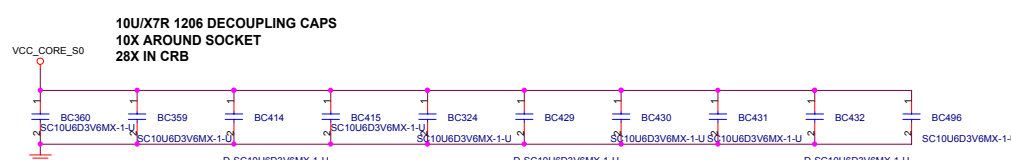
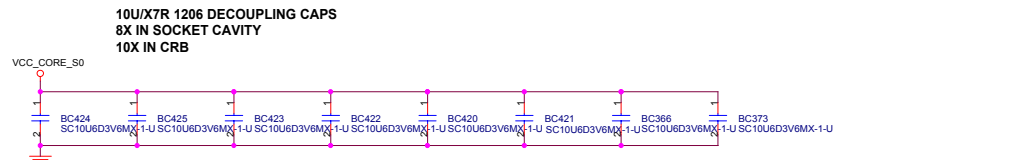
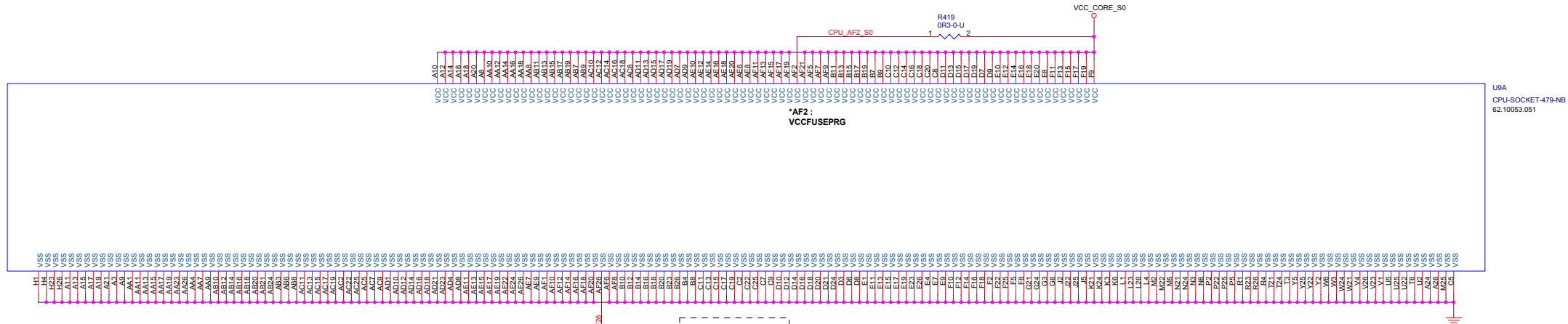
The PLL trace need match the specific
 $L4 = L2 + L3 - L1 + 3.2''$
L2 : SiS645 to Buffer length.($< 6''$)
L3 : Buffer to DIMM socket length.($< 4''$)
L1 : 2'' ~ 4''(SiS645 to DDR-Socket)
L4 = need less 12.6''

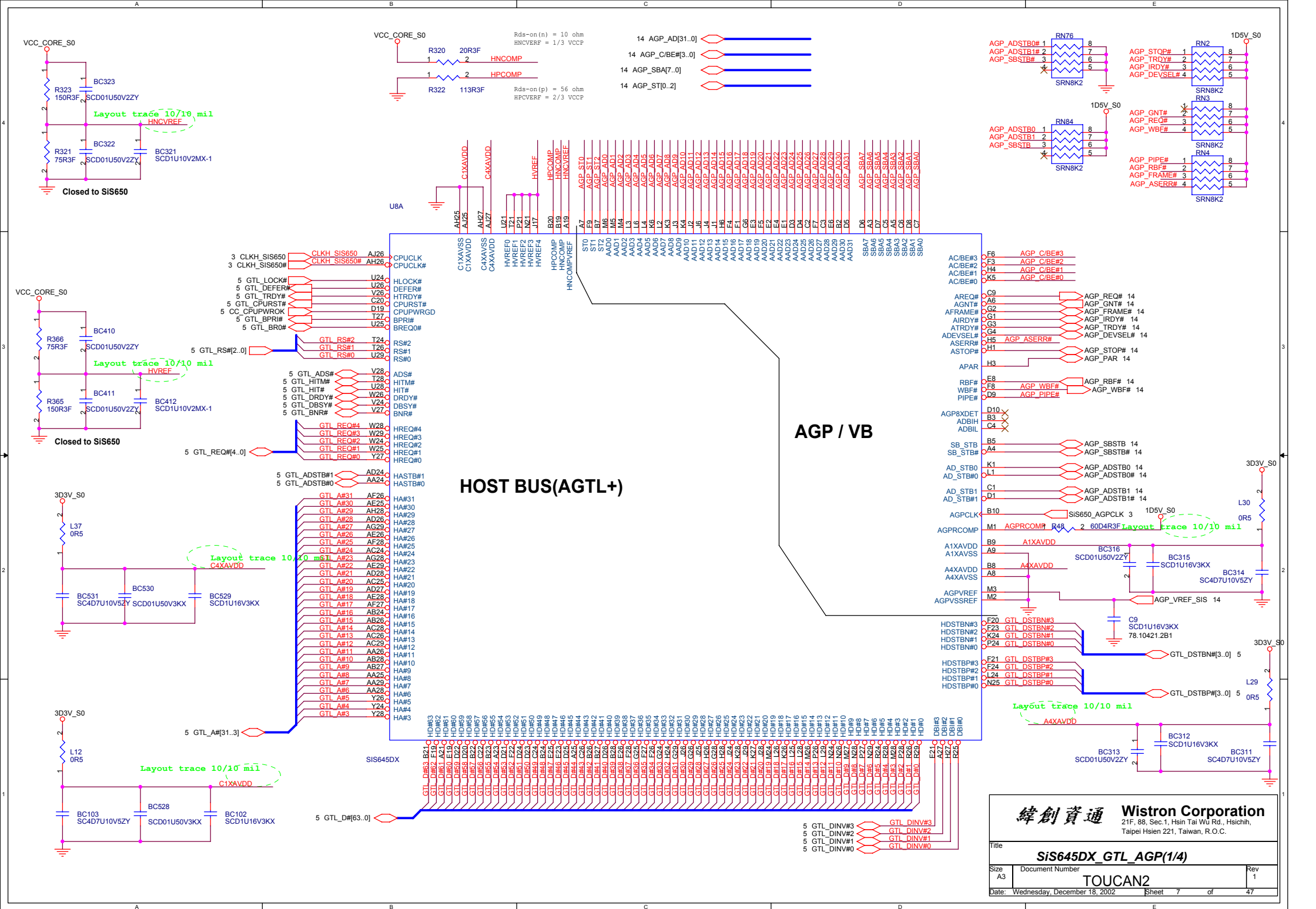


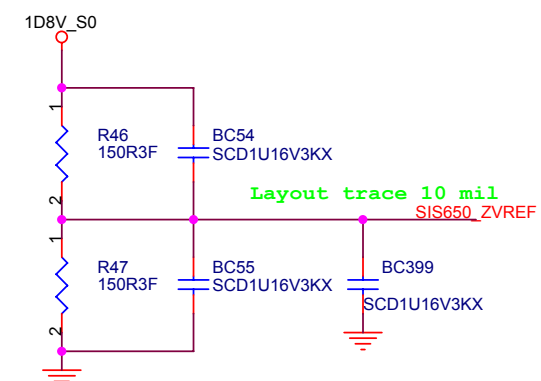
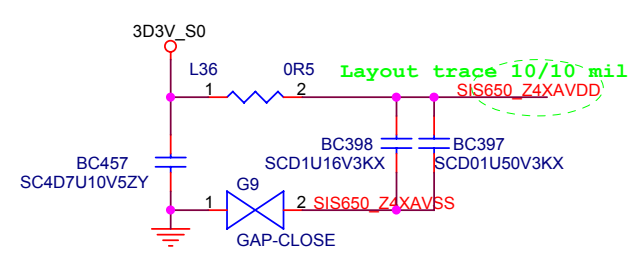
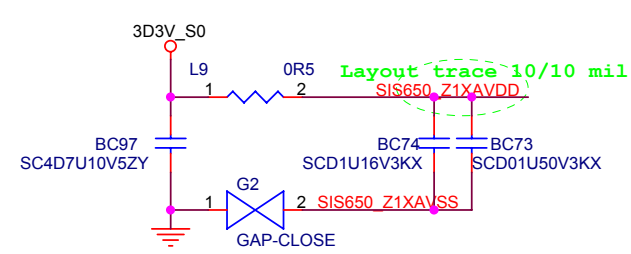
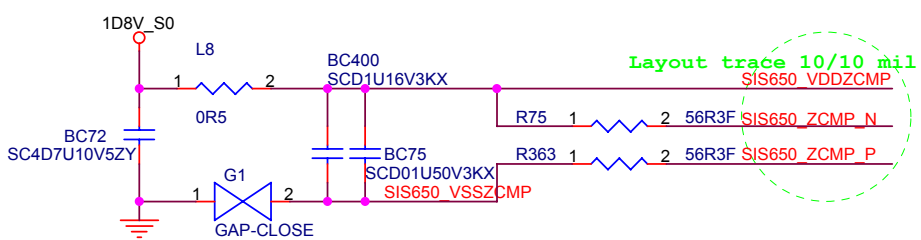
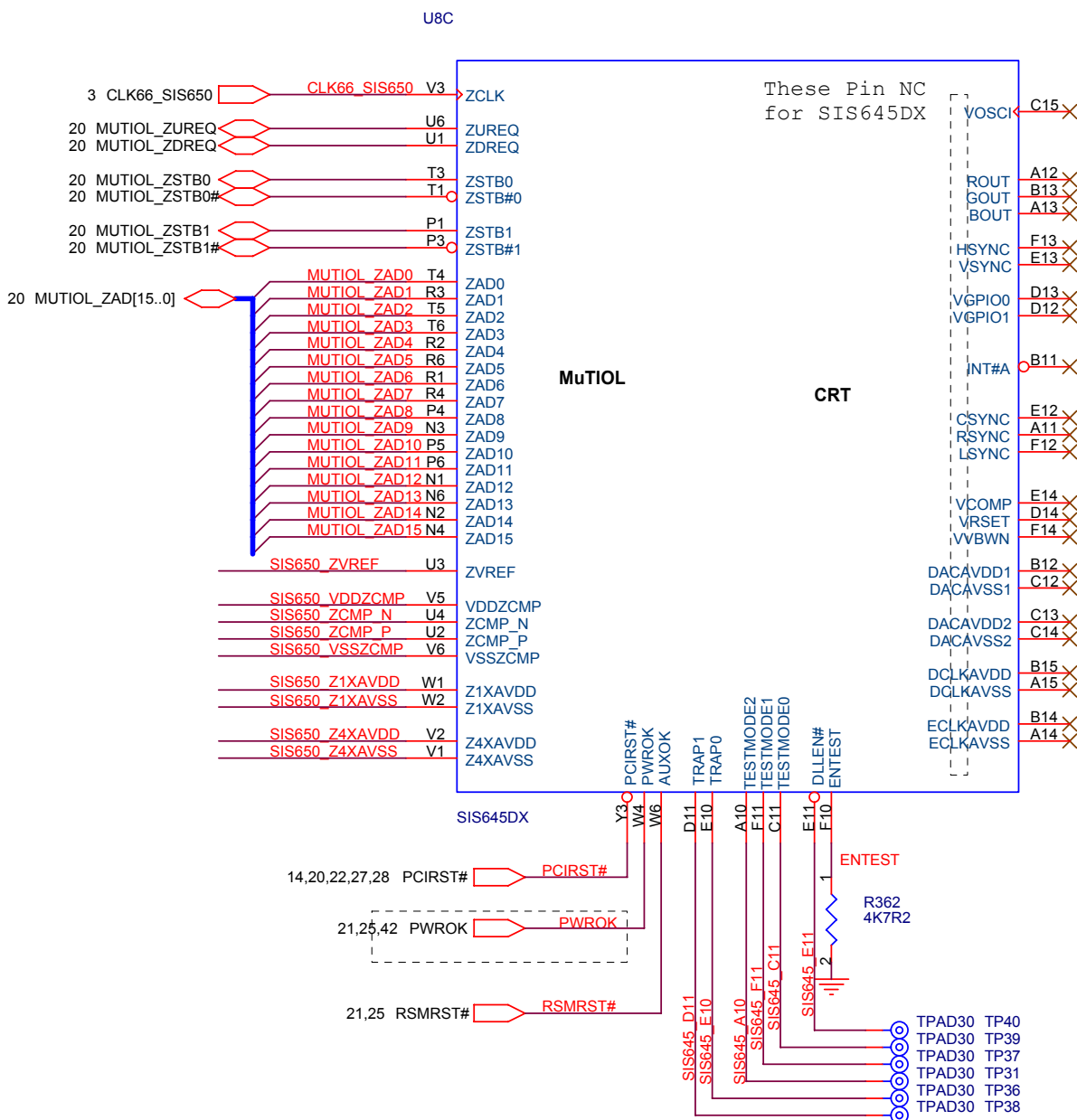
U2_DDR0#	R170	1	2	0R2-0	CLK_DDR0#	CLK_DDR0#	11
U2_DDR0	R171	1	2	0R2-0	CLK_DDR0	CLK_DDR0	11
U2_DDR1	R173	1	2	0R2-0	CLK_DDR1	CLK_DDR1	11
U2_DDR1#	R172	1	2	0R2-0	CLK_DDR1#	CLK_DDR1#	11
U2_DDR2	R132	1	2	0R2-0	CLK_DDR2	CLK_DDR2	11
U2_DDR2#	R133	1	2	0R2-0	CLK_DDR2#	CLK_DDR2#	11
U2_DDR5#	R213	1	2	0R2-0	CLK_DDR5#	CLK_DDR5#	11
U2_DDR5	R212	1	2	0R2-0	CLK_DDR5	CLK_DDR5	11
U2_DDR4#	R217	1	2	0R2-0	CLK_DDR4#	CLK_DDR4#	11
U2_DDR4	R218	1	2	0R2-0	CLK_DDR4	CLK_DDR4	11
U2_DDR3	R216	1	2	0R2-0	CLK_DDR3	CLK_DDR3	11
U2_DDR3#	R215	1	2	0R2-0	CLK_DDR3#	CLK_DDR3#	11

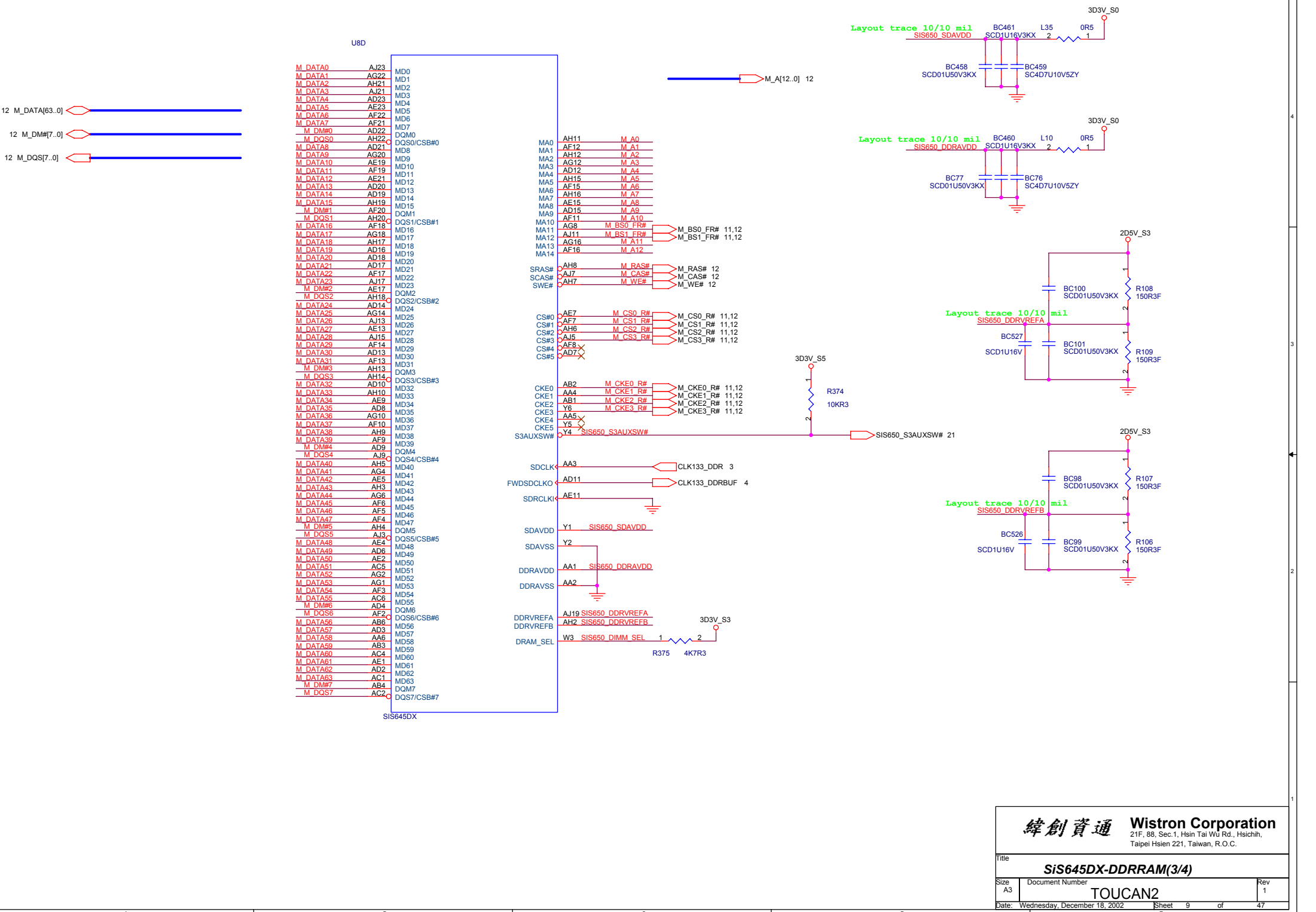


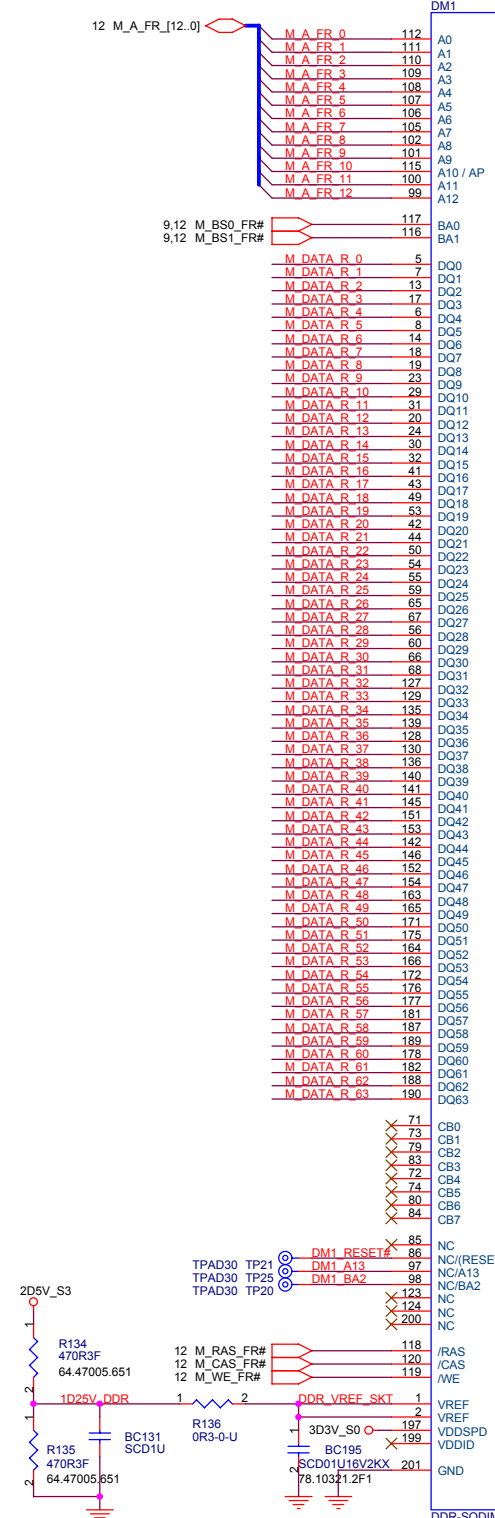
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
DDRCLK_BUFFER		
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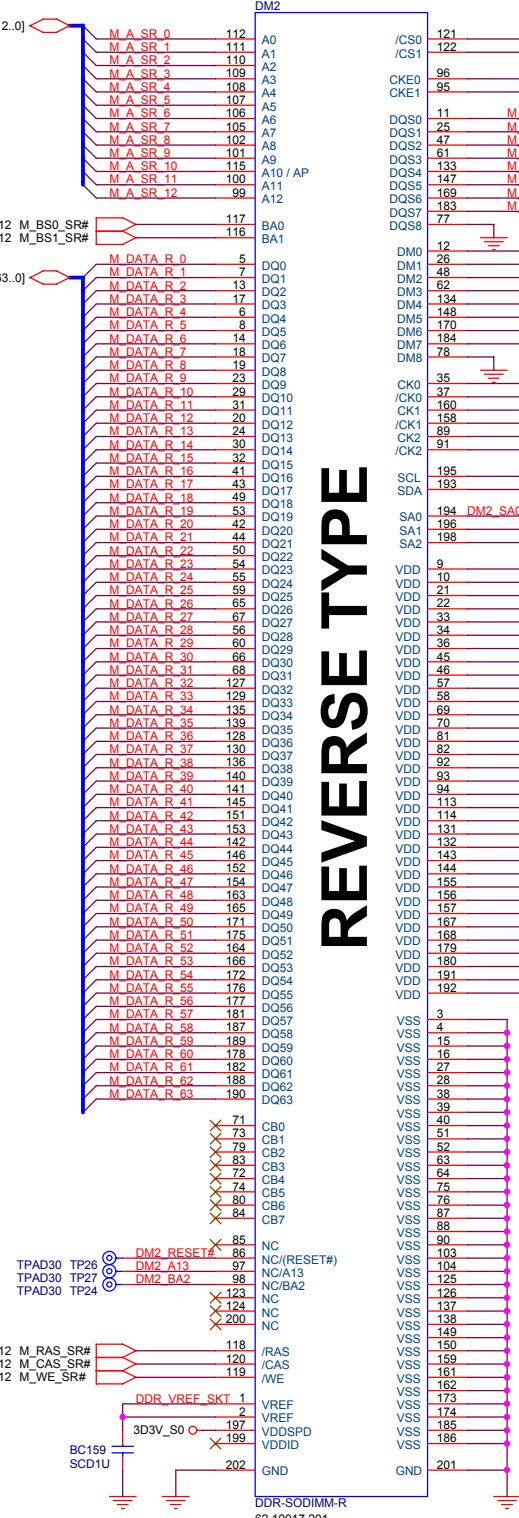
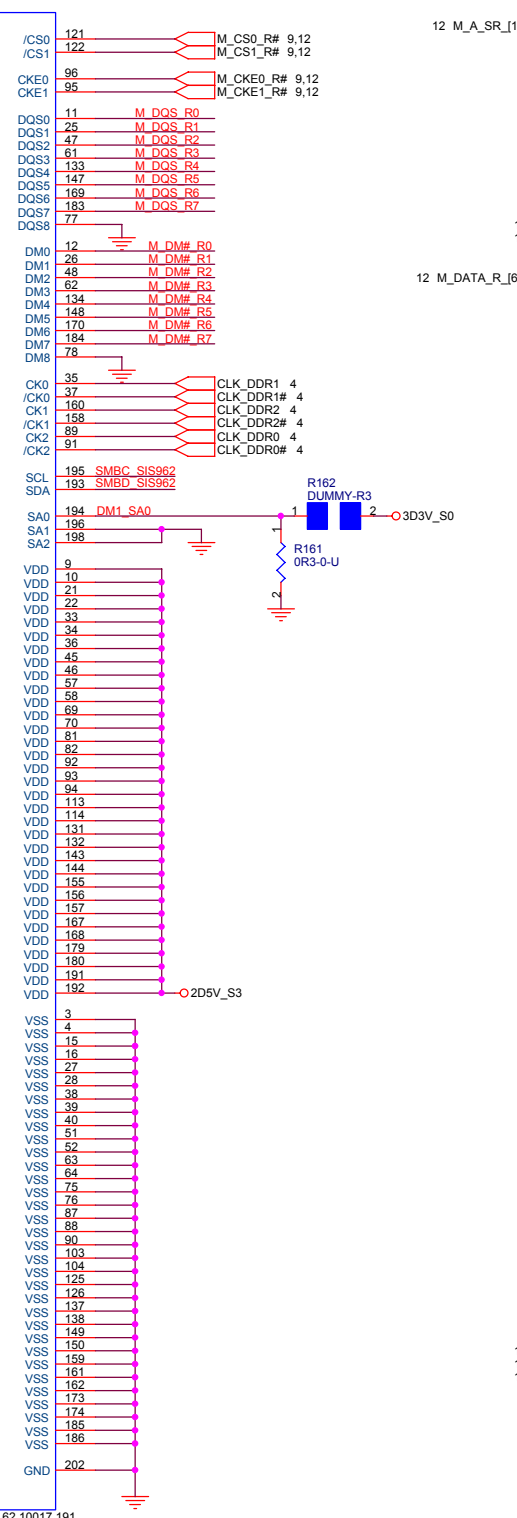




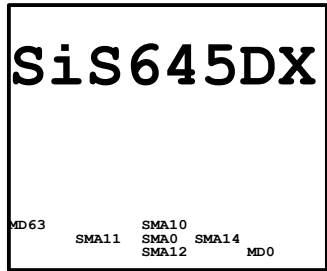
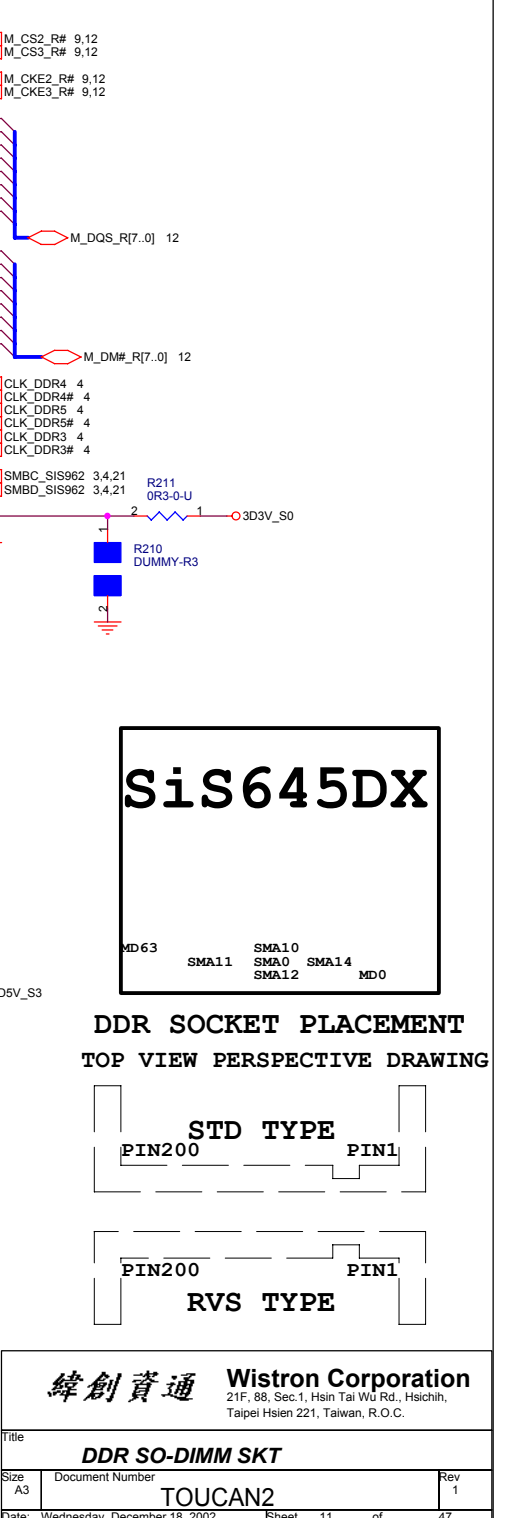




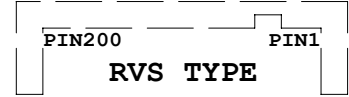
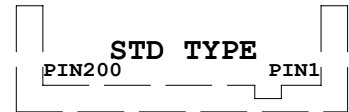
NORMAL TYPE



REVERSE TYPE



DDR SOCKET PLACEMENT
TOP VIEW PERSPECTIVE DRAWING



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Title

DDR SO-DIMM SKT

Size
A3

Document Number
TOUCAN2

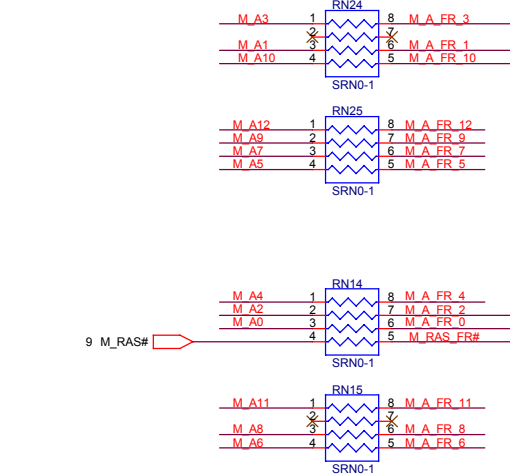
Date: Wednesday, December 18, 2002

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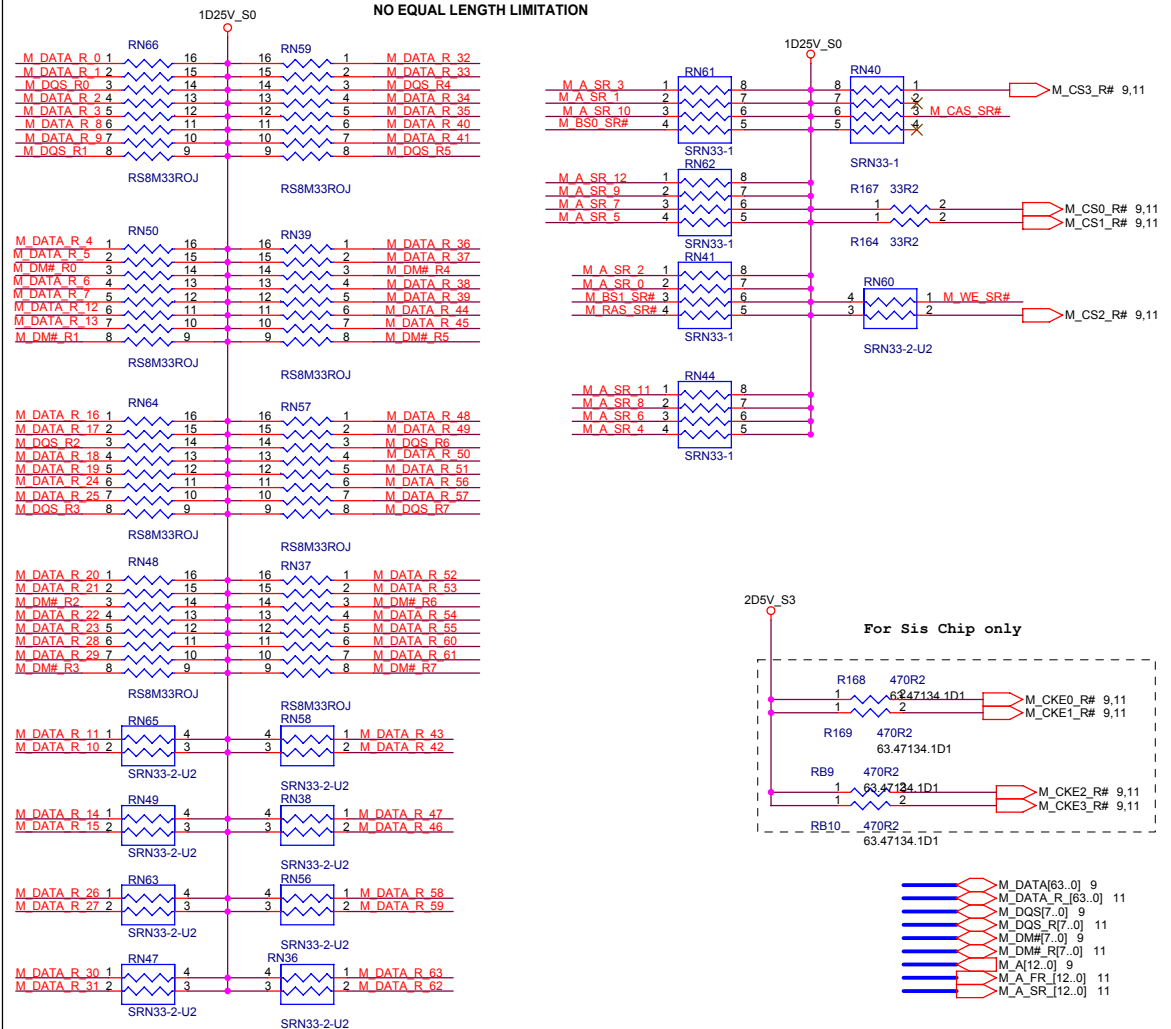
of
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Rev
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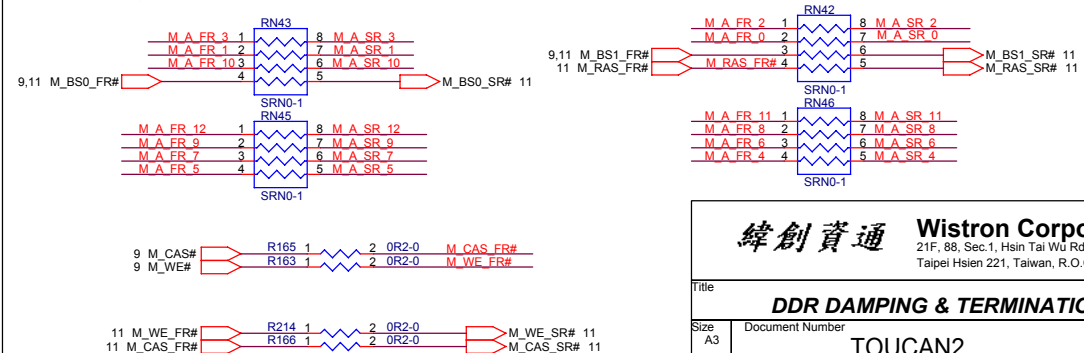
STRICT EQUAL LENGTH LIMITATION WITH DQS, CB PINS

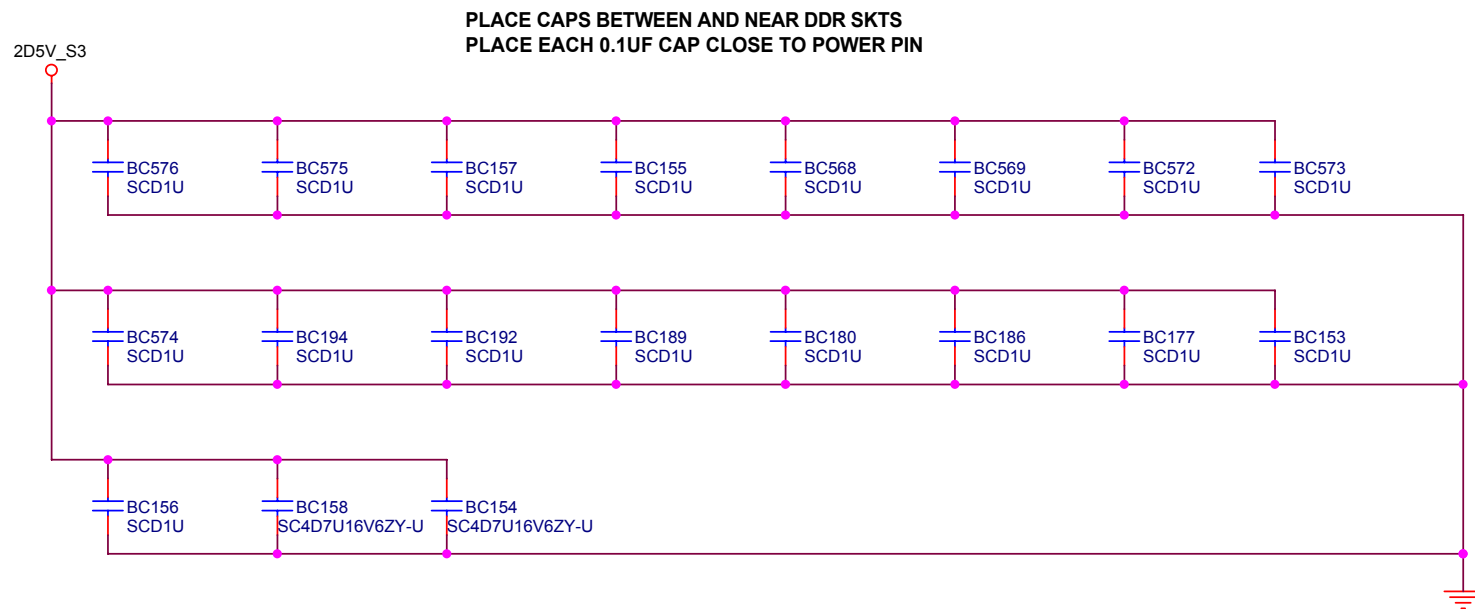
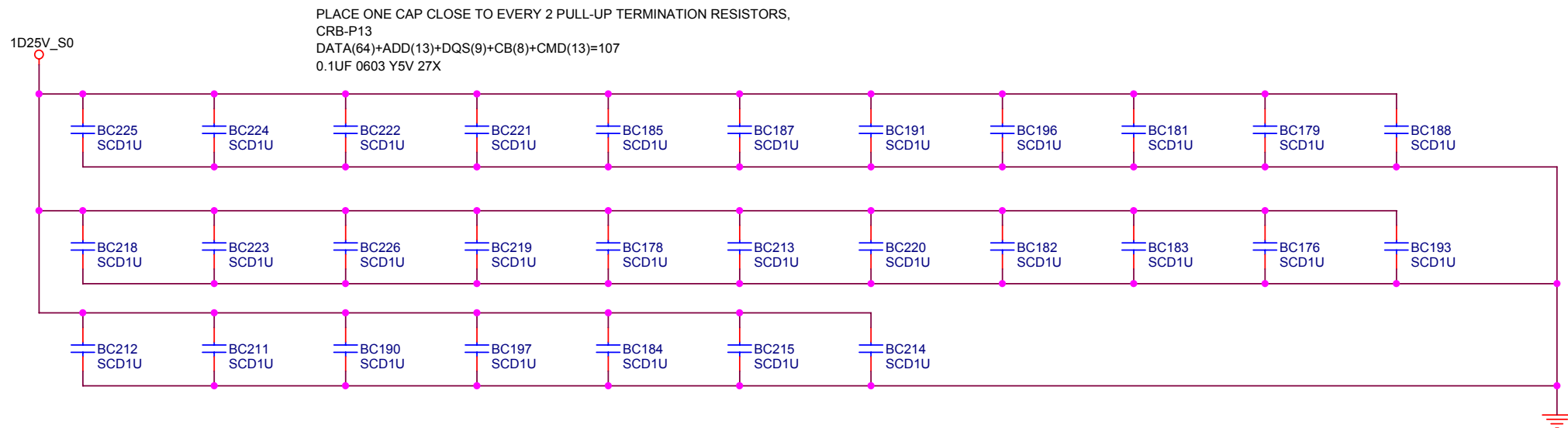


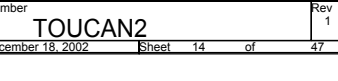
NO EQUAL LENGTH LIMITATION



PLACE BETWEEN DM1, DM2
CLOSE TO FIRST DM (DM 2) < 0.2", TO SECOND DM (DM1) < 1.1"
EQUAL LENGTH LIMITATION WITH SCK/SCK#

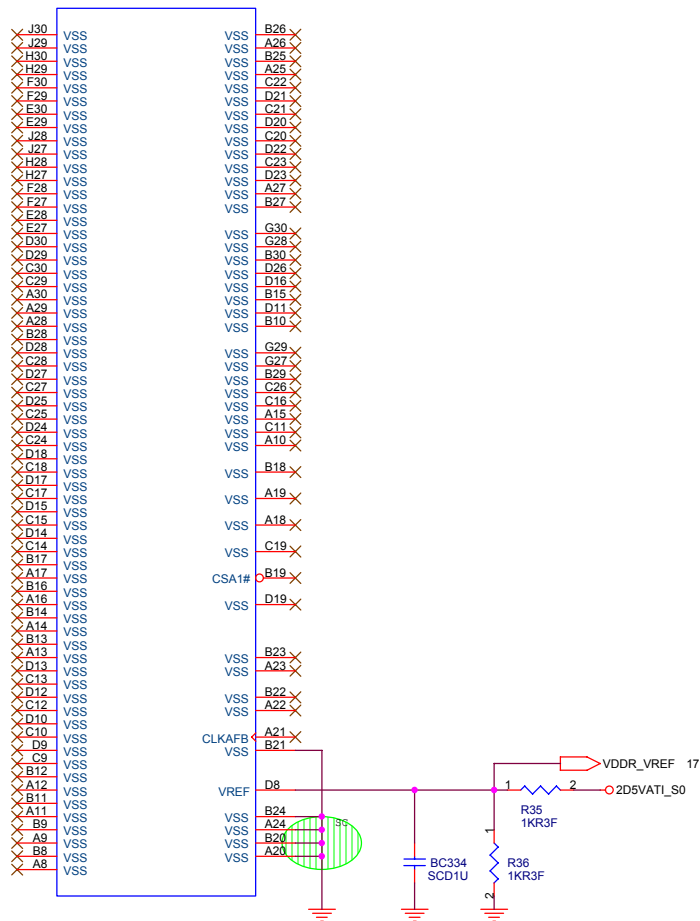






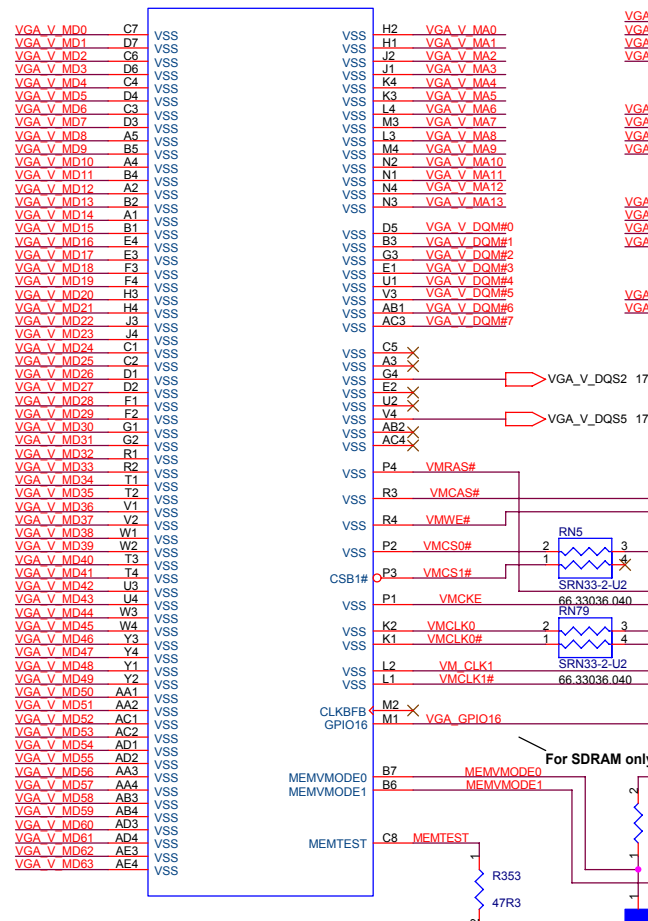
17 VGA_V_MD[0..63]
17 VGA_M_MA[0..13]
17 VGA_V_DQM#[0..7]

U11B



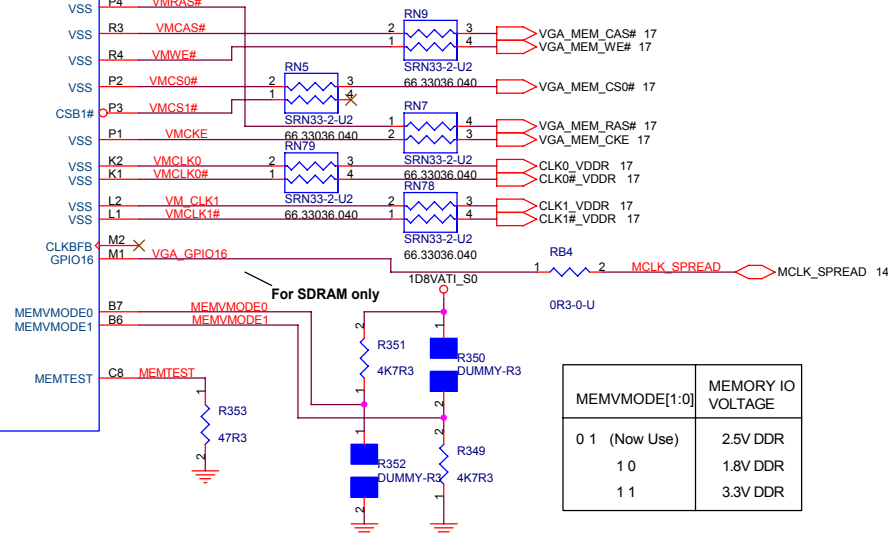
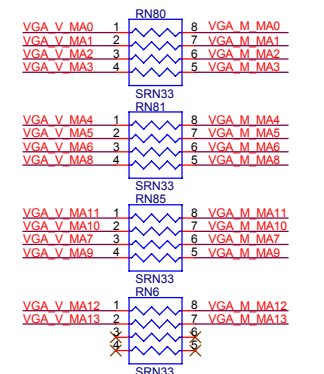
216T9NAAGA11FH-U

U11C



216T9NAAGA11FH-U

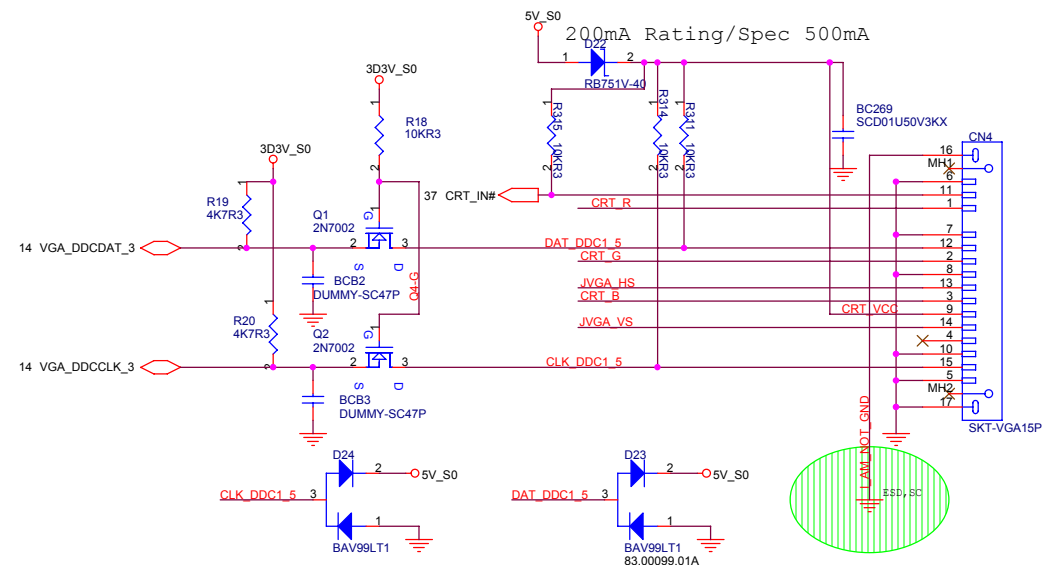
All these dampings must near M9-P.



MEMVMODE[1:0]	MEMORY IO VOLTAGE
0 1 (Now Use)	2.5V DDR
1 0	1.8V DDR
1 1	3.3V DDR

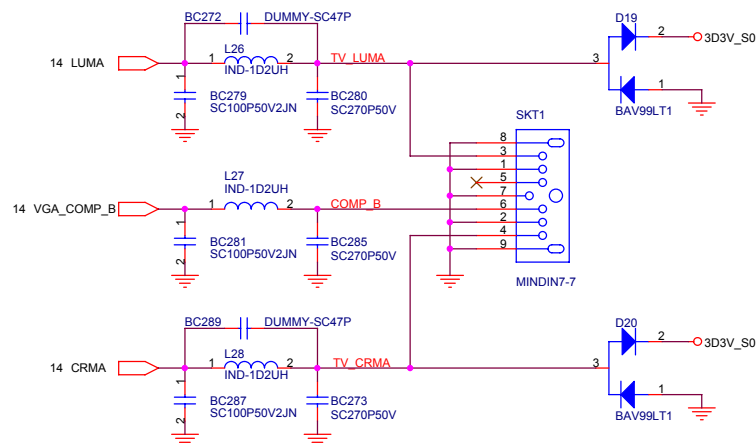


CRT CONN



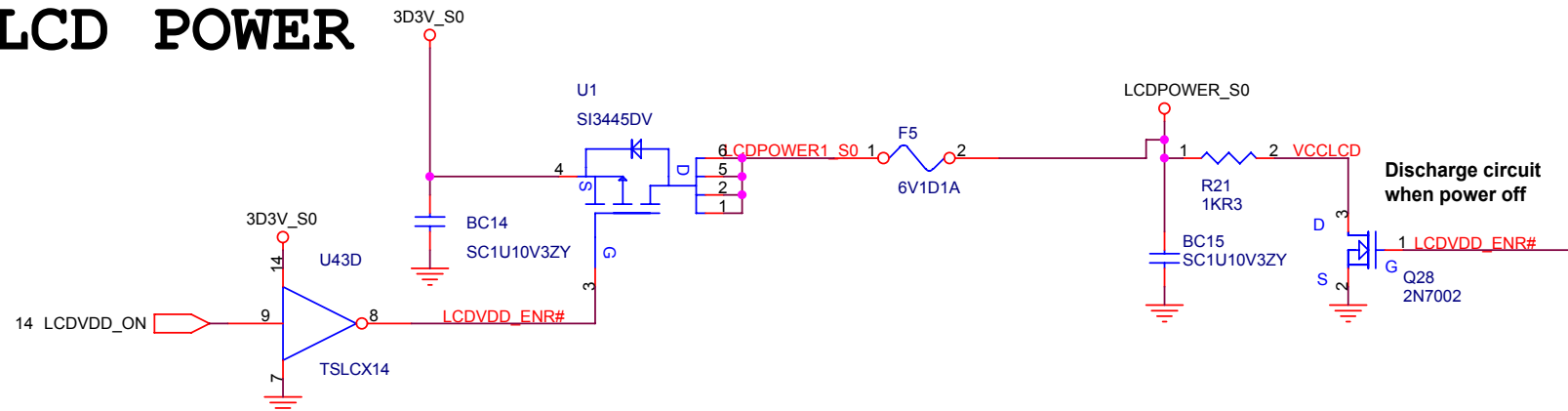
Layout Note:
Must be a ground return path between this
ground and the ground on the VGA connector.
37.4 Ω resistors must be placed after RGB
pi filter, near CRT connector.

TV CONN

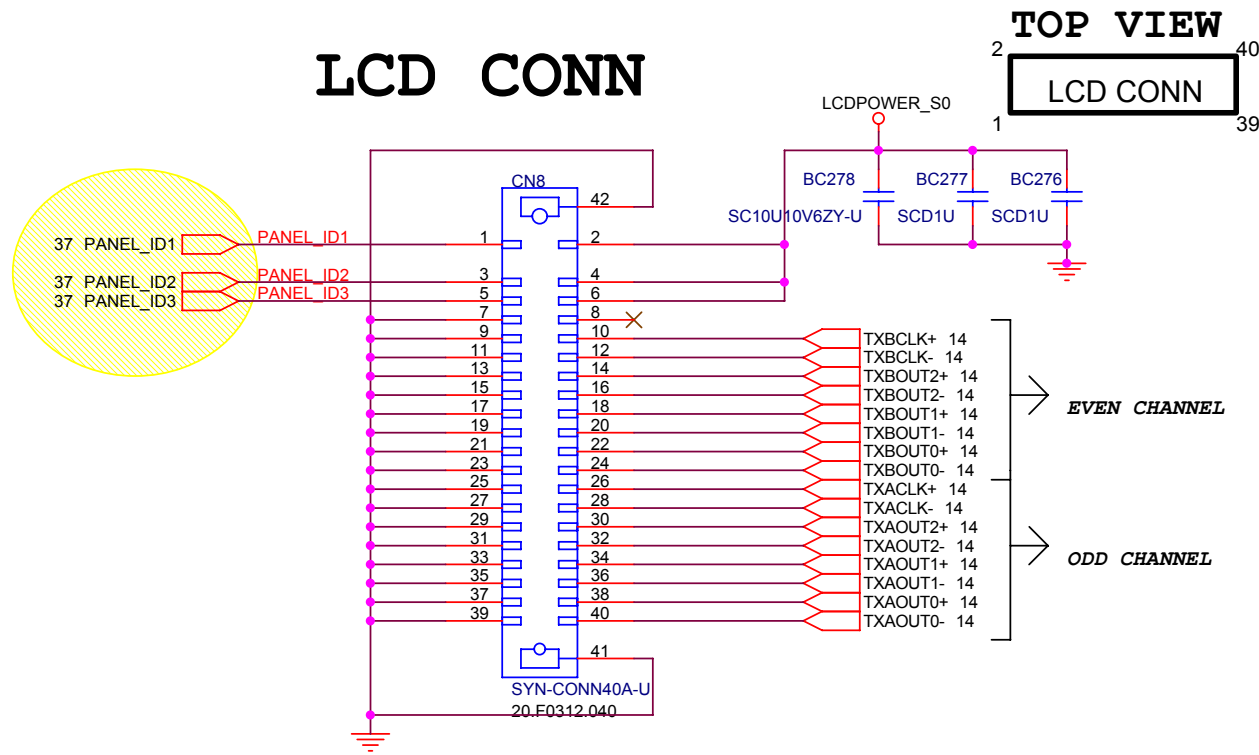


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CRT / TV			
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LCD POWER



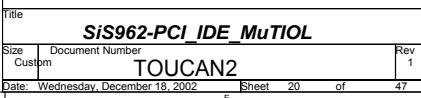
LCD CONN

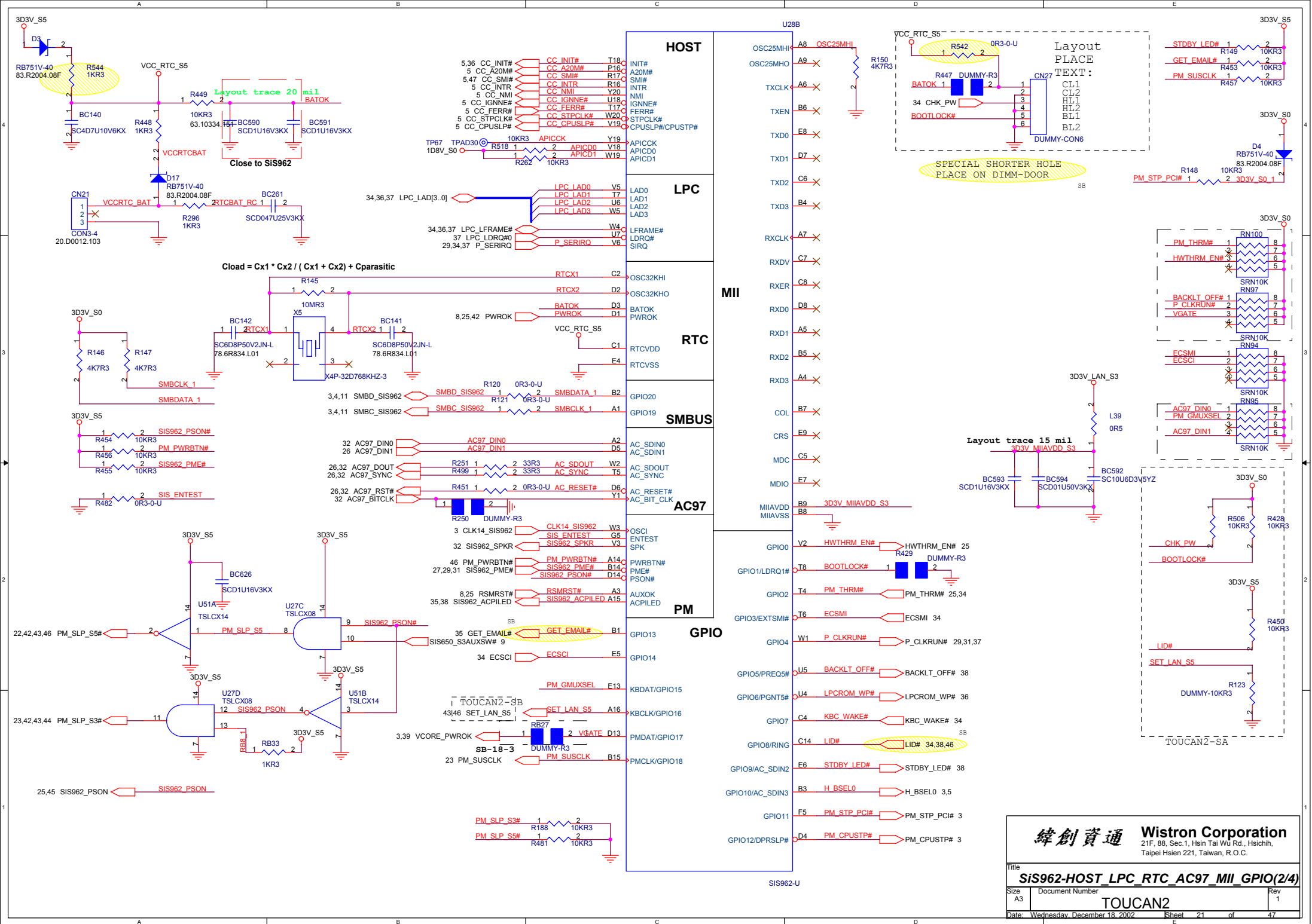


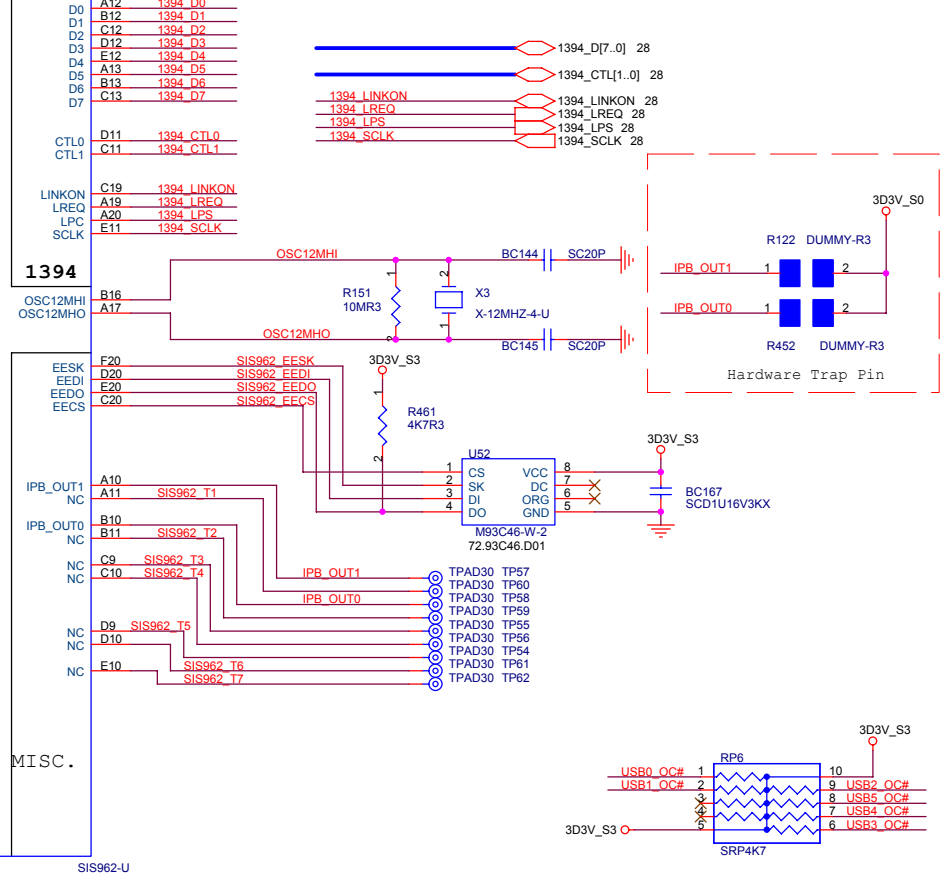
TOP VIEW

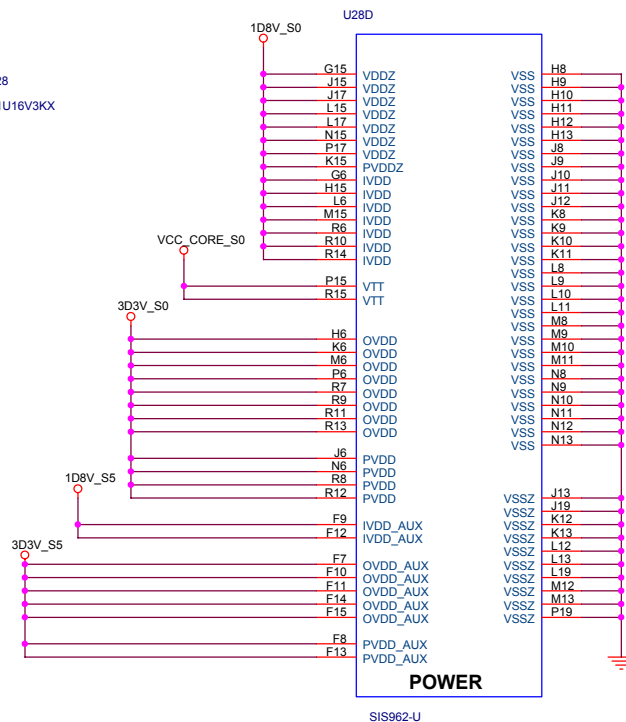
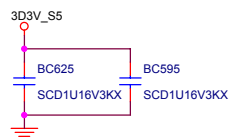
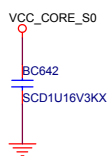
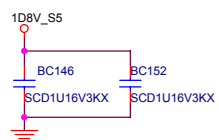
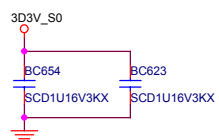
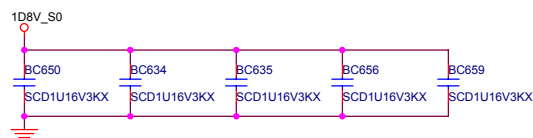
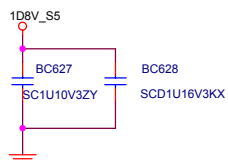
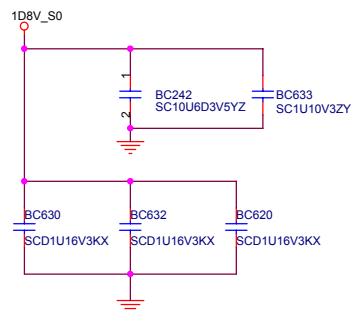
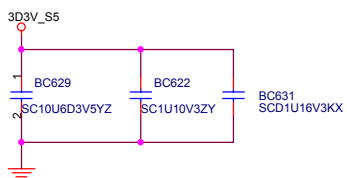
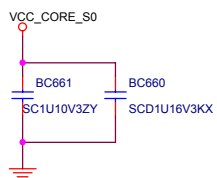
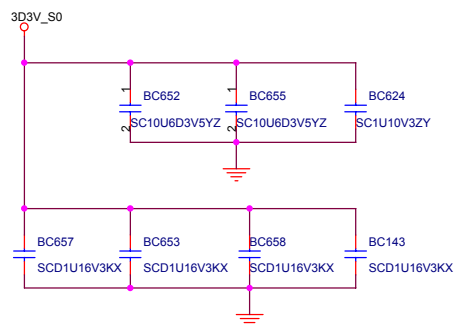


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Title LCD		
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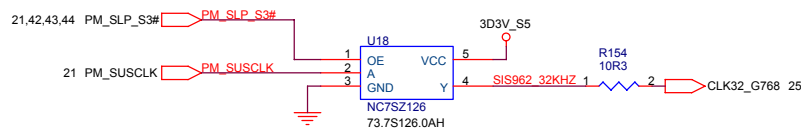




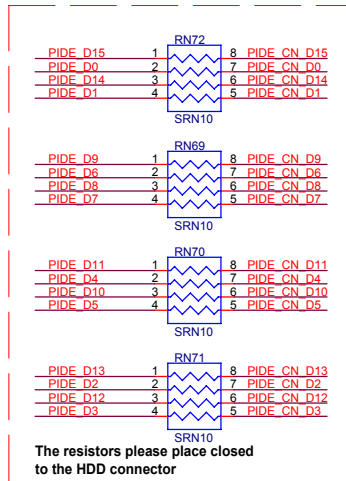




VCC_Core_S0: 30mA (1.5V)
 1D8V_S0: 420mA
 3D3V_S0: 140mA
 1D8V_S5: 70mA
 3D3V_S5: 380mA

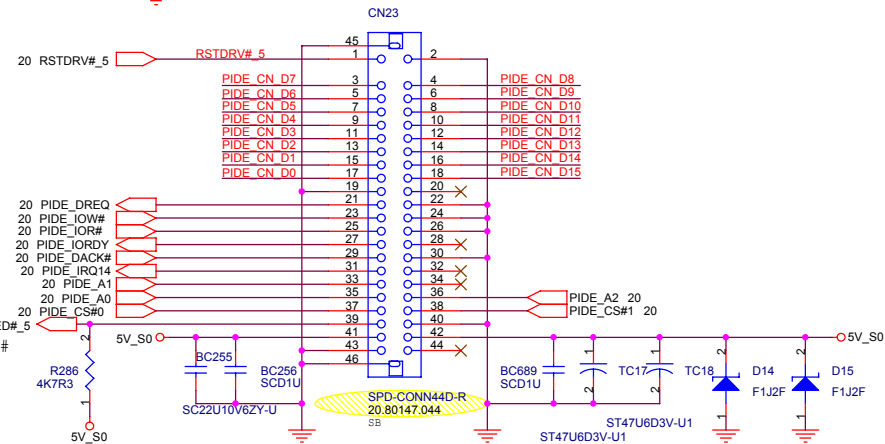
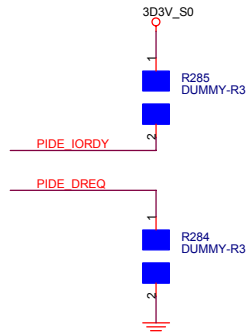


20 PIDE_D[15..0]



TOUCAN2:COULD REMOVE DAMP RESISTER

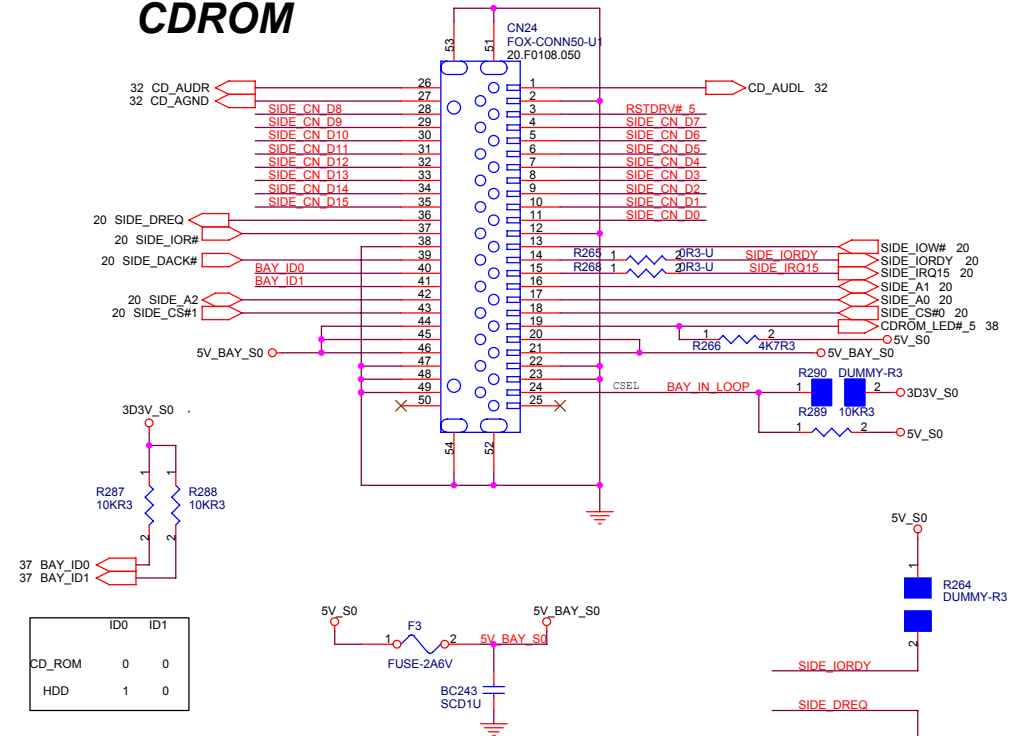
HDD



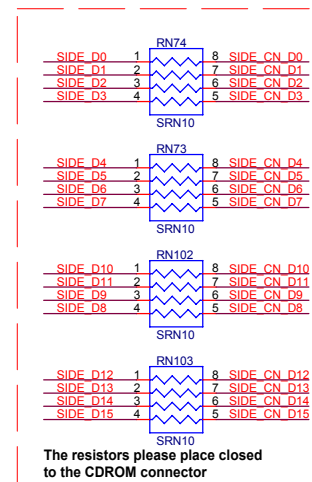
PWR TRACE 100mil

20 SIDE_D[15..0]

CDROM

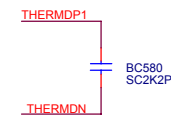
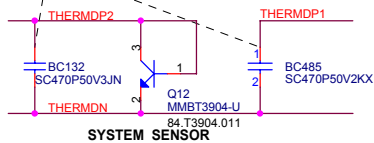
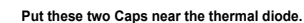


	ID0	ID1
CD_ROM	0	0
HDD	1	0

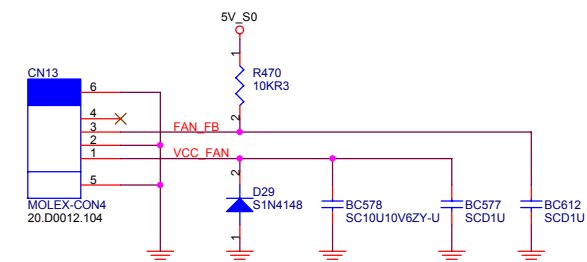
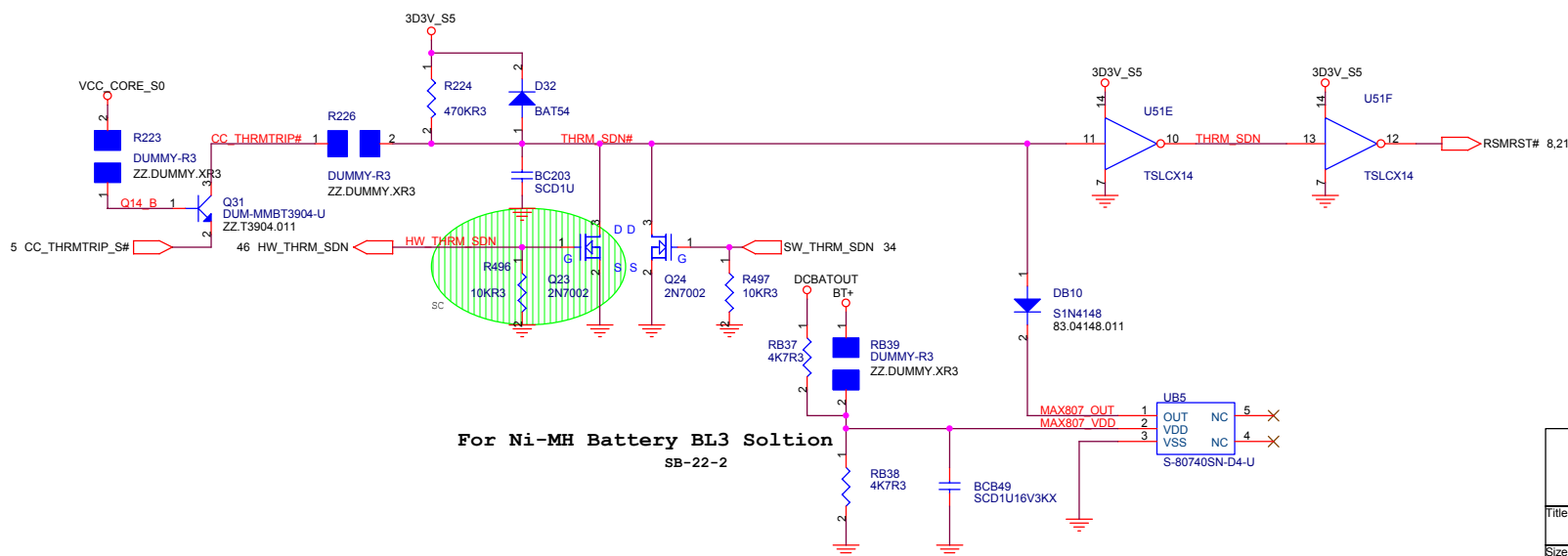
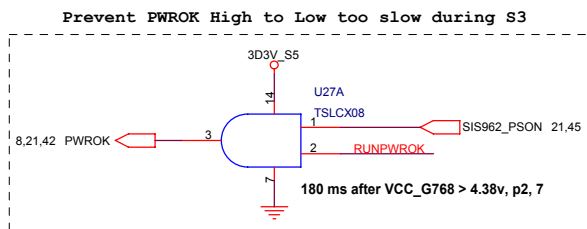
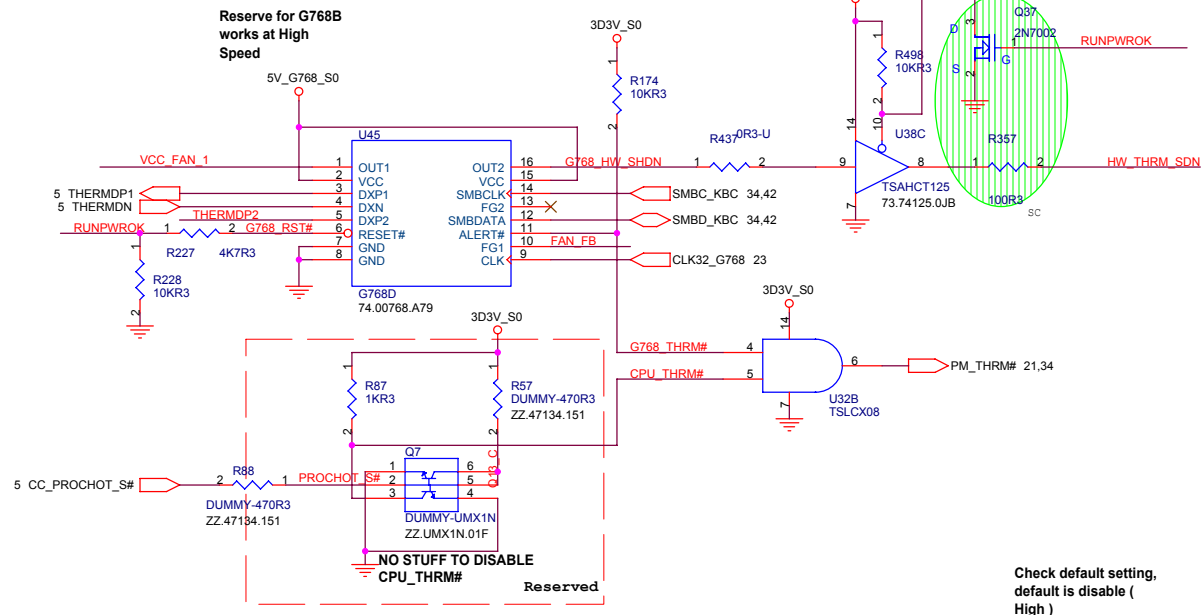
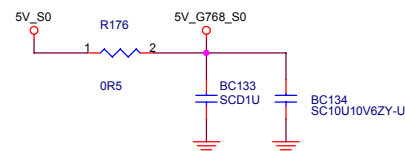


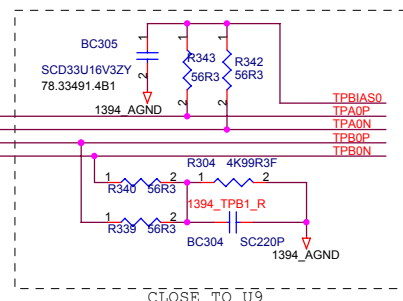
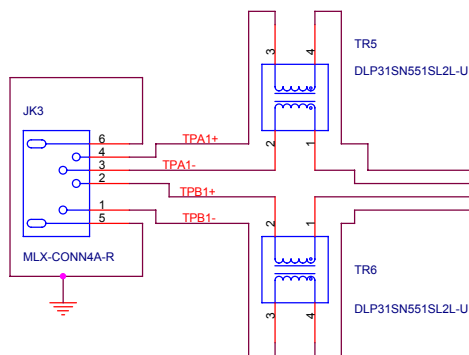
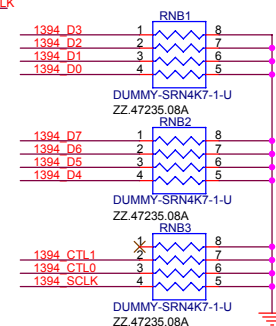
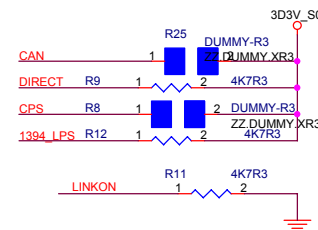
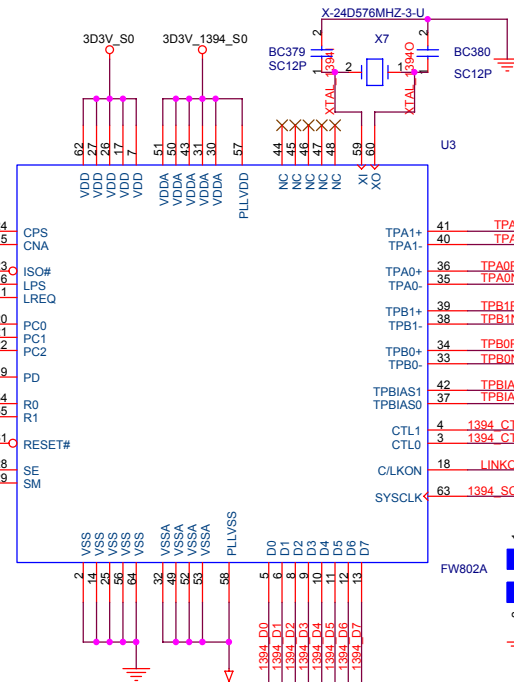
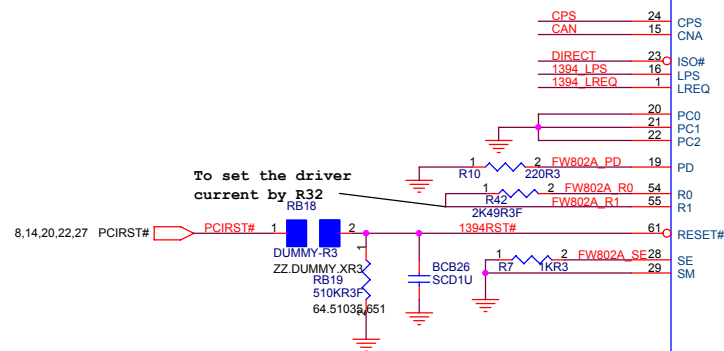
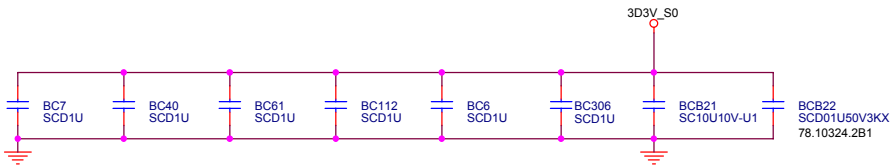
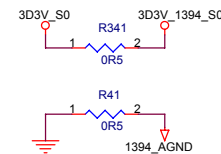
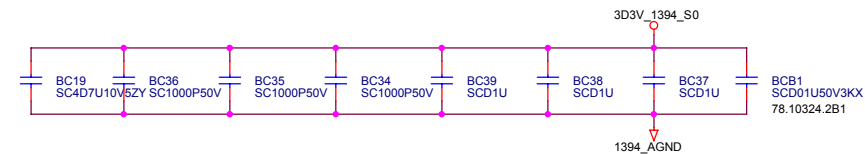
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title HDD / CDROM		
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THERMDP1/DP2/THERMDN ON THE SAME LAYER
W/S = 10/5 MIL, 12 MIL AWAY FROM OTHERS
CAPS CLOSE TO G768B

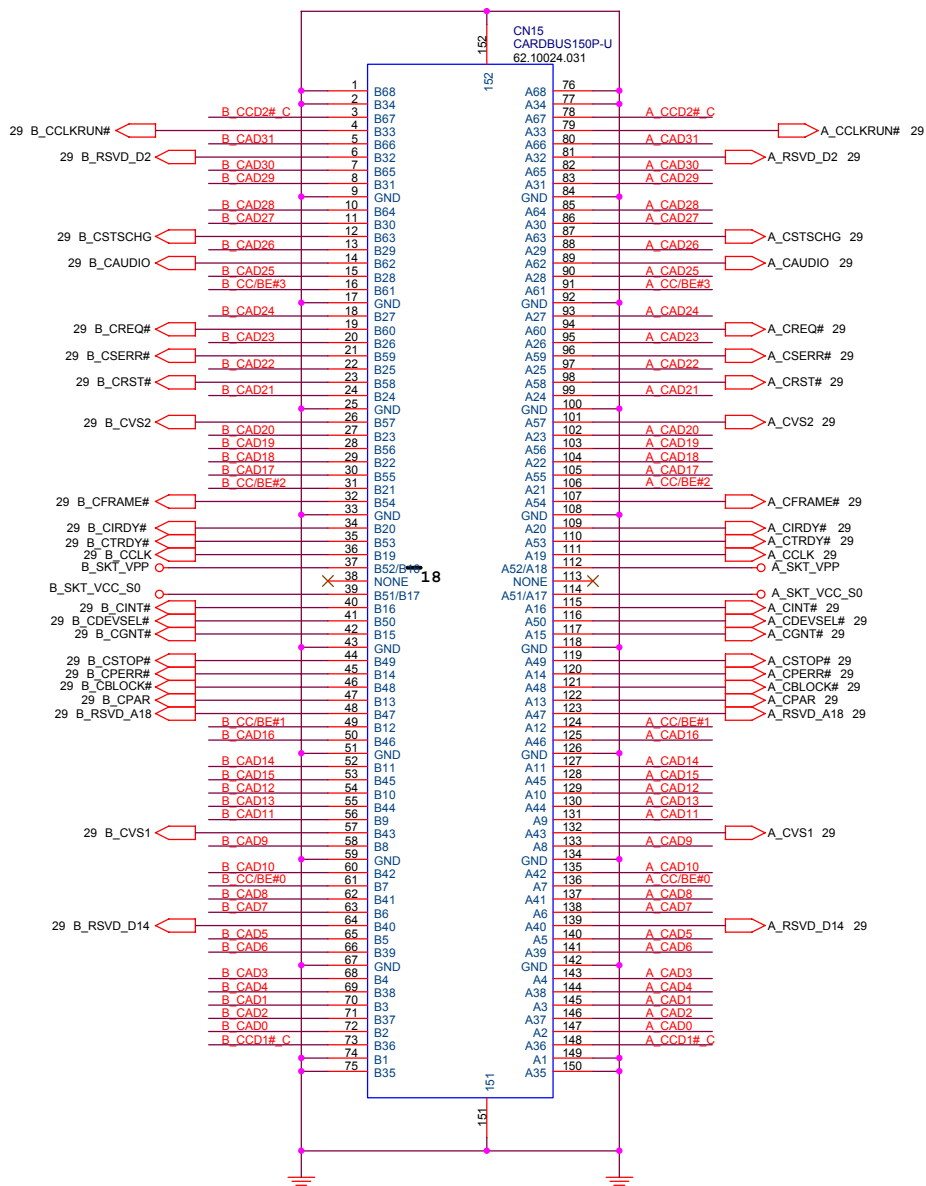




FW802B
71.00802.B0G

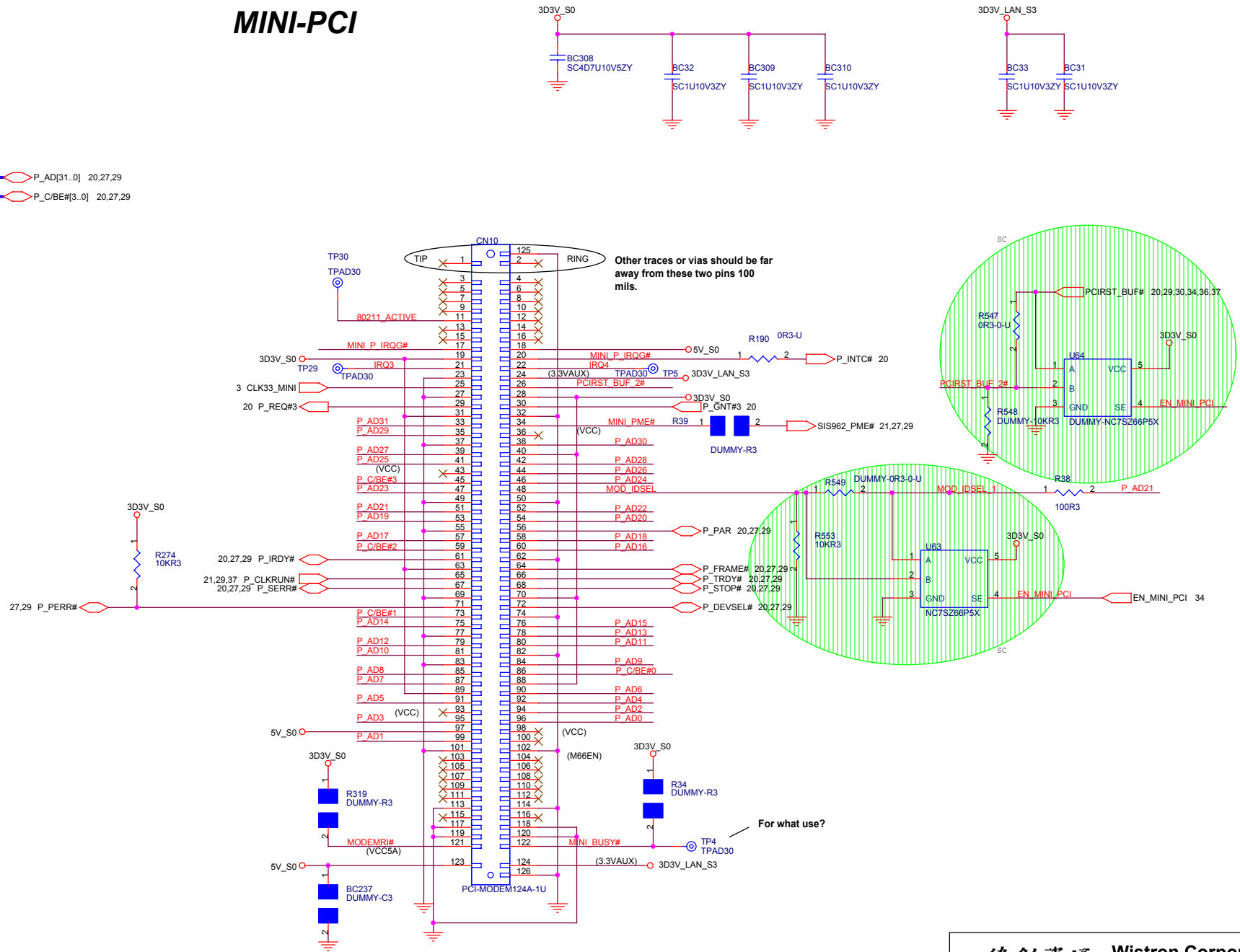
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title IEE1394-PHY_FW802A		
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MINI-PCI

P_AD[31..0] 20,27,29
P_C/BE#[3..0] 20,27,29



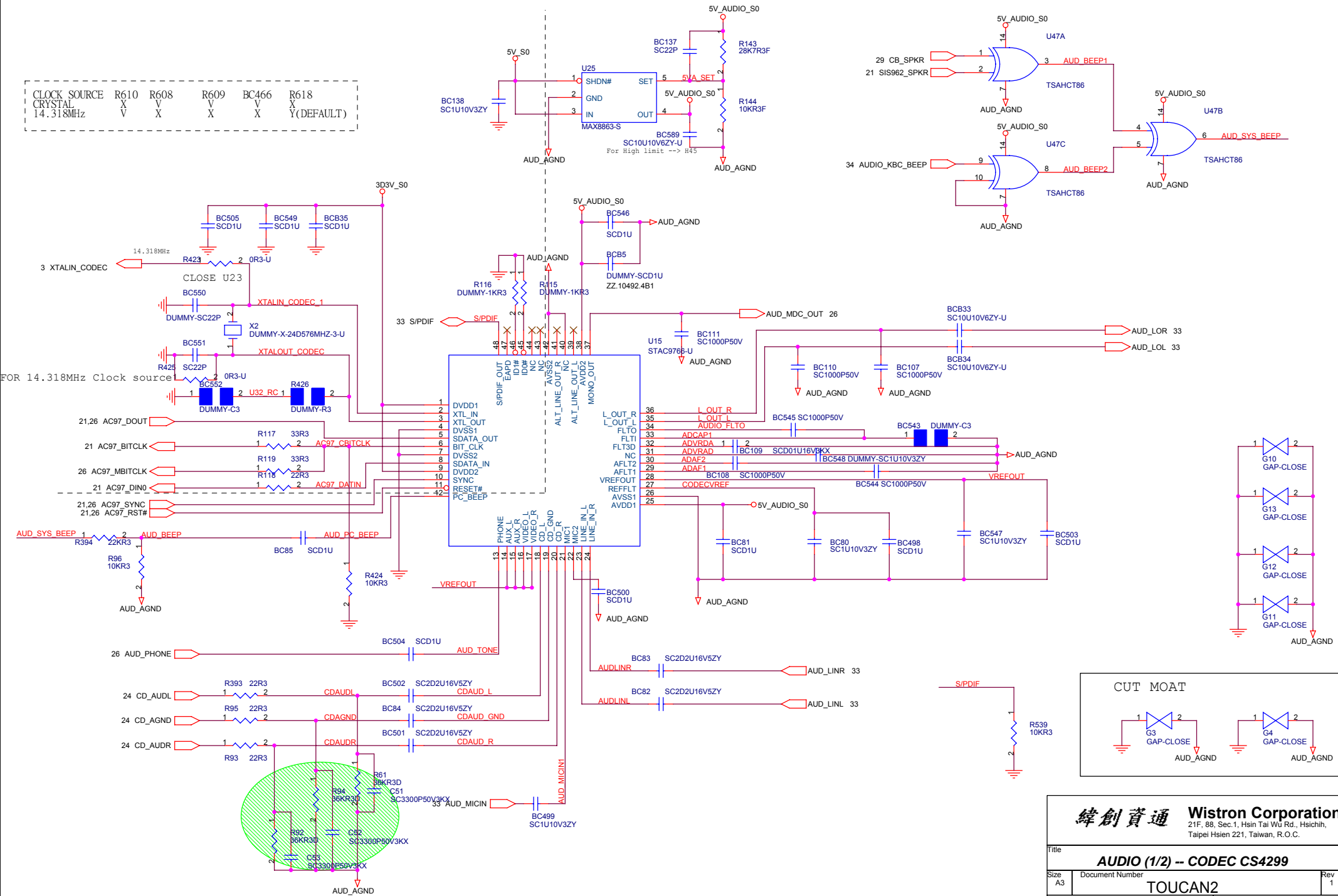
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
MINI-PCI		
Size	Document Number	Rev
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CLOCK SOURCE CRYSTAL 14.318MHz

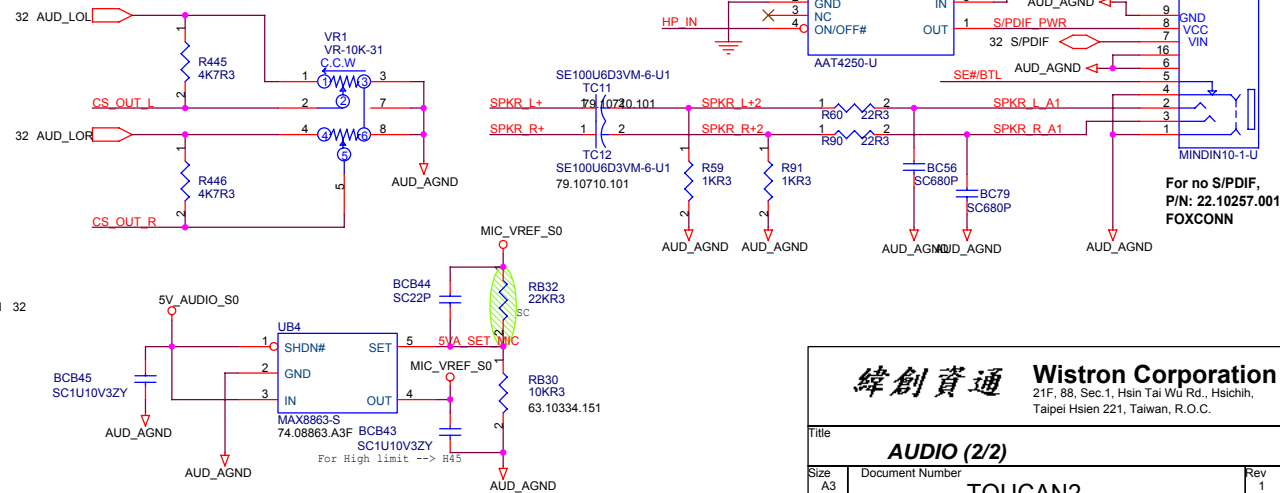
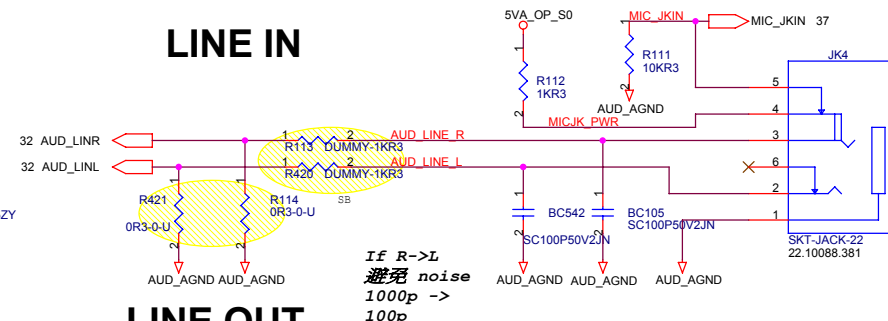
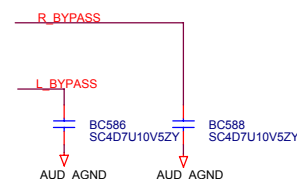
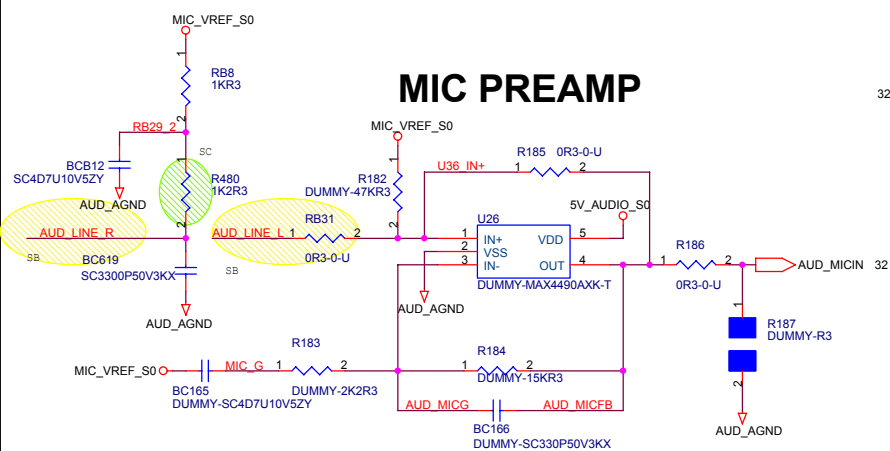
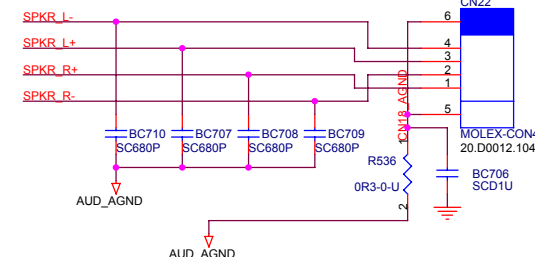
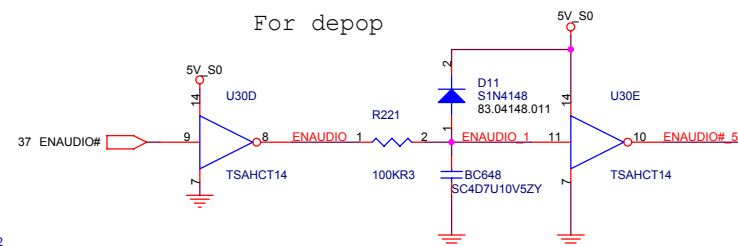
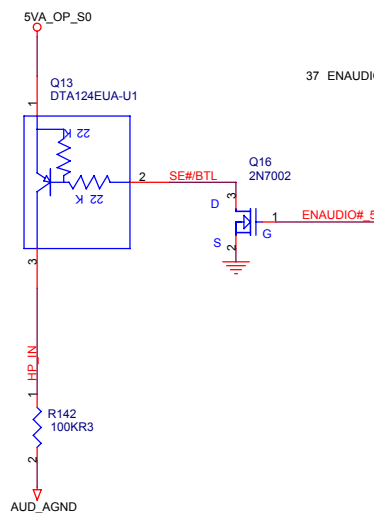
R610 X V R608 X V R609 X V BC466 X V R618 Y (DEFAULT)

FOR 14.318MHz Clock source



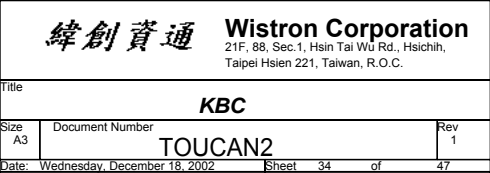
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

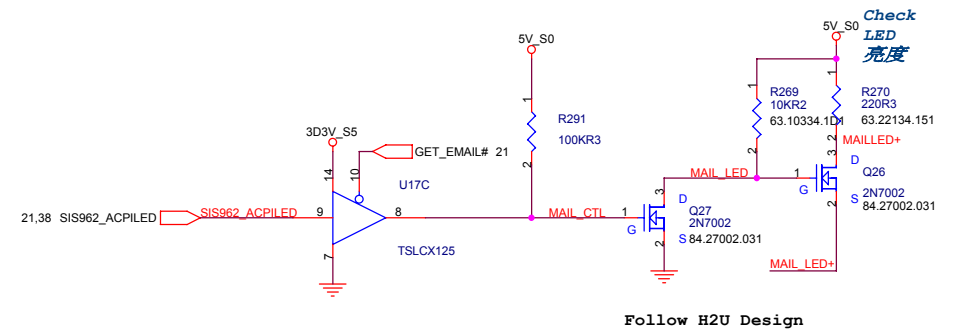
Title		
AUDIO (1/2) -- CODEC CS4299		
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Taipei Hsien 221, Taiwan, R.O.C.

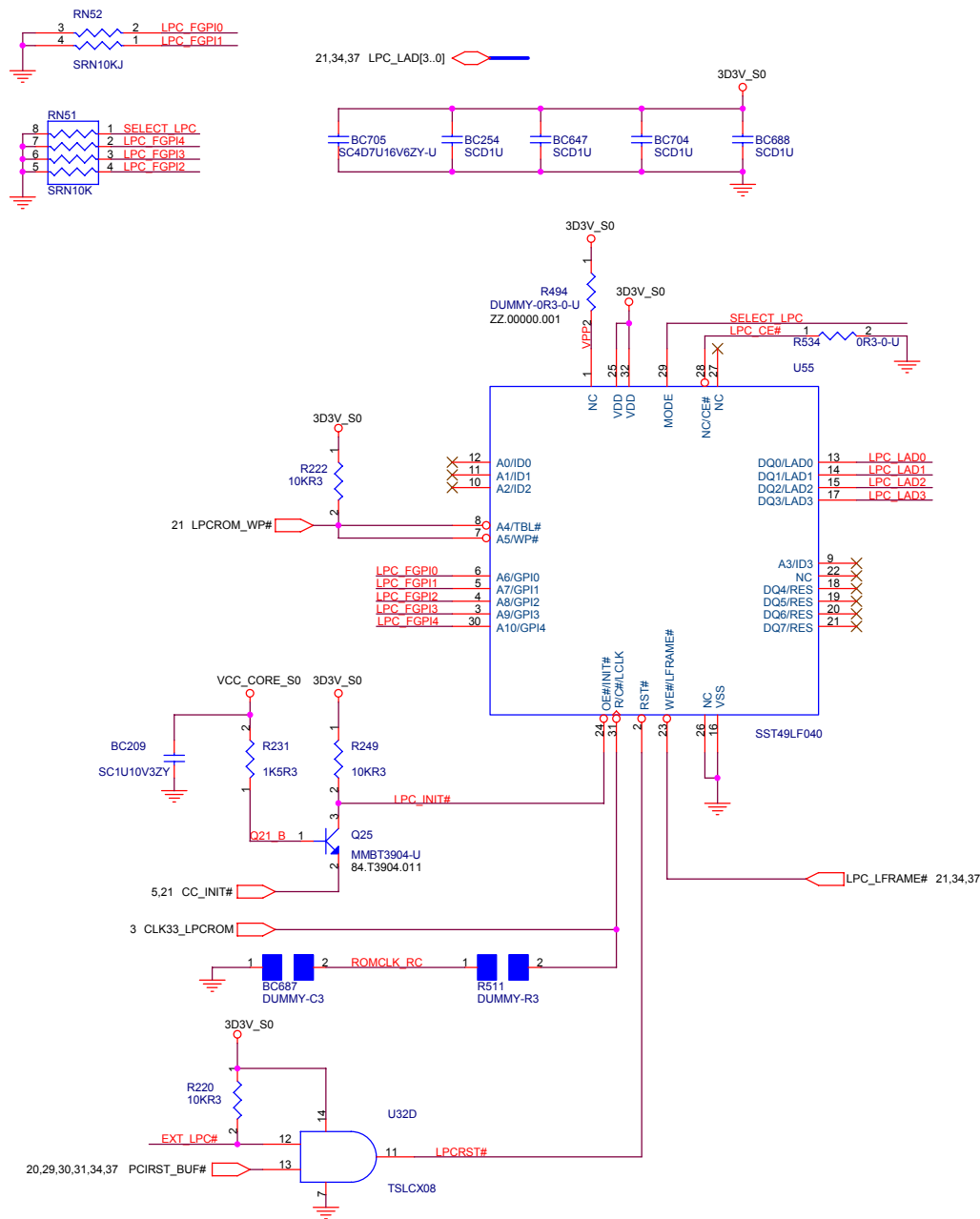
Title			
AUDIO (2/2)			
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TOUCAN2			
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		US	Eur	Jap	Other
Low Bit	MATRIXID1#	1	0	1	0
High Bit	MATRIXID2#	1	1	0	0

Internal has Serial 2LEDs

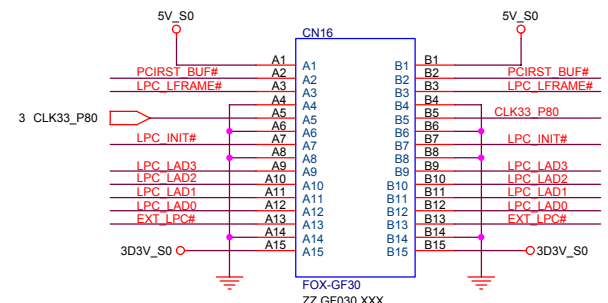


TOP VIEW

A15 (B1)
A14 (B2)
:
:
A2 (B14)
A1 (B15)

(BOTTOM VIEW)

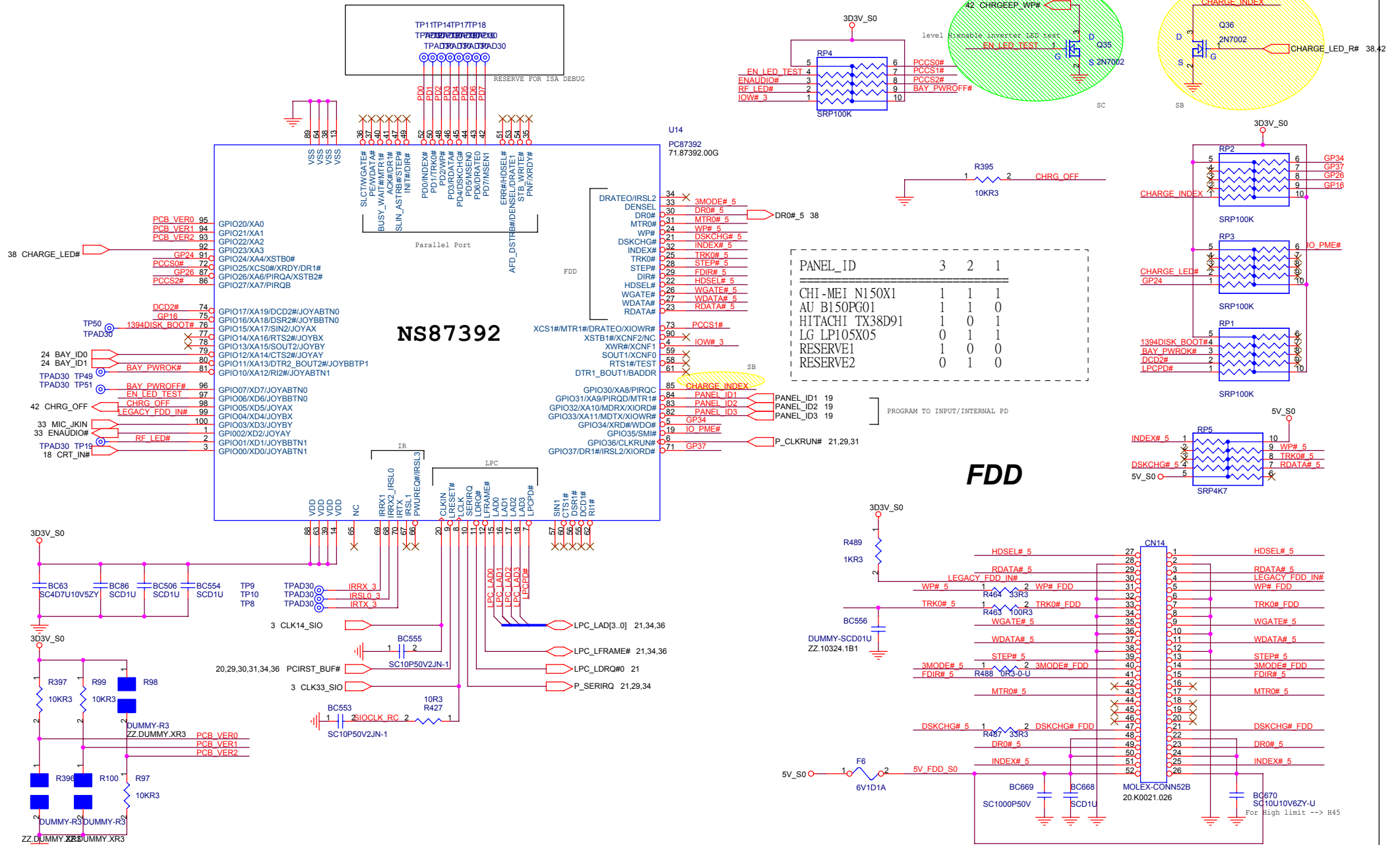
GOLDEN FINGER FOR DEBUG BOARD

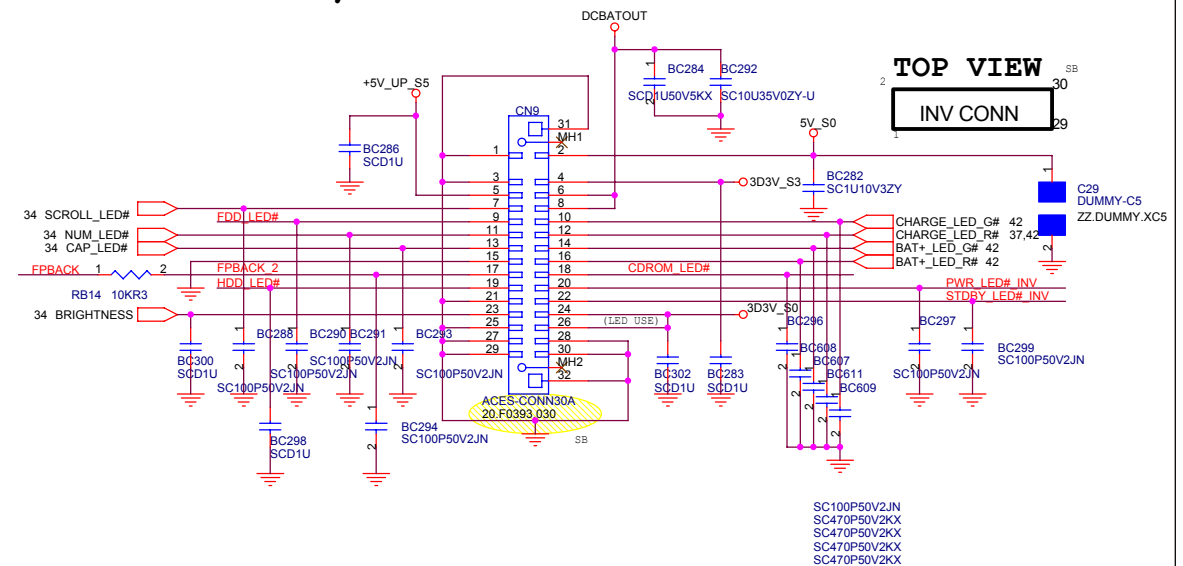
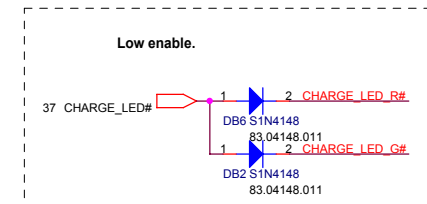


PLCC 32pin ST: 72.50040.003
PLCC 32pin SST:
72.49004.B03

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Title			
LPCROM / DEBUG PORT			
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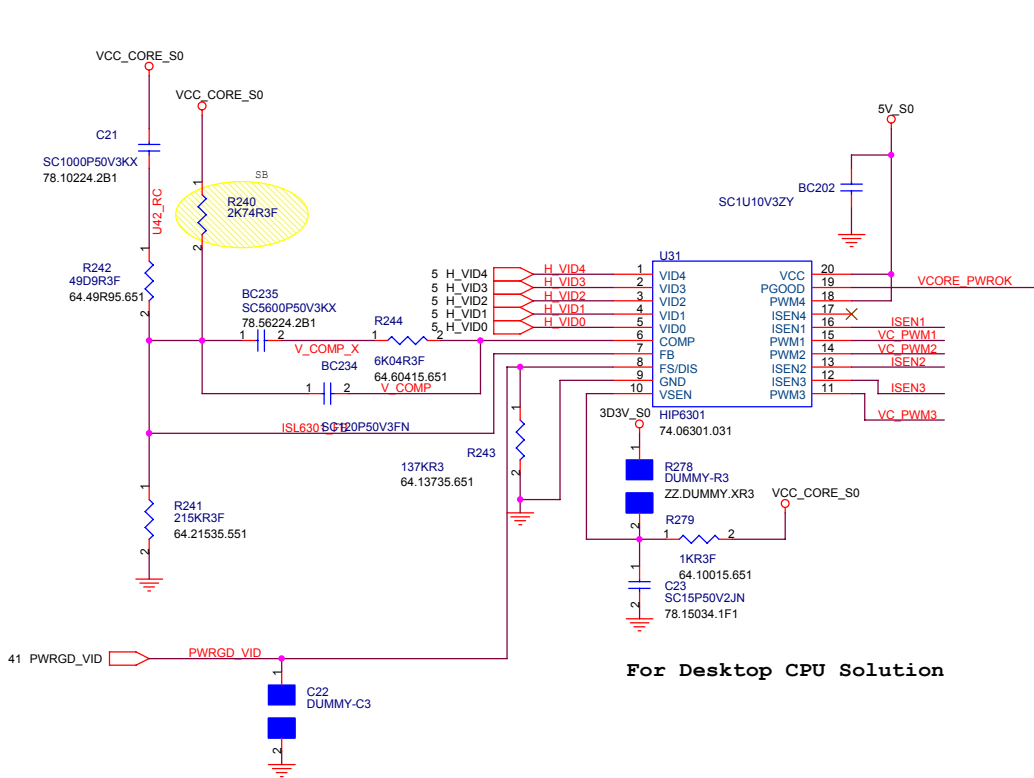




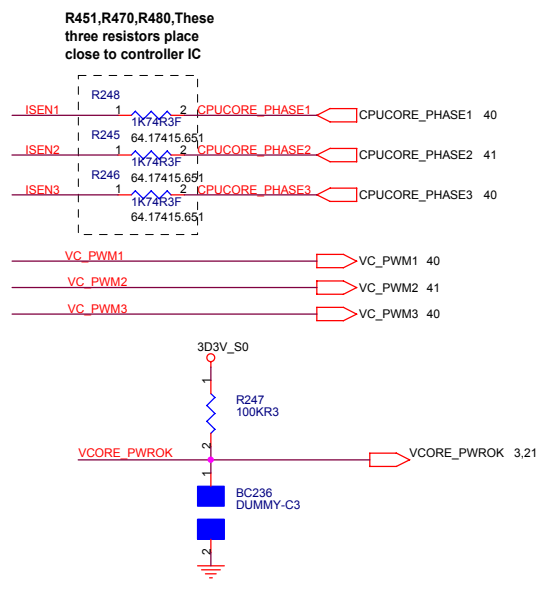
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

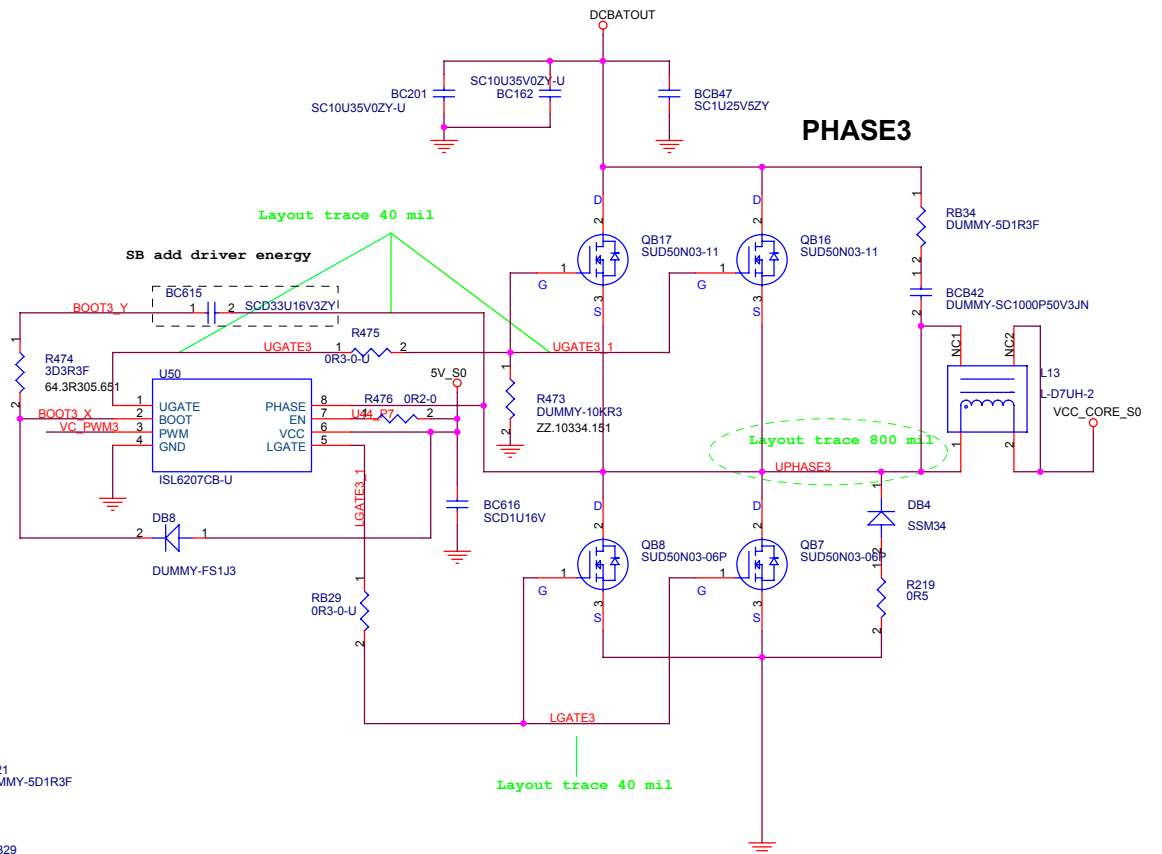
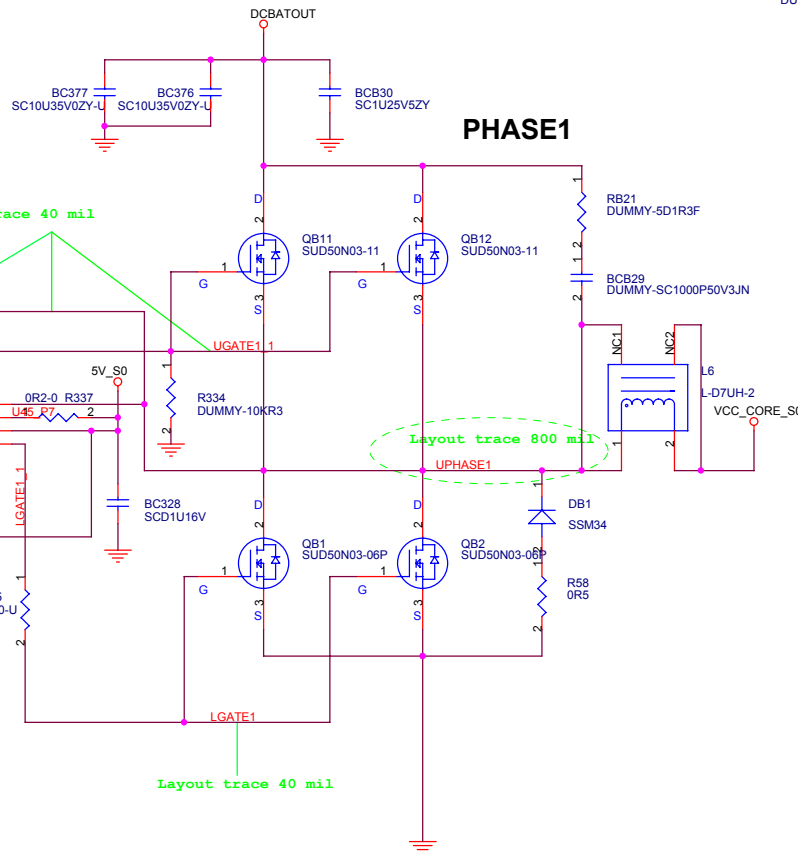
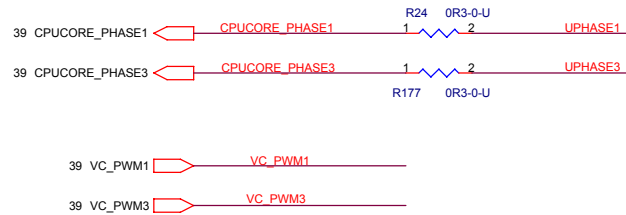
Title			
INVERTER			
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Voltage Identification Codes					
VID4	VID3	VID2	VID1	VID0	VDAC
1	1	1	1	1	OFF
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700
0	0	1	0	1	1.725
0	0	1	0	0	1.750
0	0	0	1	1	1.775
0	0	0	1	0	1.800
0	0	0	0	1	1.825
0	0	0	0	0	1.850



For Desktop CPU Solution





VCC_CORE_S0 : 1.5V or 1.525V

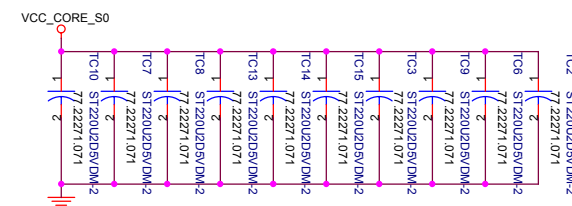
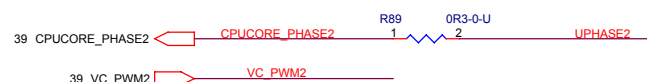
緯創資通

Wistron Corporation

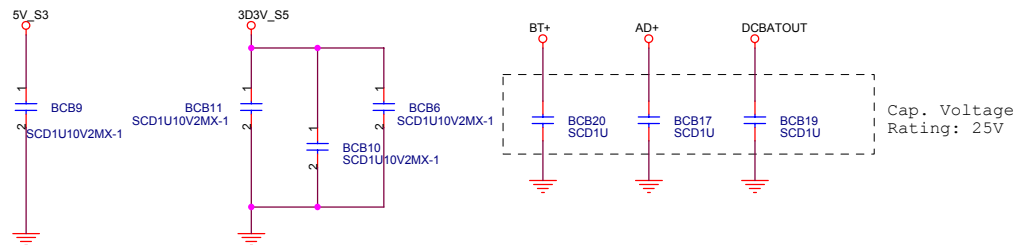
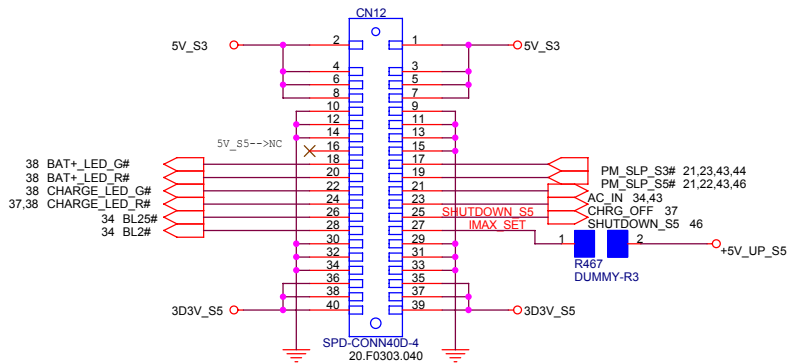
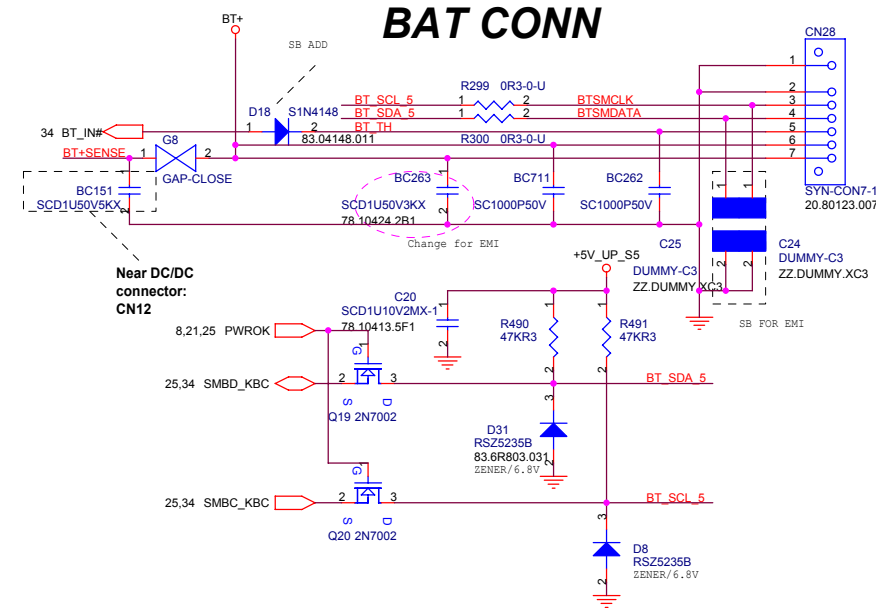
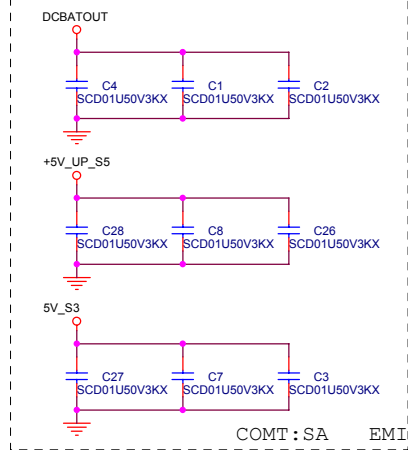
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Title		CPU D/D +VCC_CORE(2/3)	
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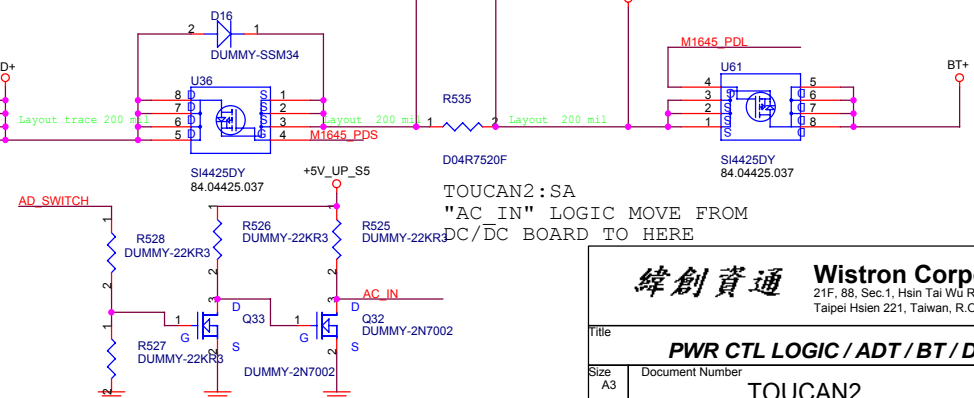
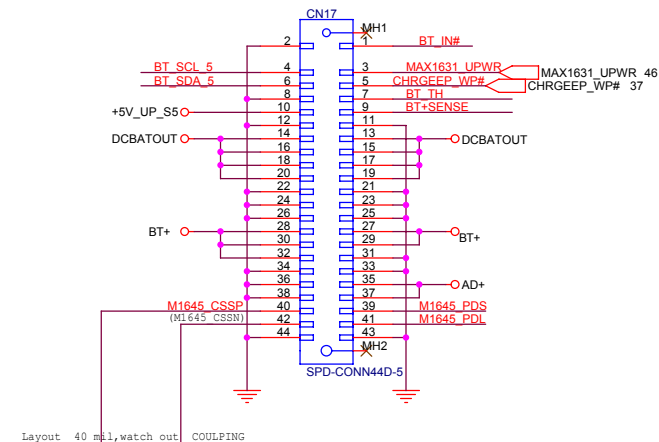
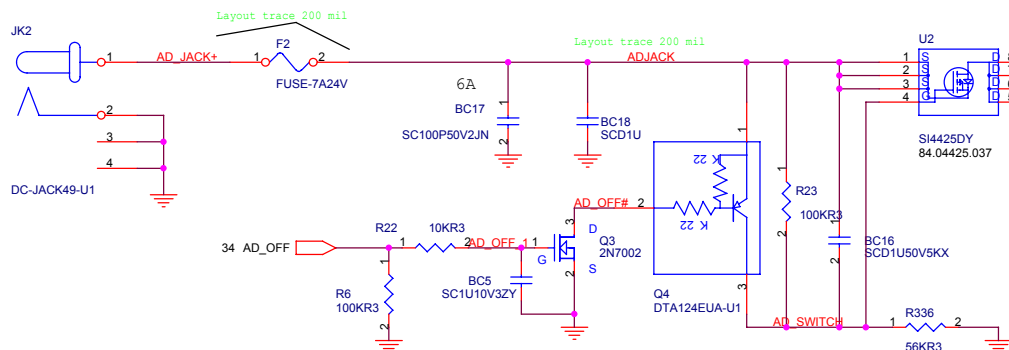
TOUCAN2



BAT CONN

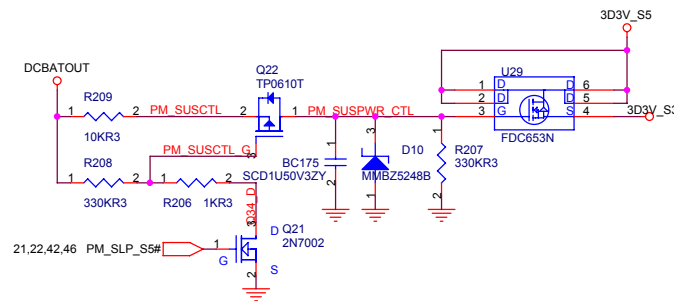
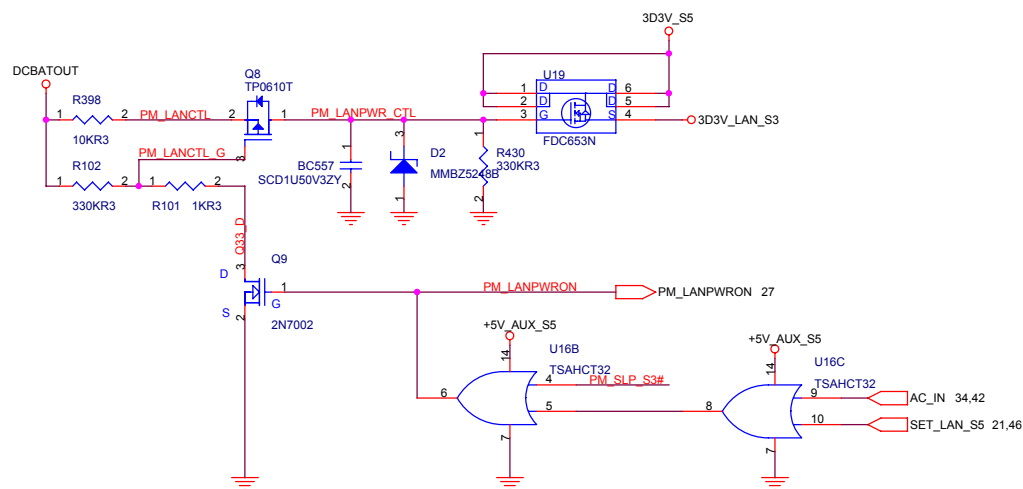
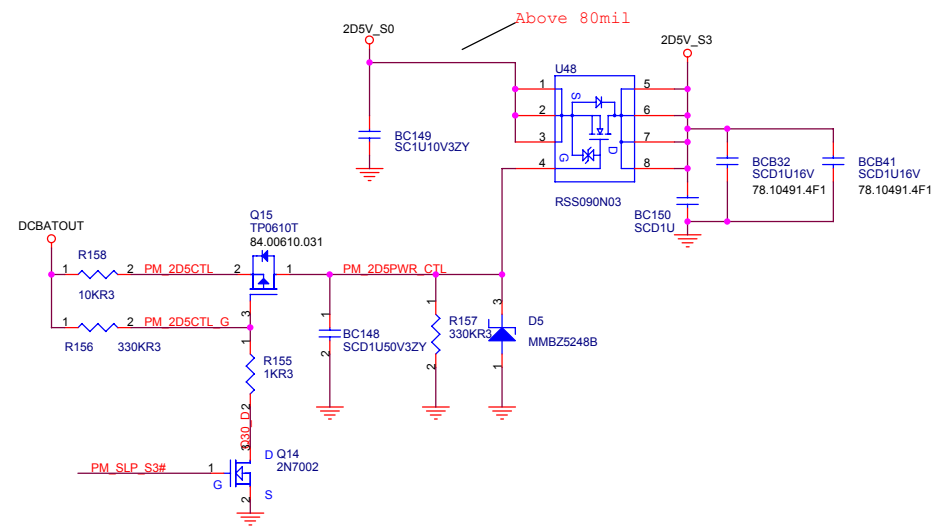
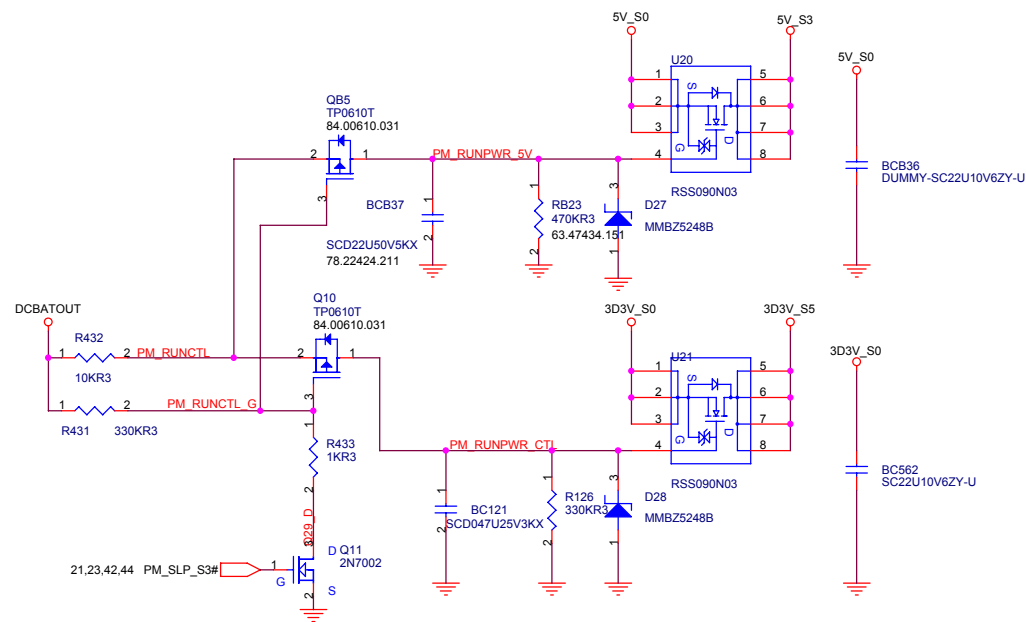


Origin: Fuse between Jack & inductor
F4:R451007, P/N: 69.47001.011



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Taipei Hsien 221, Taiwan, R.O.C.

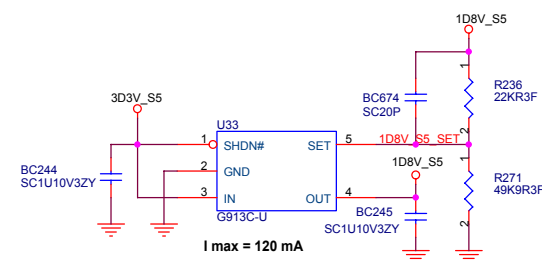
Title		
PWR CTL LOGIC / ADT / BT / DC CONN		
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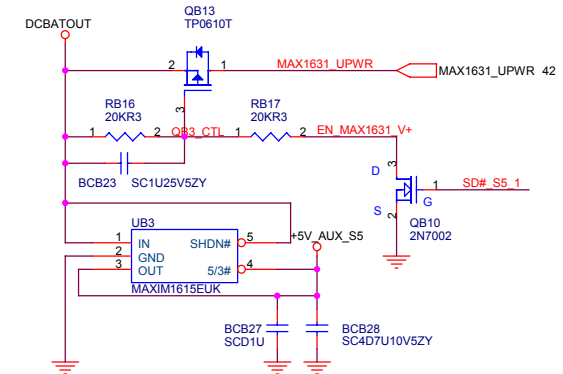
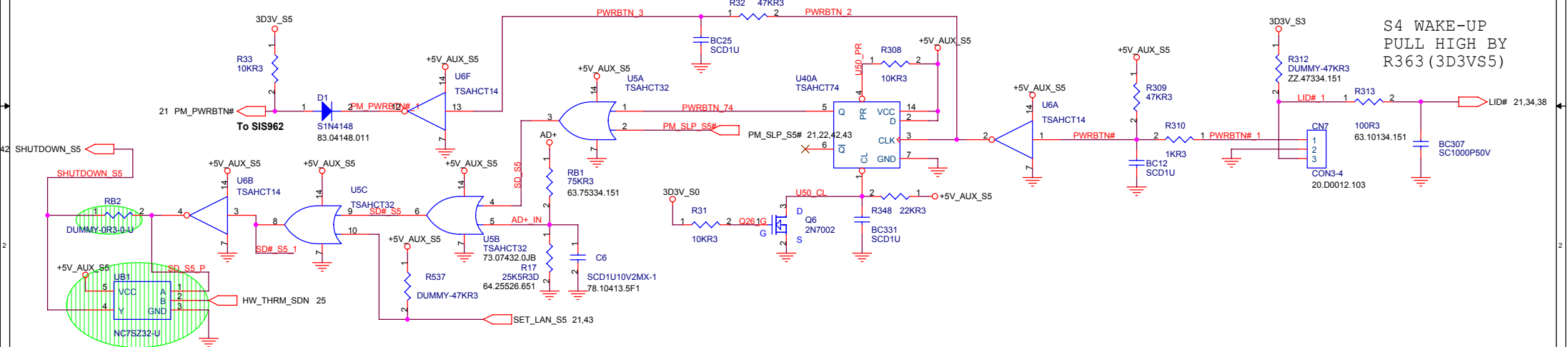
2.5VS0 --FOR
DDRCLK_BUFFER

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
DC/DC (1/3) -- 5V / 3.3V / 2.5V			
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[illegible]

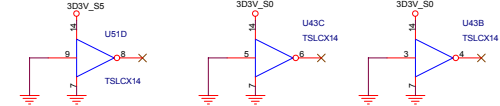
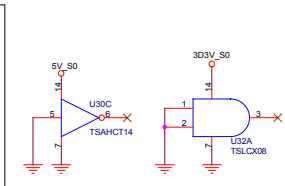
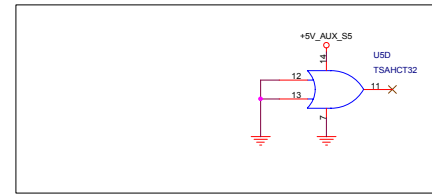
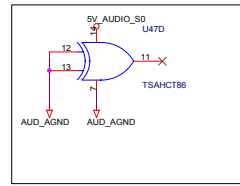
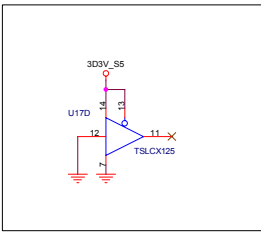
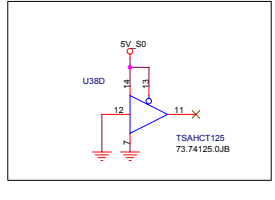
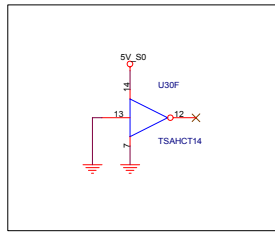
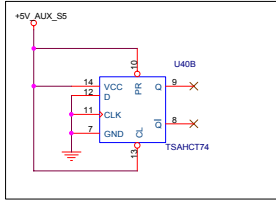
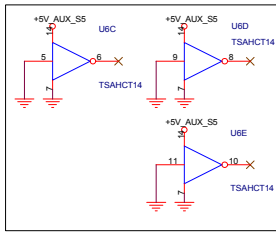
POWER BUTTON



S4 WAKE-UP
PULL HIGH BY
R363 (3D3VS5)

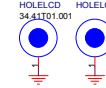
NEAR CPU

5.21 CC_SMI# TP43



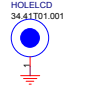
MDC Stand Off

P/N: 34.41Q08.001



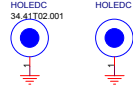
LCD Stand Off

P/N: 34.41T01.001

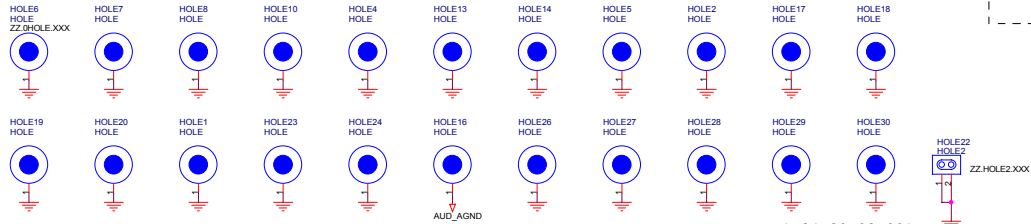


DC/DC Stand Off

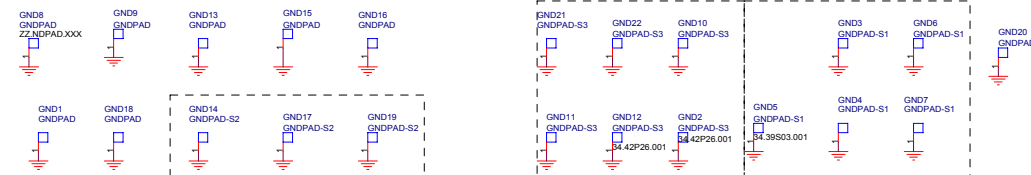
P/N: 34.41T02.001



SPARE GATES

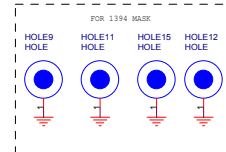
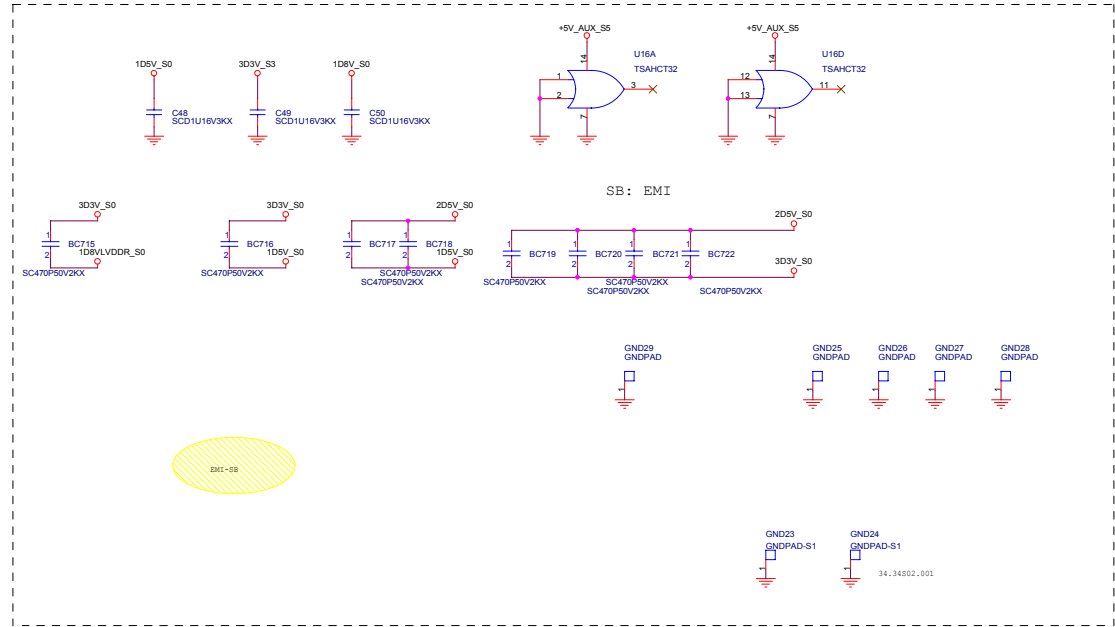


S1:34.39S03.001



S2:34.41T19.001

S3:34.42P26.001



Spring for ME

34.39S03.001	GND6 / GND7 / GND8 / GND15
34.41T19.001	GND11 / GND12 / GND17
34.42P26.001	GND1 / GND2 / GND5
	GND14 / GND18 / GND 20

緯創資通 Wistron Corporation
217-BB, Sec.1, Hsin Ta Wu Rd., Taichung, Taiwan, R.O.C.

File	MISC	Rev	1
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