

Compal Confidential

EG50_BZ

Q5WT6 Schematics Document

AMD Brazos

Brazos with Ontario / Hudson M3L

UMA only

2011-12-16

LA-8531P REV: 0.3



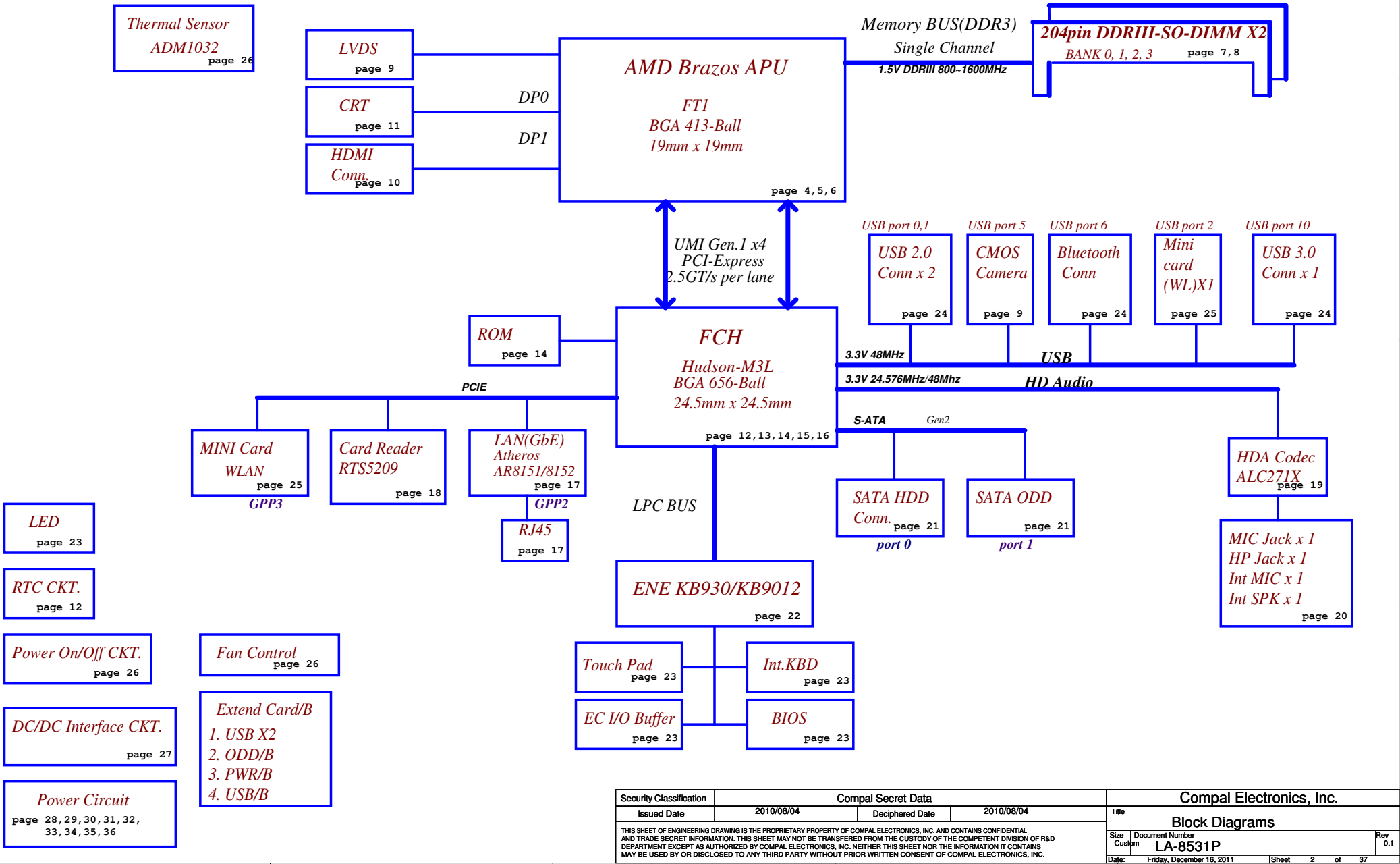
Part Number = DA60000RP00

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				Size	Document Number	Rev
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Compal Confidential

Model Name : Q5WT6

Brazos



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Size		Document Number		Rev	
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VSB	VSB always on power rail	ON	ON	ON*
+3VALW	3.3V always on power rail	ON	ON	ON*
+5VALW	5V always on power rail	ON	ON	ON*
+1.1VALW	1.1V always on power rail	ON	ON	ON*
+APU_CORE	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+APU_CORE_NB	1.0V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDRIII	ON	ON	OFF
+0.75VS	0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for APU VDD10	ON	OFF	OFF
+1.1VS	1.1VS switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+3VSG	3.3V switched power rail for GPU	ON	OFF	OFF
+1.8VSG	1.8V switched power rail for GPU	ON	OFF	OFF
+1.5VSG	1.5V switched power rail for GPU	ON	OFF	OFF
+1.0VSG	1.0V switched power rail for GPU	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address			EC SM Bus2 address		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001-011xb	NA	EMC1403-2(GPU)	1001-101xb	9EH

SM Bus Controller 0 (FCH_SMB1 ~ FCH_SMB4, SMB_ALERT#)

Device	Address	HEX
APU SIC/SID (FCH_SMB3)		
H_THERMTRIP# (FCH_ALERT#)		

SM Bus Controller 1 (FCH_SMB0)

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90
DDR DIMM2 (FCH_SMB0)	1001-001xb	92
WLAN (FCH_SMB0)		

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

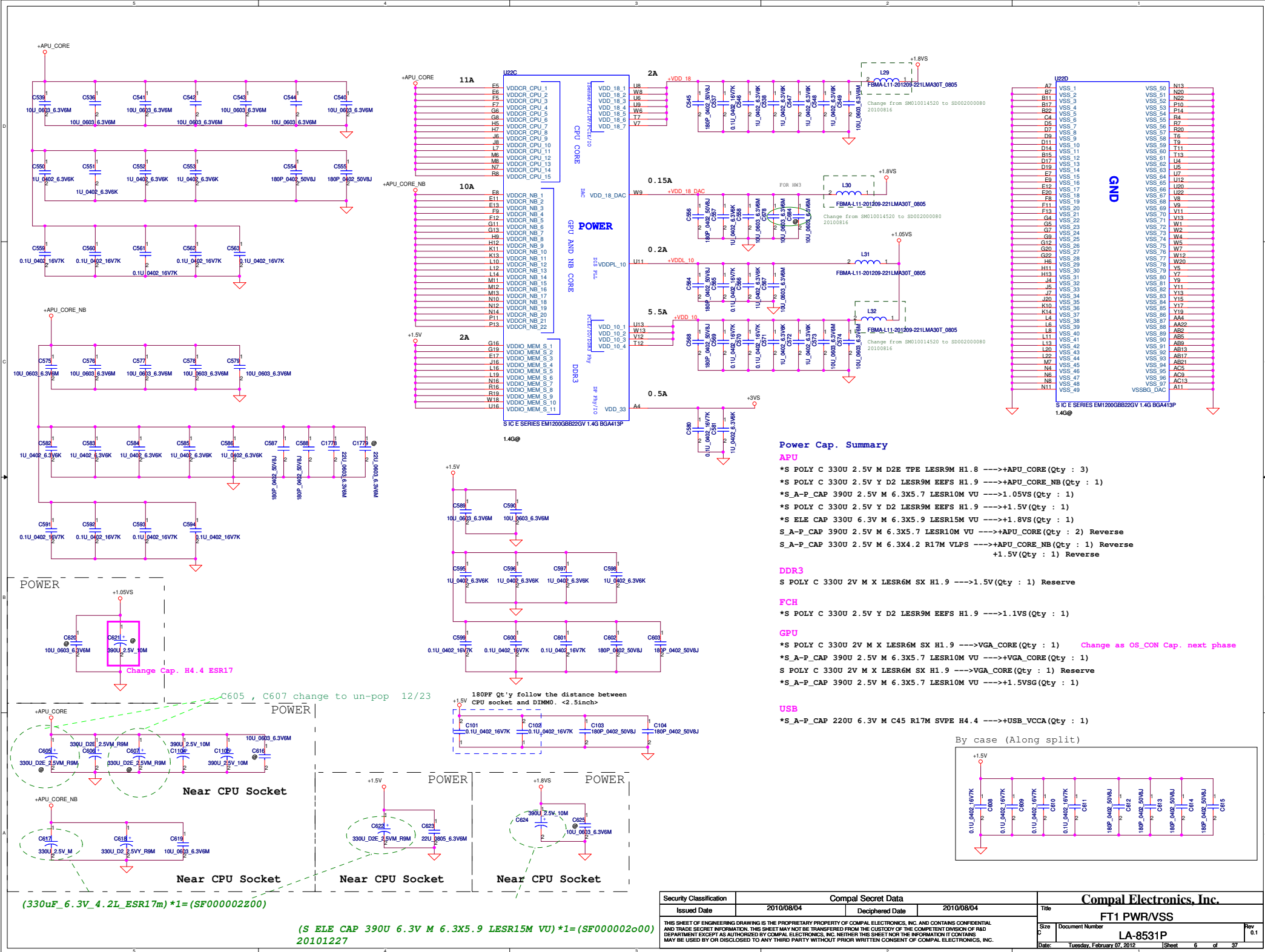
Vcc	3.3V +/- 5%				
Ra/Rc/Re	100K +/- 5%				
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max	
0	0	0 V	0 V	0 V	
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	
7	NC	2.500 V	3.300 V	3.300 V	

BTO Option Table

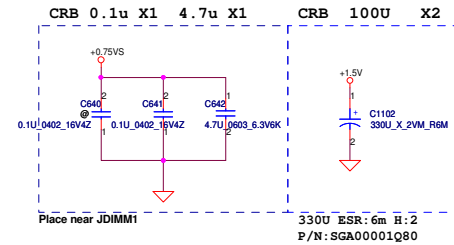
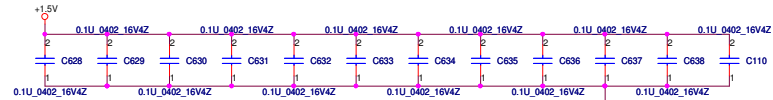
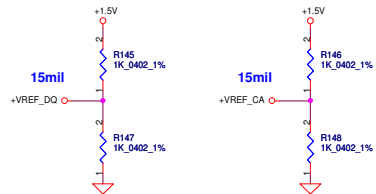
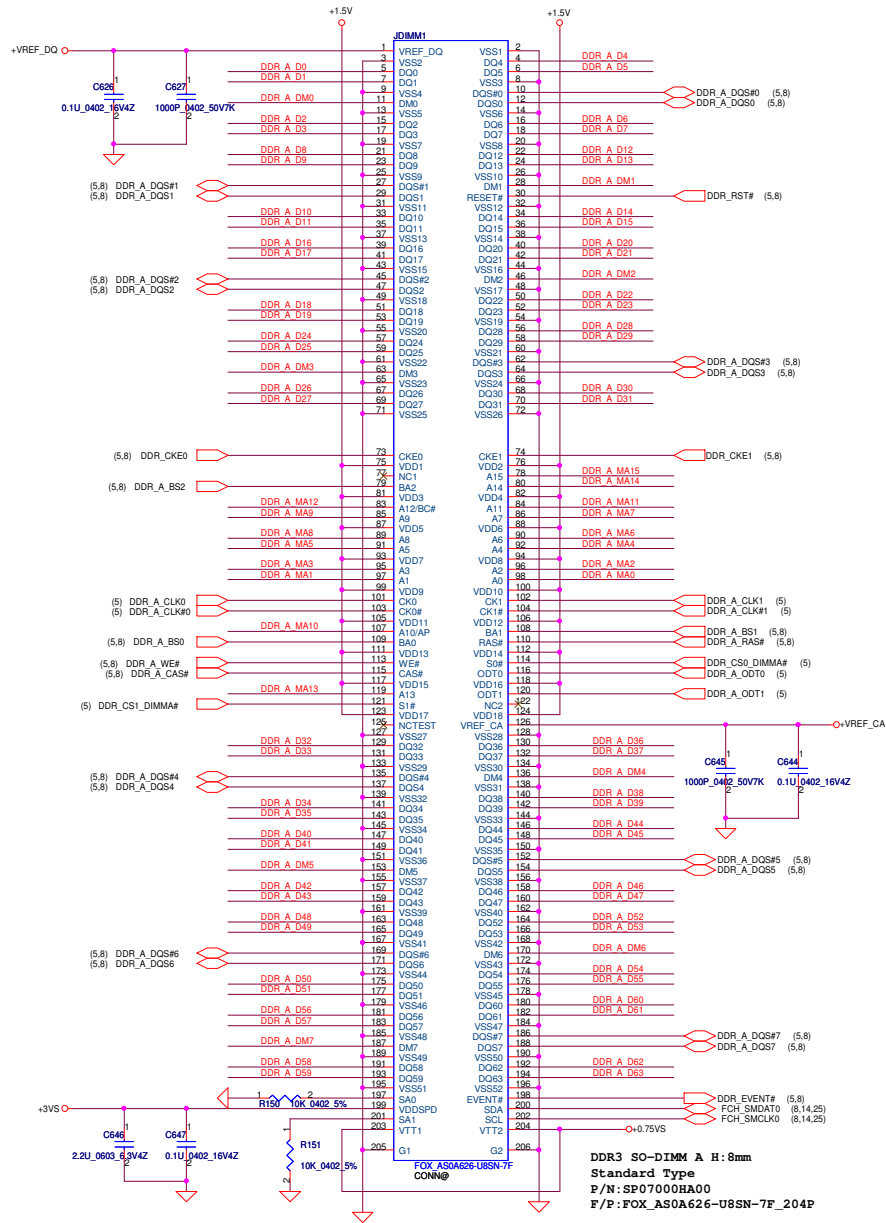
BTO Item	BOM Structure
AR8152	8152@
AR8151	8151@
Bluetooth	BT@
ALC271X	271X@
ALC281X	281X@
LVDS	LVDS@
EDP	EDP@
ODD zero power	ZERO@
APU_1.4G	1.4G@
APU_1.7G	1.7G@
normal ODD	ODD@

Project ID Table

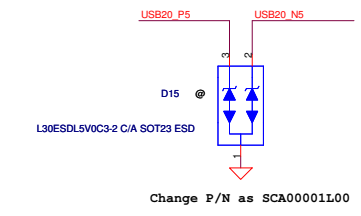
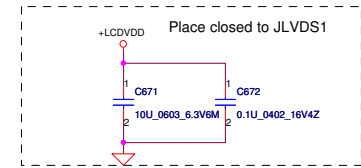
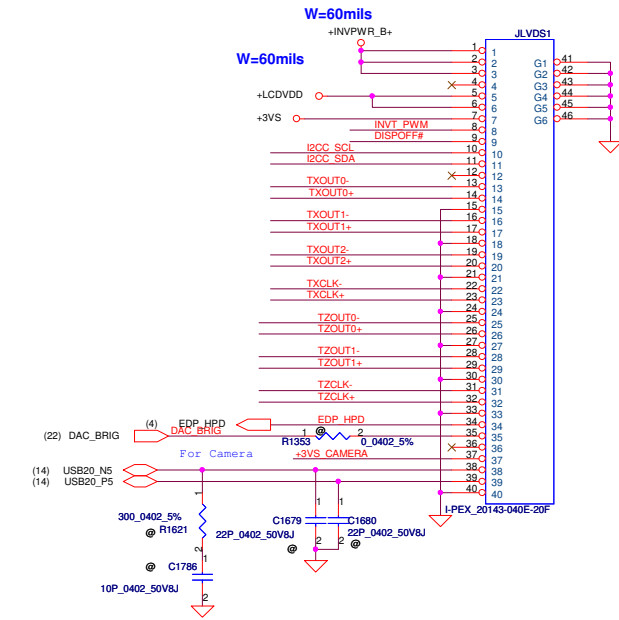
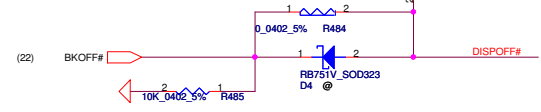
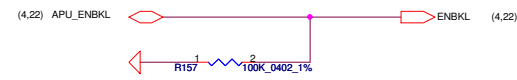
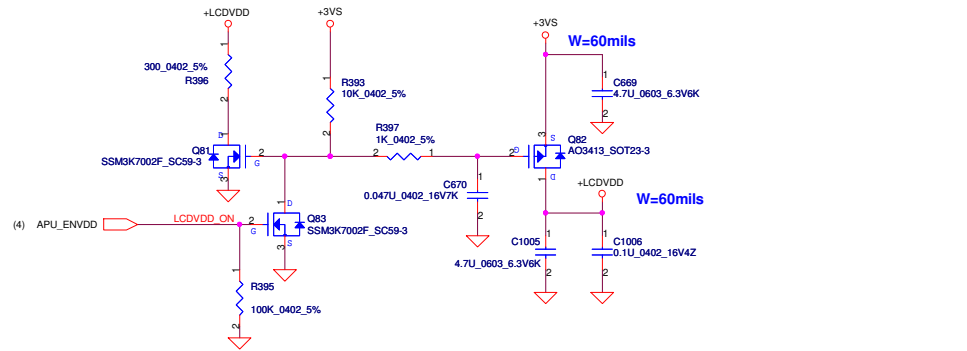
Board ID	PCB Revision
0	R01
1	R02
2	R03
3	
4	
5	
6	
7	



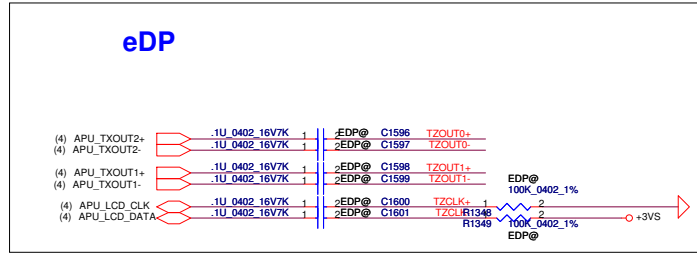
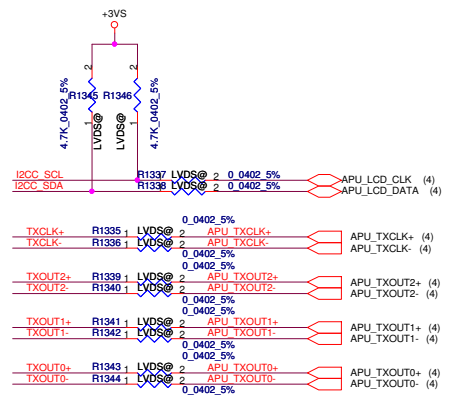
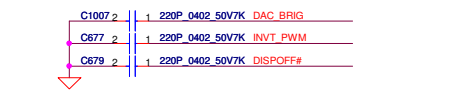
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		Deciphered Date		2010/08/04							
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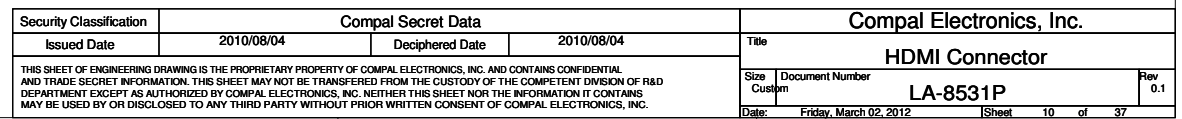
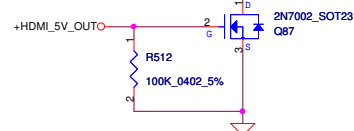
LCD POWER CIRCUIT



Change P/N as SCA000011L00



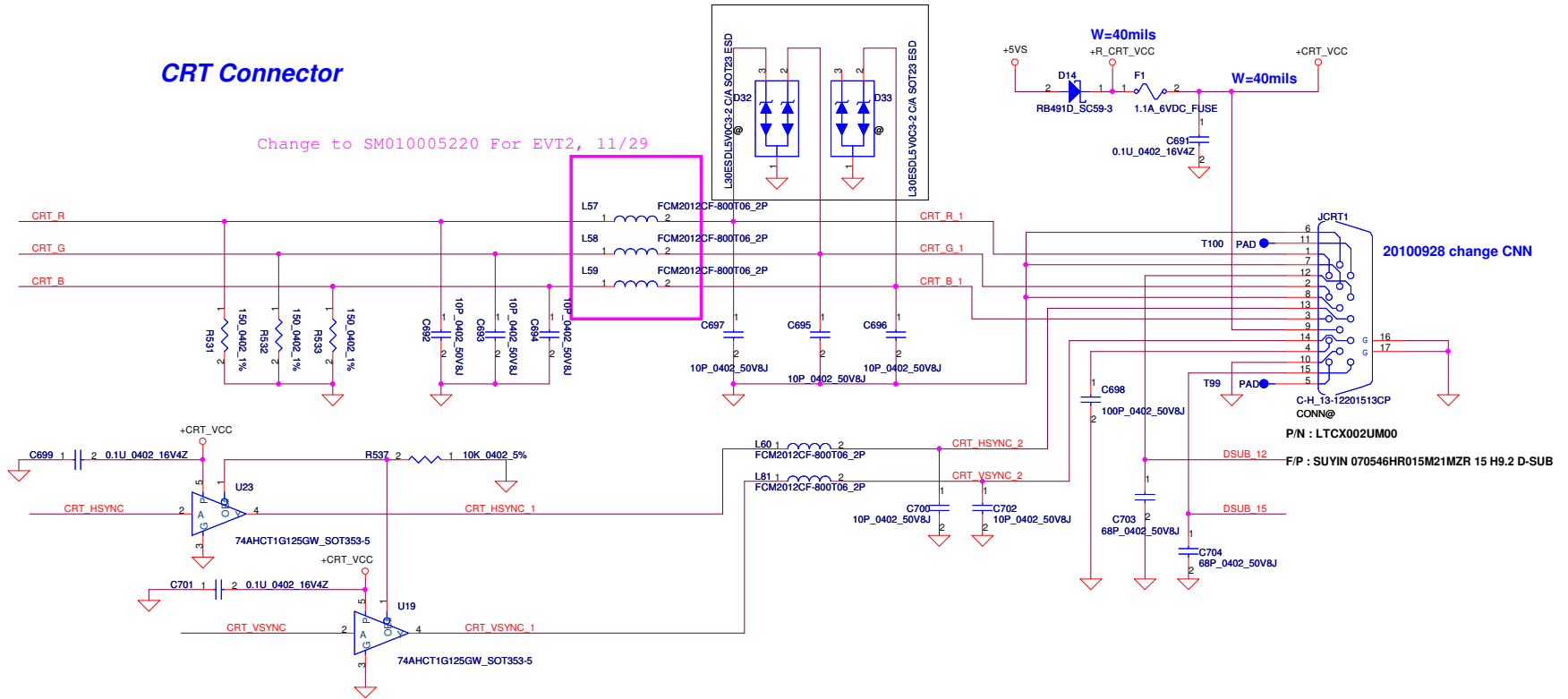
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CRT Connector

Change to SM010005220 For EVT2, 11/29

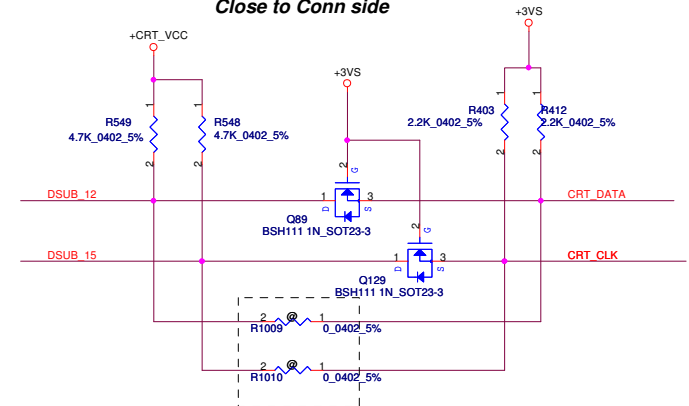
Change P/N as SCA00001L00



From APU

(4) APU_CRT_R	APU_CRT_R	CRT_R
(4) APU_CRT_G	APU_CRT_G	CRT_G
(4) APU_CRT_B	APU_CRT_B	CRT_B
(4) APU_CRT_HSYNC	APU_CRT_HSYNC	CRT_HSYNC
(4) APU_CRT_VSYNC	APU_CRT_VSYNC	CRT_VSYNC
(4) APU_CRT_DDC_SDA	APU_CRT_DDC_SDA	CRT_DATA
(4) APU_CRT_DDC_SCL	APU_CRT_DDC_SCL	CRT_CLK

Close to Conn side



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LAN
Cardeer Reader

WLAN

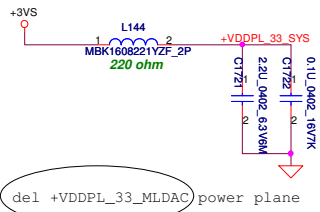
LAN

WLAN

Card Reader

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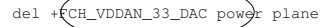
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Size	Document Number	LA8681P	Rev 0.1
Customer			
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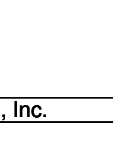
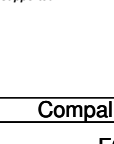
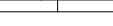
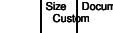
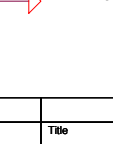
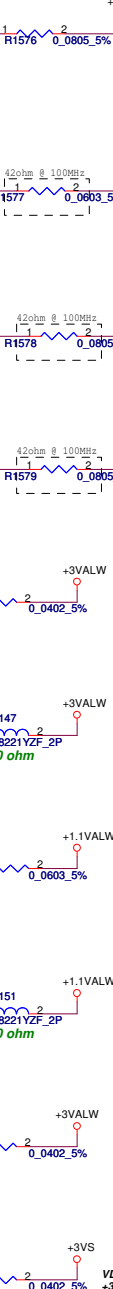
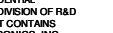
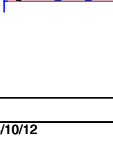
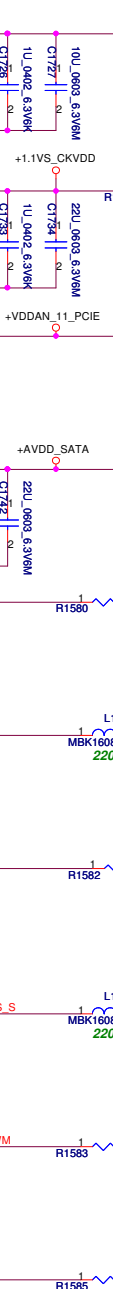
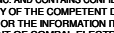
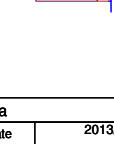
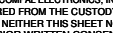
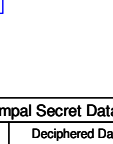
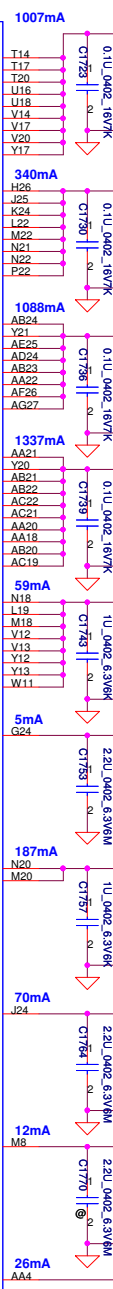
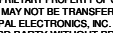
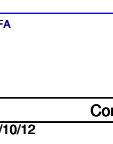
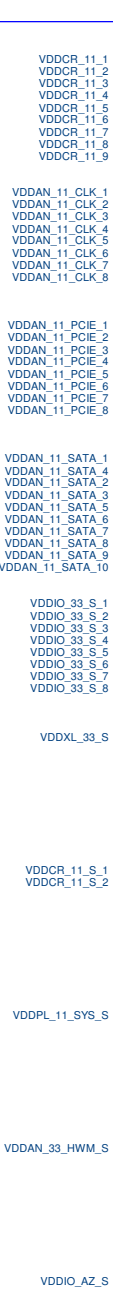
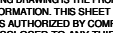
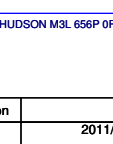
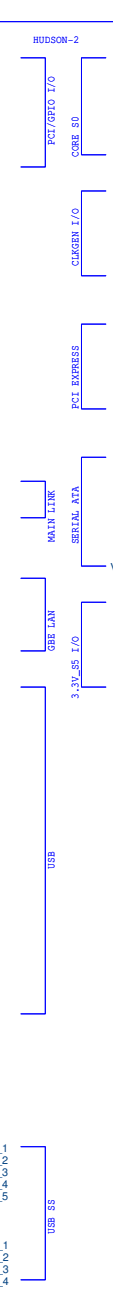
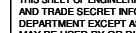
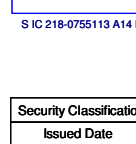
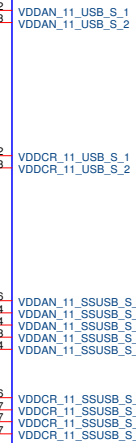
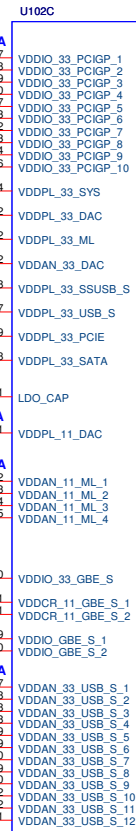
demo board connect to GND

VDDPL_33_SSUSB_S
For Hudson3 USB3.0 only
For Hudson2, connect to GND

LDO_CAP: Internally generated 1.8V
supply for the RGB outputs



demo board connect to GND

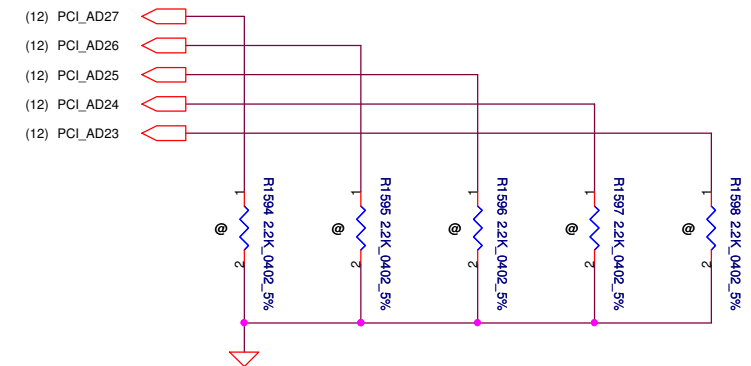
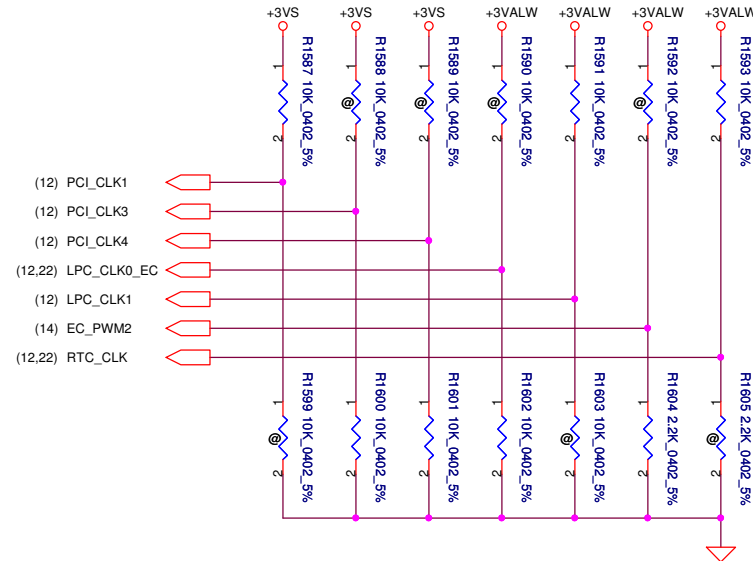


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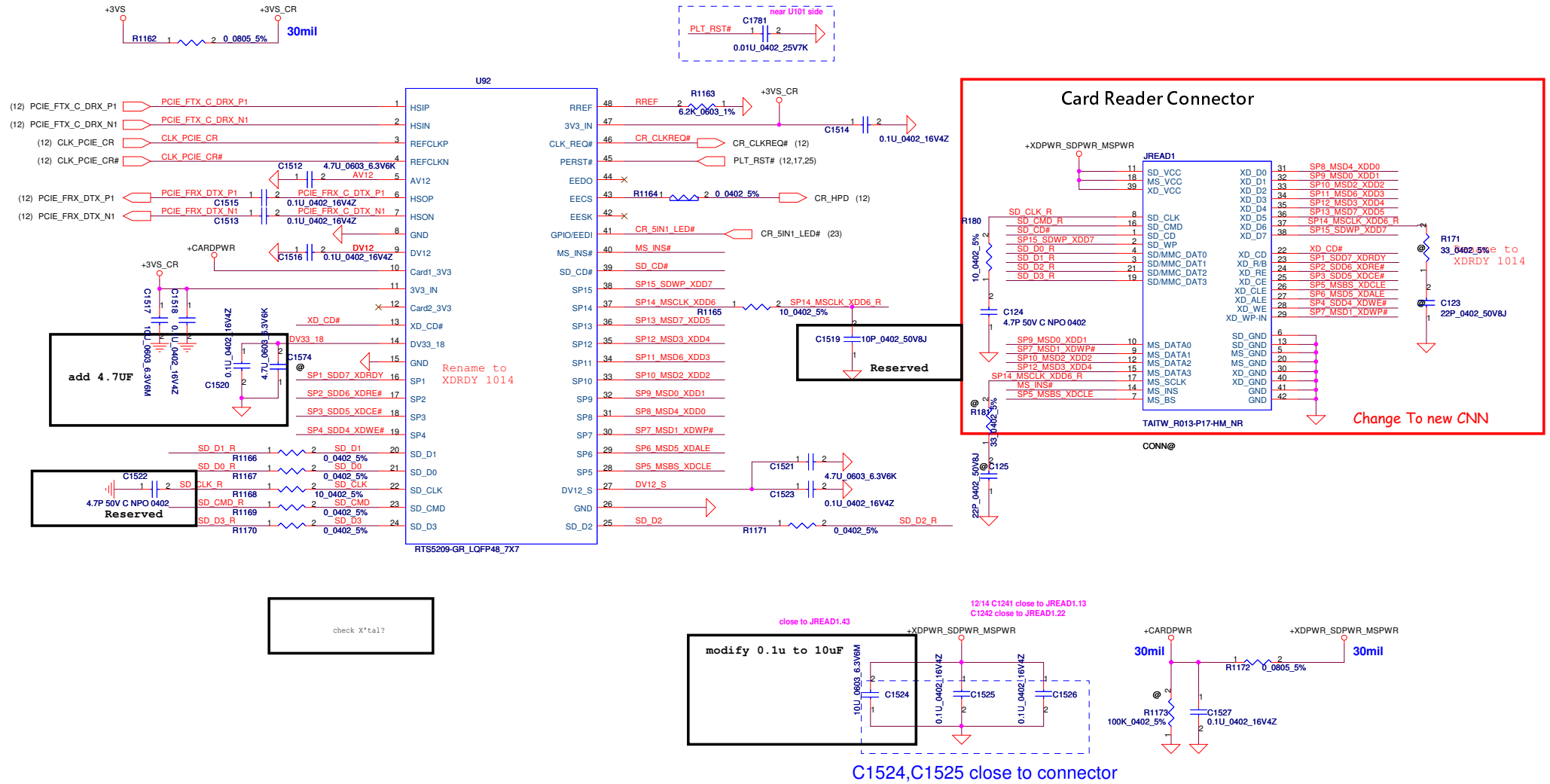
FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

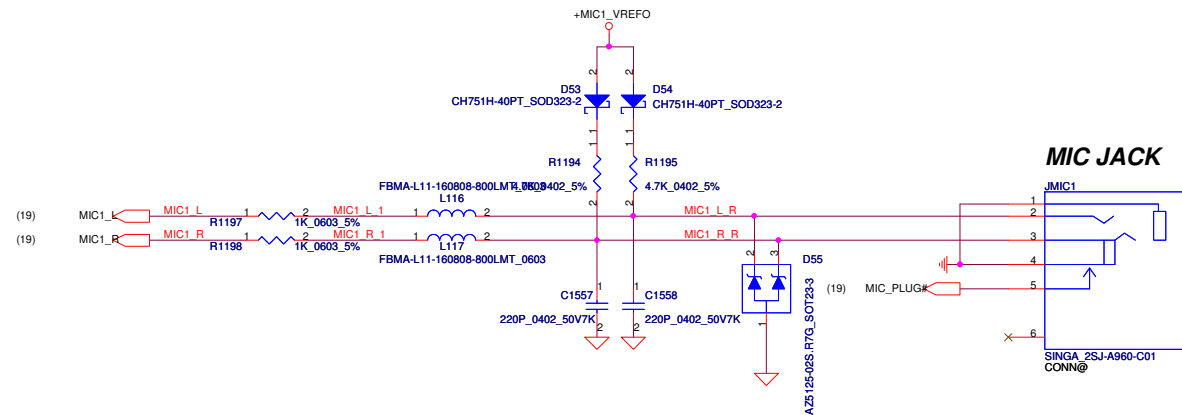
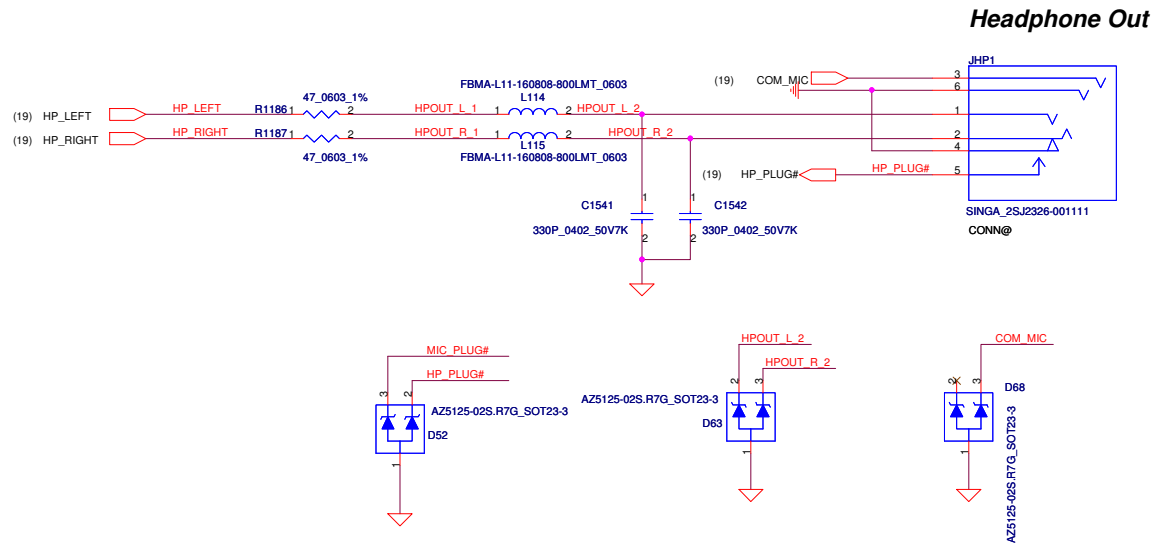
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



RTS5209-GR

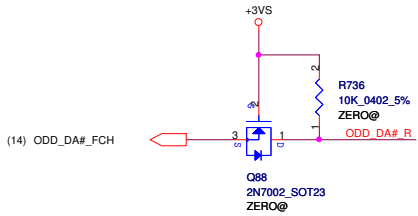
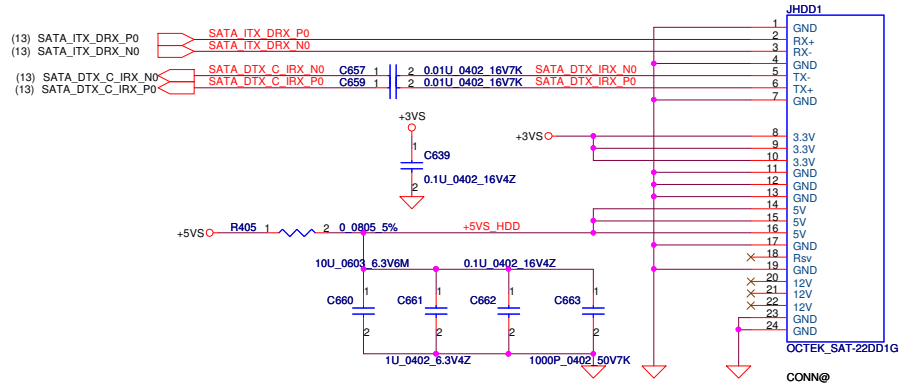


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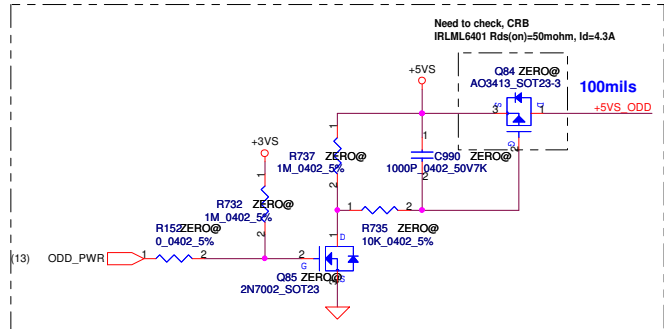
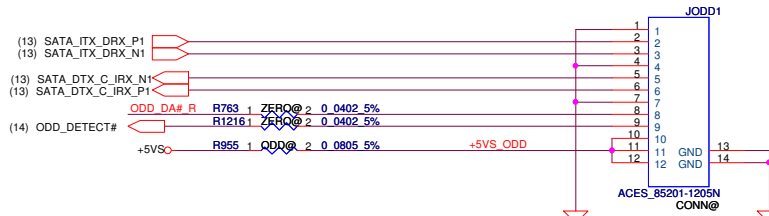
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SATA HDD Conn.

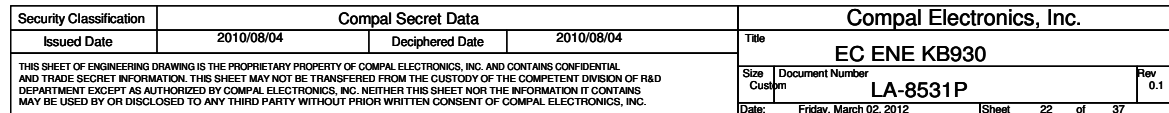


SATA ODD FFC Conn.

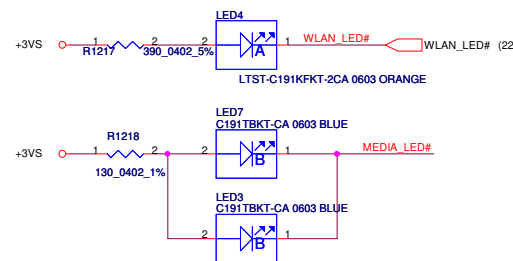
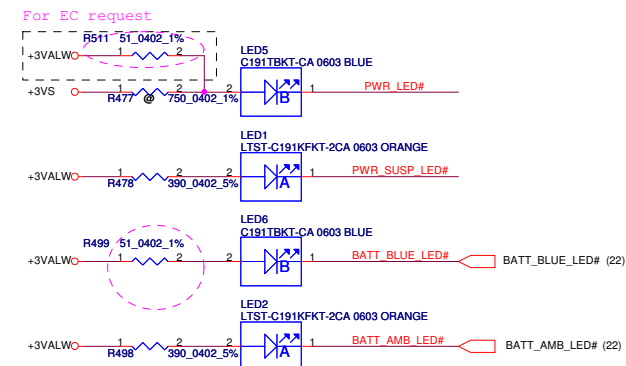
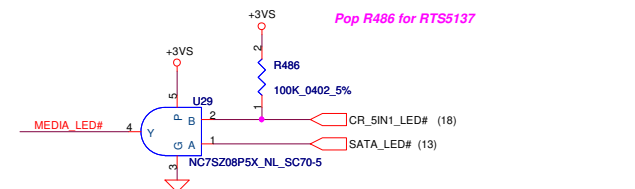
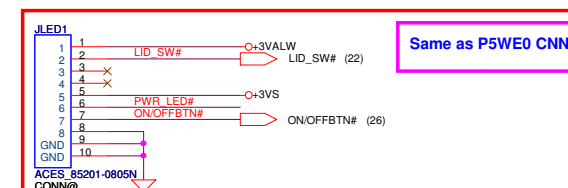
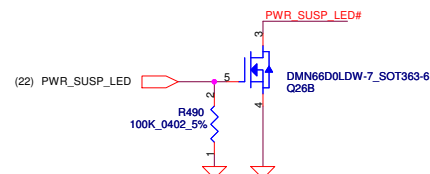
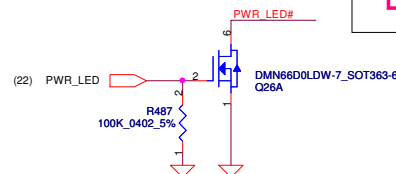
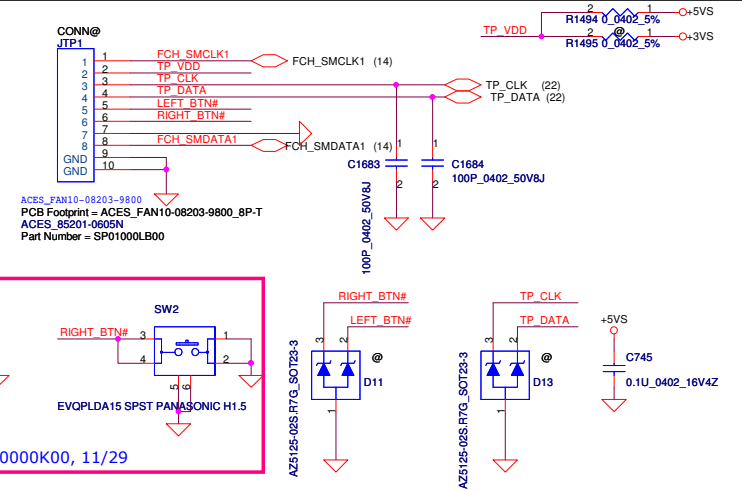
SATA ODD Conn.



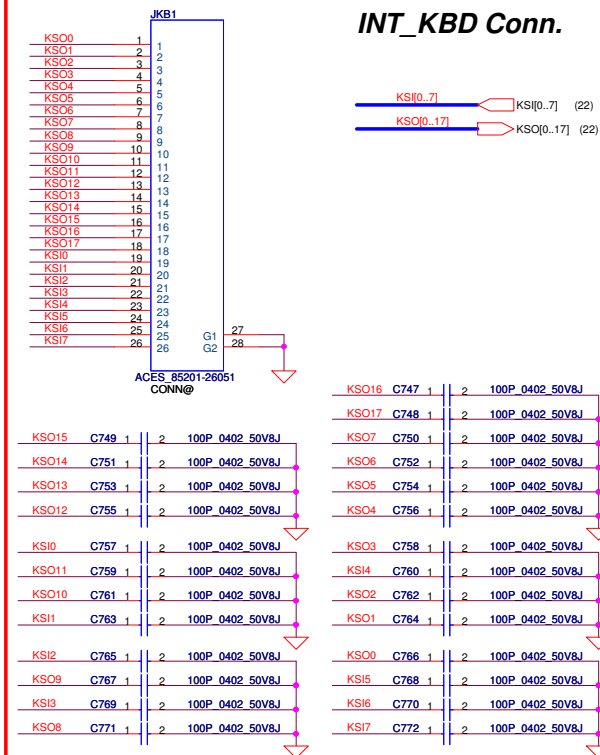
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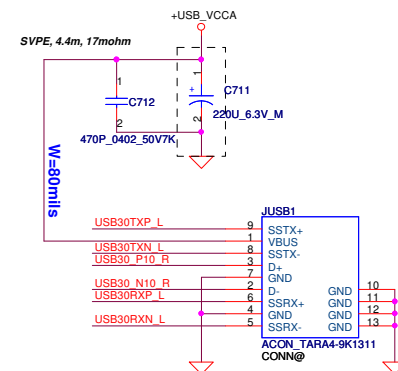
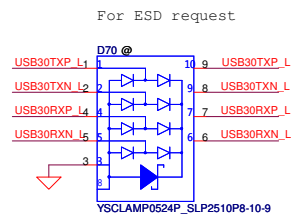
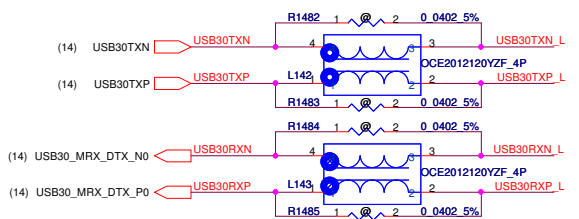
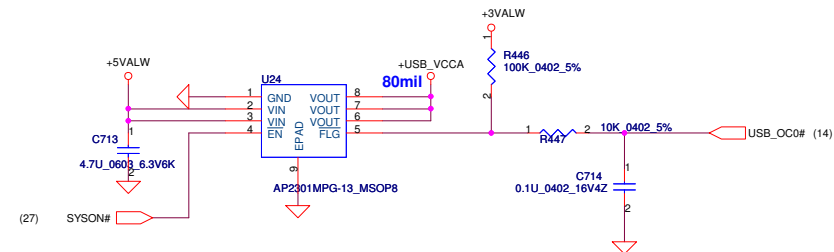
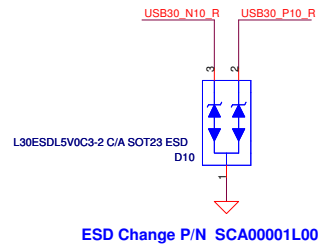
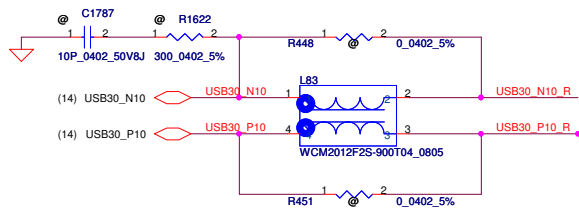


To TP/B Conn.

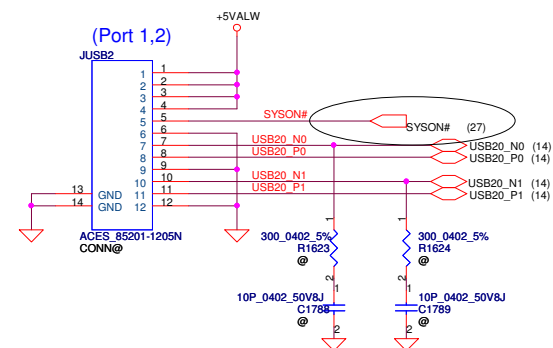
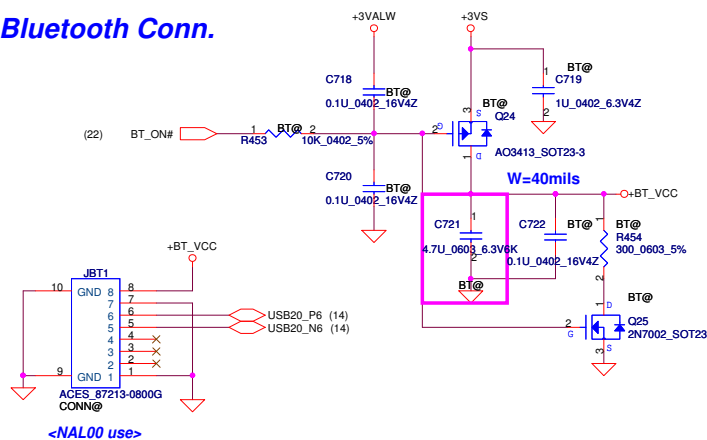


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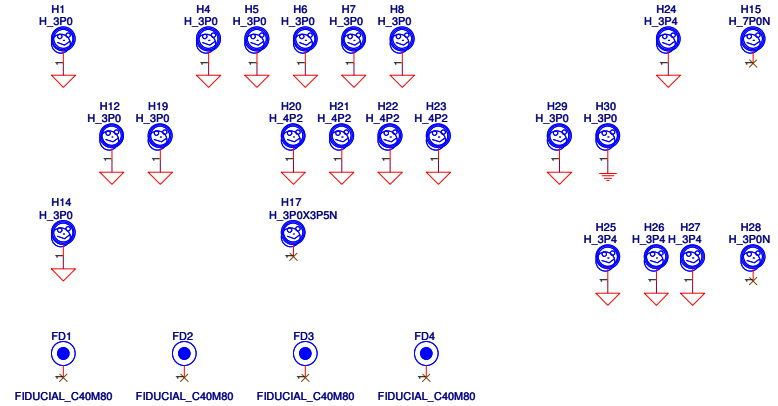
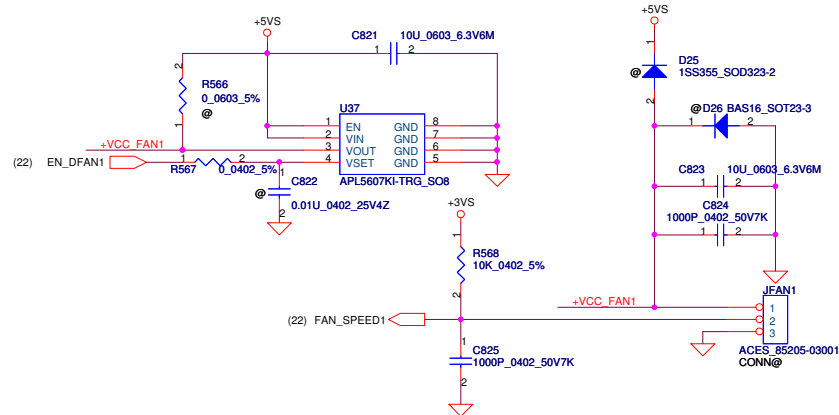
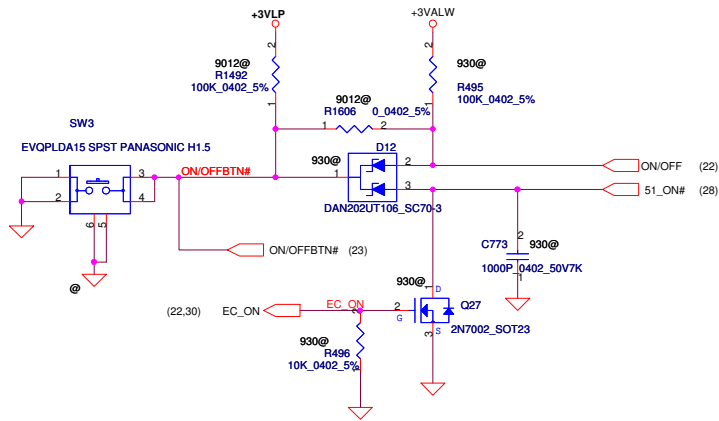




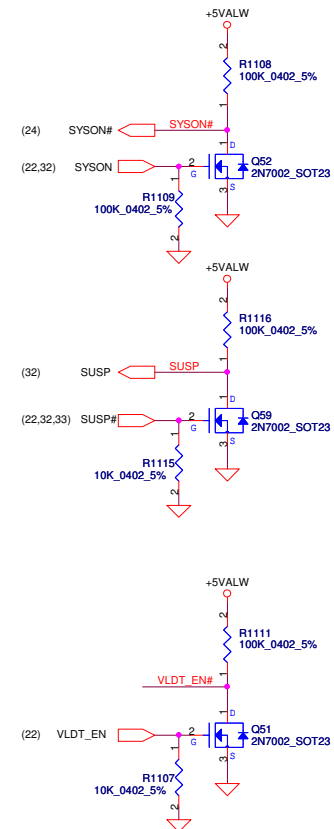
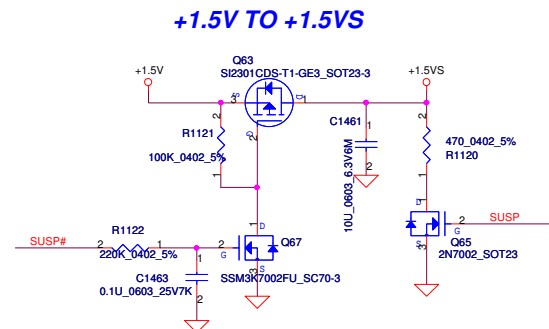
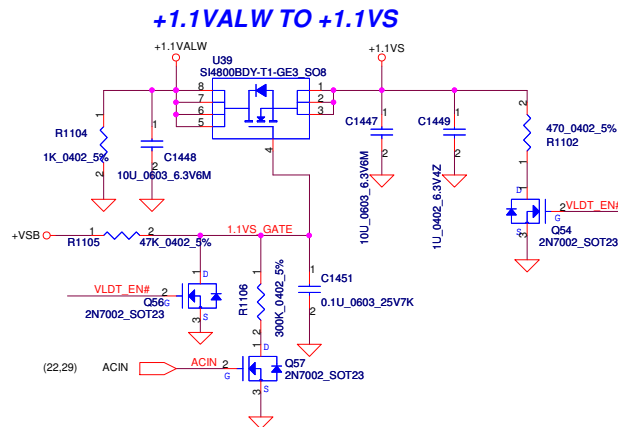
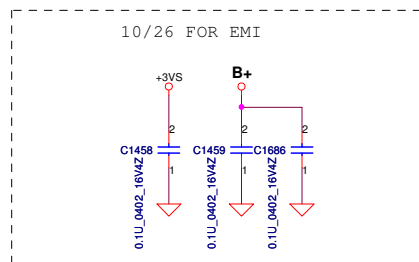
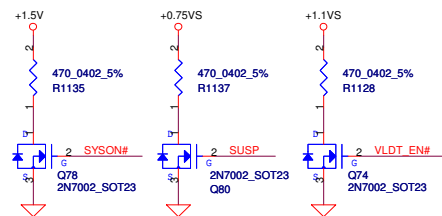
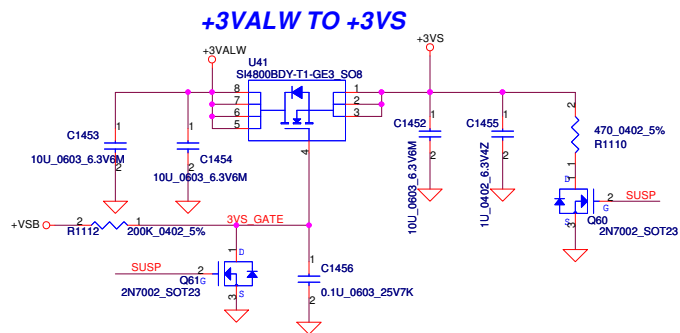
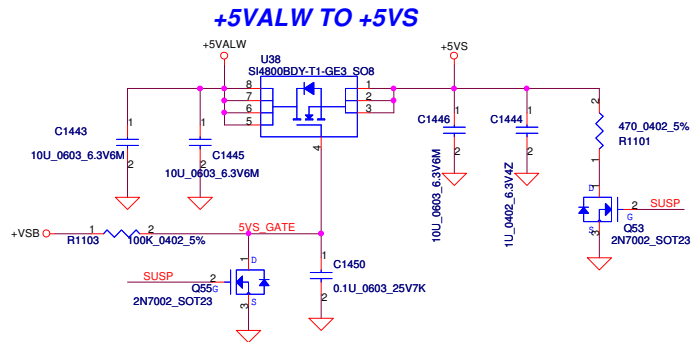
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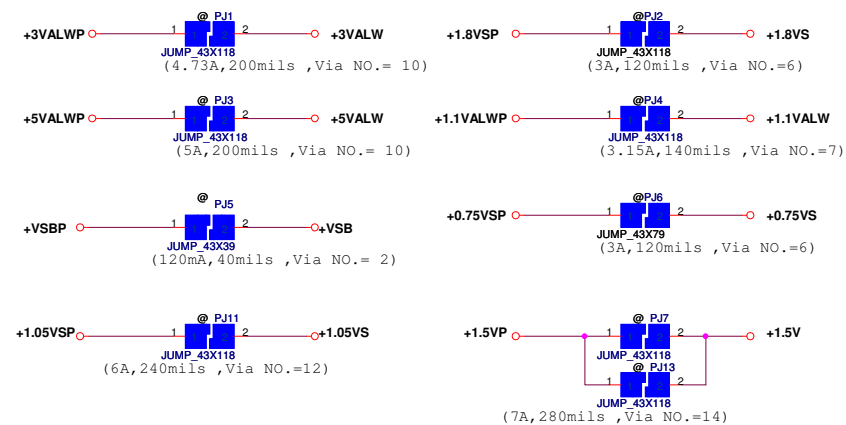
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						Size		Document Number		Rev	
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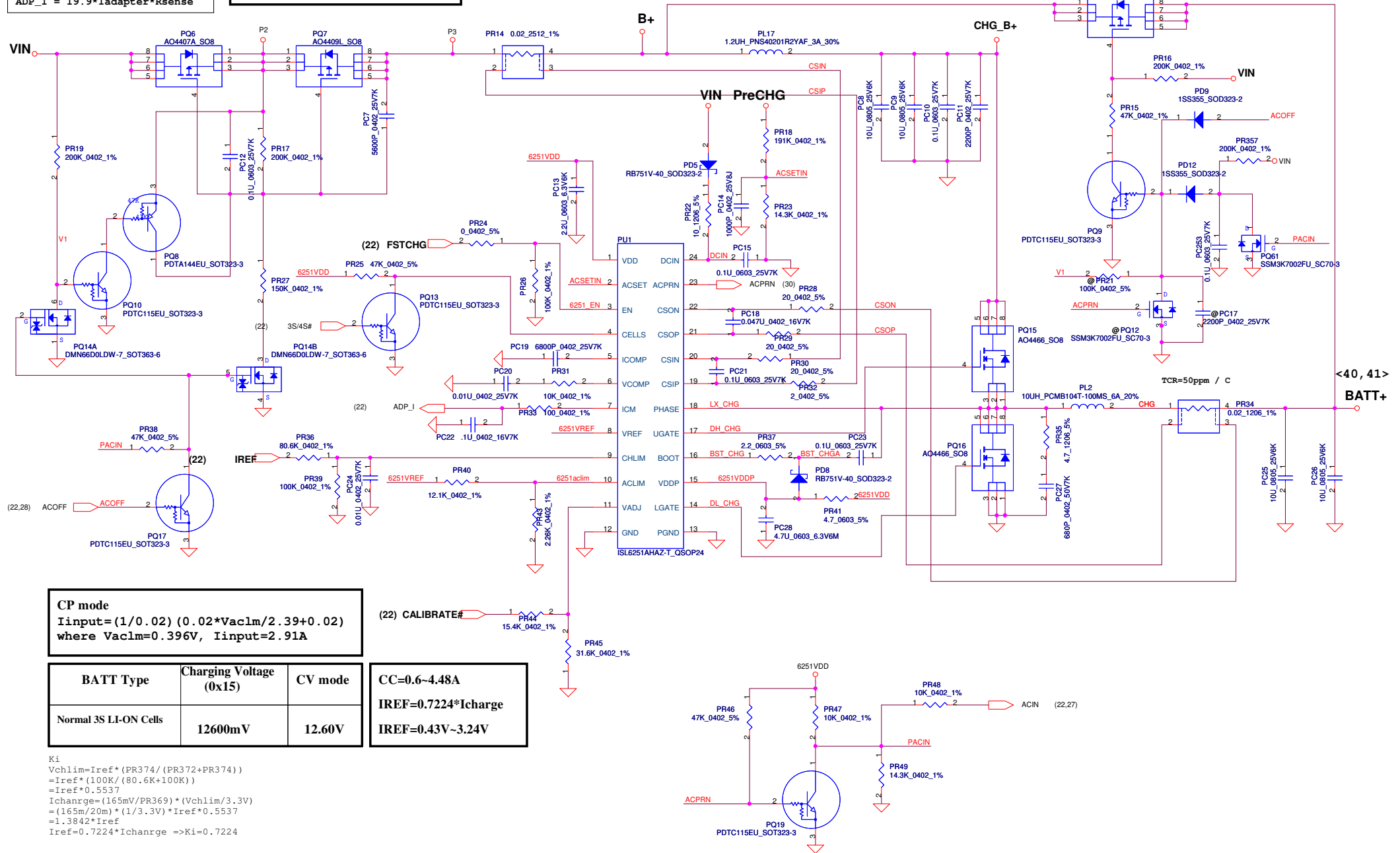


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Iada=0~3.421A (40W/19V=3.421A)

CP = 85%*Iada ; CP = 2.91A

ADP_I = 19.9*Iadapter*Rsense



CP mode
 $I_{input} = (1/0.02) (0.02 * V_{ac1m} / 2.39 + 0.02)$
where $V_{ac1m} = 0.396V$, $I_{input} = 2.91A$

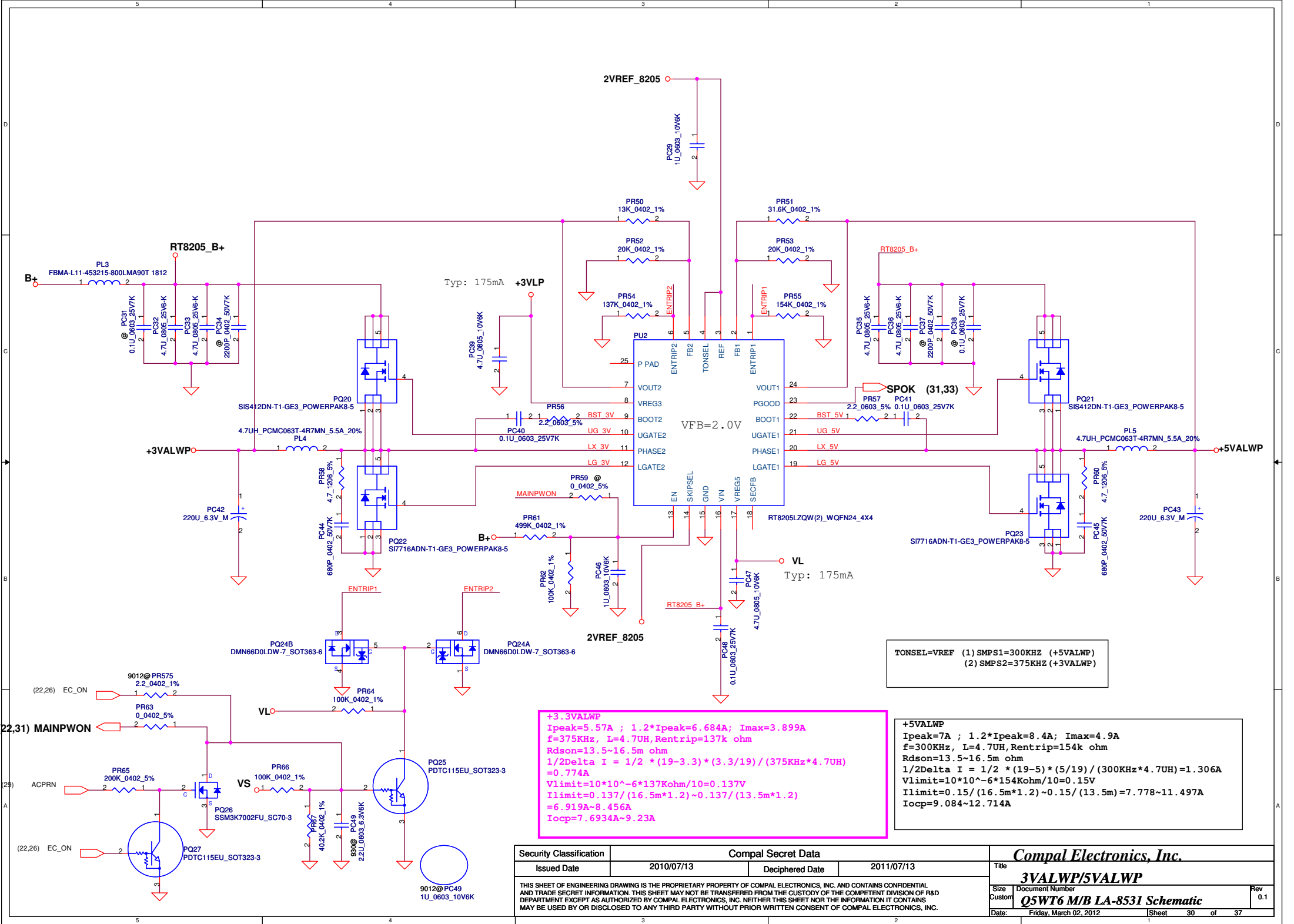
BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

CC=0.6~4.48A
 $I_{REF} = 0.7224 * I_{charge}$
 $I_{REF} = 0.43V \sim 3.24V$

Ki
 $V_{chlim} = I_{ref} * (PR374 / (PR372 + PR374))$
 $= I_{ref} * (100K / (80.6K + 100K))$
 $= I_{ref} * 0.5537$
 $I_{charge} = (165mV / PR369) * (V_{chlim} / 3.3V)$
 $= (165m / 20m) * (1 / 3.3V) * I_{ref} * 0.5537$
 $= 1.3842 * I_{ref}$
 $I_{ref} = 0.7224 * I_{charge} \Rightarrow Ki = 0.7224$

Kv
Rinternal ic=514K Rec=3K R1=PR379=15.4K R2=PR381=31.6K
 $R = 514K / (31.6K // (15.4K + 3K)) = 11.372K$
 $r = 514K / 514K // 31.6K = 28.14K$
 $V_{cell} = 0.175 * V_{adj} + 3.99V$
 $4.2V = 0.175 * V_{adj} + 3.99V \Rightarrow V_{adj} = 1.2V$
 $V_{adj} = V_{ref} * (R / (R + 514K)) + CALIBRATE * (r / (r + 514K))$
 $1.1483 = CALIBRATE * 0.6046 \Rightarrow CALIBRATE = 1.899$
 $1.899 = (4.2 - (V_{cell} + A * 0.175)) * Kv = (4.2 - (4.2 + A * 0.175)) * Kv$
 $A = V_{ref} * (R / (R + 514K)) = 0.052$
 $Kv = 9.451$

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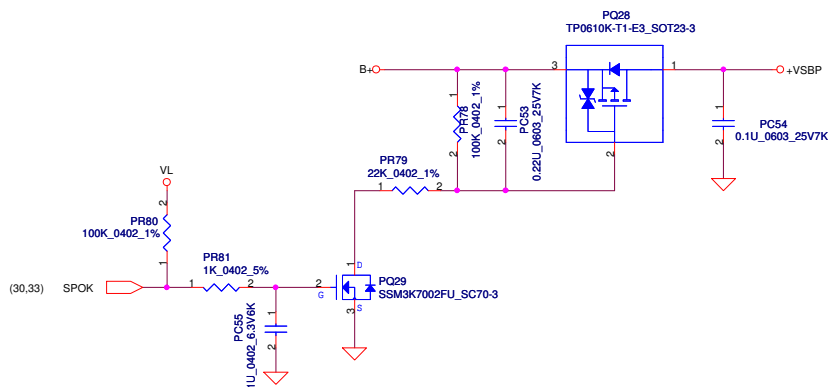
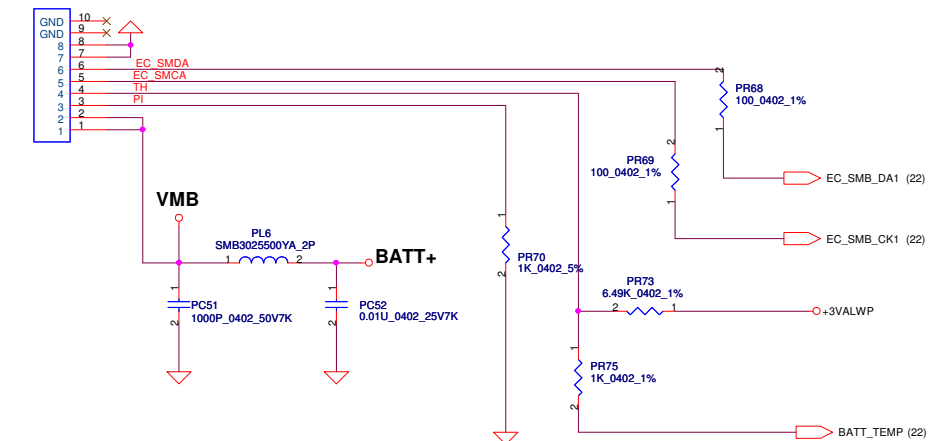
+3.3VALWP
Ipeak=5.57A ; 1.2*Ipeak=6.684A; Imax=3.899A
f=375KHz, L=4.7uH, Rentrip=137k ohm
Rdson=13.5~16.5m ohm
1/2Delta I = 1/2 *(19-3.3)*(3.3/19)/(375KHz*4.7uH)
=0.774A
Vlimit=10*10^-6*137Kohm/10=0.137V
Ilimit=0.137/(16.5m*1.2)~0.137/(13.5m*1.2)
=6.919A~8.456A
Iocp=7.6934A~9.23A

+5VALWP
Ipeak=7A ; 1.2*Ipeak=8.4A; Imax=4.9A
f=300KHz, L=4.7uH, Rentrip=154k ohm
Rdson=13.5~16.5m ohm
1/2Delta I = 1/2 *(19-5)*(5/19)/(300KHz*4.7uH)=1.306A
Vlimit=10*10^-6*154Kohm/10=0.15V
Ilimit=0.15/(16.5m*1.2)~0.15/(13.5m)=7.778~11.497A
Iocp=9.084~12.714A

TONSEL=VREF (1) SMPS1=300KHz (+5VALWP)
(2) SMPS2=375KHz (+3VALWP)

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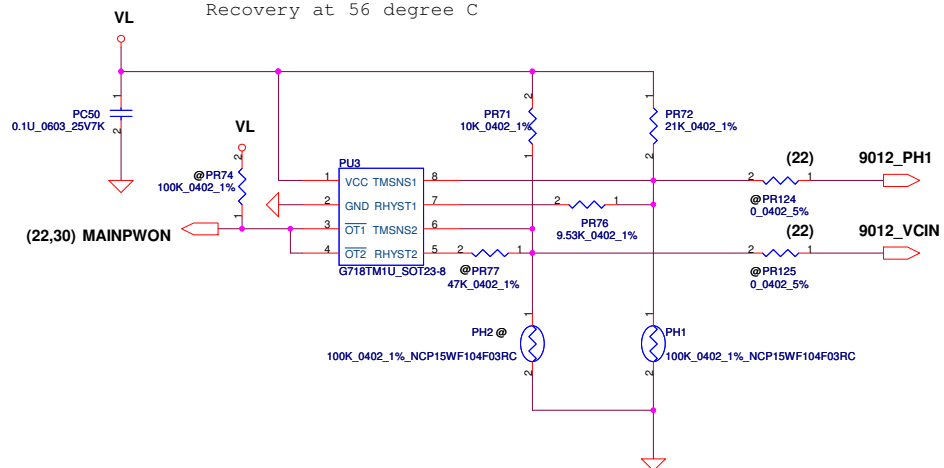
CONN@ PJP2
SUYIN_200275GR008G13GZR



PH1 under CPU botten side :

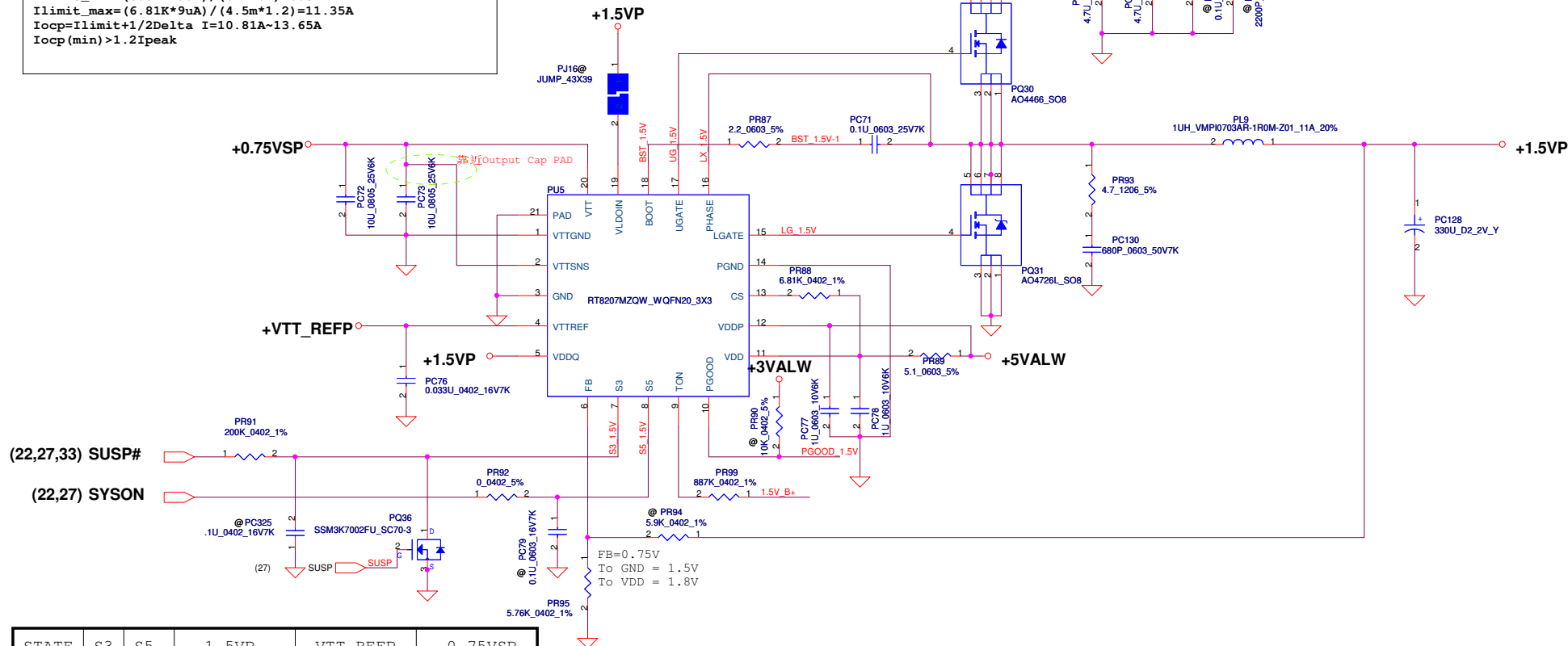
CPU thermal protection at 92 degree C

Recovery at 56 degree C



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+1.5VP
 $I_{peak}=7.7A$; $1.2*I_{peak}=9.24A$; $I_{max}=5.39A$
 $1/2\Delta I=2.305(F=300KHz)$
 $PR88=(1.2*I_{peak}-1/2\Delta I)*R_{ds(on)(max)}*1.2/9\mu A=6.65K\Omega$
 choose $PR88=6.81K\Omega$ (for safety $>1.2I_{peak}$)
 $R_{ds(on)}=6m\Omega$ (max) ; $R_{ds(on)}=4.5m\Omega$ (typical)
 $I_{limit_min}=(6.81K*9\mu A)/(6m*1.2)=8.51A$
 $I_{limit_max}=(6.81K*9\mu A)/(4.5m*1.2)=11.35A$
 $I_{ocp}=I_{limit}+1/2\Delta I=10.81A-13.65A$
 $I_{ocp(min)}>1.2I_{peak}$

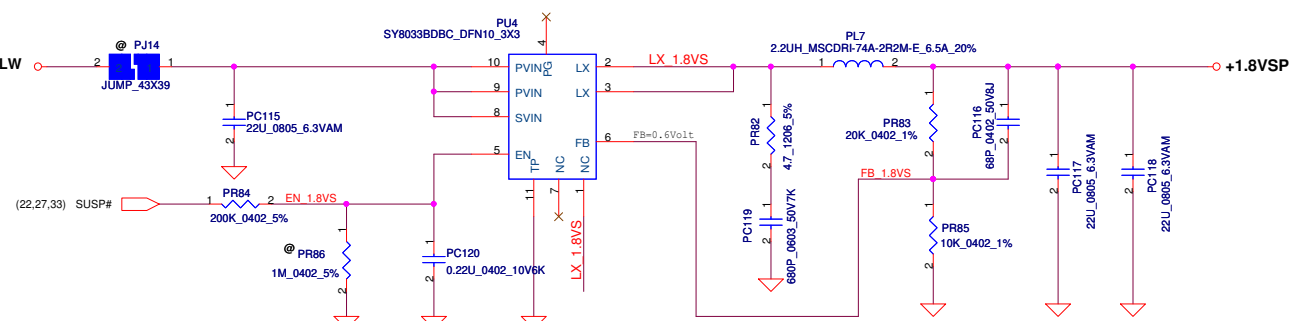


(22,27,33) SUSP#

(22,27) SYSON

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

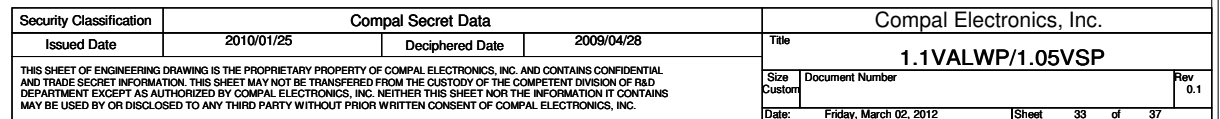
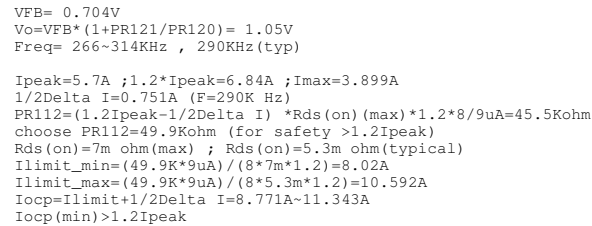
Note: S3 - sleep ; S5 - power off




```

Ipeak=4.5A ; 1.2*Ipeak=5.4A ; Imax=3.15A
1/2Delta I=0.785A (F=290K Hz)
PR123=(1.2Ipeak-1/2Delta I) *Rds(on)(max)*1.2*8/9uA=88.6Kohm
choose PR123=90.9Kohm (for safety >1.2Ipeak)
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Ilimit_min=(90.9K*9uA)/(8*18m*1.2)=6.25A
Ilimit_max=(90.9K*9uA)/(8*15m*1.2)=7.5A
Iocp=Ilimit+1/2Delta I=7.035A-8.285A
Iocp(min)>1.2Ipeak

```



Version change list (P.I.R. List)

Page 1 of 2
for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Modify 40W adapter CP point	0.1	29	PR14 change to SD00000CI10 (S RES 1/2W 0.05 +-1% 1206 100PPM/C) PR40 change to SD034470180 (S RES 1/16W 4.7K +-1% 0402)	2011/10/28	EVT
2		Modify +1.05VSP OCP	0.1	33	PR112 change to SD034499280 (S RES 1/16W 49.9K +-1% 0402)	2011/10/28	EVT
3		Modify +1.1VALWP OCP	0.1	33	PR123 change to SD034909280 (S RES 1/16W 90.9K +-1% 0402)	2011/10/28	EVT
4		Modify +1.5VP OCP	0.1	32	PR88 change to SD034681180 (S RES 1/16W 6.81K +-1% 0402)	2011/10/28	EVT
5		Modify ISN CHOKE P/N	0.1	29	PL17 change to SH00000N300 (S COIL 1.2UH +-30% PNS40201R2YAF 3A)	2011/10/28	EVT
6		Modify bead P/N	0.1	30	PL3 change to SM01000JF00 (S SUPPRE_ FBMA-L11-453215-800LMA90T 1812)	2011/10/28	EVT
7		Change boost resister from 0 ohm to 2.2 ohm for RT8207 & TPS51125	0.1	30	PR87 & PR98 & PR107 change from 0 ohm to 2.2 ohm	2011/11/17	EVT2
8		Modify power sequence for RT8207(+1.5VP & 0.75VSP)	0.1	30	PR91 change from 0 ohm to 200K ohm	2011/11/17	EVT2
9		Modify compoment P/N for material issue	0.1	29	PQ7 change from SB00000I600(S TR SI4459ADY-T1-GE3 1P SO8) to SB00000JD10 (S TR AO4409L 1P SO8)	2011/11/23	EVT2
10		design change for EC(9012)	0.1	28	delete PD1,PD2,PR1,PR2,PR4,PC6	2011/11/28	EVT2
11		design change for EC(9012)	0.1	29	add PR575(S RES 1/16W 2.2 +-1% 0402) PC49 change to 1U_0603_10V6K	2011/11/28	EVT2
12		design change for EC(9012)	0.1	31	add PR124(0_0402_5%)	2011/11/28	EVT2
13					change PR56,PR57 from 0 ohm to 2.2 ohm		
14		Improve EMI performance	0.2		add PR58,PR60,PR93,PR119 (SD001470B80,S RES 1/4W 4.7 +-5% 1206) add PC44,PC45,PC104 (SE074681K80,S CER CAP 680P 50V K X7R 0402) add PC130 (SE025681K80,S CER CAP 680P 50V K X7R 0603) change PR189,PR190 from 0 ohm to 2.2 ohm	2011/12/20	DVT
15							
16		Modify +5VALW voltage for USB port voltage drop (HW request +5VALW up 3%)	0.2	31	change PR51 from 30K ohm to 31.6K ohm	2011/12/20	DVT

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Issued Date	2010/04/12	Deciphered Date	2010/10/12	Title	PIR (PWR)
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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Modify component P/N for material shortage issue	0.2		change PC8,PC9,PC25,PC26,PC57,PC58 to SE000000QK00 (S CER CAP 10U 25V K X5R 0805 H1.25	2011/12/20	DVT
2		Change OTP from 9012 to G718	0.2	31	Delete PR124 (0_0402_5%)	2011/12/28	DVT
3		Change CP for 65W adapter	0.3	29	Change PR14 from SD000000CI10(S RES 1/2W 0.05 +-1% 1206 100PPM/C) to SD0000001F00 (S RES 1W .02 +-1% 2512)	2012/2/6	PVT
4		Change CP for 65W adapter	0.3	29	Change PR40 from 4.7K to 4.7K Change PR43 from 20K to 2.26K	2012/2/6	PVT
5		Modify for component common P/N	0.3	32	change PQ36 from SB0000009Q80 to SB0000009610	2012/2/13	PVT
6		Modify for component P/N for cost concern	0.3	32	change PC128 from SGA000002280 (S POLY C 330U 2.5V Y D2 LESR15M CX H1.9) to SGA20331E10 (S POLY C 330U 2V Y D2 LESR9M EEFSX H1.9)	2012/2/24	PVT
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