

Compal Confidential

HM51_TR/HM70_TR Discrete

NDWG2/NDWH1 LA5992 Schematic Document

Mobile AMD S1G3/RS880M/SB710

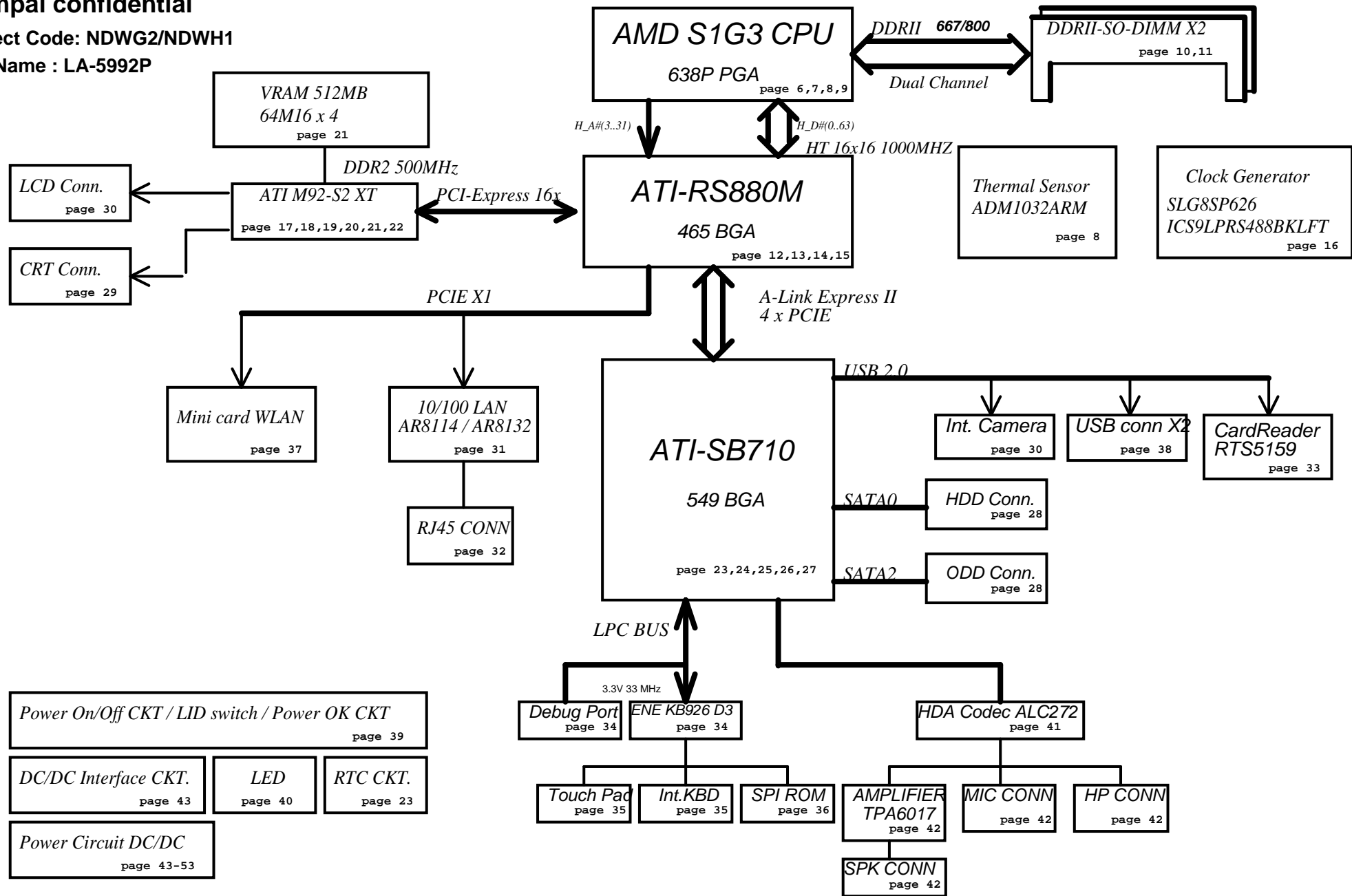
2009/12/02 Rev 1.0

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				Date	Thursday, March 18, 2010
				Sheet	1 of 55
				Rev	C

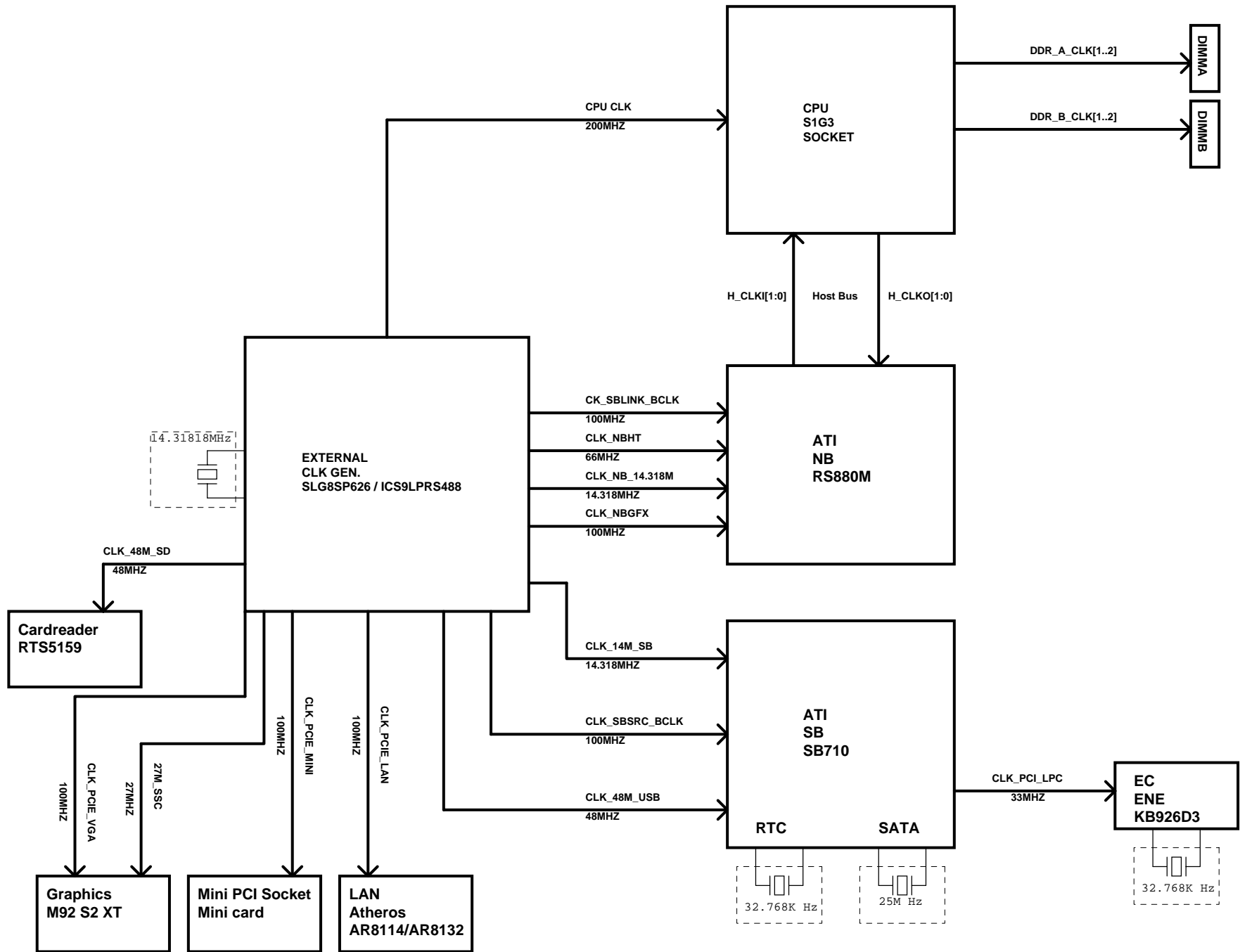
Compal confidential

Project Code: NDWG2/NDWH1

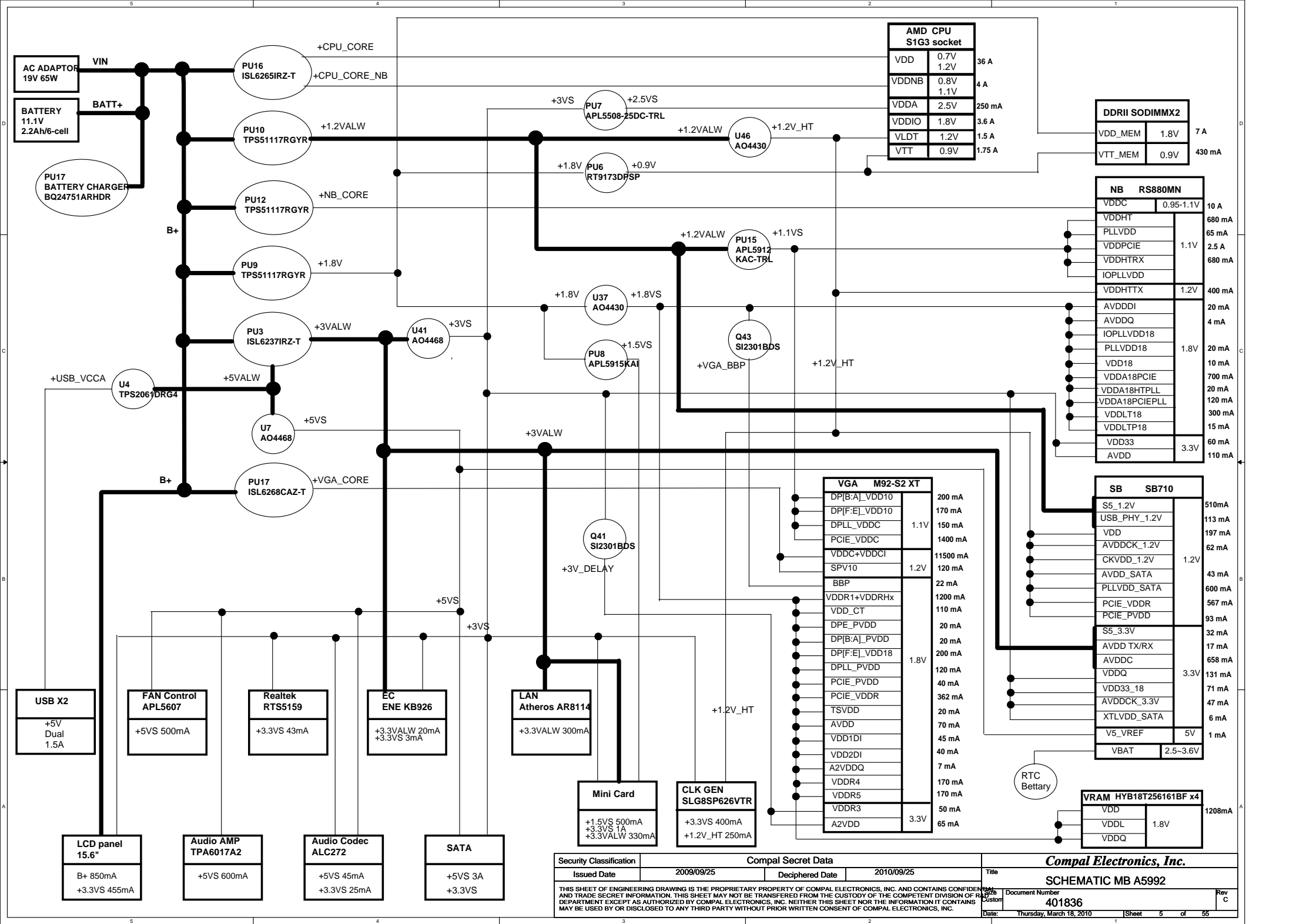
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				Date	Thursday, March 18, 2010
				Sheet	2 of 55



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				Date	Thursday, March 18, 2010
				Sheet	4 of 55

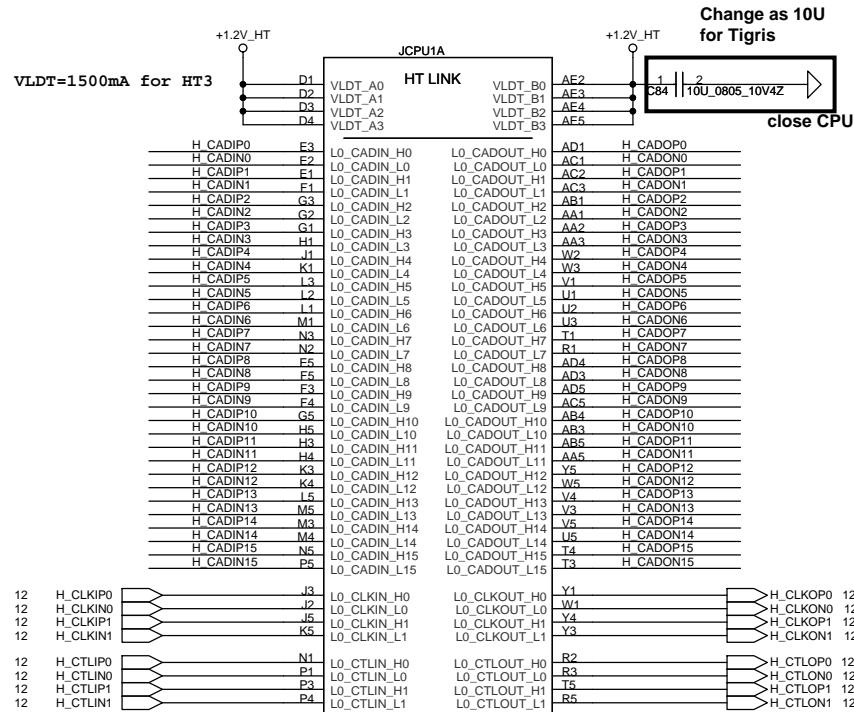


12 H_CADIP[0..15] H_CADIP[0..15]
12 H_CADIN[0..15] H_CADIN[0..15]

H_CADOP[0..15] H_CADOP[0..15] 12
H_CADON[0..15] H_CADON[0..15] 12

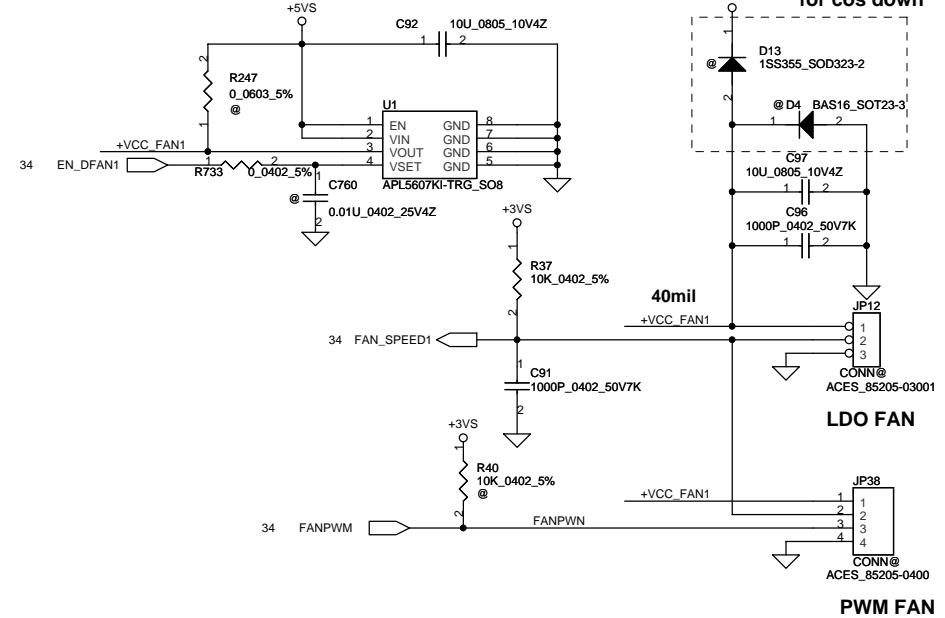
FAN Control Circuit

Reserve when PVT
for cos down

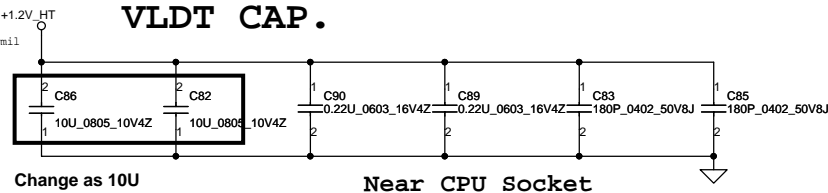


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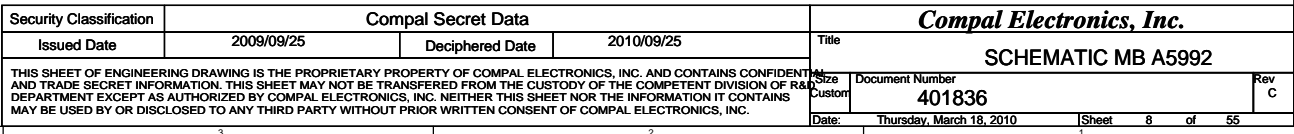
Athlon 64 S1
Processor Socket



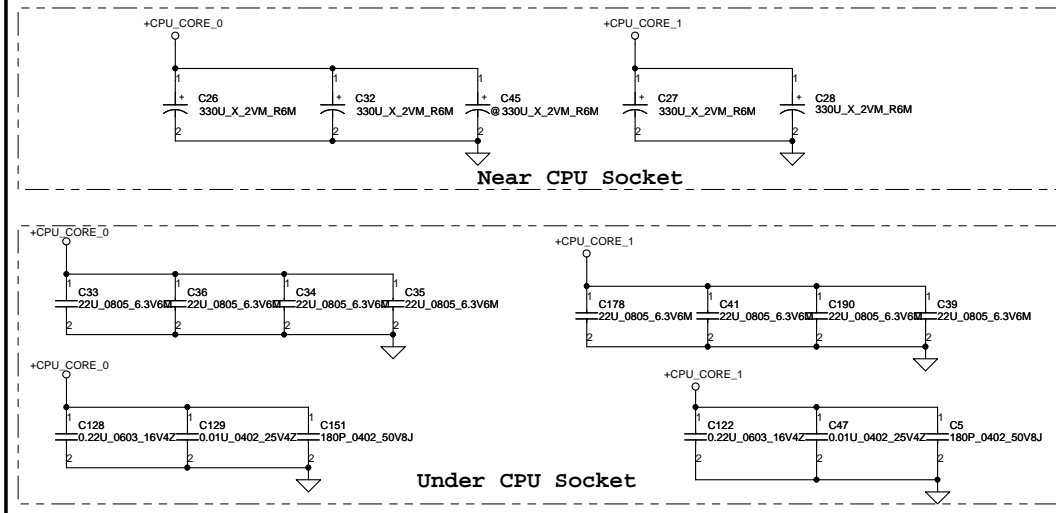
VLDT CAP.



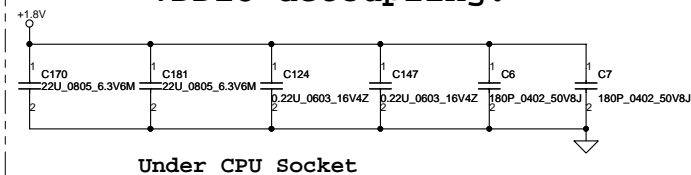
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Size	Custom	Document Number	401836	Rev C
Date:	Thursday, March 18, 2010	Sheet	6	of 55



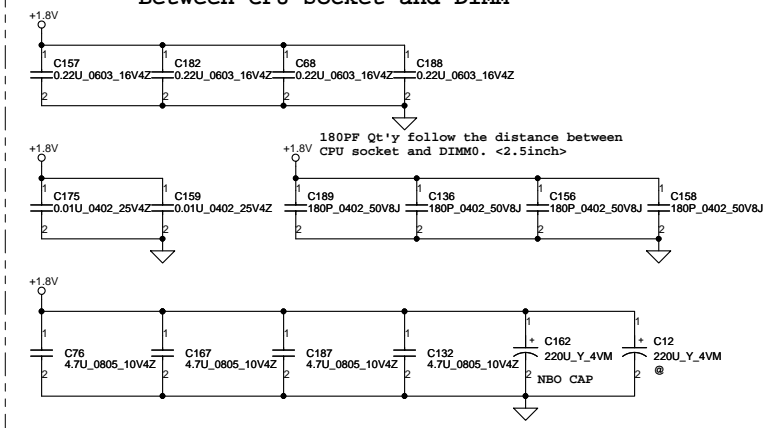
VDD(+CPU_CORE) decoupling.



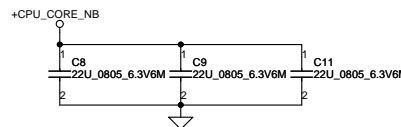
VDDIO decoupling.



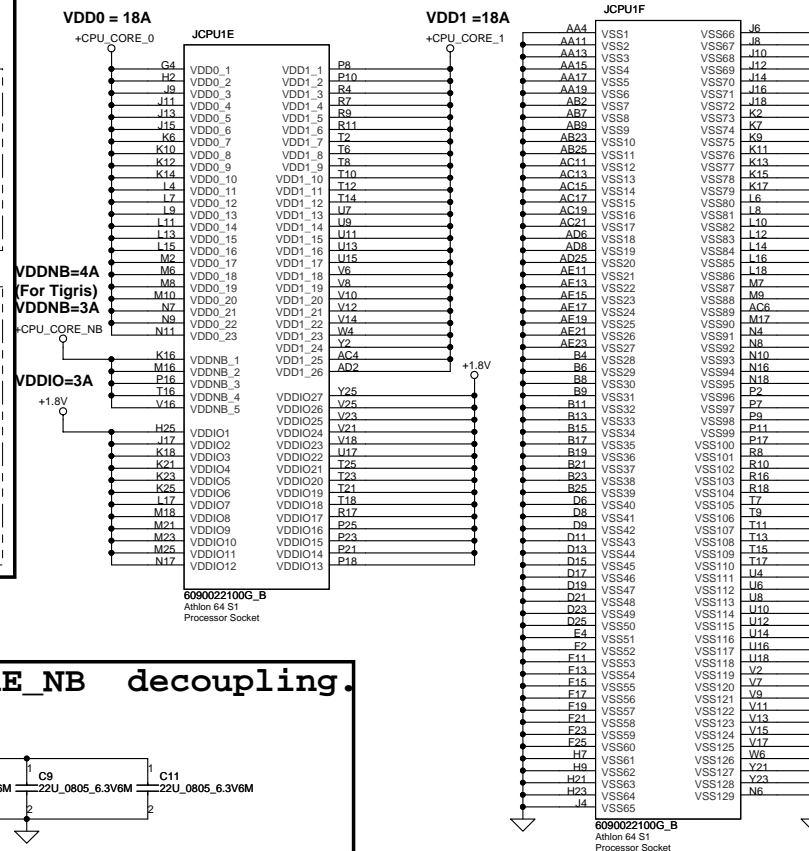
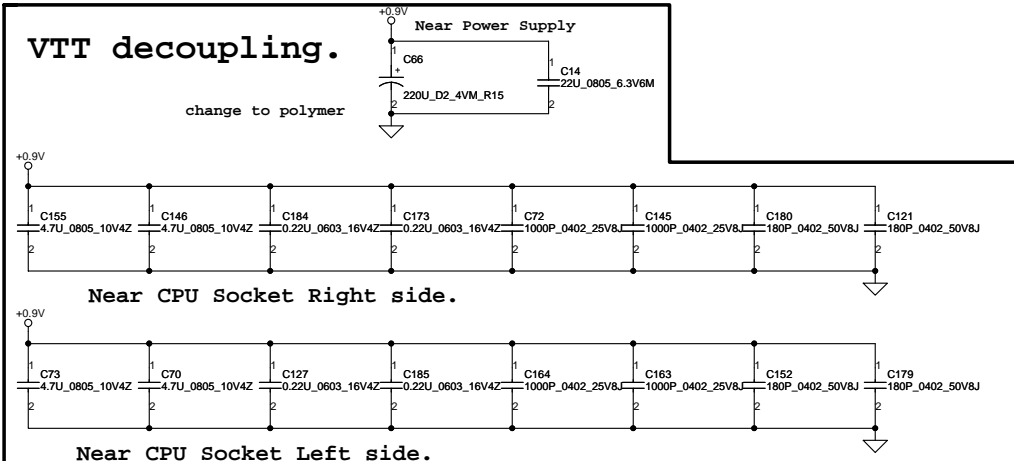
Between CPU Socket and DIMM



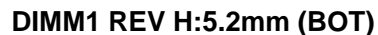
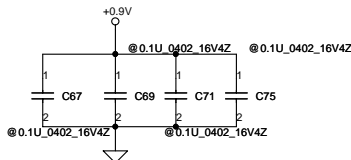
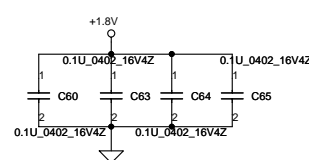
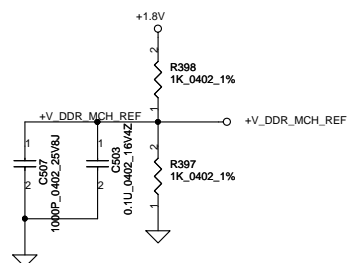
```
+CPU_CORE_NB    decoupling.
```



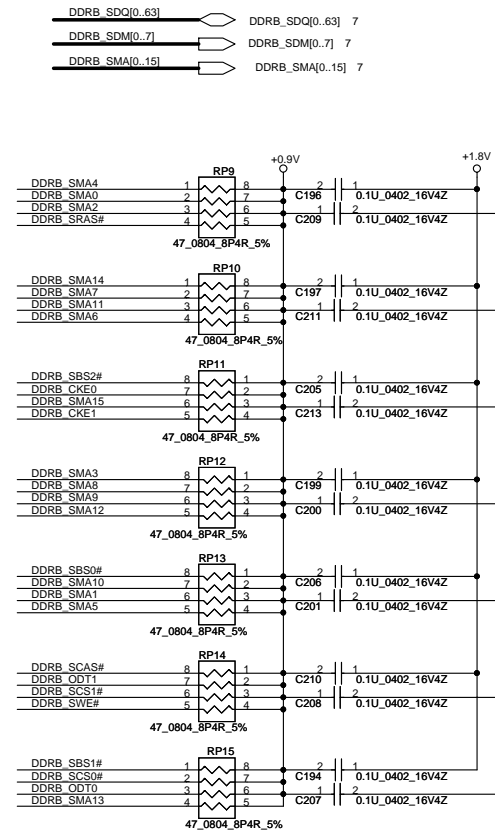
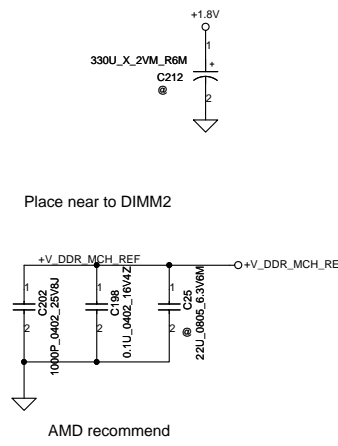
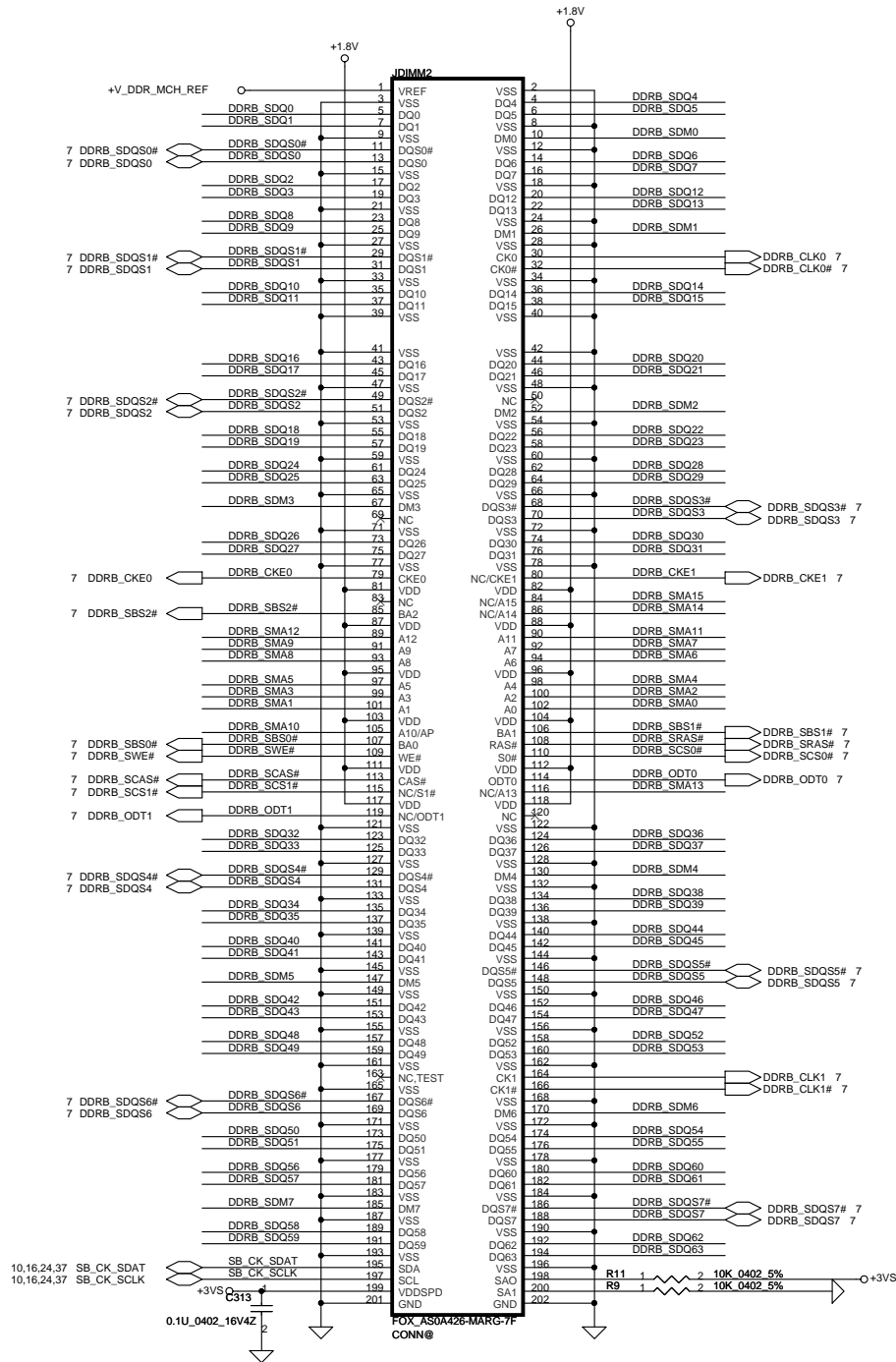
VTT decoupling.

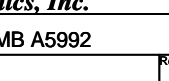
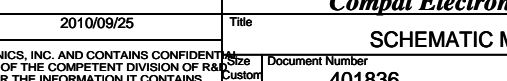
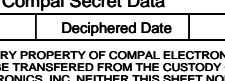
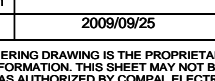
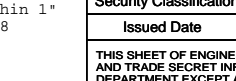
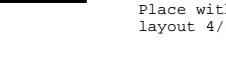
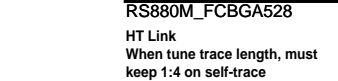
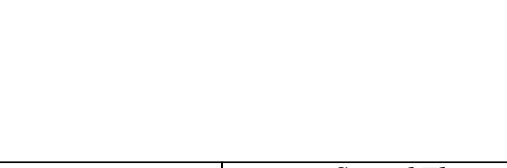
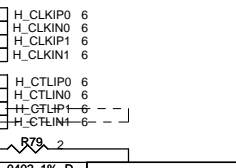
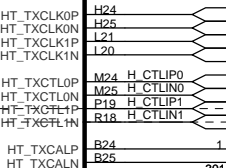
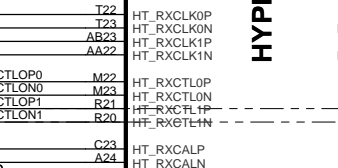
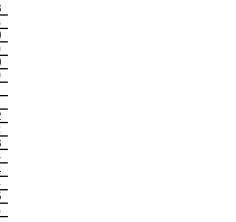
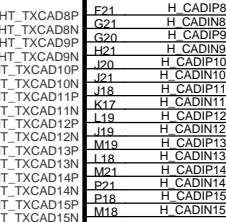
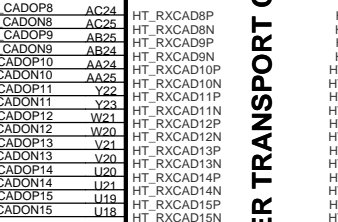
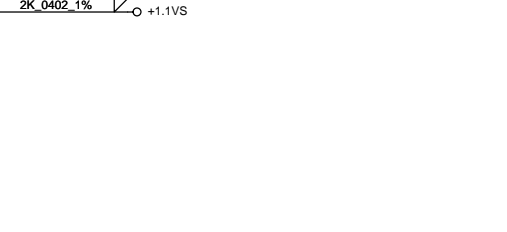
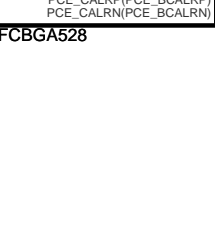
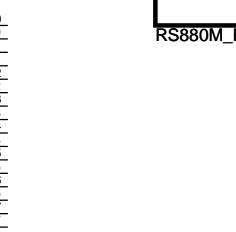
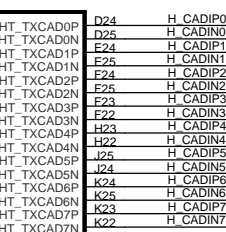
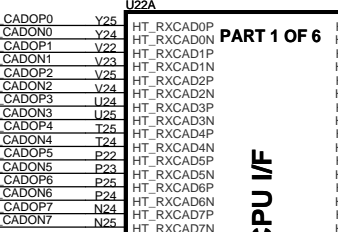
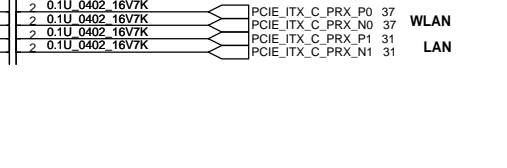
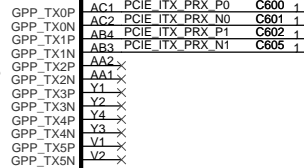
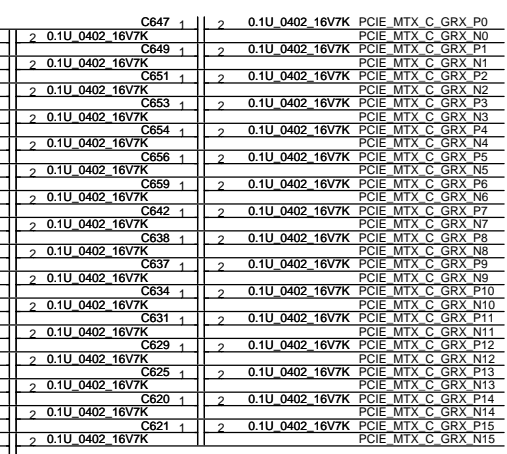
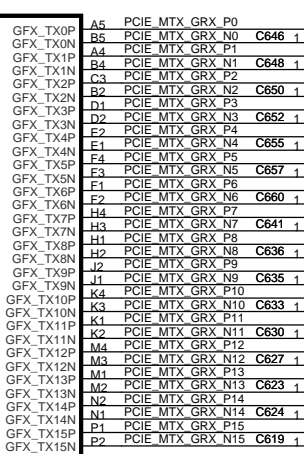
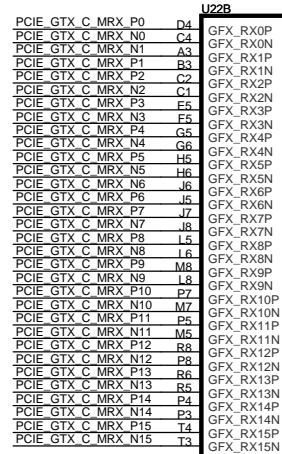
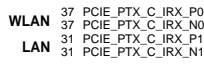
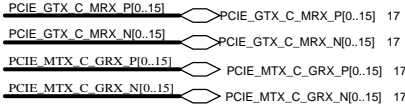
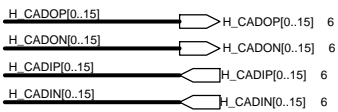


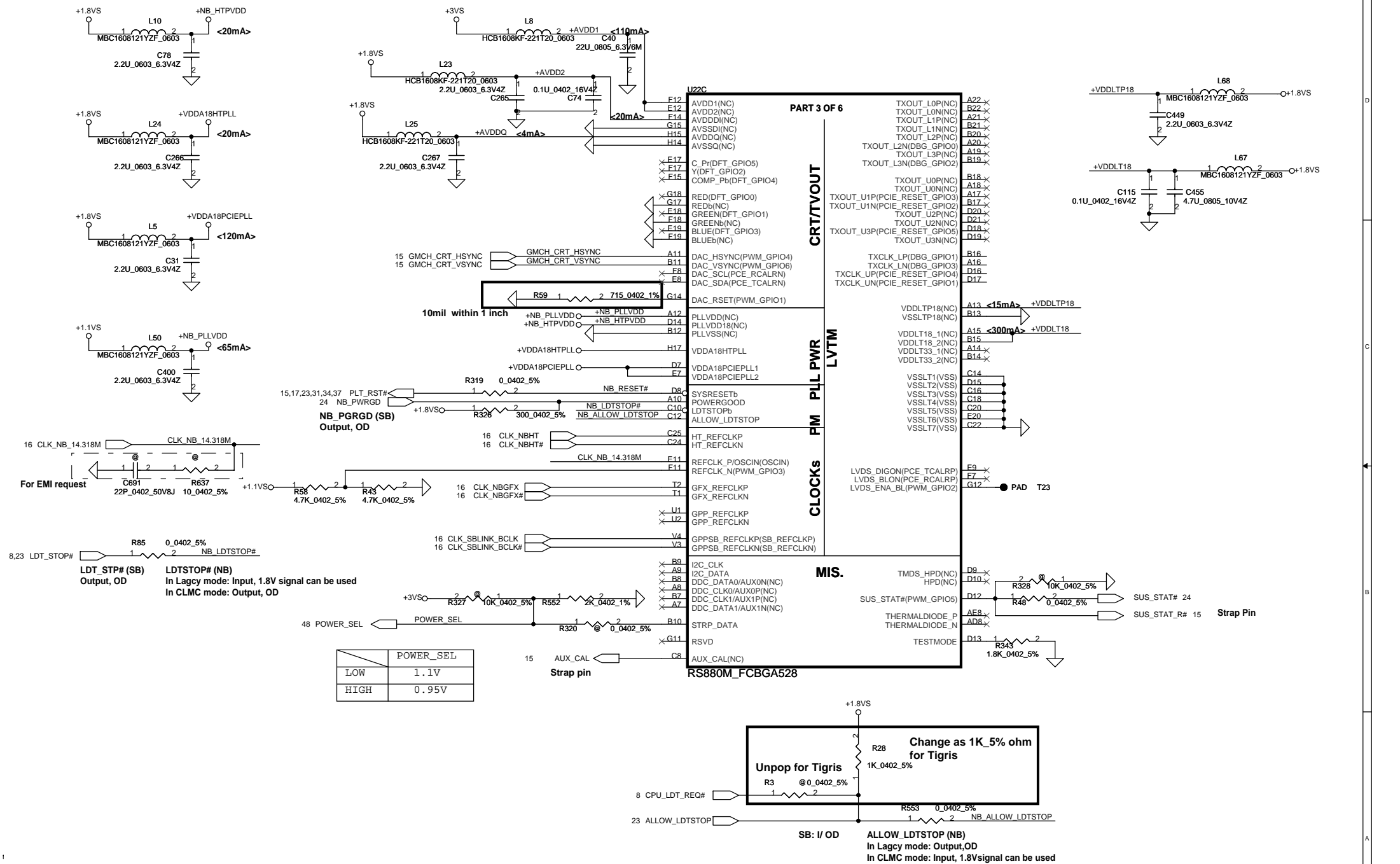
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								401836			
Date:				Thursday, March 18, 2010				Sheet		9 of 55	

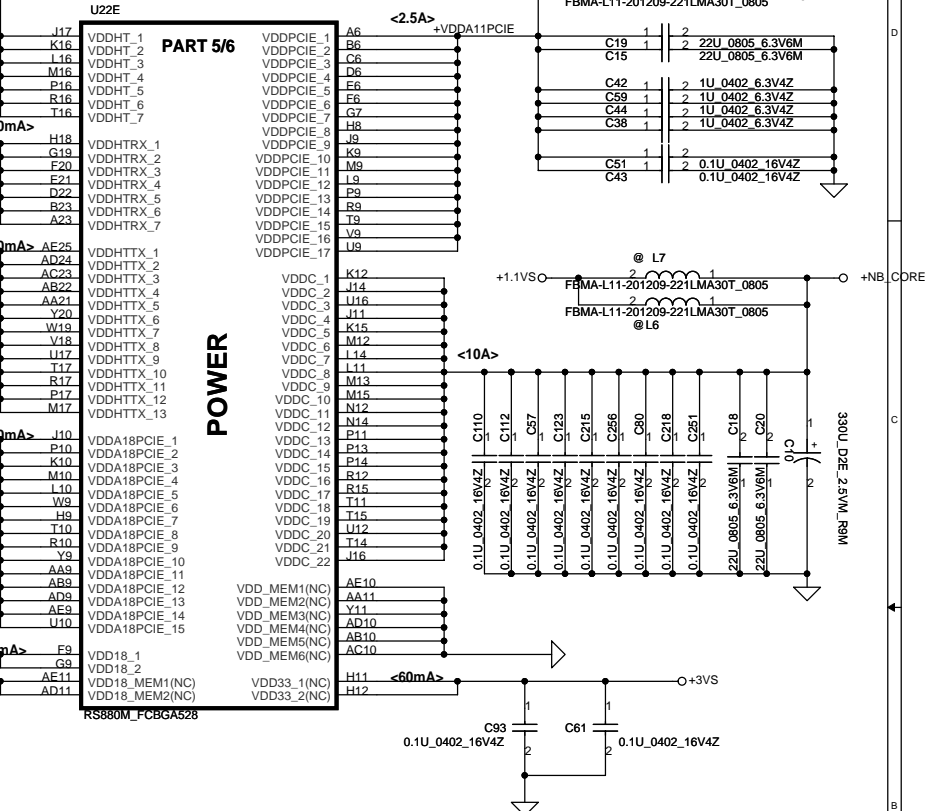
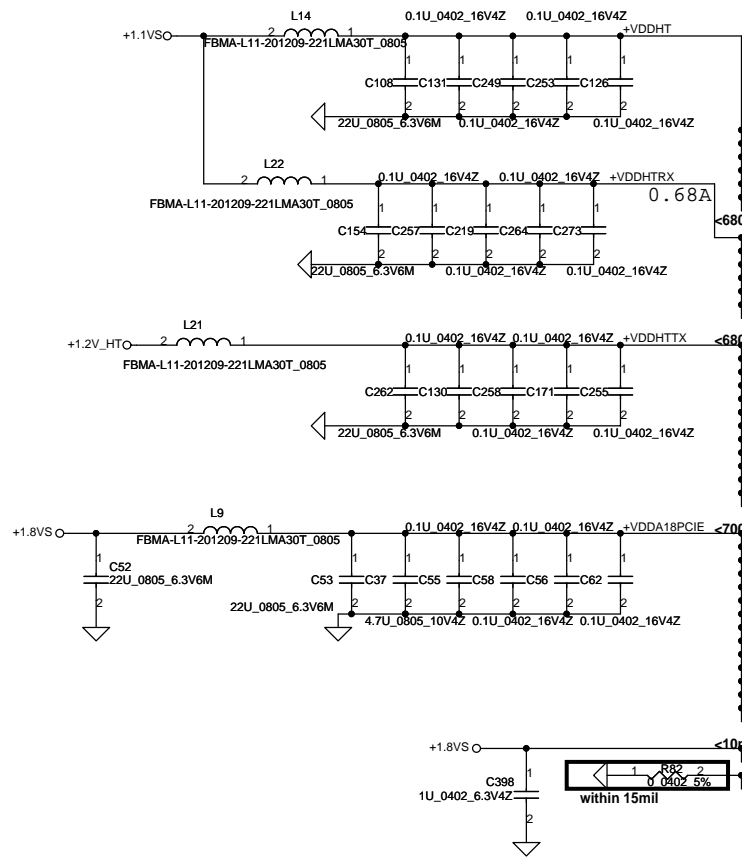
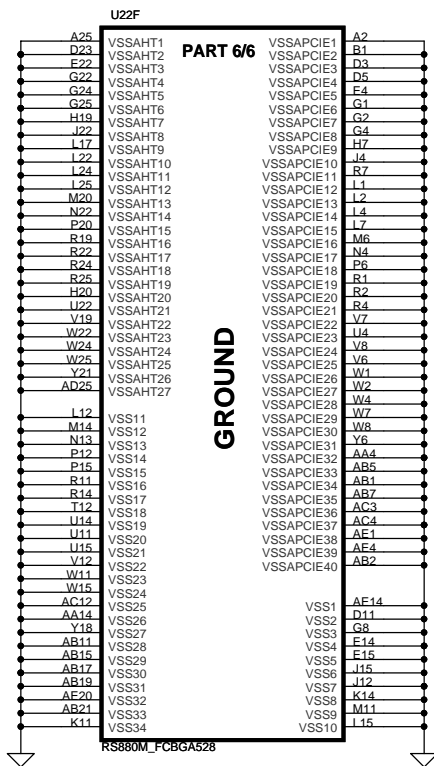


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Rev C	Doc 401836	Date Thursday, March 18, 2010	
Rev C	Doc 401836	Sheet 10	of 55

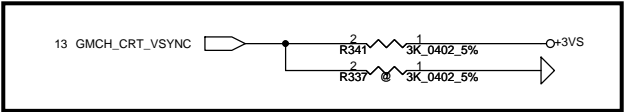






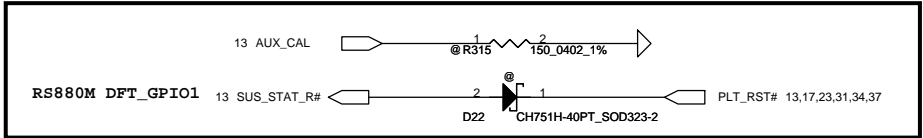


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				401836	
Date: Thursday, March 18, 2010		Sheet 14		of 55	



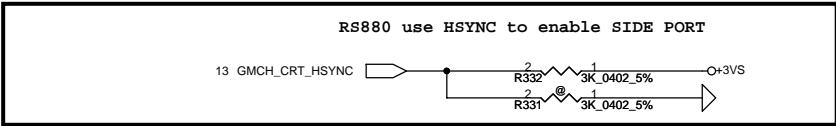
DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLED

Enables the Test Debug Bus using GPIO. (VSYNC)
1 : Disable (RS880)
0 : Enable (Rs880)



DFT_GPIO1: LOAD_EEPROM_STRAPS

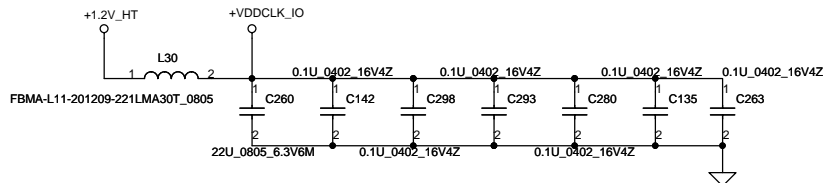
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RS740/RX780/RS880M: DFT_GPIO1 RS880M:SUS_STAT



RS880 use HSYNC to enable SIDE PORT

RS740/RS780/RS880M: Enables Side port memory (RS880M use HSYNC#)
0. Enable (RS880M)
1 : Disable(RS880M)

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				Date	Thursday, March 18, 2010
				Sheet	15 of 55



SEL_27M	1	configure as 27M and 27M_SS output
	0	configure as SRC_7 output

27M_SEL	1 *	configure as 27M and 27M_SS output
	0	configure as SRC_7 output

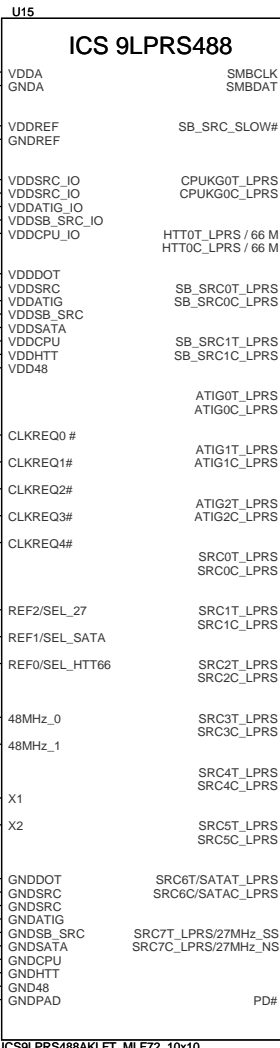
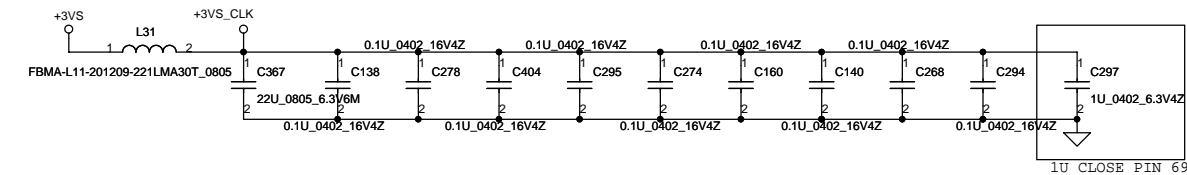
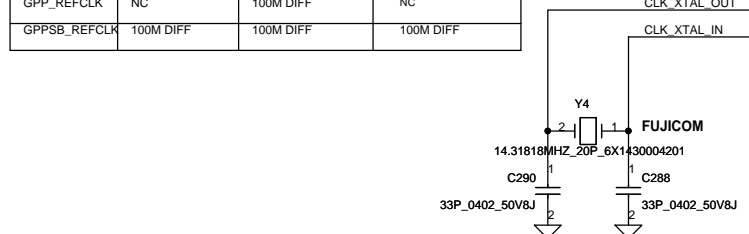
SEL_HTT66	1	configure as single-ended 66MHz output
	0 *	configure as differential 100MHz output
SEL_SATA	1 *	SS 100M SATA SRC6 output
	0	SS 100M SATA SRC6 output

LAN request
MiniCard1 request

External 14MHz CLK
for SB710

NB CLOCK INPUT TABLE

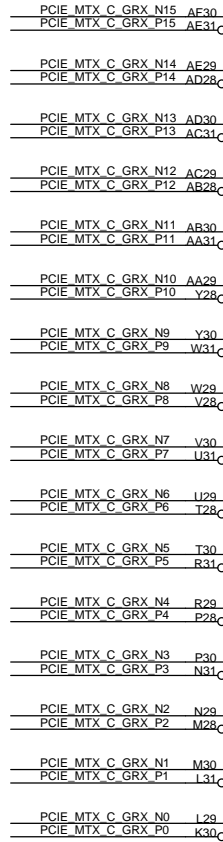
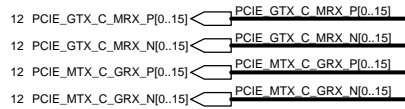
NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC
GPSPB_REFCLK	100M DIFF	100M DIFF	100M DIFF



Main--SLG8SP626VTR-SA00001Z310
Second--ICS9LPRS488CKLFT-SA000023H10

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						Size		Document Number		Rev C	
						Custom		401836			
						Date:		Thursday, March 18, 2010		Sheet 16 of 55	

PCIE LANE REVERSAL



U88A

PCIE_RX0P
PCIE_RX0NPCIE_RX1P
PCIE_RX1NPCIE_RX2P
PCIE_RX2NPCIE_RX3P
PCIE_RX3NPCIE_RX4P
PCIE_RX4NPCIE_RX5P
PCIE_RX5NPCIE_RX6P
PCIE_RX6NPCIE_RX7P
PCIE_RX7NPCIE_RX8P
PCIE_RX8NPCIE_RX9P
PCIE_RX9NPCIE_RX10P
PCIE_RX10NPCIE_RX11P
PCIE_RX11NPCIE_RX12P
PCIE_RX12NPCIE_RX13P
PCIE_RX13NPCIE_RX14P
PCIE_RX14NPCIE_RX15P
PCIE_RX15N

PCI EXPRESS INTERFACE

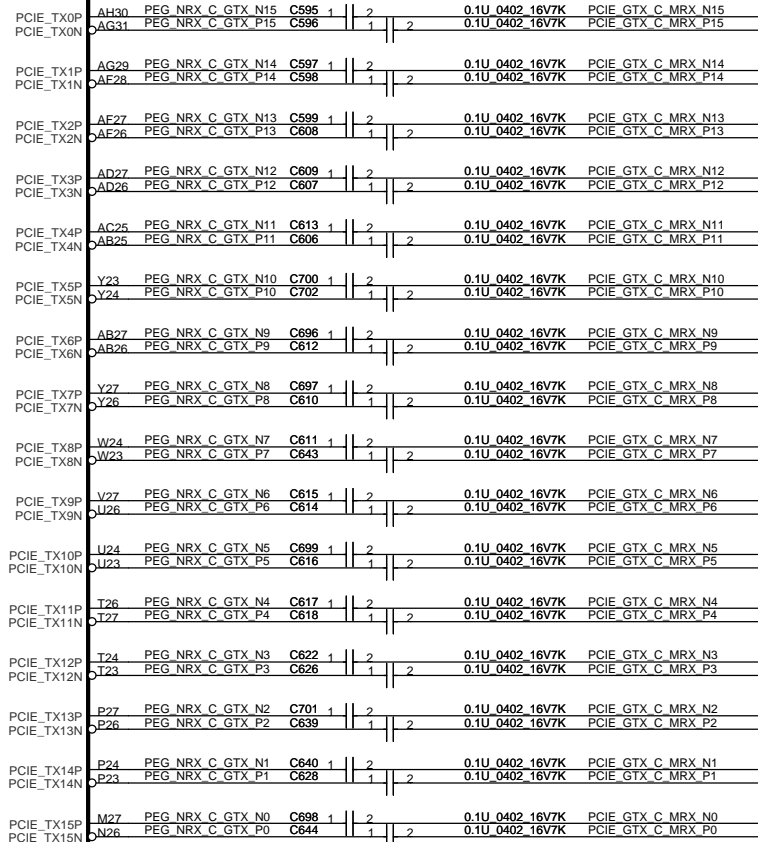
CLOCK

PCIE_REFCLKP
PCIE_REFCLKNNC#1
NC#2
NC_PWRGOOD

PERSTB

216-0728018 A12 M92-S2 XT FCBGA 0FA

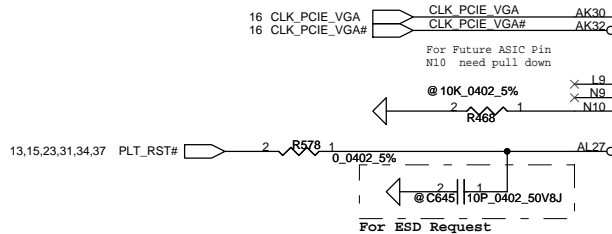
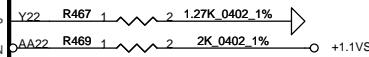
PCIE LANE REVERSAL



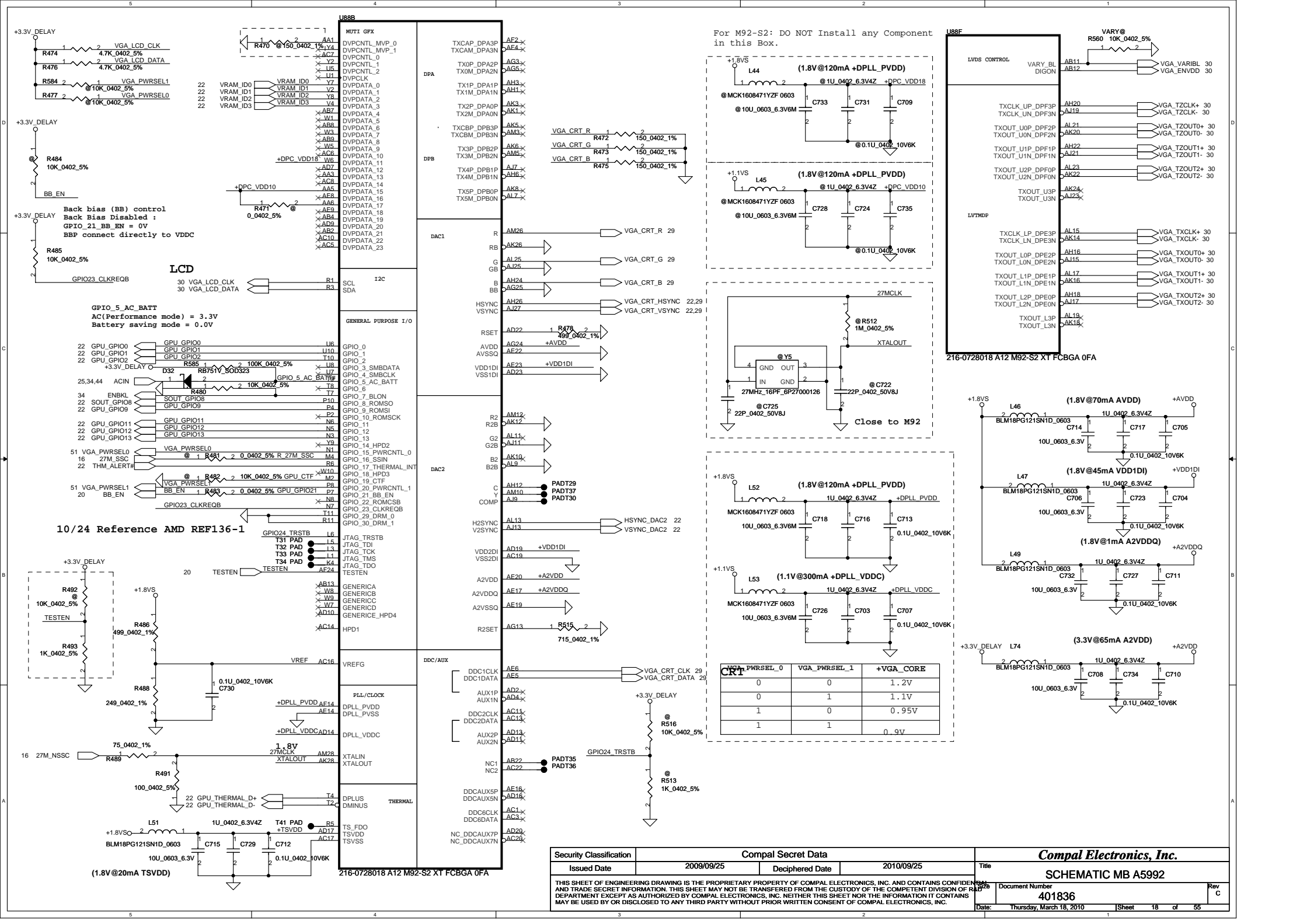
CALIBRATION

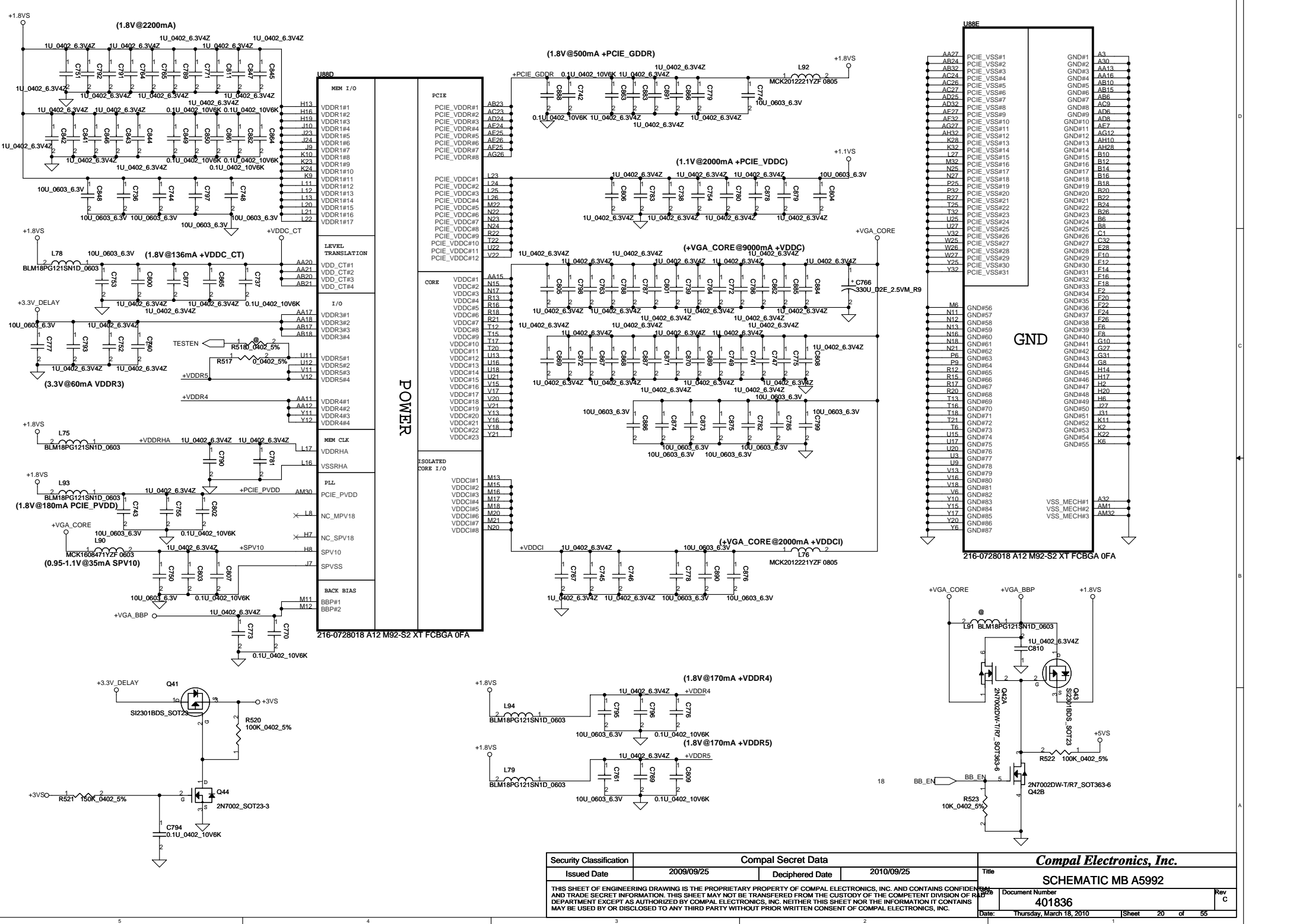
PCIE_CALRP

PCIE_CALRN



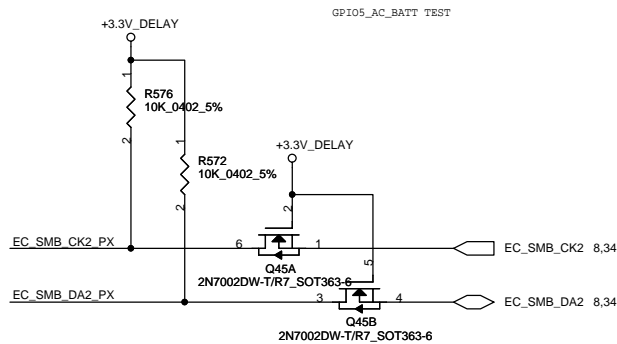
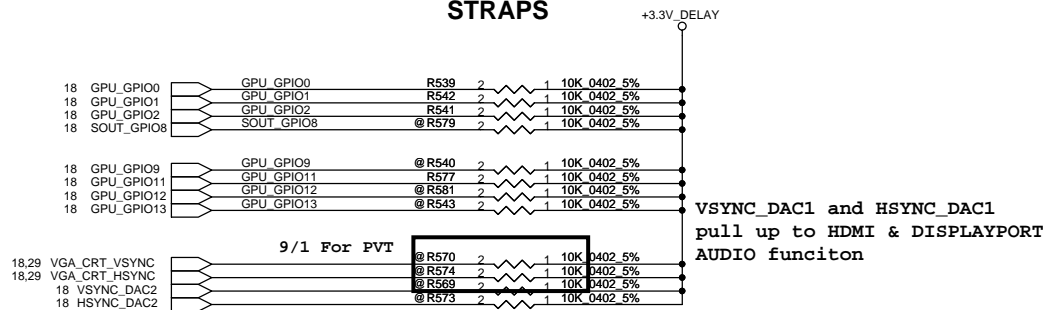
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				Date	Thursday, March 18, 2010
				Sheet	17 of 55



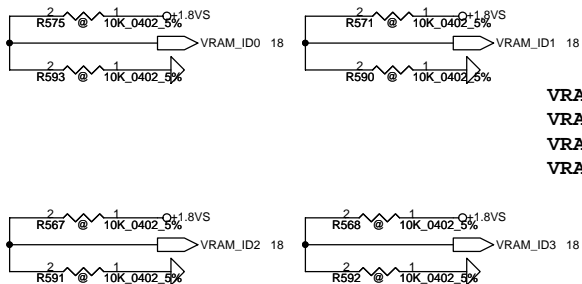
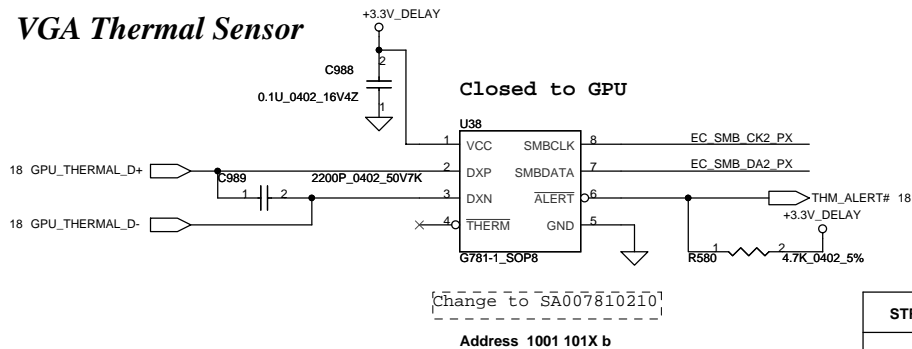


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Date:		Thursday, March 18, 2010		Sheet		20		of		55	

STRAPS



VGA Thermal Sensor



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	1
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
BIF_RX_PLL_CALIB_BP	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB		1
ROMIDCFG(2:0)	GPIO[13:11]	BIF_RX_PLL_CALIB_BP	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	ENABLE EXTERNAL BIOS ROM	0
SMS_EN_HARD	H2SYNC	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0
CCBPASS	GENERICC	IGNORE VIP DEVICE STRAPS	0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	X X

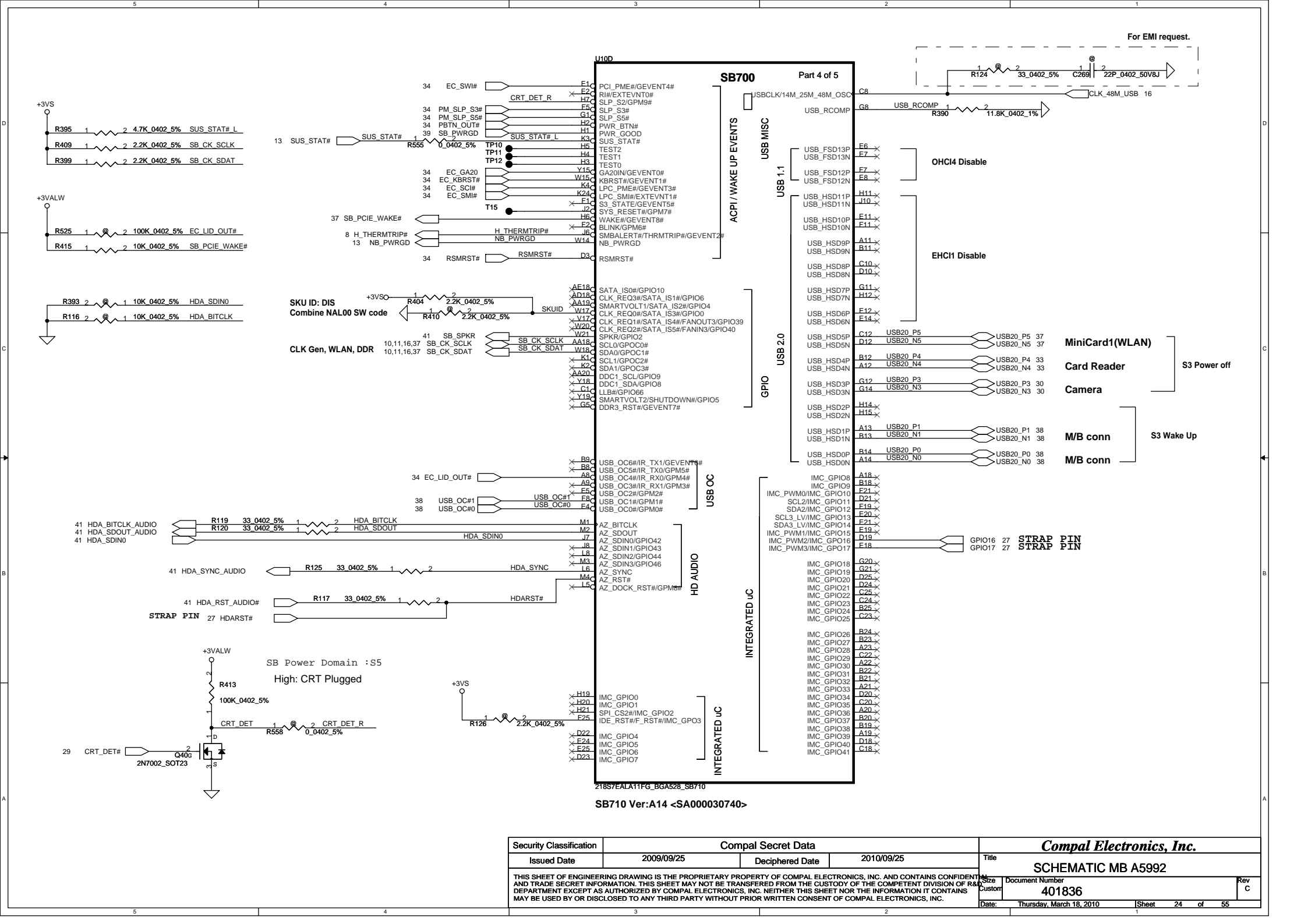
AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC	GENERICC
<p>PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET</p>	
GPIO_28_TDO	GPIO21_BB_EN

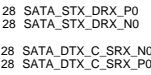
STRAPS	PIN	GPU	Project	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 3,2,1,0
VRAM_ID[3:0]	DVPDATA (3,2,1,0)	M92 S2-XT		512MB(x4)	Hynix 64Mx16 1.8V	SA00002UH20	0 0 0 1
				512MB(x4)	ATI 64Mx16 1.8V	SA00003LT10	0 0 1 0
				512MB(x4)	Samsung 64Mx16 1.8V (E-die)	SA00003IO10	0 1 0 0

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					401836	C
				Date:	Thursday, March 18, 2010	Sheet 22 of 55

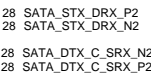


Port Number	Pri/SEC,Mas/Slave assignment	SATA drive controlled by
Port 0	Primary master	SATA controller
Port 2	Primary slave	SATA controller
Port 3	Secondary slave	SATA controller

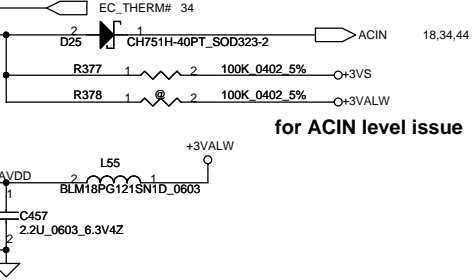
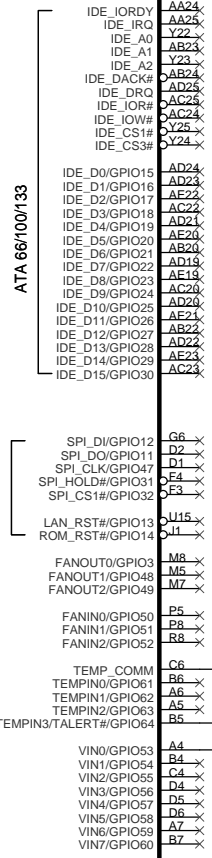
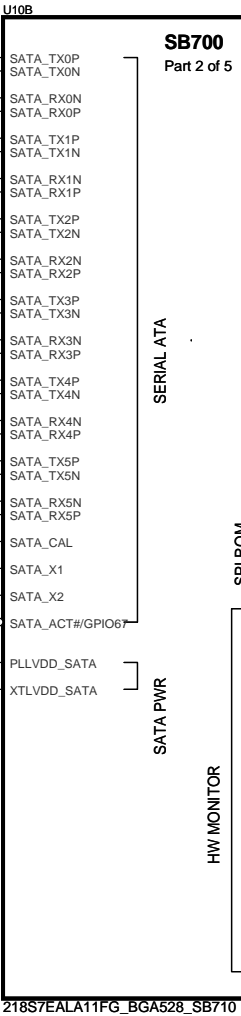
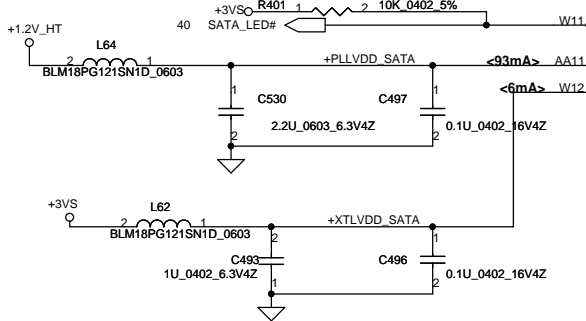
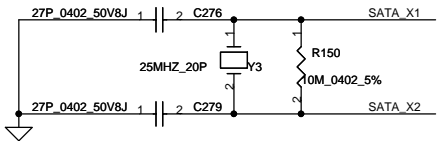
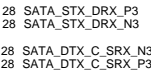
Main
HDD



Main
ODD



2nd
ODD

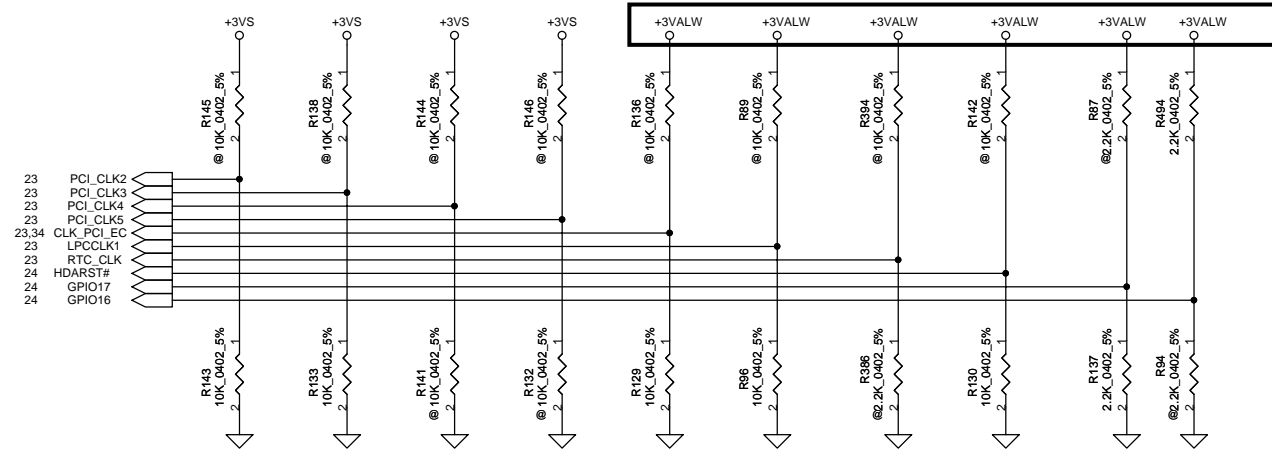


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				Date	Thursday, March 18, 2010
				Sheet	25 of 55

REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

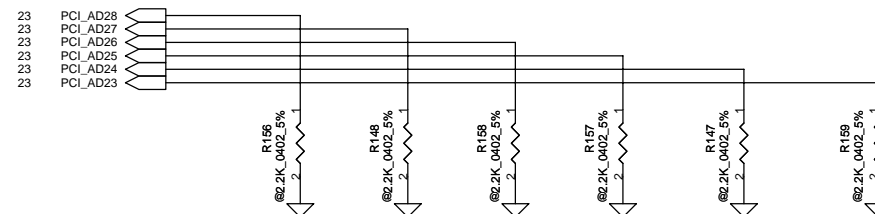
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	L,H = LPC ROM (Default L,NC) L,L = FWH ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		



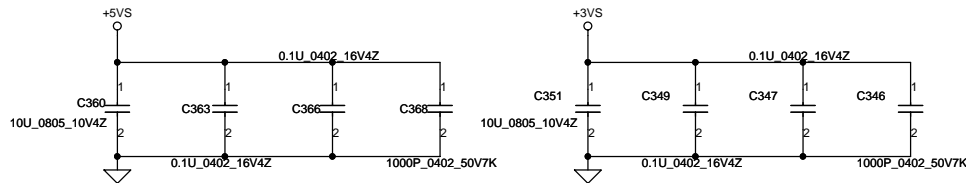
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

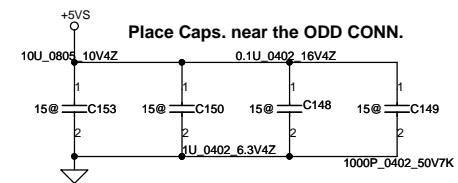
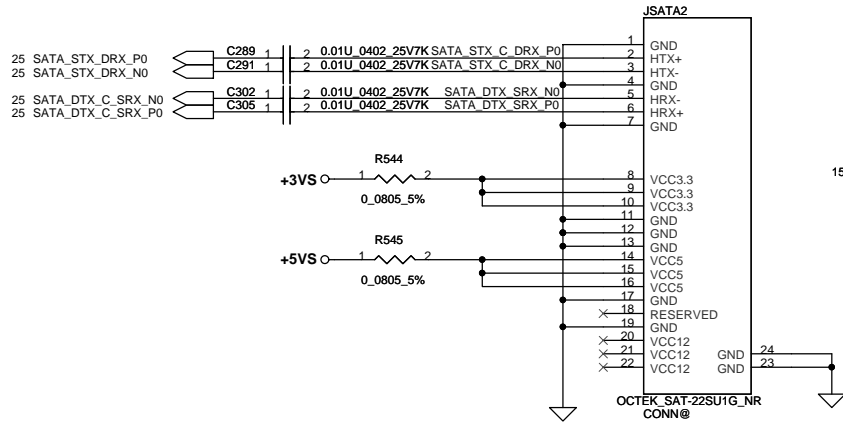
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



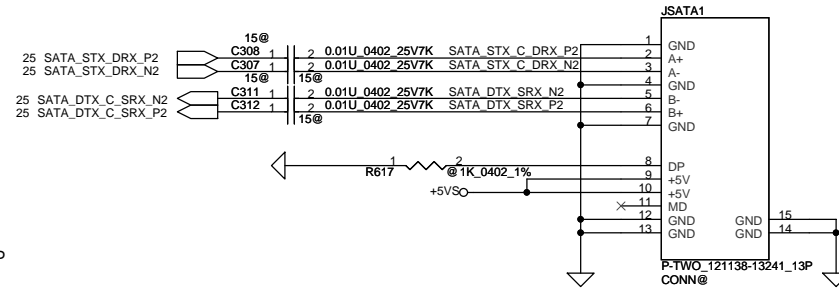
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				Date	Thursday, March 18, 2010
				Sheet	27 of 55



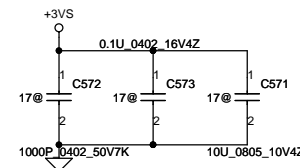
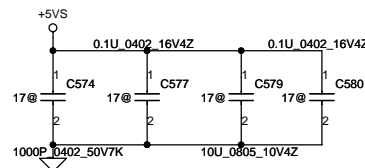
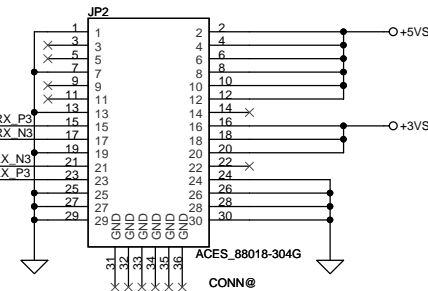
SATA HDD CONN



SATA ODD CONN

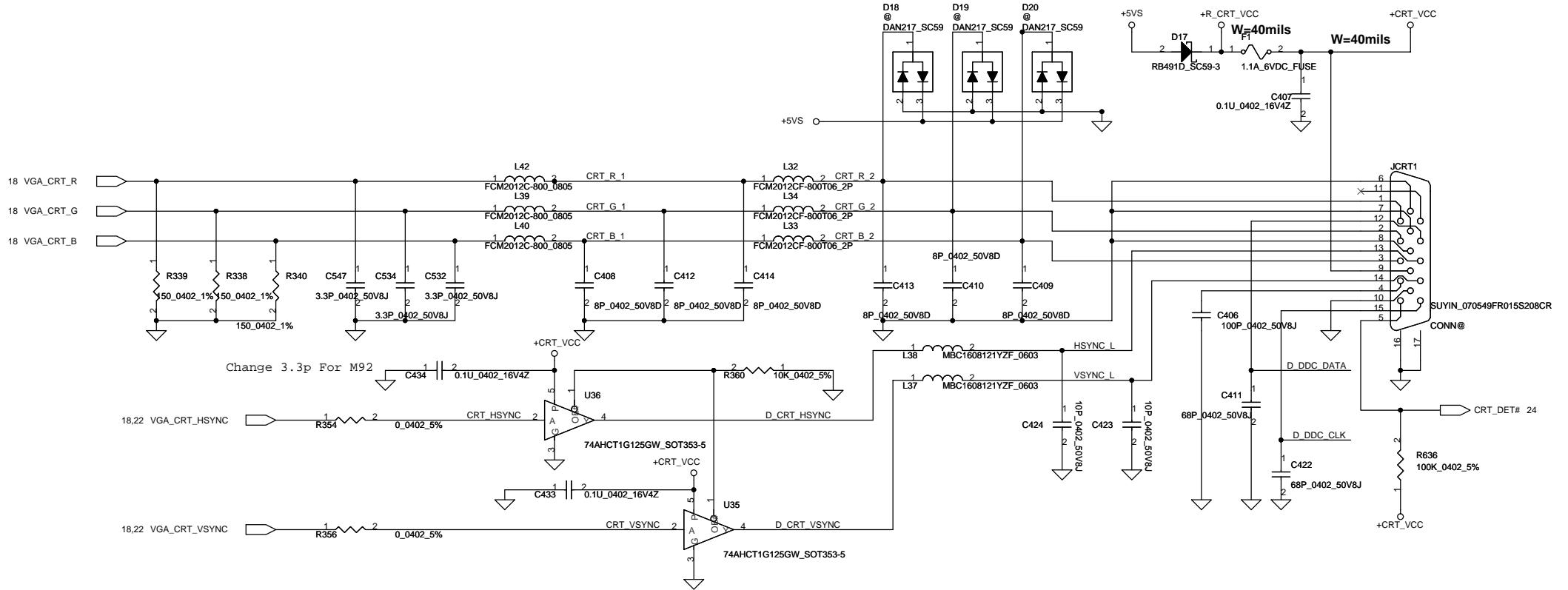


Second ODD

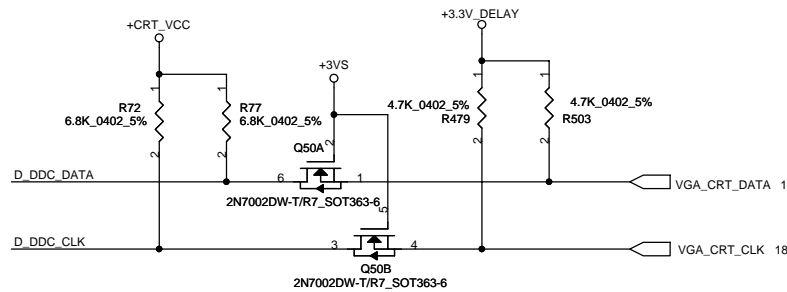


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				Date	Thursday, March 18, 2010
				Sheet	28 of 55

CRT Connector



Close to Conn side

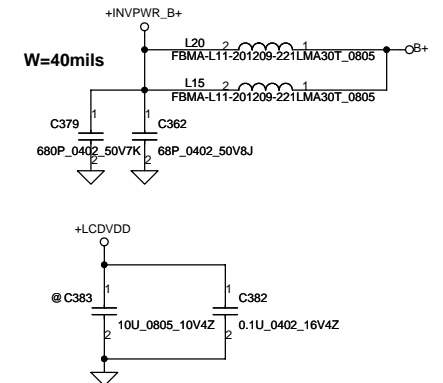
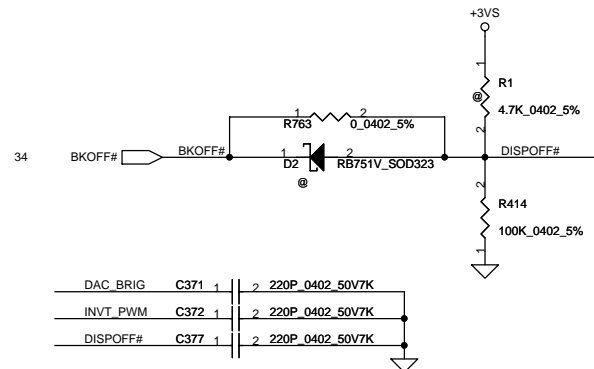


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				Date	Thursday, March 18, 2010
				Sheet	29 of 55

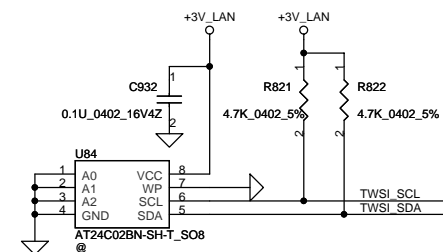
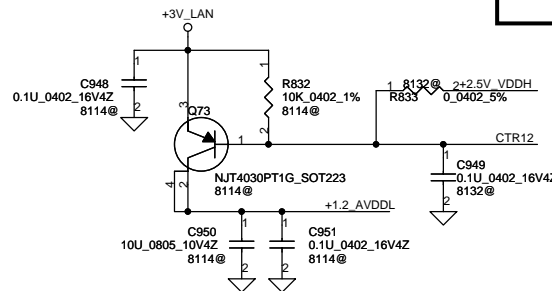
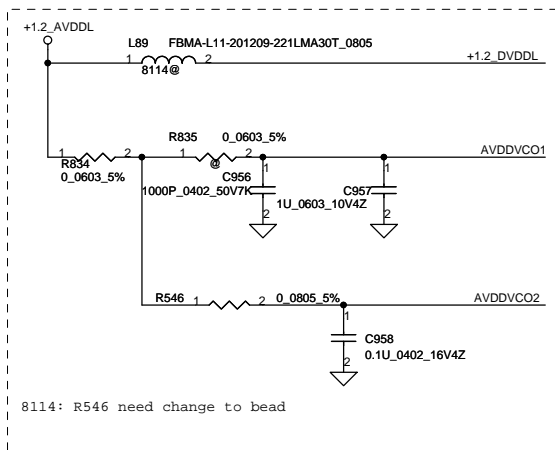
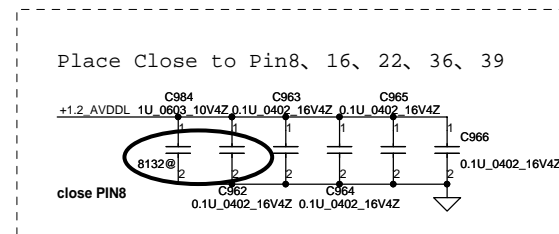
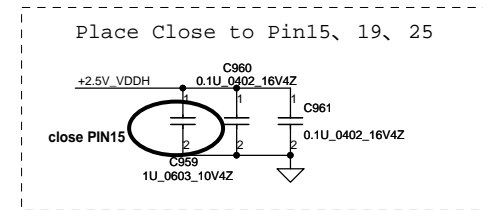
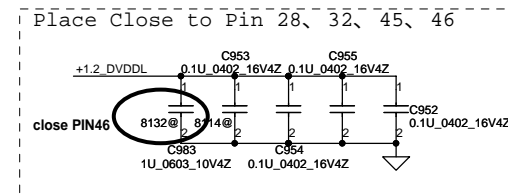
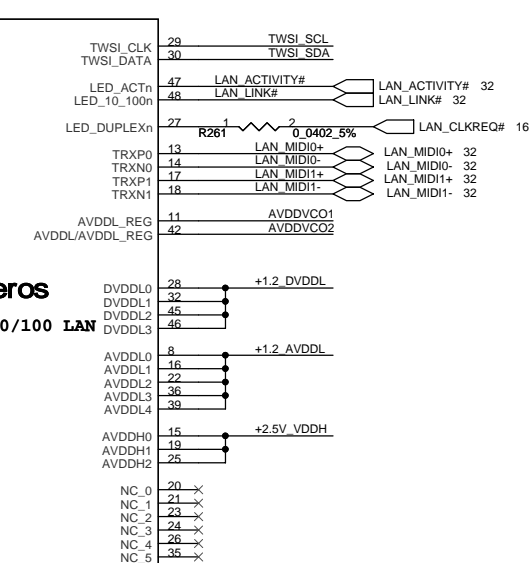
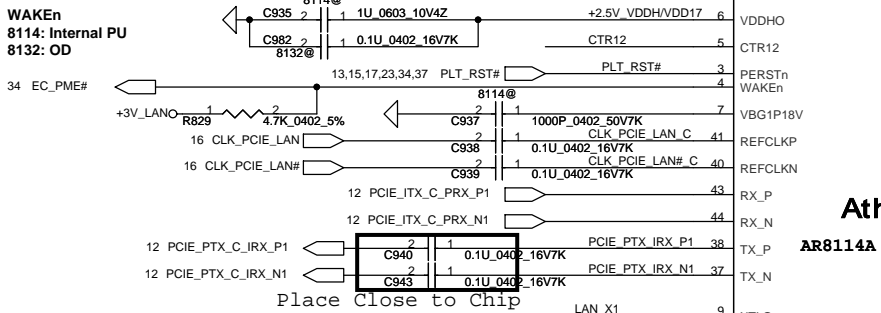
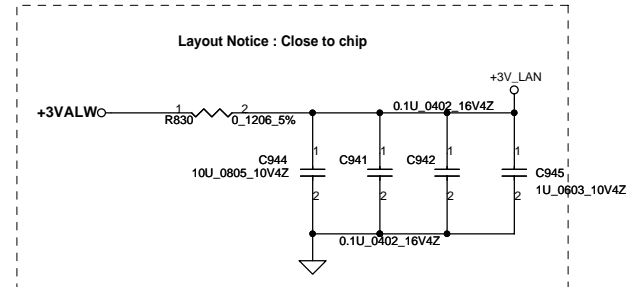
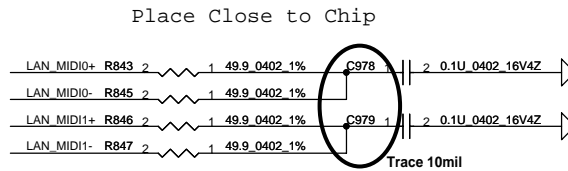
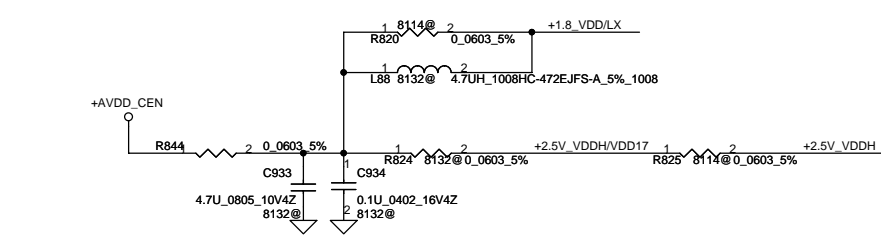
LCD POWER CIRCUIT

The schematic diagram illustrates the power and control circuitry for an LCD. Key components and connections include:

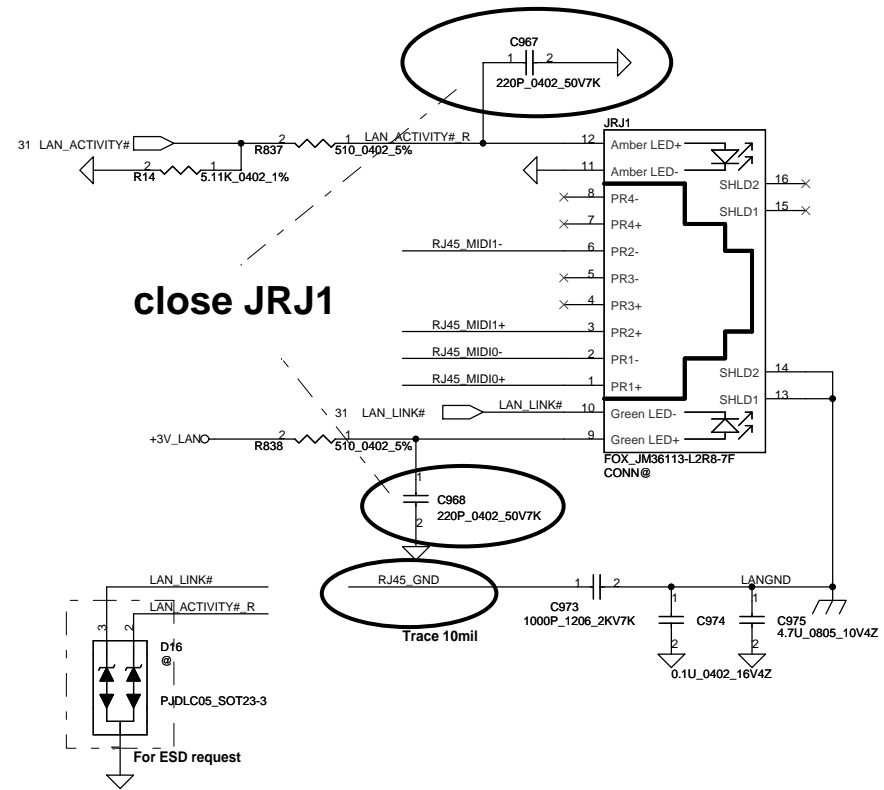
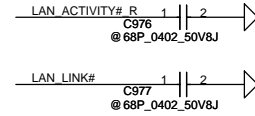
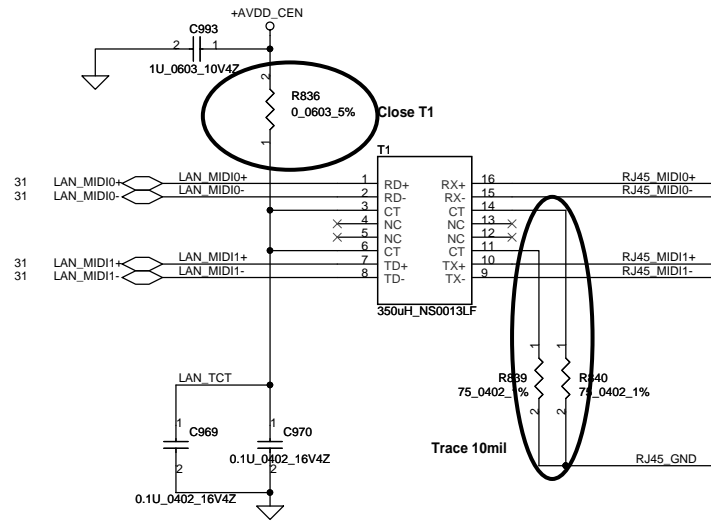
- Power Rails:** +3VS, +LCDVDD, +3VALW, +LCDVDD, +LCDVDD.
- Resistors:** R347 (100K_0402_5%), R274 (150_0603_5%), R348 (510_0402_5%), R278 (100K_0402_5%), R345 (100K_0402_5%), R764 (0_0402_5%), R561 (VARY@ 0_0402_5%).
- Capacitors:** C77 (@ 4.7U_0805_10V4Z), C431 (0.047U_0402_16V7K), C415 (4.7U_0805_10V4Z), C420 (0.1U_0402_16V4Z).
- Transistors:** Q22A (2N7002DW-T/RT_SOT363-6), Q23 (AO3413_SOT23-3), B2C0 (2N7002DW-T/RT_SOT363-6).
- Signals:** 18 VGA_ENVDD, 34 EC_INVT_PWM, 18 VGA_VARIBL, INVT_PWM.
- Dimensions:** W=60mils (twice).

[illegible]

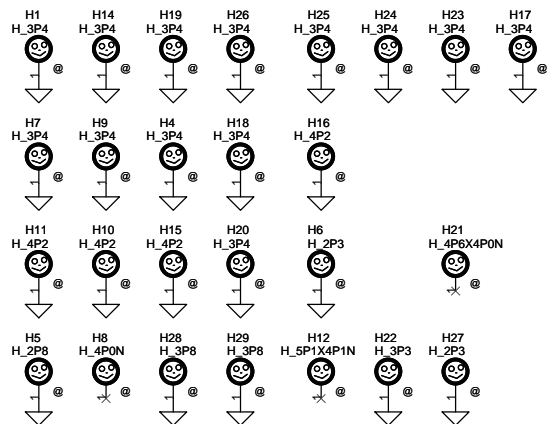
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				Custom	401836	C
				Date:	Thursday, March 18, 2010	Sheet 30 of 55



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				Date	Thursday, March 18, 2010
				Sheet	31 of 55



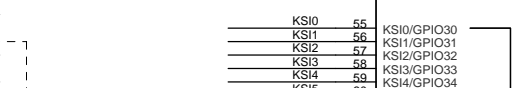
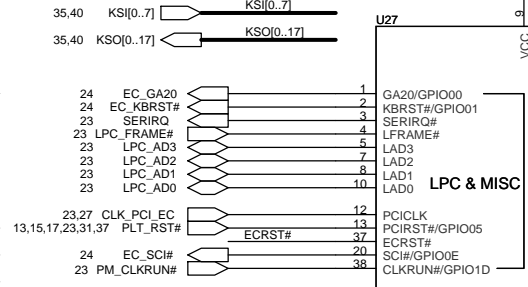
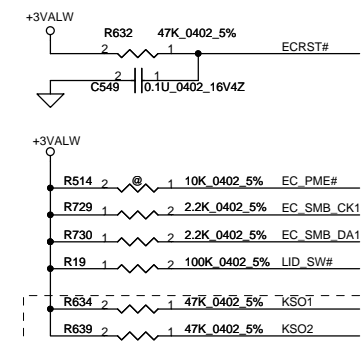
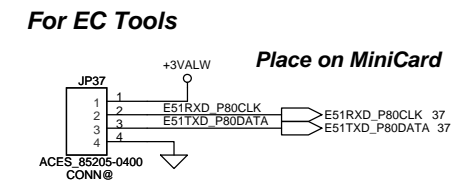
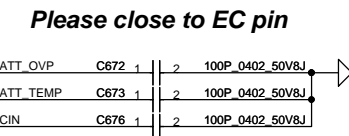
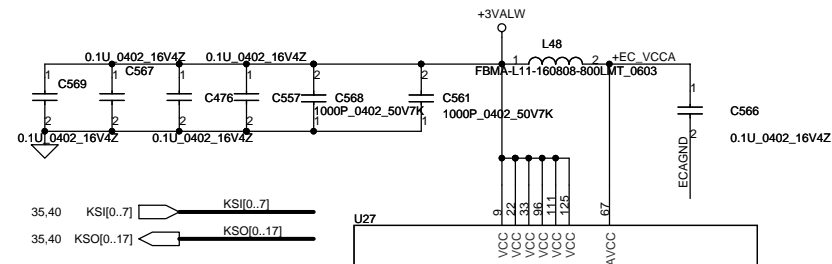
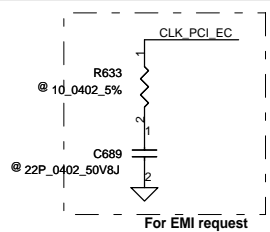
Screw Hole



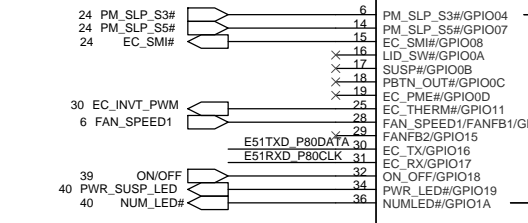
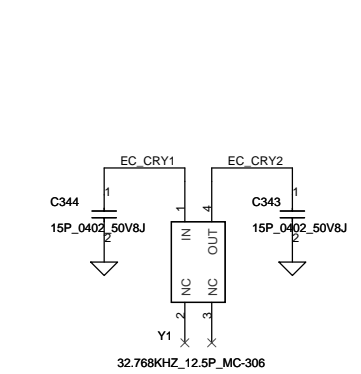
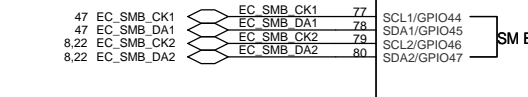
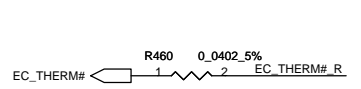
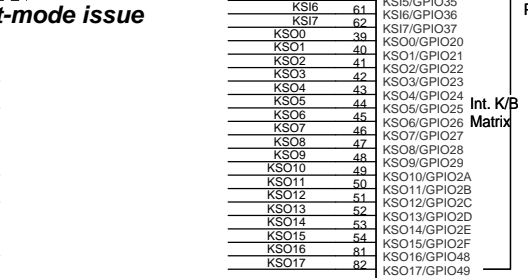
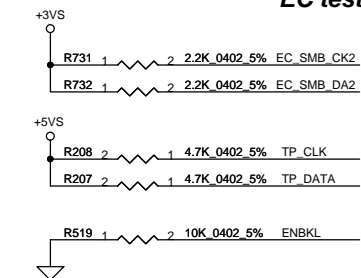
PCB Federal Mark PAD



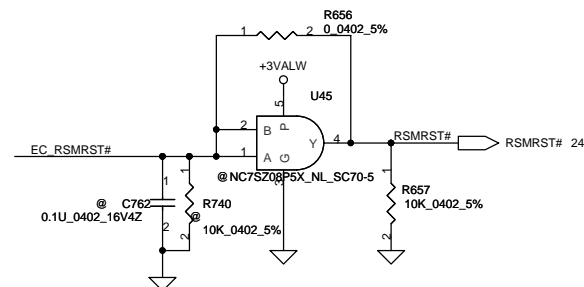
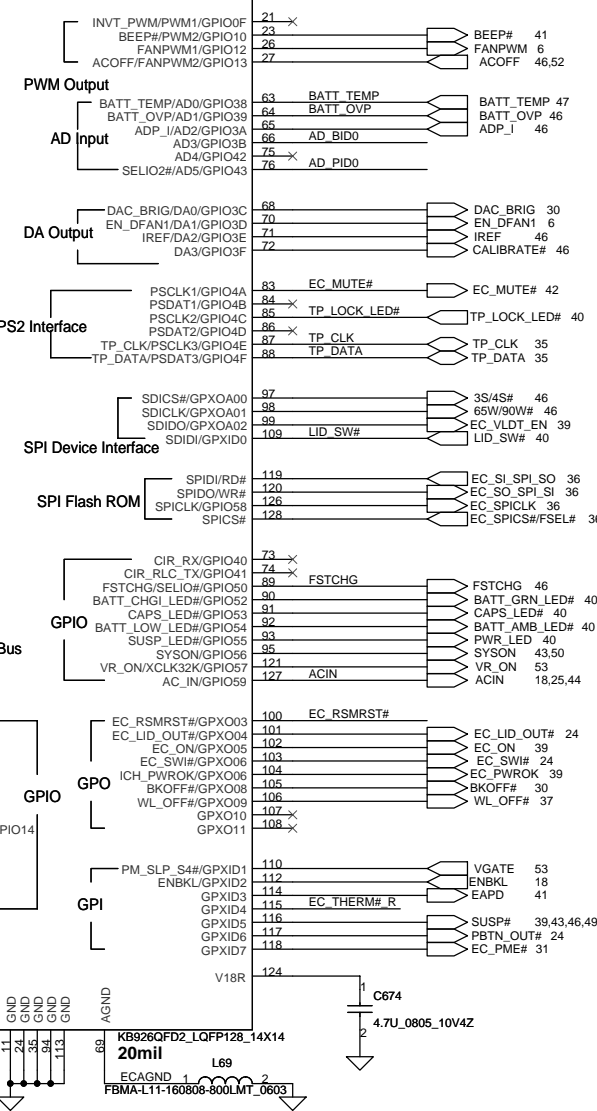
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Issued Date	2009/09/25	Deciphered Date	2010/09/25	Title	SCHEMATIC MB A5992
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				Date	Thursday, March 18, 2010
				Sheet	32 of 55



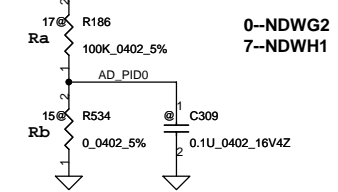
EC test-mode issue



Chagne to D3 version

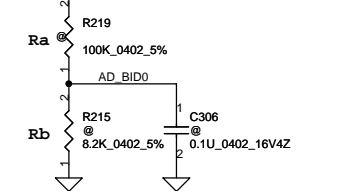


Project ID
Please see page 3.



0--NDWG2
7--NDWH1

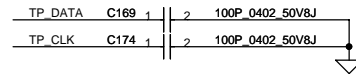
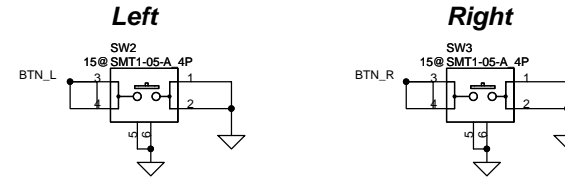
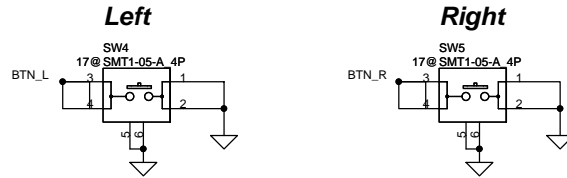
Board ID <VB support>
Please see page 3.



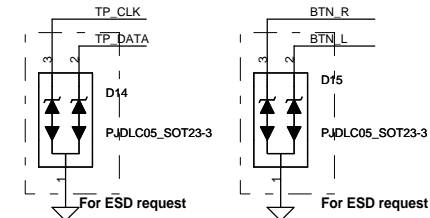
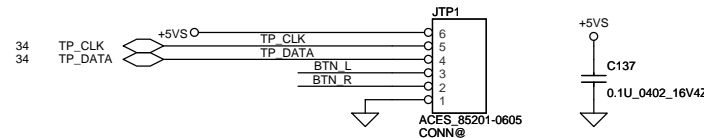
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				Rev	C
				Date	Thursday, March 18, 2010
				Sheet	34 of 55

For 17"

For 15"



TP/B Conn.

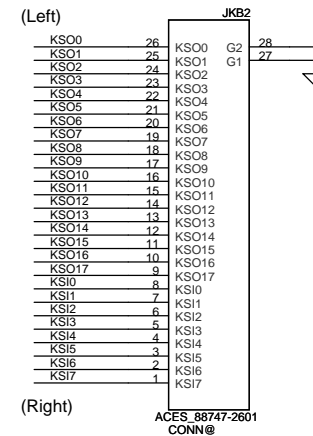
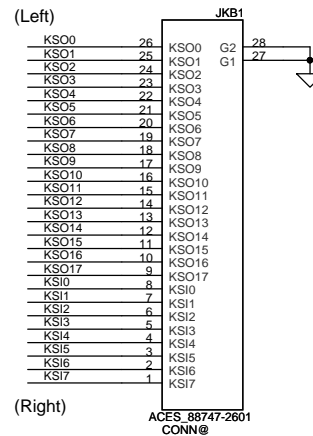
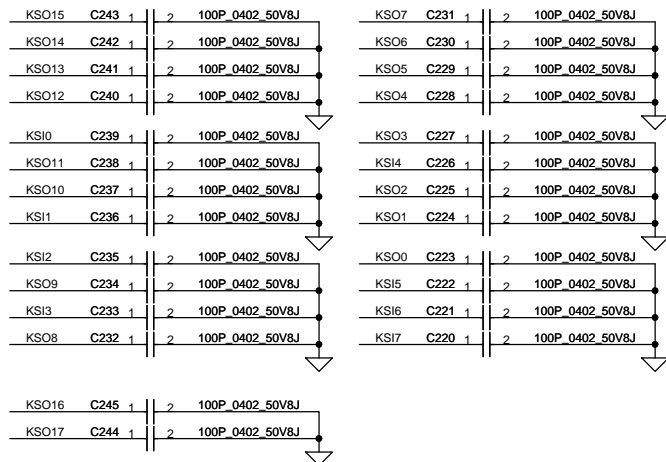


Change to SCA00000200



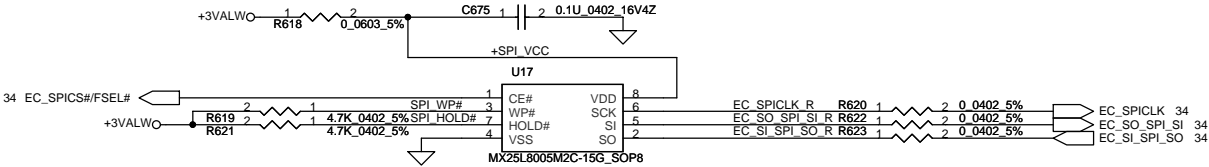
INT_KBD Conn.

KB1 for 15"
KB2 for 17"



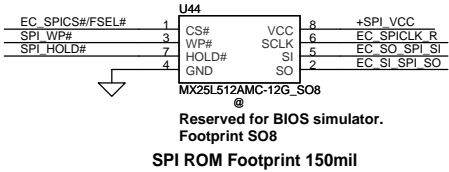
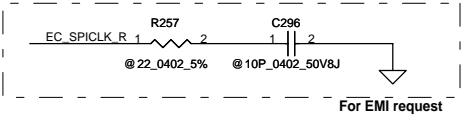
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Size Custom		Document Number 401836		Rev C
Date: Thursday, March 18, 2010		Sheet 35 of 55		

SPI Flash ROM 16M*1



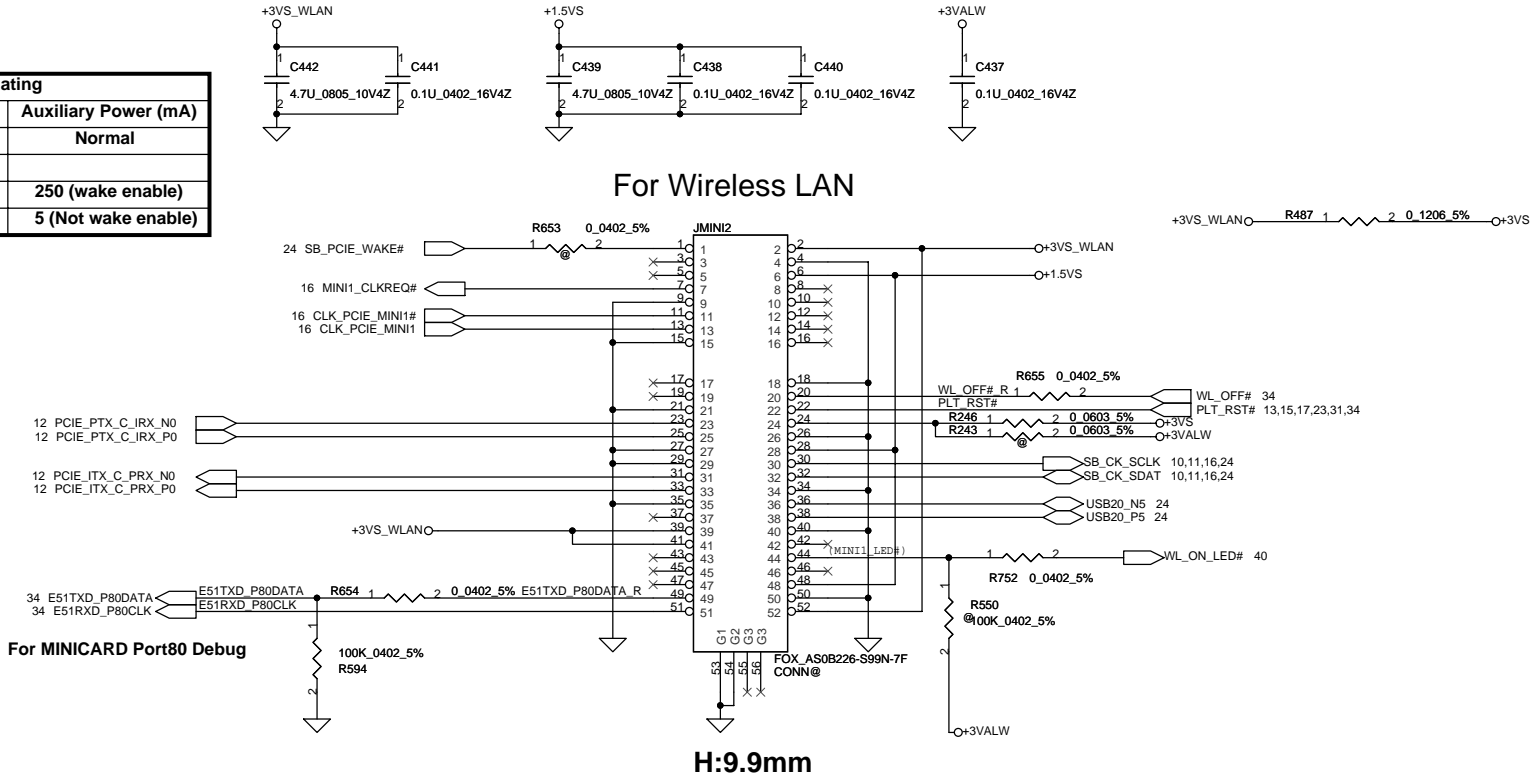
SA00000XT00 : S IC FL 8M MX25L8005M2C-15G SOP 8P
ENE suggestion SPI Frequency over 66MHz
SST: 50MHz
MXIC: 70MHz
ST: 40MHz

ONLY MXIC used in this project (66MHz)



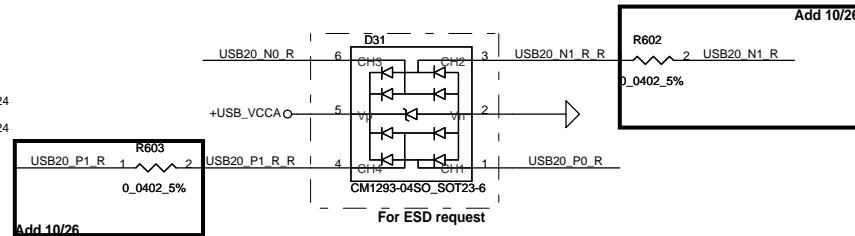
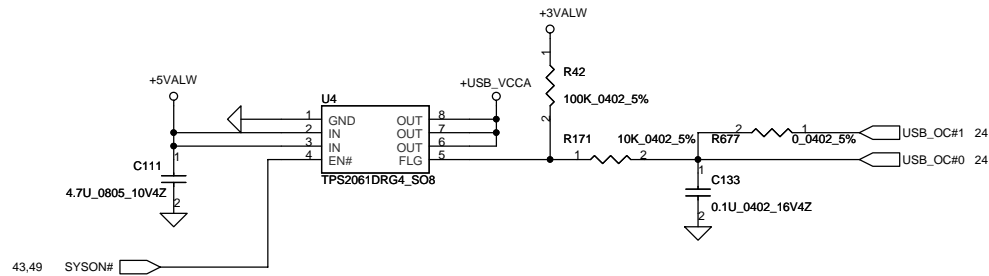
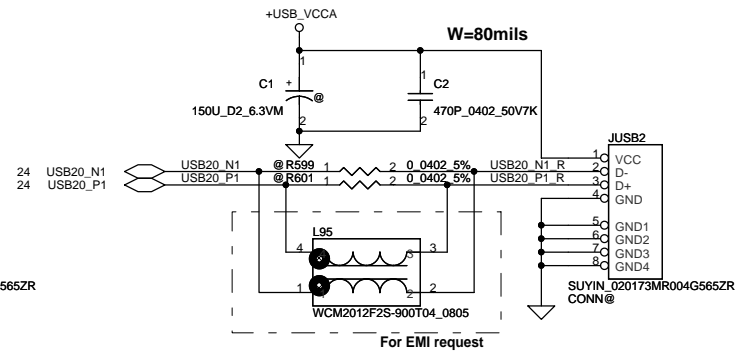
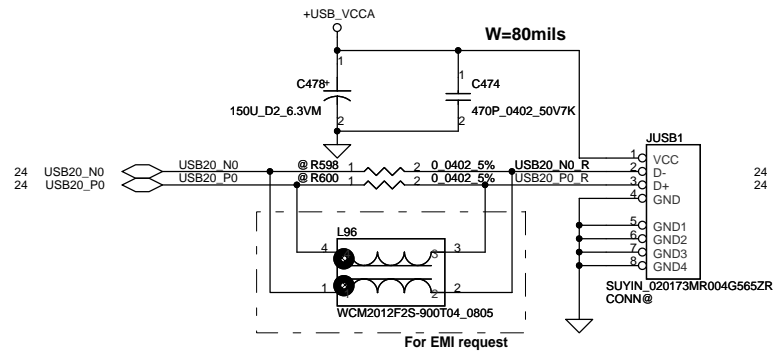
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				Date:	Thursday, March 18, 2010
				Sheet	36 of 55
				Rev	C

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



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				Custom	C
				Document Number	
				401836	
				Date:	Thursday, March 18, 2010
				Sheet	37 of 55

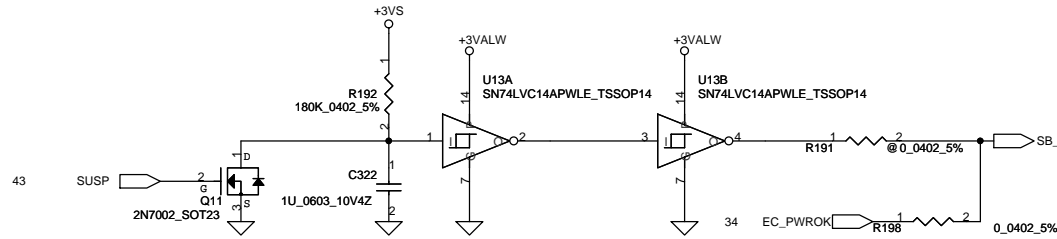
USB CONN. 1 & 2



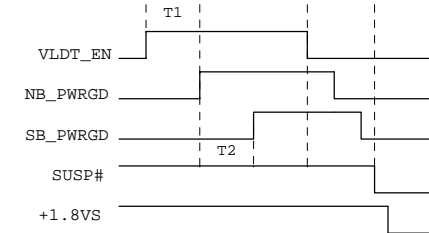
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Date		Thursday, March 18, 2010		Sheet	38 of 55

Power ON Circuit

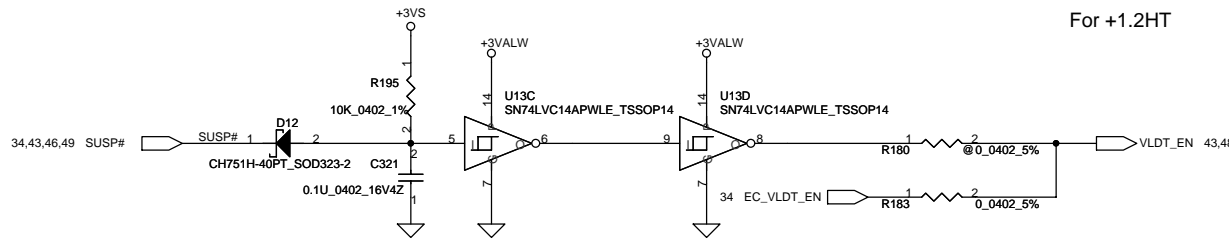
For South Bridge



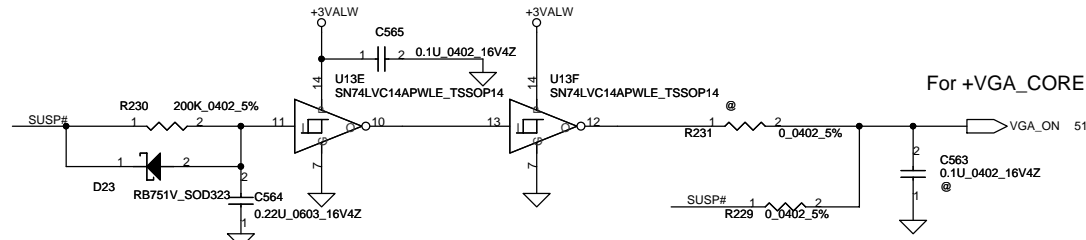
note: T1 minimum 15ms, T2 minimum 33ms/maximum 500ms, SUSP# goes to low after SB_PWRGD goes to low for power down.



For +1.2HT



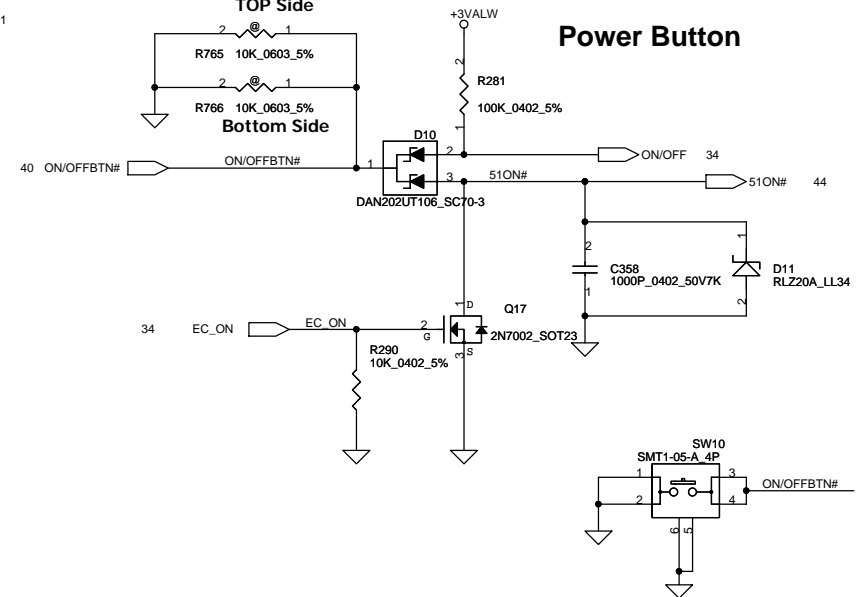
For +VGA_CORE



TOP Side

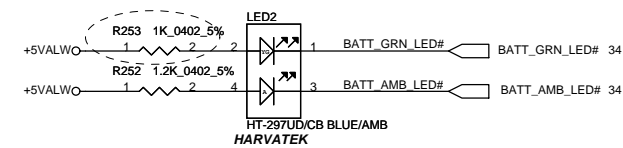
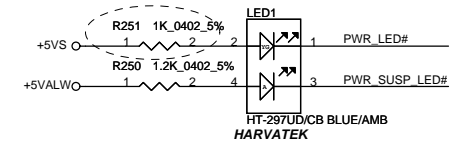
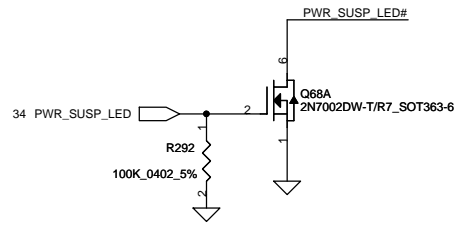
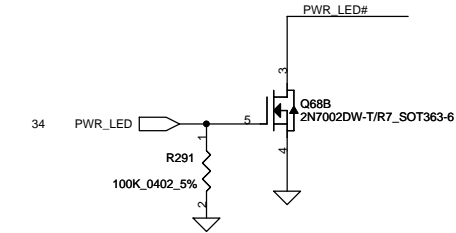
Bottom Side

Power Button

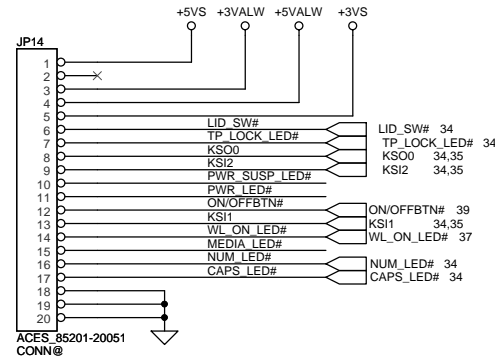


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Date	Thursday, March 18, 2010	Sheet	39	of	55

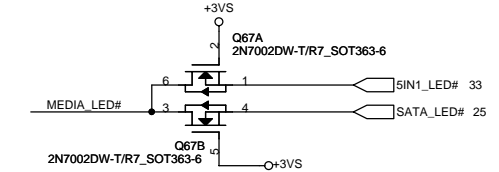
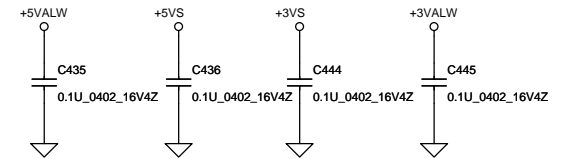
To PWR LED/B



BLUE/AMB LED

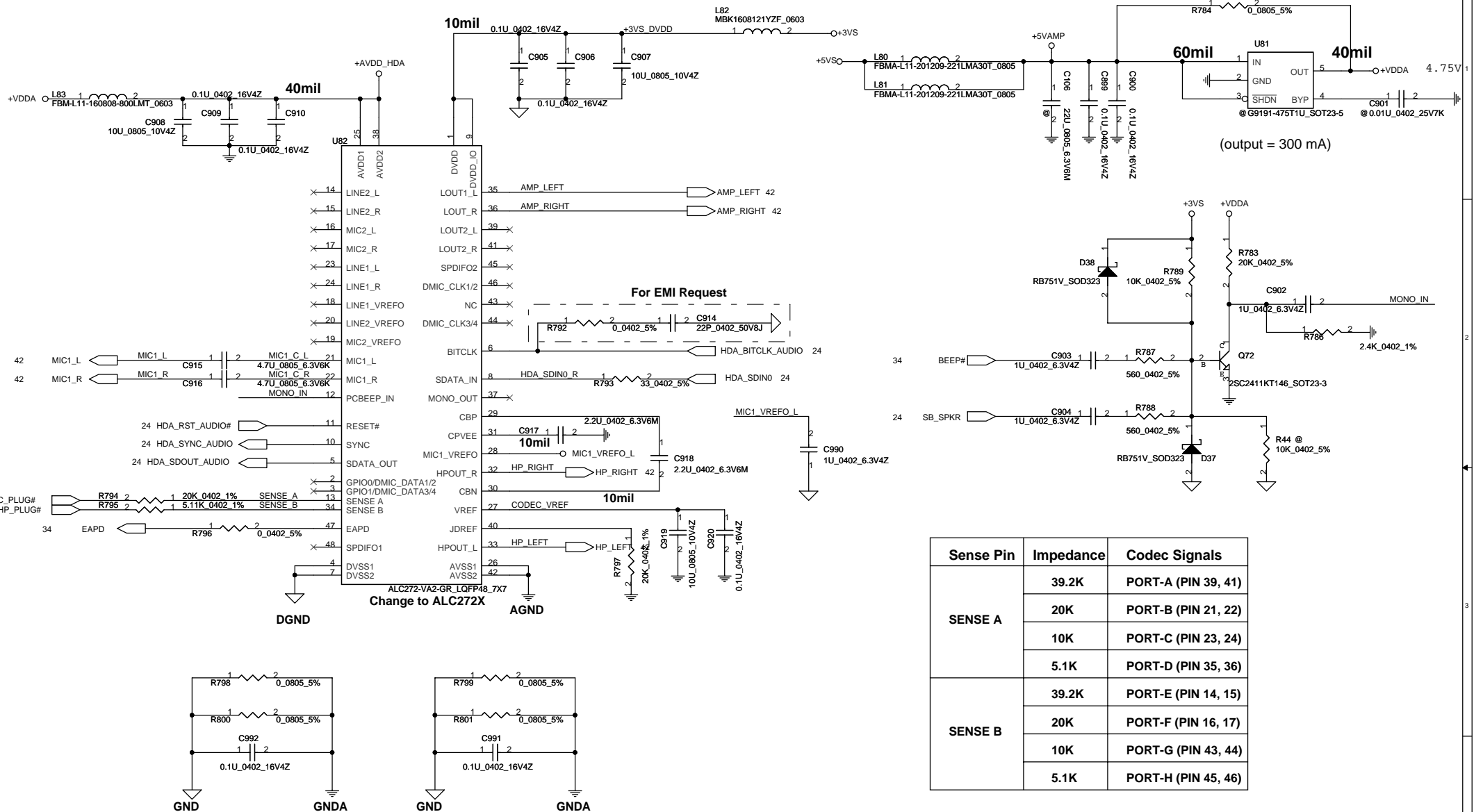


	KSO0
KSI1	WL_BTN#
KSI2	TP_LOCK_BTN#
KSI3	
KSI4	
KSI5	
KSI6	



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Date:		Thursday, March 18, 2010		Sheet 40 of 55
Document Number		401836		Rev C

HD Audio Codec



TPA6017 Medium Range Amplifier

Left Connector

Right Connector

LINE Out/Headphone Out

LINE IN/Ext.MIC JACK

(HDA Jack)

Security Classification

Compal Secret Data

Issued Date 2009/09/25 **Deciphered Date** 2010/09/25

Title SCHEMATIC MB A5992

Document Number 401836

Date Thursday, March 18, 2010 **Sheet** 42 of 55

Rev C

TPA6017 Medium Range Amplifier

Left Connector

Right Connector

LINE Out/Headphone Out

LINE IN/Ext.MIC JACK

(HDA Jack)

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				401836	C
Date: Thursday, March 18, 2010				Sheet	42 of 55

TPA6017 Medium Range Amplifier

Left Connector

Right Connector

LINE Out/Headphone Out

LINE IN/Ext.MIC JACK

(HDA Jack)

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				401836	C
Date: Thursday, March 18, 2010				Sheet	42 of 55

TPA6017 Medium Range Amplifier

Left Connector

Right Connector

LINE Out/Headphone Out

LINE IN/Ext.MIC JACK

(HDA Jack)

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				401836	C
Date: Thursday, March 18, 2010				Sheet	42 of 55

TPA6017 Medium Range Amplifier

Left Connector

Right Connector

LINE Out/Headphone Out

LINE IN/Ext.MIC JACK

(HDA Jack)

Security Classification

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Title SCHEMATIC MB A5992

Document Number 401836

Date Thursday, March 18, 2010 **Sheet** 42 of 55

Rev C

TPA6017 Medium Range Amplifier

Left Connector

Right Connector

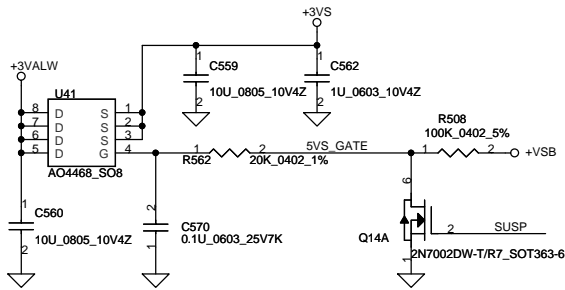
LINE Out/Headphone Out

LINE IN/Ext. MIC JACK

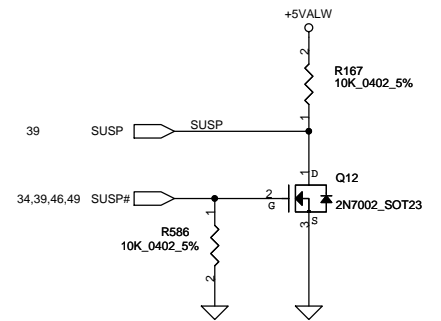
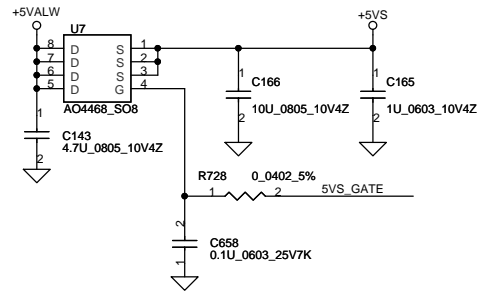
(HDA Jack)

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				401836	C
Date: Thursday, March 18, 2010				Sheet	42 of 55

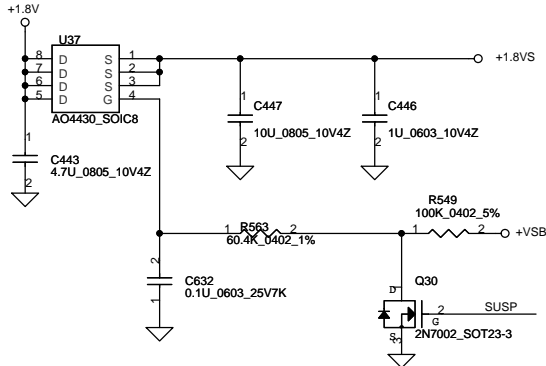
+3VALW TO +3VS



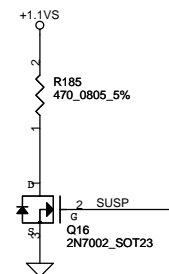
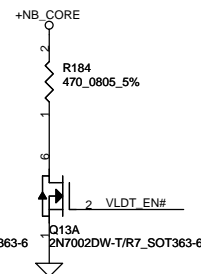
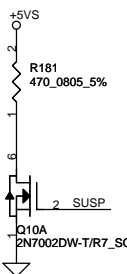
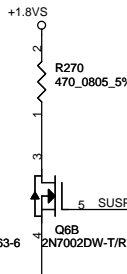
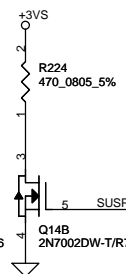
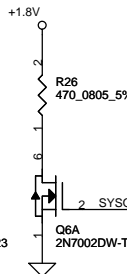
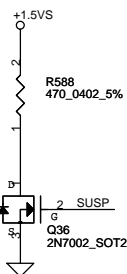
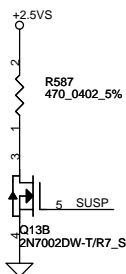
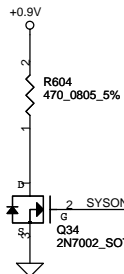
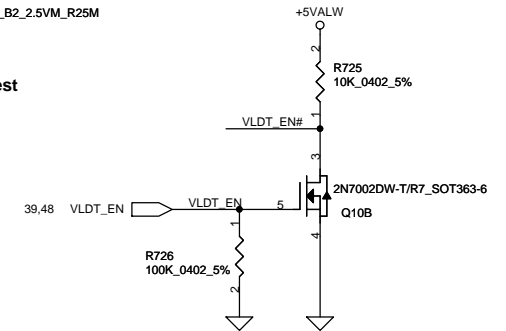
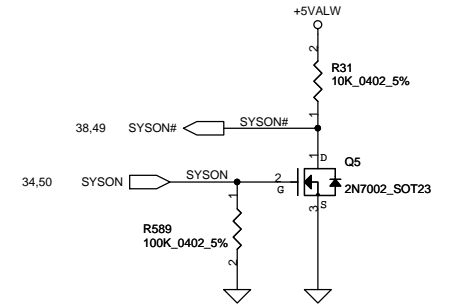
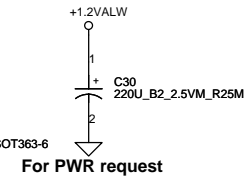
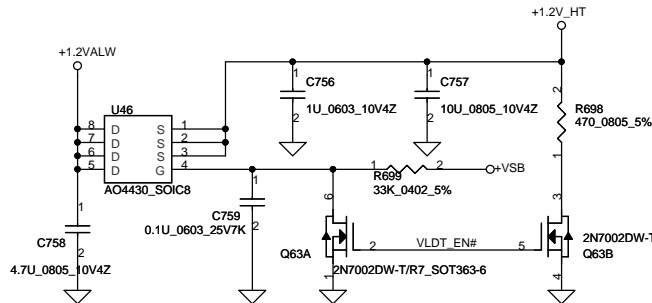
+5VALW TO +5VS



+1.8V TO +1.8VS



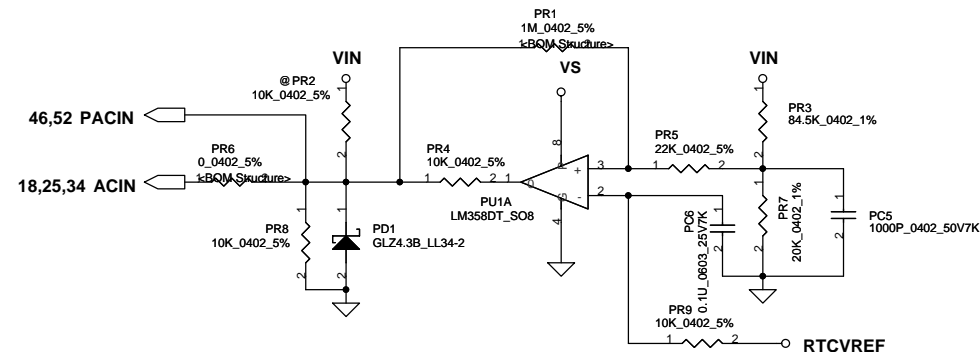
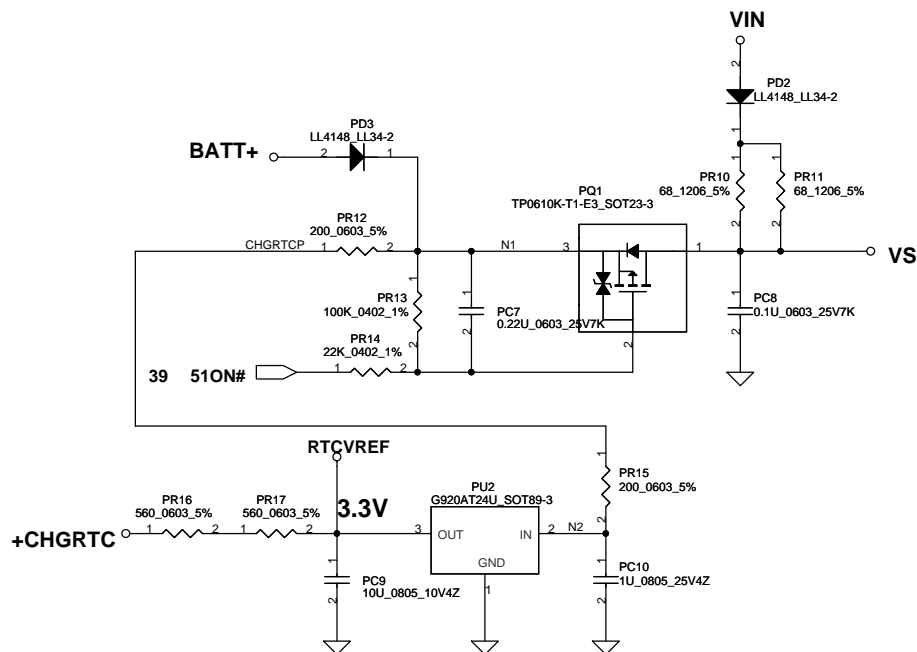
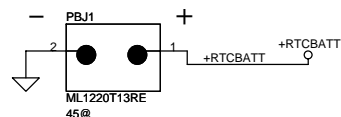
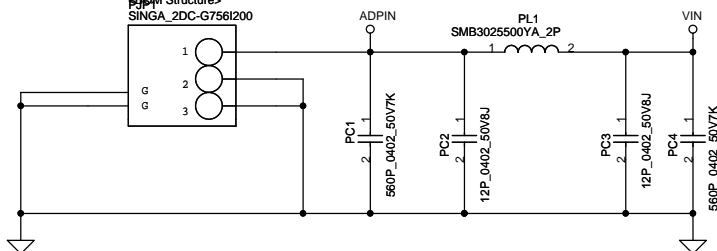
+1.2VALW TO +1.2V_HT



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				Date	Thursday, March 18, 2010
				Sheet	43 of 55

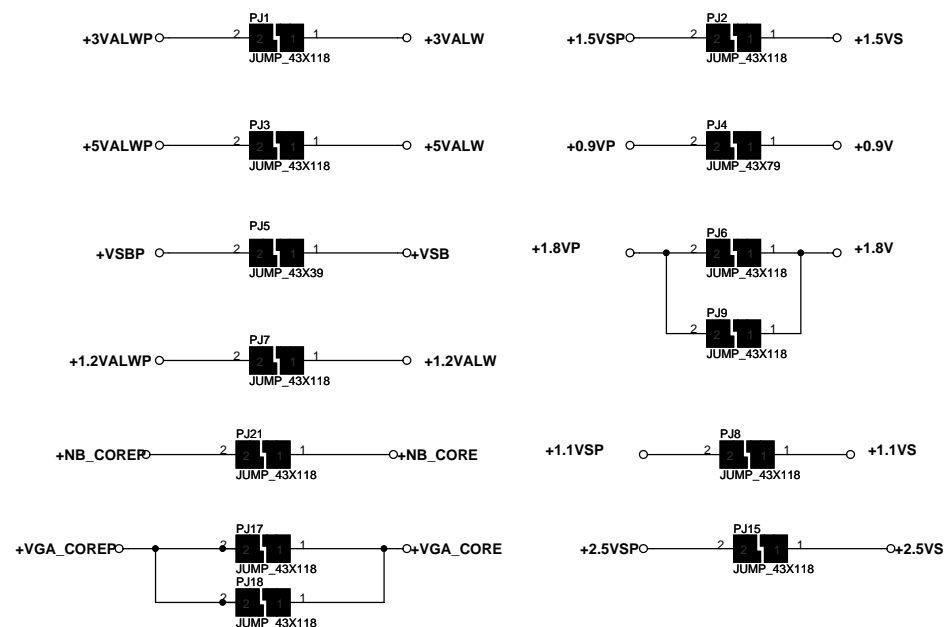
DC231000500

COMP Structure>
SINGA_2DC-G7561200

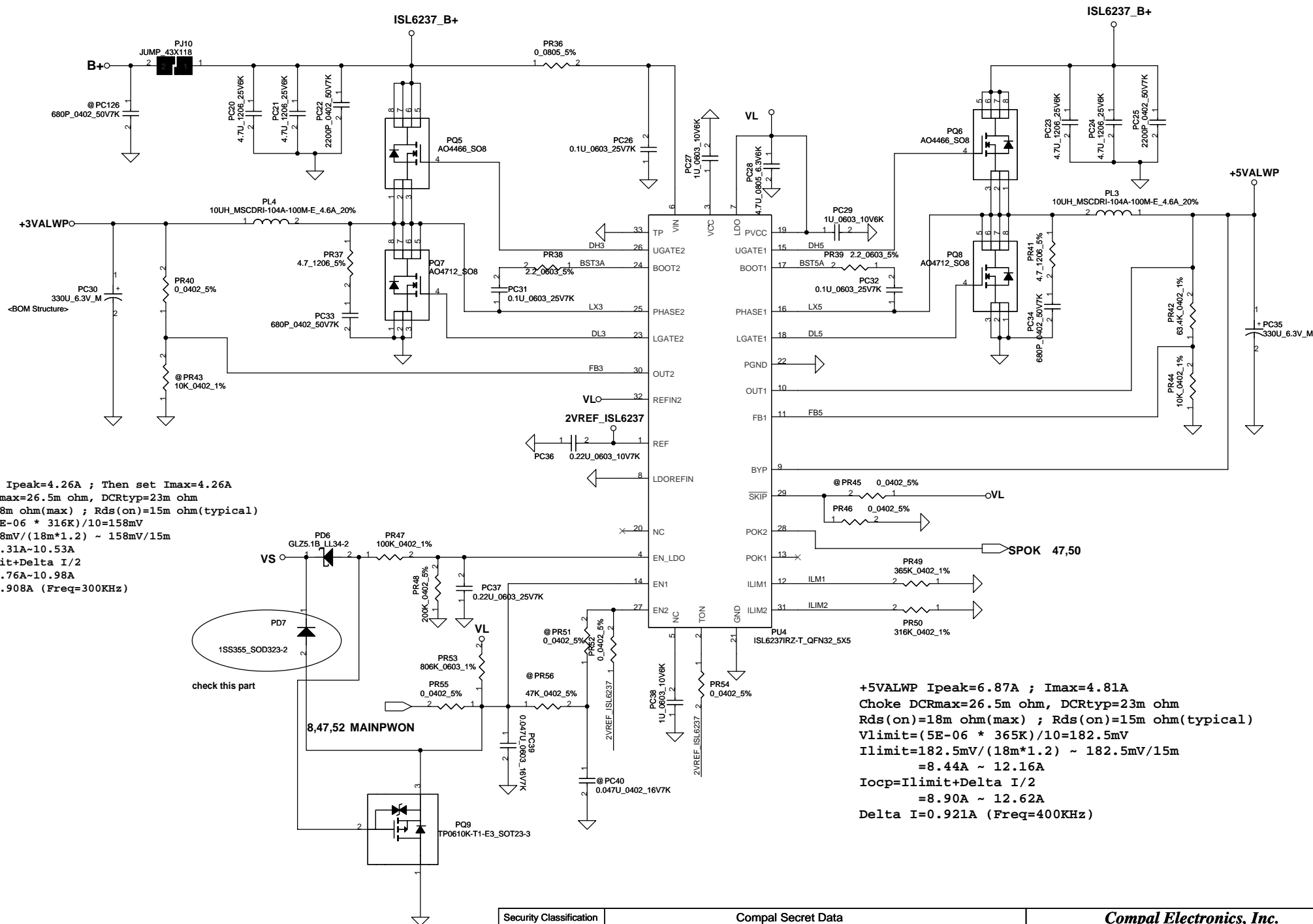


Vin Dectector

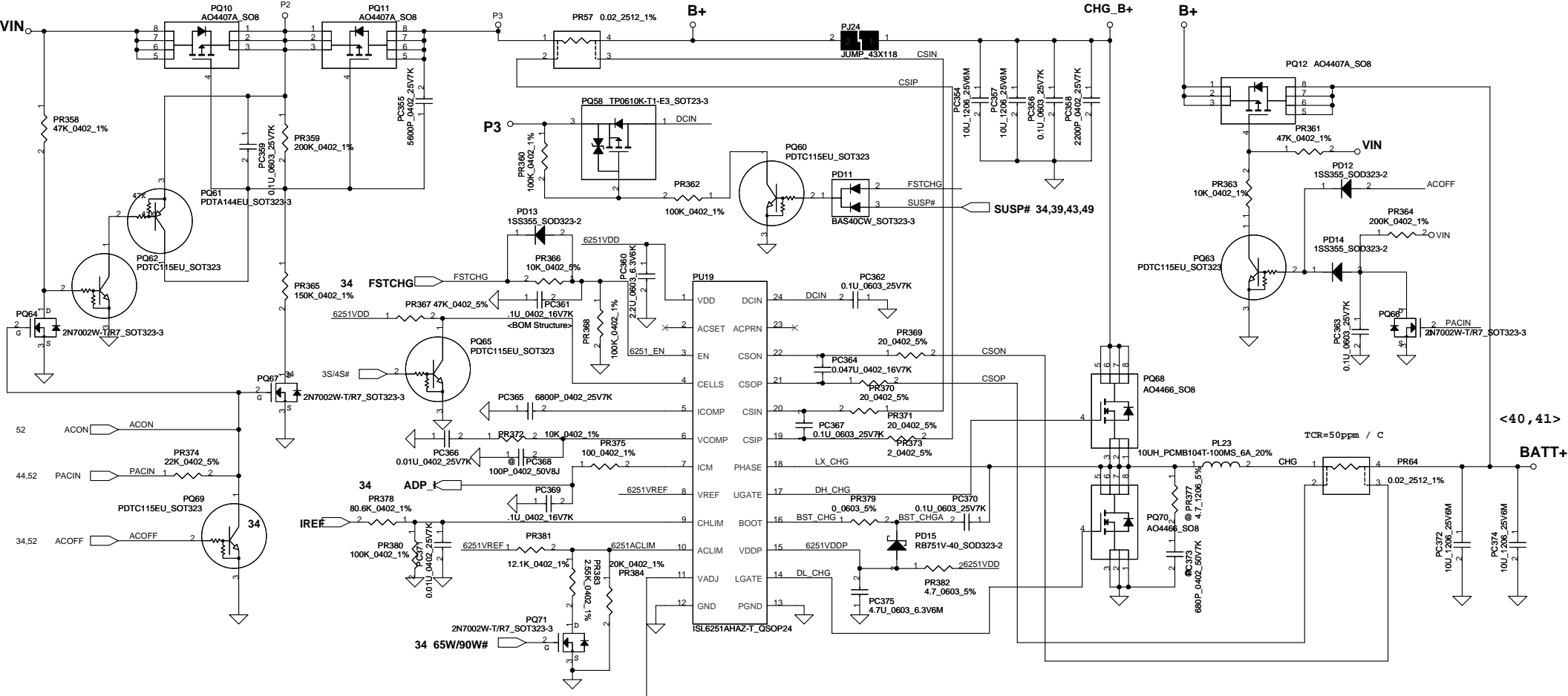
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



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Issued Date	2009/09/25	Deciphered Date	2010/09/25	Title
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				Document Number
				401836
				Rev C
				Date: Thursday, March 18, 2010
				Sheet 44 of 55



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/09/25	Deciphered Date	2010/09/25	Title	SCHEMATIC MB A5992
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				Date:	Thursday, March 18, 2010
				Sheet	45 of 55



CP mode

$I_{input} = (1/0.02) (0.05 * V_{ac1m} / 2.39 + 0.05)$
where $V_{ac1m} = 1.502V$, $I_{input} = 4.07A$

CC=0.6~4.48A

$I_{ref} = 0.7224 * I_{charge}$
 $\Rightarrow K_i = 0.7224$
 $I_{REF} = 0.43V \sim 3.24V$

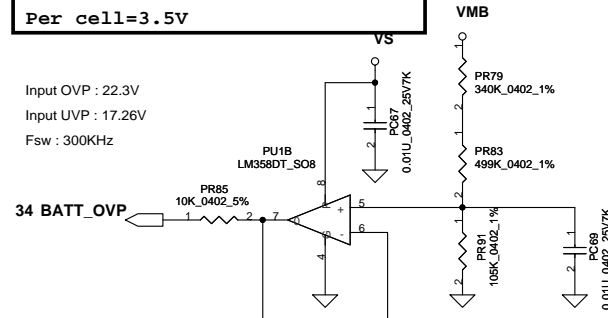
K_i
 $V_{ch1m} = I_{ref} * (PR374 / (PR372 + PR374))$
 $= I_{ref} * (100K / (80.6K + 100K))$
 $= I_{ref} * 0.5537$
 $I_{charge} = (165mV / PR369) * (V_{ch1m} / 3.3V)$
 $= (165m / 20m) * (1/3.3V) * I_{ref} * 0.5537$
 $= 1.3842 * I_{ref}$
 $I_{ref} = 0.7224 * I_{charge} \Rightarrow K_i = 0.7224$

K_v
 $R_{internal} = 514K$ $R_{ec} = 3K$ $R_1 = PR379 = 15.4K$ $R_2 = PR381 = 31.6K$
 $R = 514K // 31.6K // (15.4K + 3K) = 11.372K$
 $r = 514K // 514K // 31.6K = 28.14K$
 $V_{cell} = 0.175 * V_{adj} + 3.99V$
 $4.2V = 0.175 * V_{adj} + 3.99V \Rightarrow V_{adj} = 1.2V$
 $V_{adj} = V_{ref} * (R / (R + 514K)) + CALIBRATE * (r / (r + 514K))$
 $1.1483 = CALIBRATE * 0.6046 \Rightarrow CALIBRATE = 1.899$
 $1.899 = (4.2 - (V_{cell} + A * 0.175)) * K_v = (4.2 - (4.2 + A * 0.175)) * K_v$
 $A = V_{ref} * (R / (R + 514K)) = 0.052$
 $K_v = 9.451$

LI-3S :13.5V---BATT-OVP=2.007V

BATT-OVP=0.1487*VMB
Per cell=3.5V

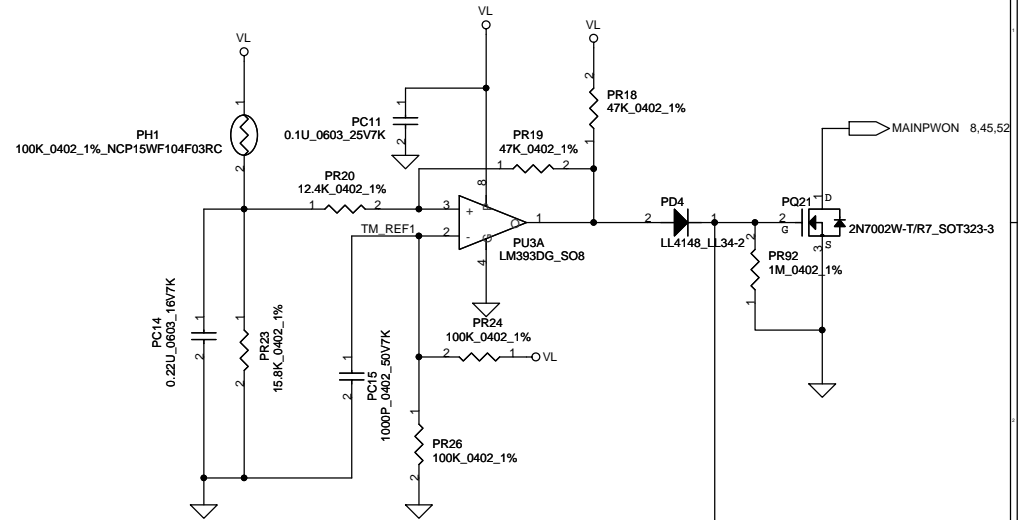
Input OVP : 22.3V
Input UVP : 17.26V
Fsw : 300KHz



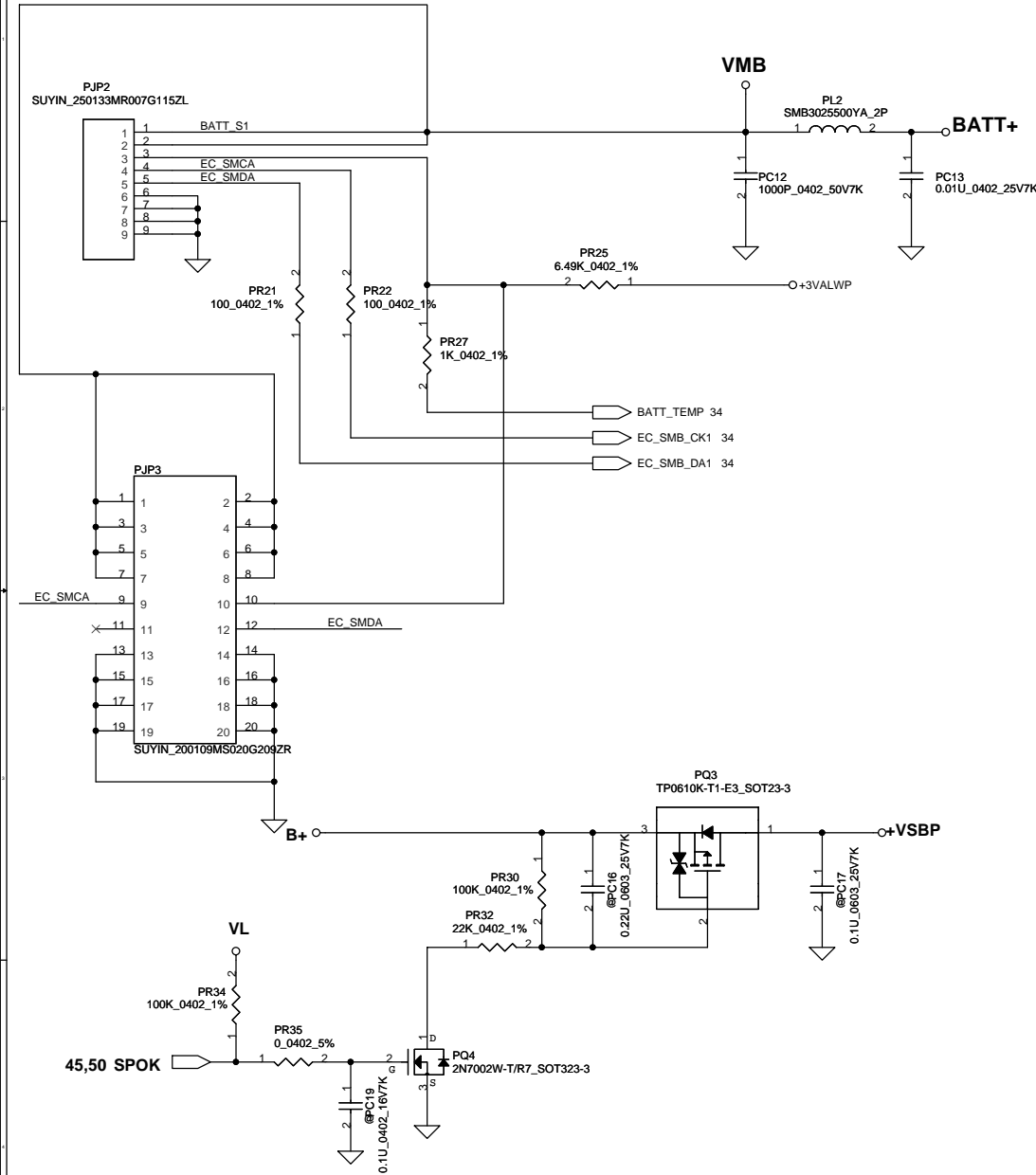
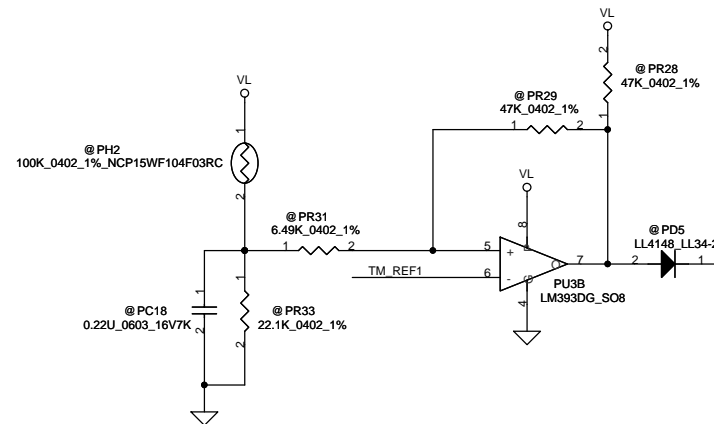
BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

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Issued Date	2009/09/25	Deciphered Date	2010/09/25	Title	SCHEMATIC MB A5992
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				Rev	C
				Date:	Thursday, March 18, 2010
				Sheet	46 of 55

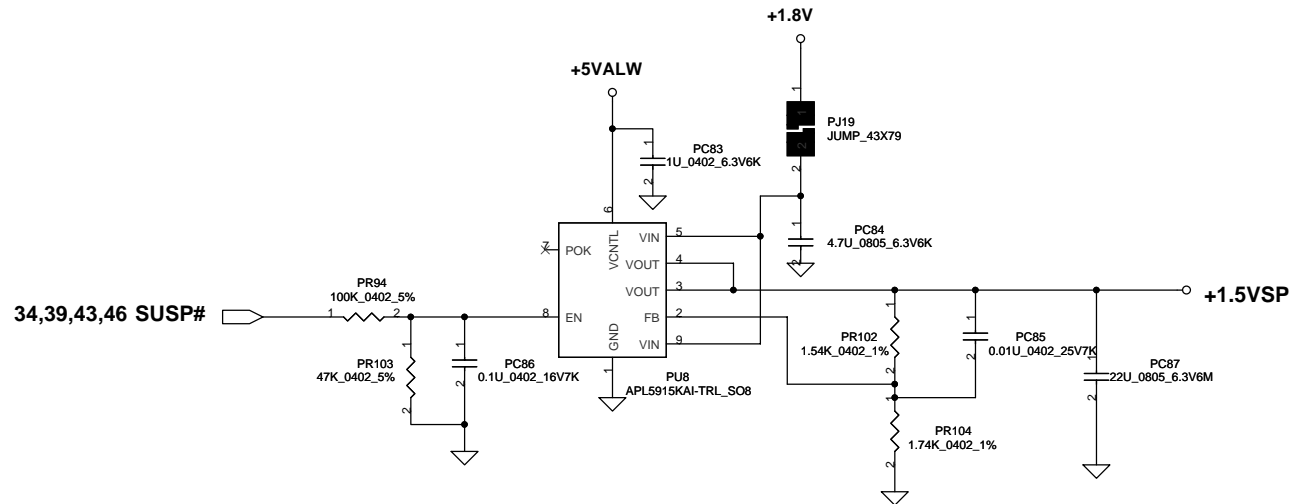
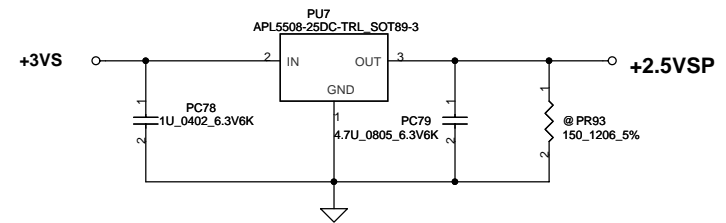
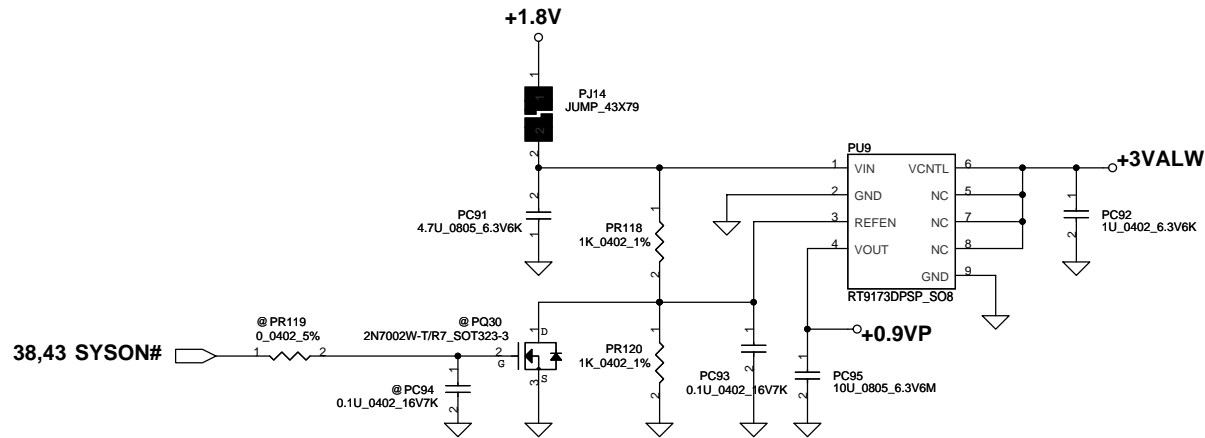
PH1 under CPU botten side :
CPU thermal protection at 92 degree C



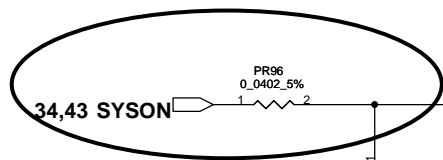
PH2 near main Battery CONN :
BAT. thermal protection at 75 degree C



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Issued Date	2009/09/25	Deciphered Date	2010/09/25	Title	SCHEMATIC MB A5992
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				Rev	C
				Date:	Thursday, March 18, 2010
				Sheet	47 of 55

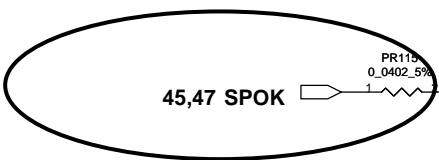
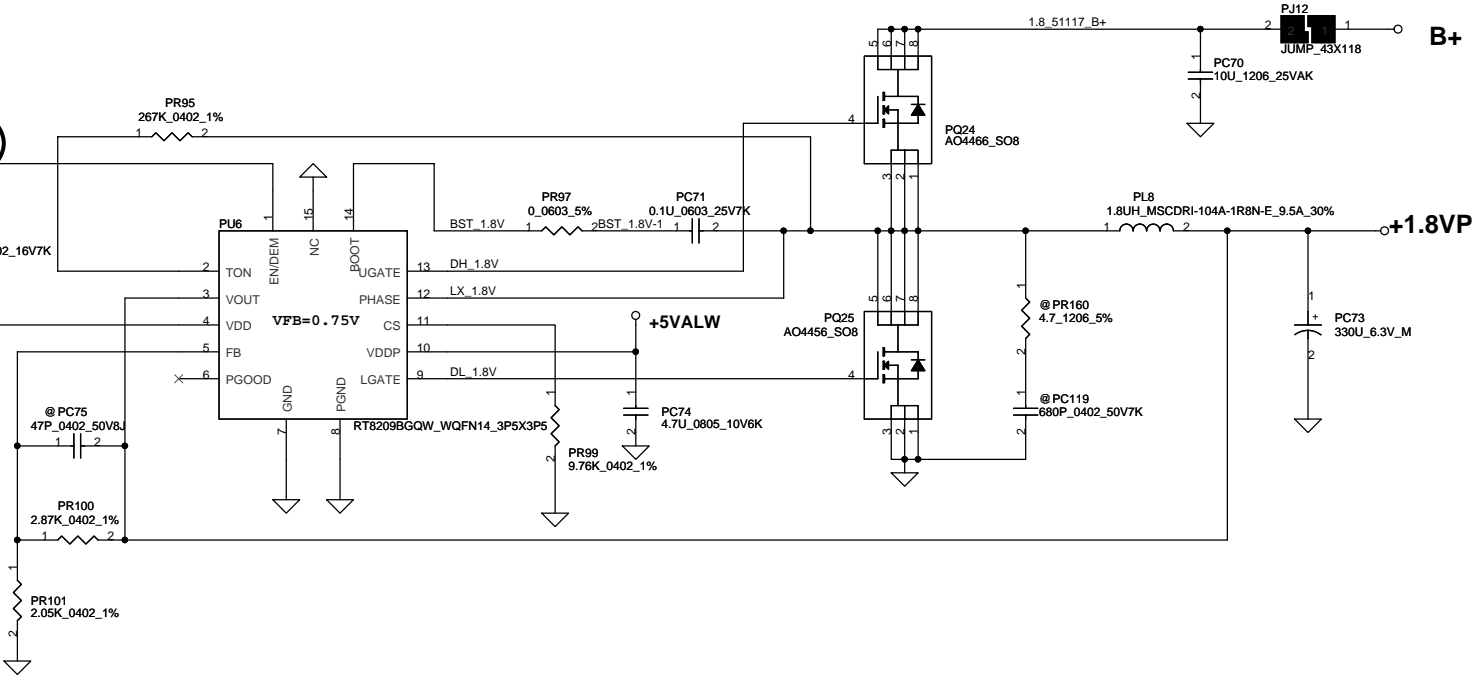


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				401836	Rev C
Date: Thursday, March 18, 2010				Sheet	49 of 55



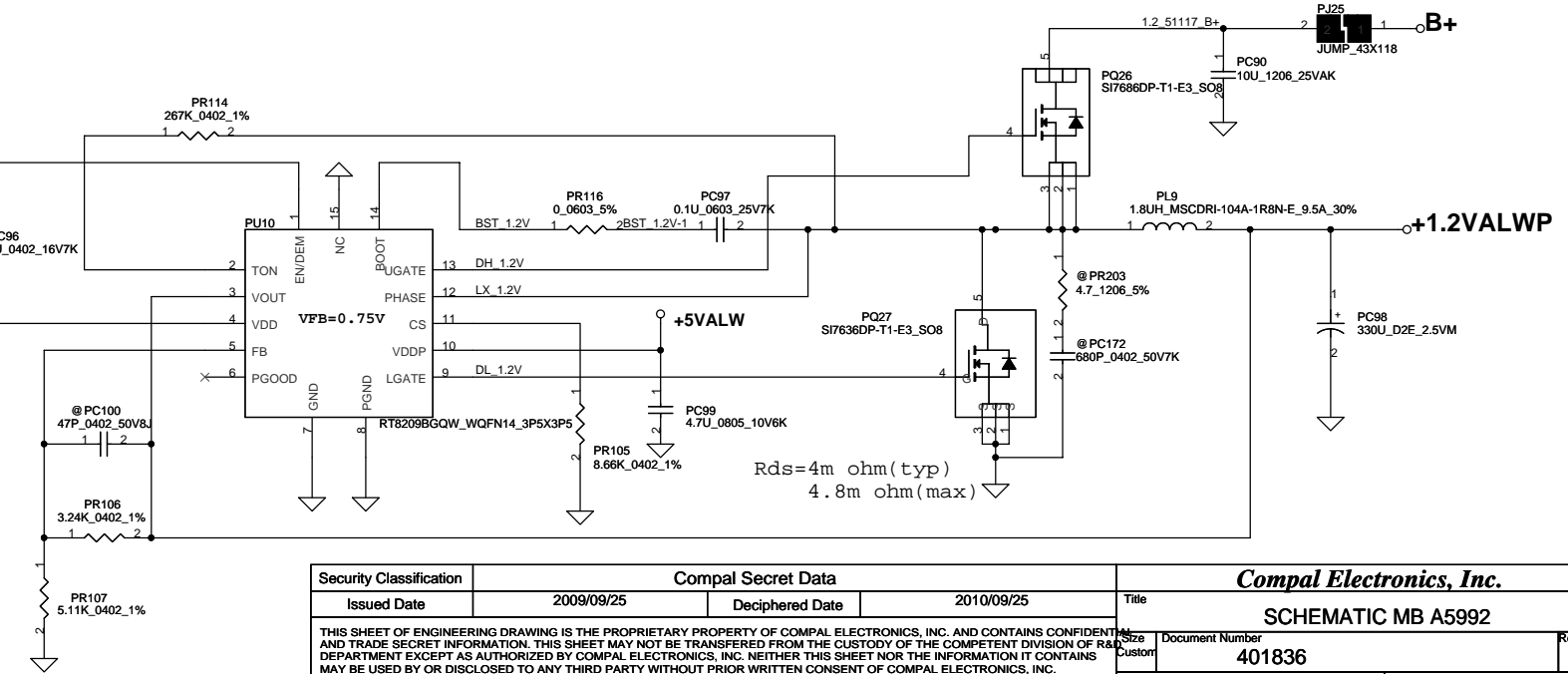
VFB=0.75V
 $V_o = VFB * (1 + PR111 / PR112) = 0.75 * (1 + 14K / 10K) = 1.8V$
 $R_{ton} = 267K \Rightarrow F_{aw} = 297KHz$

Cout ESR=15m ohm
 $I_{peak} = 11.96A$, $I_{max} = 8.372A$
 $\Delta I = ((19 - 1.8) * (1.8 / 19)) / (L * F_{sw})$
 $((19 - 1.8) * (1.8 / 19)) / (1.8u * 297000) = 3.048A$
 $\Rightarrow 1 / 2 \Delta I = 1.524A$
 $R_{trip} = 9.76K$
 $I_{ocp} = 15.20A - 24.71A$



VFB=0.75V
 $V_o = VFB * (1 + PR119 / PR120) = 0.75 * (1 + 6.04K / 10K) = 1.203V$
 $R_{ton} = 267K \Rightarrow F_{sw} = 298KHz$

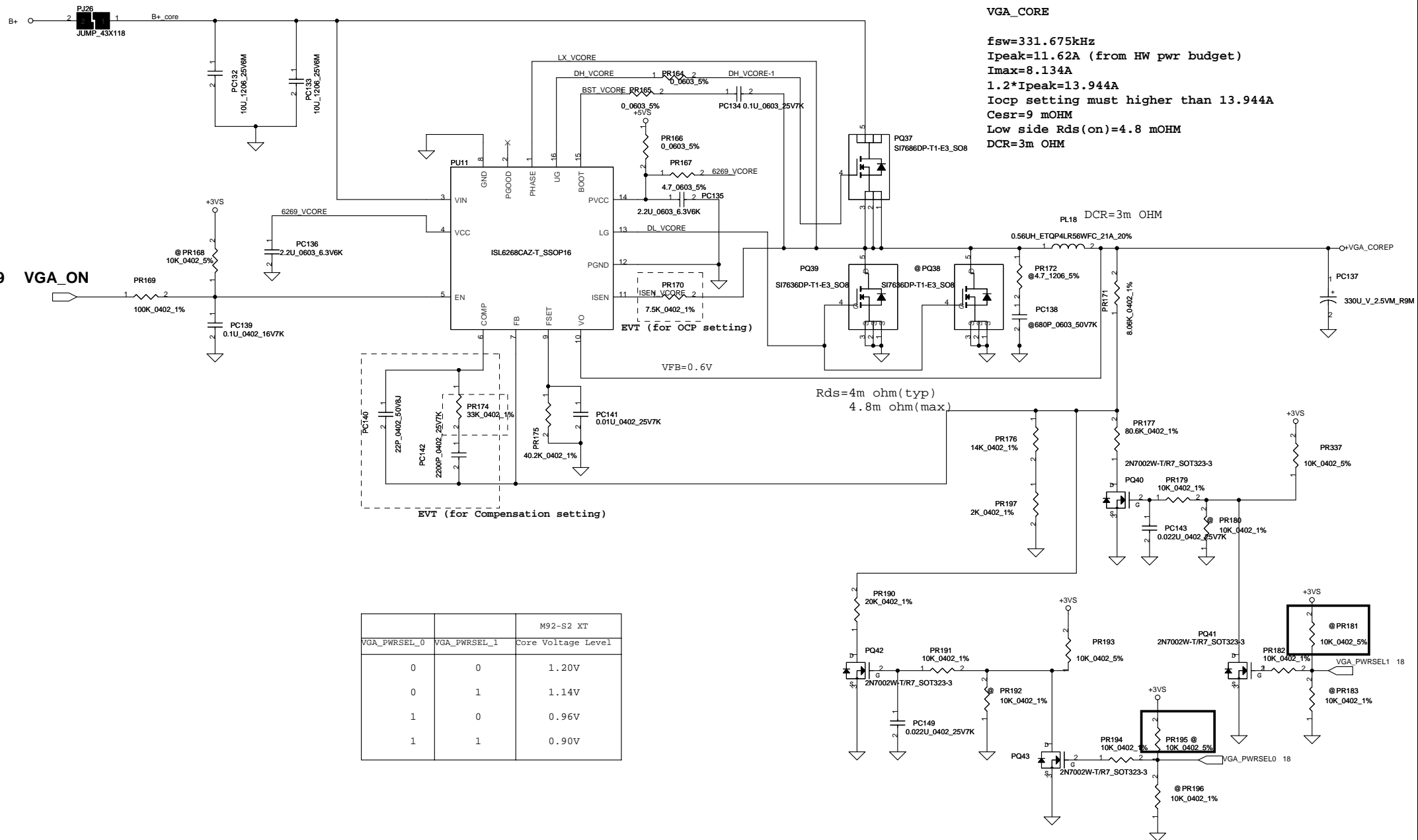
1.2VP $I_{peak} = 7.4A$; $I_{max} = 5.180A$
 $\Delta I = ((19 - 1.2) * (1.2 / 19)) / (L * F_{sw})$
 $((19 - 1.2) * (1.2 / 19)) / (1.8u * 298000) = 2.10A$
 $\Rightarrow 1 / 2 \Delta I = 1.05A$
 $R_{dson} = 15m / 18m ohm$
 $set R_{trip} = 8.66K$
 $I_{cop_min} = 4.77A$
 $I_{cop_max} = 7.74A$



$R_{ds} = 4m ohm (typ)$
 $4.8m ohm (max)$

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						Size		Document Number		Rev	
						Custom		401836		C	
						Date:		Thursday, March 18, 2010		Sheet 50 of 55	

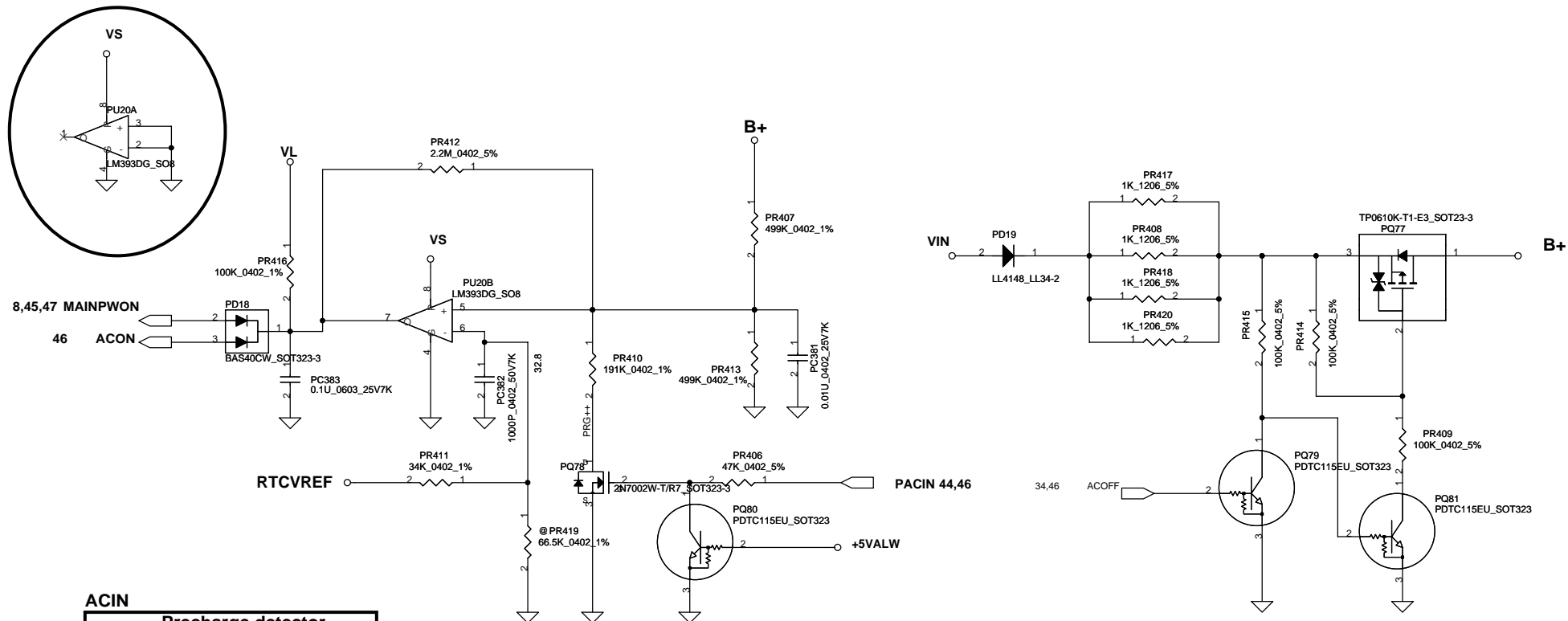
39 VGA_ON



		M92-S2 XT
VGA_PWRSEL_0	VGA_PWRSEL_1	Core Voltage Level
0	0	1.20V
0	1	1.14V
1	0	0.96V
1	1	0.90V

VGA_CORE

fsw=331.675kHz
Ipeak=11.62A (from HW pwr budget)
Imax=8.134A
1.2*Ipeak=13.944A
Iocp setting must higher than 13.944A
Cesr=9 mOHM
Low side Rds(on)=4.8 mOHM
DCR=3m OHM



ACIN

Precharge detector

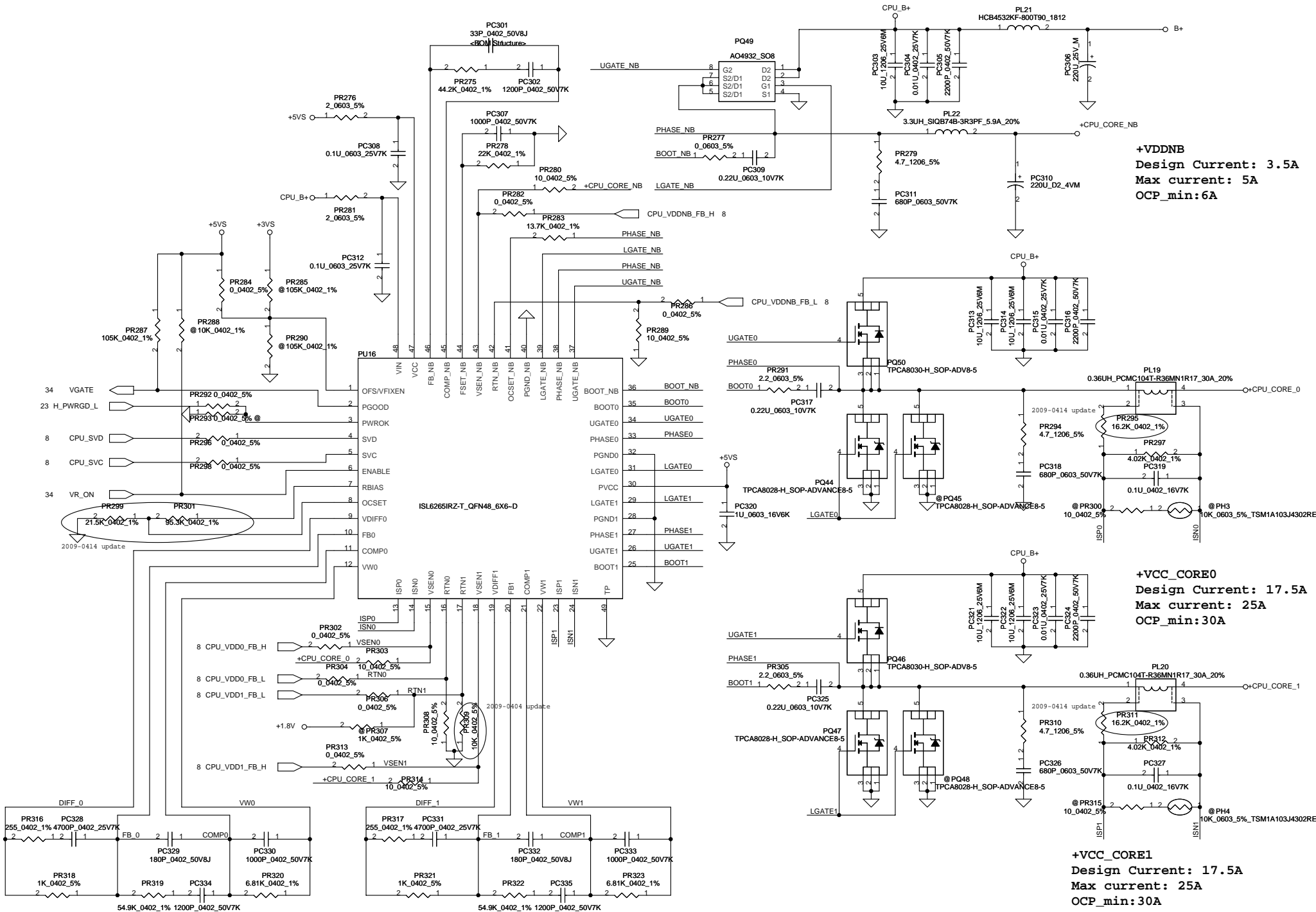
	Min.	typ.	Max
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector

	Min.	typ.	Max
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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				Date	Thursday, March 18, 2010
				Sheet	52 of 55



Security Classification		Compal Secret Data		Title	
Issued Date	2009/09/25	Deciphered Date	2010/09/25	Document Number	401836
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Date: Thursday, March 18, 2010					Sheet 53 of 55

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	HW required to adjust from 1.14V to 1.12V	HW required to adjust from 1.14V to 1.12V	0.1	42	Change PR271 from SD034300180 (S RES 1/16W 3K +-1% 0402) to SD034324180 (S RES 1/16W 3.24K 0402 1%)	09, 05/07	to PVT
2	Power sequense adjust.	HW required to adjust power sequense.	0.1	42	Add PC208 SE076104K80 (S CER CAP .1U 16V K X7R 0402)	09, 05/07	to PVT
3	Power sequense adjust.	HW required to adjust power sequense.	0.1	42	Change PR247 from SD028000080 (S RES 1/16W 0 +-5% 0402) to SD028130180 (S RES 1/16W 1.3K 0402 5%)	09, 05/07	to PVT
4	NB_COREP working frequency has issue.	Because NB_COREP working frequency will be gitter while system at heavy loading. Change to larger ESR Cap will be solve.	0.1	42	Change PC210 from SGAI9331D00 (S POLY C 330U 2.5V M D2 TPE LESR15M H1.8) to SGA00002B00 (S POLY C 330U 6.3V M D2E ESR25M TPE H1.8)	09, 05/07	to PVT
5	BOM error	BOM error	0.1	42	Add PR270 SD28100280(S RES 1/16W 10K 0402 5%)	09, 05/07	to PVT
6	BOM error	BOM error	0.1	42	Change PR103 from SD028470280(S RES 1/16W 47K 0402 5%) to SD028100280(S RES 1/16W 10K 0402 5%)	09, 05/07	to PVT
7							
8	Change Power Source	For WLAN wakeup	1.0	37	Change R550 to +3VALW	09, 05/07	Pre-MP
9							
10							
11							
12							
13							
14							
15							
16							
17							
18							

DD