


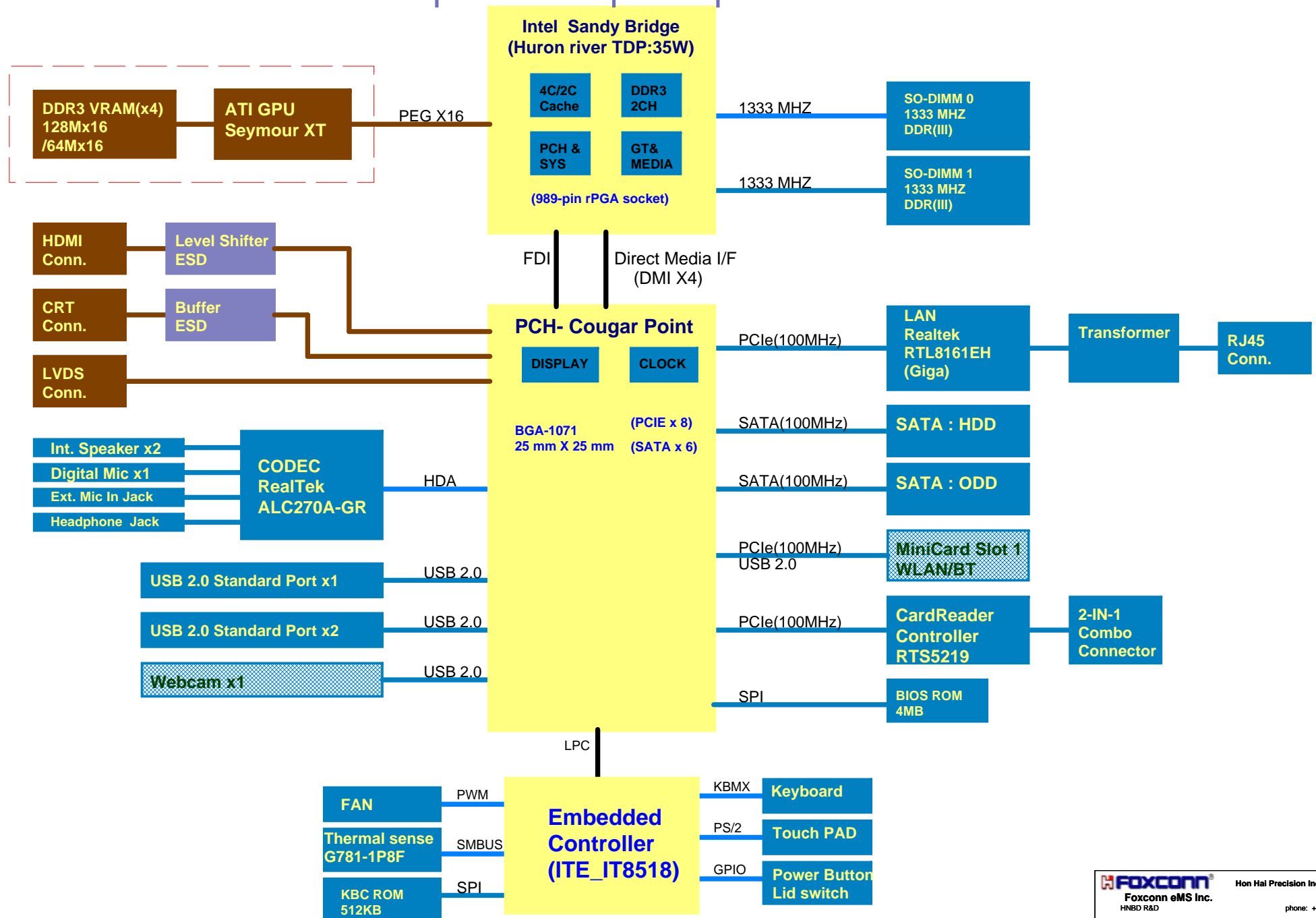
## PROJECT : CHICAGO (For Intel Huron River Platform)

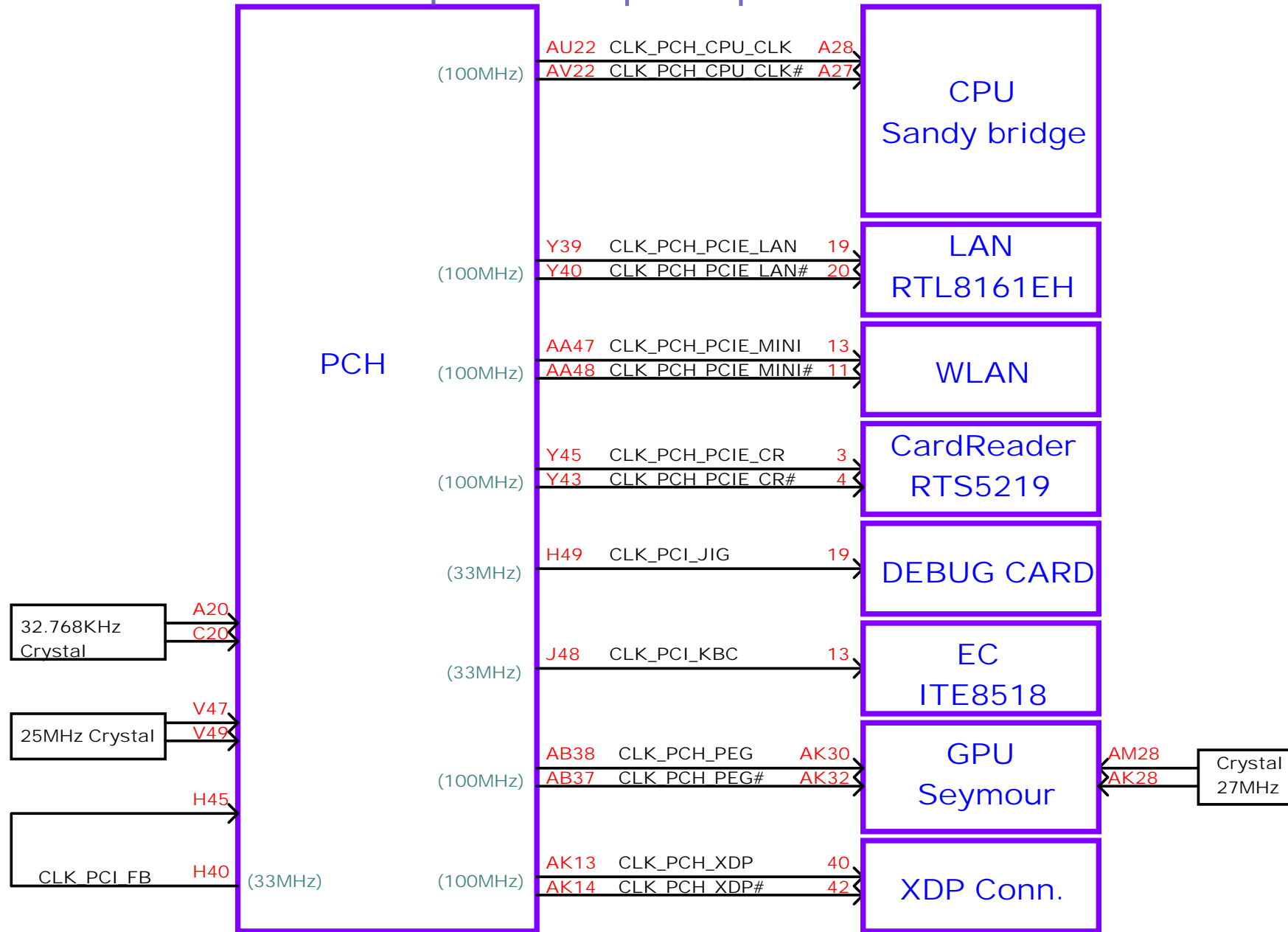
01 -- COVER SHEET	23 -- CougarPoint (HDA, SATA..)
02 -- SYSTEM BLOCK DIAGRAM	24 -- CougarPoint (PCI-E, CLK..)
03 -- CLOCK MAP	25 -- CougarPoint (DMI, FDI..)
04 -- POWER SEQUENCY DIAGRAM	26 -- CougarPoint (USB, GPIO..)
05 -- POWER MAP	27 -- CougarPoint (PWR/GND)
06 -- SMBUS MAP	28 -- CougarPoint (PWR, GND)
07 -- Blank	29 -- DDR3 (SO-DIMM 0&1)
08 -- DCIN/BATT	30 -- VGA (PCI-E/STRAP) 1/3
09 -- PWR_CHARGE	31 -- VGA_S3 (IO) 2/3
10 -- PWR_5V/3.3V	32 -- VGA_S3 (DDR3) 3/3
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13 -- PWR_VCORE	35 -- Audio (CODEC_ALC270A)
14 -- PWR_OTHER	36 -- Audio (JACK+AMP+SPK+Mute)
15 -- PWR_ATVDD	37 -- LAN (RTL8161EH)
16 -- PWR_1.8VS	38 -- Mini PCIe & FAN
17 -- PWR_VCCSA	39 -- USBx2/USB DB/SATA CONN.
18 -- Sandy Bridge (DMI, PEG, FDI)	40 -- Card Reader (RTL5219-GR)
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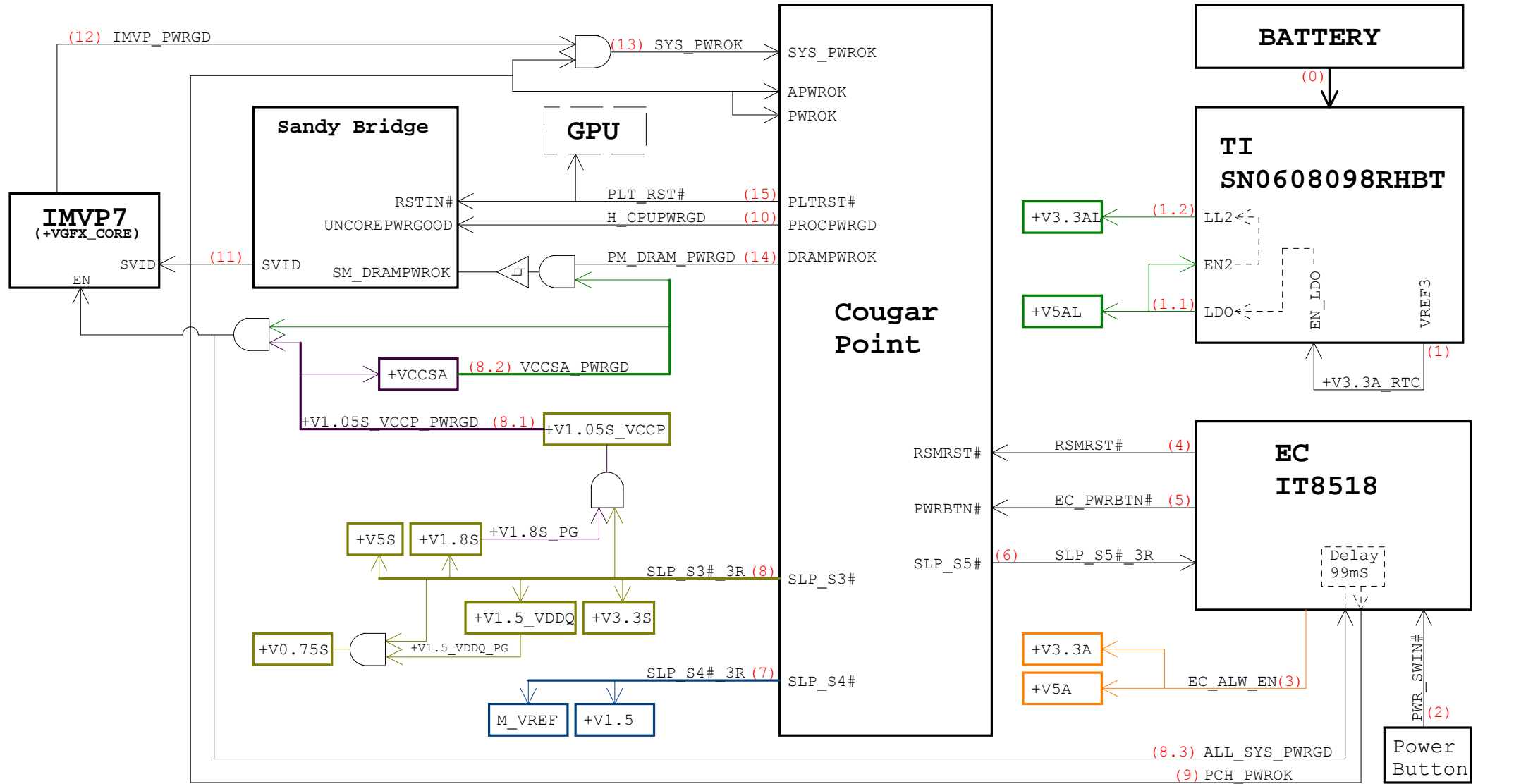
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Title		
<b>Index Page</b>		
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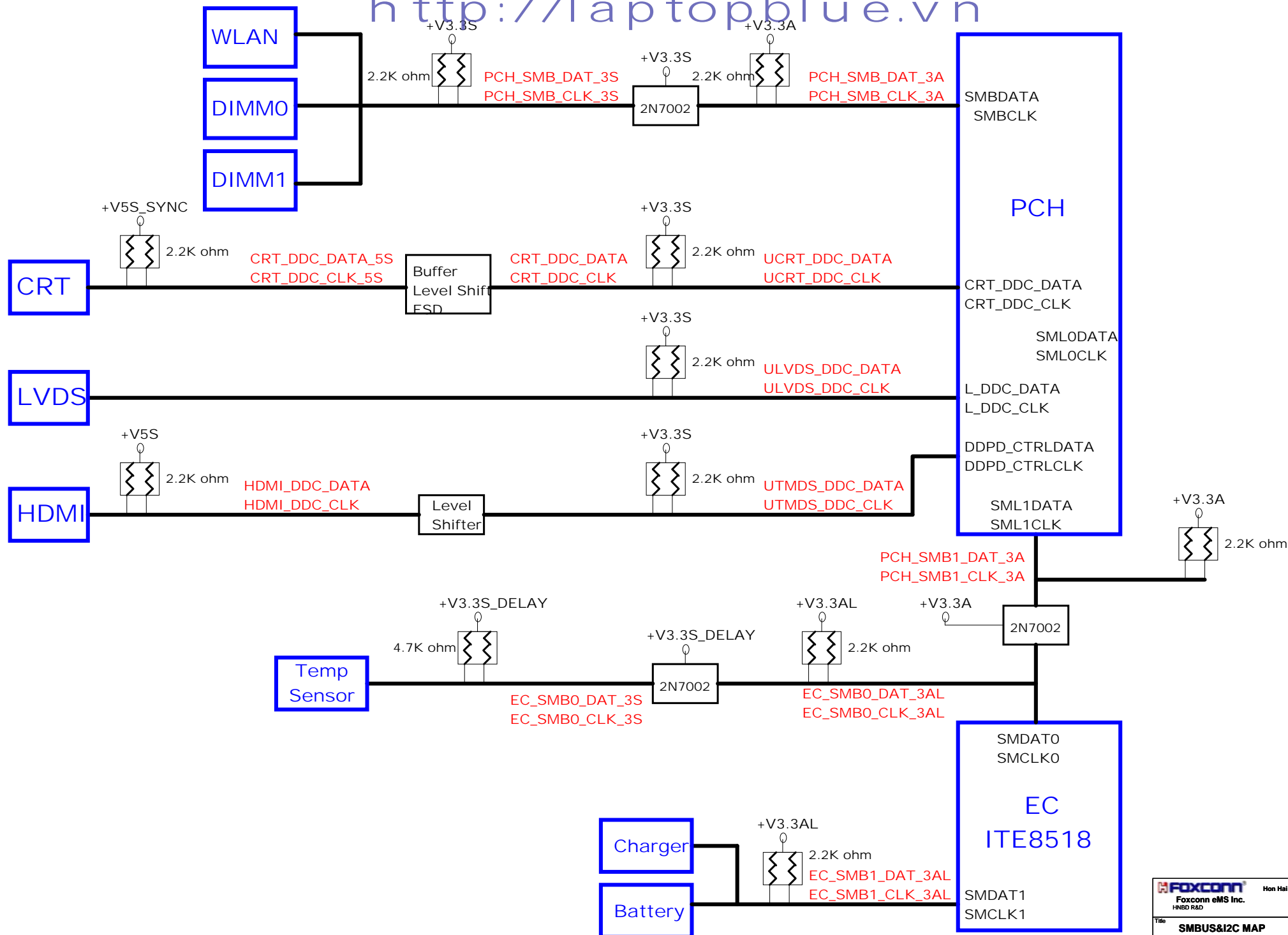






# POWER MAP



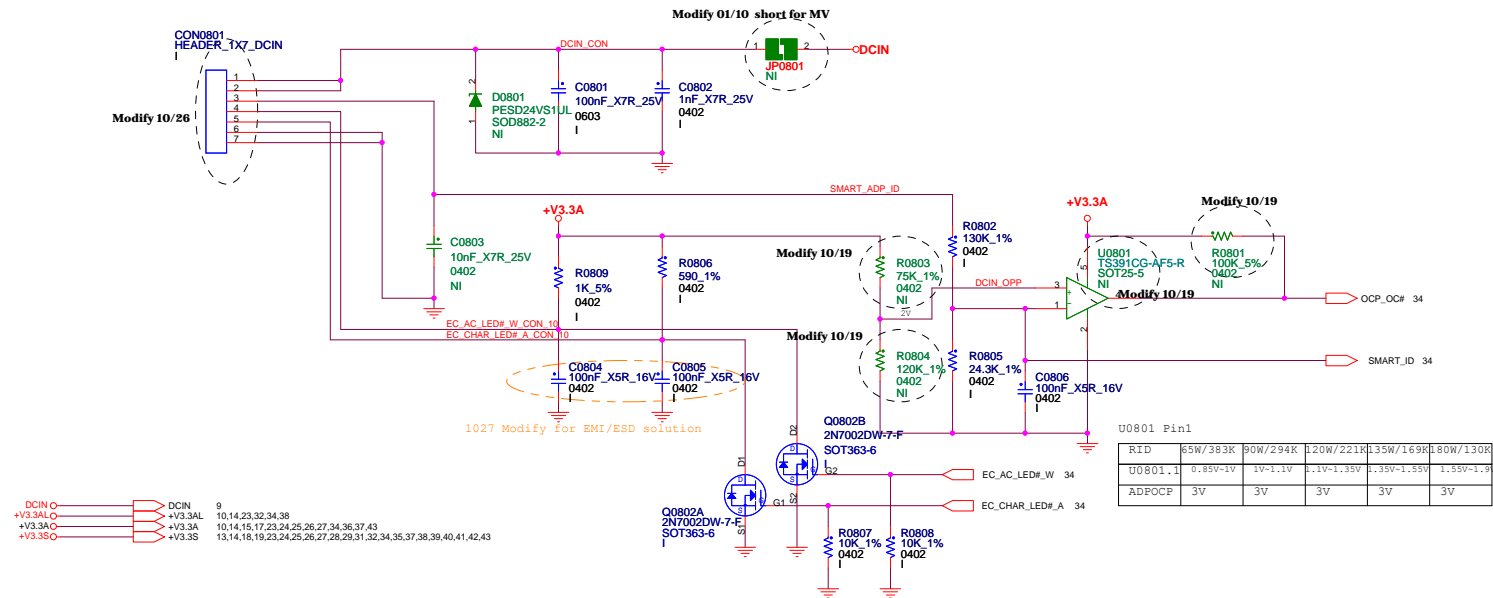


h t t p : / / l a p t o p b l u e . v n

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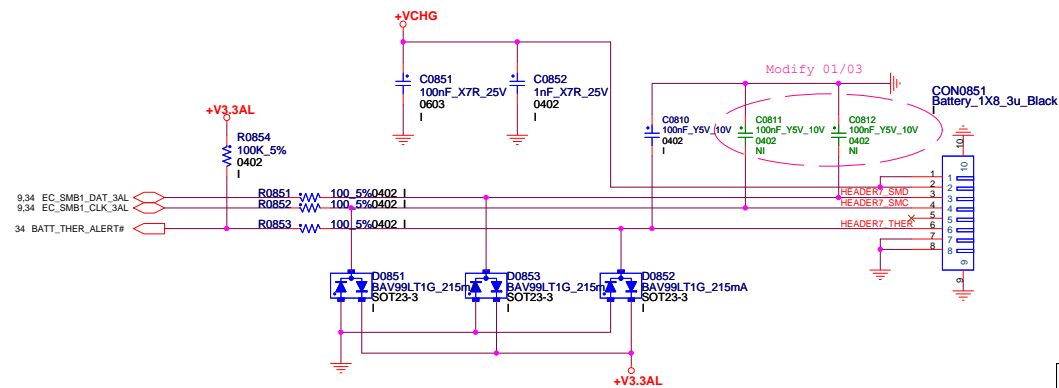
# DC\_JACK WIRE to BOARD CONNECTOR

2010.1203.0



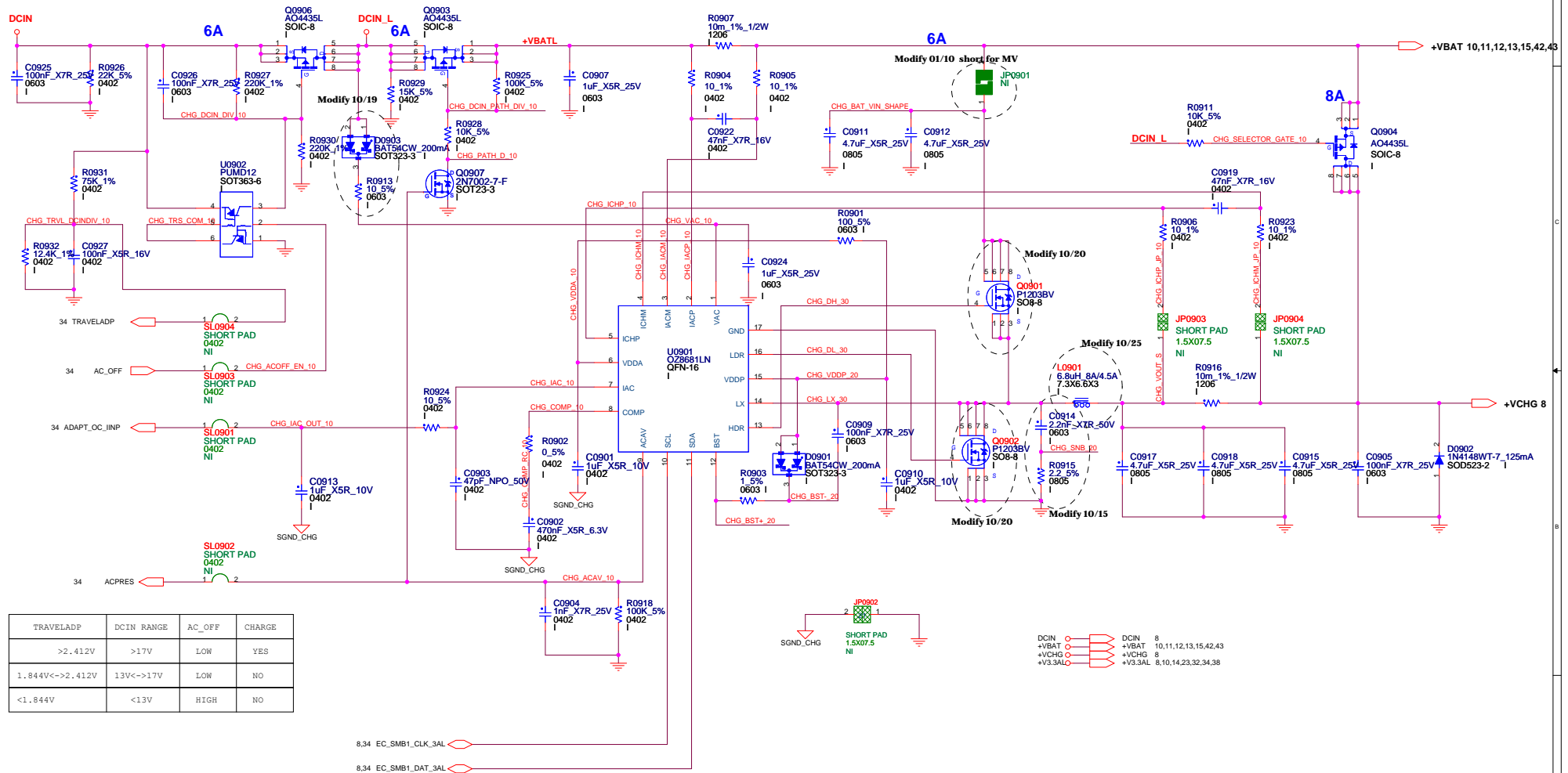
## BATTERY CONNECTOR

2010.0914.0





# BATTERY CHARGER



TRAVELADP	DCIN_RANGE	AC_OFF	CHARGE
>2.412V	>17V	LOW	YES
1.844V<->2.412V	13V<->17V	LOW	NO
<1.844V	<13V	HIGH	NO





## +V1.5 POWER SUPPLY

2010.1026.0



- +V1.5:
1. **I/P Current:**  
 $I_{in} = V_o / I_o (0.75 \times V_{in}) = 1.78A$
  2. **Ripple Current:**  
 $I_{rip} = 3.34A$
  3. **Ripple Voltage:**  
 $ESR / I = 9m\Omega$   
 $V_{rip} = 30.6mV$
  4. **Inductor Spec:**  
 $I_{sat} = 36A$   
 $I_{dc} = 18A$   
 $DCR = 3.3m\Omega$
  5. **MOSFET Spec:**  

<b>H-side MOSFET: IRF8707PBF</b>	<b>L-side MOSFET: IRF8707PBF</b>
$R_{ds(ON)} = 17.5m\Omega$ ( $V_{gs} = 4.5V$ )	$R_{ds(ON)} = 17.5m\Omega$ ( $V_{gs} = 4.5V$ )
$I_{cont} = 11A$ ( $T = 25^\circ C$ )	$I_{cont} = 11A$ ( $T = 25^\circ C$ )
$I_{peak} = 88A$ (Pause = 10 us)	$I_{peak} = 88A$ (Pause = 10 us)
  6. **Frequency:**  
 $F = 290KHz$  ( $R_{0902} = 0\Omega$ )
  7. **OCP:**  
 $Set = R1207$  to  $120K$   
 $V_{trip} = R1207 \times 10uA = 1.2V$   
 $I_{ocp} = (V_{trip} / 8 \times R_{ds(on)}) + I_{ripple} / 2 = 10A$

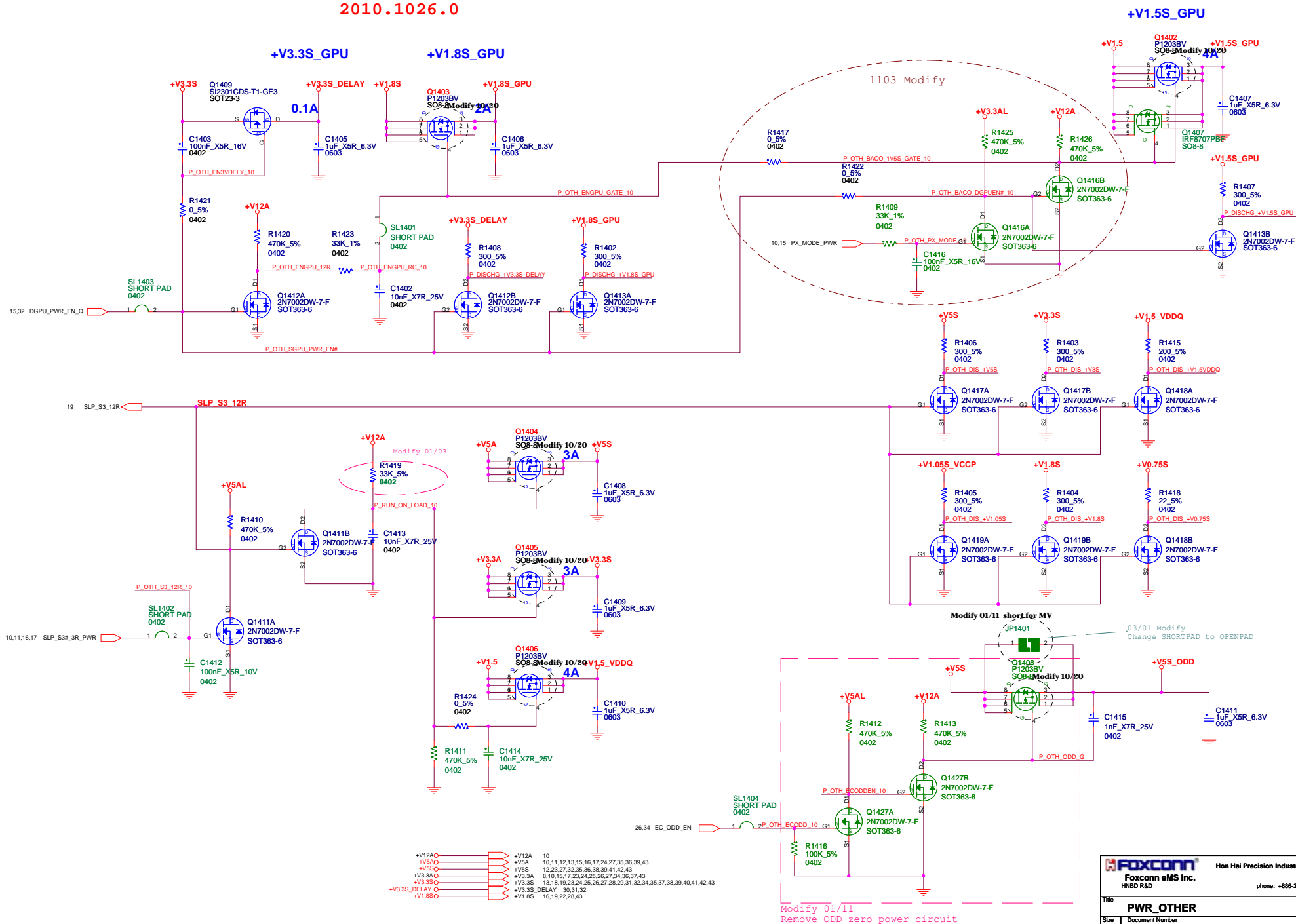
## +V0.75S POWER SUPPLY

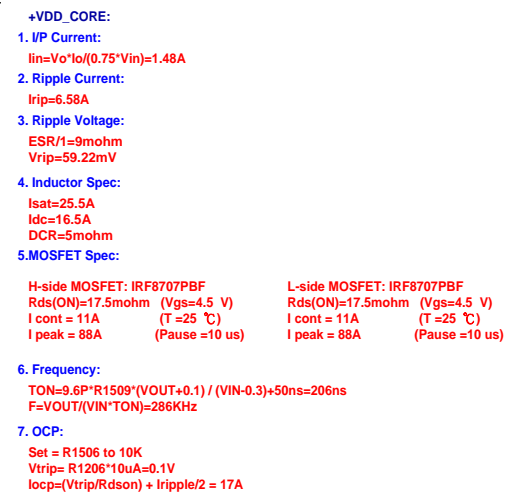
2010.1026.0





2010.1026.0





2010.1020.0



# +V1.8S POWER SUPPLY

2010.1025.0

+V1.8S:

1. I/P Current:

$$I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.44A$$

2. Ripple Current:

$$I_{rip} = 0.53A$$

3. Ripple Voltage:

$$ESR/3 = 3.3m\Omega$$

$$V_{rip} = 1.75mV$$

4. Inductor Spec:

$$I_{sat} = 14A$$

$$I_{dc} = 8A$$

$$DCR = 20m\Omega$$

5. MOSFET Spec:

H-side P-MOSFET:

L-side N-MOSFET:

$$R_{ds(ON)} = 110m\Omega \quad (V_{gs} = 4.5V)$$

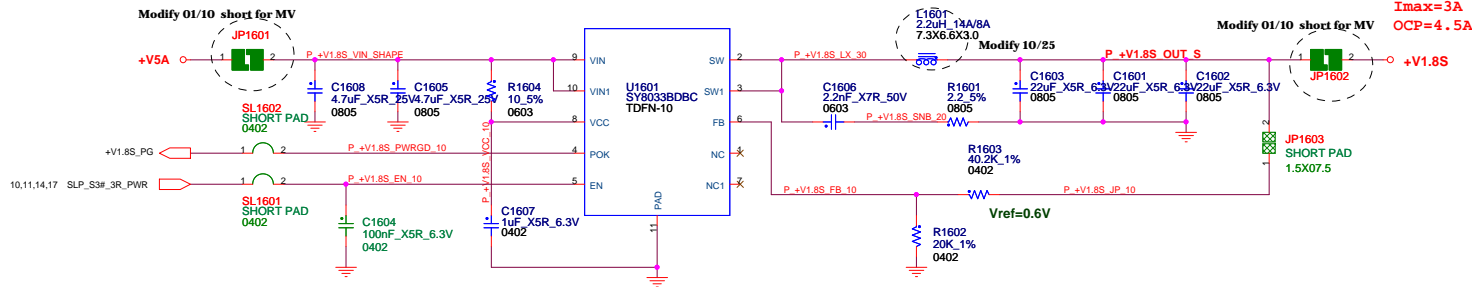
$$R_{ds(ON)} = 75m\Omega \quad (V_{gs} = 4.5V)$$

6. Frequency:

$$F = 1MHz \quad (min = 800KHz, max = 1.2MHz)$$

7. OCP:

$$I_{ocp} = 4A(min) / 4.5A(typ) / 5A(max)$$



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+1.8VS

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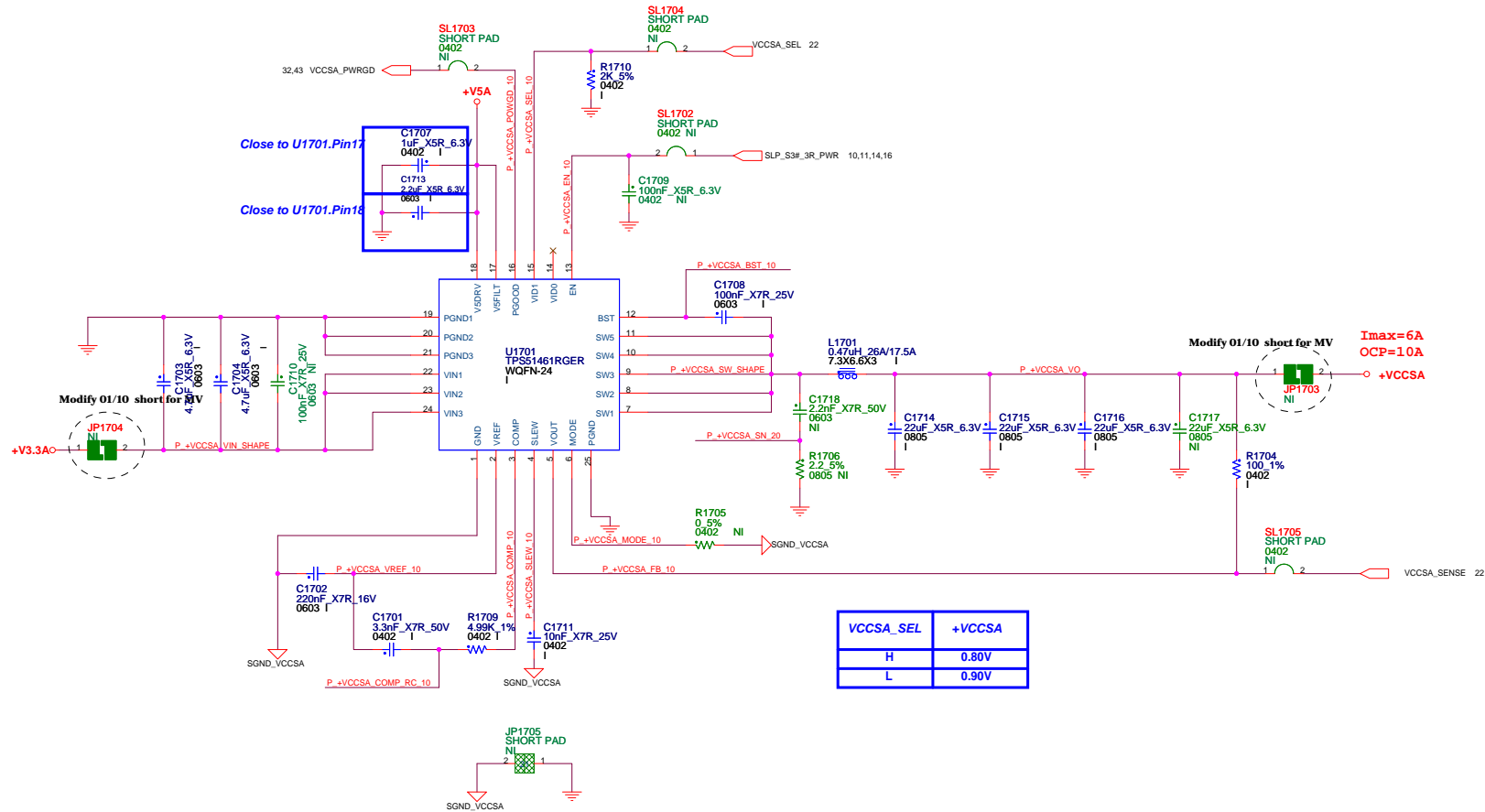
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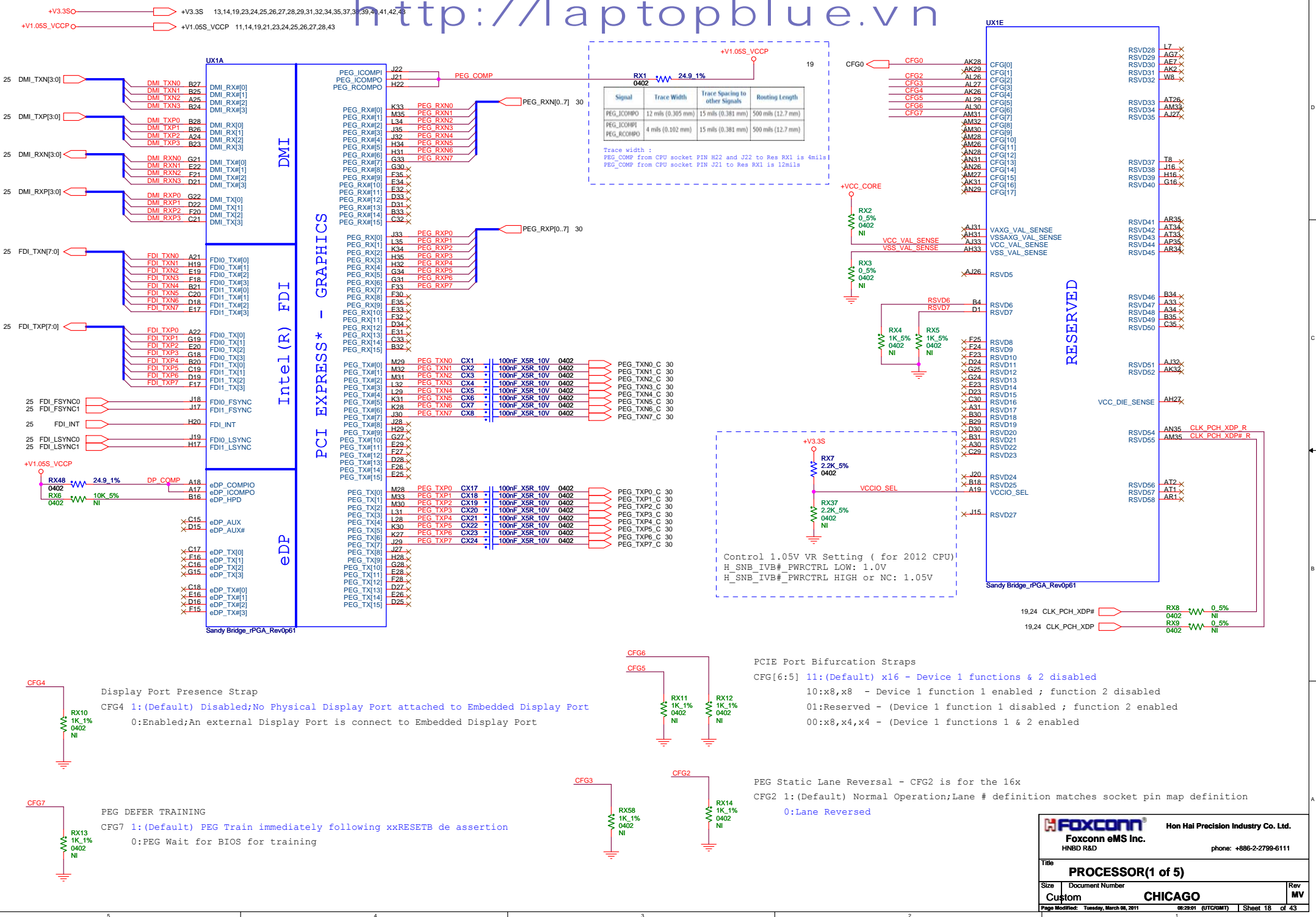


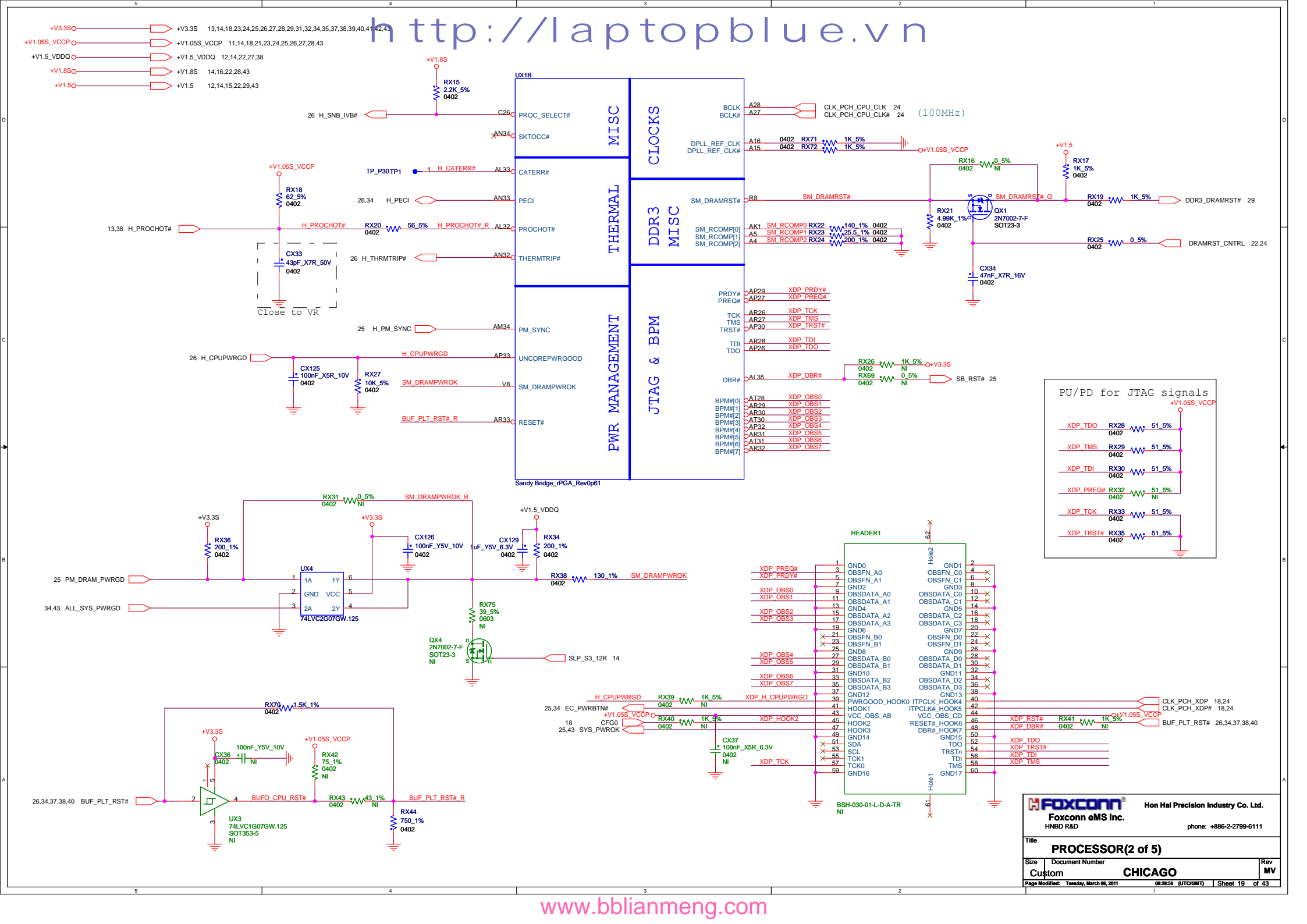
# +VCCSA POWER SUPPLY

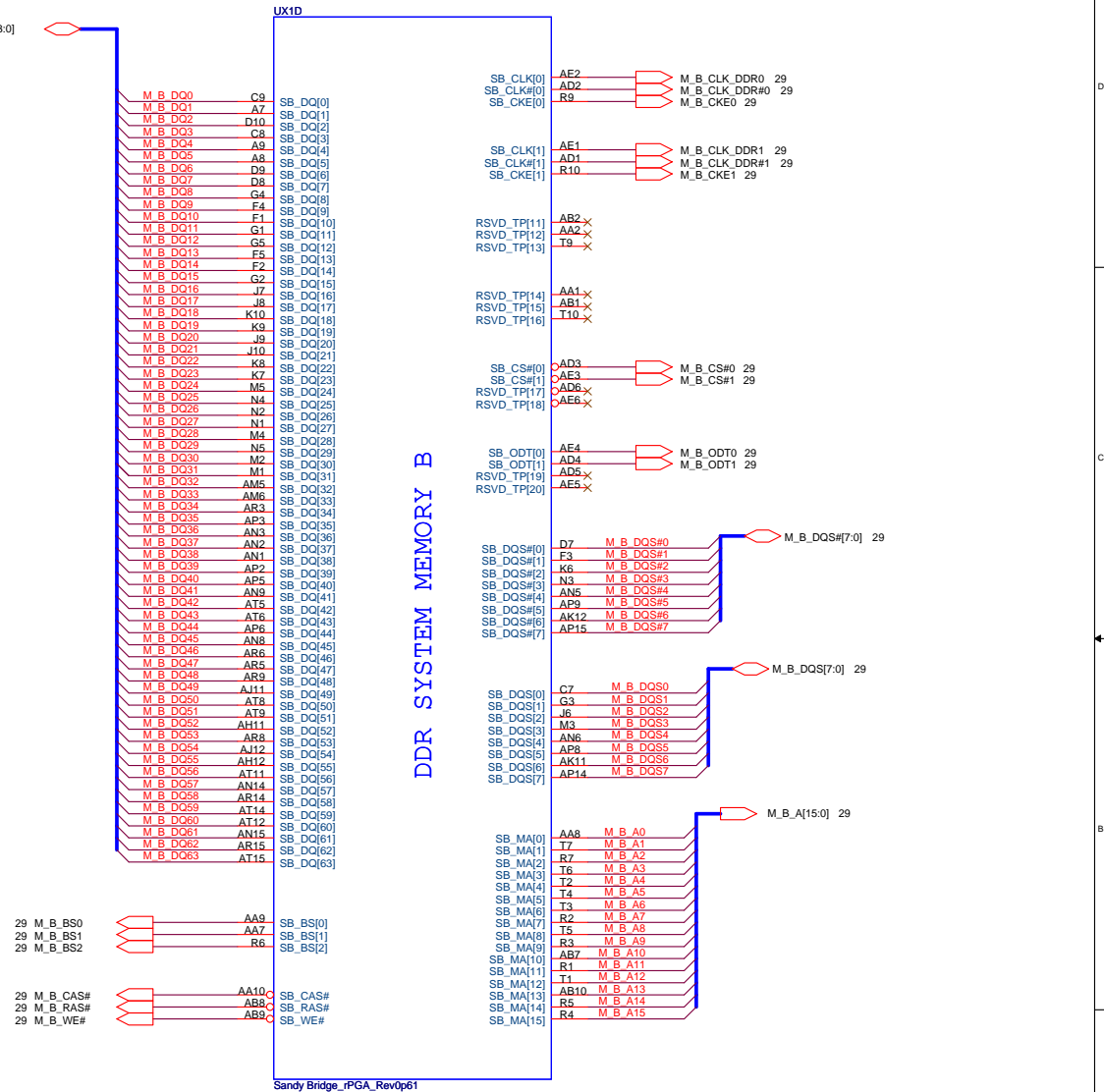
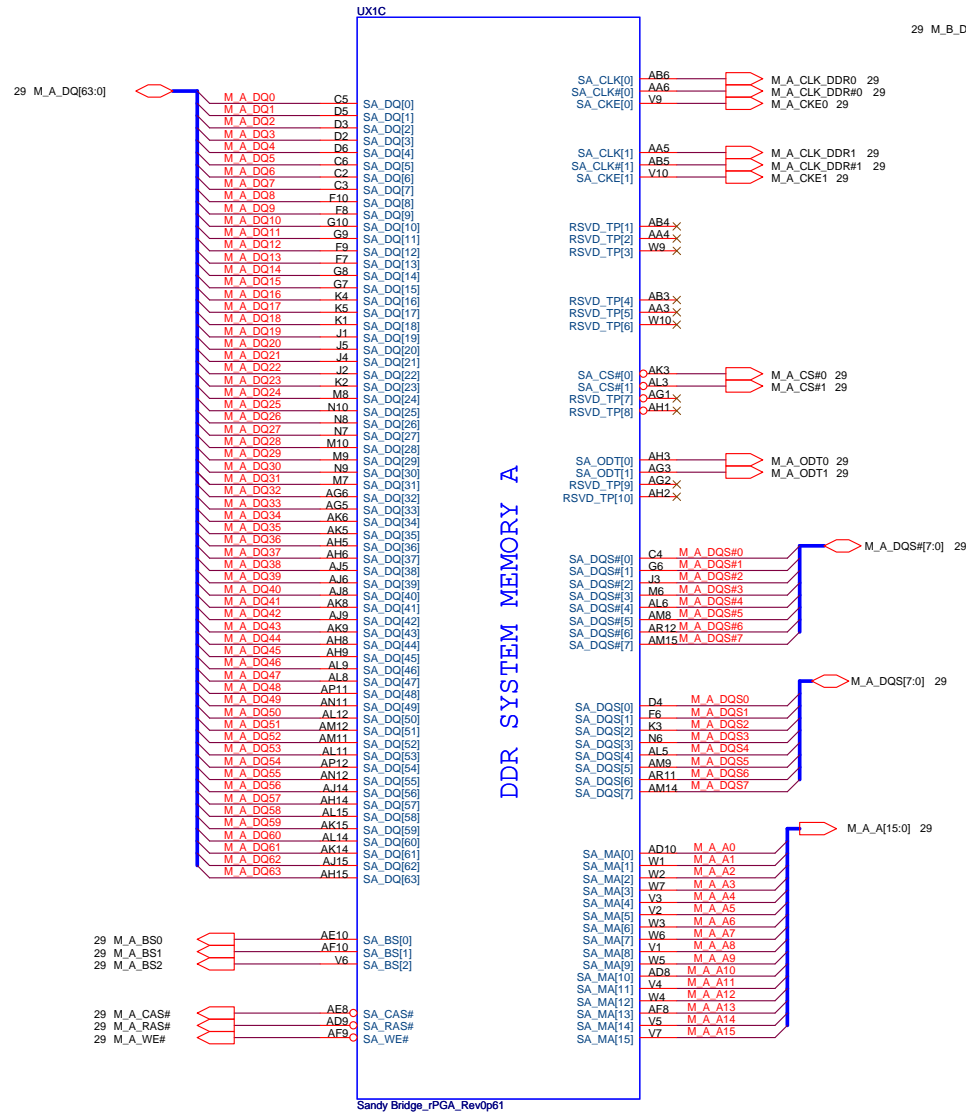
2010.1026.0



- +VCCSA:**
- 1. I/P Current:**  
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 2.18A$
  - 2. Ripple Current:**  
 $I_{rip} = 1.39A$
  - 3. Ripple Voltage:**  
 $ESR/4 = 1mohm$   
 $V_{rip} = 1.39mV$
  - 4. Inductor Spec:**  
 $I_{sat} = 26A$   
 $I_{dc} = 17.5A$   
 $DCR = 4.2mohm$
  - 5. MOSFET Spec:**
  - 6. Frequency:**  
 $F = 1MHz$  (R1705=Open)
  - 7. OCP:**  
Min : 6A / Typ : 7.5A

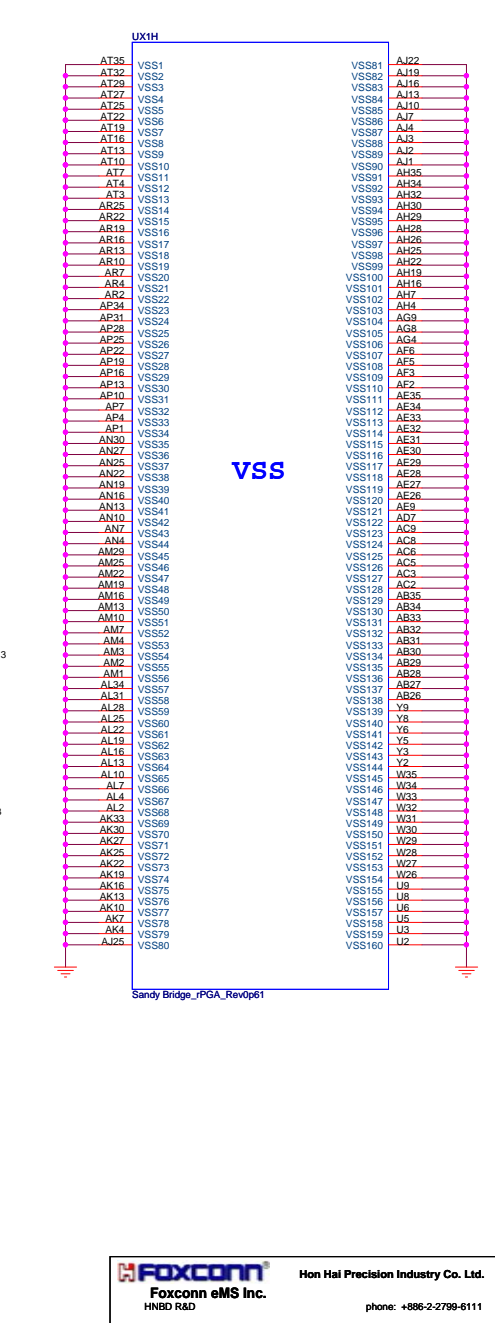
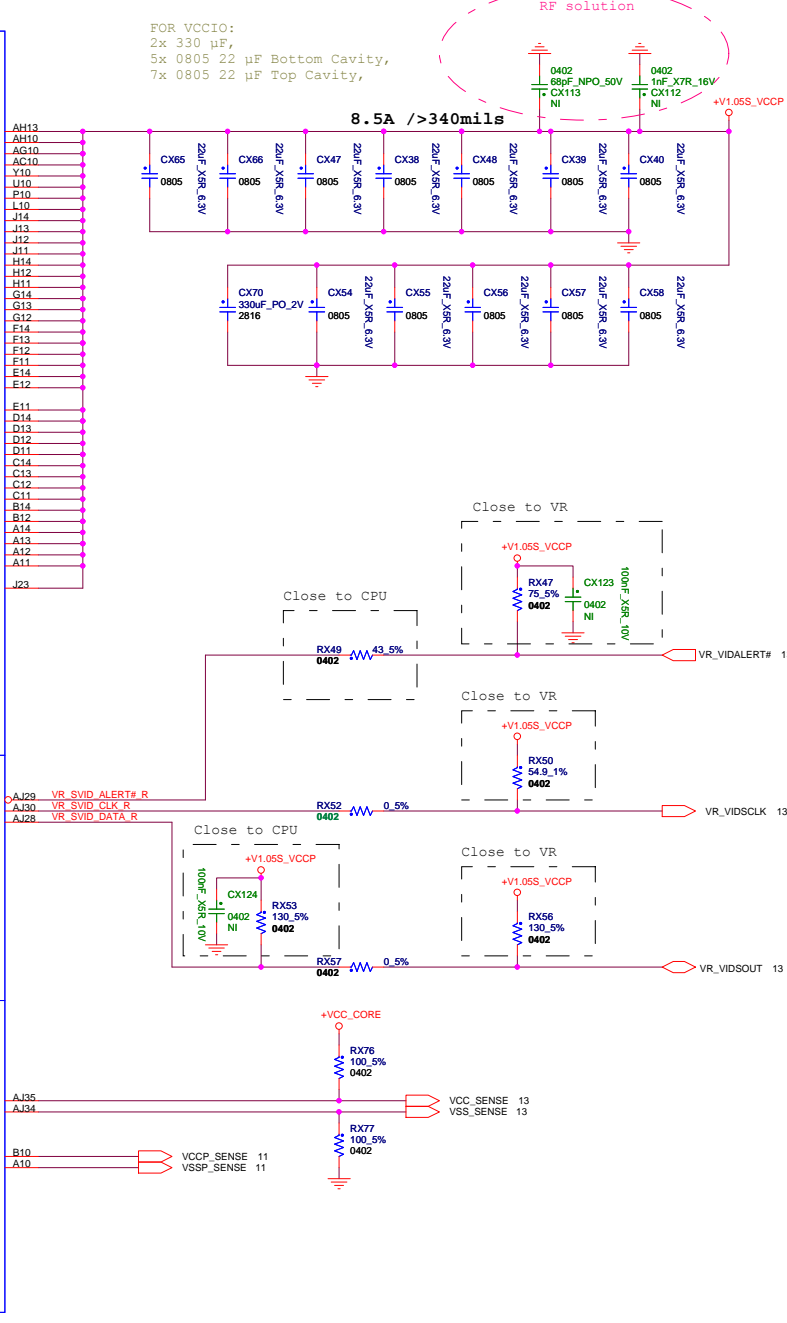
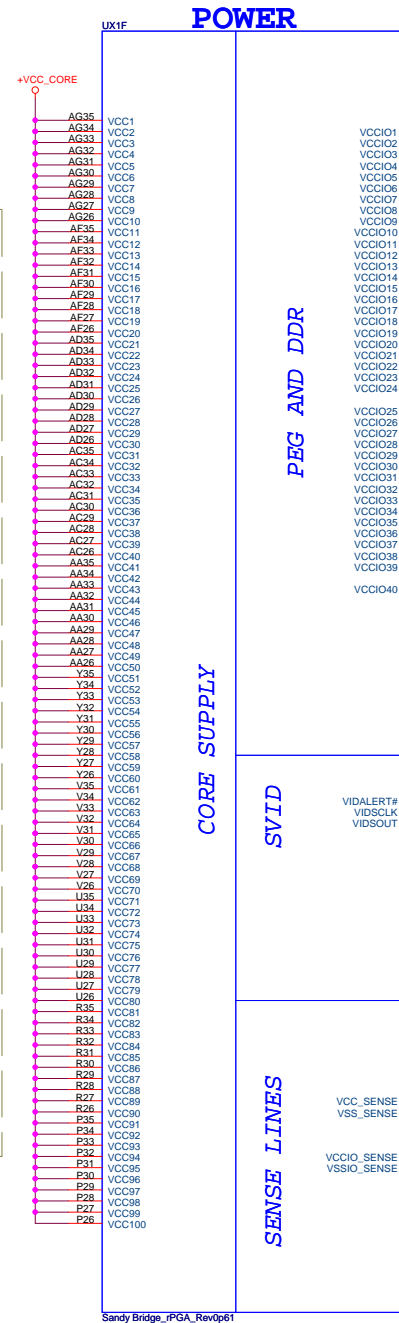
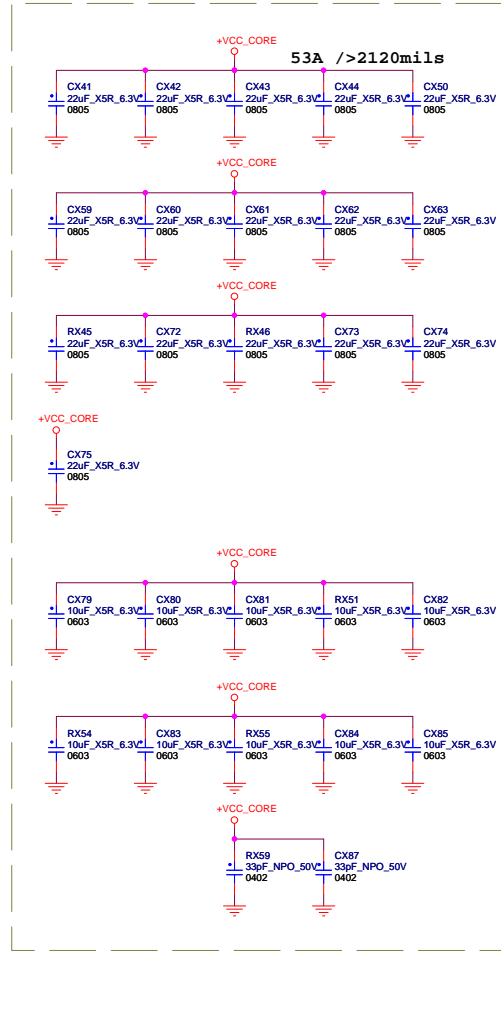


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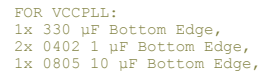


+V1.05S\_VCCP → +V1.05S\_VCCP 11,14,18,19,23,24,25,26,27,28,43  
 +VCC\_CORE → +VCC\_CORE 13,18,43

FOR VCC:  
 4x 330 µF Bottom Edge,  
 10x 0603 10 µF Bottom Cavity,  
 8x 0805 22 µF Top Cavity,  
 8x 0805 22 µF Top Edge,

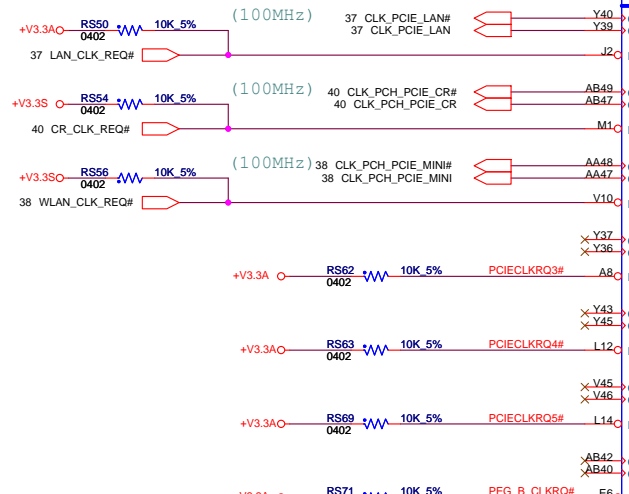
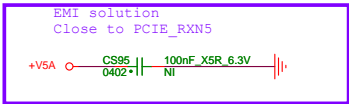
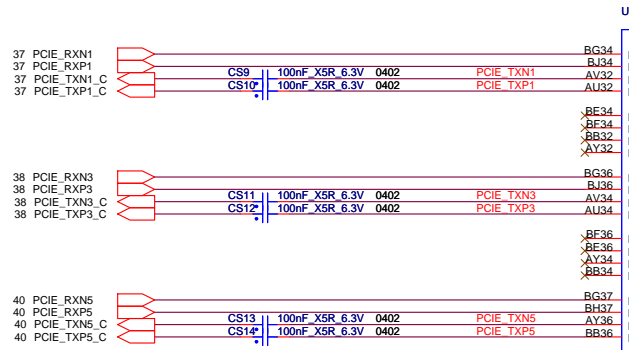


```
FOR VAXG:
2x 330  $\mu$ F Bottom Edge,
4x 0805 22  $\mu$ F Top & Bottom Cavity,
8x 0805 22  $\mu$ F Top & Bottom Edge,
```



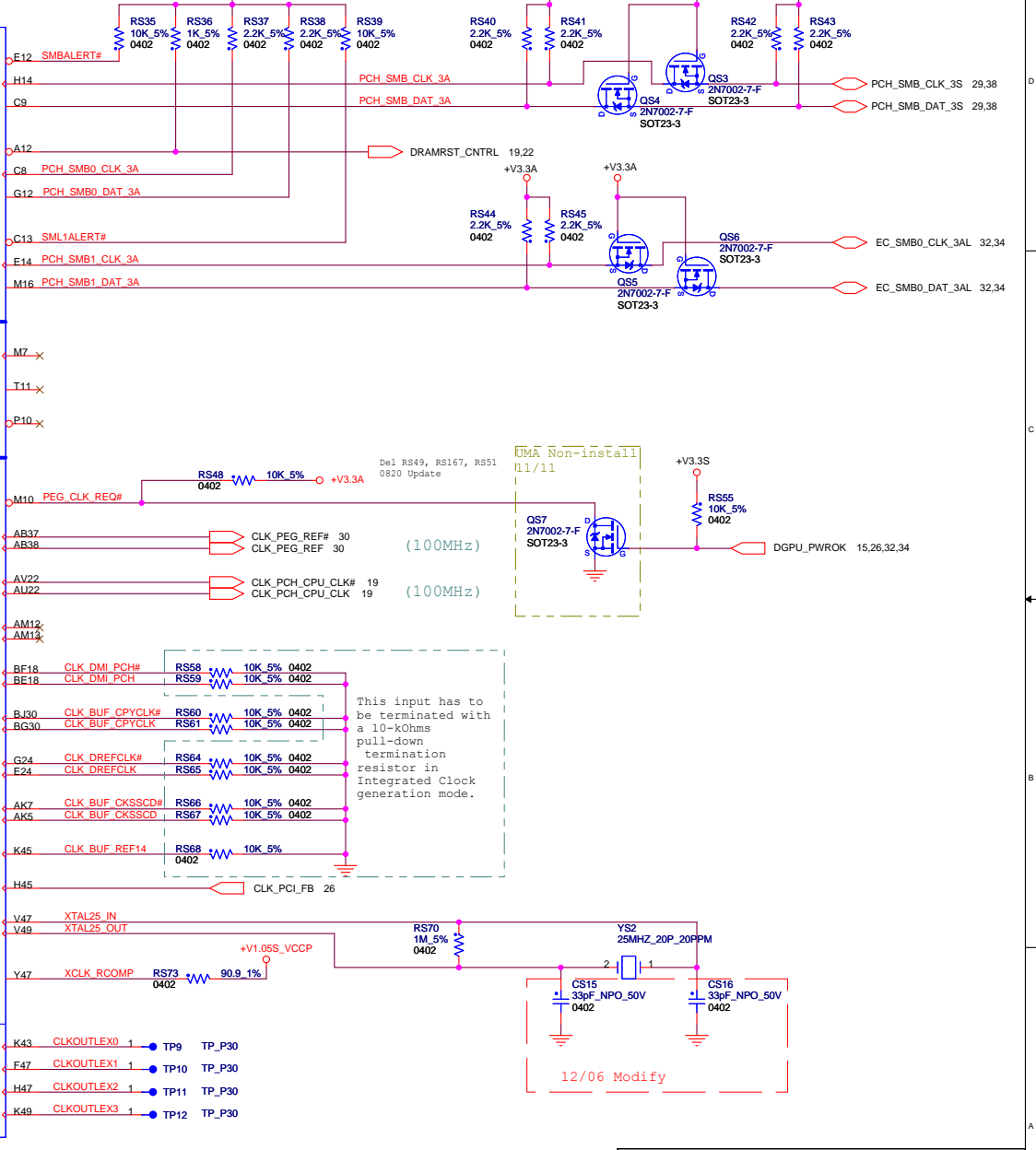
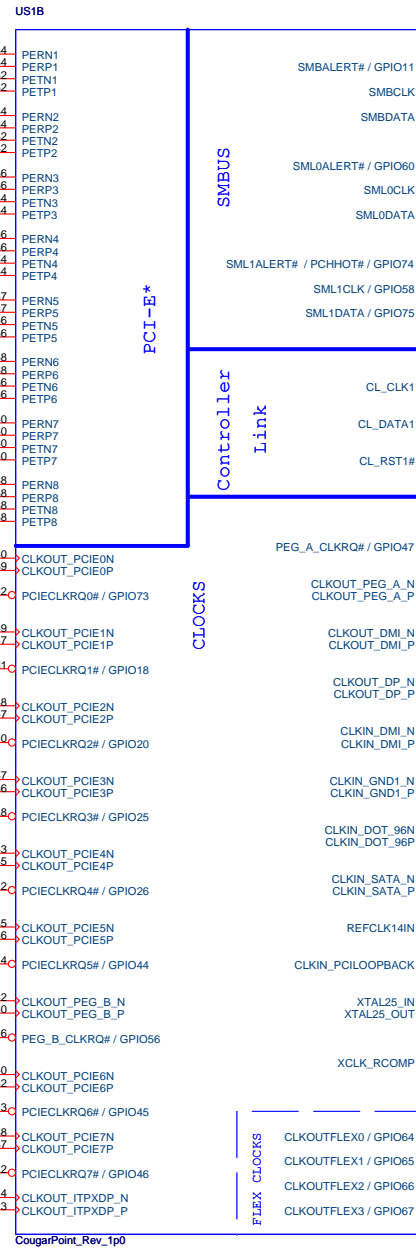






PCI-E Port Table

Port	Function
Port0	LAN
Port1	Card Reader
Port2	WLAN
Port3	Un-used
Port4	Un-used
Port5	Un-used
Port6	Un-used
Port7	Un-used



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US1C

FDI

DSWVRMEN

PM SLP SUS#

CougarPoint\_Rev\_1p0

System Power Management

12/06 Modify

Modify CS30/CS53/CS101 to non-stuff on 01/11

US1D

LVDS

CRT

CougarPoint\_Rev\_1p0

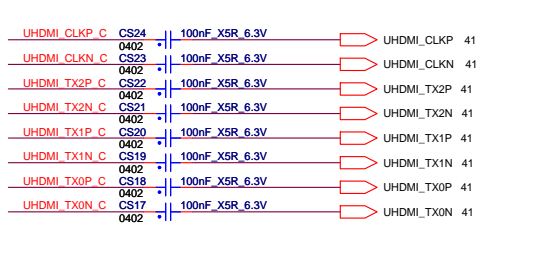
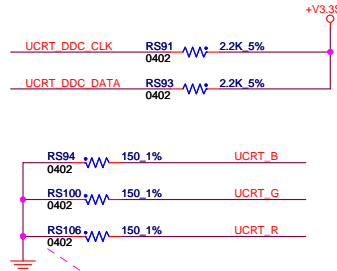
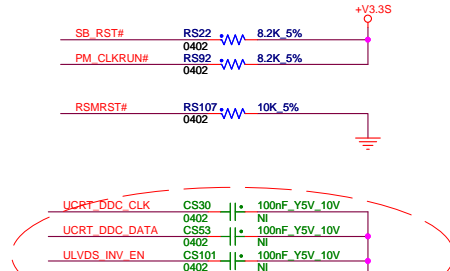
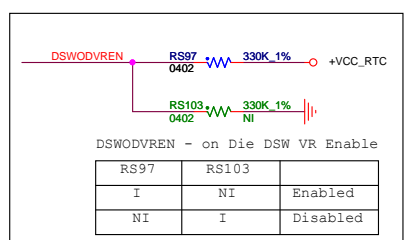
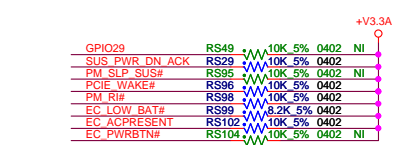
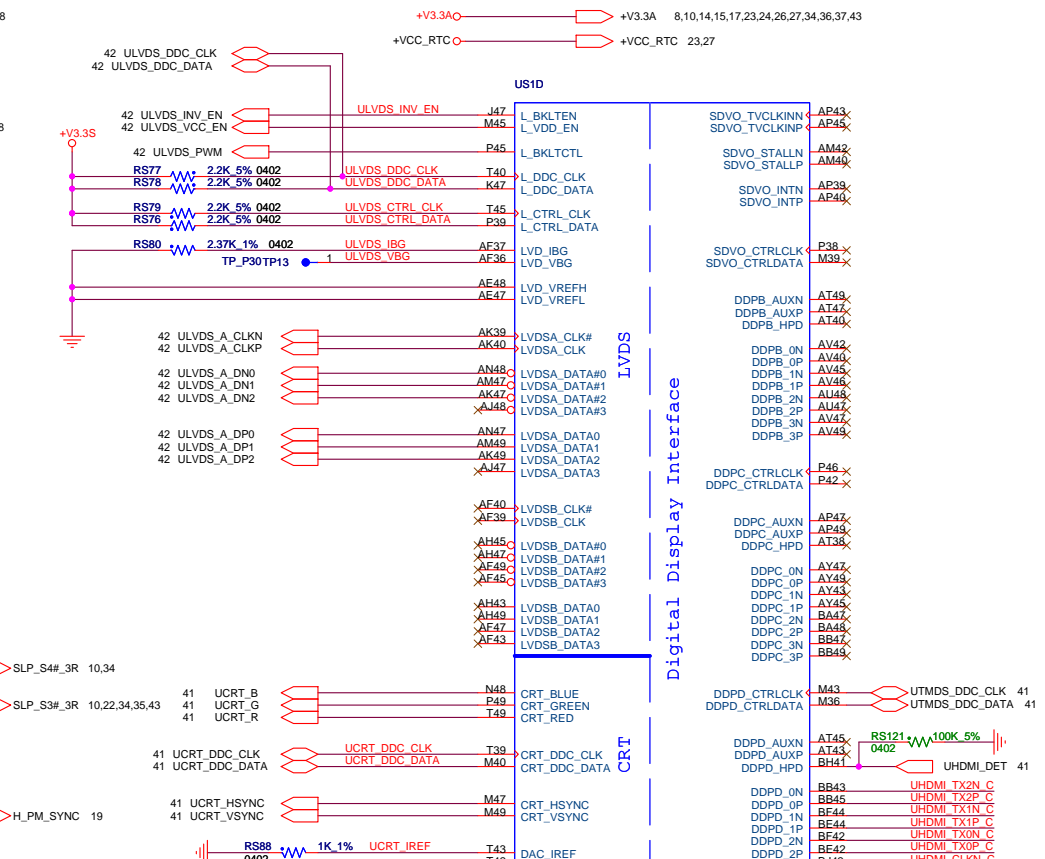
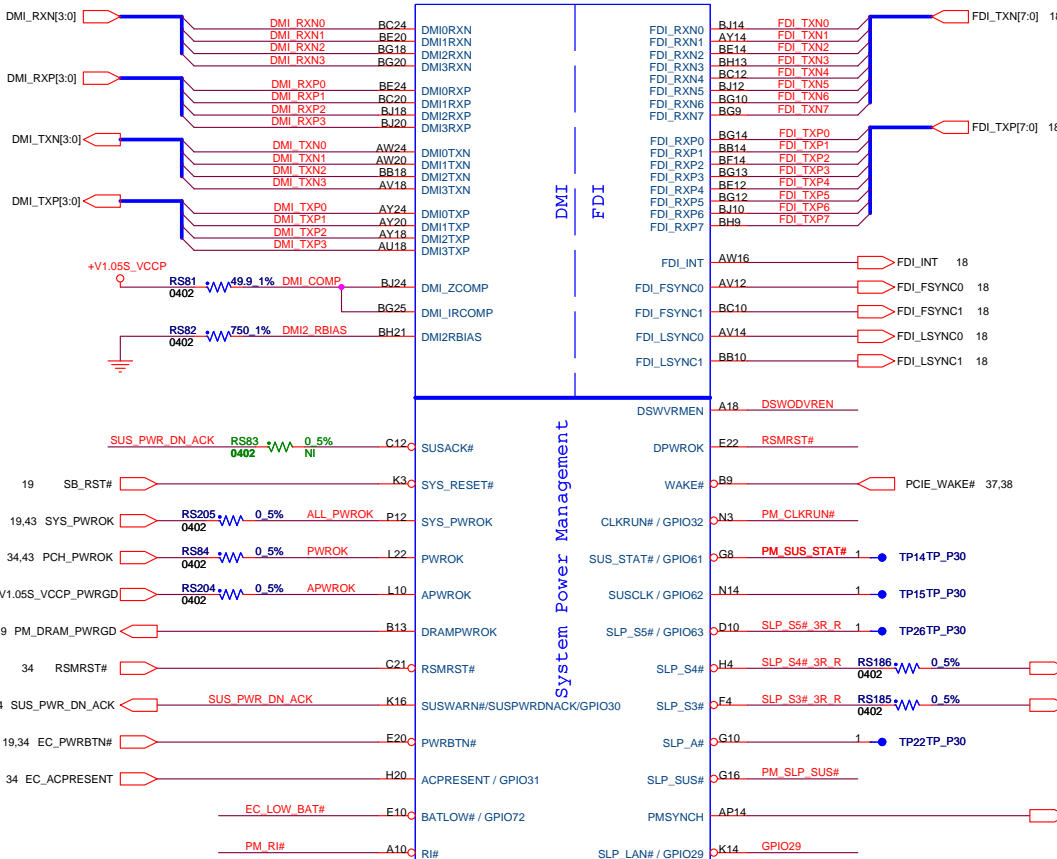
Digital Display Interface

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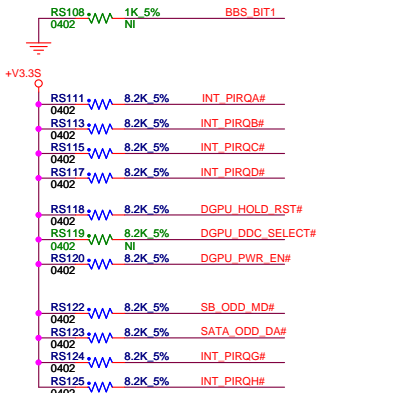
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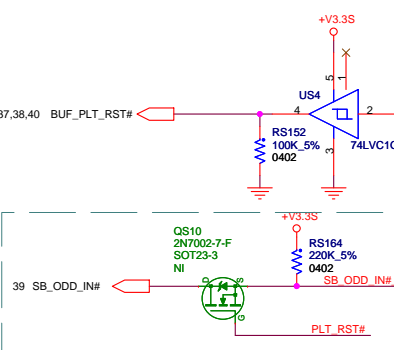
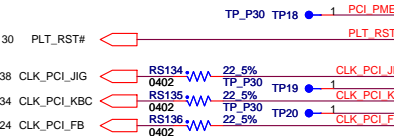
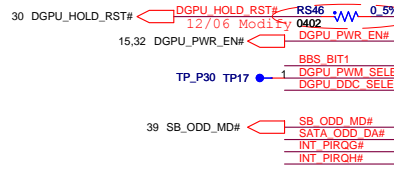
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Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



Del RS121 8.2Kohm to +V3.3S  
0820 Update



02/24 Modify same as the PV build

US1E

RSVD

PCI

USB

CougarPoint\_Rev\_1p0

PLTRST#

CLKOUT\_PCI0

CLKOUT\_PCI1

CLKOUT\_PCI2

CLKOUT\_PCI3

CLKOUT\_PCI4

OC0# / GPIO59

OC1# / GPIO40

OC2# / GPIO41

OC3# / GPIO42

OC4# / GPIO43

OC5# / GPIO8

OC6# / GPIO10

OC7# / GPIO14

OC8# / GPIO9

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OC229# / GPIO10

OC230# / GPIO10

OC231# / GPIO10

OC232# / GPIO10

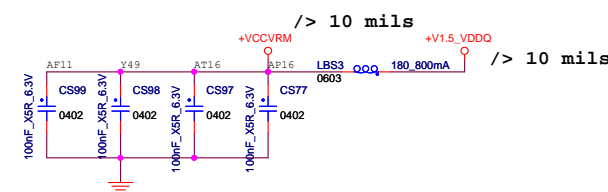
OC233# / GPIO10

OC234# / GPIO10

OC235# / GPIO10

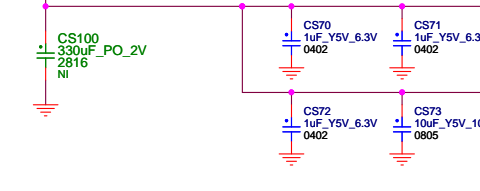
OC236# / GPIO10

OC237# / GPIO10

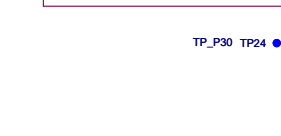


US11		
AY4	VSS[159]	VSS[269]
AY42	VSS[160]	VSS[260]
AY46	VSS[161]	VSS[261]
AY8	VSS[162]	VSS[262]
B11	VSS[163]	VSS[263]
B15	VSS[164]	VSS[264]
B19	VSS[165]	VSS[265]
B23	VSS[166]	VSS[266]
B27	VSS[167]	VSS[267]
B31	VSS[168]	VSS[268]
B35	VSS[169]	VSS[269]
B39	VSS[170]	VSS[270]
B7	VSS[171]	VSS[271]
F45	VSS[172]	VSS[272]
BB12	VSS[173]	VSS[273]
BB16	VSS[174]	VSS[274]
BB20	VSS[175]	VSS[275]
BB22	VSS[176]	VSS[276]
BB24	VSS[177]	VSS[277]
BB28	VSS[178]	VSS[278]
BB30	VSS[179]	VSS[279]
BB38	VSS[180]	VSS[280]
BB4	VSS[181]	VSS[281]
BB46	VSS[182]	VSS[282]
BC14	VSS[183]	VSS[283]
BC18	VSS[184]	VSS[284]
BC22	VSS[185]	VSS[285]
BC26	VSS[186]	VSS[286]
BC32	VSS[187]	VSS[287]
BC34	VSS[188]	VSS[288]
BC36	VSS[189]	VSS[289]
BC40	VSS[190]	VSS[290]
BC42	VSS[191]	VSS[291]
BC48	VSS[192]	VSS[292]
BD46	VSS[193]	VSS[293]
BD5	VSS[194]	VSS[294]
BE22	VSS[195]	VSS[295]
BE26	VSS[196]	VSS[296]
BE40	VSS[197]	VSS[297]
BE10	VSS[198]	VSS[298]
BE12	VSS[199]	VSS[299]
BE16	VSS[200]	VSS[300]
BE20	VSS[201]	VSS[301]
BE24	VSS[202]	VSS[302]
BE28	VSS[203]	VSS[303]
BE30	VSS[204]	VSS[304]
BE38	VSS[205]	VSS[305]
BF40	VSS[206]	VSS[306]
BF8	VSS[207]	VSS[307]
BF16	VSS[208]	VSS[308]
BF20	VSS[209]	VSS[309]
BF24	VSS[210]	VSS[310]
BF28	VSS[211]	VSS[311]
BF30	VSS[212]	VSS[312]
BF32	VSS[213]	VSS[313]
BF34	VSS[214]	VSS[314]
BF38	VSS[215]	VSS[315]
BH11	VSS[216]	VSS[316]
BH15	VSS[217]	VSS[317]
BH17	VSS[218]	VSS[318]
BH19	VSS[219]	VSS[319]
BH20	VSS[220]	VSS[320]
BH22	VSS[221]	VSS[321]
BH31	VSS[222]	VSS[322]
BH33	VSS[223]	VSS[323]
BH35	VSS[224]	VSS[324]
BH39	VSS[225]	VSS[325]
BH43	VSS[226]	VSS[326]
BH7	VSS[227]	VSS[327]
D3	VSS[228]	VSS[328]
D12	VSS[229]	VSS[329]
D16	VSS[230]	VSS[330]
D18	VSS[231]	VSS[331]
D22	VSS[232]	VSS[332]
D24	VSS[233]	VSS[333]
D26	VSS[234]	VSS[334]
D30	VSS[235]	VSS[335]
D32	VSS[236]	VSS[336]
D34	VSS[237]	VSS[337]
D38	VSS[238]	VSS[338]
D42	VSS[239]	VSS[339]
D8	VSS[240]	VSS[340]
E18	VSS[241]	VSS[341]
E26	VSS[242]	VSS[342]
G18	VSS[243]	VSS[343]
G20	VSS[244]	VSS[344]
G26	VSS[245]	VSS[345]
G28	VSS[246]	VSS[346]
G36	VSS[247]	VSS[347]
G48	VSS[248]	VSS[348]
H12	VSS[249]	VSS[349]
H18	VSS[250]	VSS[350]
H22	VSS[251]	VSS[351]
H24	VSS[252]	VSS[352]
H26	VSS[253]	
H30	VSS[254]	
H32	VSS[255]	
H34	VSS[256]	
F3	VSS[257]	
	VSS[258]	

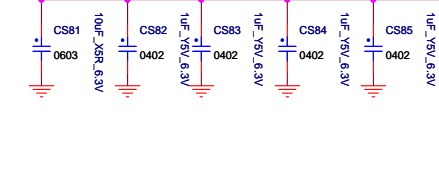
1300mA />52mils



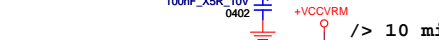
20mA />5mils



2925mA />240mils



50mA />10mils



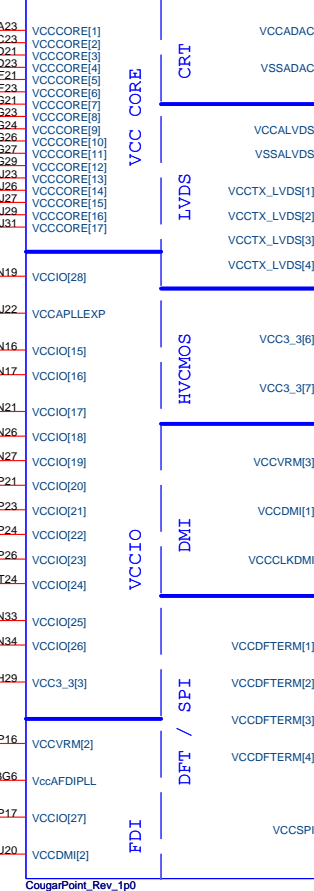
>10mils



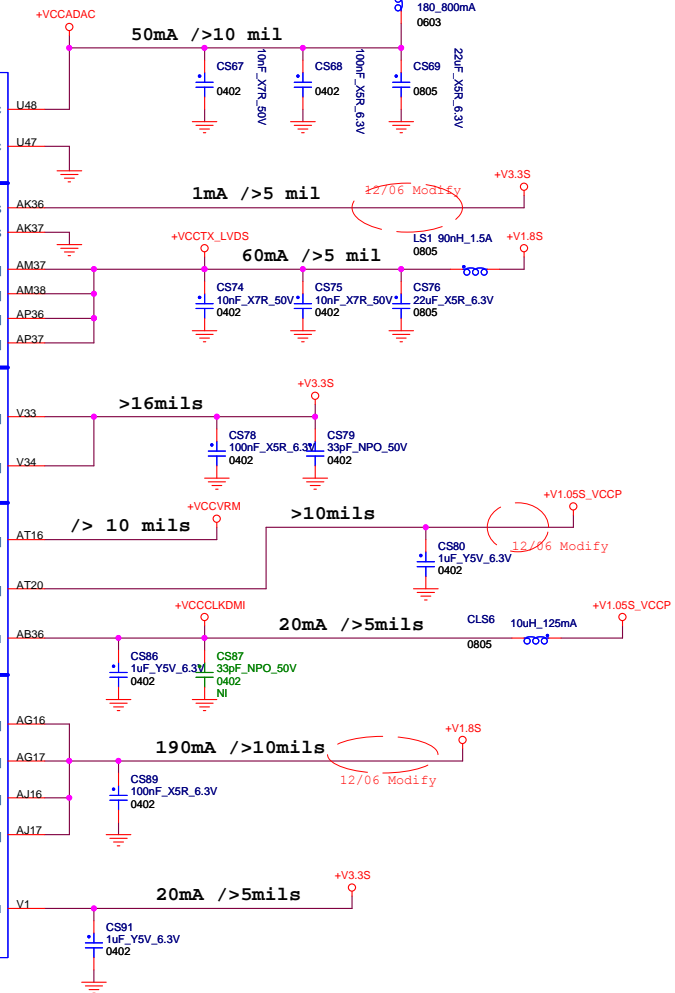
>10mils

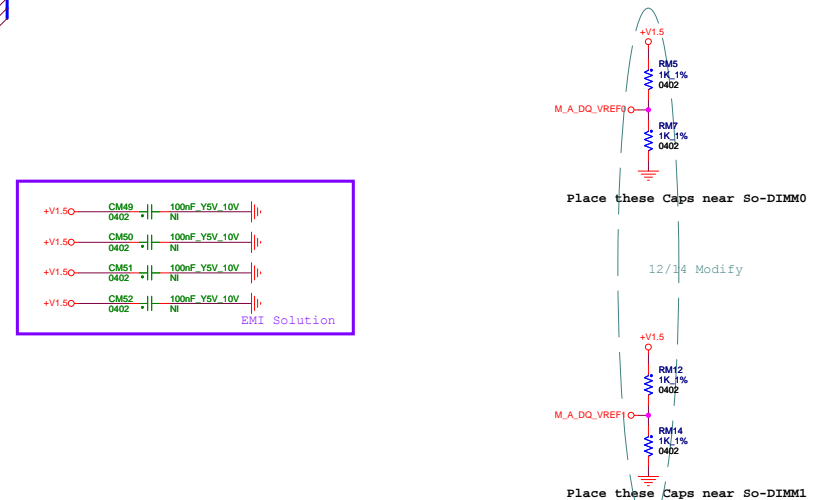
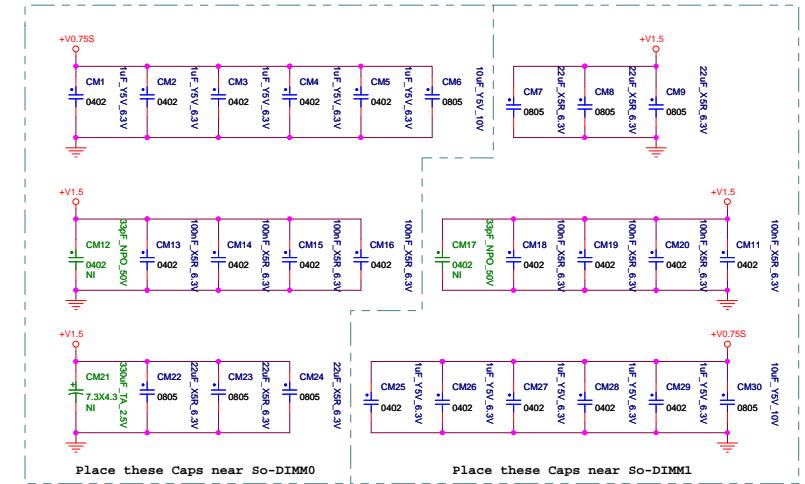


## POWER

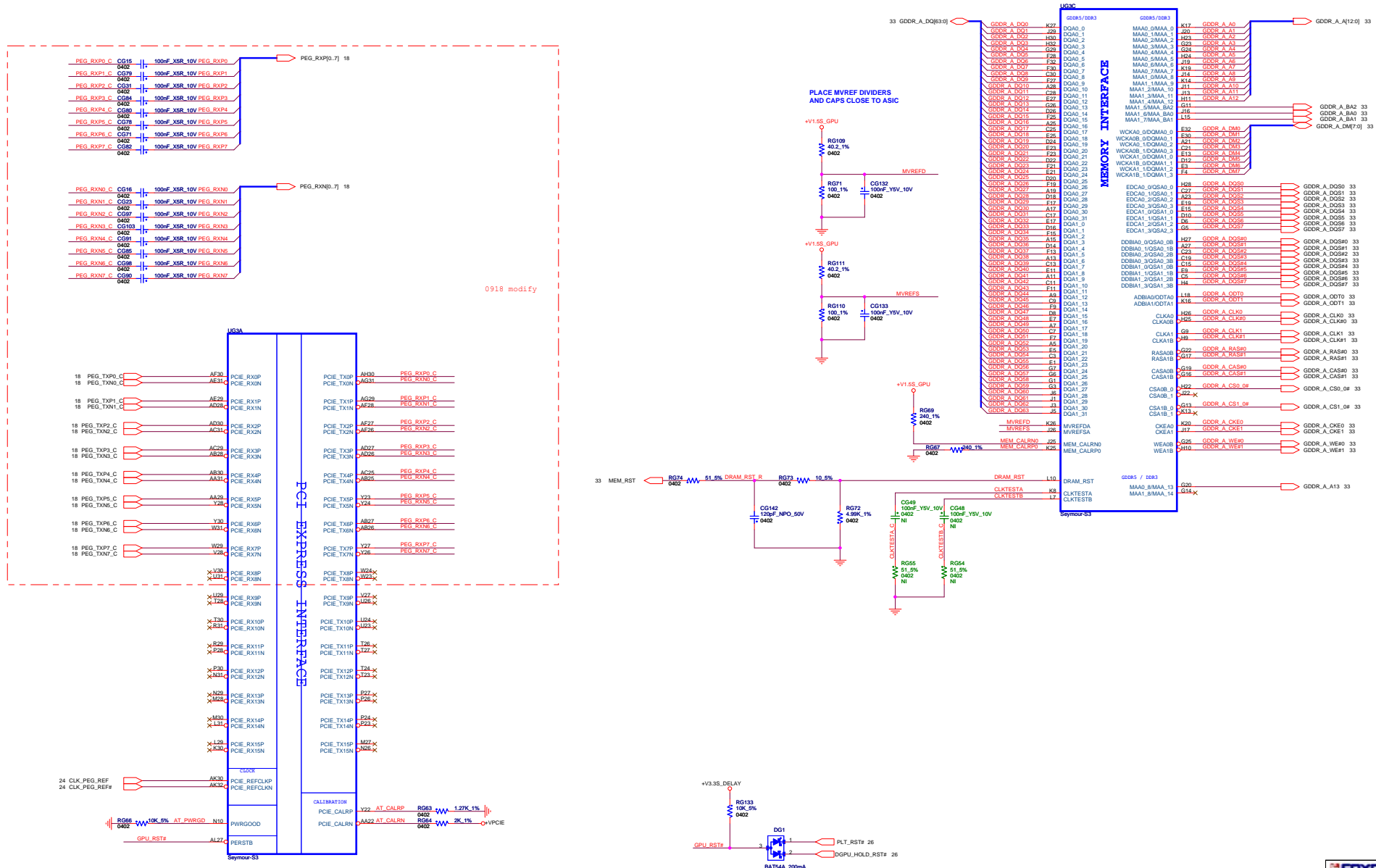


CougarPoint\_Rev\_1p0

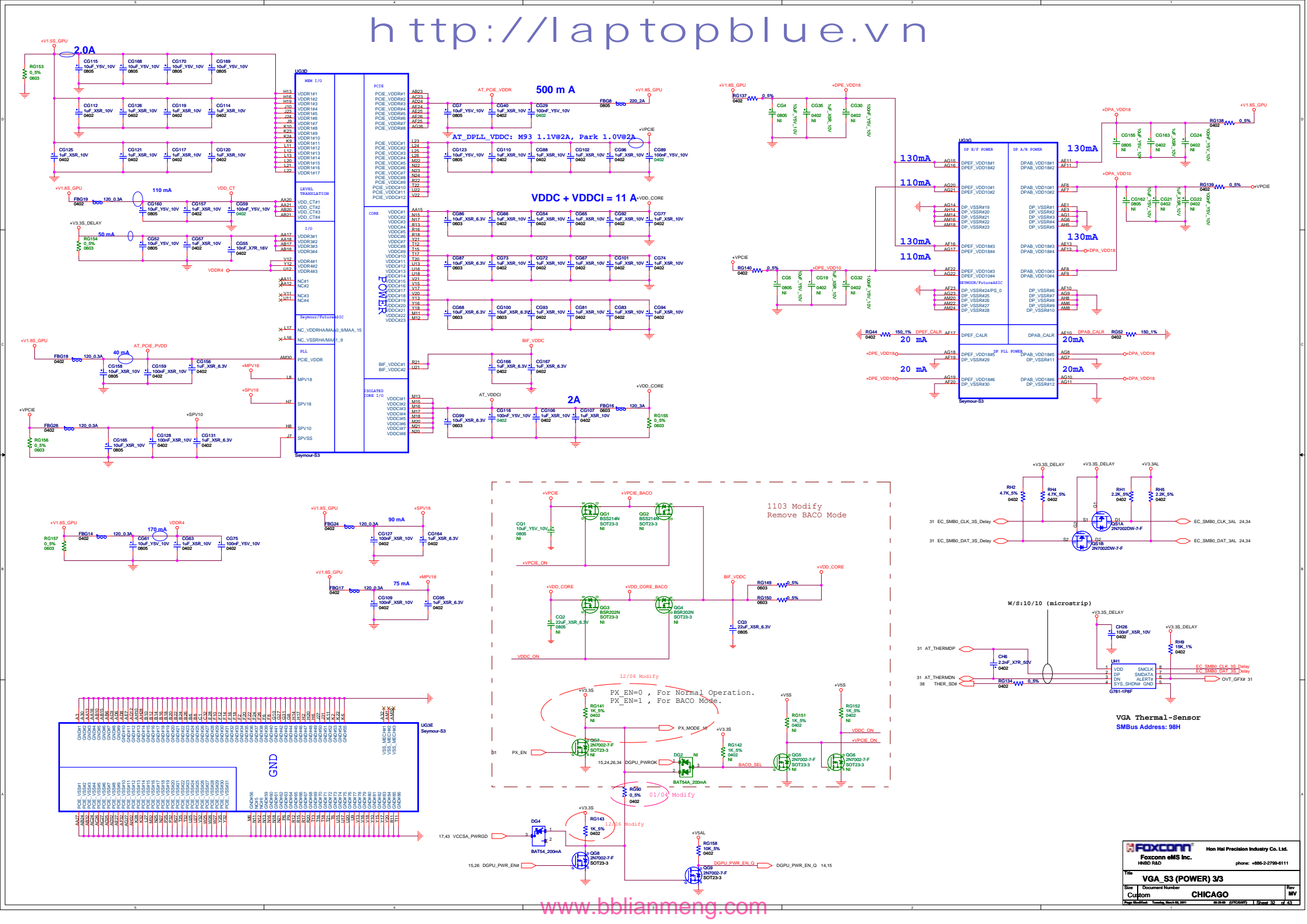




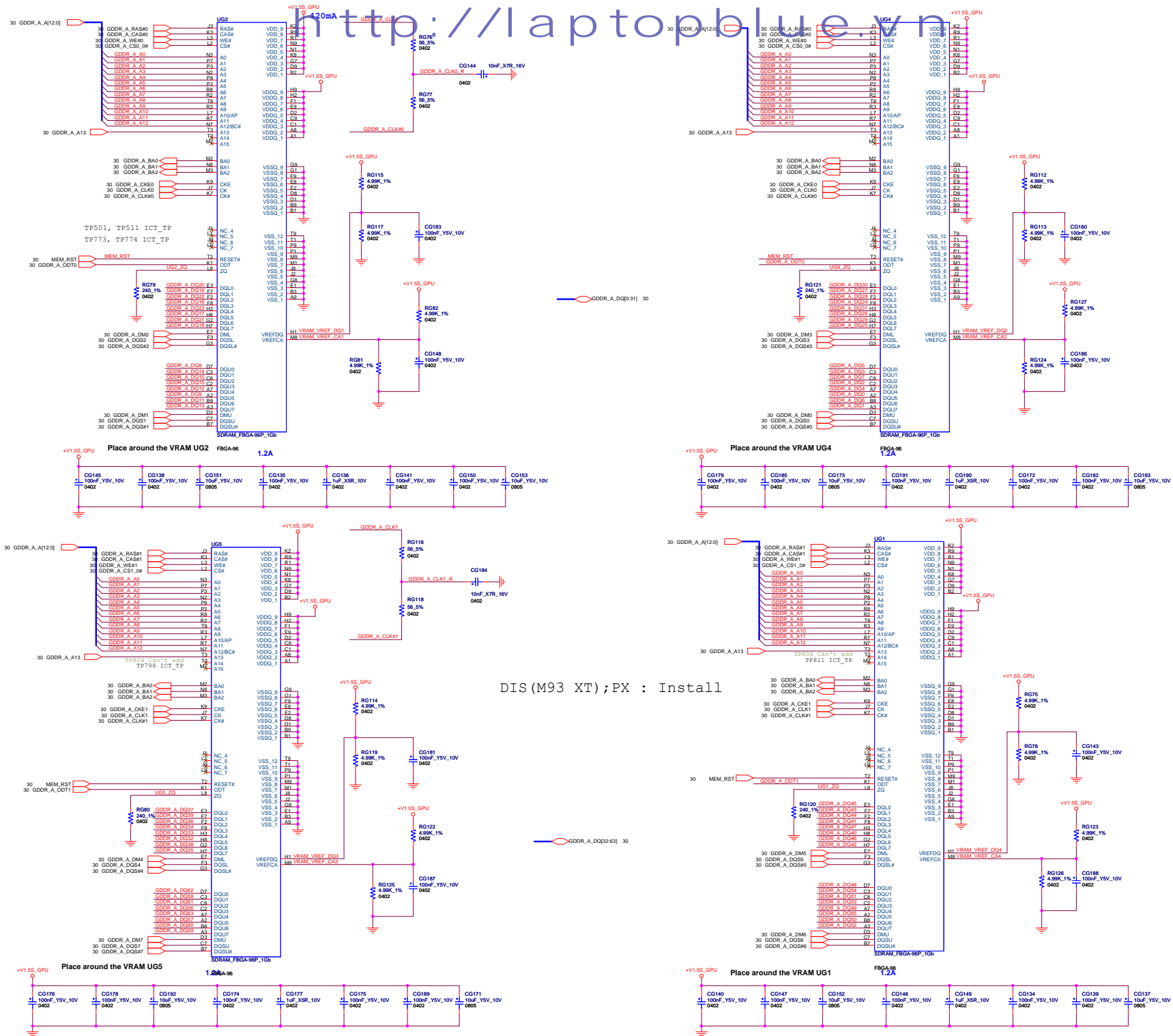


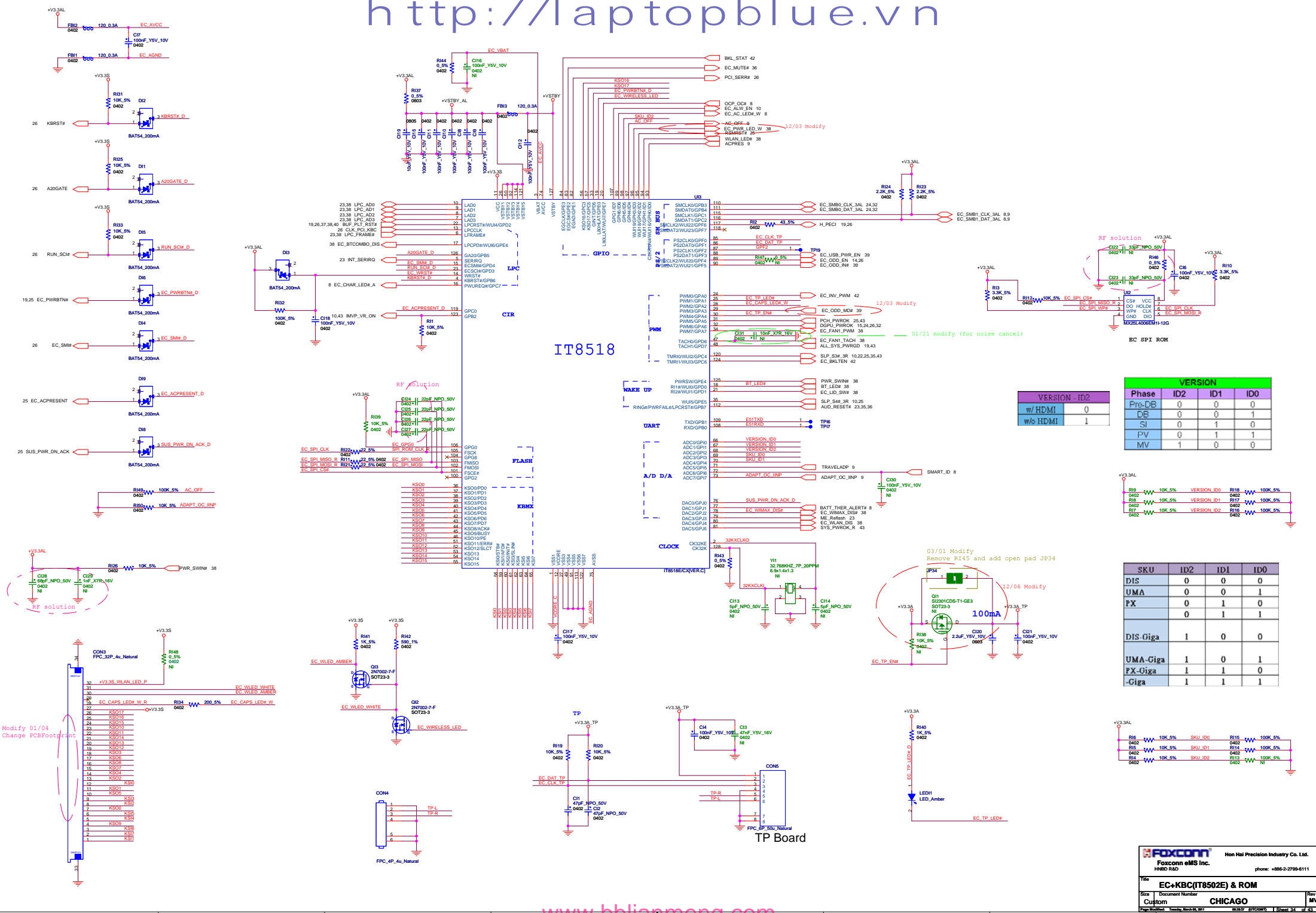












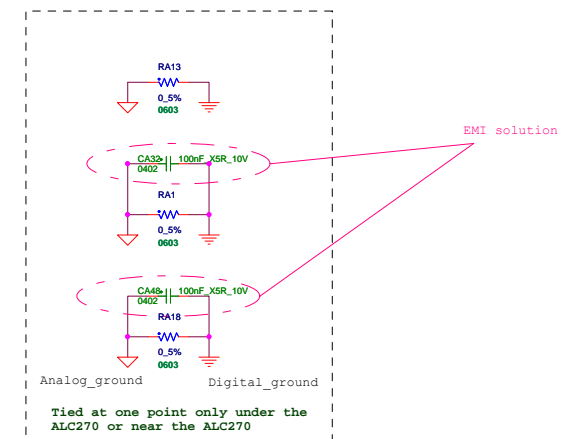
IT5518

VERSION	ID2
w/ HDMI	0
w/o HDMI	1

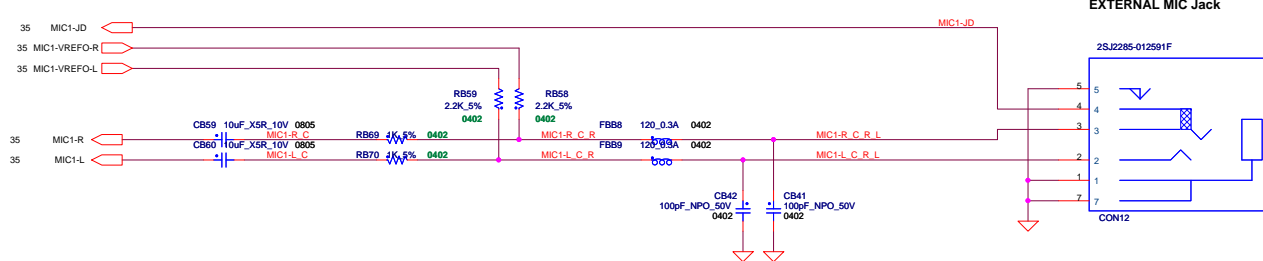
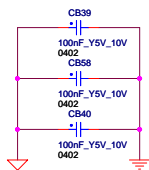
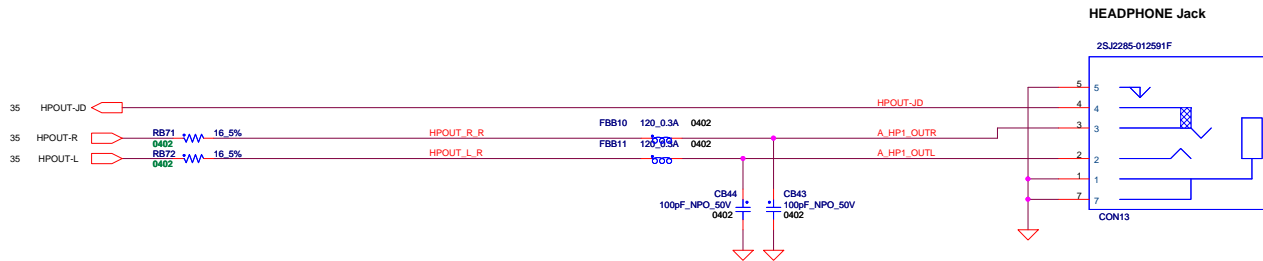
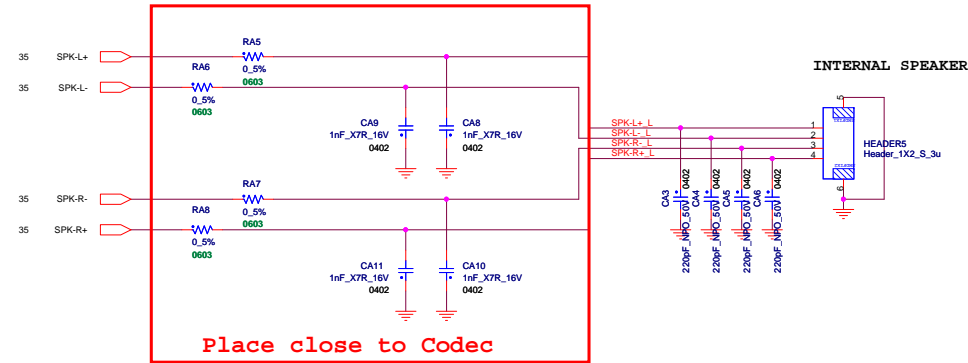
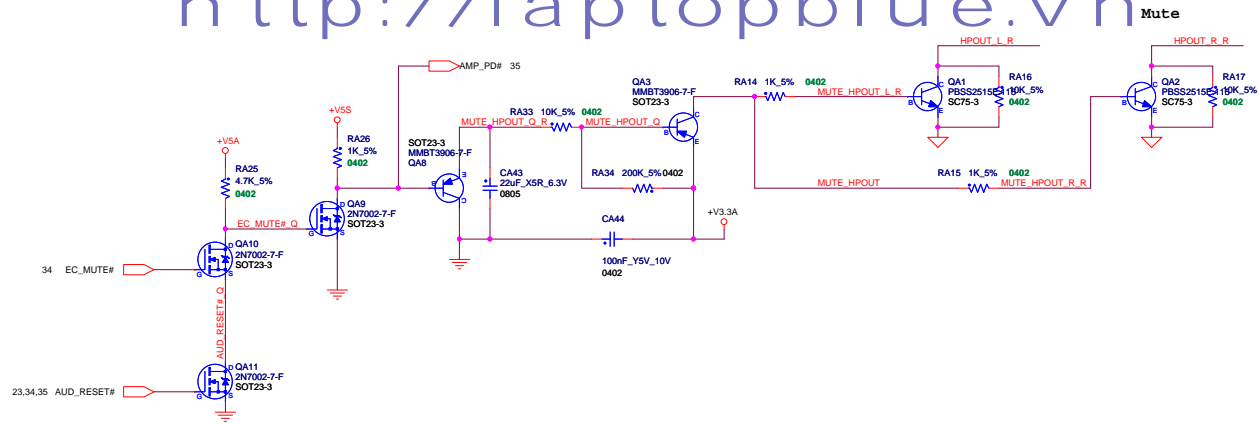
VERSION				
Phase	ID2	ID1	ID0	
Pre-DB	0	0	0	
DB	0	0	1	
SI	0	1	0	
PV	0	1	1	
MV	1	0	0	

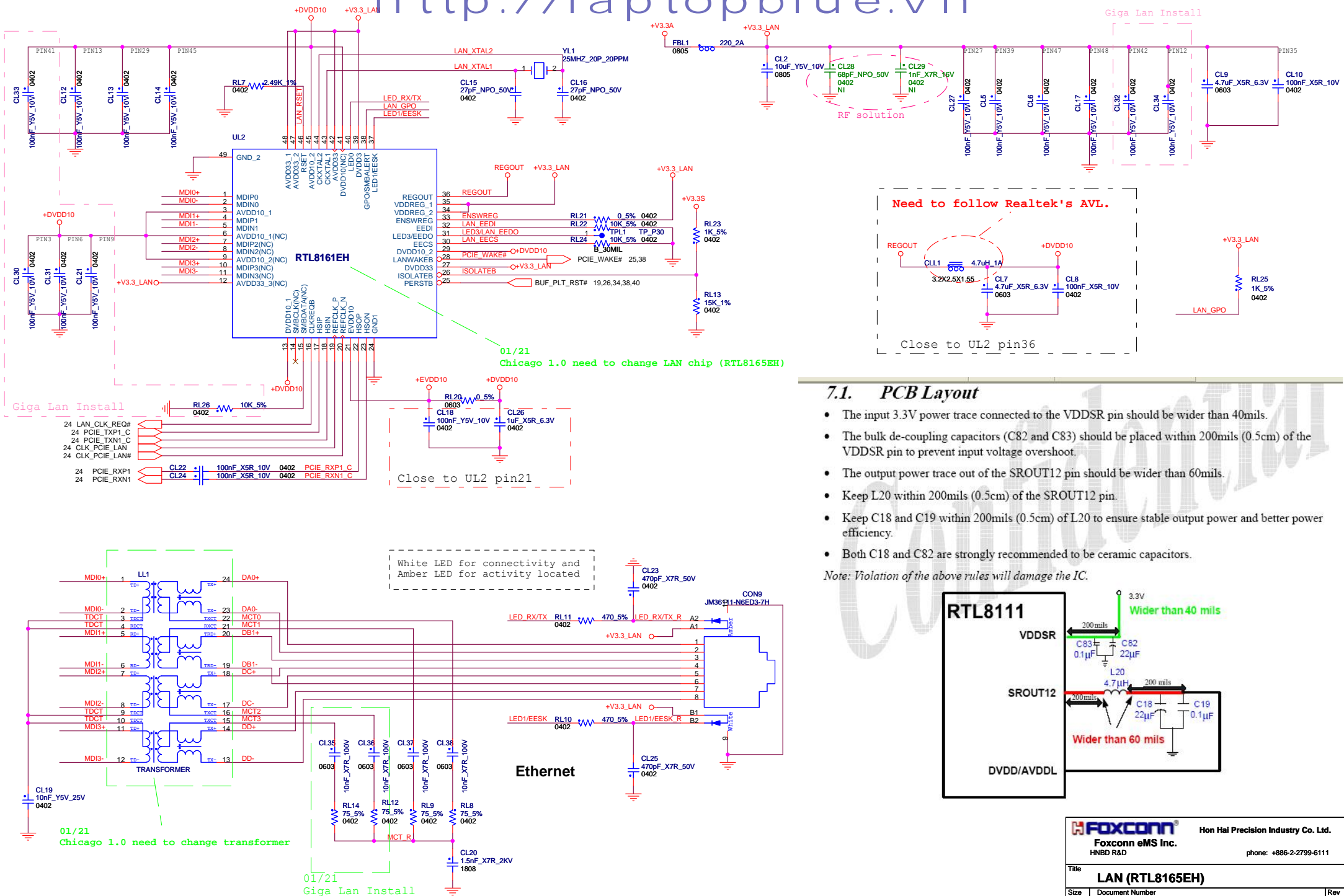
SKU	ID2	ID1	ID0
DIS	0	0	0
UMA	0	0	1
PX	0	1	0
	0	1	1
DIS Giga	1	0	0
UMA-Giga	1	0	1
PX-Giga	1	1	0
-Giga	1	1	1

Modify 01/04  
Change PCB Footprint



```
<<Attention>>
For power_on/off de-pop circuit and system booting warning
signal: Please System BIOS Engineer Note :
1. If you want the system make warning signal after power on
, please let EC_MUTE# High first.
2. When you want to exit your Bios Programming Code, please let
the EC_MUTE# Low. (The programming is different from before. )
```

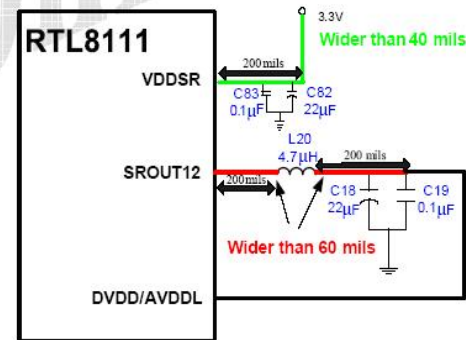


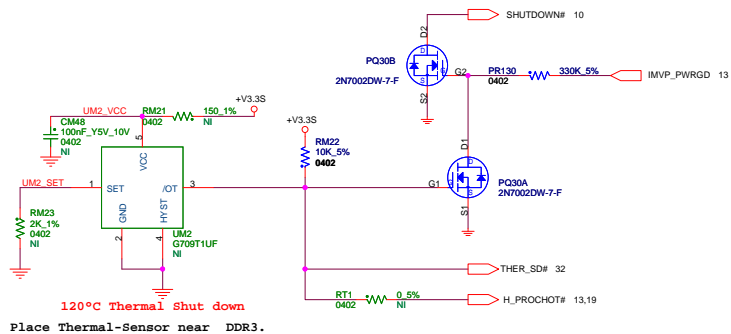
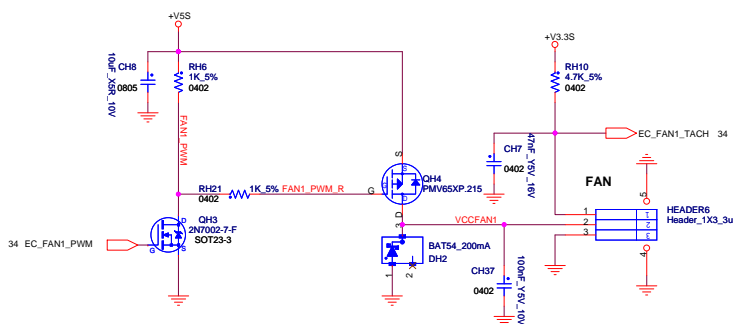
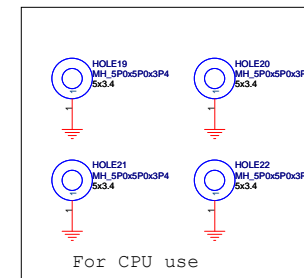
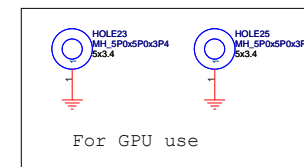
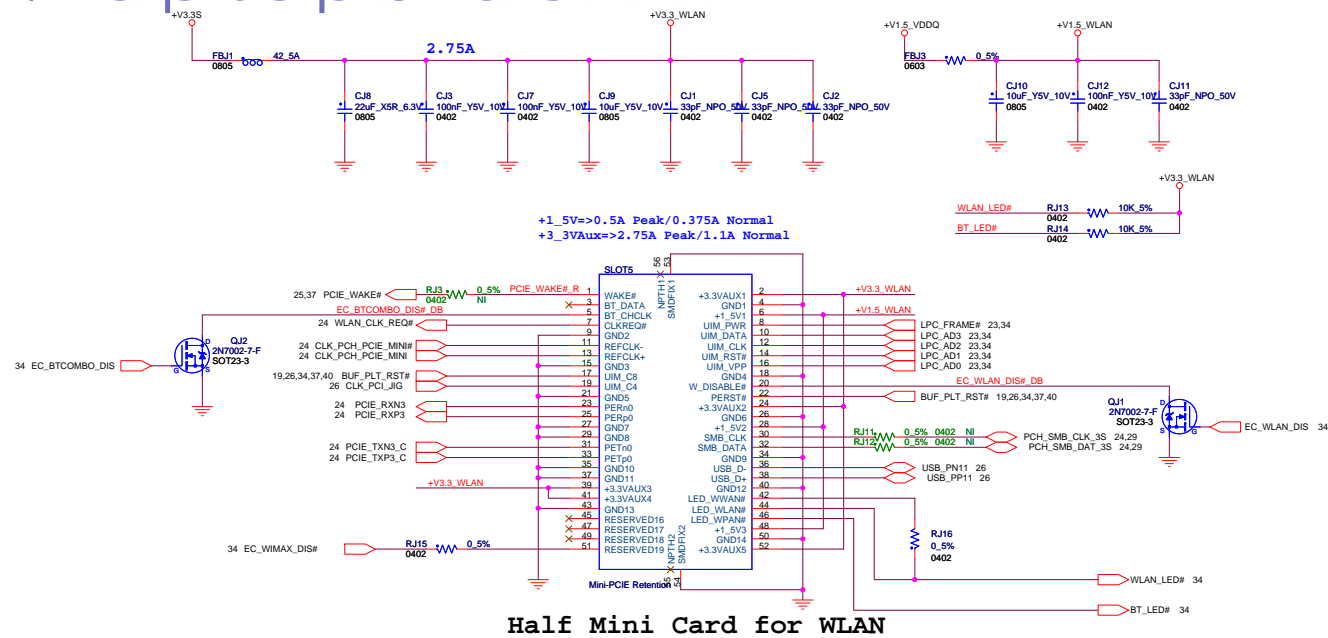


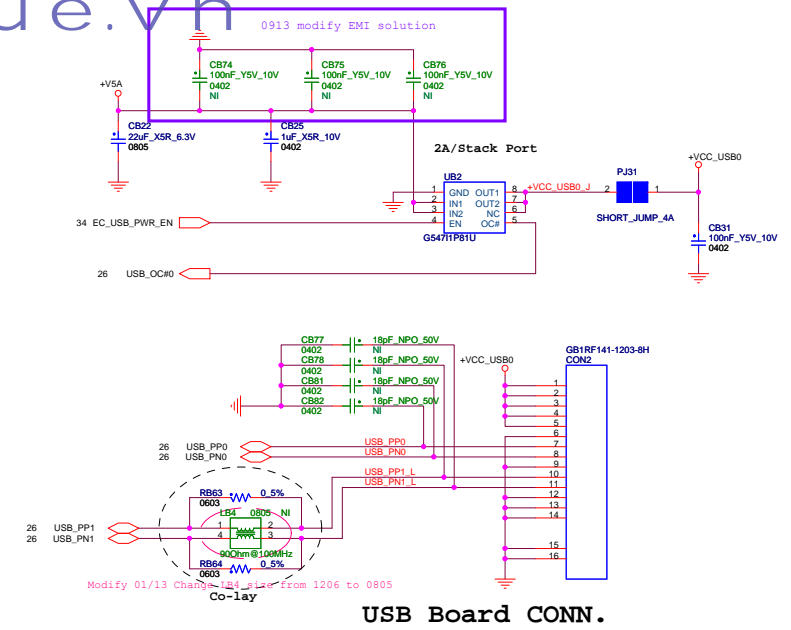
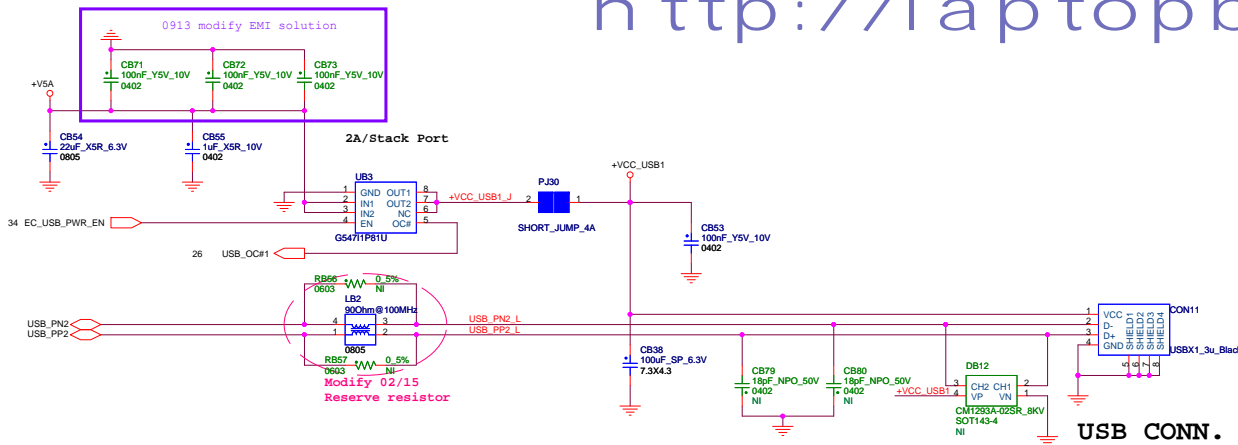
### 7.1. PCB Layout

- The input 3.3V power trace connected to the VDDSR pin should be wider than 40mils.
- The bulk de-coupling capacitors (C82 and C83) should be placed within 200mils (0.5cm) of the VDDSR pin to prevent input voltage overshoot.
- The output power trace out of the SROUT12 pin should be wider than 60mils.
- Keep L20 within 200mils (0.5cm) of the SROUT12 pin.
- Keep C18 and C19 within 200mils (0.5cm) of L20 to ensure stable output power and better power efficiency.
- Both C18 and C82 are strongly recommended to be ceramic capacitors.

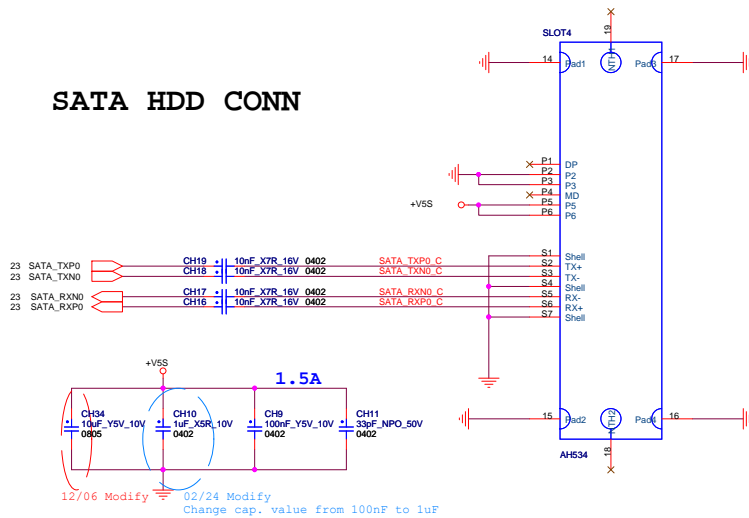
*Note: Violation of the above rules will damage the IC.*



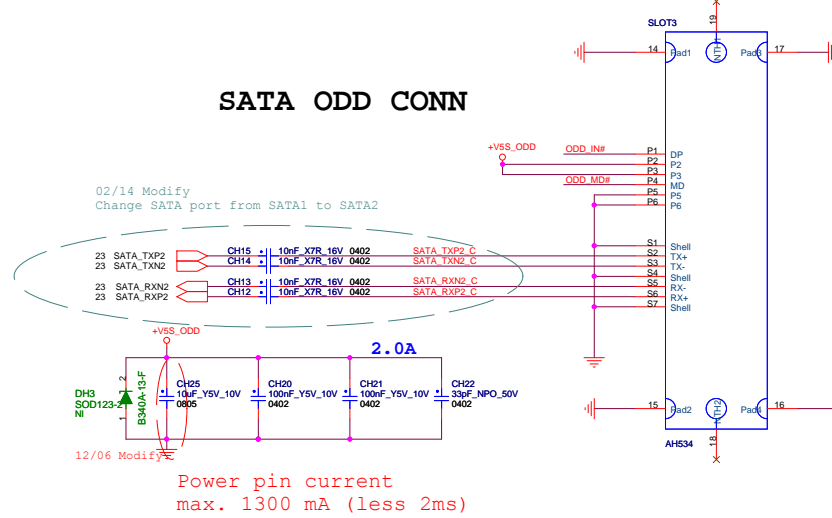
[illegible]



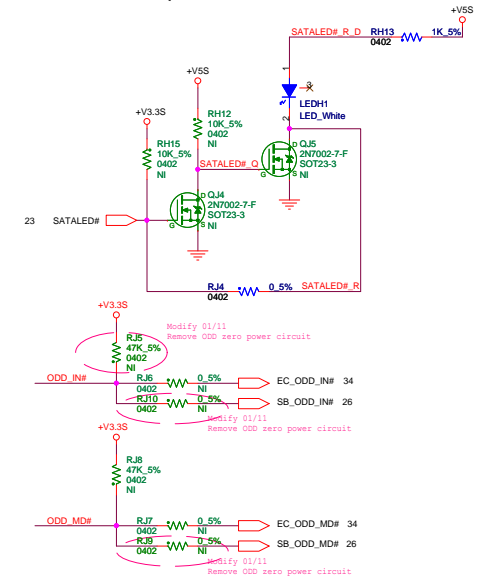
## SATA HDD CONN

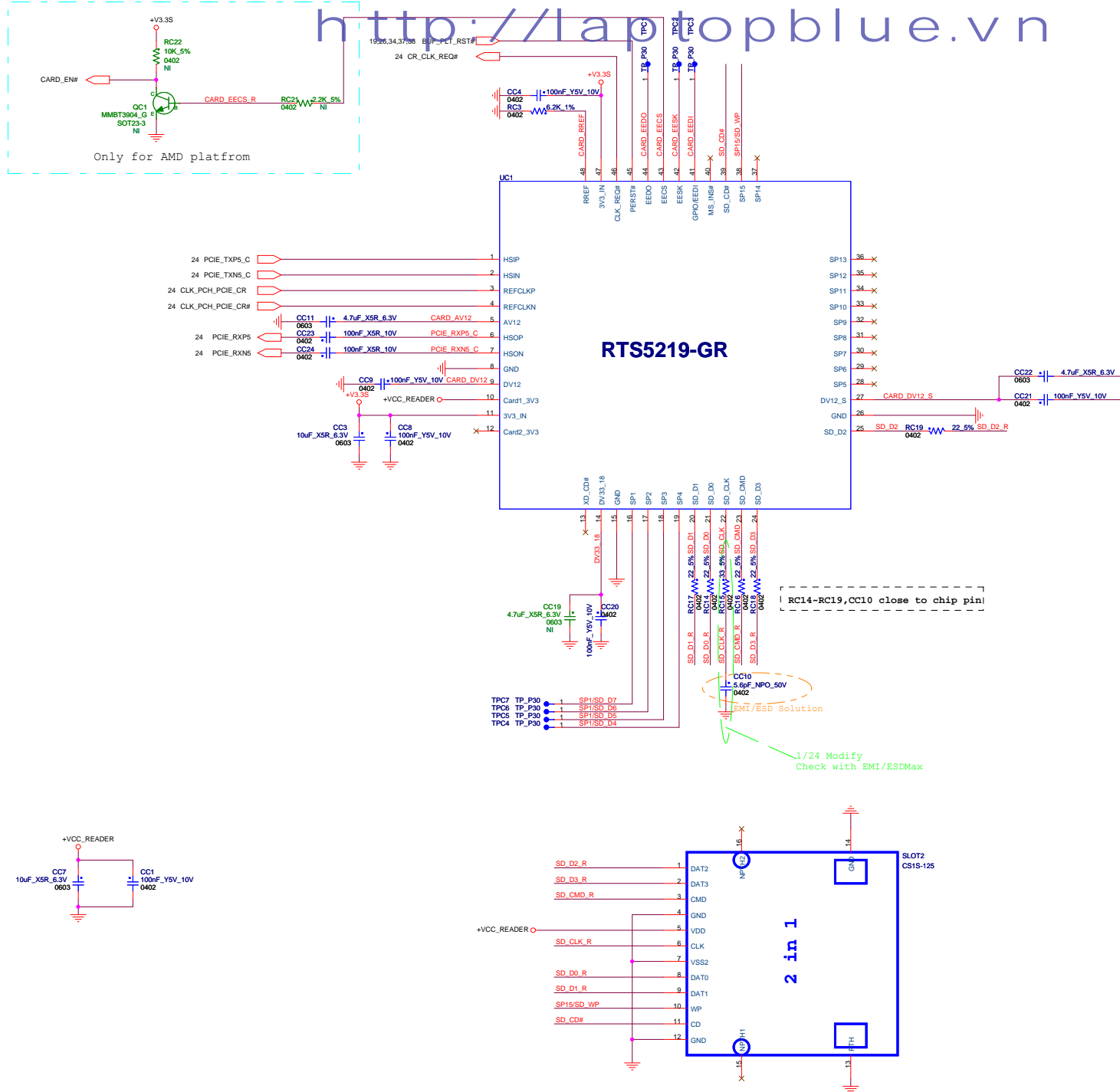


## SATA ODD CONN

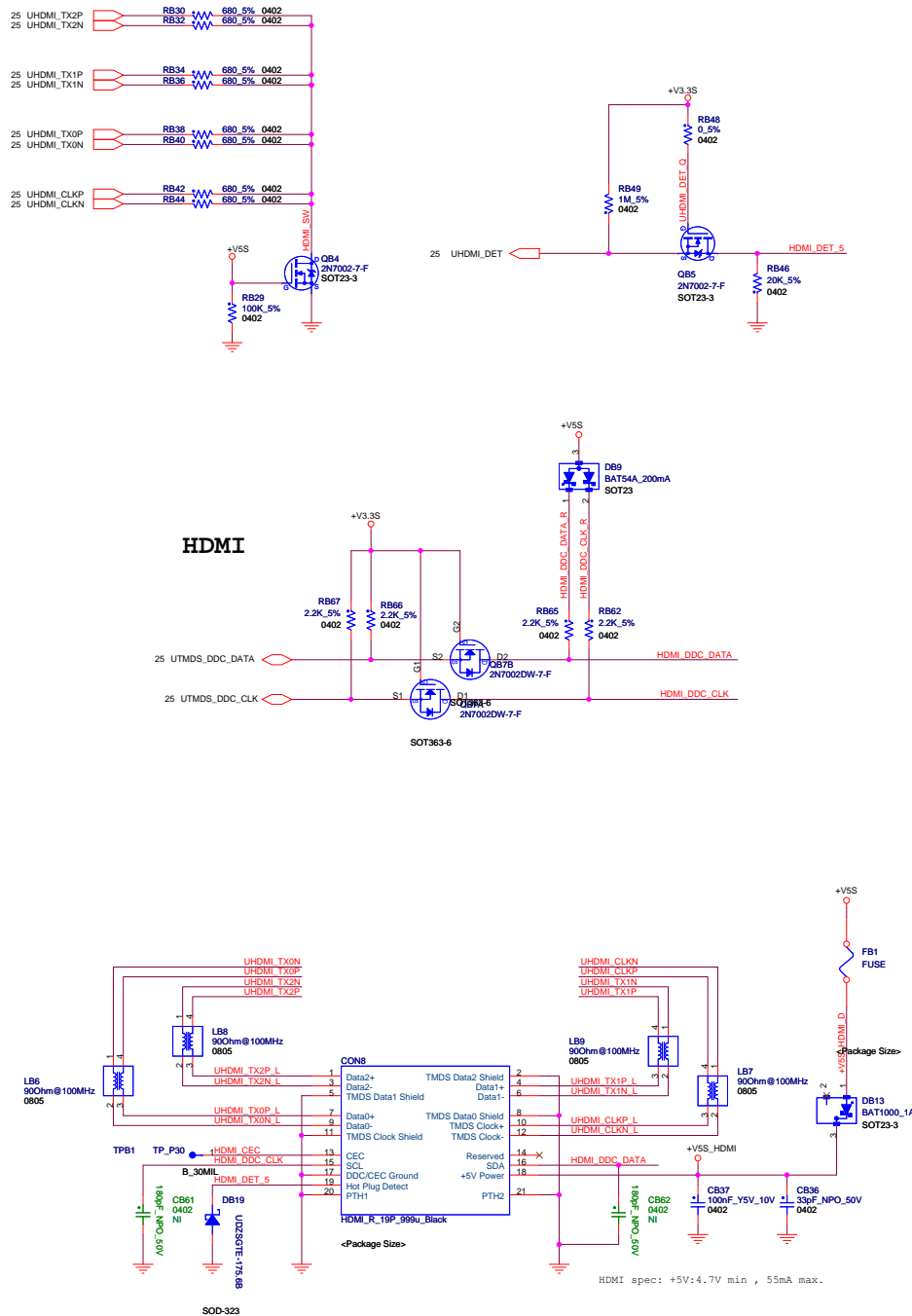


## HDD/ODD Status LED

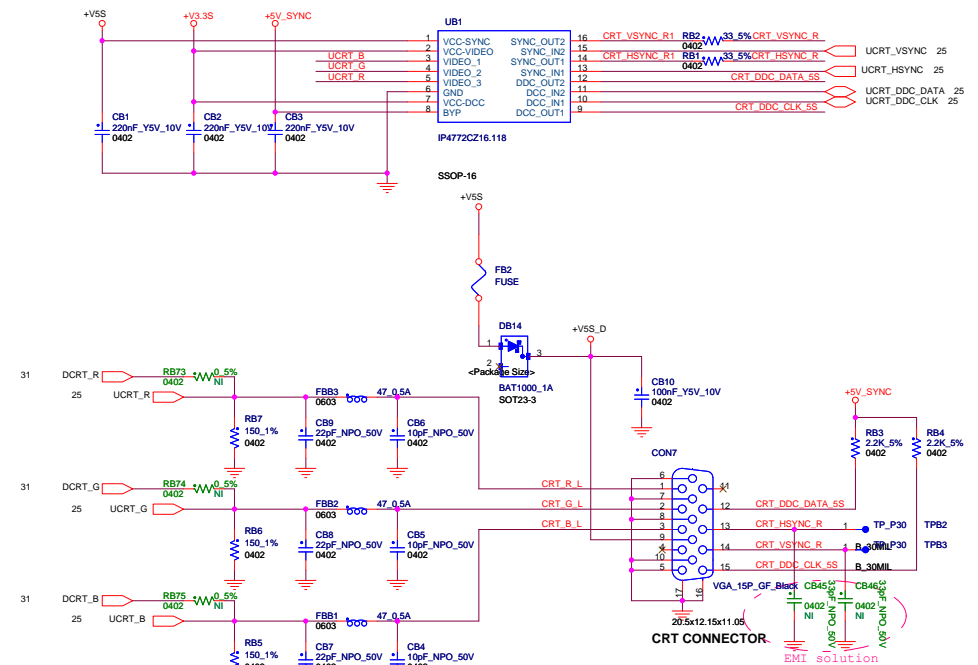


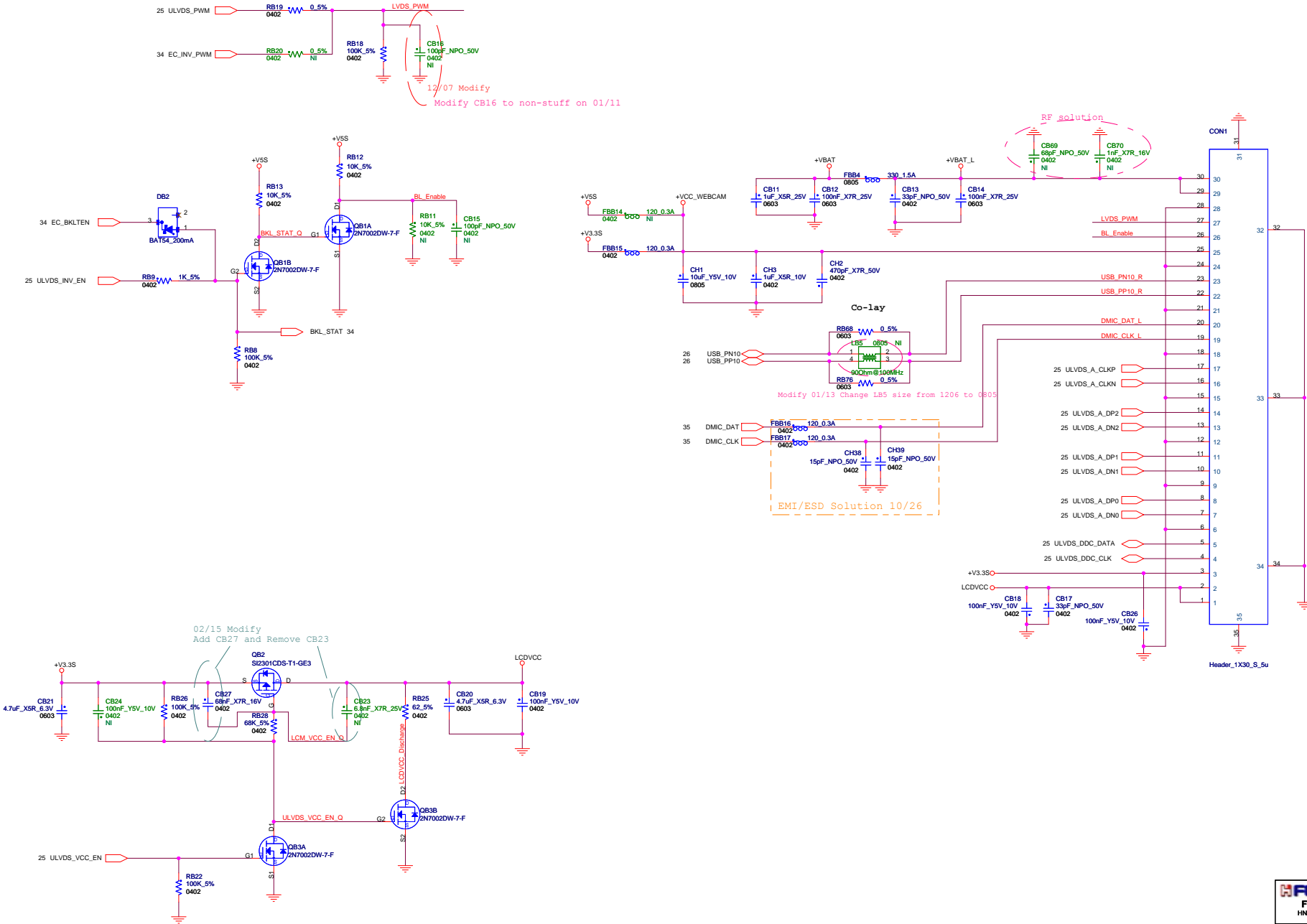


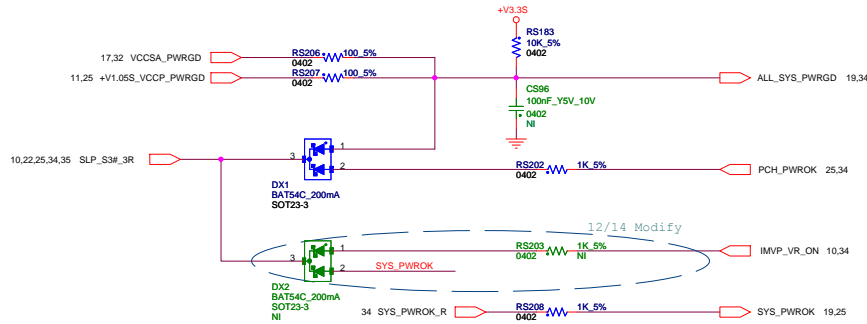




CRT







+V5S  
+V3.3S  
+V3.3S\_DELAY

+V5S 12,14,23,27,32,35,36,38,39,41,42  
+V3.3S 13,14,18,19,23,24,25,26,27,28,29,31,32,34,35,37,38,39,40,41,42  
+V3.3S\_DELAY 14,30,31,32

12/07 Modify  
1117 Modify

Modify 11/11

