

Compal confidential

Schematics Document

Mobile Yonah uFCPGA with Intel
Calistoga_GM/PM+ICH7-M core logic

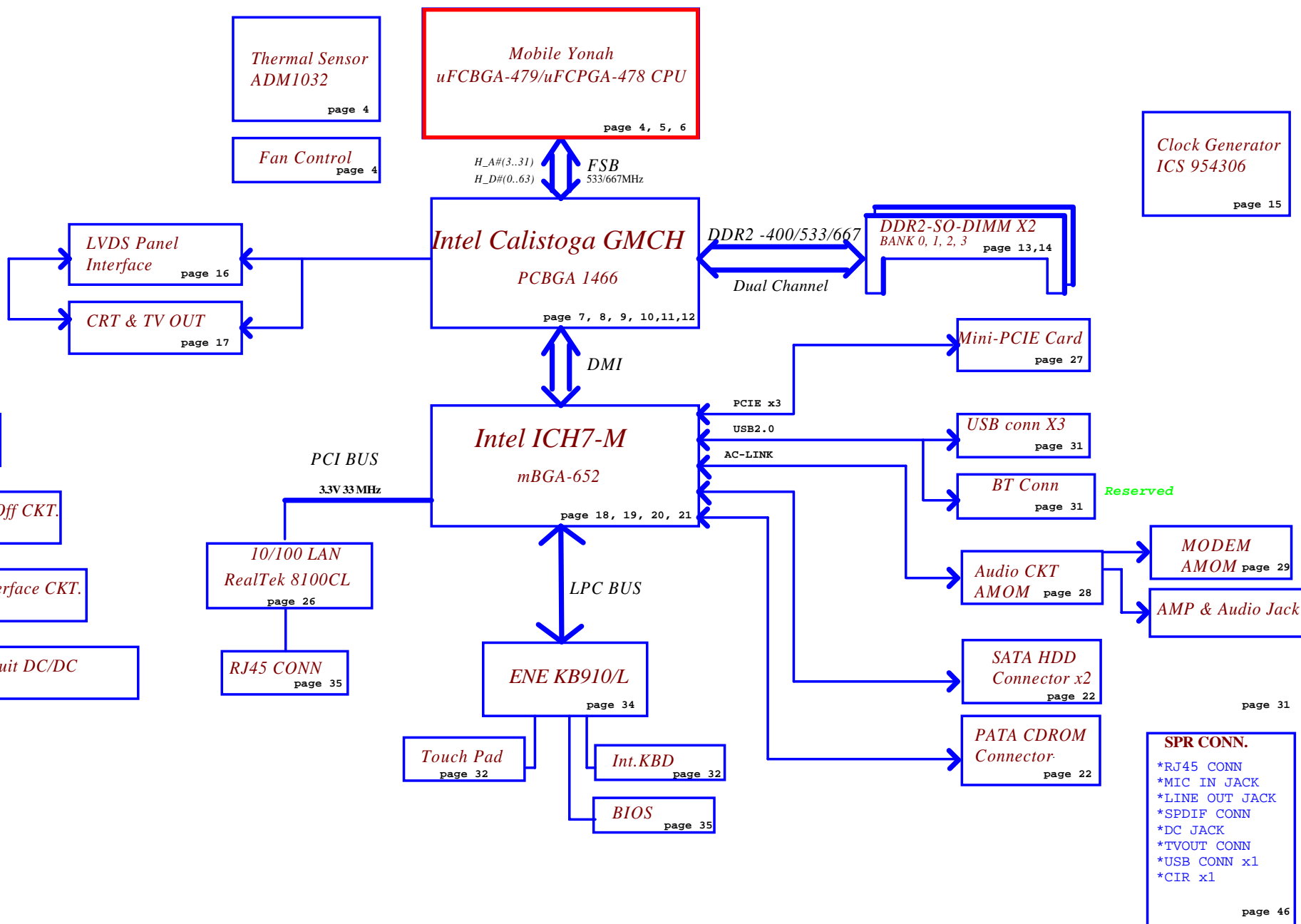
2006-05-19

REV:0.1

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PCB



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						Size	Document Number			Rev
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Voltage Rails

power plane State	+B LDO3 LDO5	+5VALW +3VALW	+1.8V +5V	+5VS +3VS +2.5VS +1.5VS +0.9VS +CPU_CORE +VCCP
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

O MEANS ON
X MEANS OFF

PCI Devices

EXTERNAL	IDSEL#	REQ/GNT#	PIRQ
CARD BUS & 1394	AD22	2	C,D,E,G
RealTek 8100CL	AD24	1	E

Load BOM check item

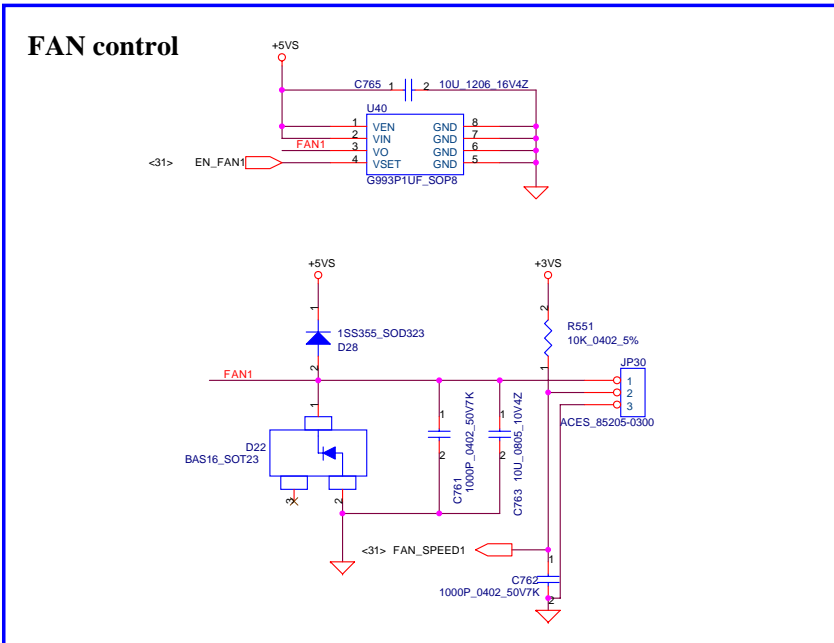
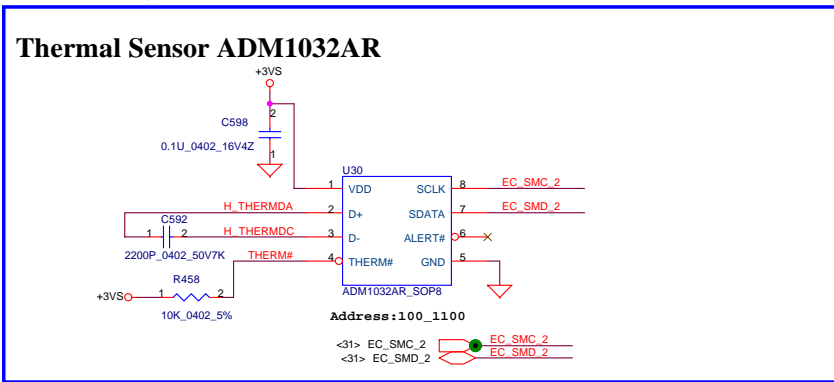
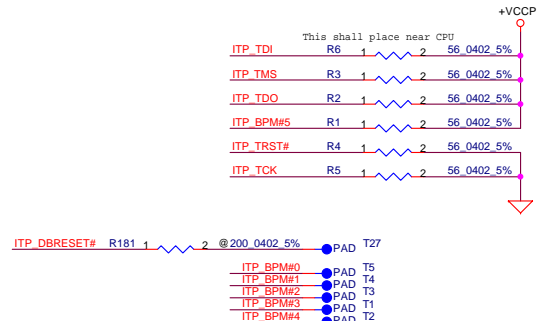
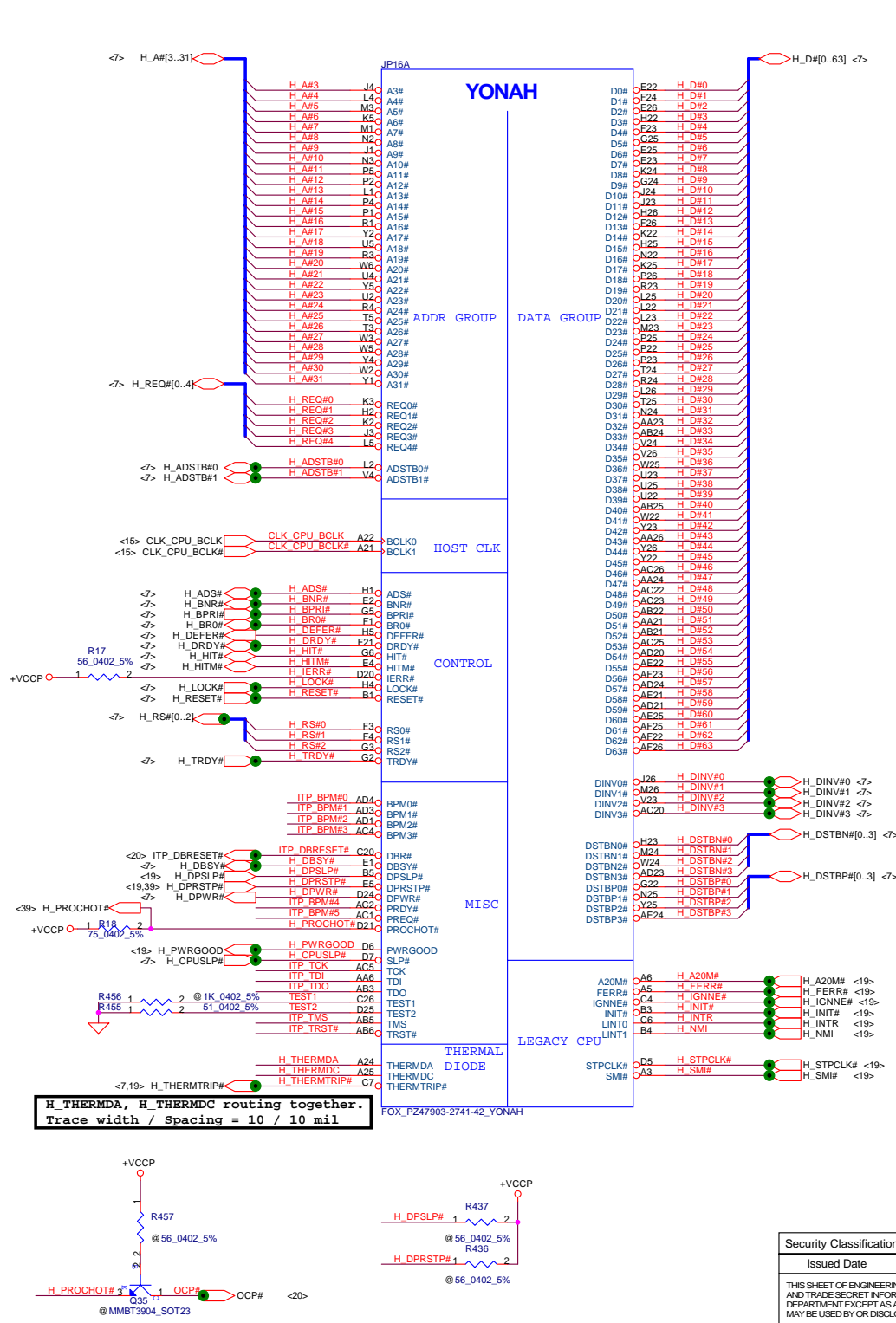
- 1.U31 GM/PM/GML part number
- 2.U6 ICH7 part number

BOM: 43144132L01 (GM)
43144132L02 (GML)

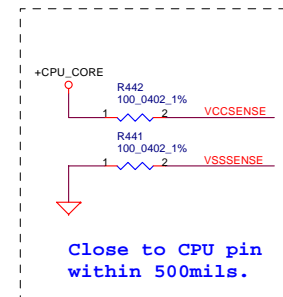
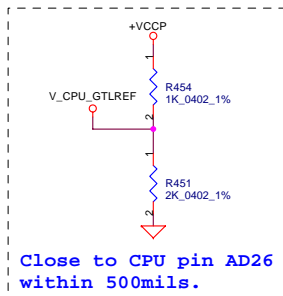
Jump-Short:

PJP4,PJP6,PJP7,PJP8,PJP10,PJP12,PJP14,PJP18,PJP19,PJP20,PJP25

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Issued Date	2005/03/10	Deciphered Date	2006/03/10	Yonah CPU in mFCPGA479	
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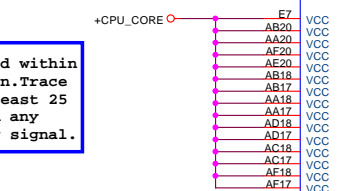
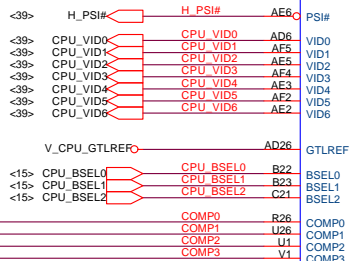
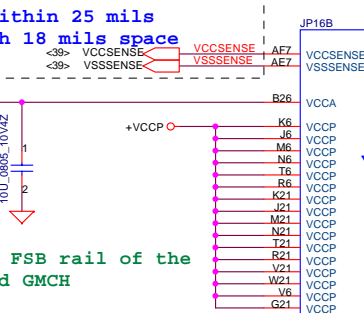
+1.5vs is a power source required by the PL clock generator on the processorsilicon

Length match within 25 mils
The trace width 18 mils space
7 mils

+VCCP is the FSB rail of the processor and GMCH

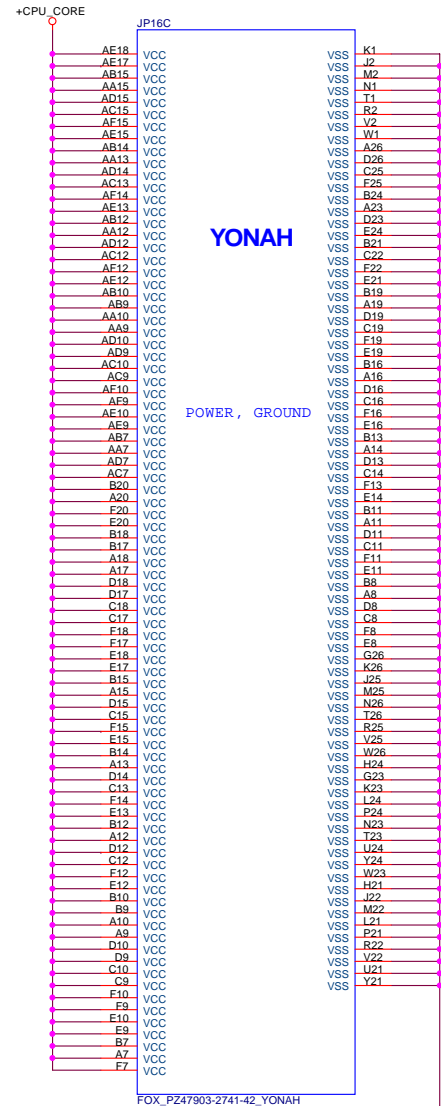
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal.



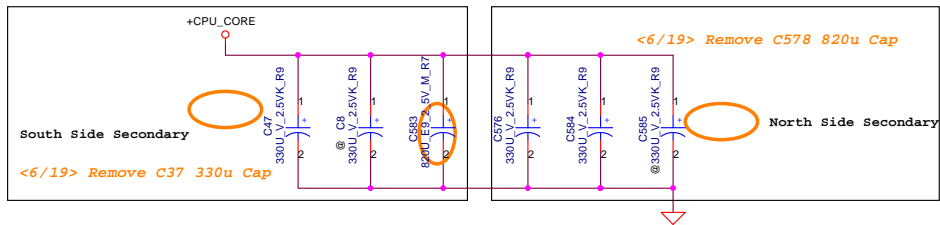
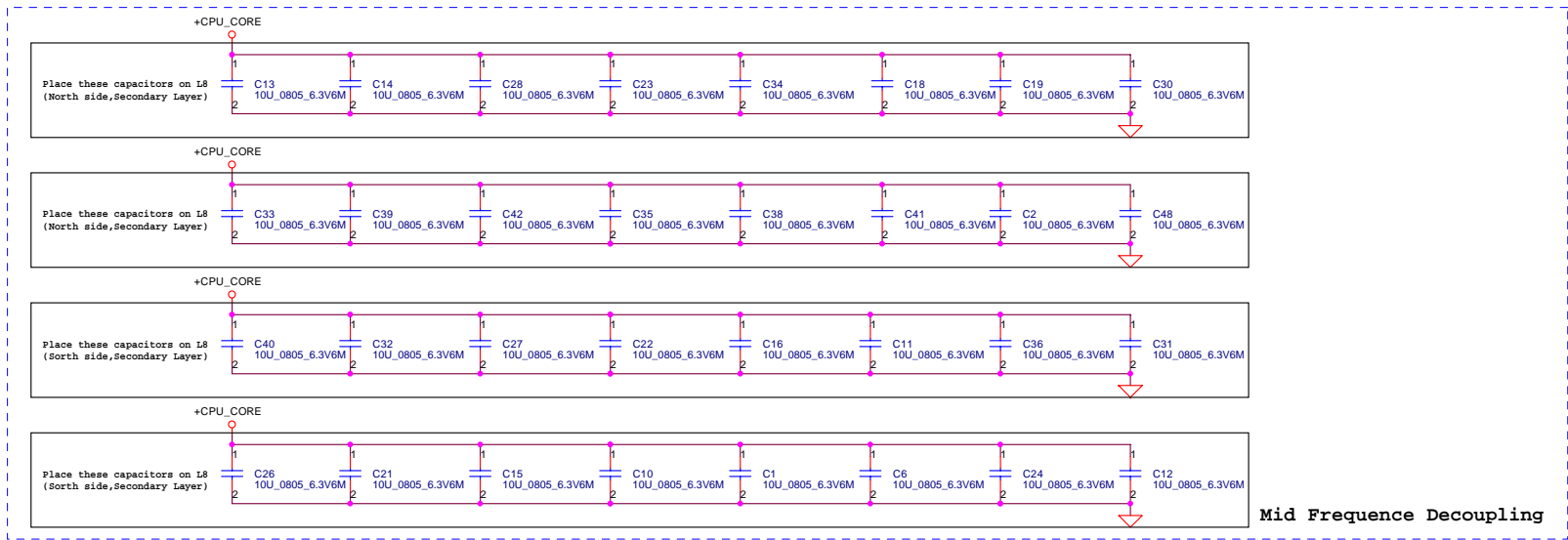
YONAH

POWER, GROUND, RESERVED SIGNALS AND NC

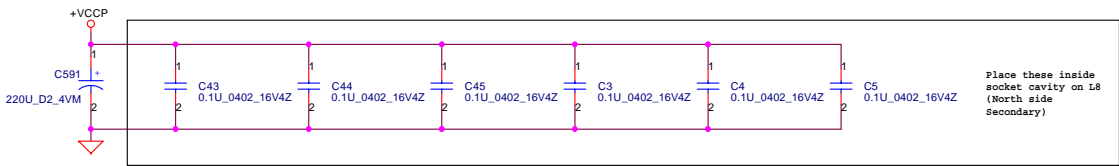


YONAH

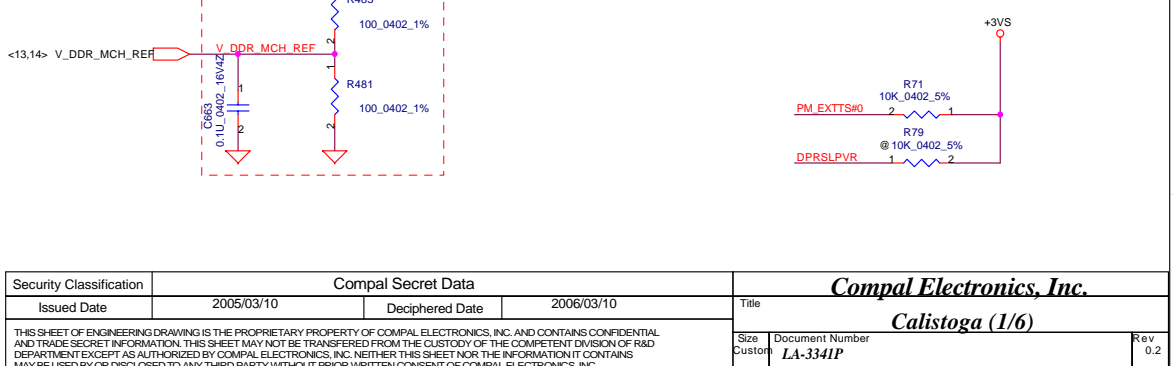
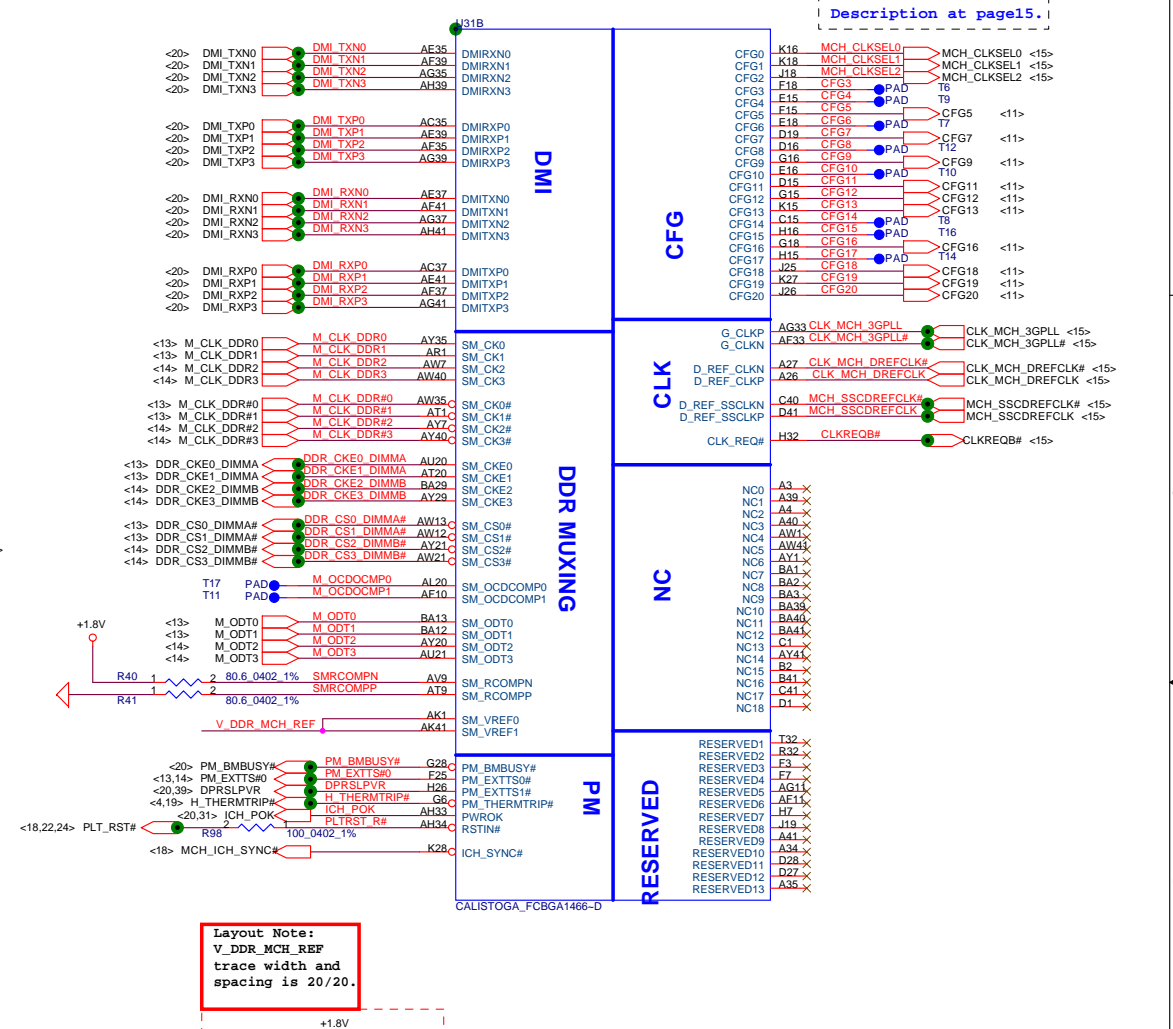
POWER, GROUND

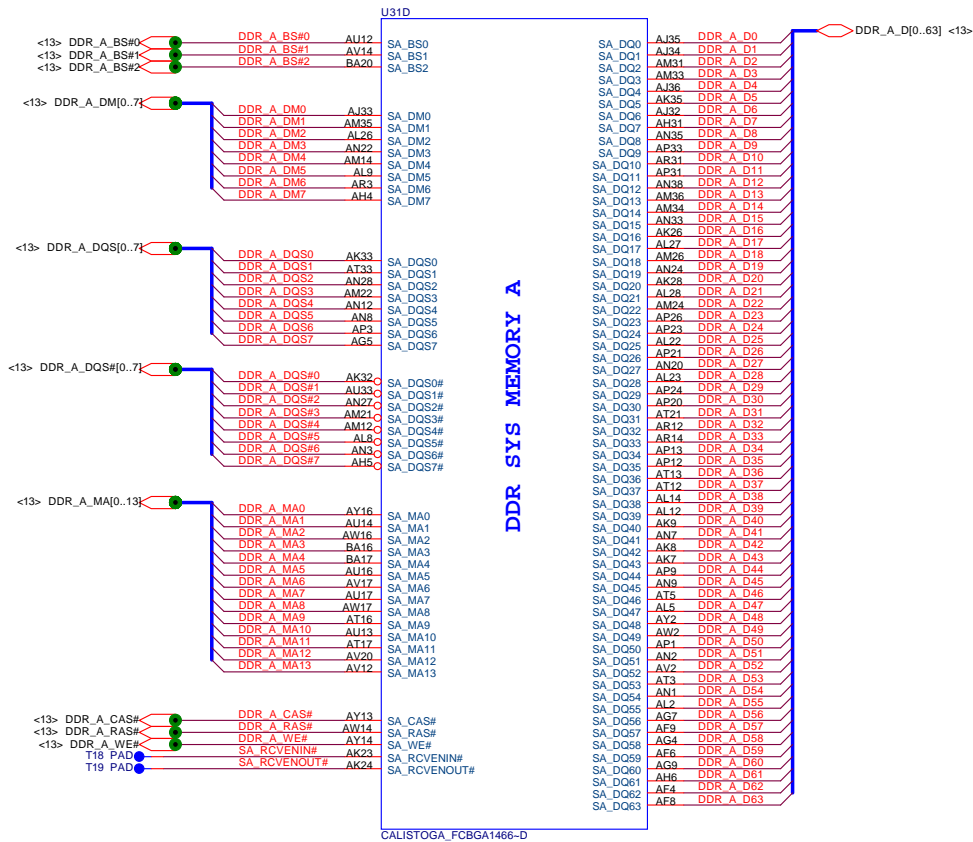


ESR <= 1.5m ohm
 Capacitor > 1980uF

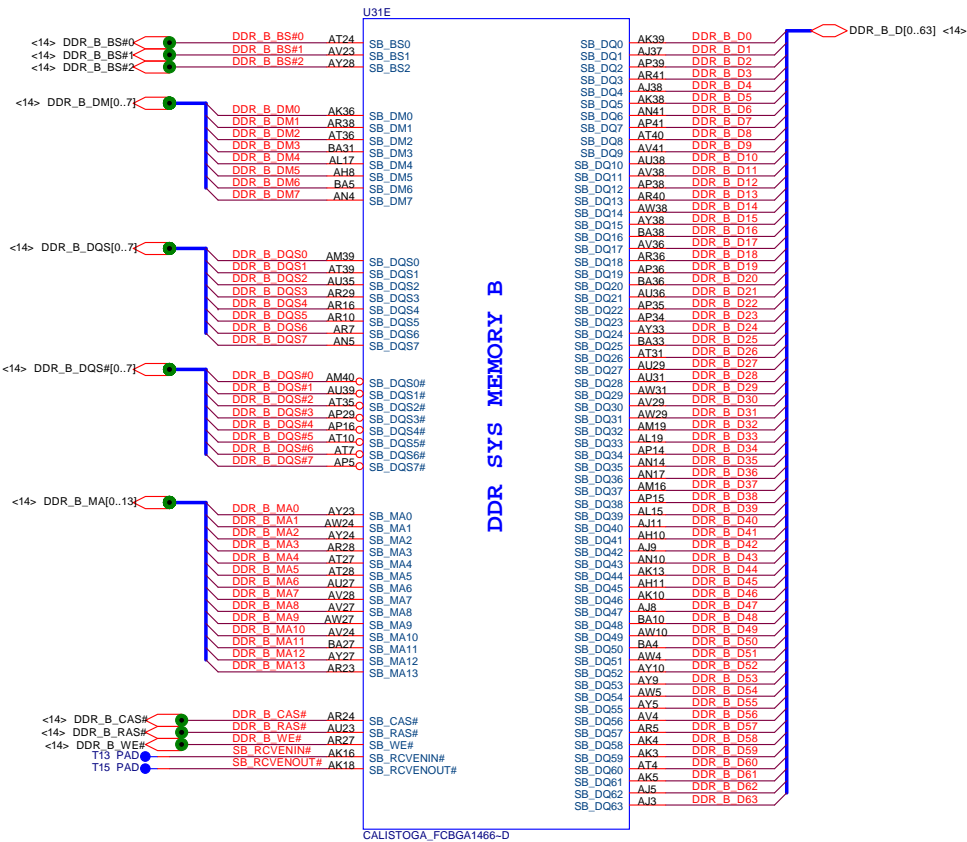


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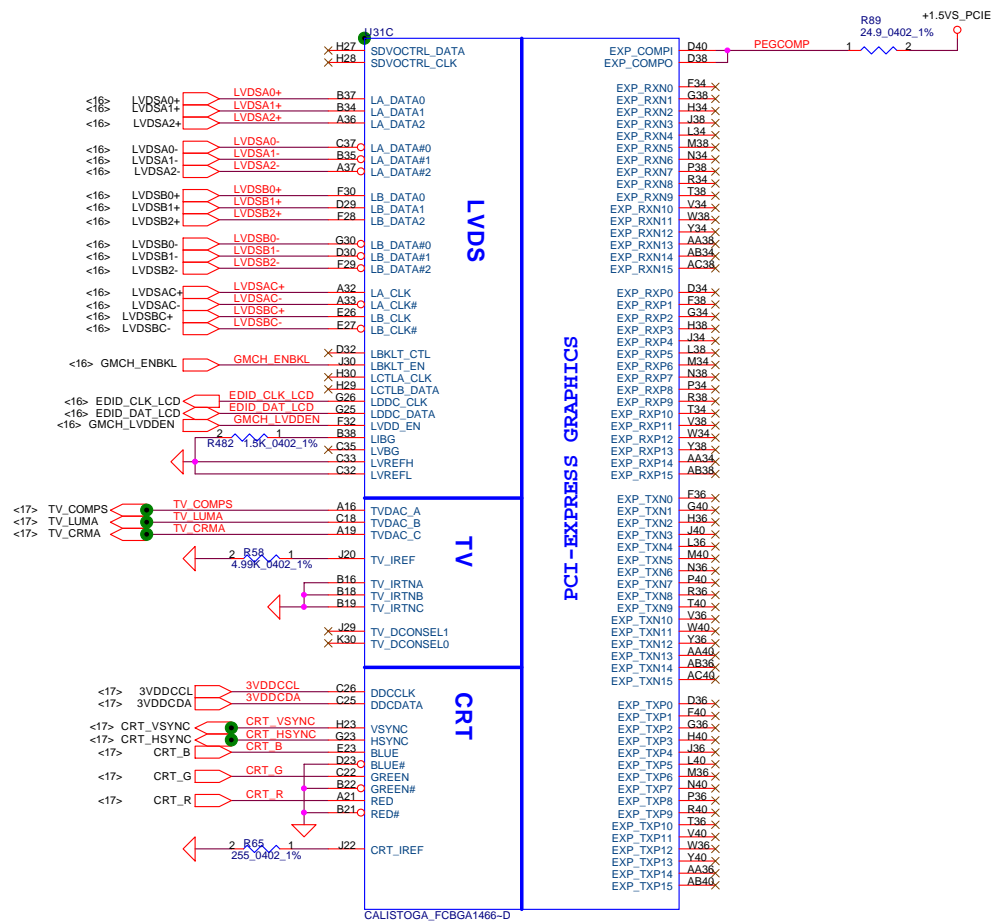
CALISTOGA_FCBGA1466-D



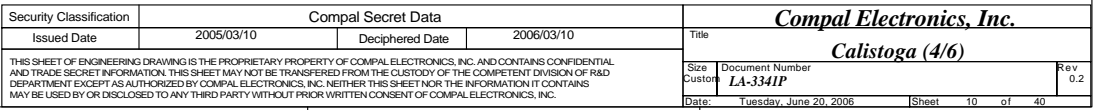
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Calistoga (2/6)



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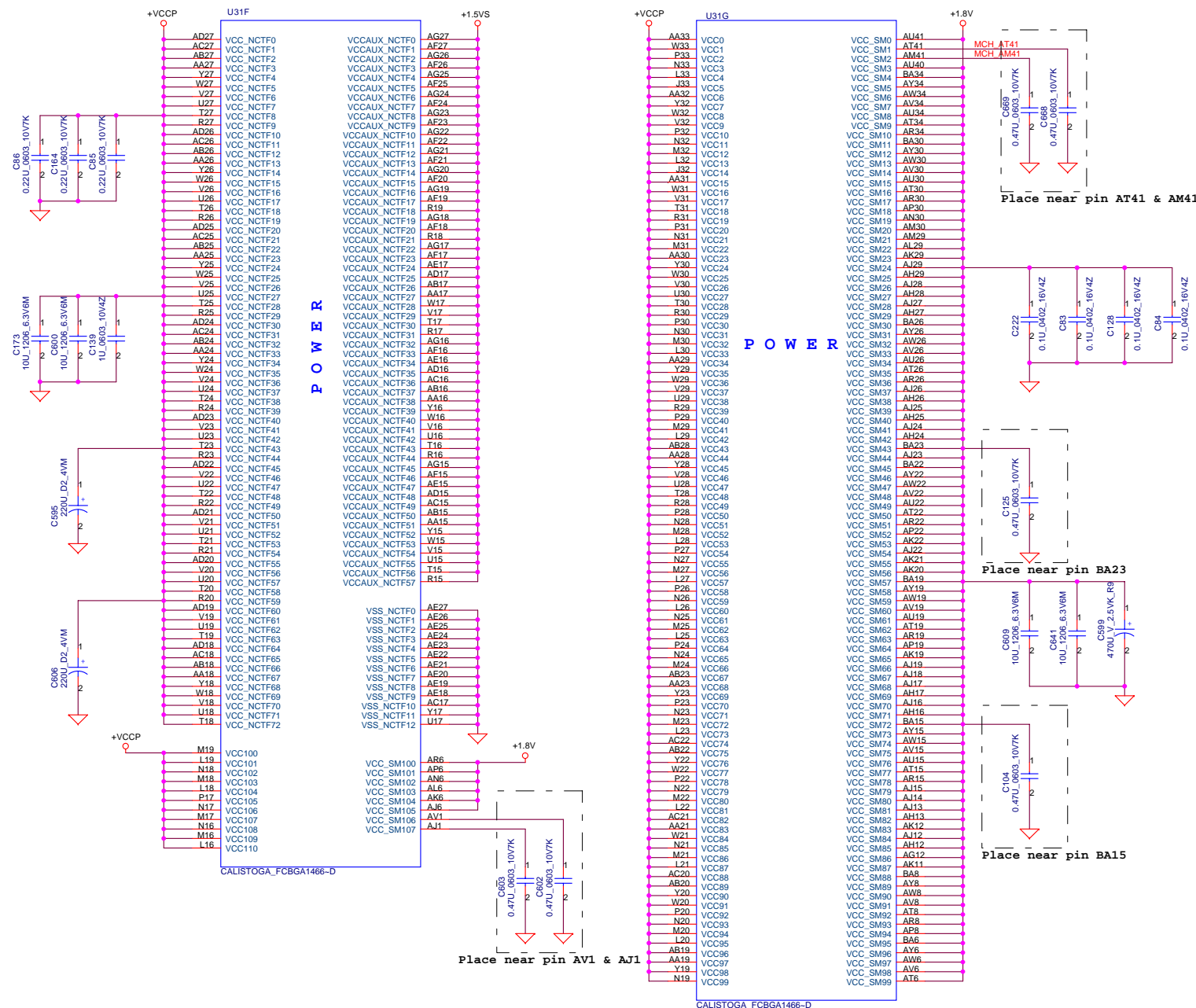
Strap Pin Table

CFG[3:17] have internal pull up

CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU *(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation (Default) *
CFG6	0 = Reserved
PSB 4X CLK Enable	1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG10 CFG18	10 = 1.05V *(Default) 01 = 1.5V
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present *(Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.

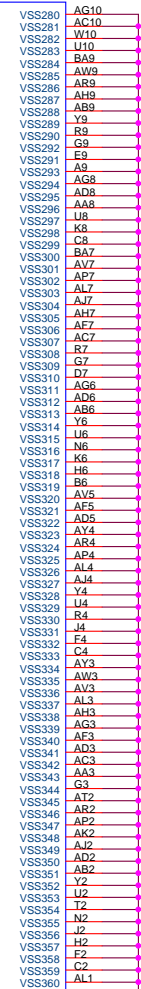
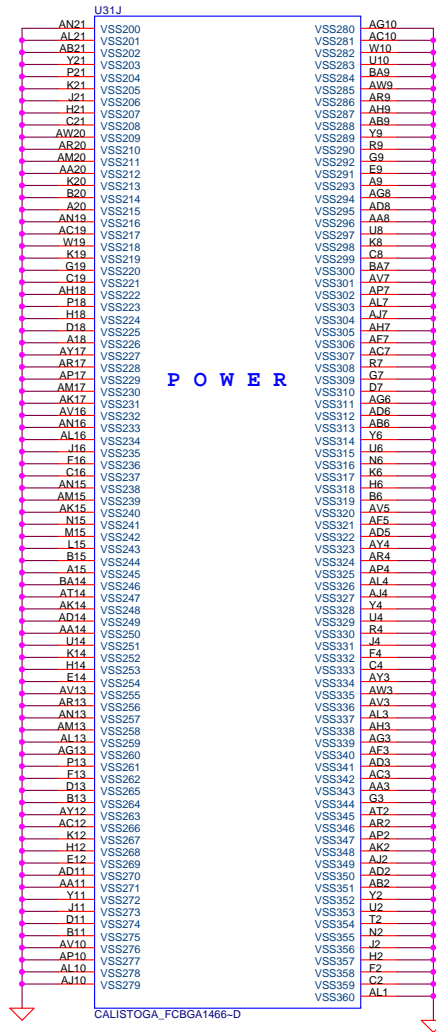
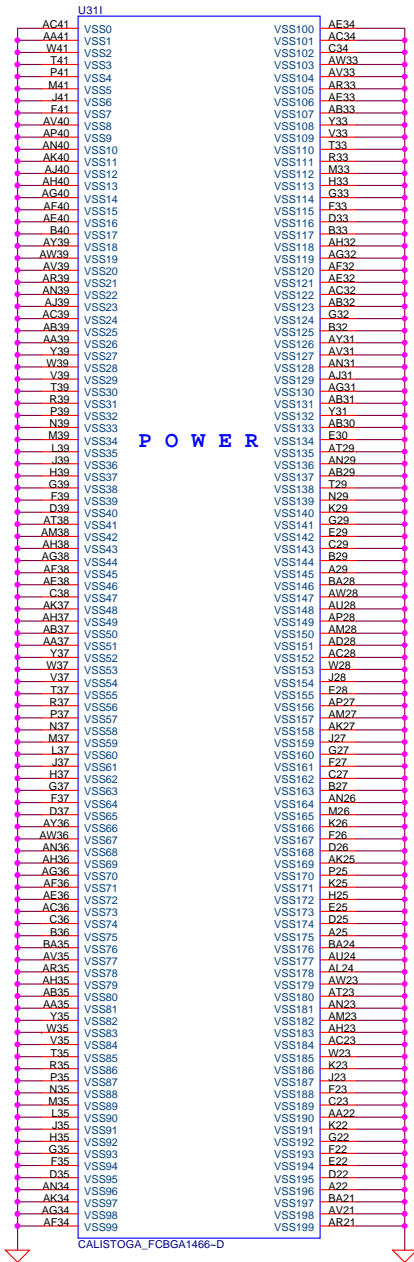
<7>	CFG5	R48	1	2	@ 2.2K 0402 5%
<7>	CFG7	R54	1	2	@ 2.2K 0402 5%
<7>	CFG9	R51	1	2	@ 2.2K 0402 5%
<7>	CFG11	R47	1	2	@ 2.2K 0402 5%
<7>	CFG12	R49	1	2	@ 2.2K 0402 5%
<7>	CFG13	R50	1	2	@ 2.2K 0402 5%
<7>	CFG16	R53	1	2	@ 2.2K 0402 5%
<7>	CFG18	R74	1	2	@ 1K 0402 5%
<7>	CFG19	R82	1	2	@ 1K 0402 5%
<7>	CFG20	R87	1	2	@ 1K 0402 5%



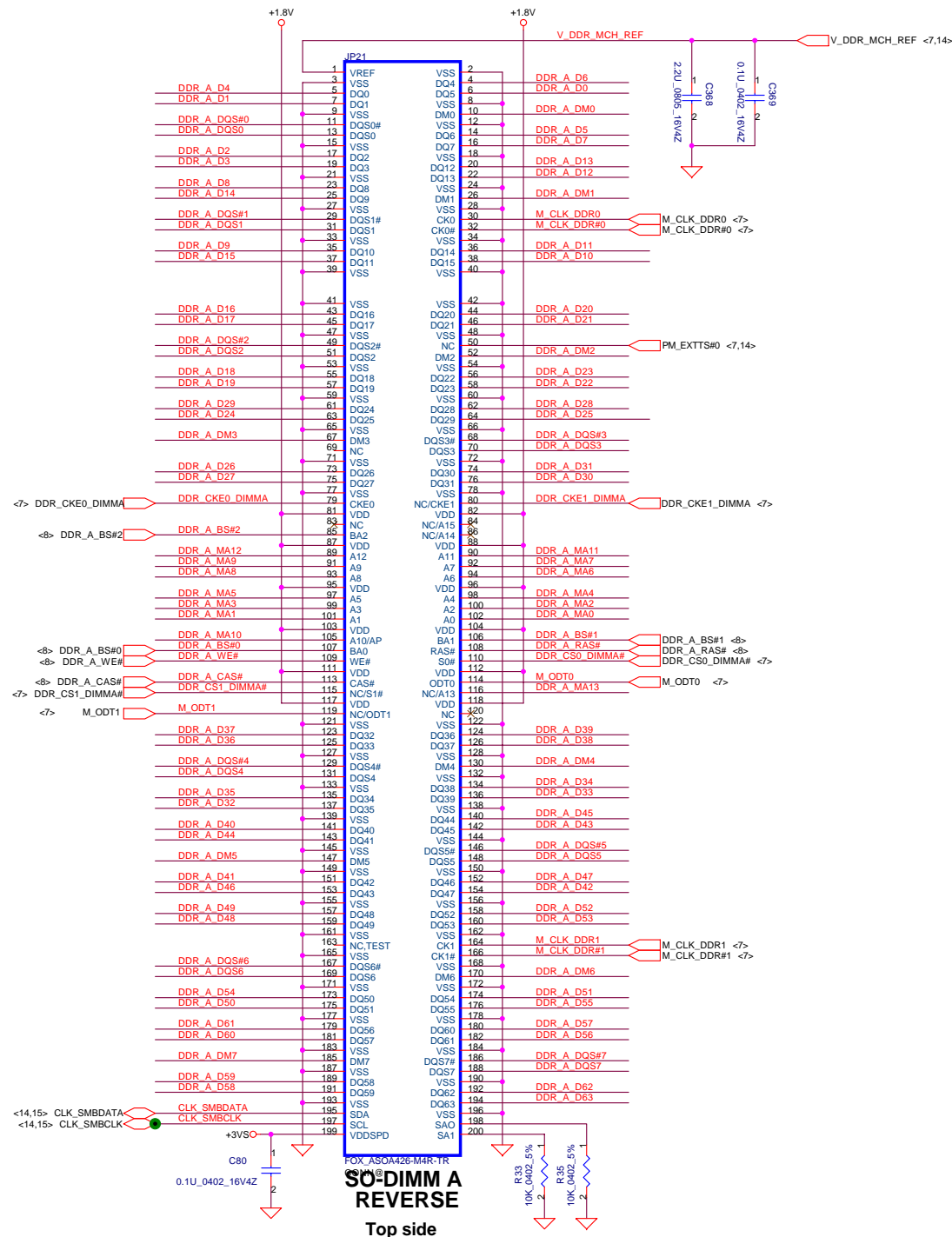
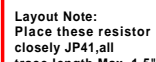
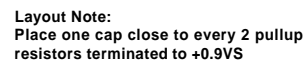
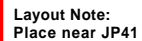
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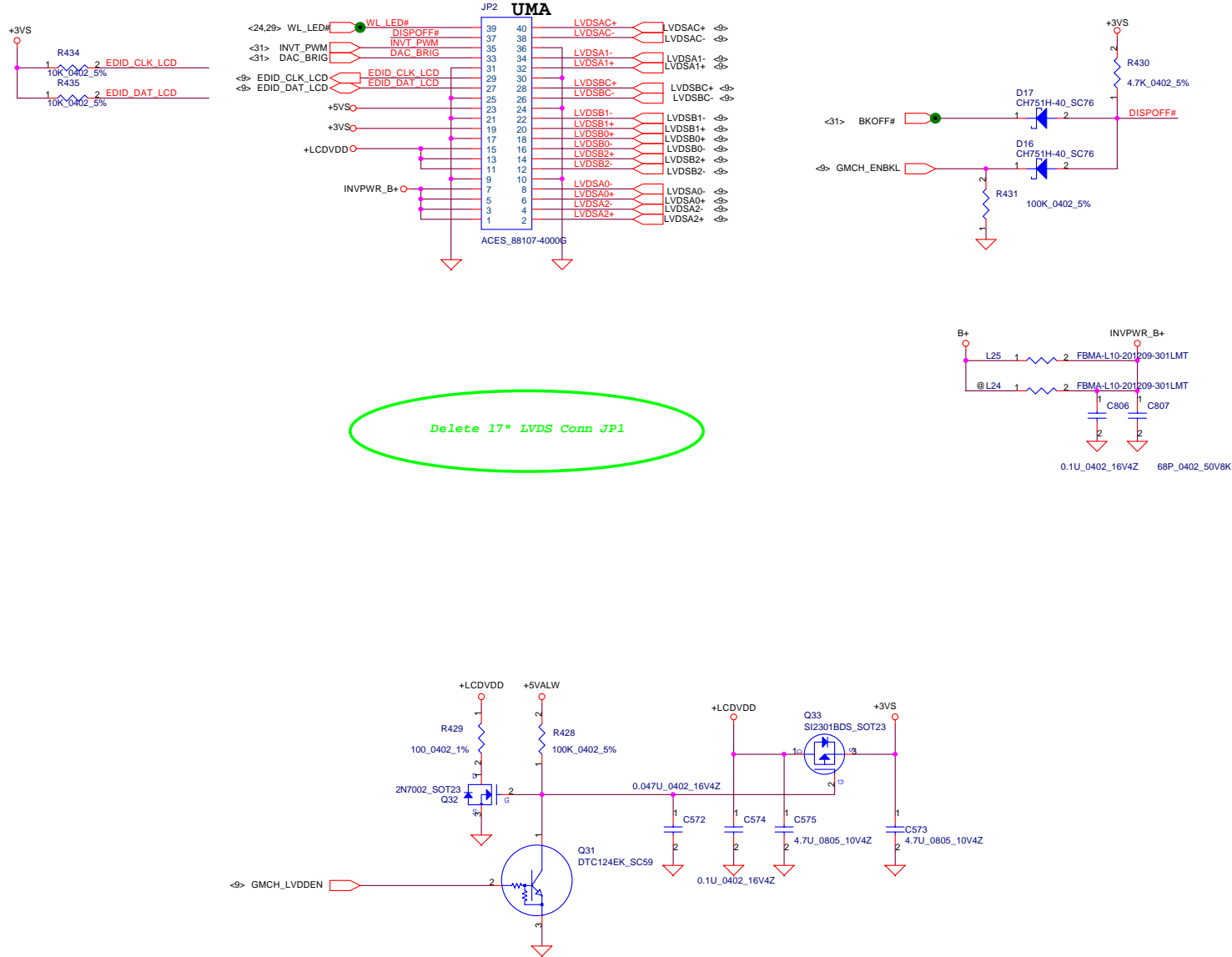
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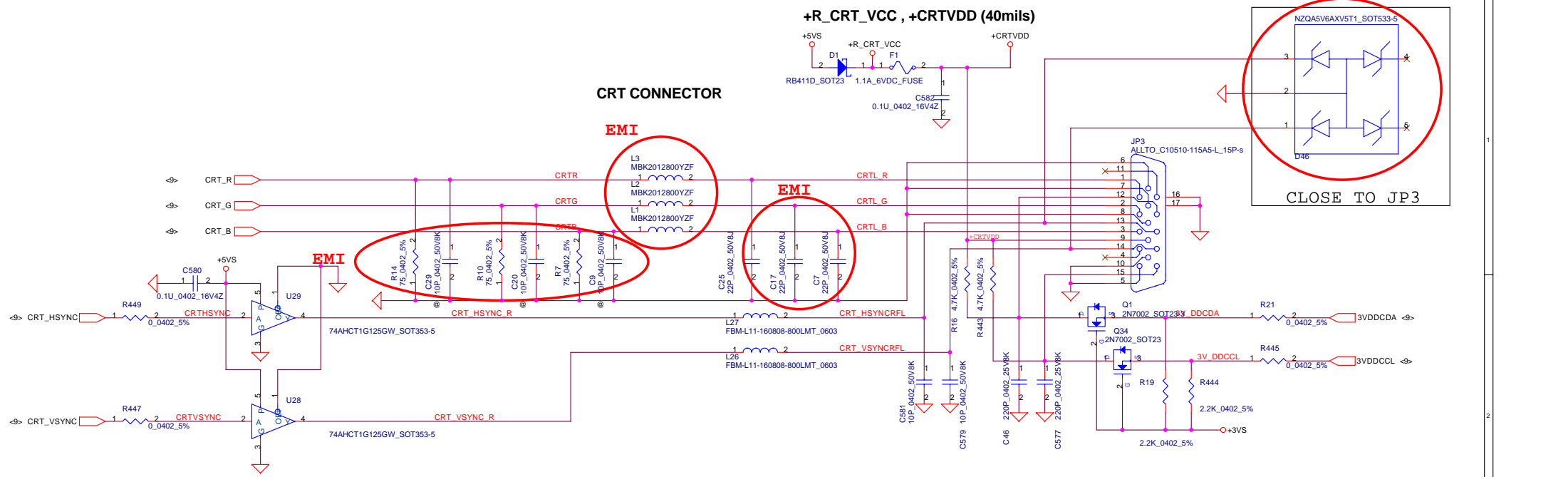
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LCD Panel & inverter Connector



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				LVDS Connector					
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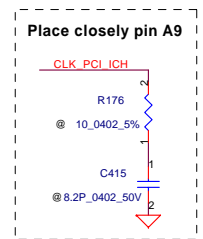
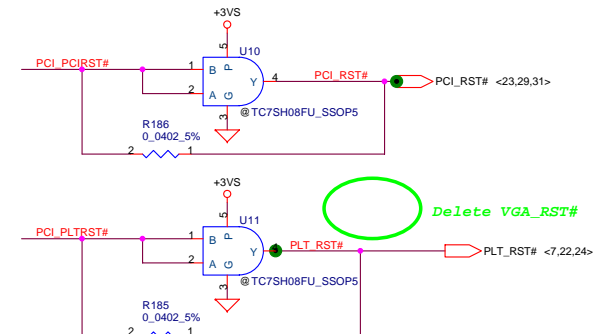
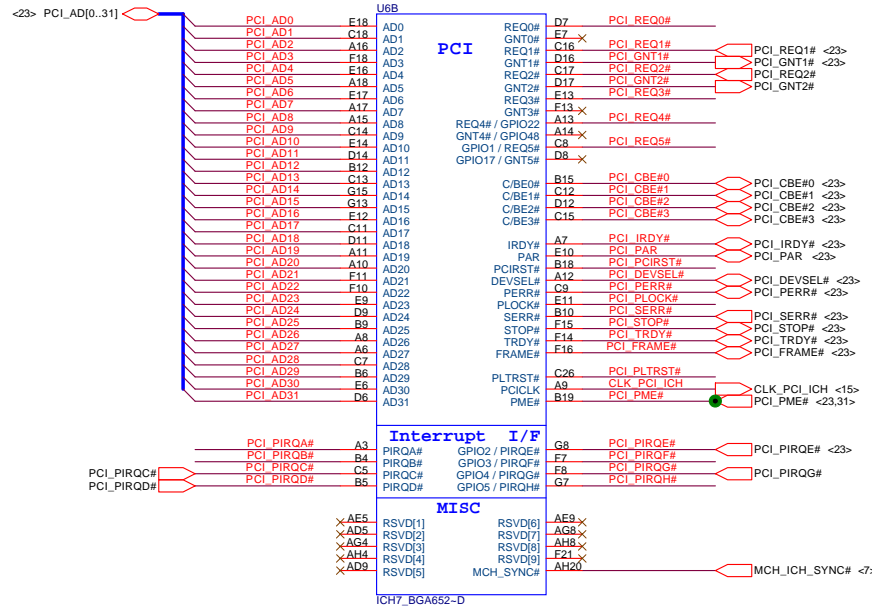
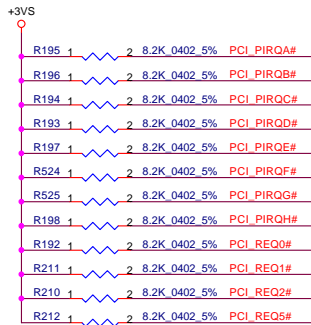
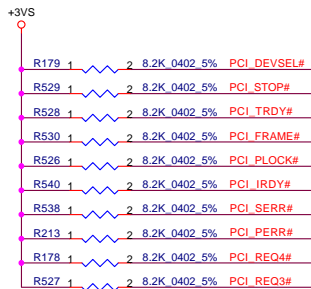
TV-Out Connector
S-Video

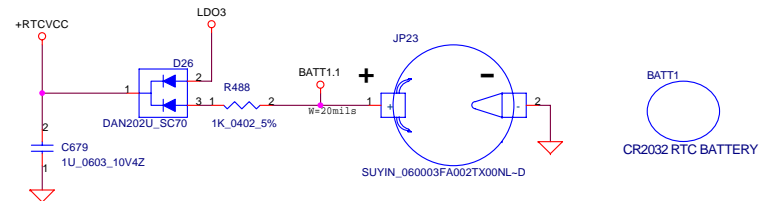
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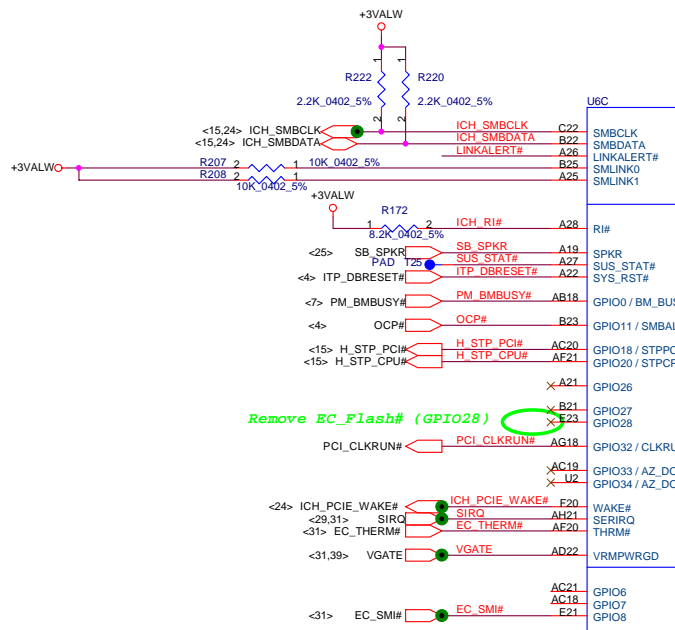
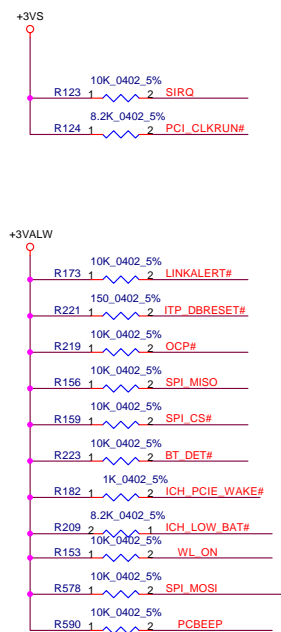
CRT & TVout Connector

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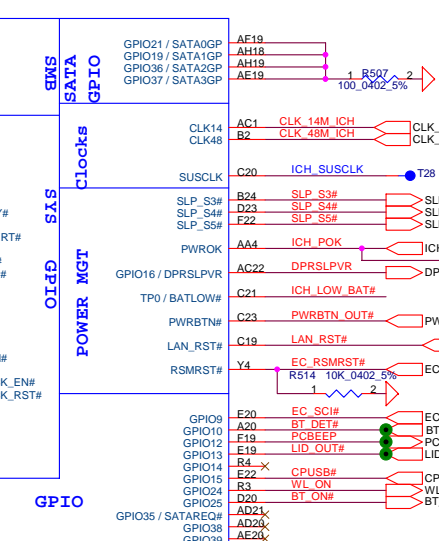
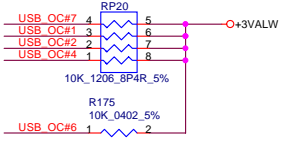
Remove EC_Flash# (GPIO28)

PCI_CLKRUN#

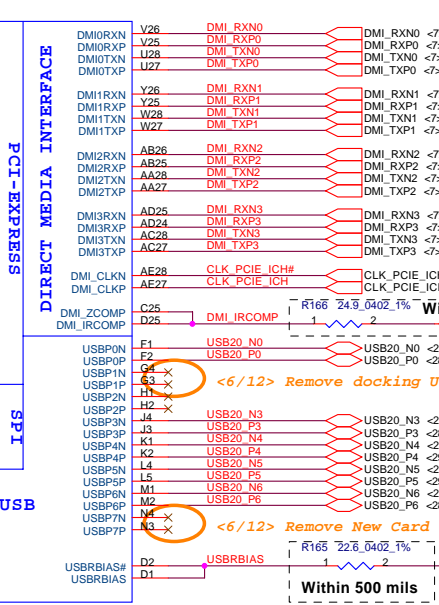
Delete 17" New Card PCIE traces

<6/20> Remove New Card trace

To mini PCIE Card

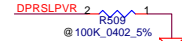
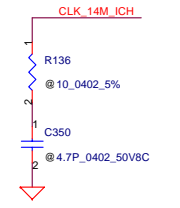
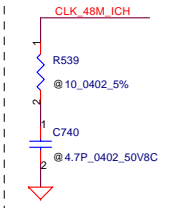


Need update symbol

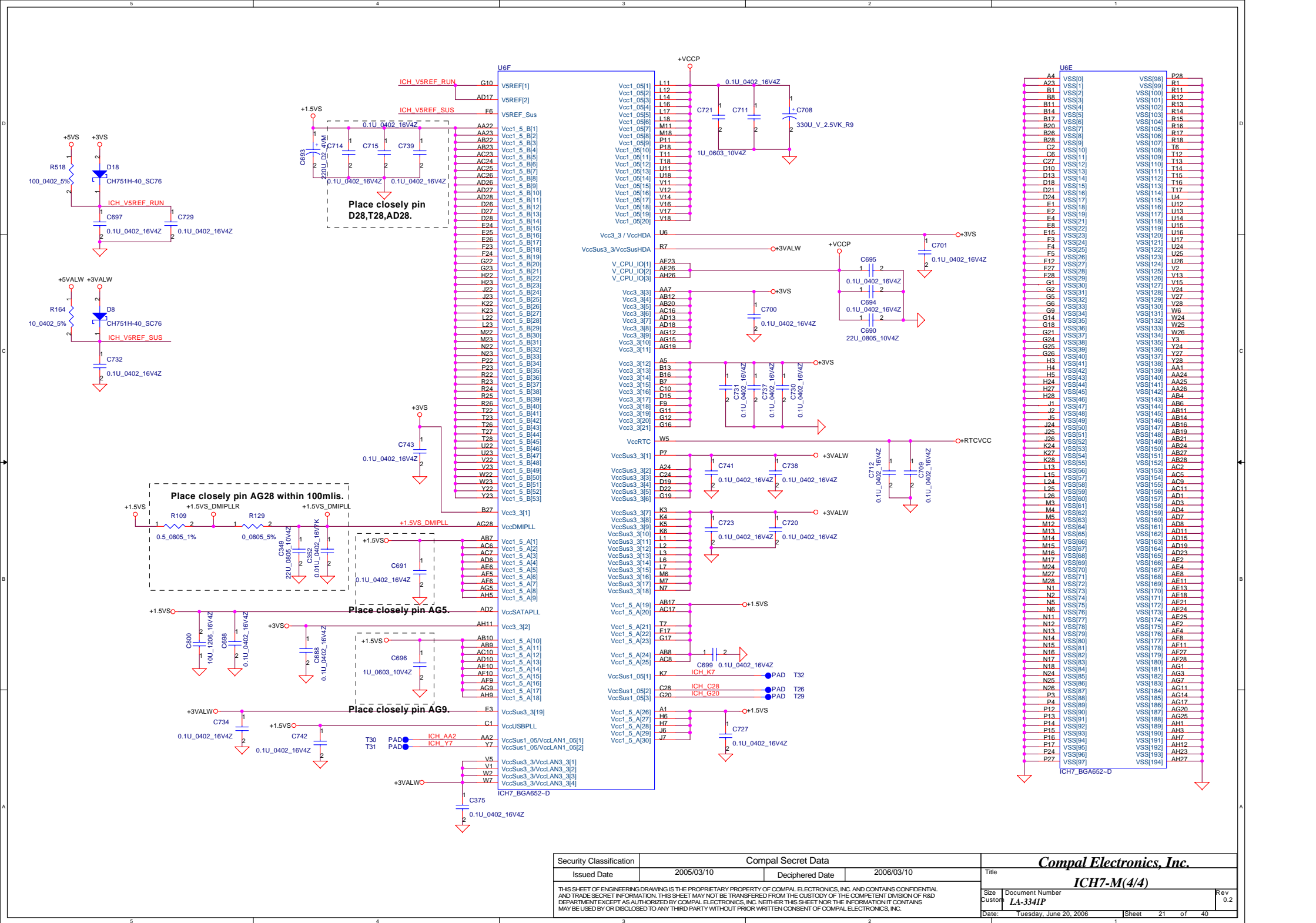


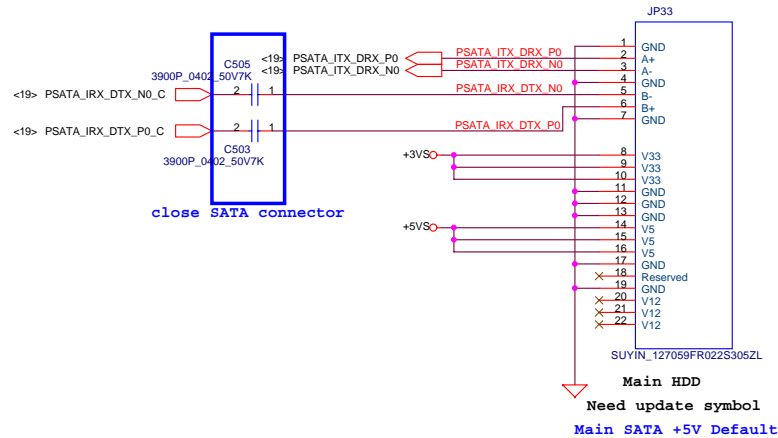
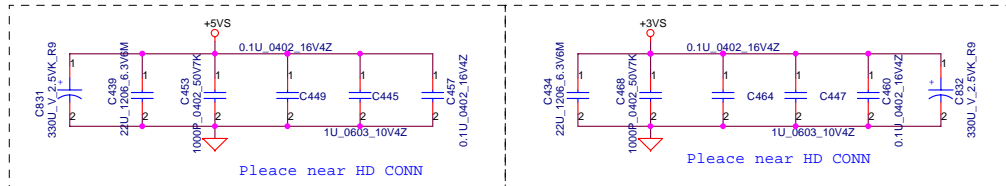
Place closely pin B2

Place closely pin AC1



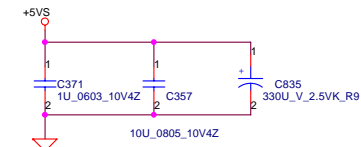
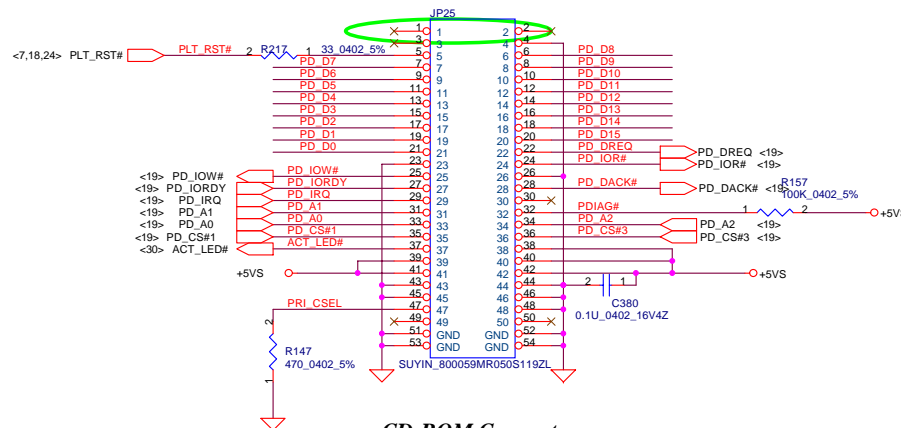
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						Size		Document Number		Rev	
						Custom		LA-334IP		0.2	
						Date:		Tuesday, June 20, 2006		Sheet 20 of 40	





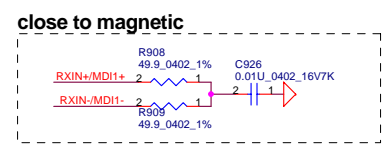
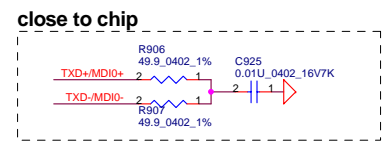
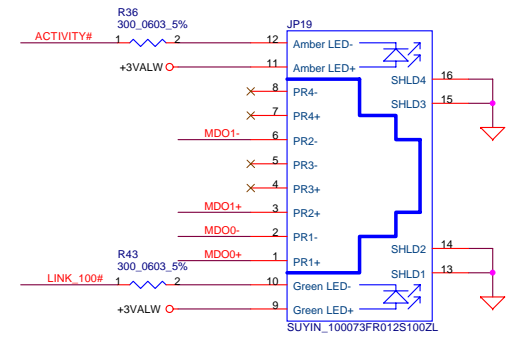
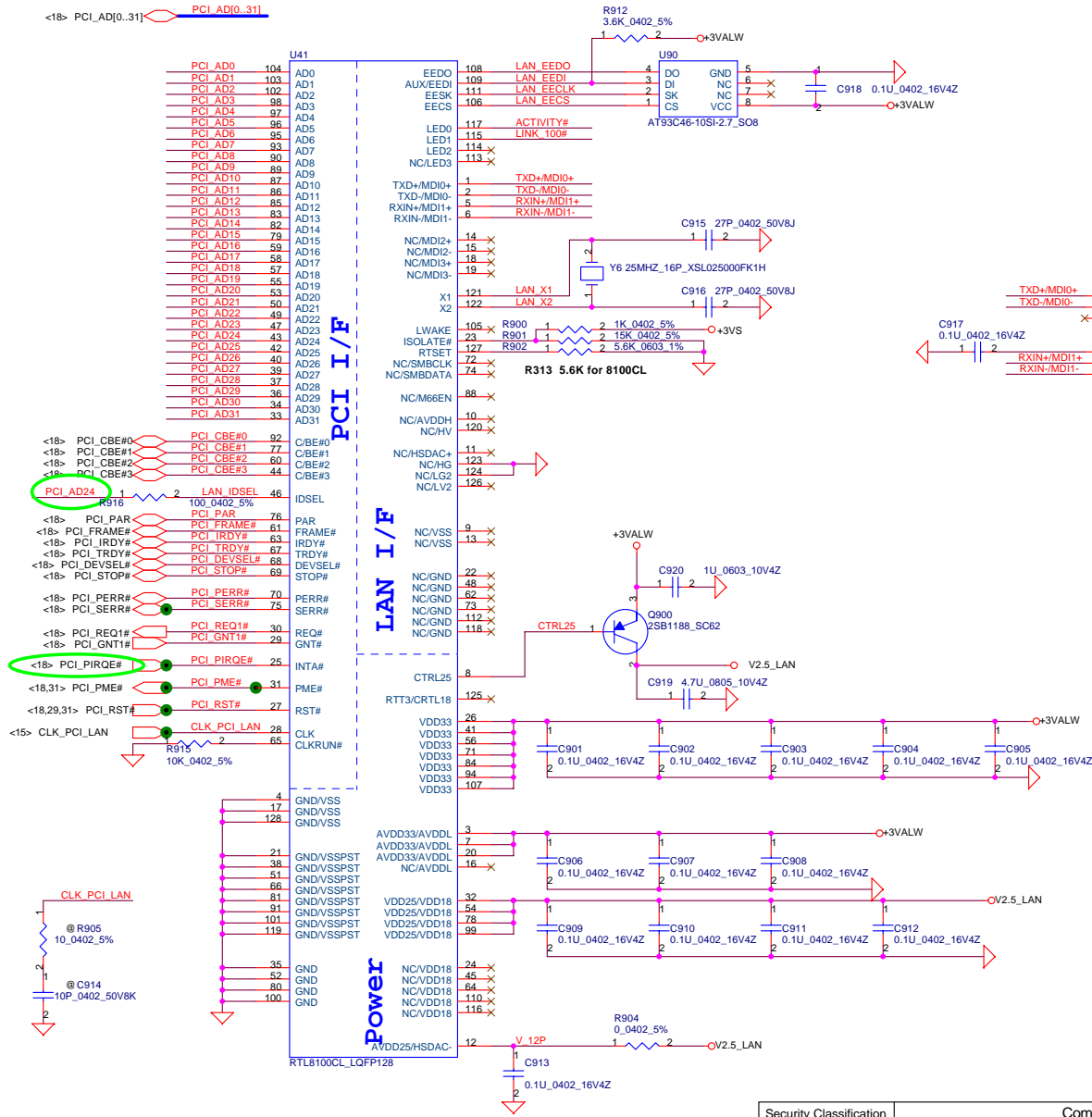
PD_D[0..15] PD_D[0..15] <19>

Delete CD traces (JP25 pin1,2 and3)



CD-ROM Connector

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						Size Custom		Document Number		Rev 0.2	
						LA-3341P					
Date:		Tuesday, June 20, 2006		Sheet		23		of 40			

The schematic diagram illustrates the electrical connections for the Molex 67910-0002 connector, which interfaces with the Intel Atom D5015. The connector pins are labeled JP18 and are connected to various system signals and components.

Connector Signals and Connections:

- Pin 1:** ICH_PCIE_WAKE#
- Pin 2:** WL_PRIORITY
- Pin 3:** BT_PRIORITY
- Pin 4:** CLK_PCIE_MCARD#
- Pin 5:** CLK_PCIE_MCARD
- Pin 6:** PCIE_RXN3
- Pin 7:** PCIE_RXP3
- Pin 8:** PCIE_TXN3
- Pin 9:** PCIE_TXP3
- Pin 10:** PLT_RST#
- Pin 11:** ICH_SMBCLK
- Pin 12:** ICH_SMBDATA
- Pin 13:** LED_WLAN_OUT#
- Pin 14:** WIRELESS_LED_BT

Key Components and Connections:

- Power Supply:** The circuit is powered by a 3V3 supply. A 1.5V3 supply is also present, connected to the WL_PRIORITY signal.
- Capacitors:** Several capacitors are used for decoupling and timing, including C608 (0.1uF, 0402, 16V4Z), C797 (0.1uF, 0402, 16V4Z), C78 (0.1uF, 0402, 16V4Z), and C167 (0.1uF, 0402, 16V4Z).
- Resistors:** Resistors R600 (1k, 0402, 5%), R593 (100k, 0402, 5%), R594 (100k, 0402, 5%), and R582 (470, 0402, 5%) are used for signal conditioning and pull-up/pull-down.
- Transistors:** The circuit includes several transistors: Q48 (DTA114YKA, SC59), Q49 (2N7002, SOT23), and Q50 (2N7002, SOT23).
- Diodes:** A diode D2 (BAS16, SOT23) is used for signal isolation.

Signal Connections:

- PLT_RST#:** Connected to the PLT_RST# signal and the W/L ON signal.
- ICH_SMBCLK:** Connected to the ICH_SMBCLK signal and the ICH_SMBDATA signal.
- LED_WLAN_OUT#:** Connected to the LED_WLAN_OUT# signal and the WIRELESS_LED_BT signal.
- WIRELESS_LED_BT:** Connected to the WIRELESS_LED_BT signal and the WIRELESS_LED signal.

The component is identified as MOLEX_67910-0002.

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<6/12> Remove PCM_SPK

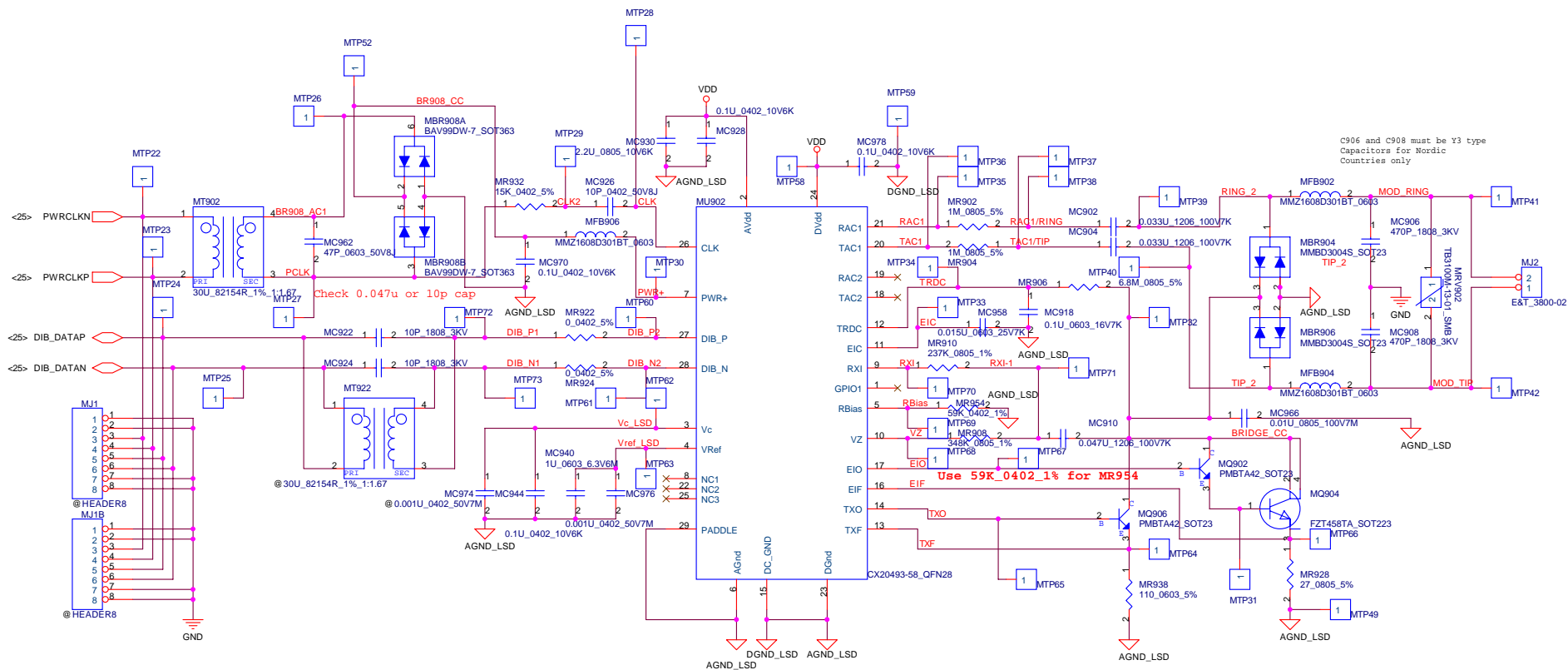
For Layout:

Place decoupling caps near the power pins of SmartAMC device.

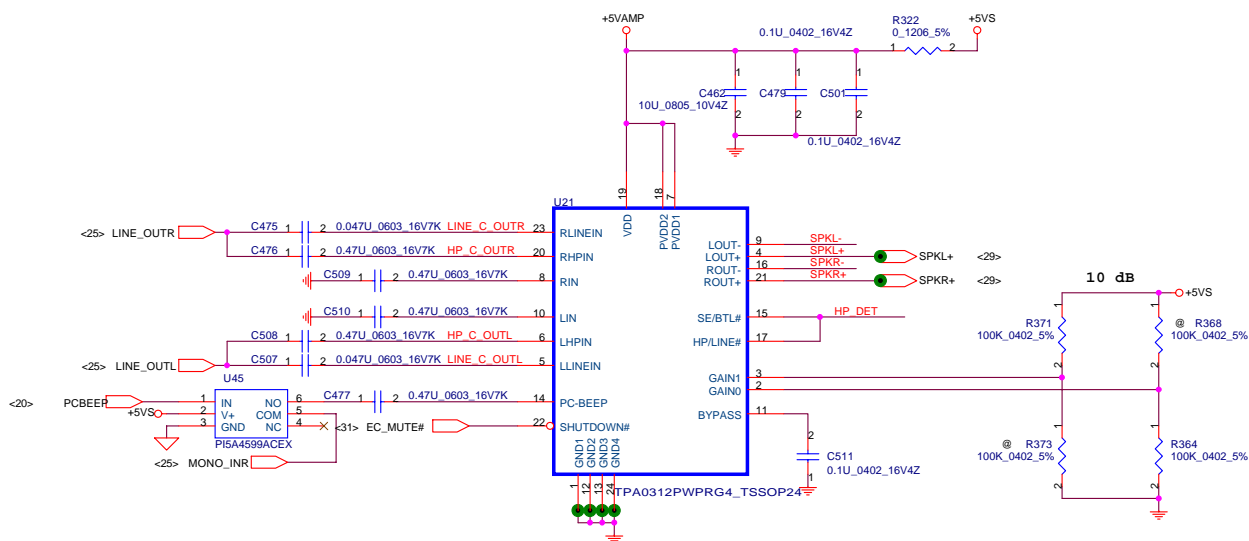
HP_DET#	JACK_DET#	PORT-A	PORT-B	EQ
0	0	ON	OFF	Disable
0	NC	ON	OFF	Disable
NC	0	OFF	ON	Disable
NC	NC	ON	OFF	Enable

MIC_DET	PORT-C	PORT-F
0	ON	OFF
NC	OFF	ON

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				Tuesday, June 20, 2006	0.2
				Sheet	25 of 40

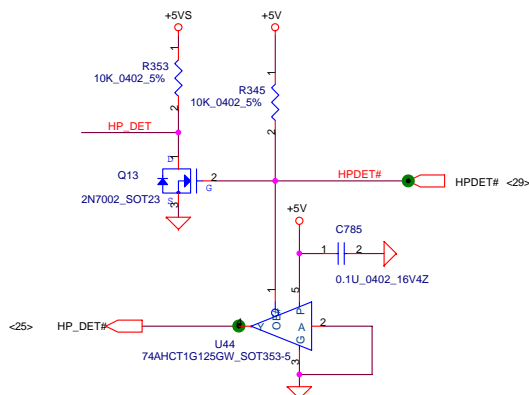
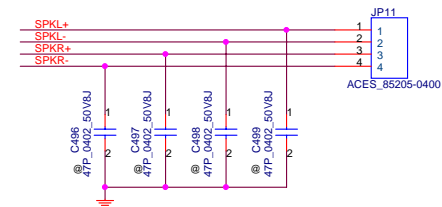


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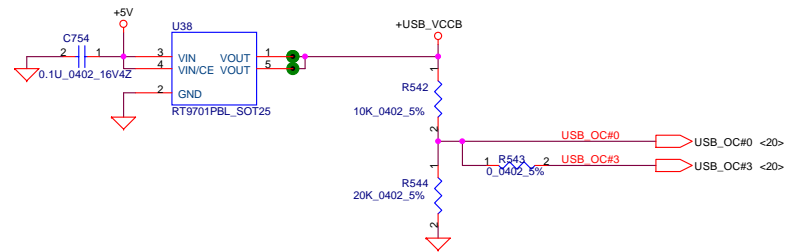


HEADPHONE OUT/LINE OUT

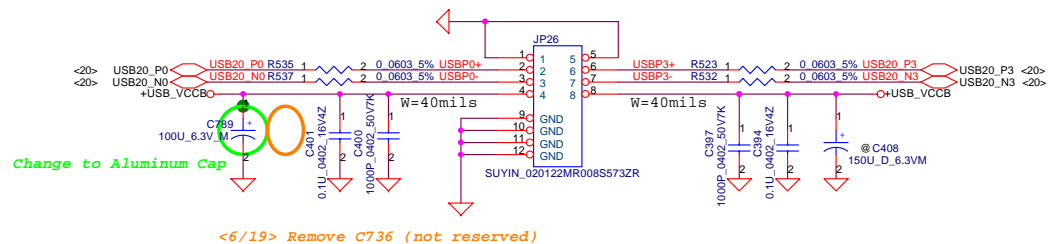
Gain Settings			
GAIN0	GAIN1	SE/BTL#	Av(inv)
0	0	0	6 dB
0	1	0	* 10 dB
1	0	0	15.6 dB
1	1	0	21.6 dB
X	X	1	4.1 dB



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Issued Date	2005/03/10	Deciphered Date	2006/03/10	AMP & Audio Jack	
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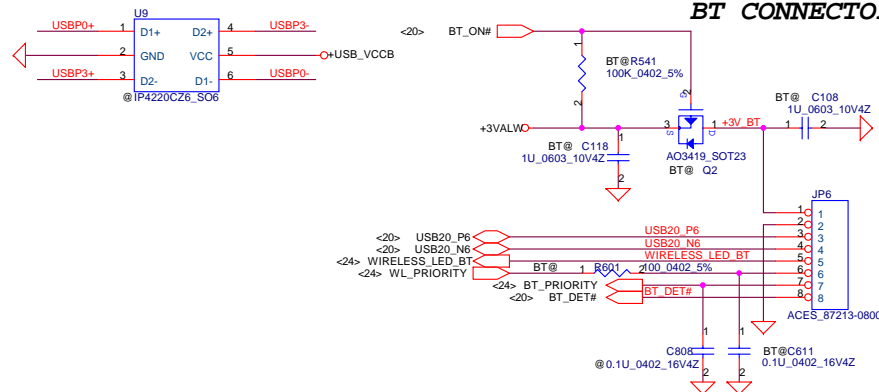


USB CONNECTOR (Left side)



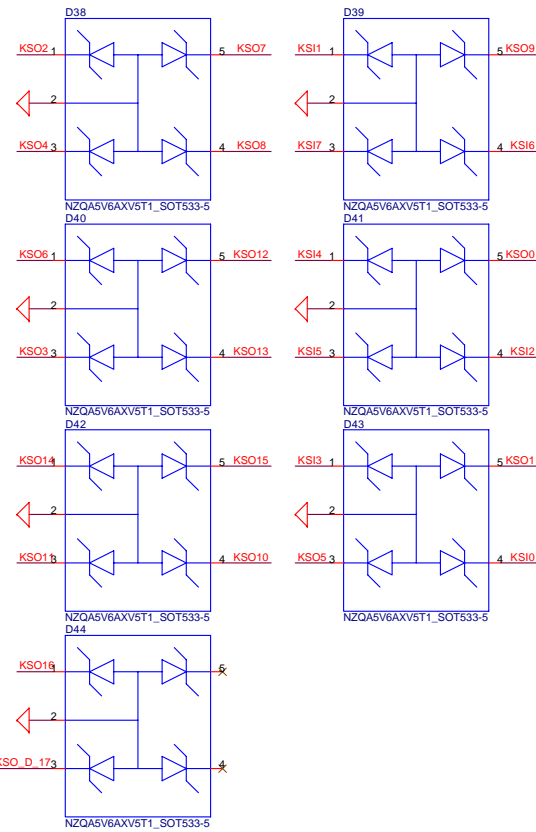
BT CONNECTOR

Reserve Bluetooth

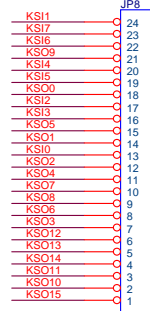


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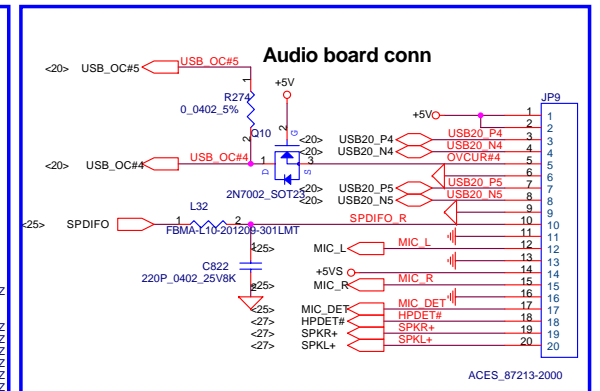
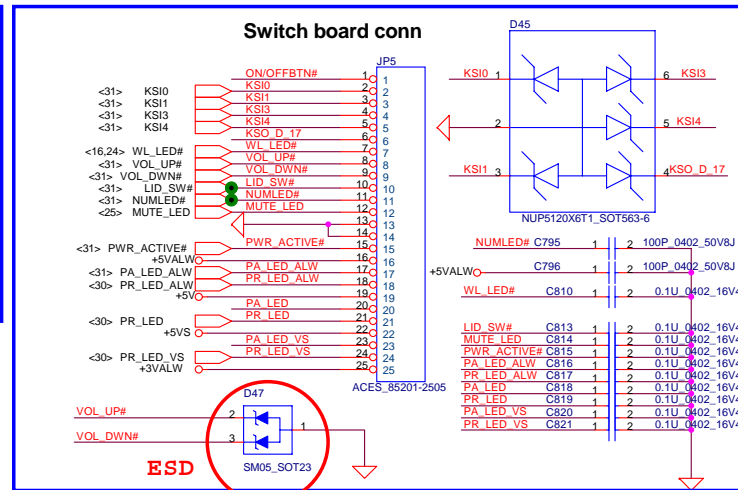
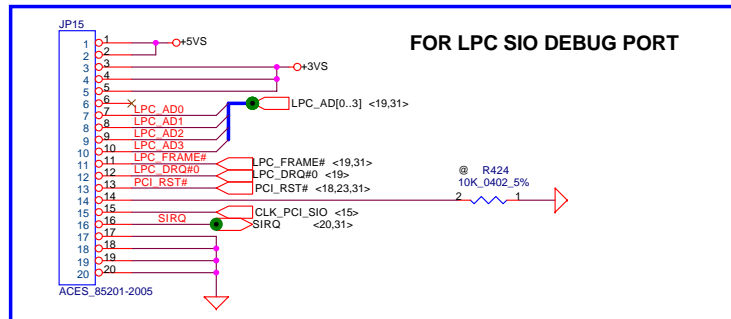
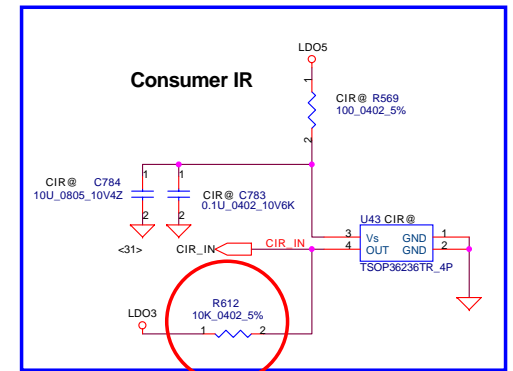
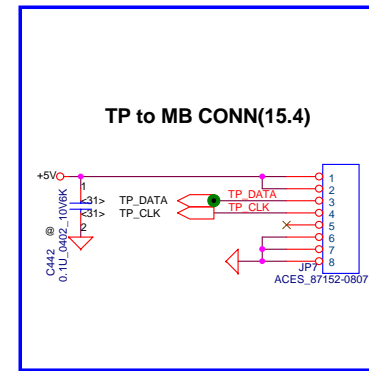
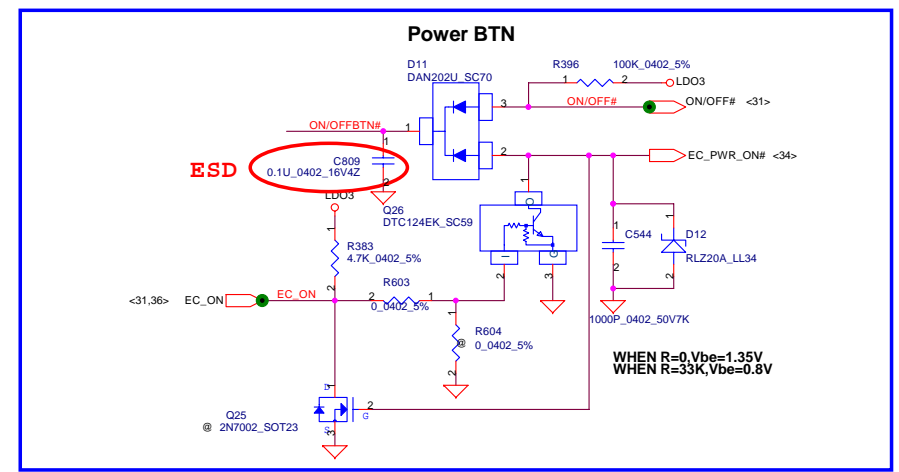
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15.4 (TYPE "C" KB)



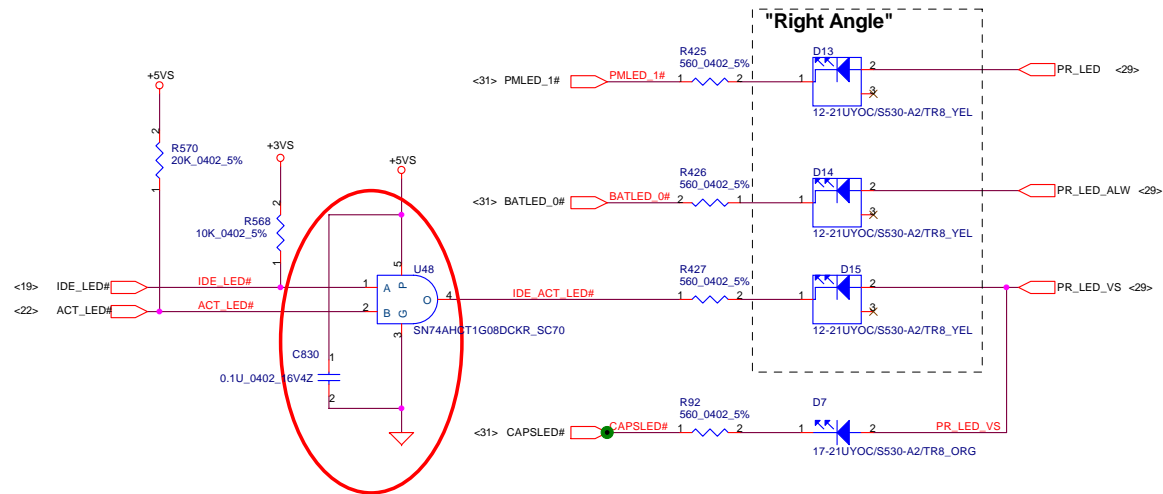
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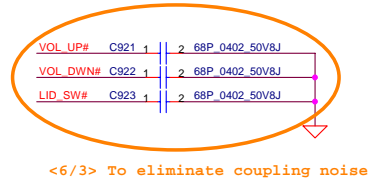
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For PR

FOR POWER BUTTON BACKLIGHT SYSTEM POWER

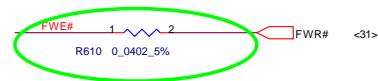
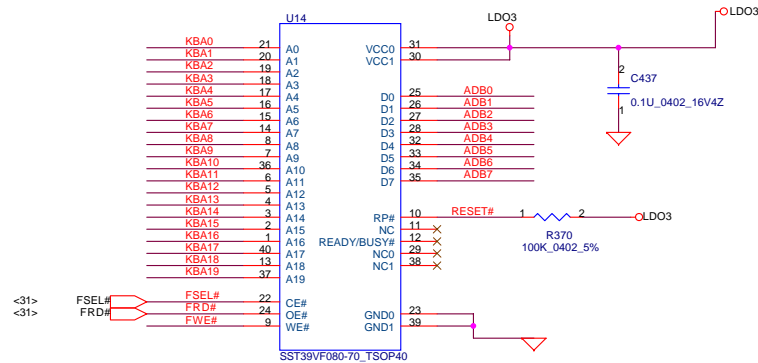
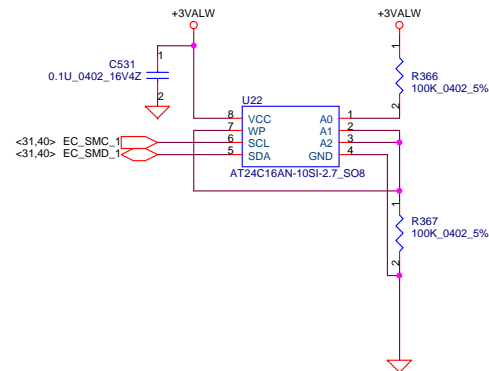
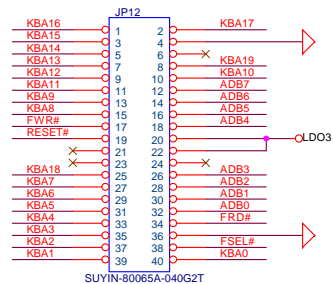


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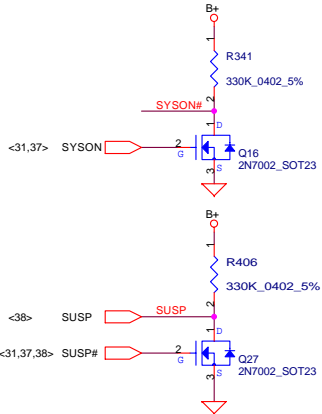
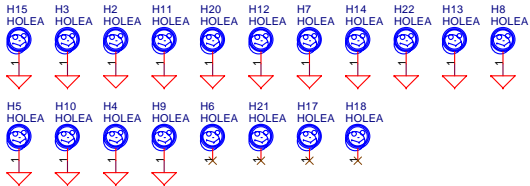
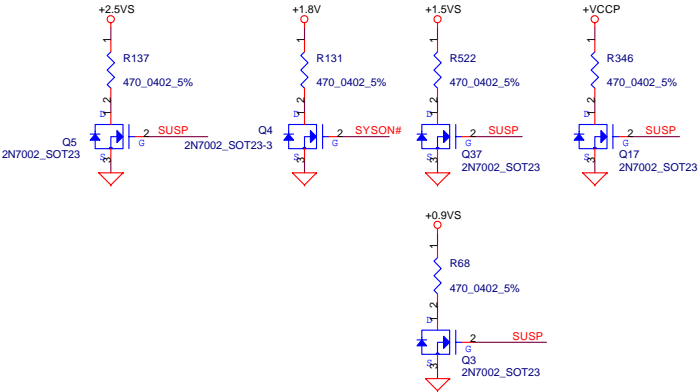
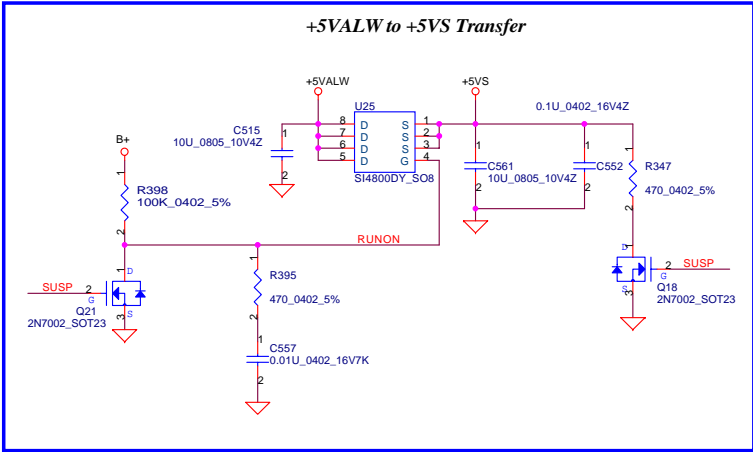
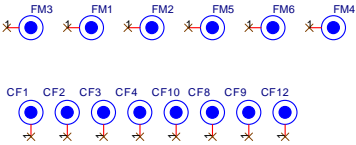
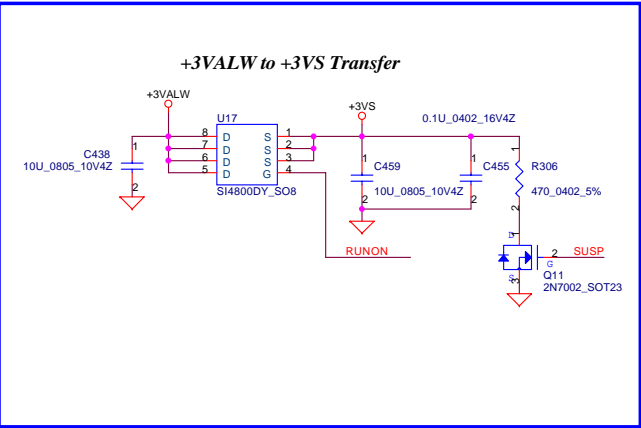
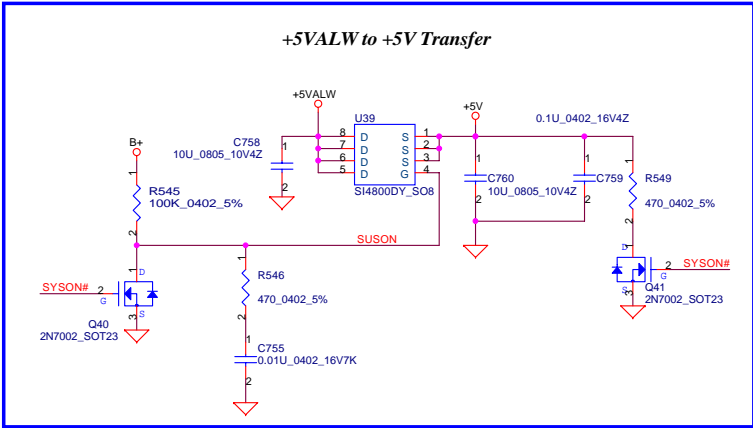


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					LA-3341P	
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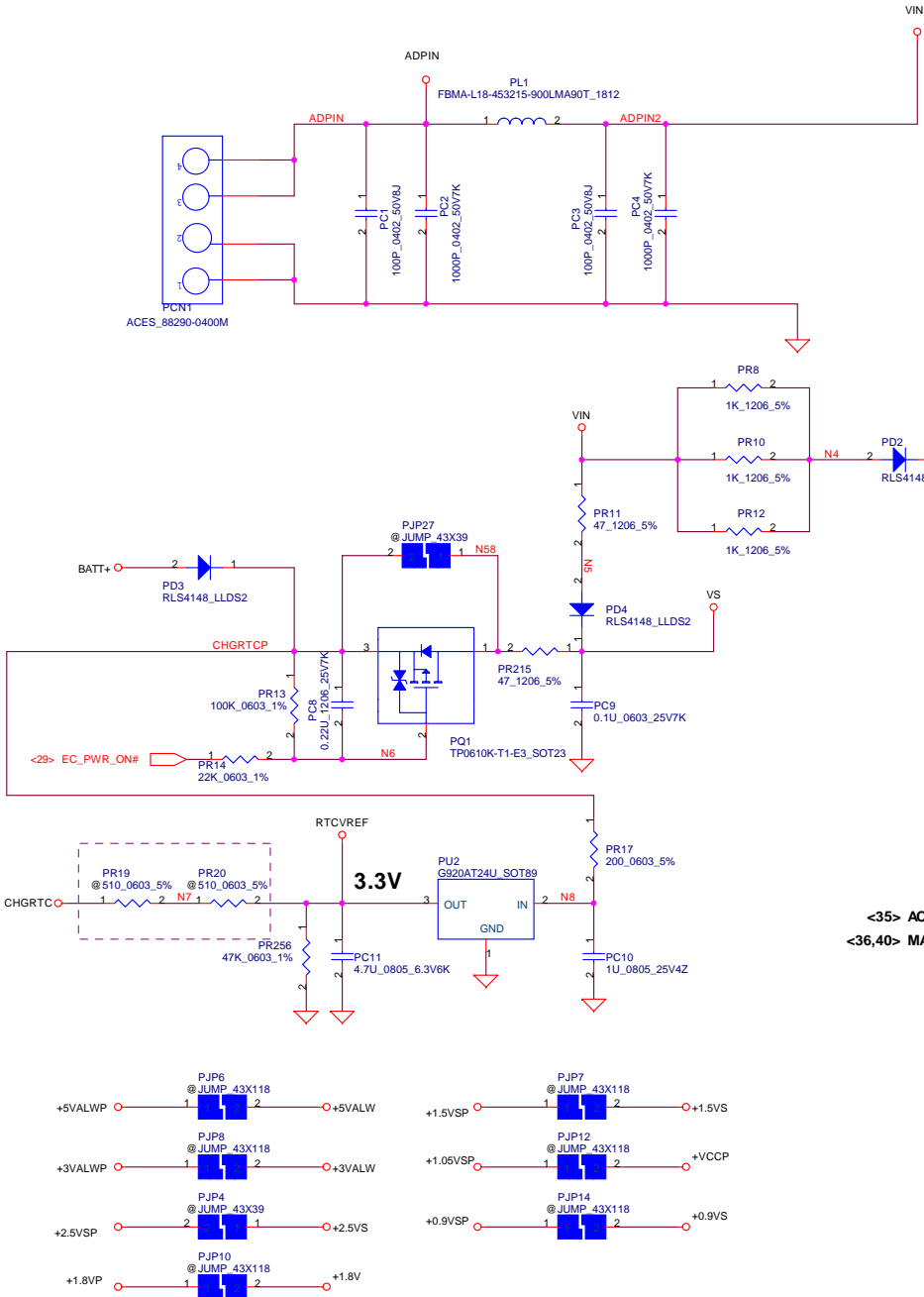
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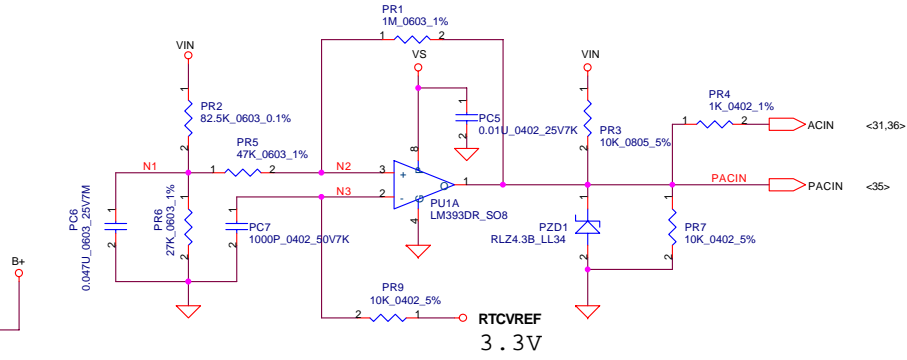
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				Date:	Tuesday, June 20, 2006
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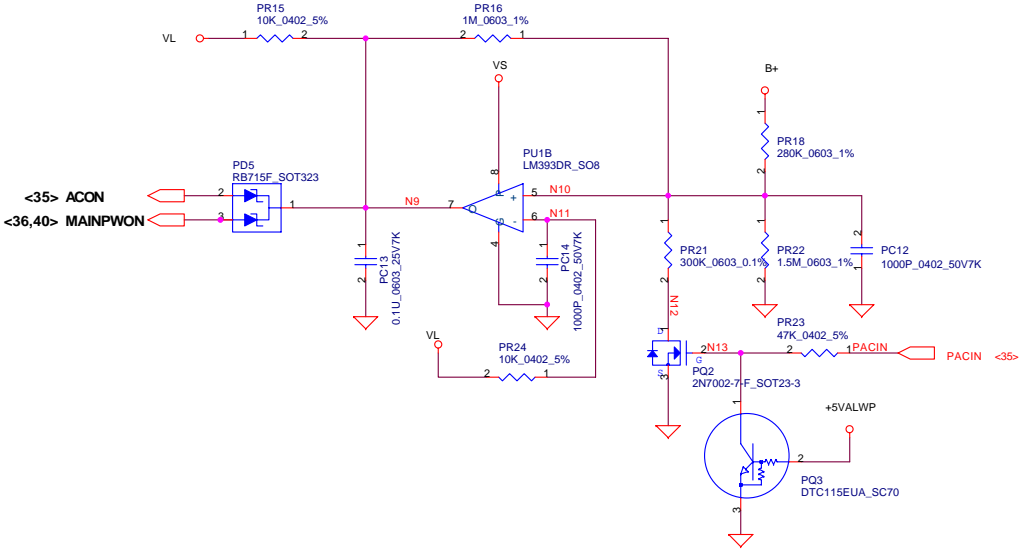


Vin Detector :			
14.698	14.285	13.879	
13.818	13.411	13.000	



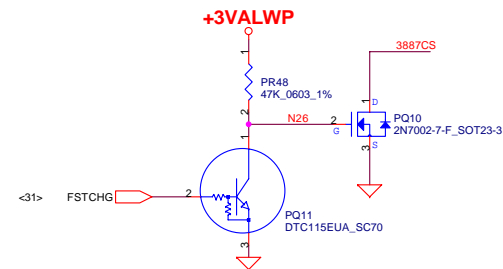
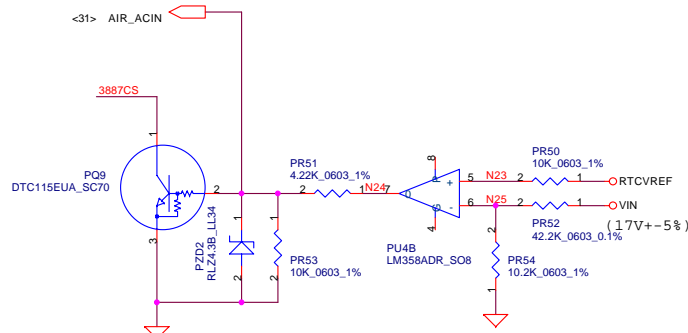
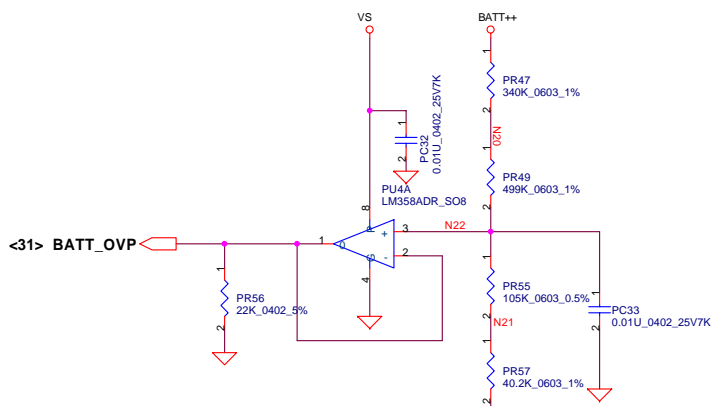
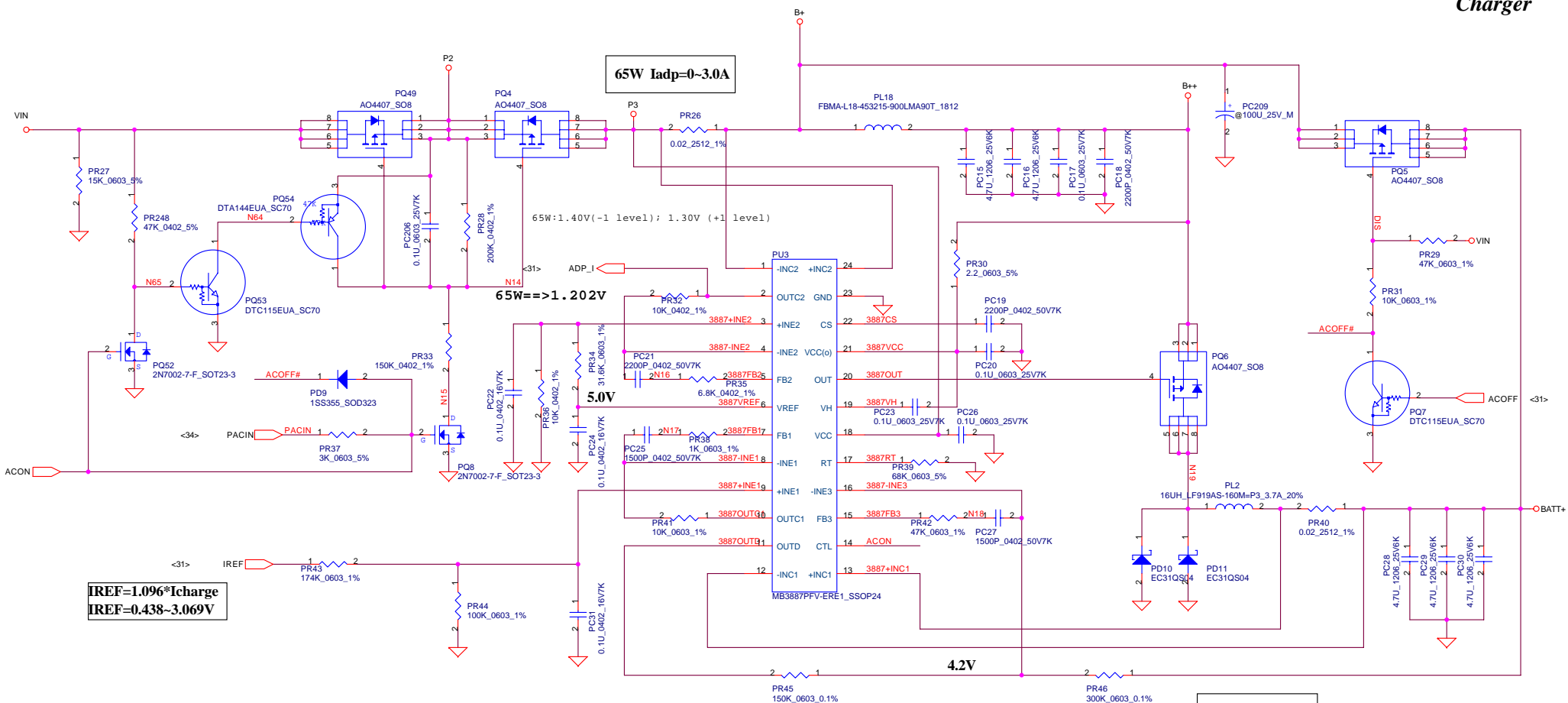
ACIN:			
Precharge detector			
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10.927	10.600	10.223	

BATT			
Precharge detector			
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6.108	5.933	5.704	



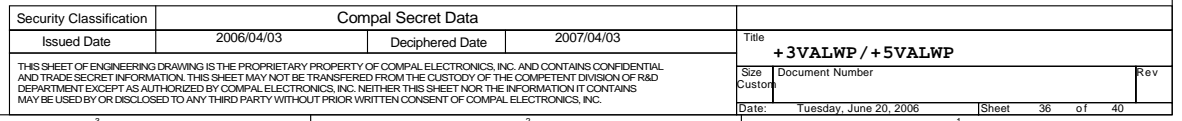
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						Size		Document Number		Rev	
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Charger

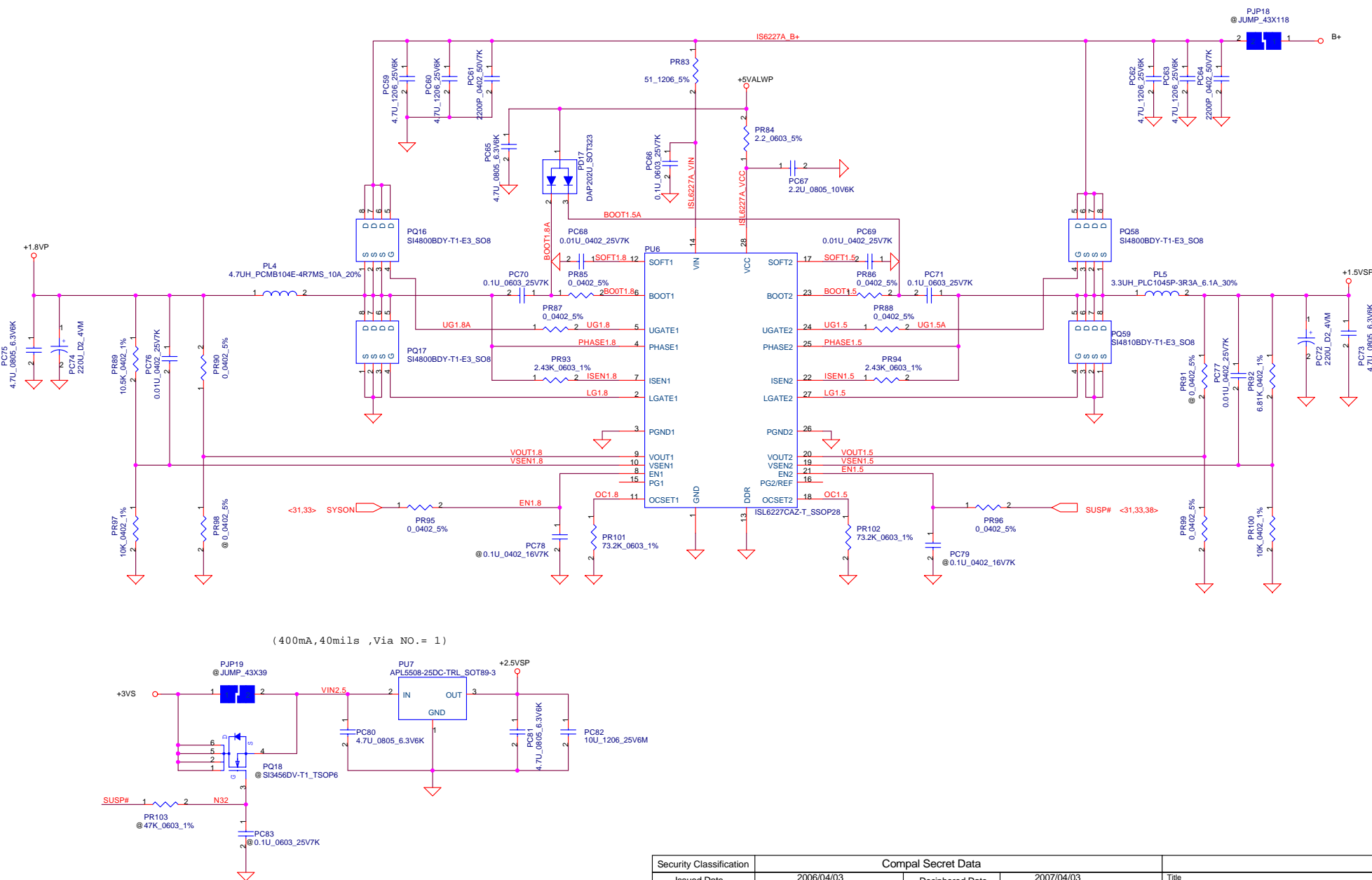


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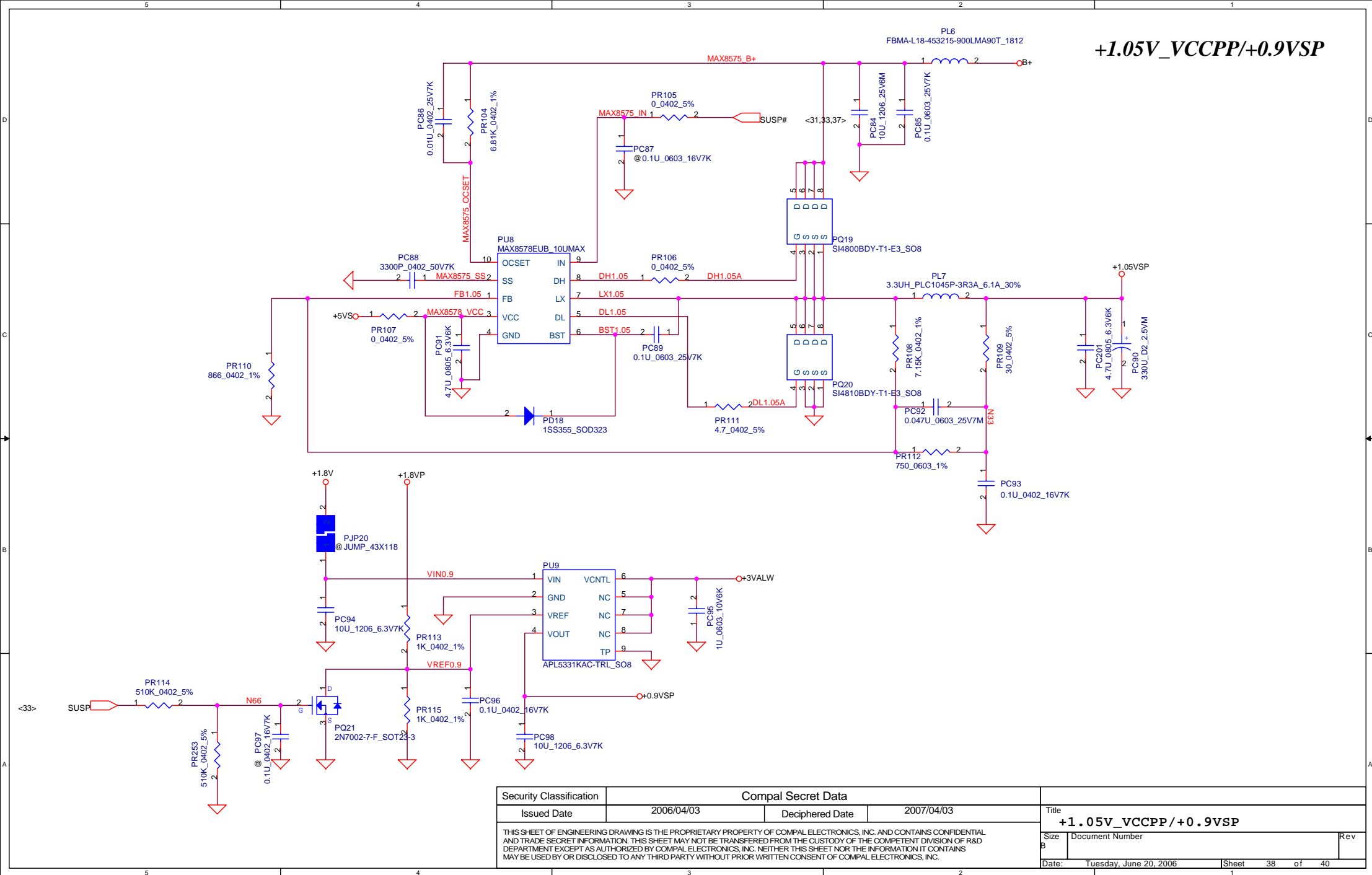
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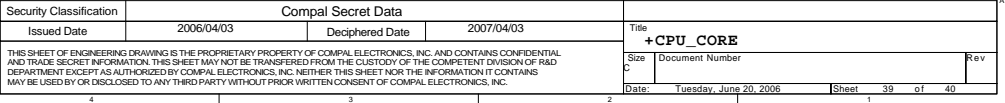


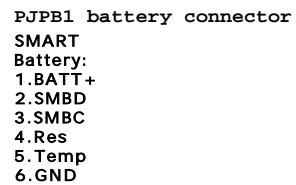
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