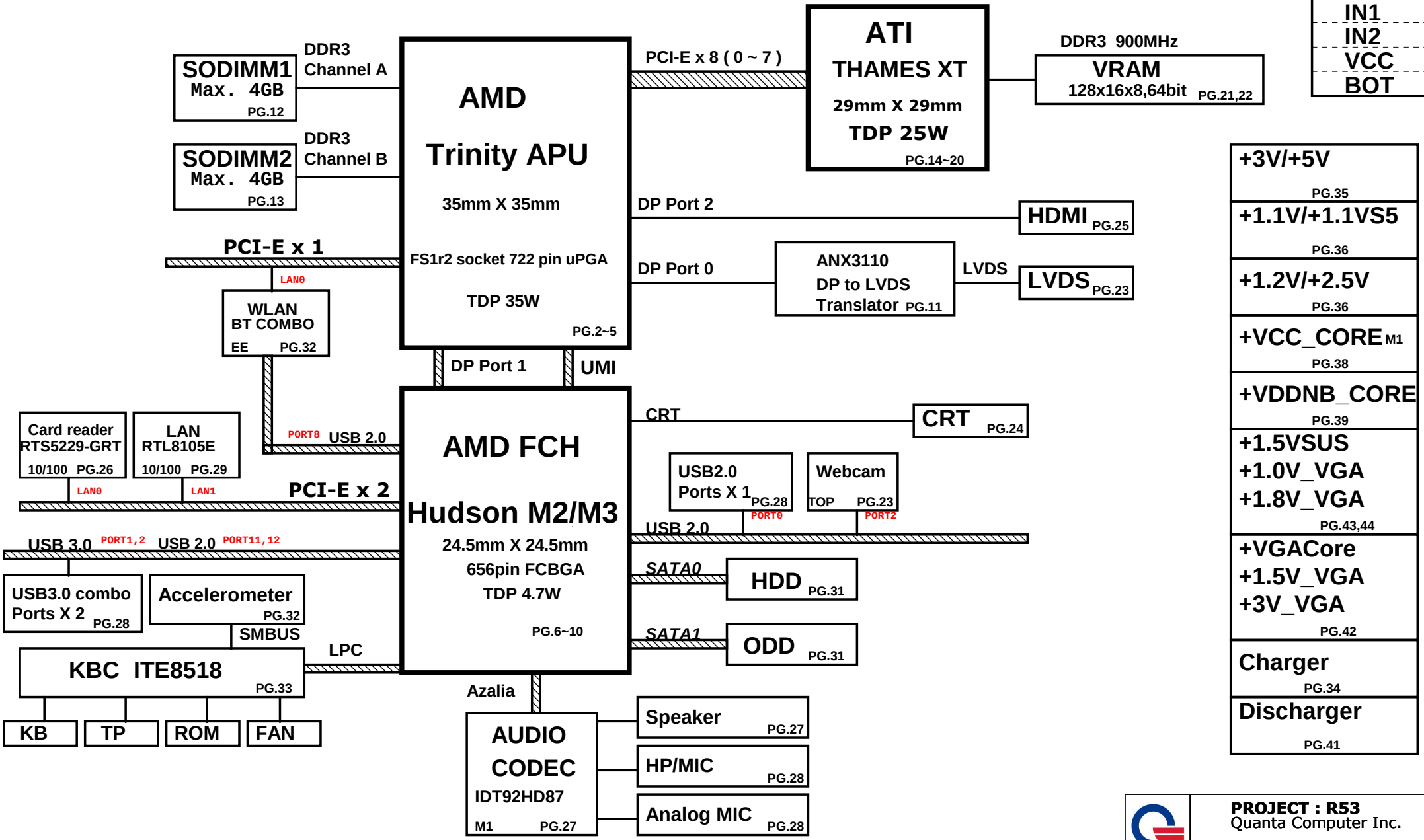
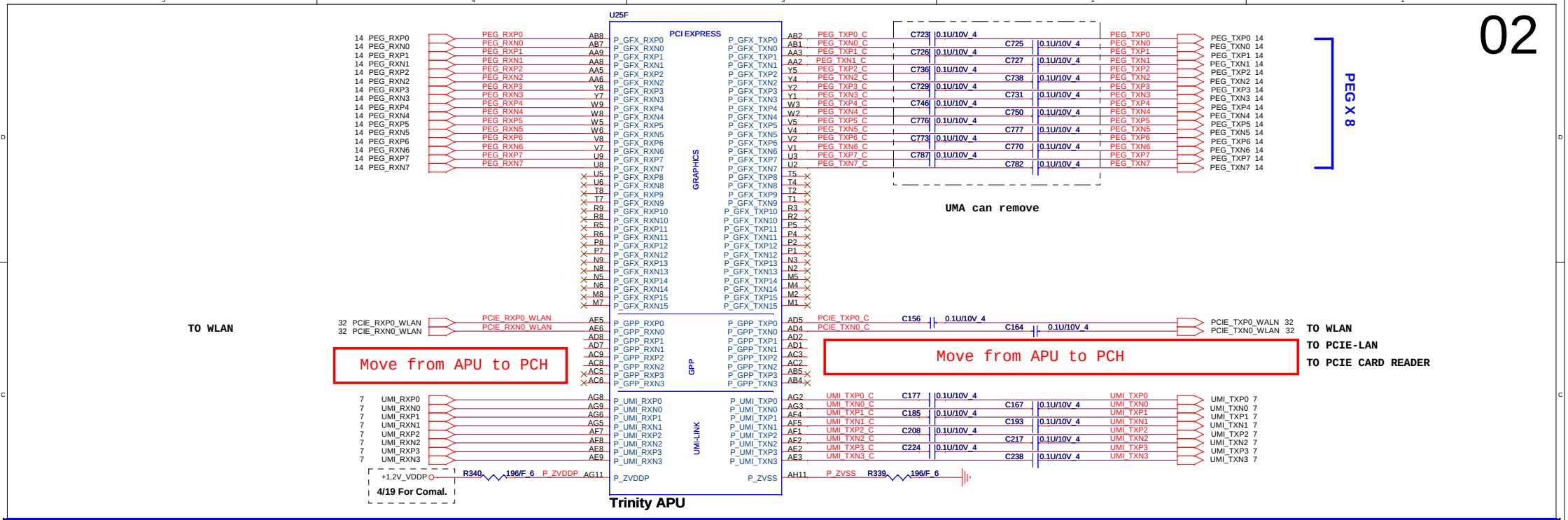
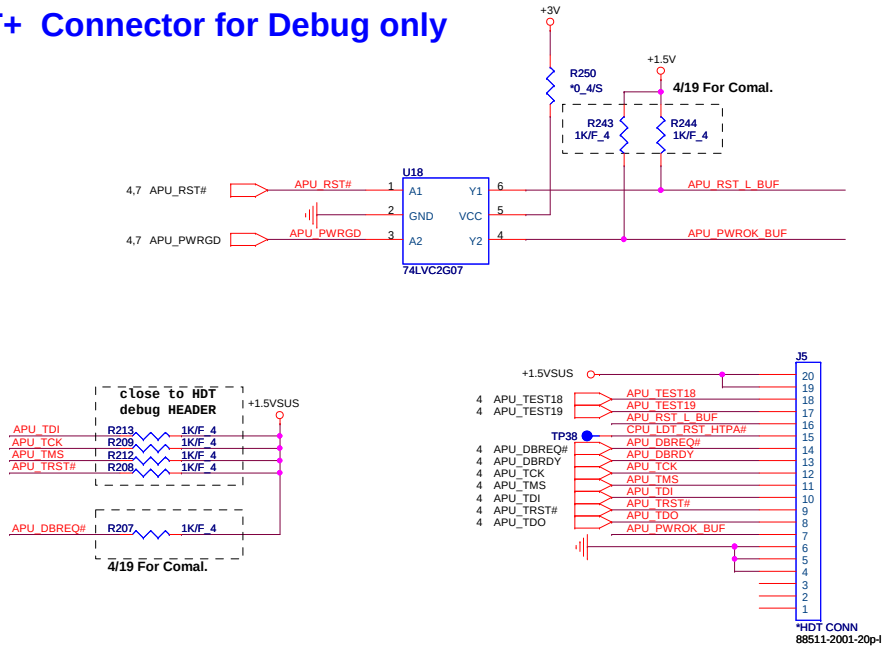
R53 AMD Comal UMA/Muxless SYSTEM DIAGRAM



PROJECT : R53 Quanta Computer Inc.		
Size Custom	Document Number BLOCK EE DIAGRAM	Rev 1A
Date: Tuesday, November 22, 2011	Sheet 1 of 44	

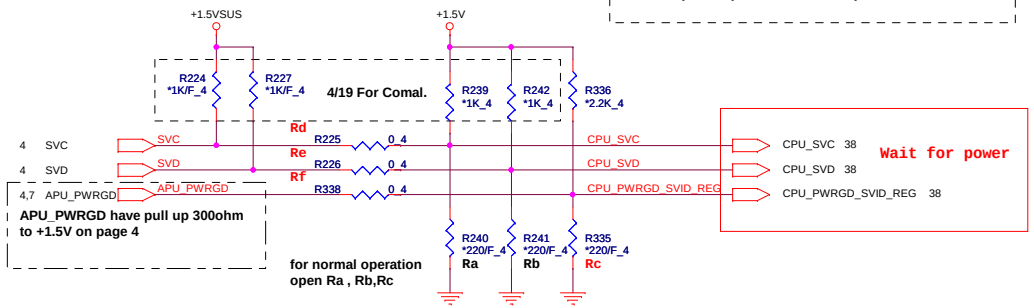


HDT+ Connector for Debug only



VID Override Circuit

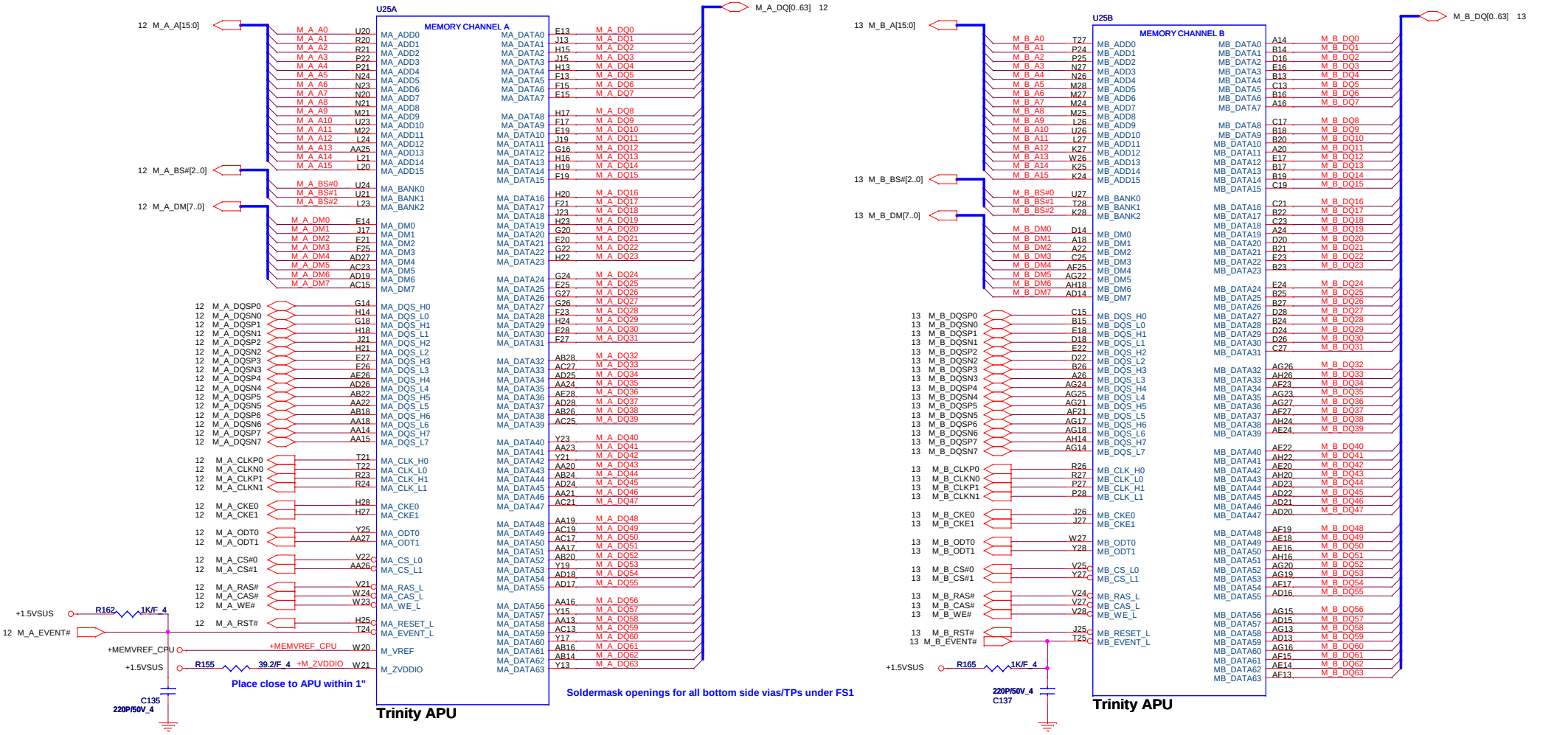
		BOOT VOLTAGE	
SVC	SVD	VFIX_+VDD =VCC/GND	VFIX_+VDD =OPEN
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8

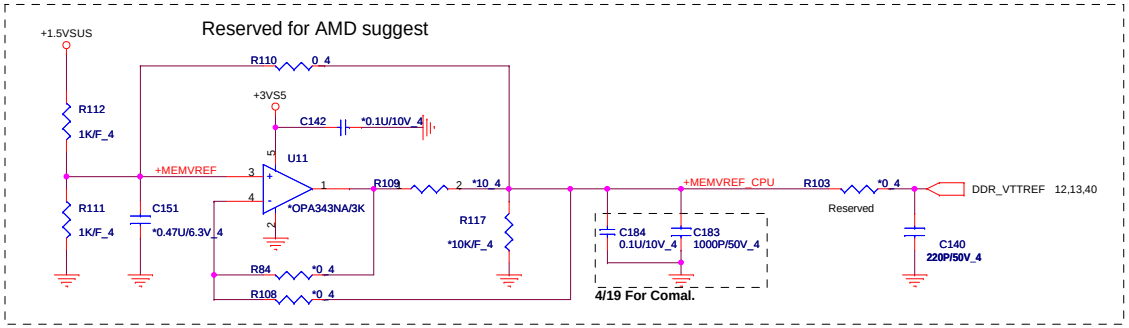


PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Llano PCIE/UMI/GPP	1A

Date: Monday, November 14, 2011 Sheet 2 of 44

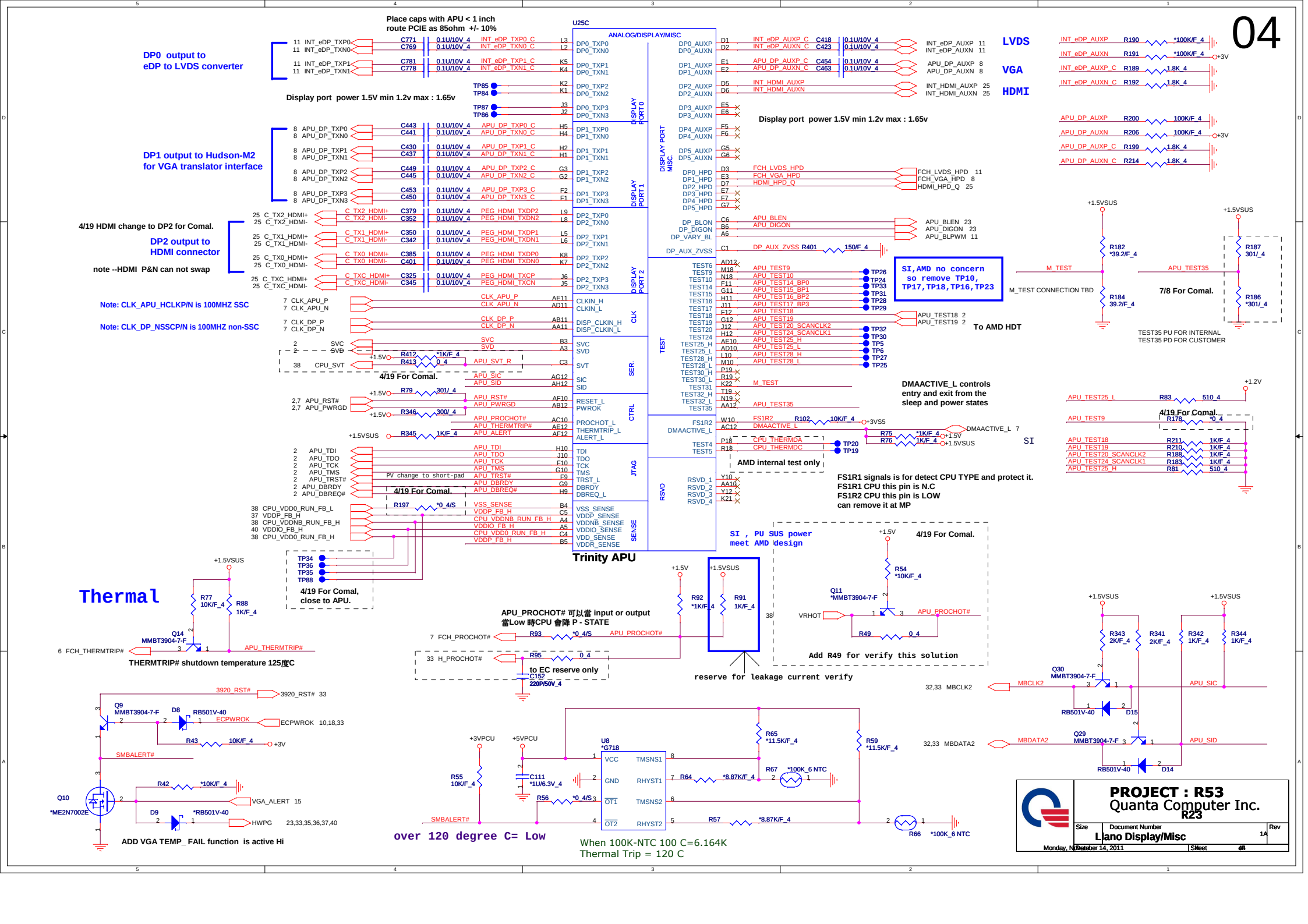




PROJECT : R53
Quanta Computer Inc.

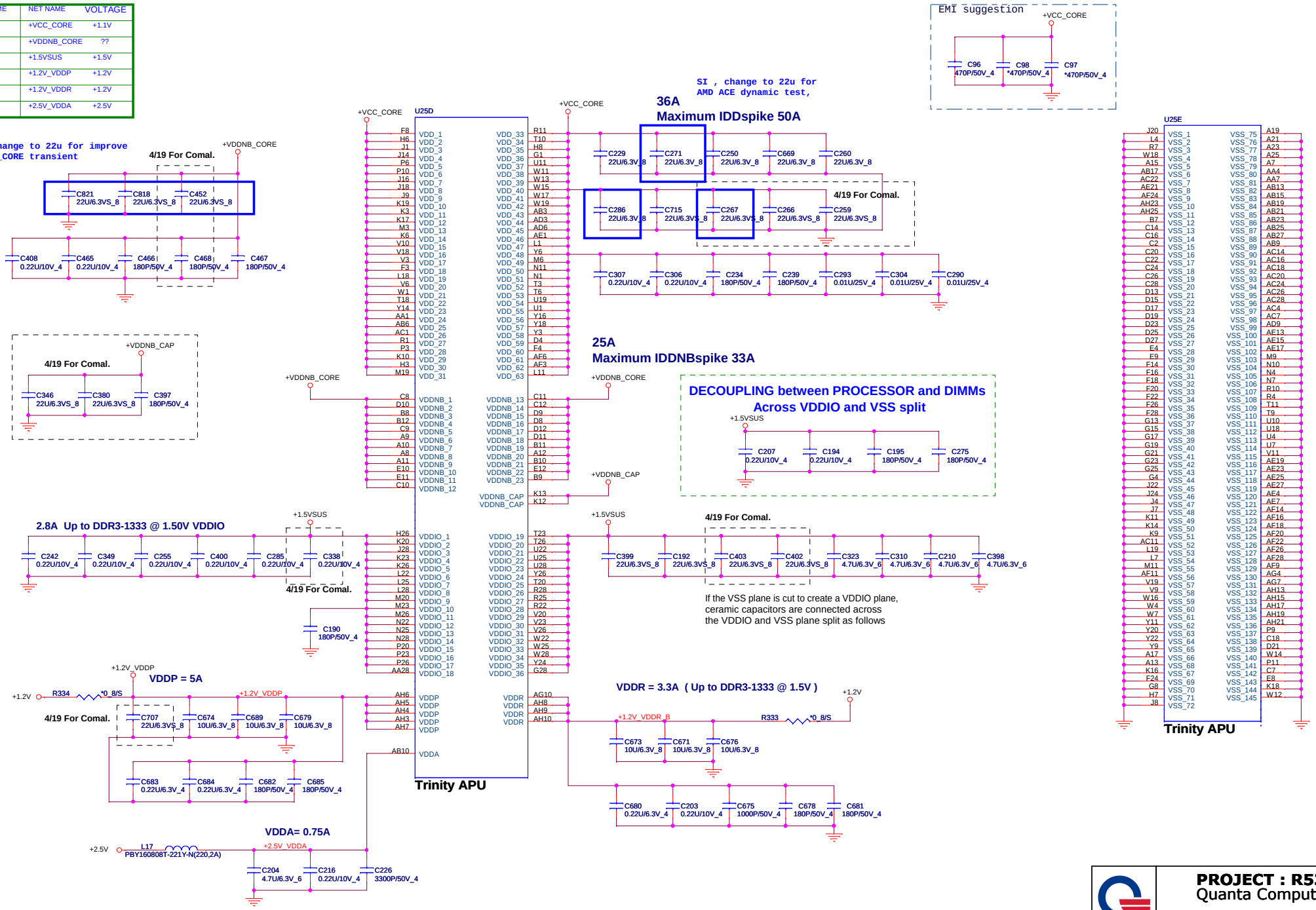
Size	Document Number	Rev
Custom	Llano DDR3 MEM I/F	1A

Date: Monday, November 14, 2011 | Sheet 3 of 44


04
Place caps with APU < 1 inch
route PCIE as 85ohm +/- 10%
U25C
ANALOG/DISPLAY/MISC
DP0 output to
eDP to LVDS converter
Display port power 1.5V min 1.2v max : 1.65v
DP1 output to Hudson-M2
for VGA translator interface
4/19 HDMI change to DP2 for Comal.
DP2 output to
HDMI connector
note --HDMI P&N can not swap
Note: CLK_APU_HCLKP/N is 100MHZ SSC
Note: CLK_DP_NSSCP/N is 100MHZ non-SSC
4/19 For Comal.
4/19 For Comal,
close to APU.
Trinity APU
LVDS
VGA
HDMI
Display port power 1.5V min 1.2v max : 1.65v
SI,AMD no concern
so remove TP10,
TP17,TP18,TP16,TP23
To AMD HDT
M_TEST CONNECTION TBD
7/8 For Comal.
TEST35 PU FOR INTERNAL
TEST35 PD FOR CUSTOMER
DMAACTIVE_L controls
entry and exit from the
sleep and power states
SI
AMD internal test only
FS1R1 signals is for detect CPU TYPE and protect it.
FS1R1 CPU this pin is N.C
FS1R2 CPU this pin is LOW
can remove it at MP
SI , PU SUS power
meet AMD design
4/19 For Comal.
Add R49 for verify this solution
reserve for leakage current verify
APU_PROCHOT# 可以當 input or output
當Low 時CPU 會降 P - STATE
to EC reserve only
Thermal
THERMTRIP# shutdown temperature 125度C
ADD VGA TEMP_ FAIL function is active Hi
over 120 degree C= Low
When 100K-NTC 100 C=6.164K
Thermal Trip = 120 C
PROJECT : R53
Quanta Computer Inc.
R23
Size
Document Number
Llano Display/Misc
Rev
1A
Monday, November 14, 2011
Sheet
44

APU POWER TABLE

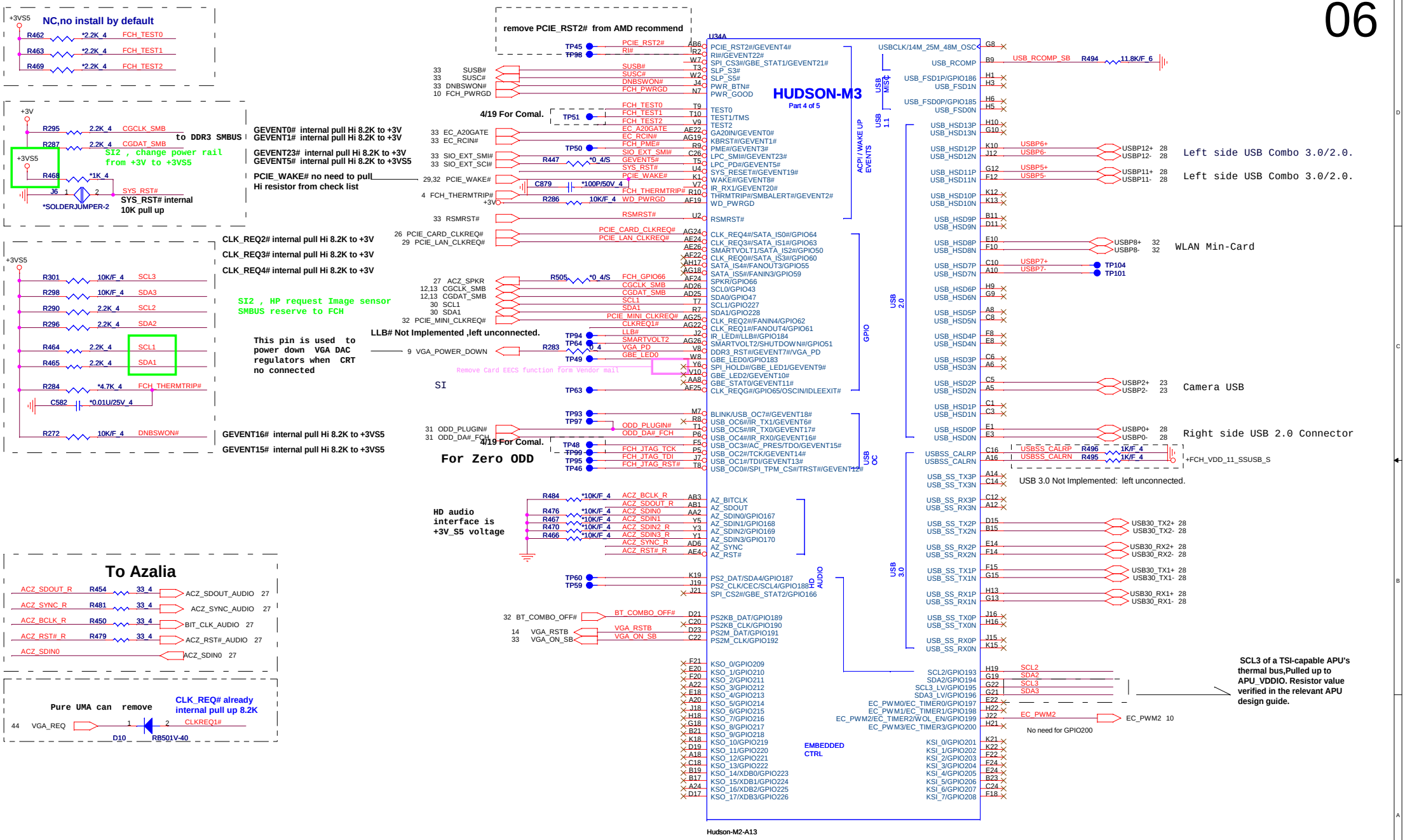
PIN NAME	NET NAME	VOLTAGE
VDD	+VCC_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V



PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Llano POWER/GND	1A

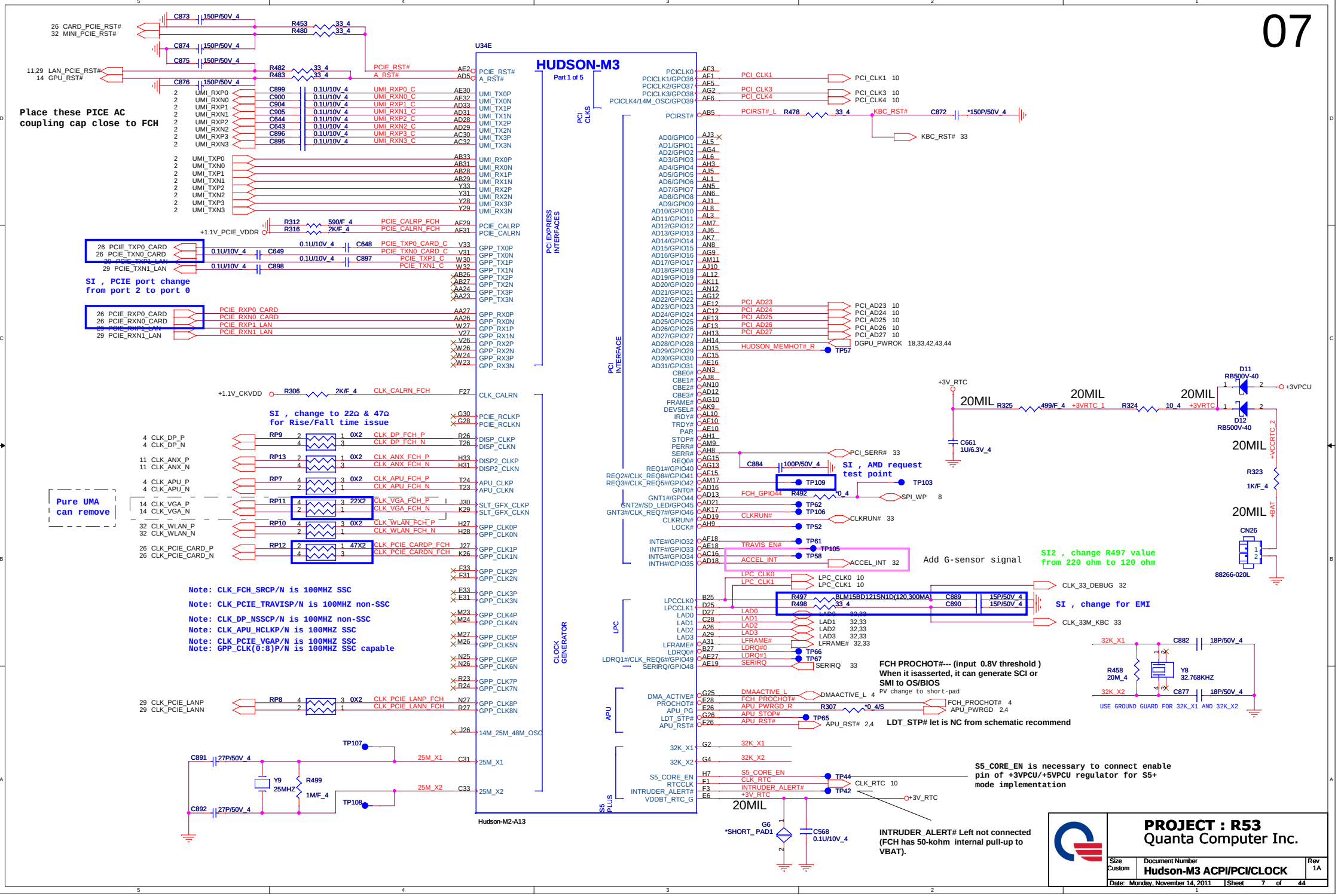
Date: Friday, November 11, 2011 Sheet 5 of 44



PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Hudson-M3 GPIO/USB/AZ/RGMII	1A

Date: Friday, November 11, 2011 Sheet 6 of 44



PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Hudson-M3 ACPI/PCI/CLOCK	1A

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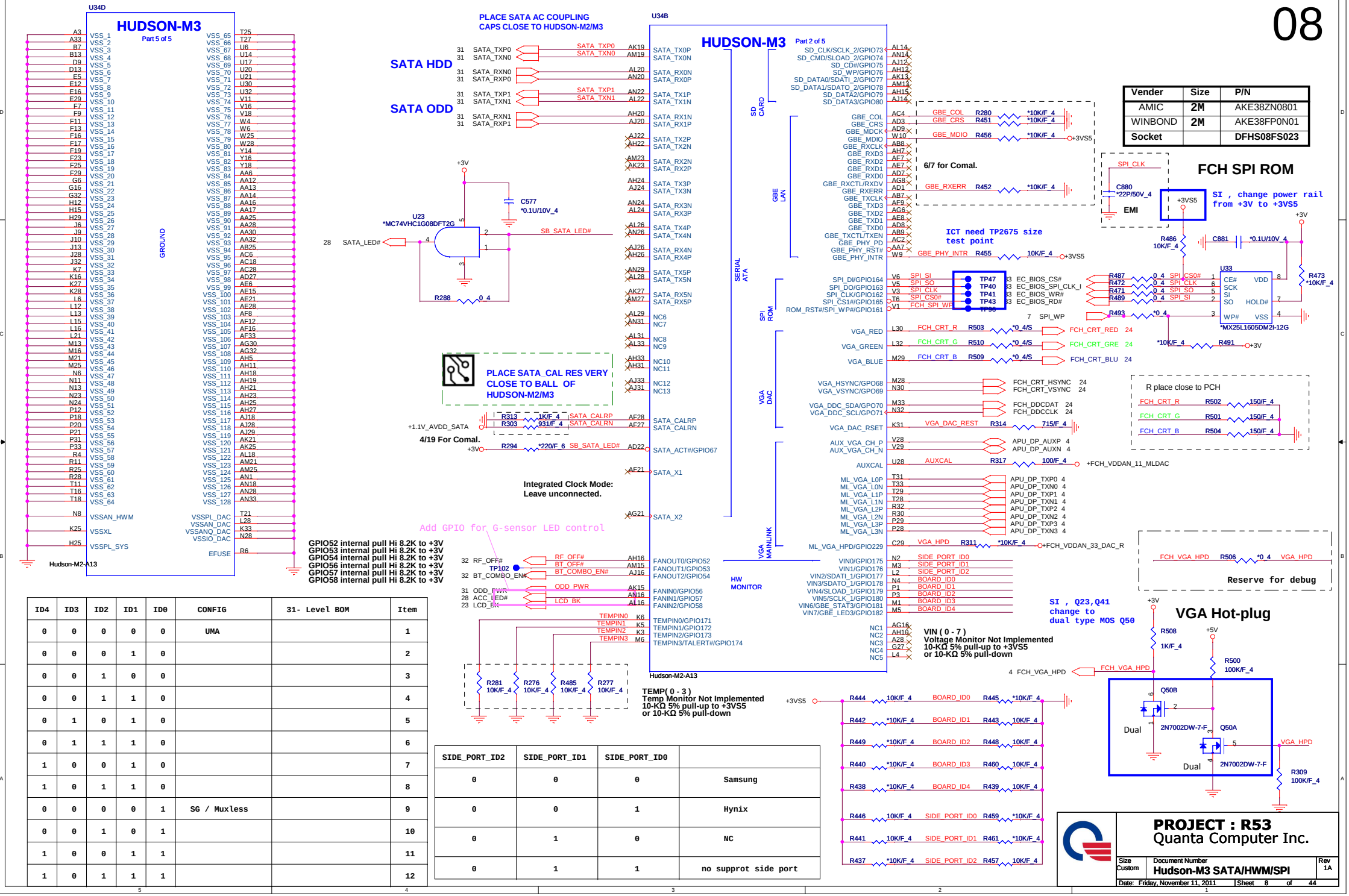
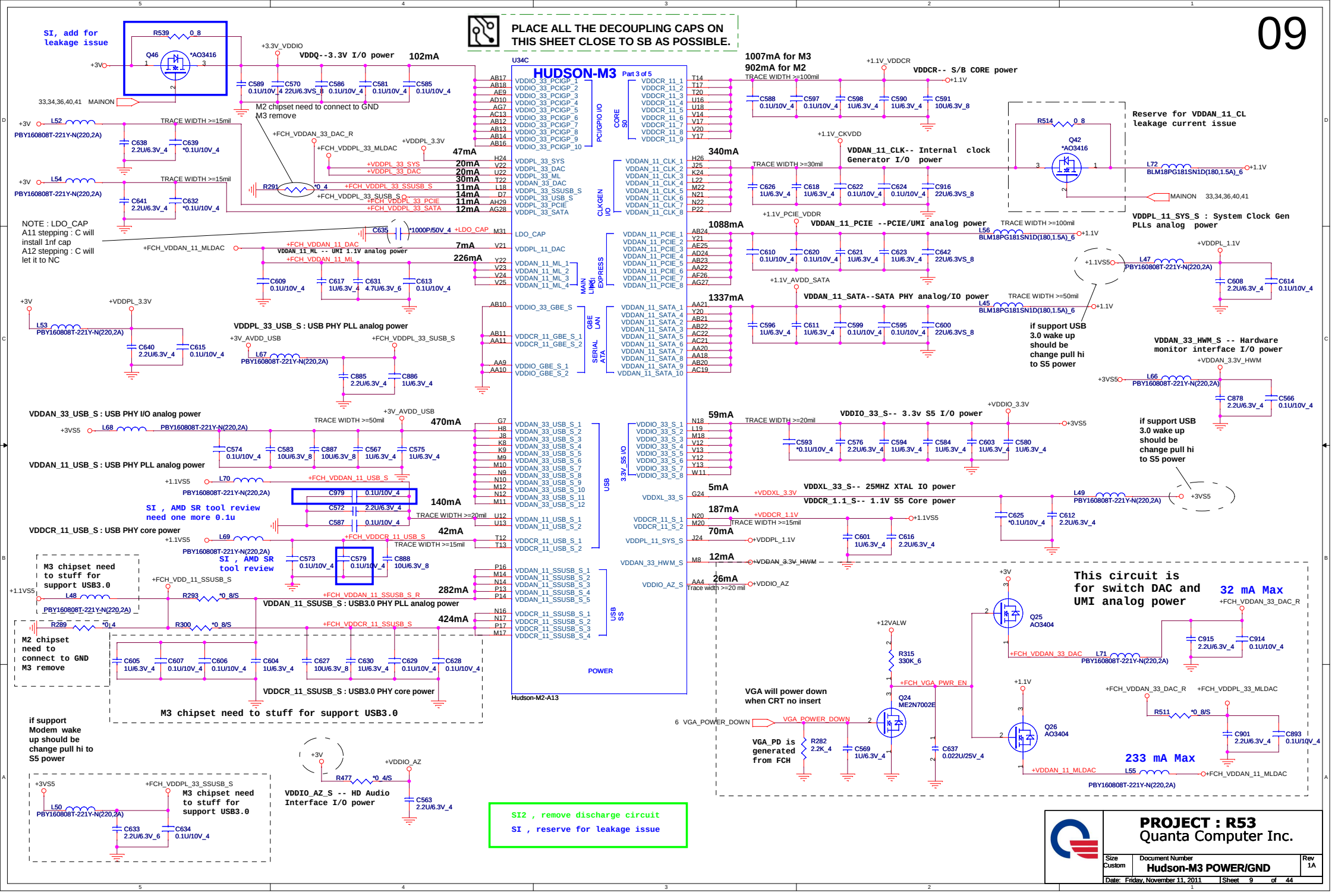


Vender	Size	P/N
AMIC	2M	AKE38ZN0801
WINBOND	2M	AKE38FP0N01
Socket		DFHS08FS023

ID4	ID3	ID2	ID1	ID0	CONFIG	31- Level BOM	Item
0	0	0	0	0	UMA		1
0	0	0	1	0			2
0	0	1	0	0			3
0	0	1	1	0			4
0	1	0	1	0			5
0	1	1	1	0			6
1	0	0	1	0			7
1	0	1	1	0			8
0	0	0	0	1	SG / Muxless		9
0	0	1	0	1			10
1	0	0	1	1			11
1	0	1	1	1			12

SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	0	Samsung
0	0	1	Hynix
0	1	0	NC
0	1	1	no supprot side port



PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Hudson-M3 POWER/GND	1A

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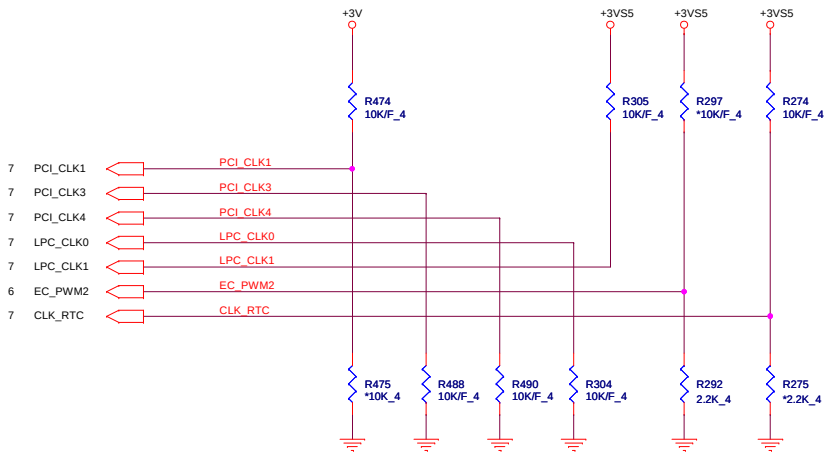
STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



REQUIRED STRAPS

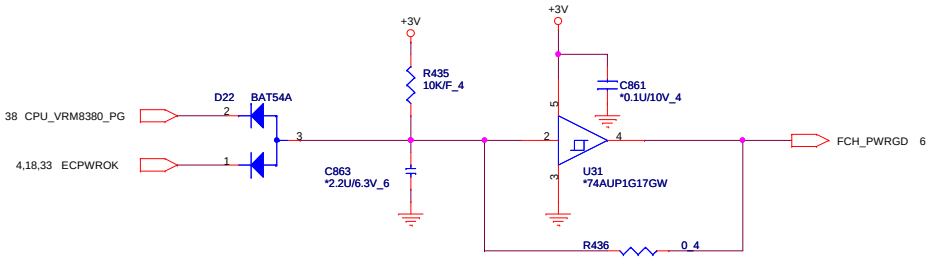
	--------	PCI_CLK1	--------	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH	--------	ALLOW PCIE Gen2 DEFAULT	--------	USE DEBUG STRAP	non_Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE ENABLED
PULL LOW	--------	FORCE PCIE Gen1	--------	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM	S5 PLUS MODE DISABLED DEFAULT

DEBUG STRAPS

FCH has 15K Internal Pull Up for PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

FCH PWRGD



PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Hudson-M3 STRAP/PWRGD	1A

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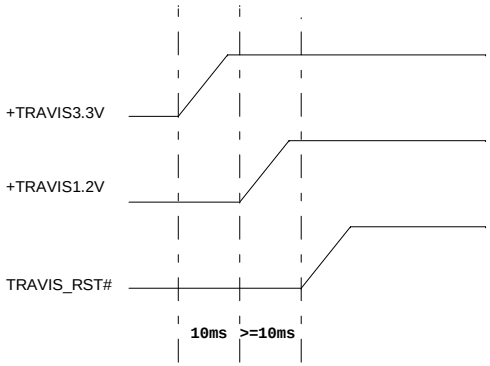
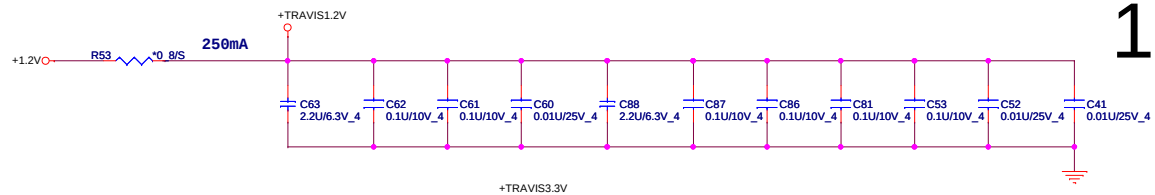
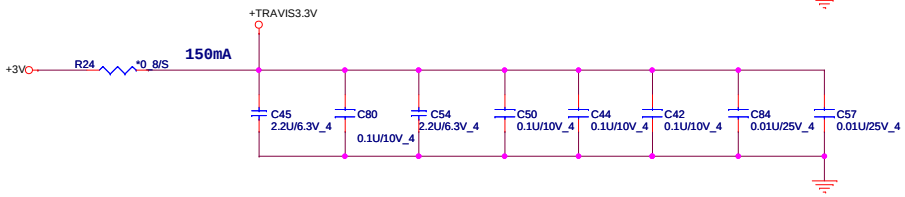
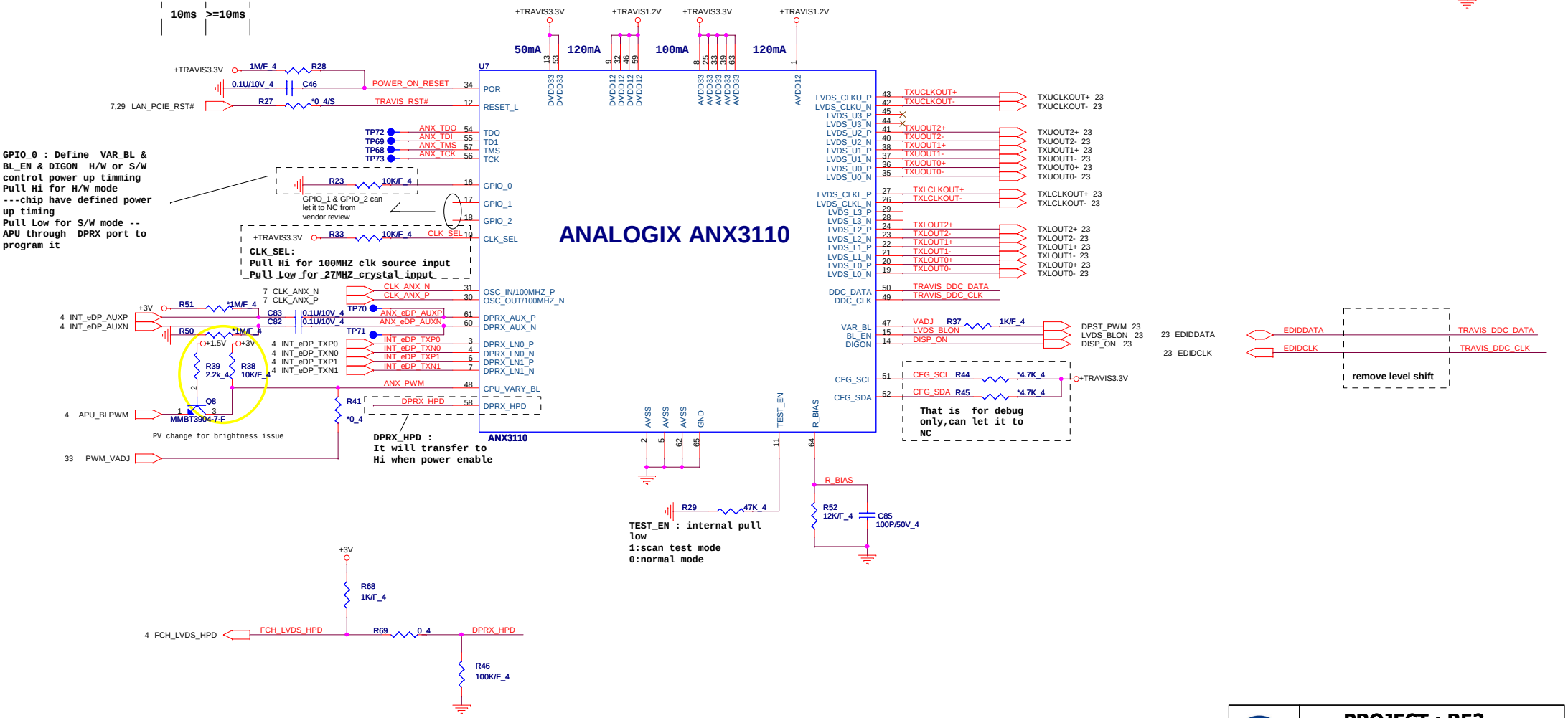
ANX3110 Power Up Sequence

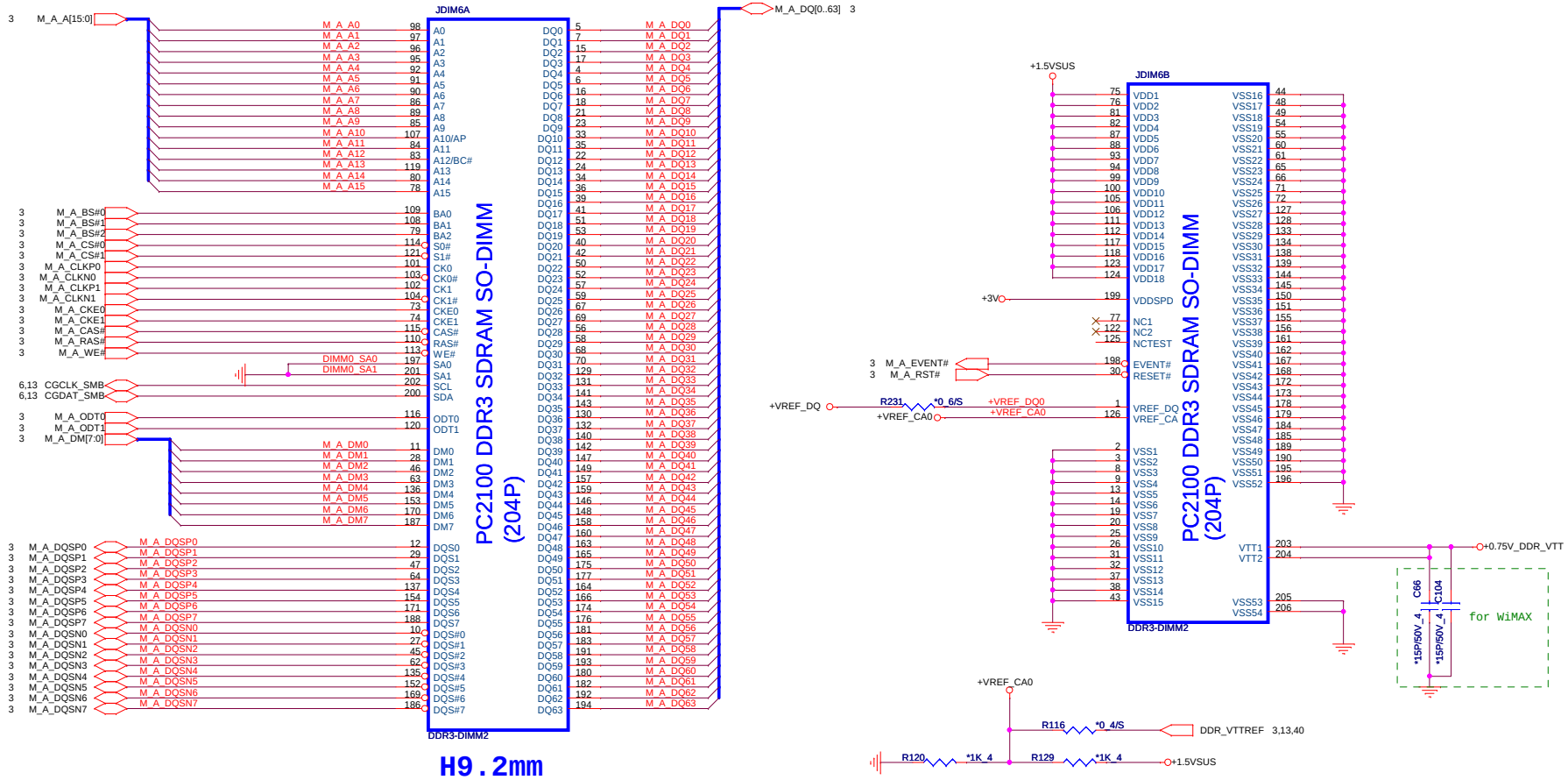




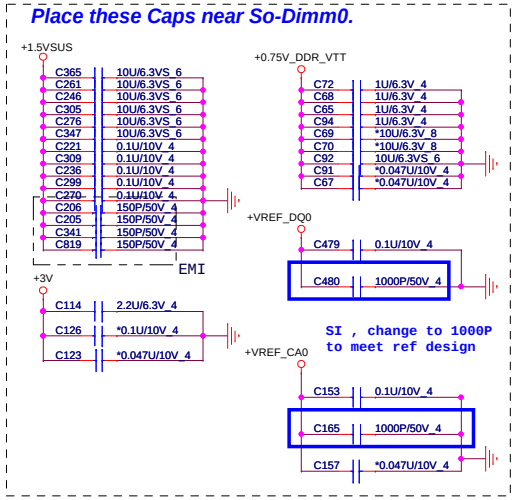


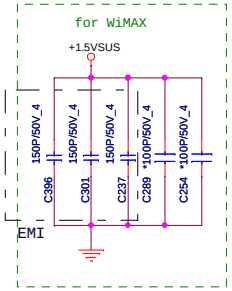


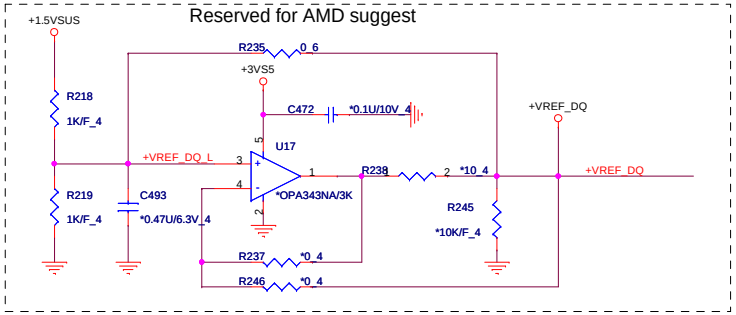
PROJECT : R53 Quanta Computer Inc.		
Size Custom	Document Number **ANX3110**	Rev 1A
Date: Friday, November 11, 2011	Sheet 11 of 44	



H9.2mm







13,40 +0.75V_DDR_VTT
2,3,4,5,13,40,41,44 +1.5VSUS
2,4,6,8,9,10,11,13,14,18,23,24,25,26,27,28,29,30,31,32,33,41,42,44 +3V

PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-0	1A

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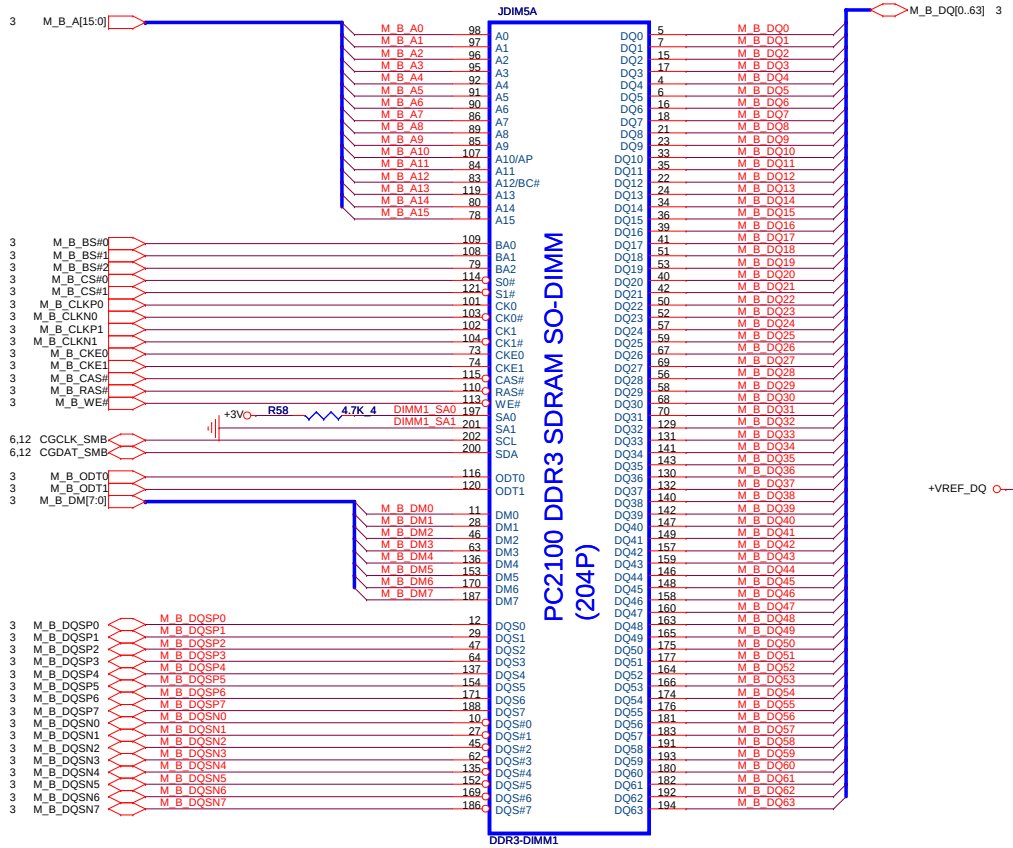
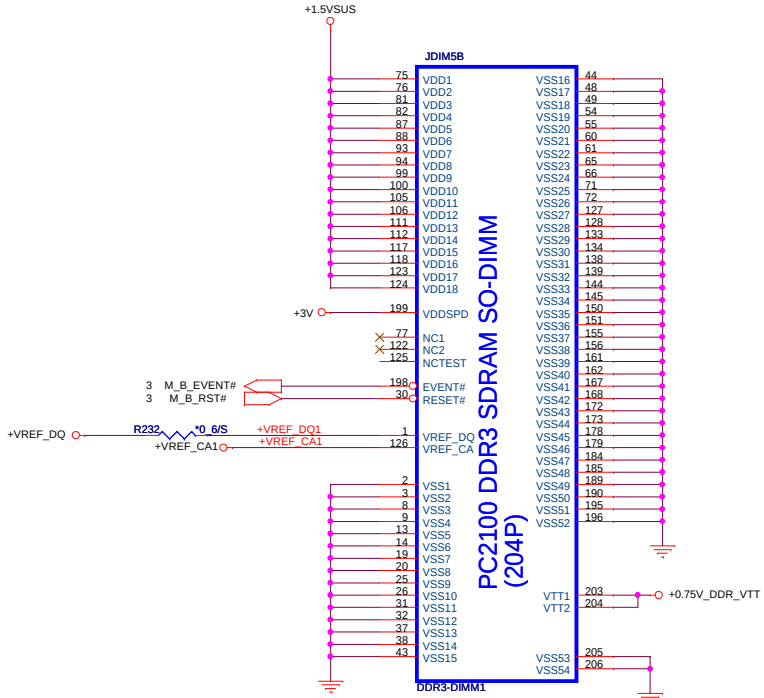
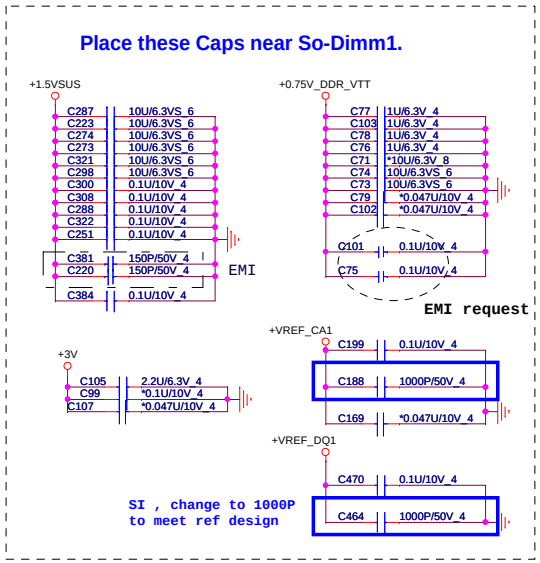




H5.2mm



12,40 +0.75V_DDR_VTT
2,3,4,5,12,40,41,44 +1.5VSUS
2,4,6,8,9,10,11,12,14,18,23,24,25,26,27,28,29,30,31,32,33,41,42,44 +3V

PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-1	1A

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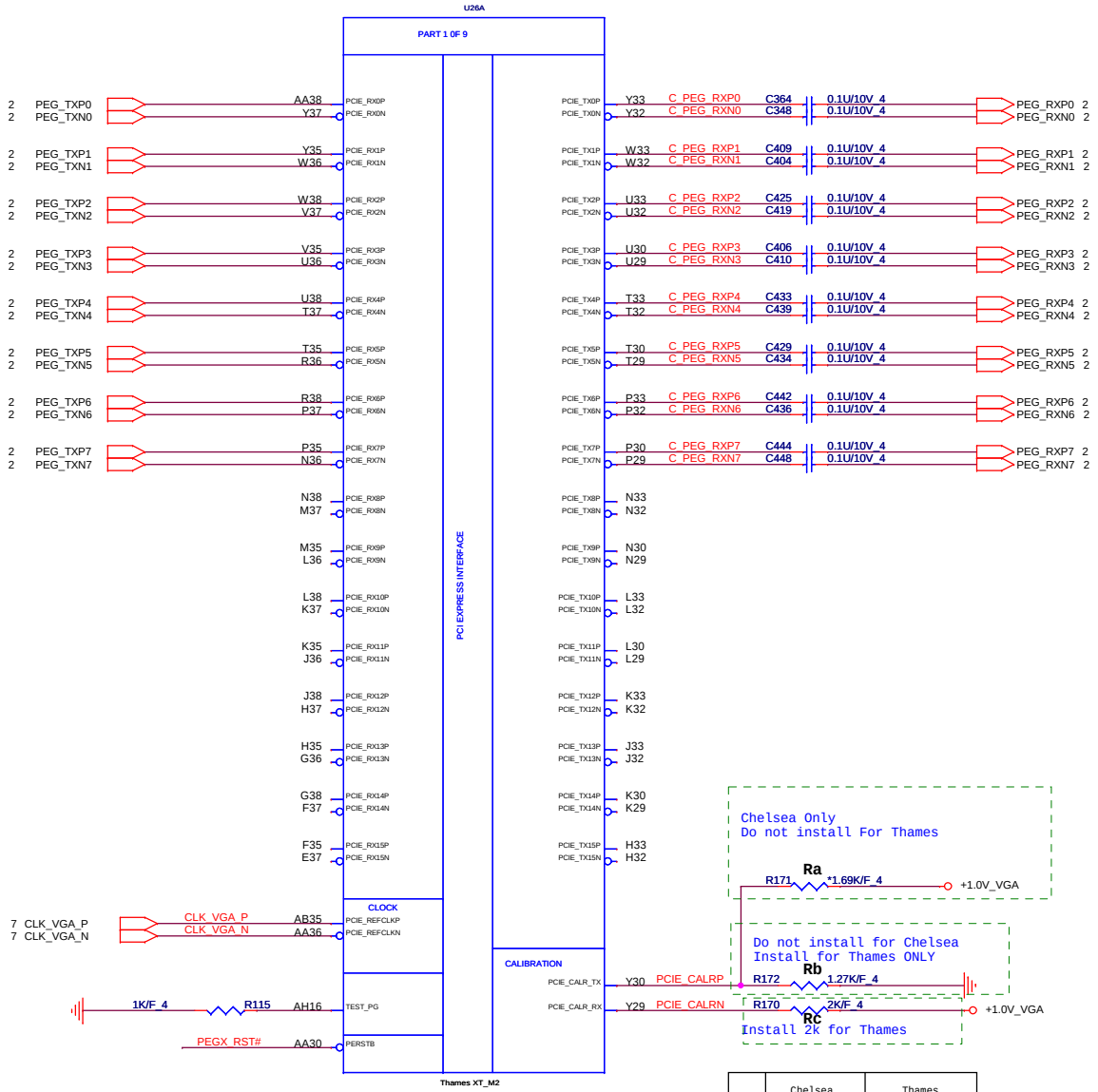
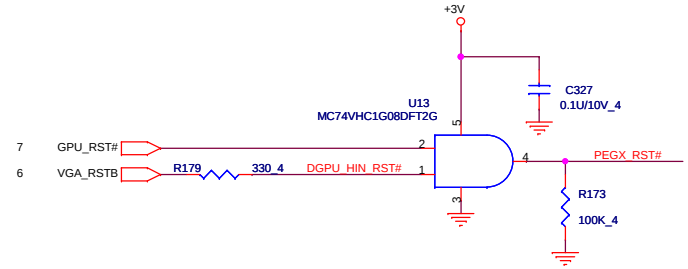


	Chelsea	Thames
Ra	1.69K	n/a
Rb	n/a	1.27K
Rc	1K	2K



16,18,19,44 +1.0V_VGA +1.0V_VGA
15,16,18,19,43 +1.8V_VGA +1.8V_VGA

PROJECT : R53
Quanta Computer Inc.

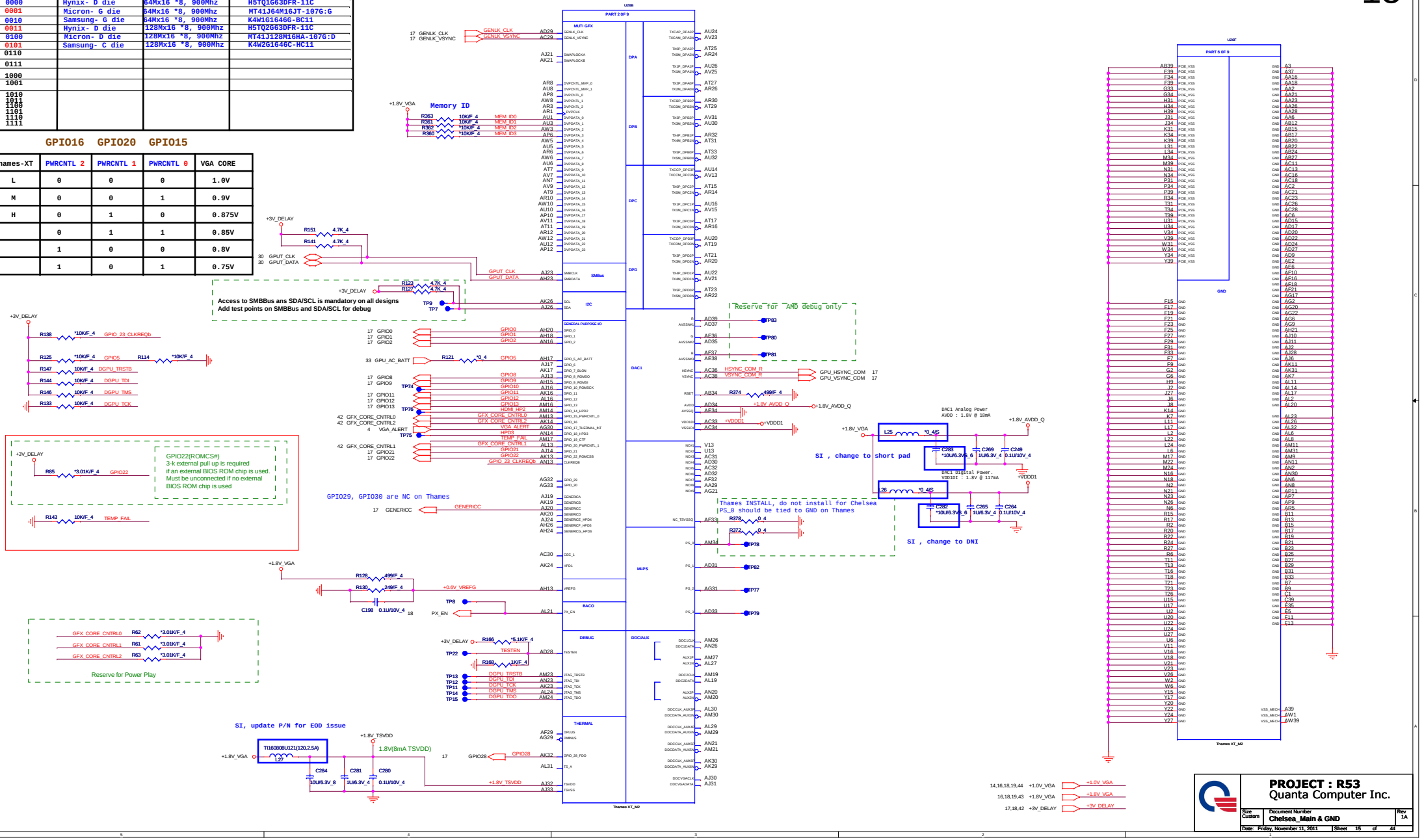
Size	Document Number	Rev
Custom	Chelsea_PCIE_Interface	1A

Date: Monday, November 14, 2011 Sheet 14 of 44

MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Hynix- D die	64Mx16 *8, 900Mhz	H5TQ1G63DFR-11C
0001	Micron- G die	64Mx16 *8, 900Mhz	MT41J64M16JT-107G:G
0010	Samsung- G die	64Mx16 *8, 900Mhz	K4W1G1646G-BC11
0011	Hynix- D die	128Mx16 *8, 900Mhz	H5TQ2G63DFR-11C
0100	Micron- D die	128Mx16 *8, 900Mhz	MT41J128M16HA-107G:D
0101	Samsung- C die	128Mx16 *8, 900Mhz	K4W2G1646C-HC11
0110			
0111			
1000			
1001			
1010			
1011			
1100			
1101			
1110			
1111			

GPIO16 GPIO20 GPIO15

Thames-XT	PWRCNTL 2	PWRCNTL 1	PWRCNTL 0	VGA CORE
L	0	0	0	1.0V
M	0	0	1	0.9V
H	0	1	0	0.875V
	0	1	1	0.85V
	1	0	0	0.8V
	1	0	1	0.75V

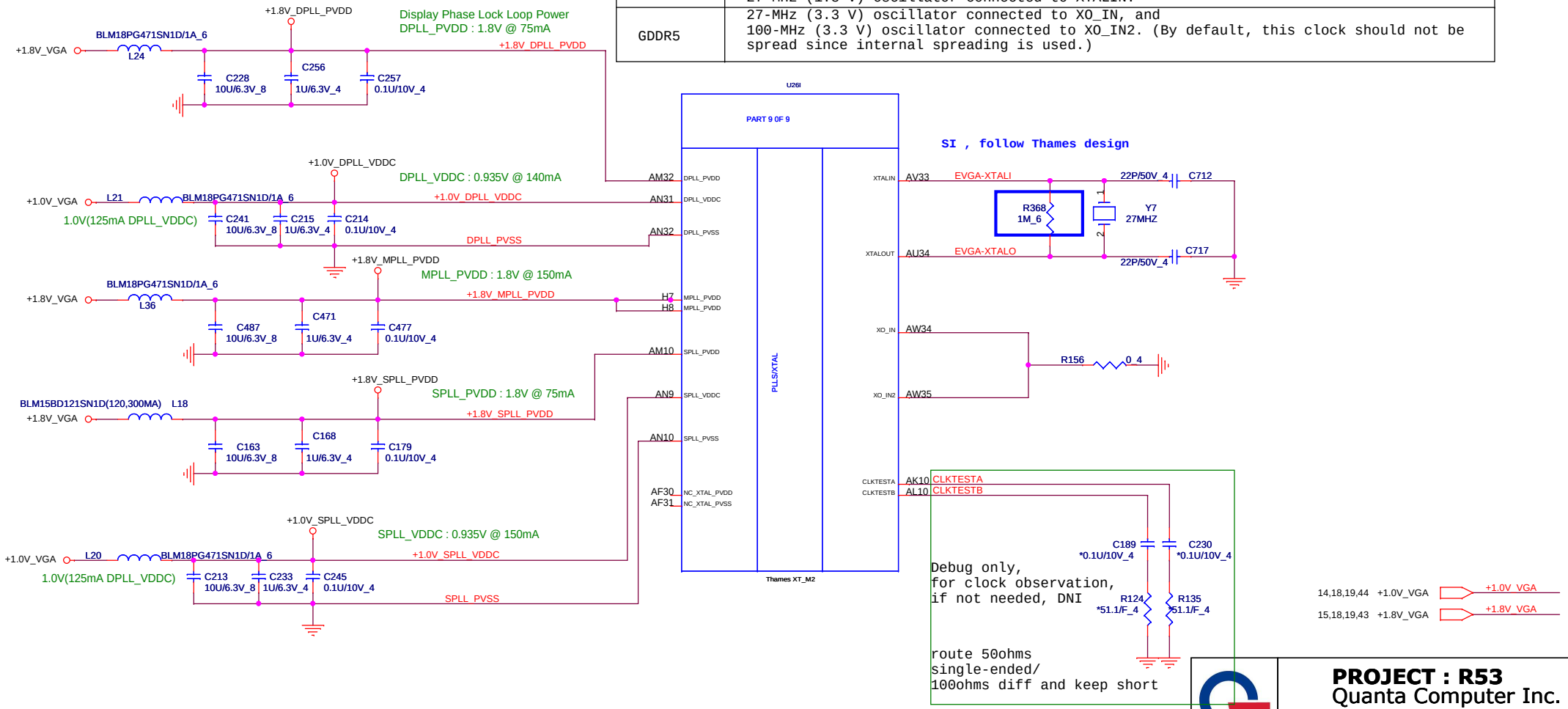


PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Chelsea_Main & GND	1A

Date: Friday, November 11, 2011 Sheet 15 of 44

Memory Type	
DDR3	27-MHz (± 30 ppm) crystal connected to XTALIN/XTALOUT, or 27-MHz (1.8 V) oscillator connected to XTALIN.
GDDR5	27-MHz (3.3 V) oscillator connected to XO_IN, and 100-MHz (3.3 V) oscillator connected to XO_IN2. (By default, this clock should not be spread since internal spreading is used.)



PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Chelsea_XTAL	1A

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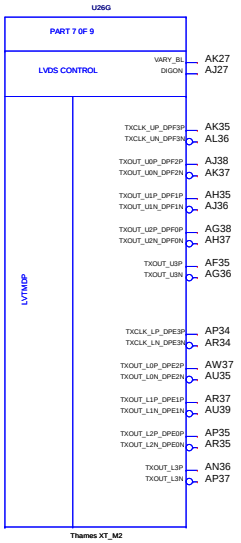
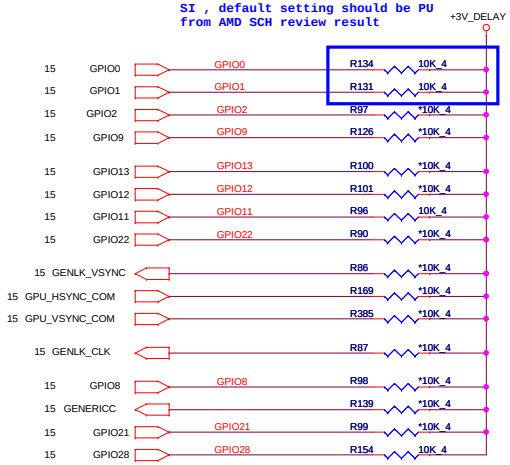


CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET				
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIE Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIE Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
			NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOS ARE USEED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET	
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

SI , default setting should be PU from AMD SCH review result

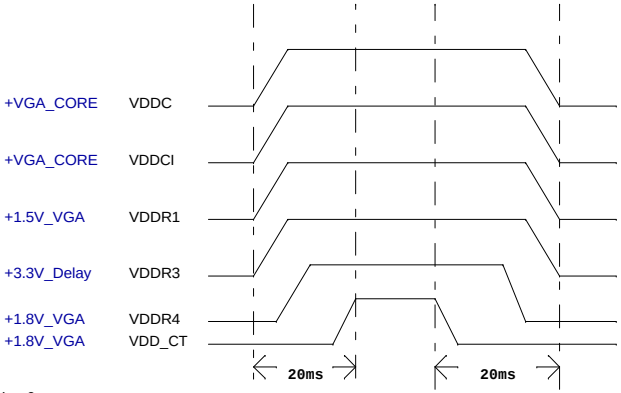


Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

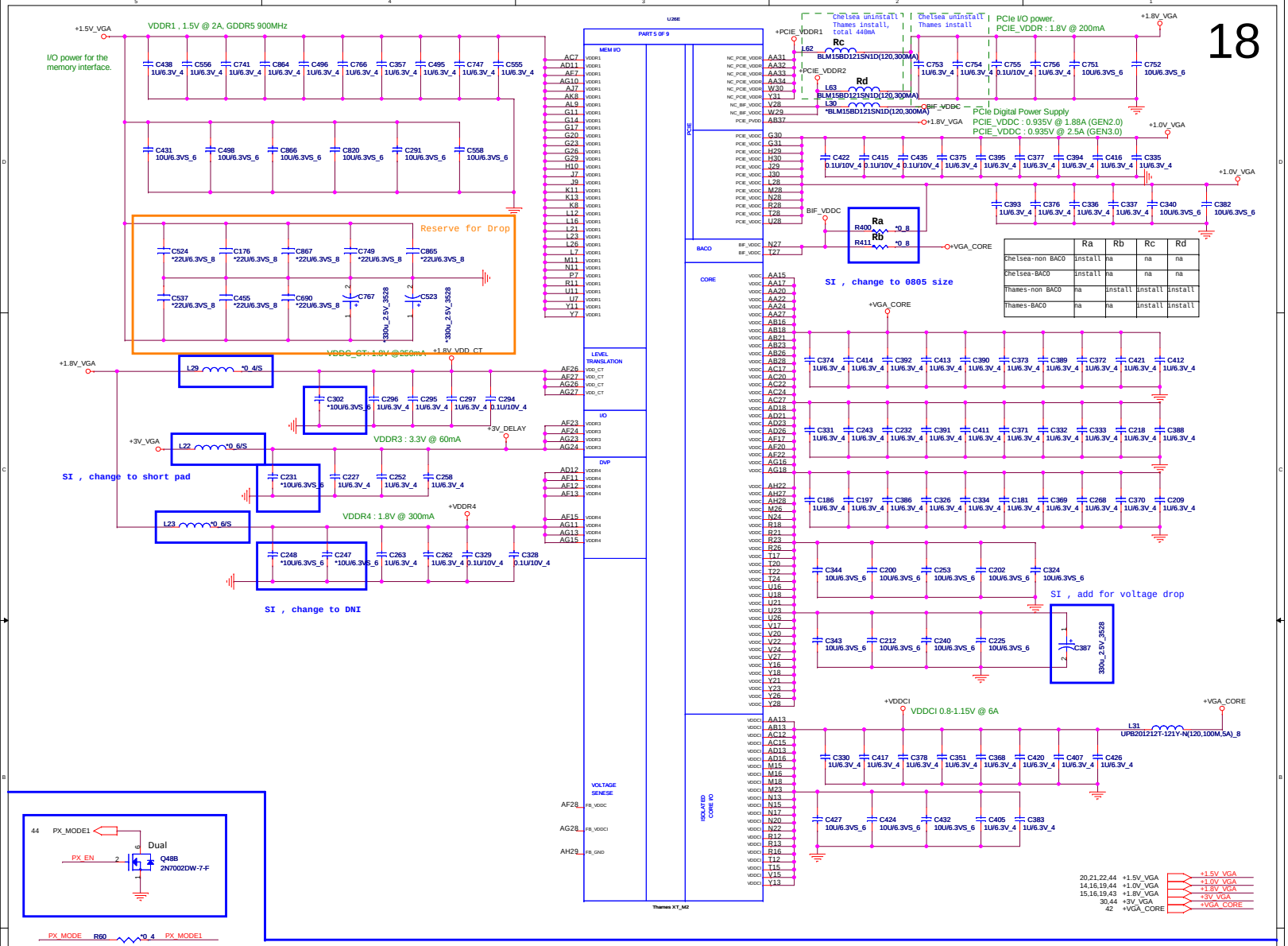
Power Up/Down Sequence



PROJECT : R53
Quanta Computer Inc.

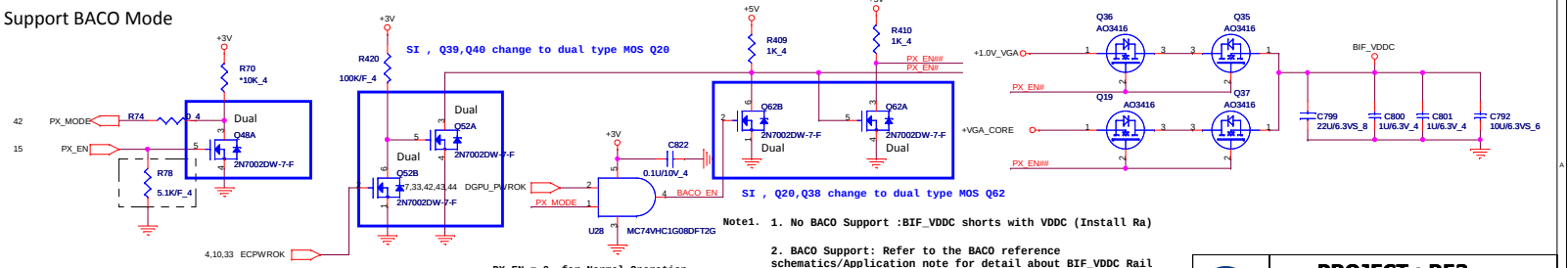
Size	Document Number	Rev
Custom	Chelsea_LVDS / STRAP	1A

Date: Friday, November 11, 2011 Sheet 17 of 44



	Ra	Rb	Rc	Rd
Chelsea-non BACO	install	na	na	na
Chelsea-BACO	install	na	na	na
Thames-non BACO	na	install	install	install
Thames-BACO	na	na	install	install

Support BACO Mode



Note1. 1. No BACO Support :BIF_VDDC shorts with VDDC (Install Ra)

2. BACO Support: Refer to the BACO reference schematics/Application note for detail about BIF_VDDC Rail if BACO is Supported (Uninstall Ra)

PX_EN = 0, for Normal Operation
PX_EN = 1, for BACO MODE

PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Chelsea_Power & BACO	1A

Date: Monday, November 14, 2011 | Sheet 18 of 44

For Thames a dedicated BEAD is required
for each DPAB_VDD18, DPCD_VDD18, DPEF_VDD18

For Thames a dedicated BEAD is required
for each DPAB_VDD10, DPCD_VDD10, DPEF_VDD10

DP/TMDS/LVDS Transmitter Power
HDMI mode: 1.8V@237mA per port
DP mode: 1.8V@188mA per port

DP/TMDS/LVDS Transmitter Power
0.935V@222mA per port

U26H

PART 8 0F 9

DP_VDDR

DP_VDDC

DP GND

CALIBRATION

+1.8V_VGA
L59 *0_4/S
DPAB_VDD18
C709 *10U/6.3VS_6
C711 1U/6.3V_4
C714 0.1U/10V_4
AN24 DP_VDDR
AP24 DP_VDDR
AP25 DP_VDDR
AP26 DP_VDDR
AU28 DP_VDDR
AV29 DP_VDDR

+1.8V_VGA
L57 *0_4/S
DPCD_VDD18
C699 *10U/6.3VS_6
C708 1U/6.3V_4
C702 0.1U/10V_4
AP20 DP_VDDR
AP21 DP_VDDR
AP22 DP_VDDR
AP23 DP_VDDR
AU18 DP_VDDR
AV19 DP_VDDR

+1.8V_VGA
L61 *0_4/S
DPEF_VDD18
C732 *10U/6.3VS_6
C728 1U/6.3V_4
C733 0.1U/10V_4
AH34 DP_VDDR
AJ34 DP_VDDR
AF34 DP_VDDR
AG34 DP_VDDR
AM37 DP_VDDR
AL38 DP_VDDR

SI , change to short pad

SI , change to DNI

R150 150/F_4 AW28 DPAB_CALR
R365 150/F_4 AW18 DPCD_CALR
R377 150/F_4 AM39 DPEF_CALR

DP_VDDC AP31
DP_VDDC AP32
DP_VDDC AN33
DP_VDDC AP33
DP_VDDC AP13
DP_VDDC AT13
DP_VDDC AP14
DP_VDDC AP15
DP_VDDC AL33
DP_VDDC AM33
DP_VDDC AK33
DP_VDDC AK34

DP_VSSR AN27
DP_VSSR AP27
DP_VSSR AP28
DP_VSSR AW24
DP_VSSR AW26
DP_VSSR AN29
DP_VSSR AP29
DP_VSSR AP30
DP_VSSR AW30
DP_VSSR AW32
DP_VSSR AN17
DP_VSSR AP16
DP_VSSR AP17
DP_VSSR AW14
DP_VSSR AW16
DP_VSSR AN19
DP_VSSR AP18
DP_VSSR AP19
DP_VSSR AW20
DP_VSSR AW22
DP_VSSR AN34
DP_VSSR AP39
DP_VSSR AR39
DP_VSSR AU37
DP_VSSR AF39
DP_VSSR AH39
DP_VSSR AK39
DP_VSSR AL34
DP_VSSR AV27
DP_VSSR AR28
DP_VSSR AV17
DP_VSSR AR18
DP_VSSR AN38
DP_VSSR AM35

DPAB_VDD10
+1.0V_VGA
*0_4/S L60
C722 0.1U/10V_4
C721 1U/6.3V_4
C720 *10U/6.3VS_6

DPCD_VDD10
+1.0V_VGA
*0_4/S L58
C710 0.1U/10V_4
C706 1U/6.3V_4
C700 *10U/6.3VS_6

SI , change to short pad

DPEF_VDD10
+1.0V_VGA
*0_4/S L28
C279 0.1U/10V_4
C278 1U/6.3V_4
C277 *10U/6.3VS_6

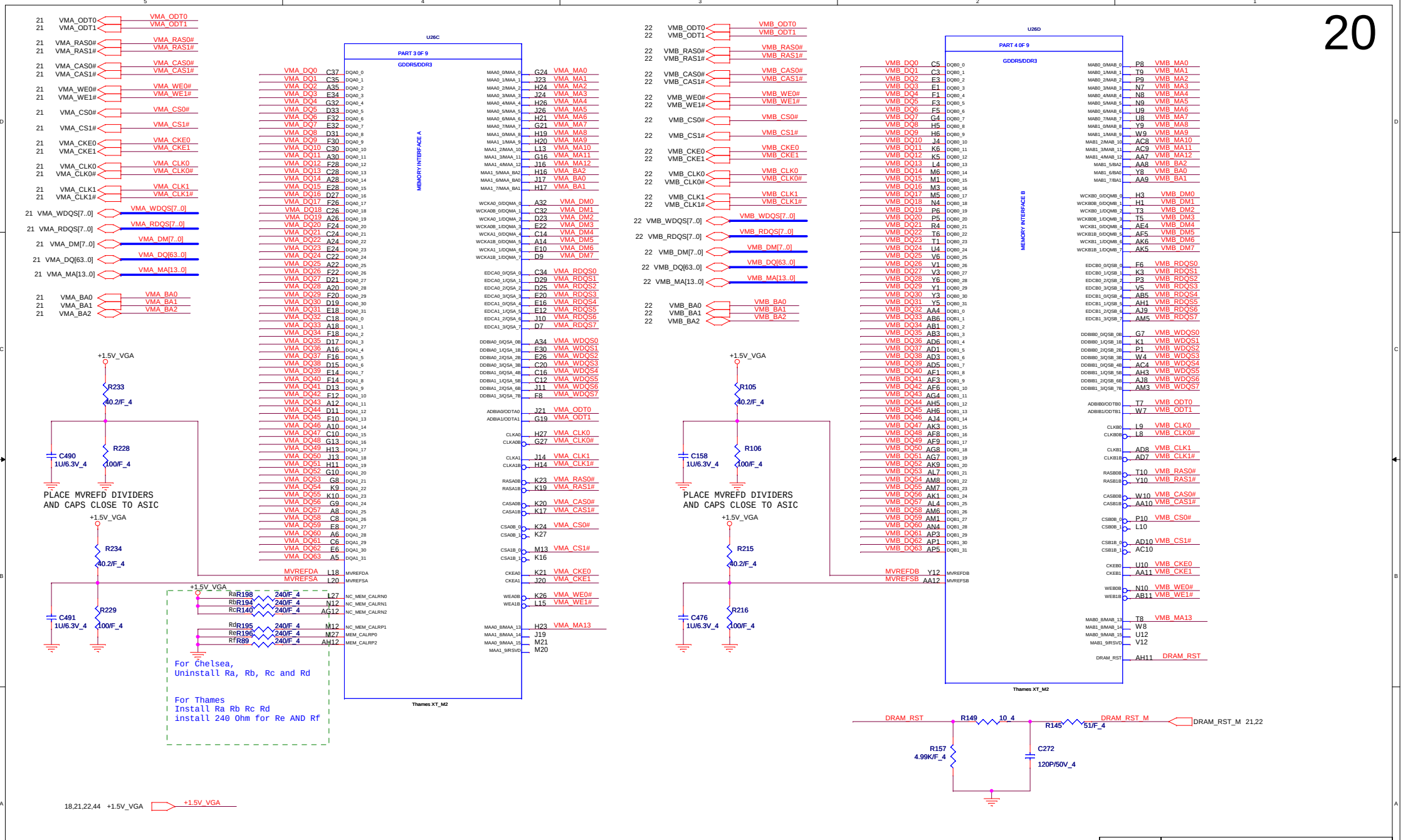
SI , change to DNI

Thames XT_M2

PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Chelsea_DP Powers	1A

Date: Monday, November 14, 2011 Sheet 19 of 44

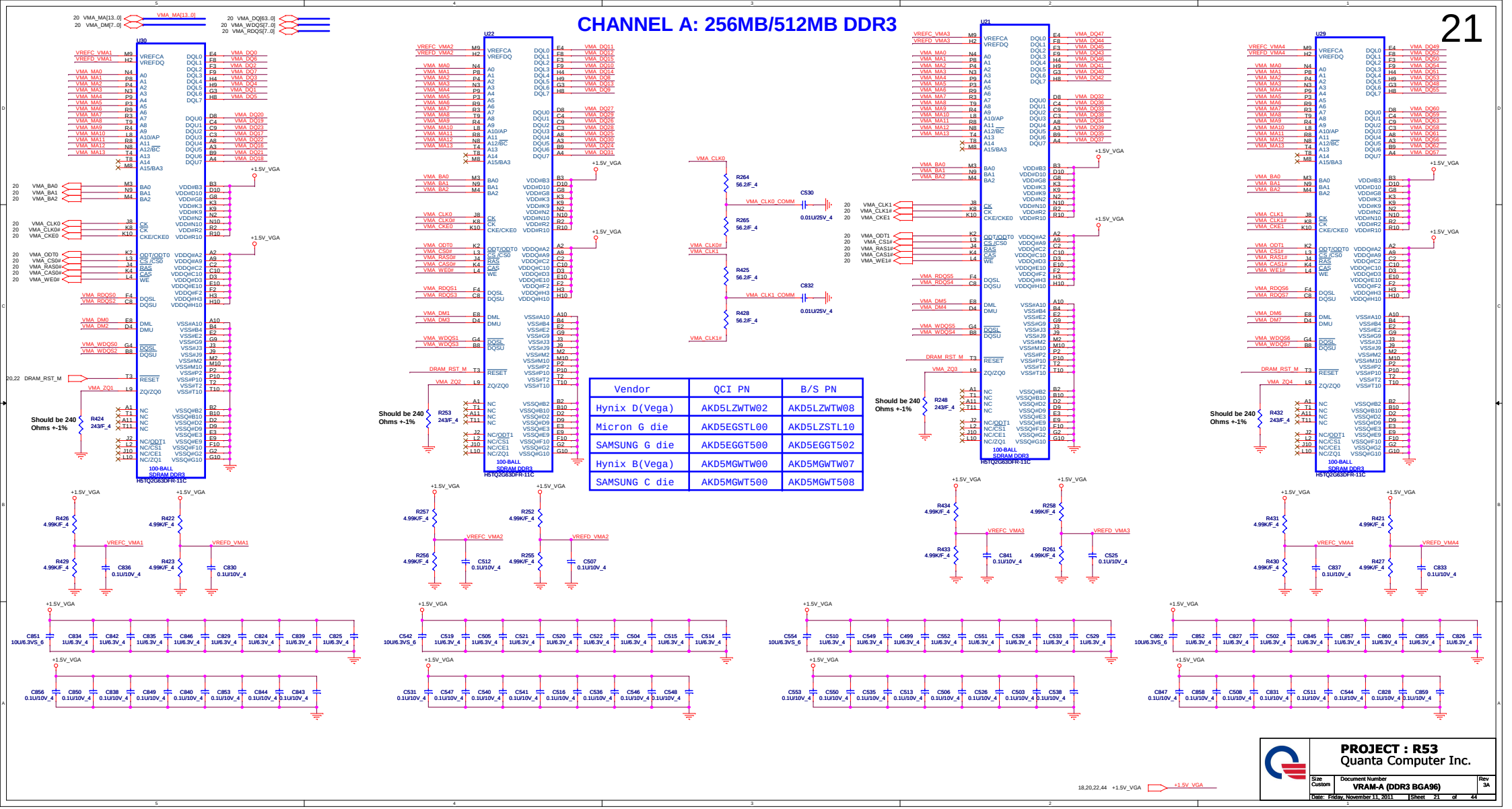


PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Chelsea_MEM_Interface	1A

Date: Friday, November 11, 2011 | Sheet 20 of 44

CHANNEL A: 256MB/512MB DDR3



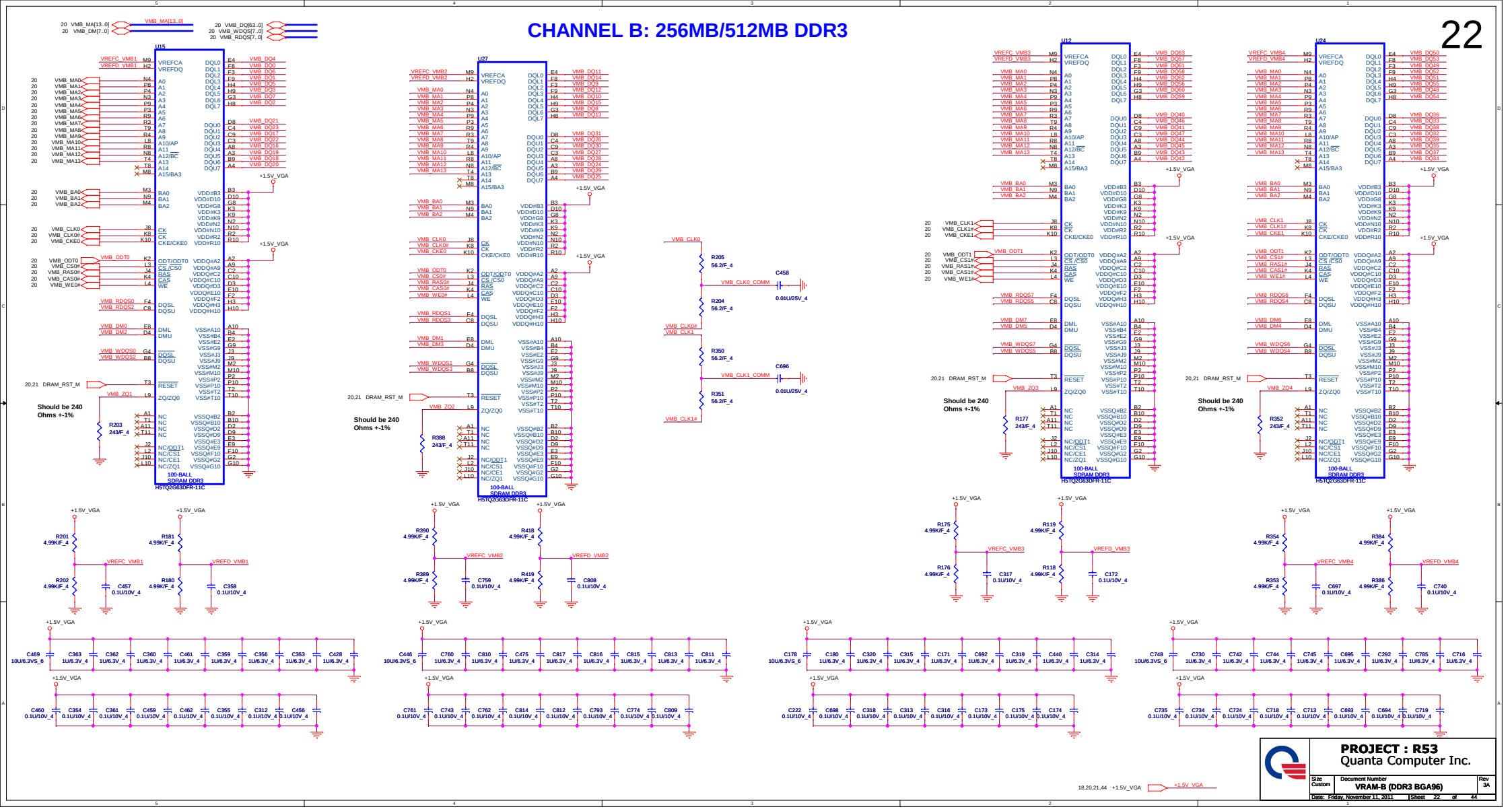
Vendor	QCI PN	B/S PN
Hynix D(Vega)	AKD5LZWTW02	AKD5LZWTW08
Micron G die	AKD5EGSTL00	AKD5LZSTL10
SAMSUNG G die	AKD5EGGT500	AKD5EGGT502
Hynix B(Vega)	AKD5MGWTW00	AKD5MGWTW07
SAMSUNG C die	AKD5MGWT500	AKD5MGWT508

PROJECT : R53
Quanta Computer Inc.

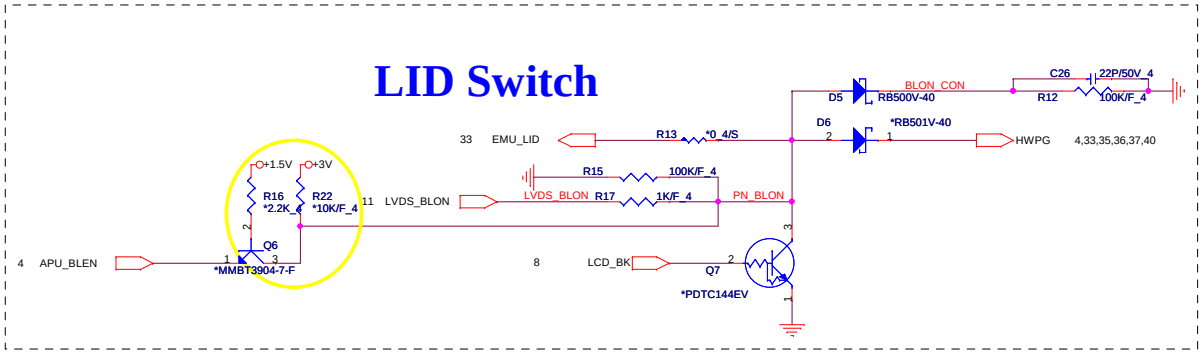
Size	Document Number	Rev
Custom	VRAM-A (DDR3 BGA96)	3A

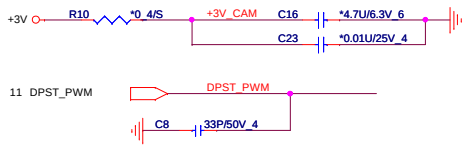
Date: Friday, November 11, 2011 Sheet 21 of 44

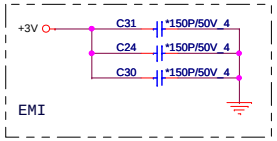
CHANNEL B: 256MB/512MB DDR3

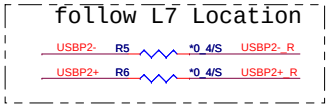


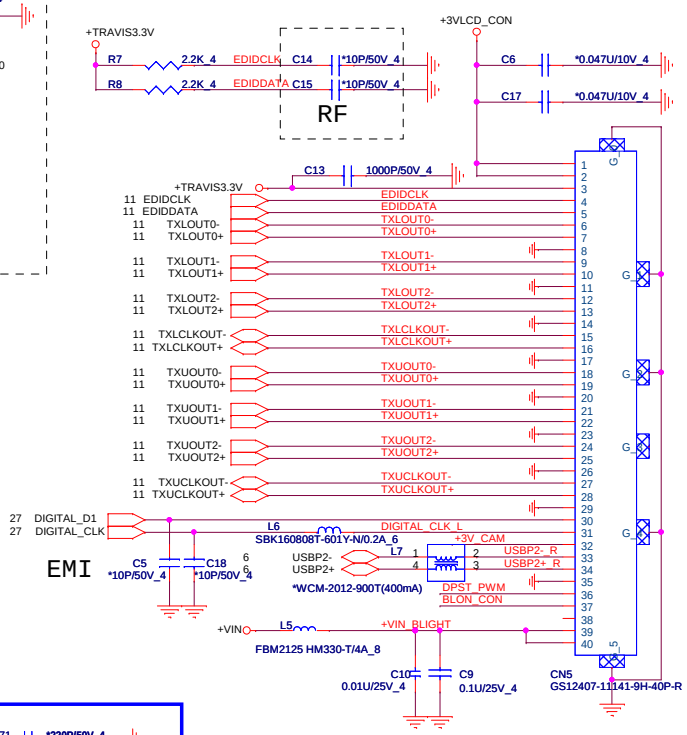
LID Switch

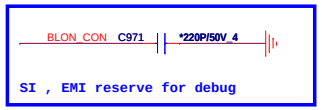


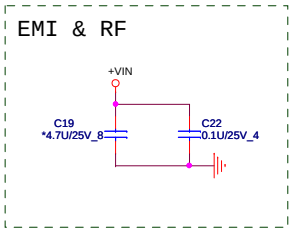


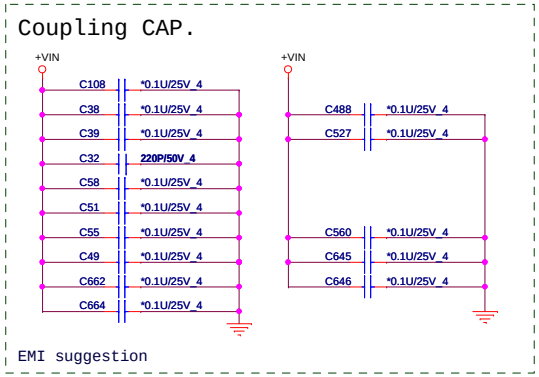


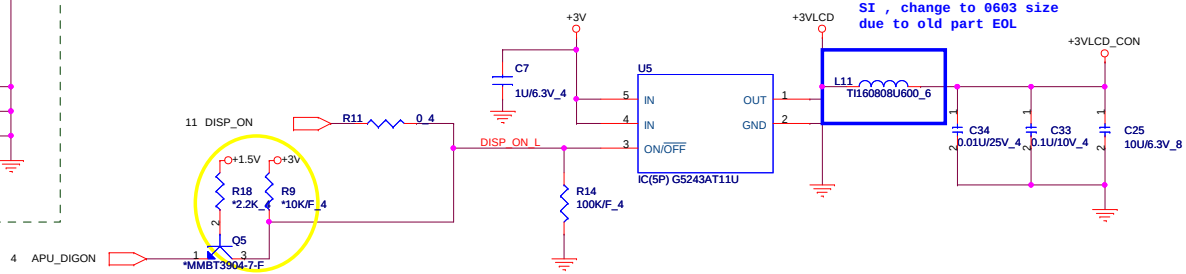












4,7,30,33,34,35 +3VPCU
2,4,6,8,9,10,11,12,13,14,18,24,25,26,27,28,29,30,31,32,33,41,42,44 +3V
9,34,41,44 +12VALW
34,35,36,37,39,40,41,42,44 +VIN

PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID/CAM	1A

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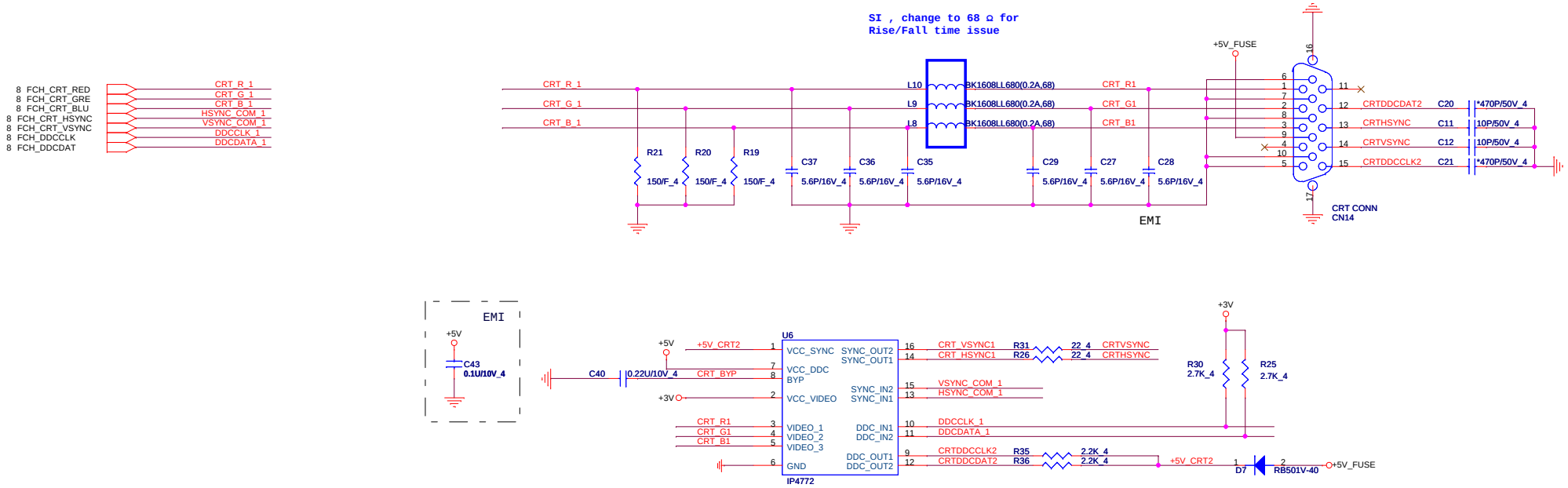
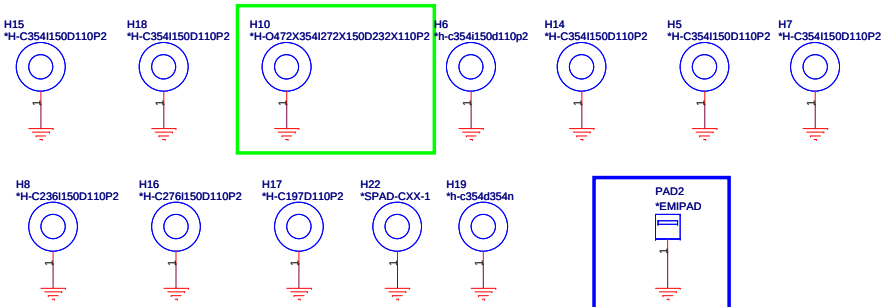
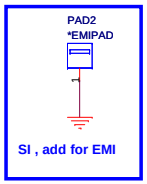
CRT PORT



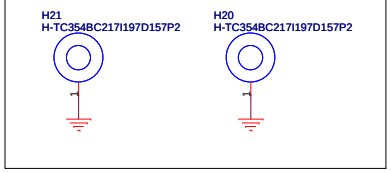
HOLE

SI2 , update footprint

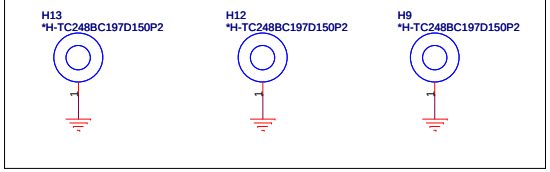




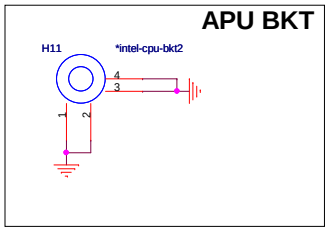
FCH NUT



VGA BKT



APU BKT



PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT,Hole	1A

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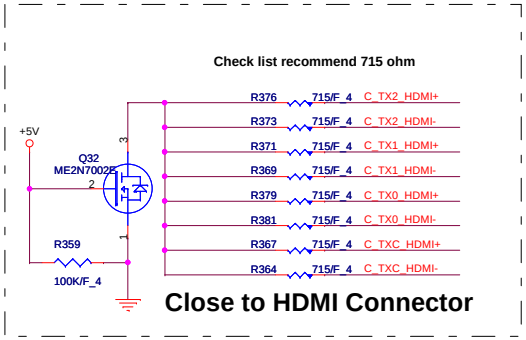
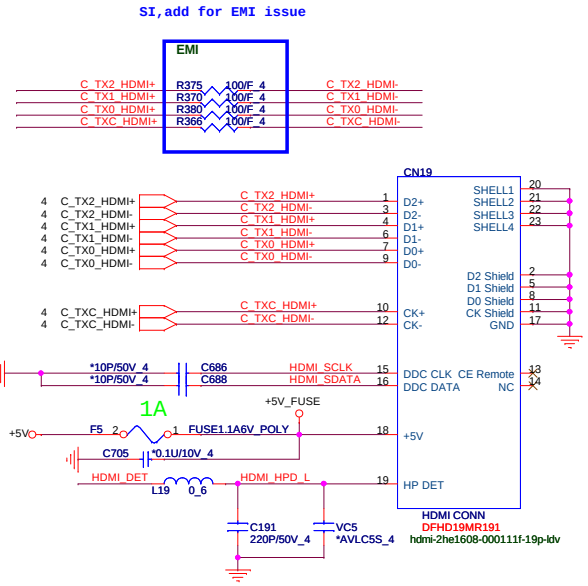
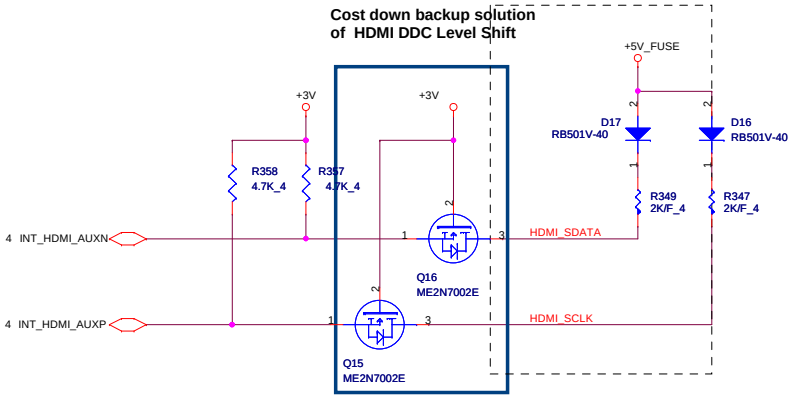
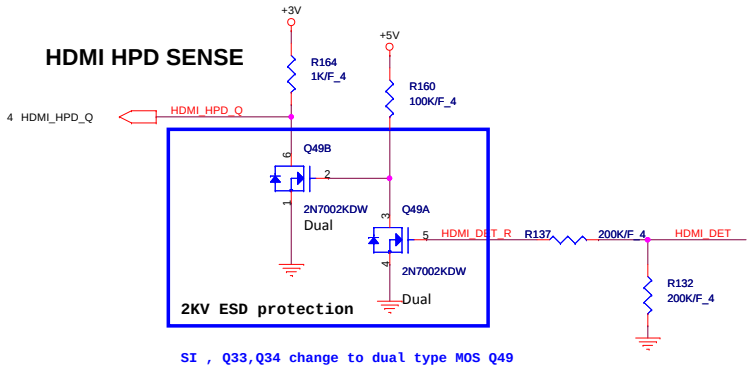
HDMI PORT









PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDMI CONN	1A

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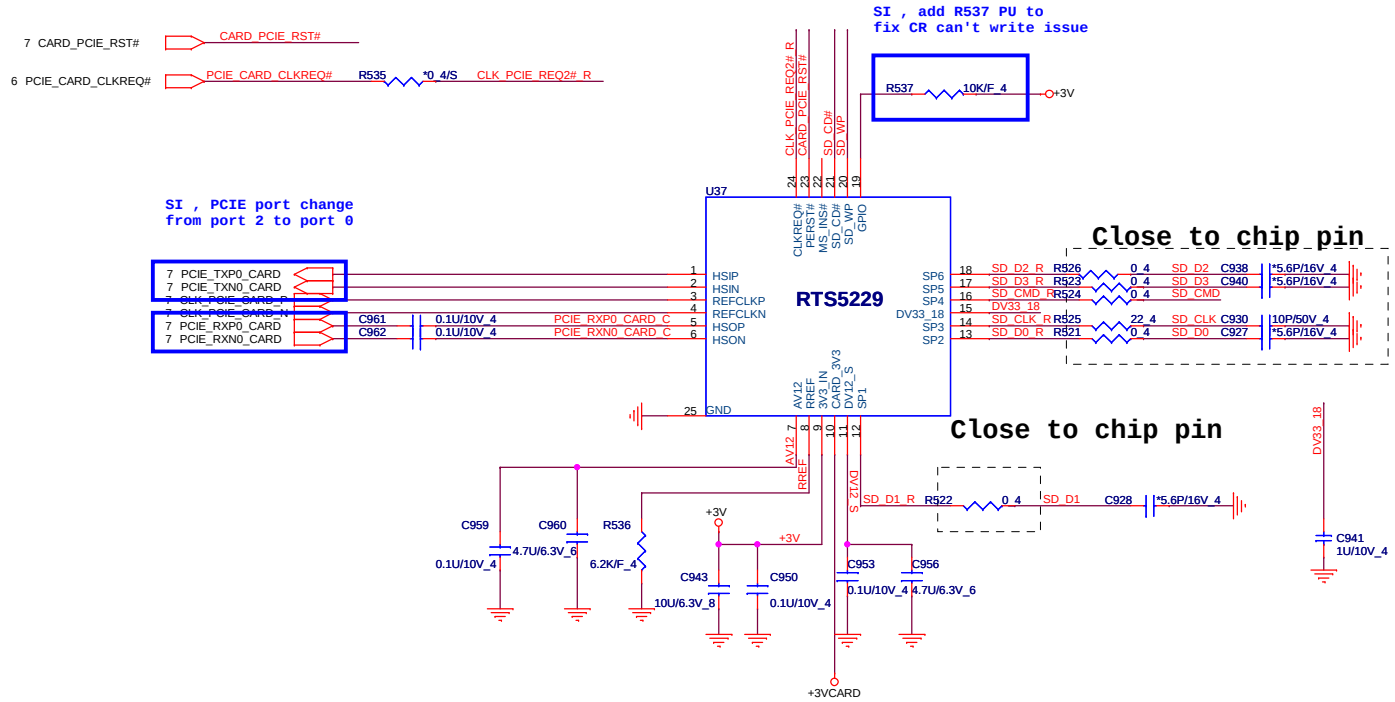

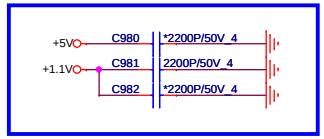

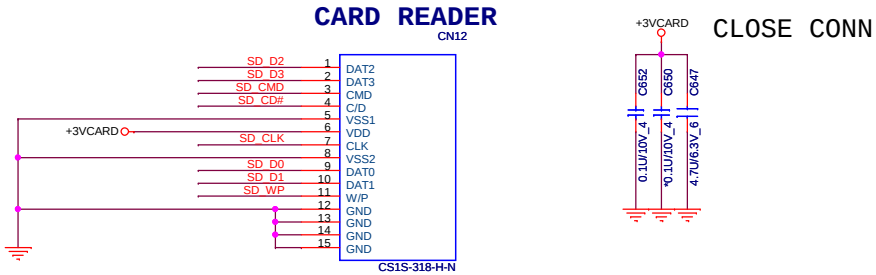

PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTS5219 & CR SOCKET &HOLE	1A

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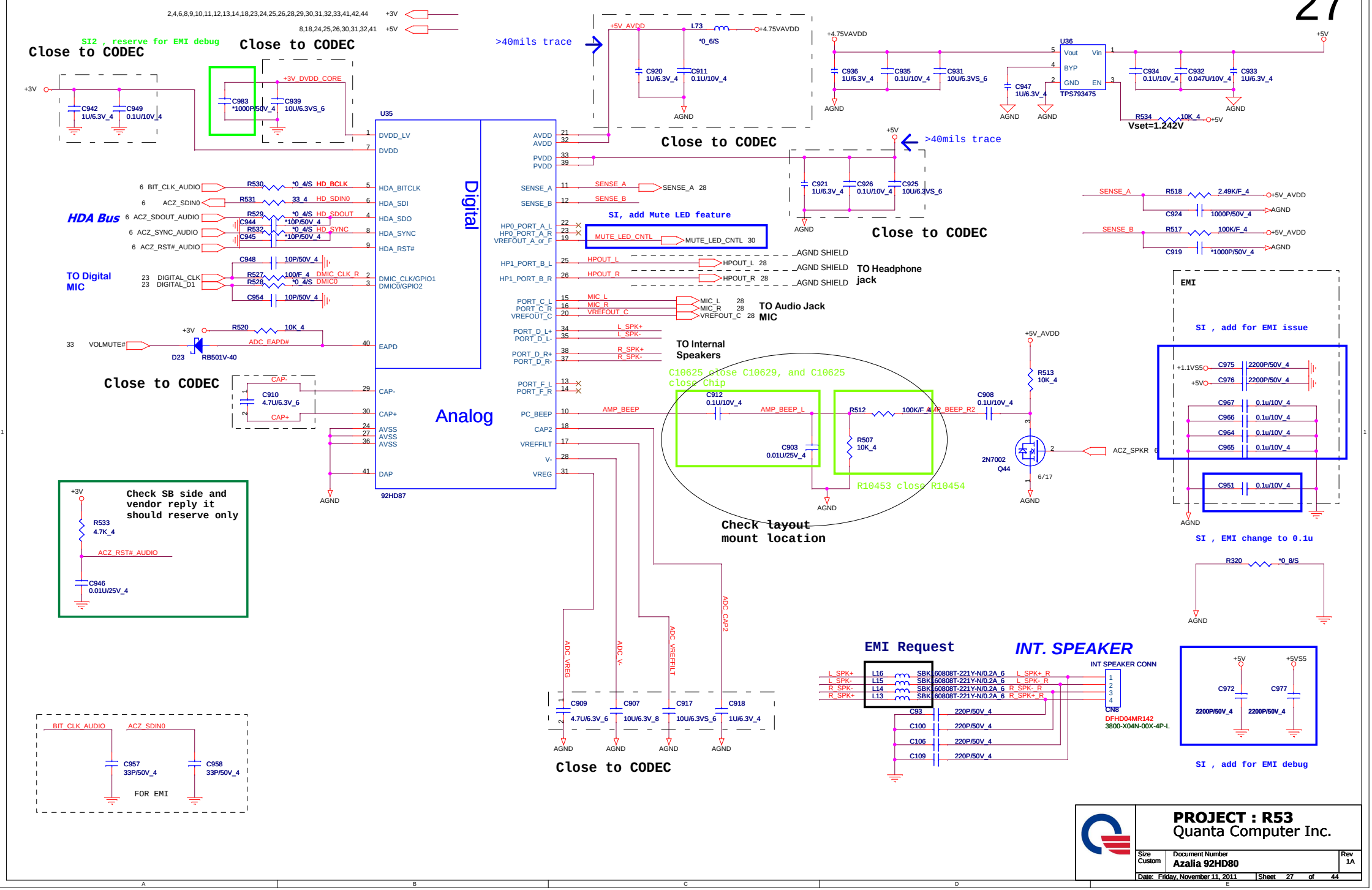

PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Azalia 92HD80	1A

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USB3.0 X 2/USB2.0 COMBO

28

USB 3.0

SI,add choke remove R for EMI issue

EMI 1A

C823 1000P/50V_4

CN21 USB3.0 CONN

USB30_TX1- C486 *ADUC10S020R5

USB30_TX1+ C474 *ADUC10S020R5

USBP11- C489 *ADUC10S020R5

USBP11+ C494 *ADUC10S020R5

USB30_RX1- C500 *ADUC10S020R5

USB30_RX1+ C497 *ADUC10S020R5

R230 *0_4 L35 R236 *0_4 WCM2012-90

R249 0_4 *WCM2012-90 L37 R247 0_4

R221 0_4 *WCM2012-90 L33 R220 0_4

C482 0.1U/10V_4 USB30_TX1-_R

C478 0.1U/10V_4 USB30_TX1+_R

USB 3.0

SI,add choke remove R for EMI issue

EMI 1A

C848 1000P/50V_4

CN22 USB3.0 CONN

USB30_TX2- C543 *ADUC10S020R5

USB30_TX2+ C532 *ADUC10S020R5

USBP12- C545 *ADUC10S020R5

USBP12+ C557 *ADUC10S020R5

USB30_RX2- C561 *ADUC10S020R5

USB30_RX2+ C559 *ADUC10S020R5

R268 *0_4 L41 R269 *0_4 WCM2012-90

R271 0_4 *WCM2012-90 L42 R270 0_4

R267 0_4 *WCM2012-90 L40 R266 0_4

C539 0.1U/10V_4 USB30_TX2-_R

C534 0.1U/10V_4 USB30_TX2+_R

Right SIDE USBX1

9/14 SI for HW

USBP0- R34 *0_4 USBP0-_R

USBP0+ R32 *0_4 USBP0+_R

C59 0.1U/10V_4 +5VS5

L12 WCM2012-90

C48 1000P/50V_4 SATA_LED#

C47 1000P/50V_4 PWRLED_RIGHT

EMI request

CN6 USB BOARD

USBPW_ON# C56 220P/50V_4 EMI request

U32

VIN1 VIN2 EN GND OUT3 OUT2 OUT1 OC

G547N2P81U

C883 1U/6.3V_4

100 mils (Iout=2.5A)

+5V_USBP0

C869 470P/50V_4

C871 0.1U/10V_4

C868 470P/50V_4

C870 0.1U/10V_4

C854 100U/25V

Line out

AGND SHIELD

HPOUT_L HPOUT_R

R310 16/F_4 R302 16/F_4

BLM18BD601SN1D L51 L46

R299 *20K/F_4 R308 *20K/F_4 C602 1000P/50V_4 C636 1000P/50V_4

C619 0.1U/10V_4 VC11 *AVLC5S_4 VC10 *AVLC5S_4 C592 0.1U/10V_4

CN24 HP-JACK-BLACK

Normal Open

SENSE_PHONE

VC9 *AVLC5S_4 AGND

R285 20K/F_4 SENSE_A

SENSE_MIC R273 10K/F_4 SENSE_A

VC6 *AVLC5S_4 AGND

MIC

VREFOUT_C

C564 1U/6.3V_4 R279 3.9K/F_4 R278 3.9K/F_4

MIC_L C578 2.2U/6.3V_6

MIC_R C565 2.2U/6.3V_6

BLM18BD601SN1D L44 L43

C562 220P/50V_4 C571 220P/50V_4

VC7 *AVLC5S_4 VC8 *AVLC5S_4

CN23 HP-JACK-BLACK

Normal Open

COMPONENT CHOICES:
The selection of ferrite beads can have a large effect on THD+N, causing failures versus the WLP requirements.
At this time, IDT has verified three ferrite beads that will meet the WLP performance requirements:
Murata: BLM18BD601SN1
TDK: MMZ1608Y601BTA
Taiyo Yuden: LF BK 1608HM601-T

PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB/BT/Audio JacK	1A

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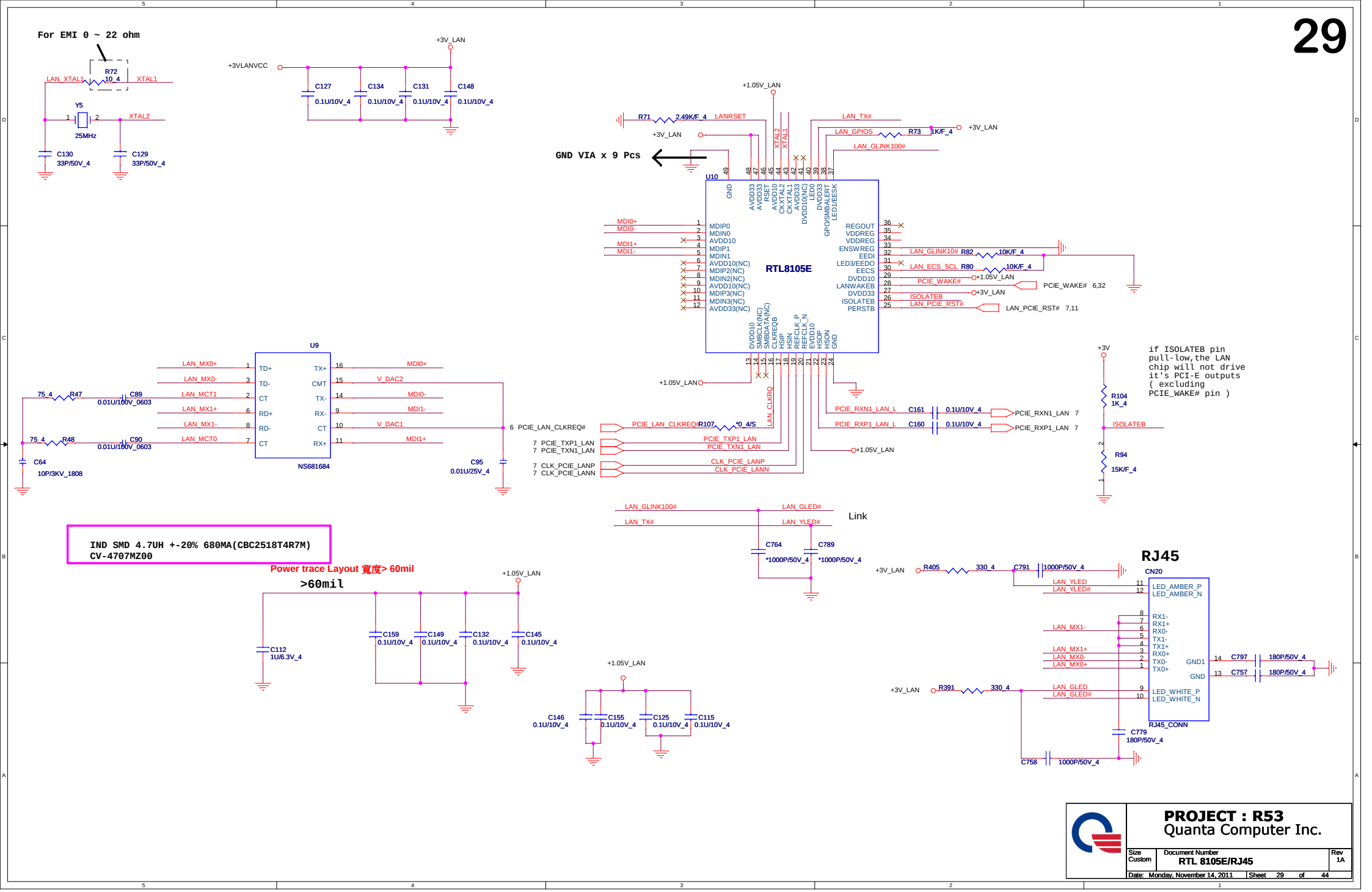

PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTL 8105E/RJ45	1A

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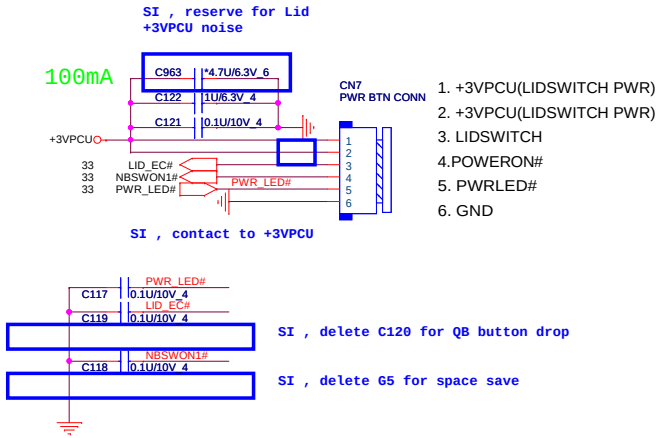
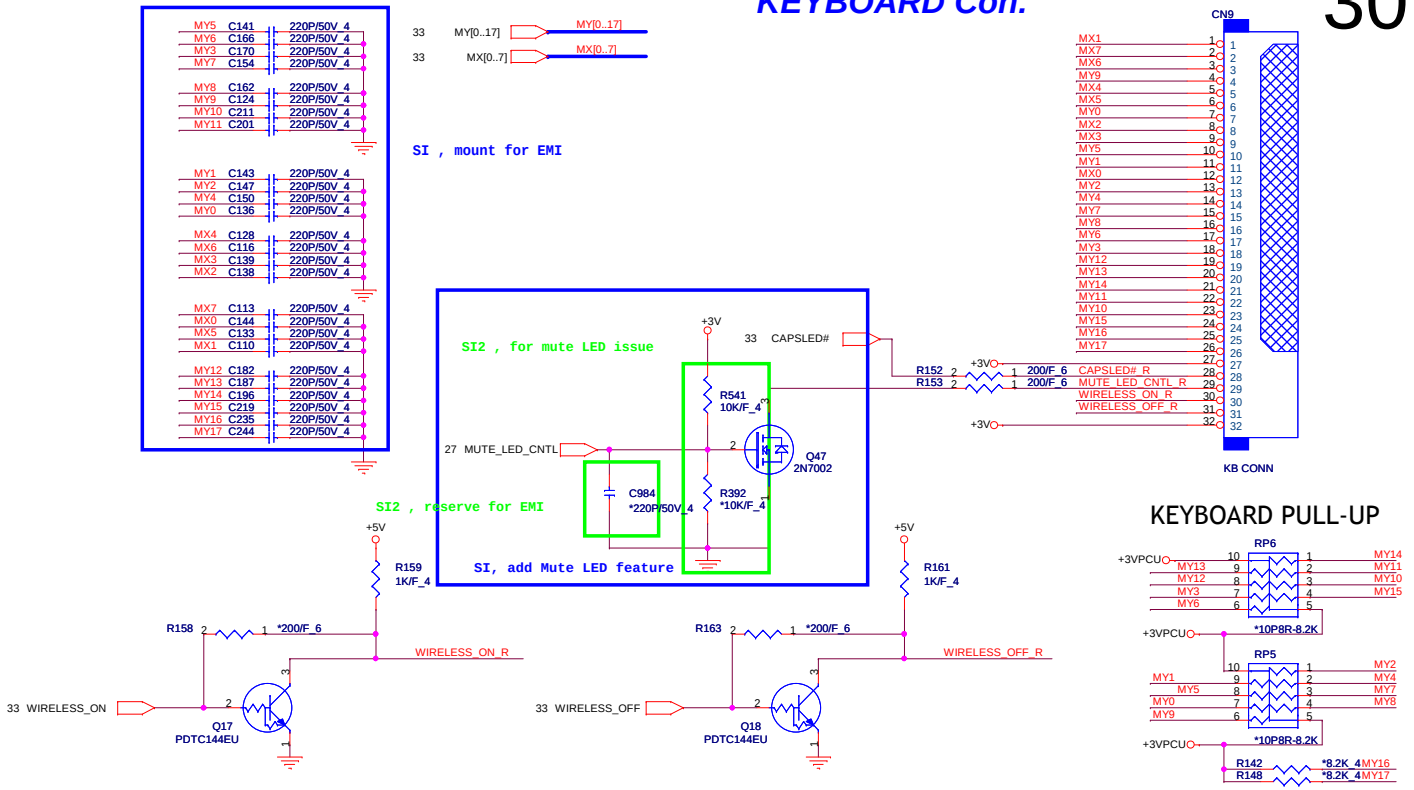
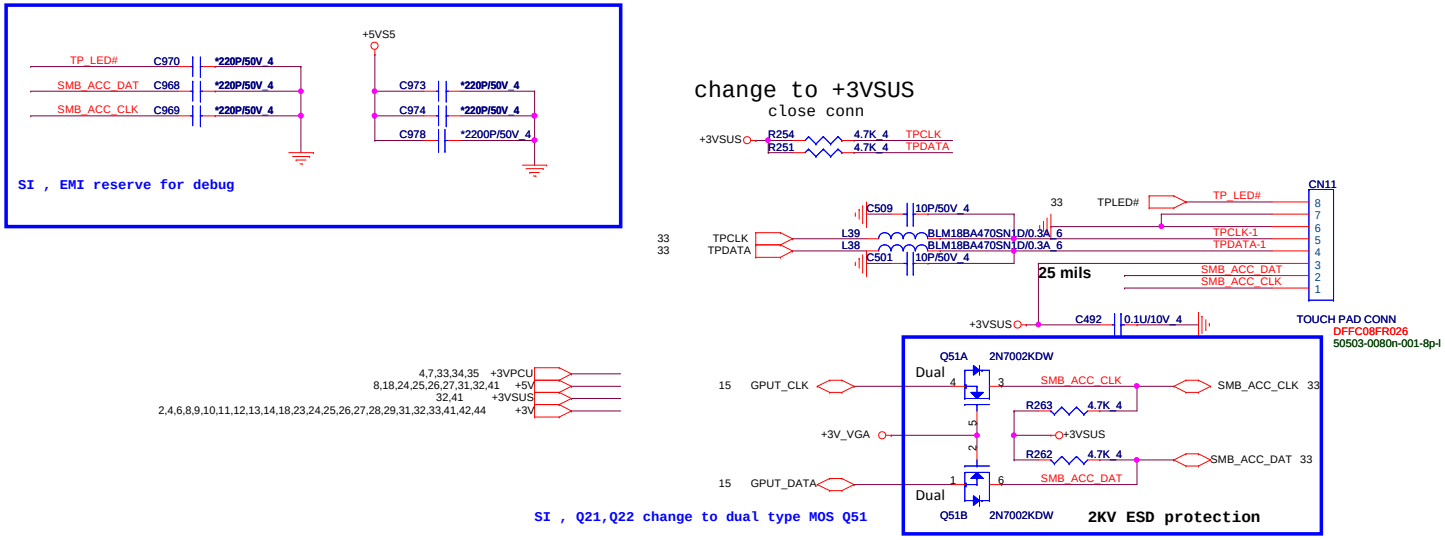
POWER BOTTON CONNECT



KEYBOARD Con.



TOUCH PAD Con.



PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB/SW/TP	1A

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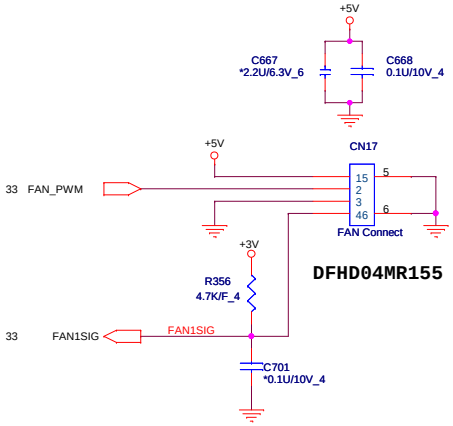
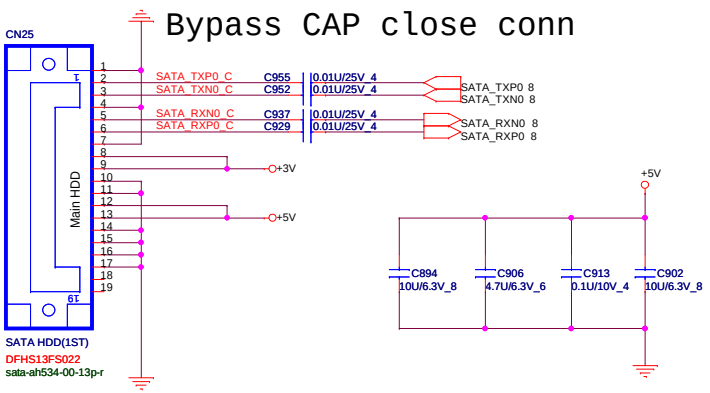
CPU FAN

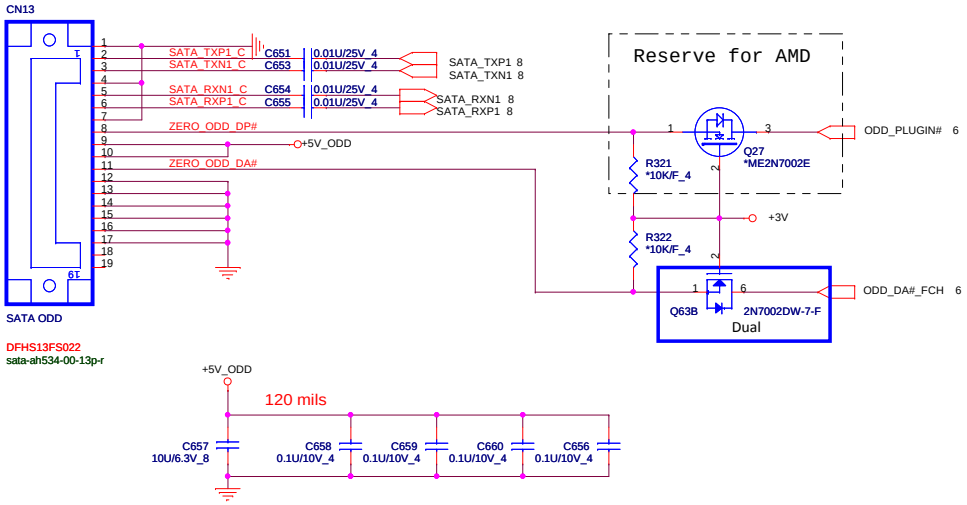


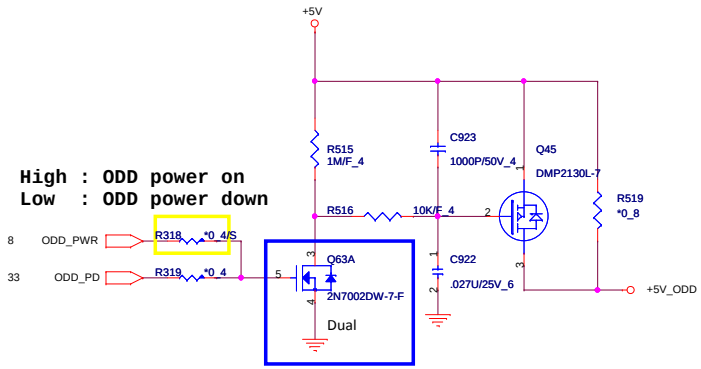
SATA HDD CONNECTOR



SATA ODD CONNECTOR

SATA ODD





SI , Q28,Q43 change to dual type MOS Q63

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDD/ODD/FAN	1A

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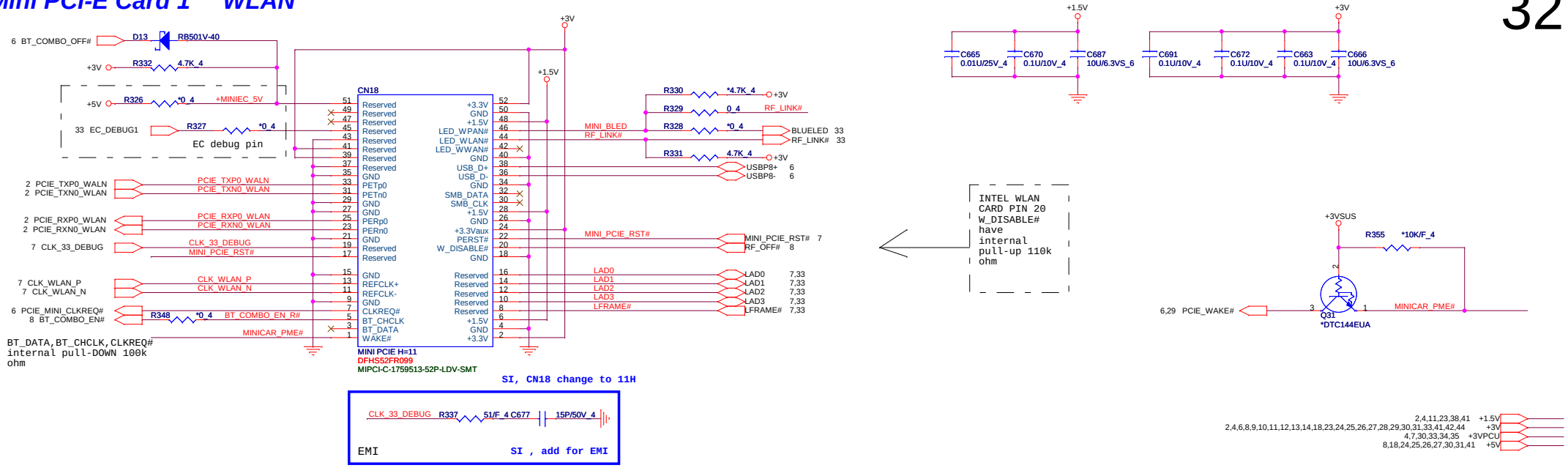
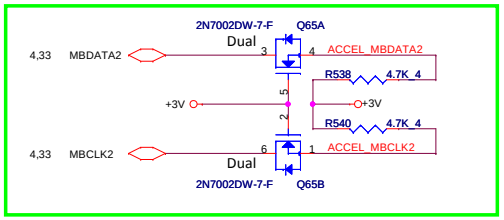
Mini PCI-E Card 1 WLAN

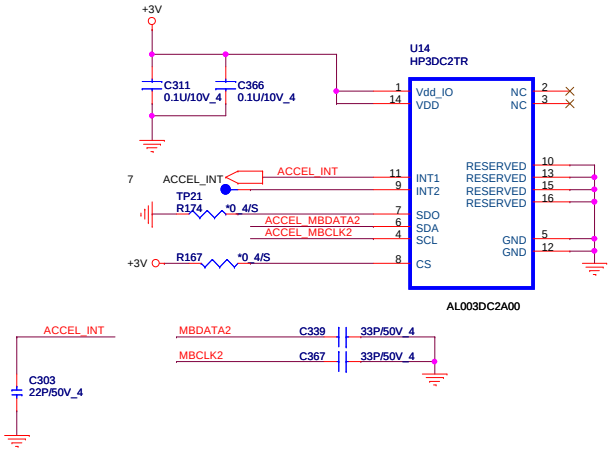


SI, CN18 change to 11H

Accelerometer Sensor



SI2 , add for avoid leakage
from SUS power



PROJECT : R53 Quanta Computer Inc.		
Size Custom	Document Number **MINI PCIE & G-sensor**	Rev 1A
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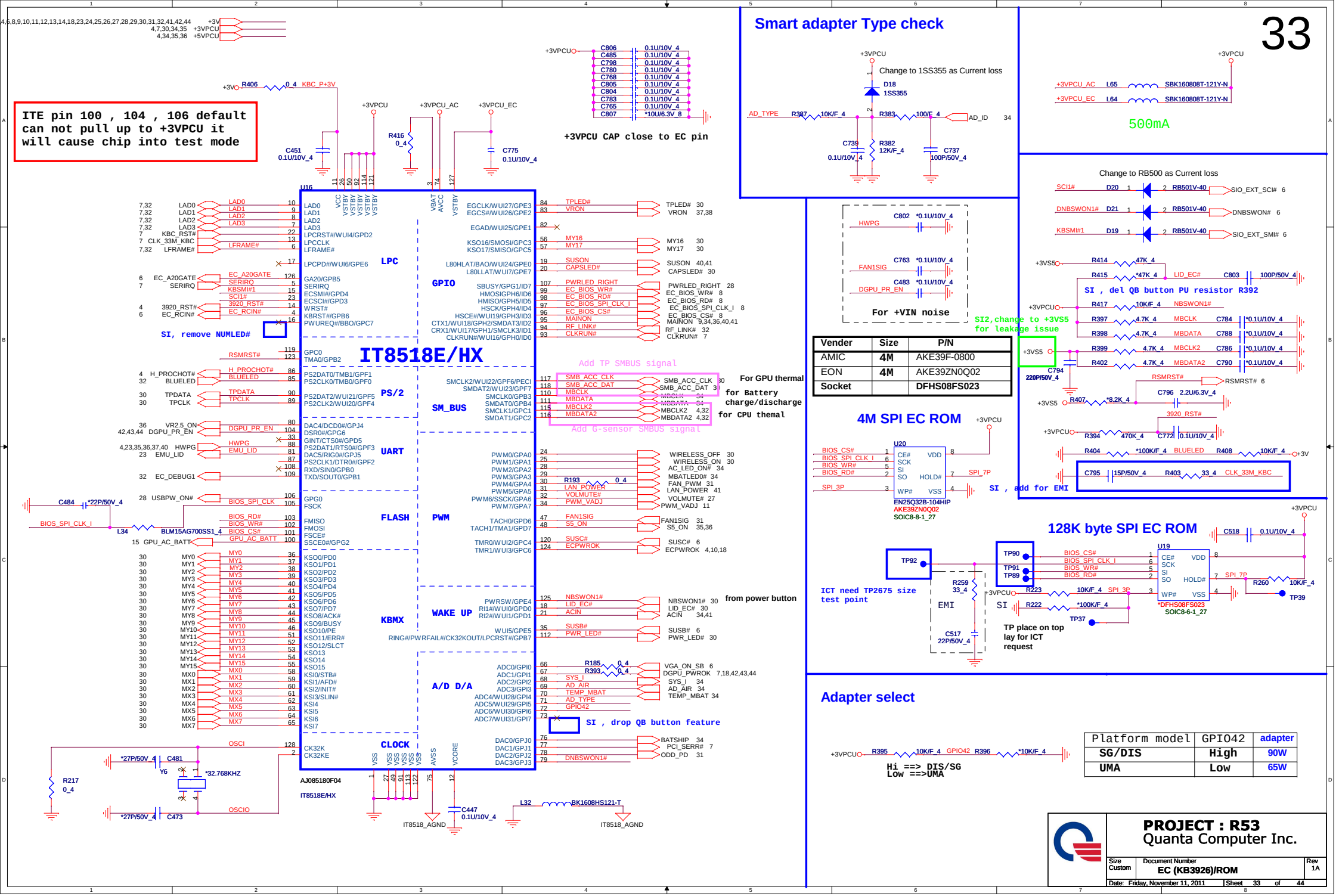

Vender	Size	P/N
AMIC	4M	AKE39F-0800
EON	4M	AKE39ZN0Q02
Socket		DFHS08FS023

Platform model	GPIO42	adapter
SG/DIS	High	90W
UMA	Low	65W

PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	EC (KB3926)/ROM	1A

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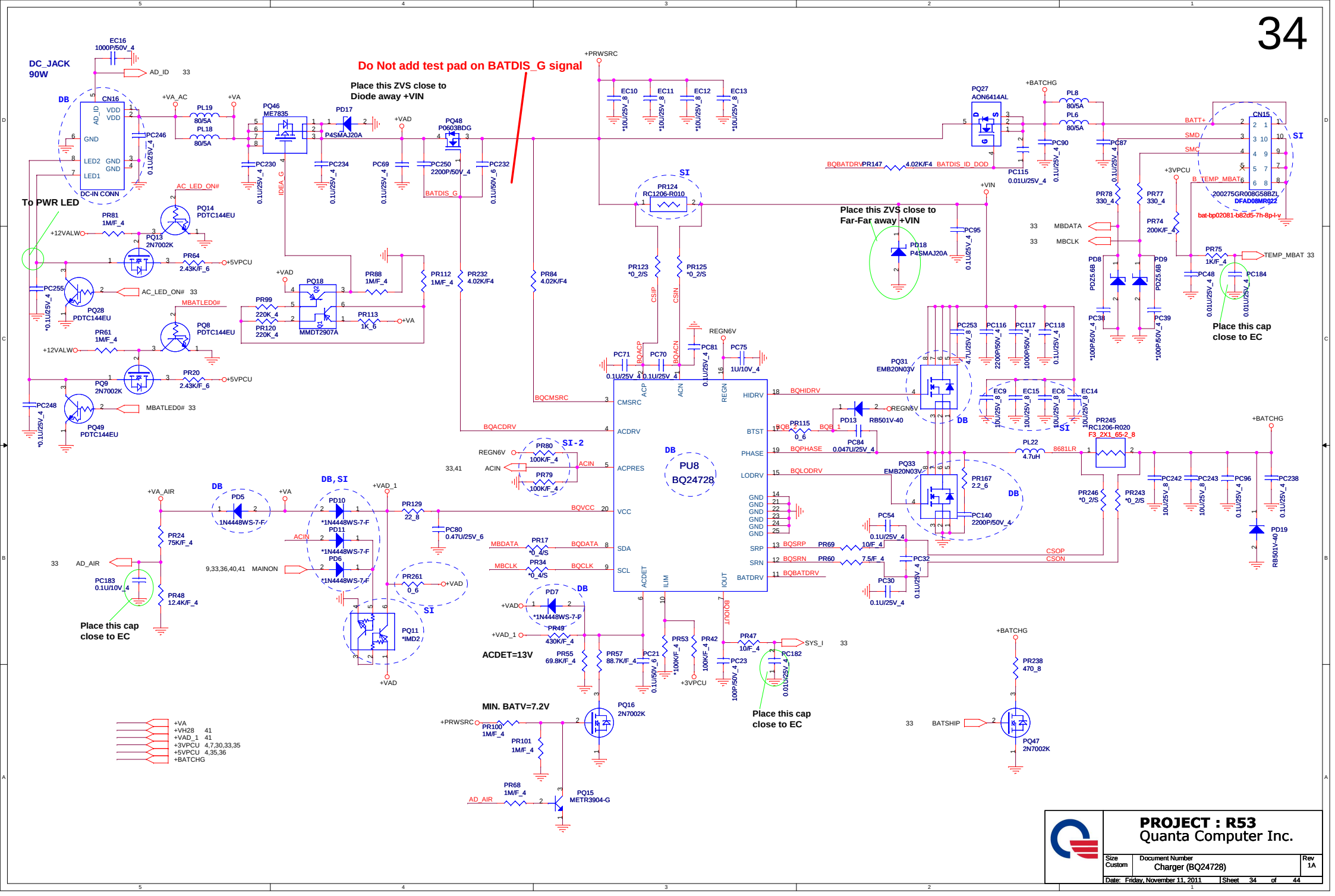
DC_JACK
90W
CN16
DC-IN CONN
To PWR LED
Do Not add test pad on BATDIS_G signal
Place this ZVS close to
Diode away +VIN
Place this ZVS close to
Far-Far away +VIN
Place this cap
close to EC
PU8
BQ24728
ACDET=13V
MIN. BATV=7.2V
CN15
200275GR008G58BZL
DFAD08MR022
bat-bp02081-b82d5-7h-8p-l-v
PROJECT : R53
Quanta Computer Inc.
Size
Custom
Document Number
Charger (BQ24728)
Rev
1A
Date: Friday, November 11, 2011
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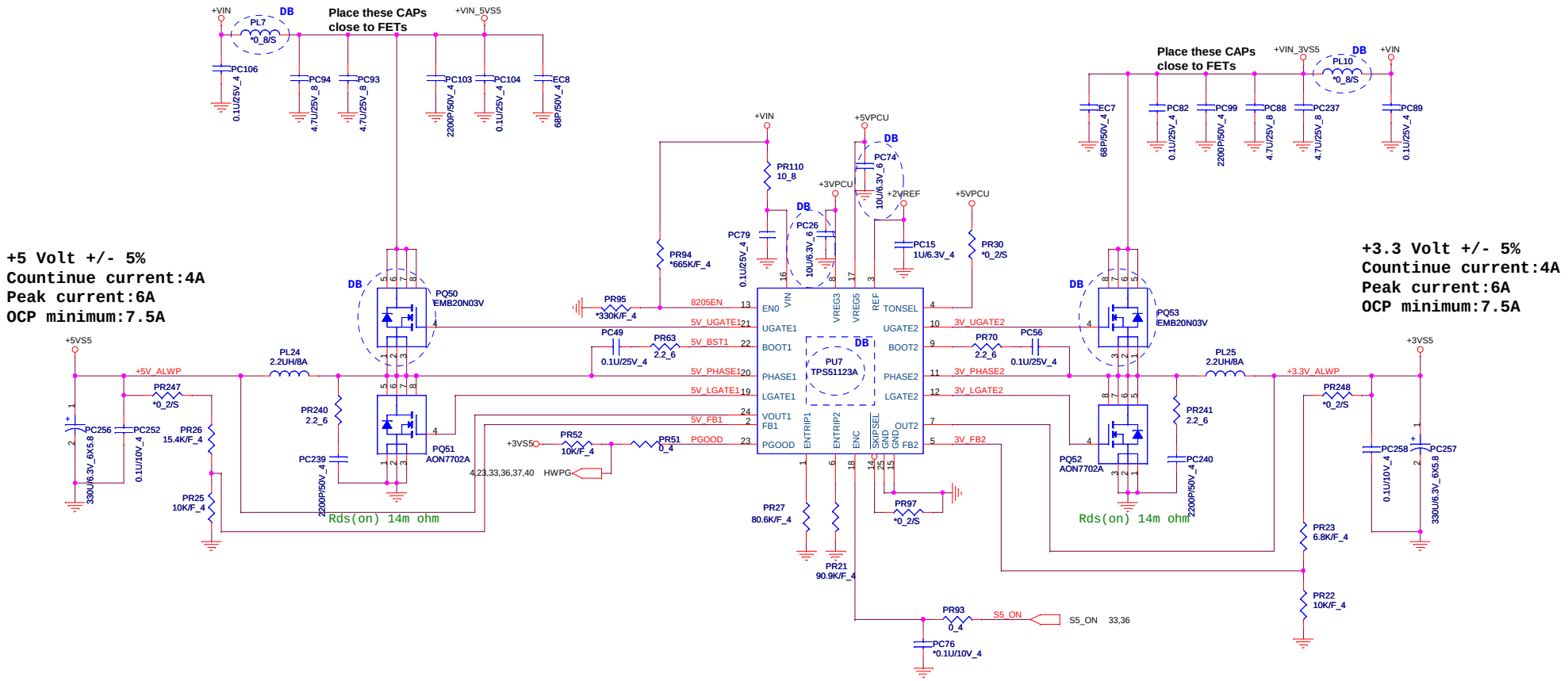
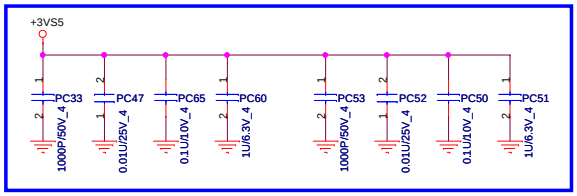


DB for prevent interference



PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	3/5VPCU(TPS51123A)	1A

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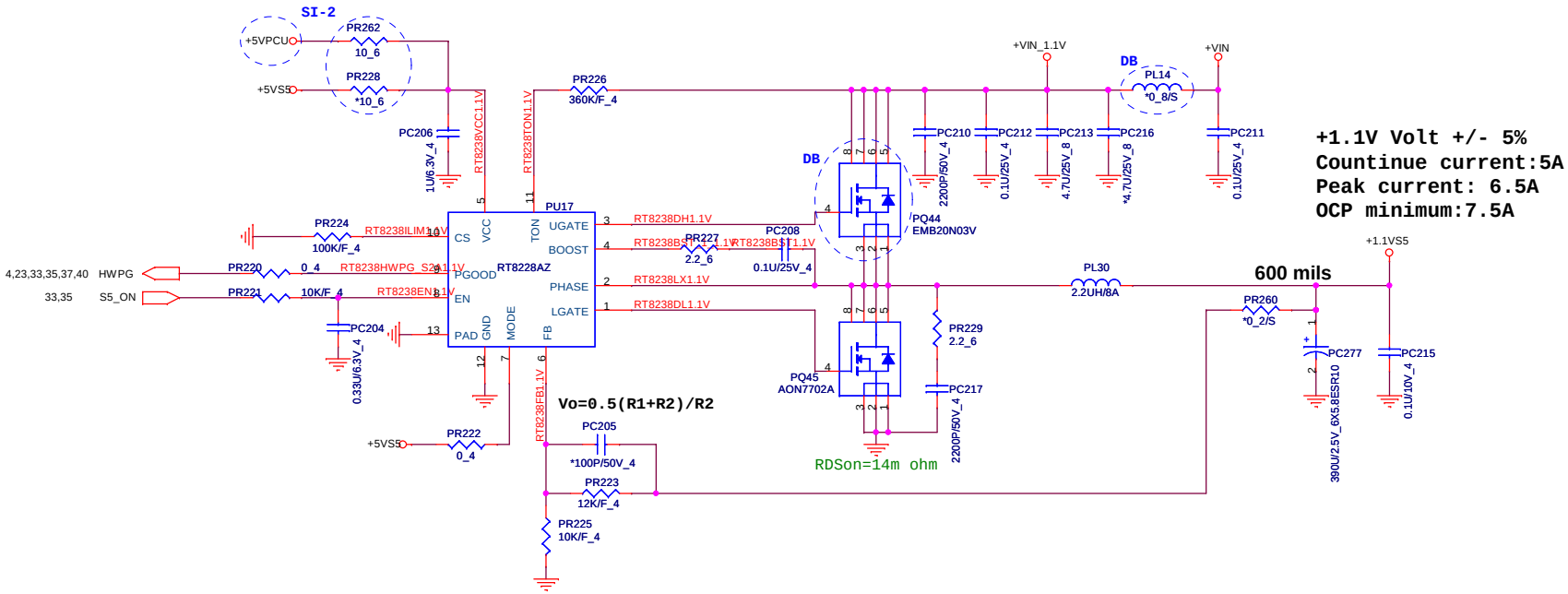
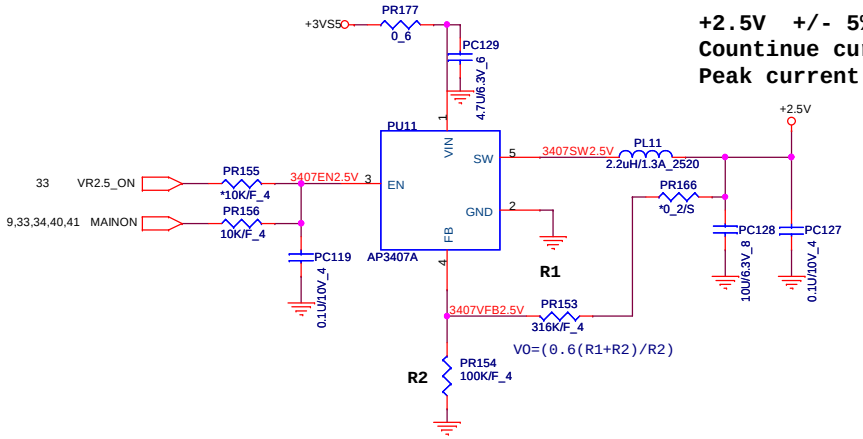


+1.1V Volt +/- 5%
Countinue current:5A
Peak current: 6.5A
OCP minimum:7.5A



+2.5V +/- 5%
Countinue current:0.3A
Peak current:0.75A

PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.1VS5 (RT8228)/2.5V	1A

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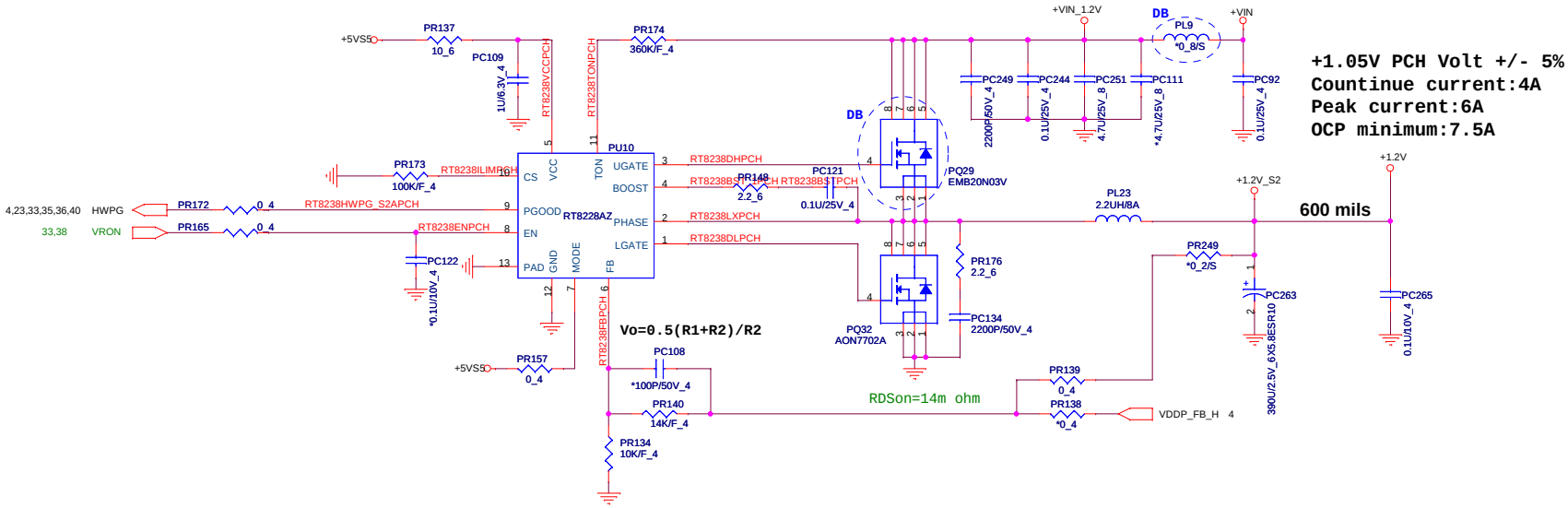

PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.2V (RT8228)	1A

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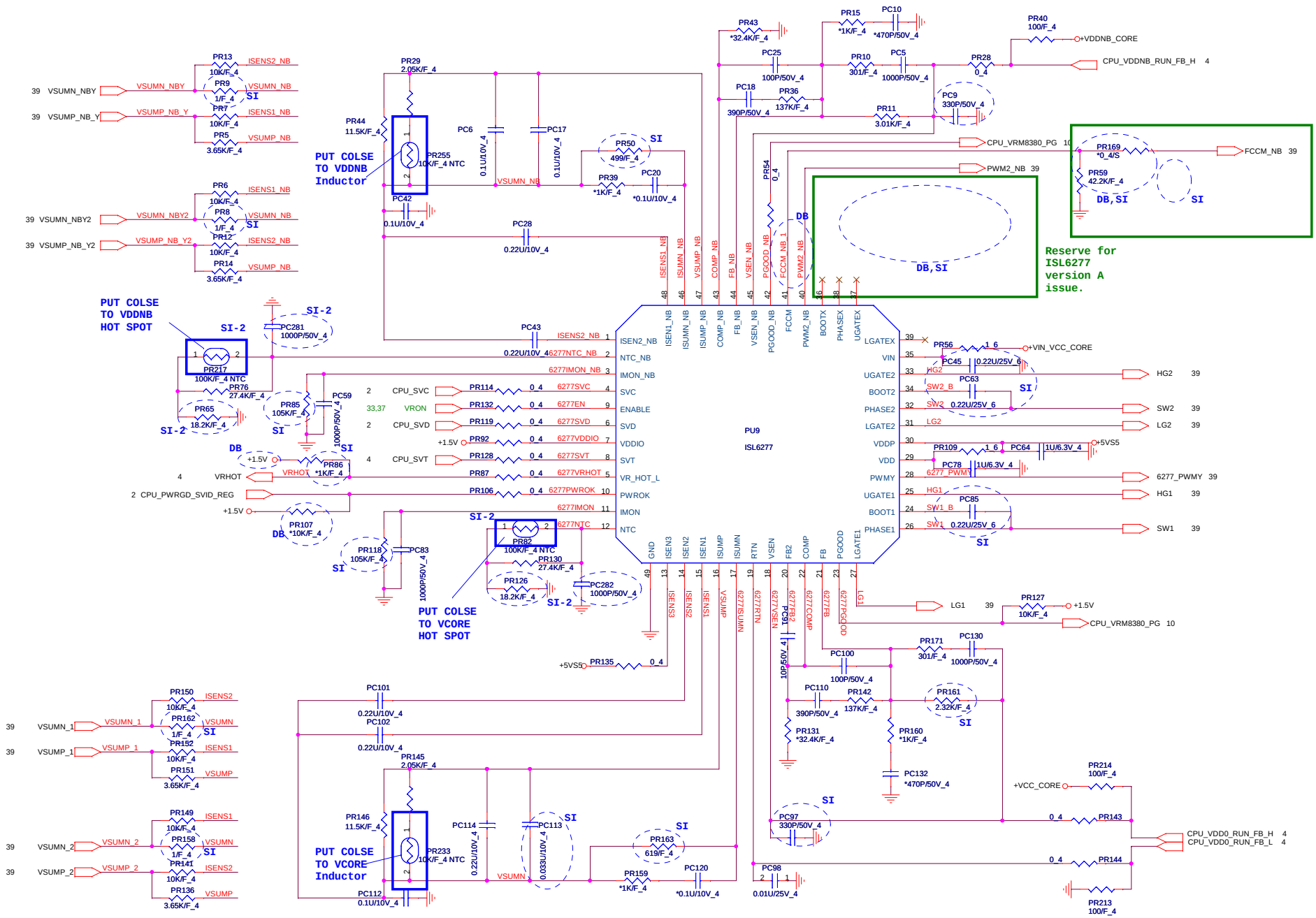
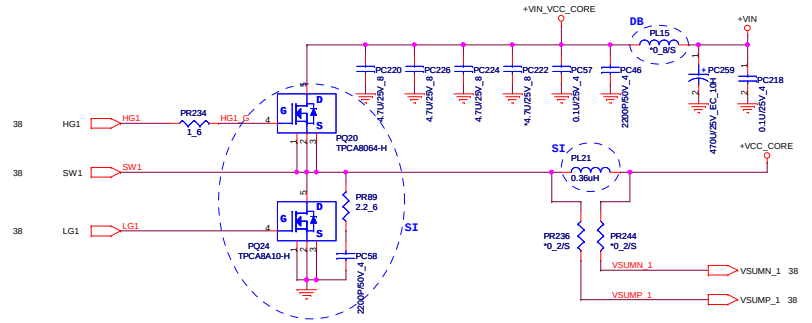
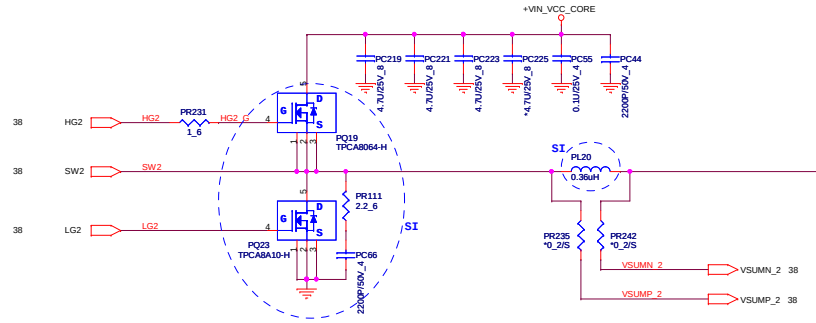
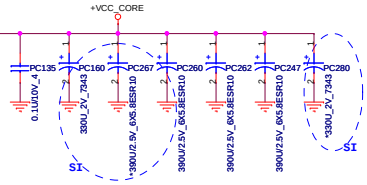
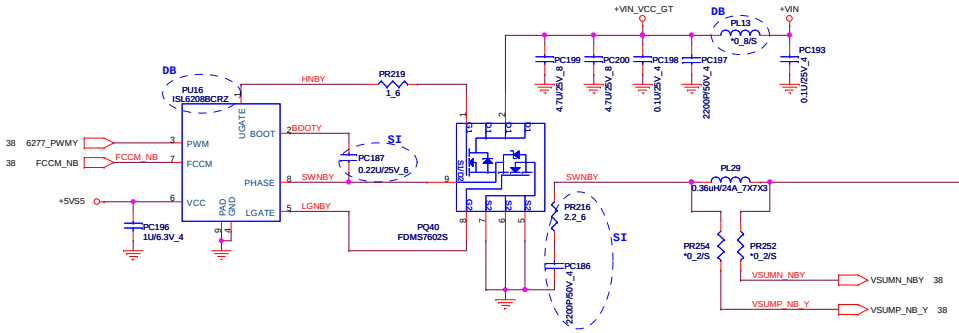

PU9
ISL6277
PUT COLSE TO VDDNB Inductor
PUT COLSE TO VDDNB HOT SPOT
PUT COLSE TO VCORE HOT SPOT
PUT COLSE TO VCORE Inductor
Reserve for ISL6277 version A issue.
+VDDNB_CORE
CPU_VDDNB_RUN_FB_H
CPU_VRM8380_PG
PWM2_NB
FCCM_NB
+VIN_VCC_CORE
HG2
SW2
LG2
+5VS5
6277_PWMY
HG1
SW1
LG1
+1.5V
CPU_VRM8380_PG
+VCC_CORE
CPU_VDD0_RUN_FB_H
CPU_VDD0_RUN_FB_L
VSUMN_NBY
VSUMP_NB_Y
VSUMN_NBY2
VSUMP_NB_Y2
VSUMN_1
VSUMP_1
VSUMN_2
VSUMP_2
CPU_SVC
VRON
CPU_SVD
CPU_SVT
VRHOT
CPU_PWRGD_SVID_REG



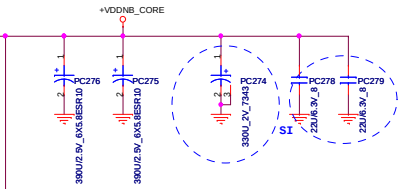


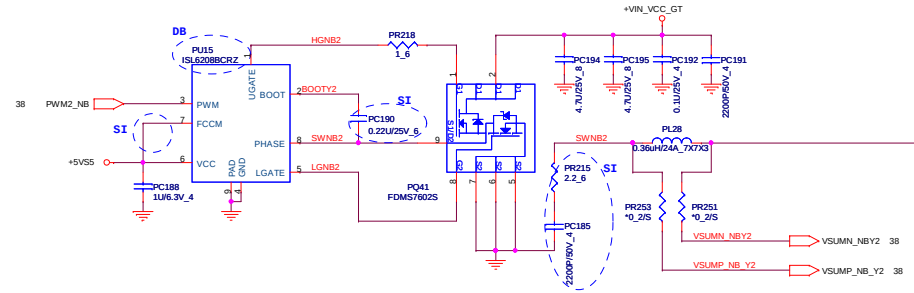
CPU CORE Volt
Countinue current:36A
Peak current:50A
OCP minimum:60A





VDDNB Volt
Countinue current:25A
Peak current:33A
OCP minimum:40A





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Quanta Computer Inc.

Size	Document Number	Rev
Custom	ISL6208	1A

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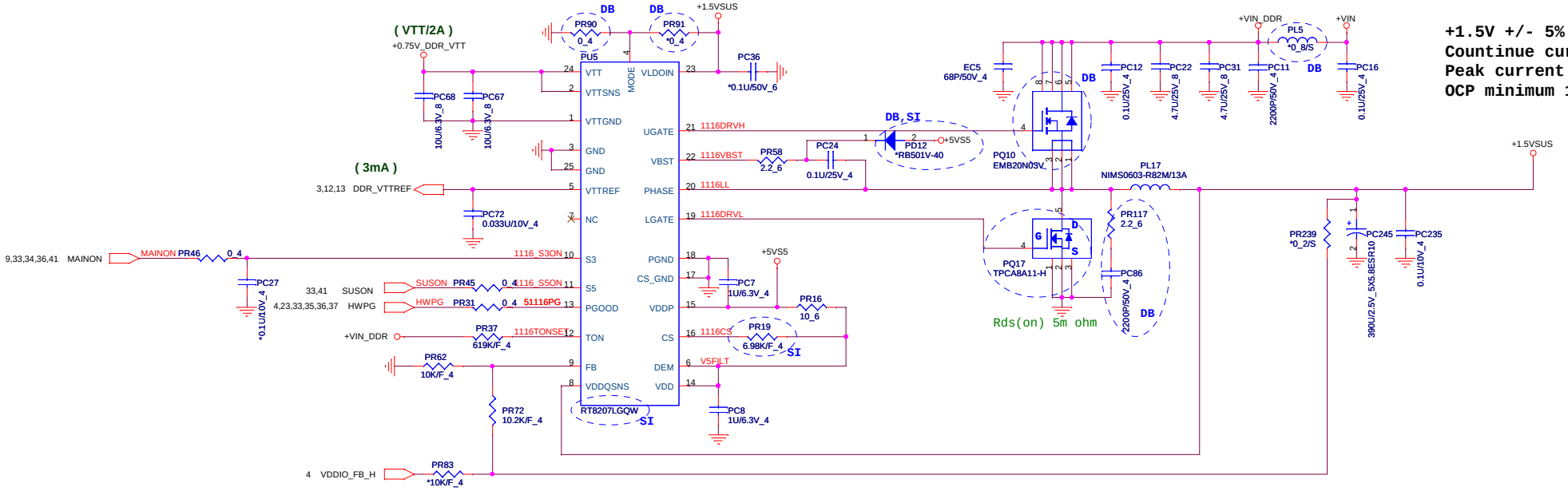

+1.5V +/- 5%
Countinue current:10A
Peak current:12A
OCP minimum 15A

PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDRIII(G5616)	1A

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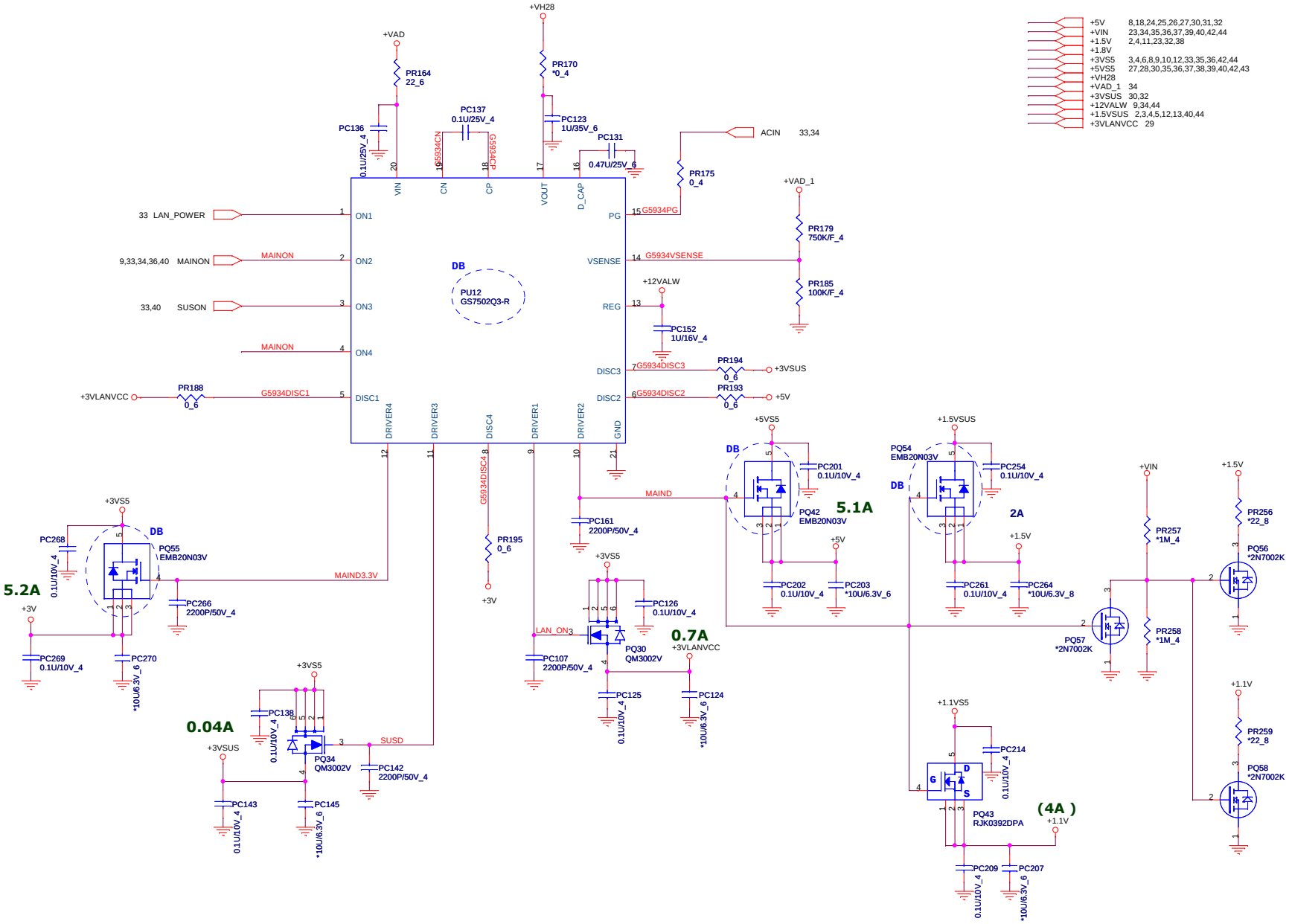

PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Dis-charge IC (GS7502)	1A

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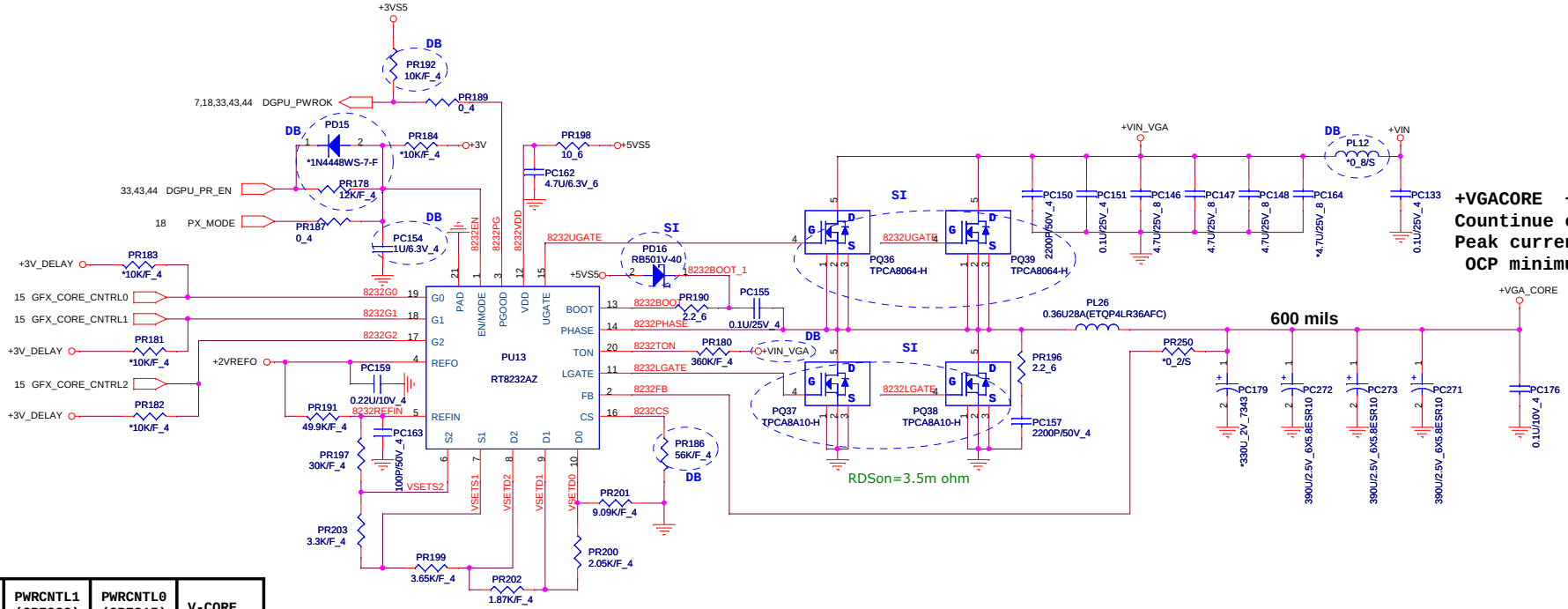
VGA Core



+VGACORE +/- 5%
Countinue current:20A
Peak current:23A
OCP minimum 33A

Symour-XT	PWRCNTL2 (GPIO16)	PWRCNTL1 (GPIO20)	PWRCNTL0 (GPIO15)	V-CORE
L	0	0	0	1.0V
M	0	0	1	0.9V
H	0	1	0	0.875V
	0	1	1	0.85V
	1	0	0	0.8V
	1	0	1	0.75V

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGACORE (RT8232AZ)	1A

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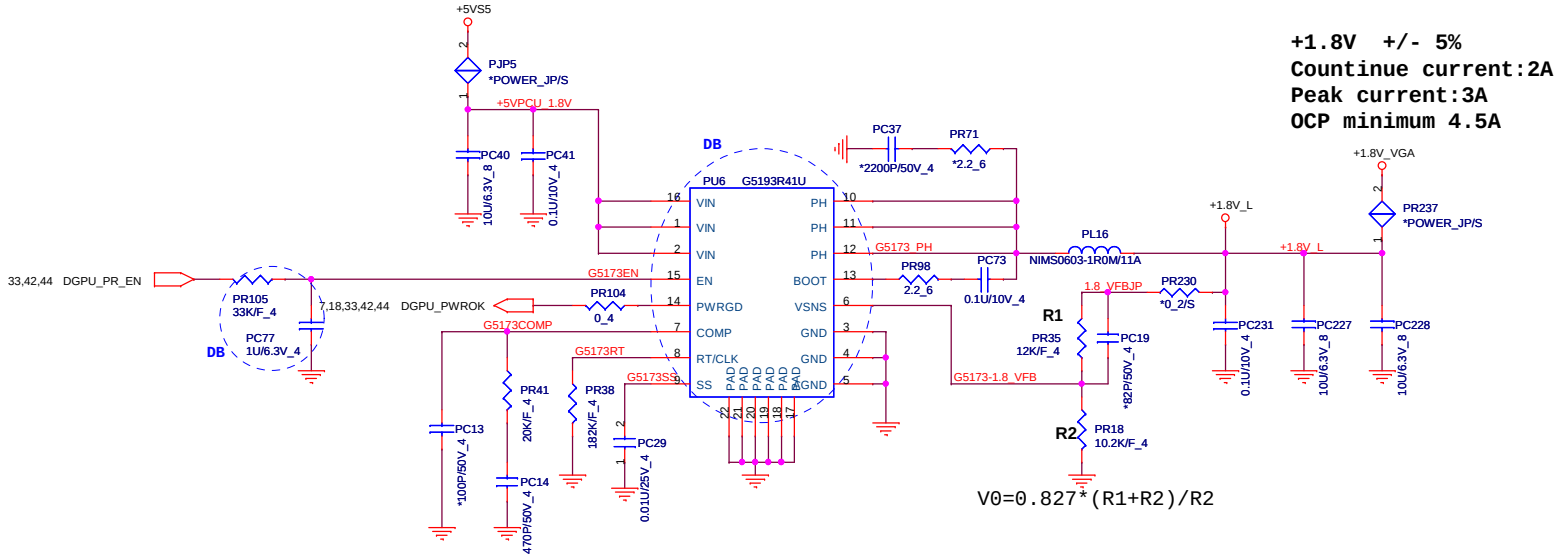
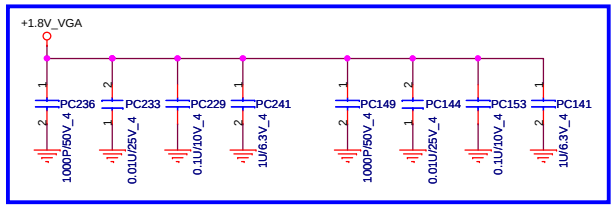


+1.8V +/- 5%
Countinue current:2A
Peak current:3A
OCP minimum 4.5A

V0=0.827*(R1+R2)/R2

DB for prevent interference



PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.8V_VGA (G5193)	1A

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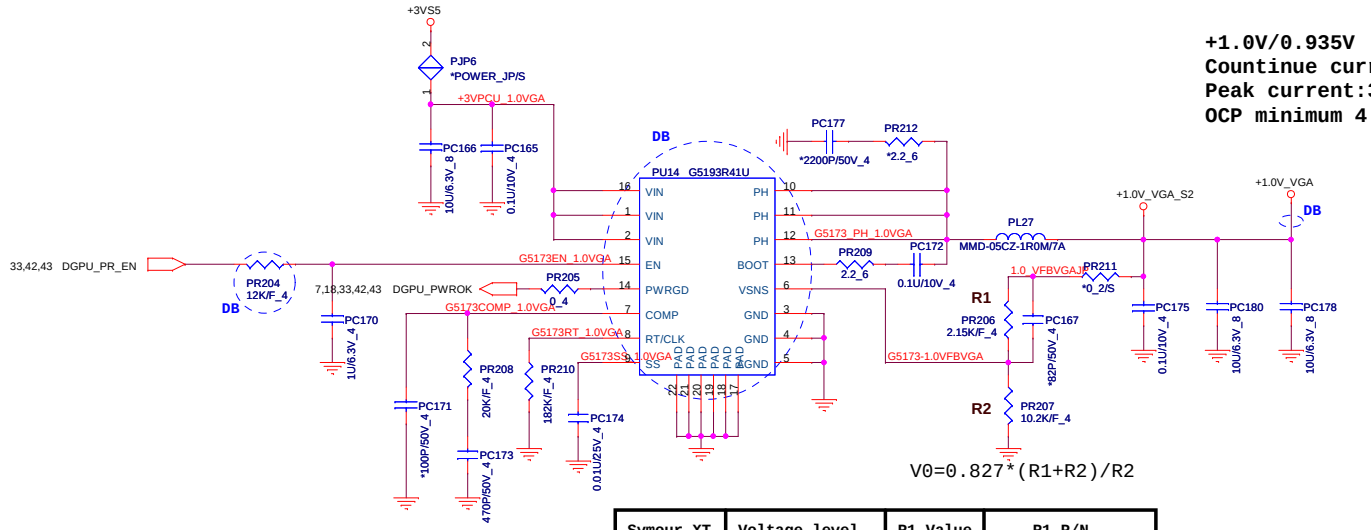
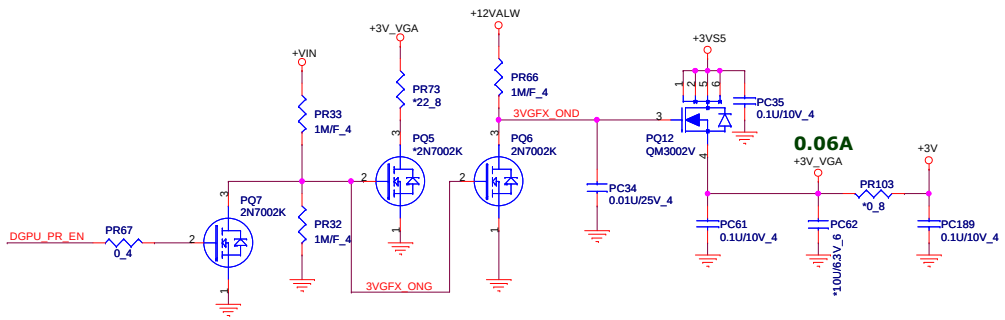


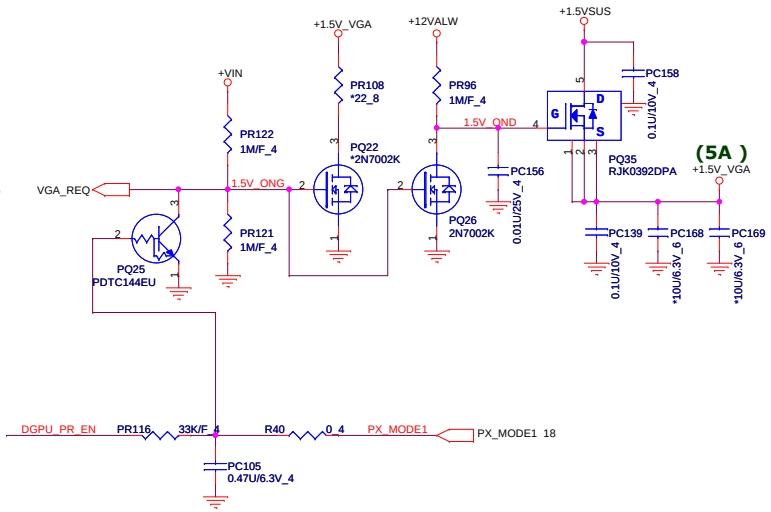
+1.0V/0.935V +/- 5%
Countinue current:2A
Peak current:3A
OCP minimum 4.5A

+3V	2,4,6,8,9,10,11,12,13,14,18,23,24,25,26,27,28,29,30,31,32,33,41,42
+VIN	23,34,35,36,37,39,40,41,42
+3VS5	3,4,6,8,9,10,12,33,35,36,41,42
+5VS5	27,28,30,35,36,37,38,39,40,41,42,43
+3V_VGA	18,30
+12VALW	9,34,41
+1.5VSUS	2,3,4,5,12,13,40,41
+1.5V_VGA	18,20,21,22

V0=0.827*(R1+R2)/R2

Symour-XT	Voltage level	R1 Value	R1 P/N
17W	1.0V	2.15K	CS22152FB07
25W	0.935V	1.37K	CS21372FB19





PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.0V_VGA (G5193)	1A

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