

COMPAL CONFIDENTIAL

MODEL NAME : JAL21  
PCB NO : LA-4042P (DAA00000T0L)  
BOM P/N : 43153331L01

M09 Maybach DIS  
uFCPGA Mobile Penryn  
Intel Cantiga PM + ICH9M

2007-10-30  
REV : 0.1

@ : Nopop Component

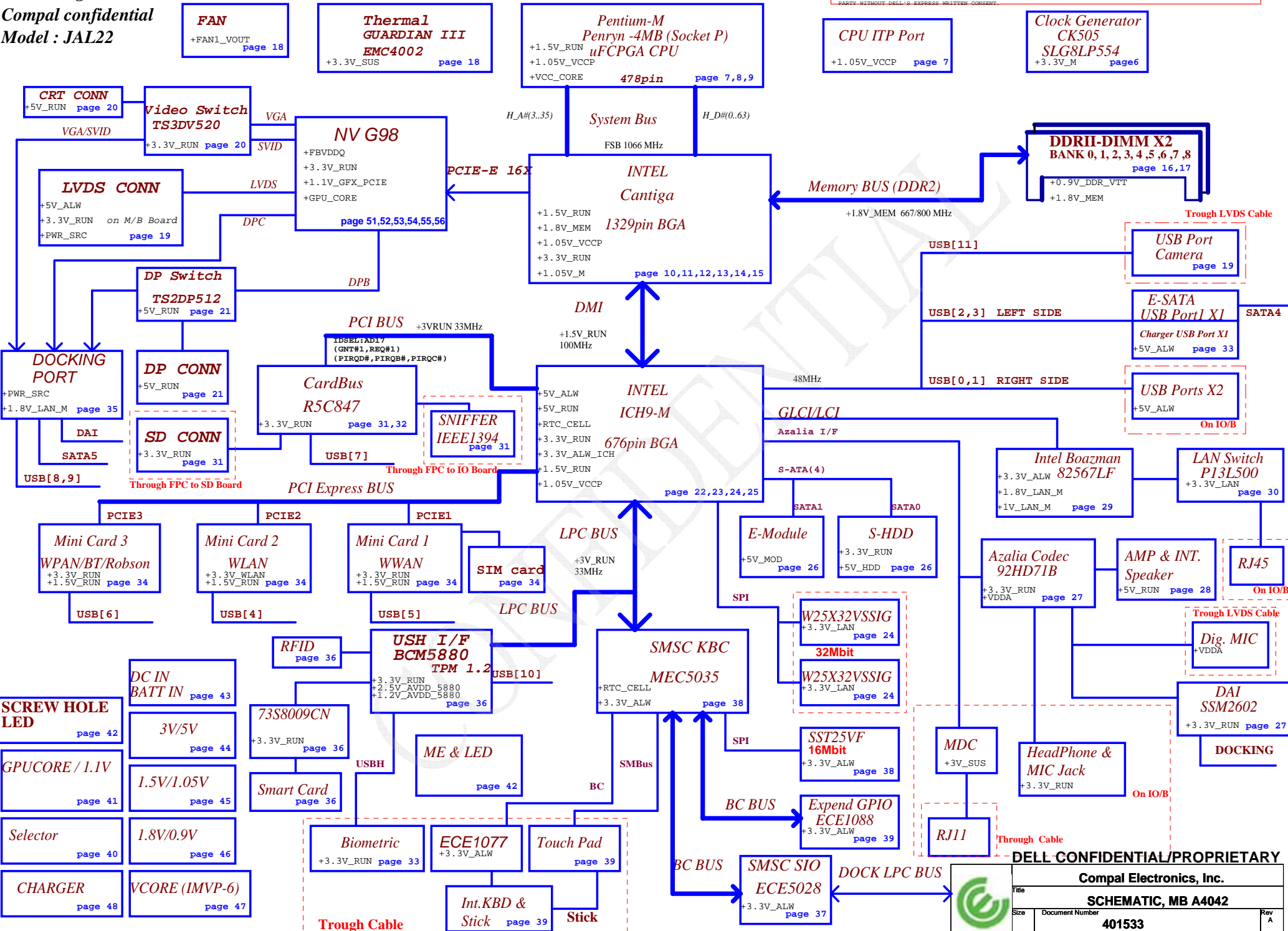
MB PCB	
Part Number	Description
DAA00000R0L	PCB 03P LA-4051P REV0 M/B

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Block Diagram  
Compal confidential  
Model : JAL22



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## POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	ON
S4 (Suspend to DISK) / M1	LOW	HIGH	HIGH	LOW	HIGH	ON	ON	ON	OFF	ON
S5 (SOFT OFF) / M1	LOW	HIGH	LOW	LOW	HIGH	ON	ON	ON	OFF	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

## PM TABLE

State power plane	+15V_ALW +5V_ALW +3.3V_ALW_ICH +3.3V_RTC_LDO	+3.3V_SUS +1.8V_MEM	+5V_RUN +3.3V_RUN +2.5V_RUN +1.5V_RUN +0.9V_DDR_VTT +GPU_CORE +VCC_CORE +1.05V_VCCP +FBVDDQ +1.1V_GFX_PCIE	+3.3V_M +1.05V_M (M-OFF)	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

## PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
R5C847	AD17	REQ#1 / GNT#1	PIRQ[B..D]

ICH9-M	USB PORT#	DESTINATION
	0	JUSB1 (Ext Right Side Top)
	1	JUSB1 (Ext Right Side Bottom)
	2	JESA1 (Ext Left Side Bottom)
	3	JESA1 (Ext Left Side TOP)
	4	WLAN
	5	WWAN
	6	WPAN
	7	Card Bus/Express card
	8	DOCKING
	9	DOCKING
	10	USH->BIO
	11	Camera

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	MINI CARD-3 BT/UWB
Lane 4	EXPRESS CARD
Lane 5	None
Lane 6	10/100/1G LAN

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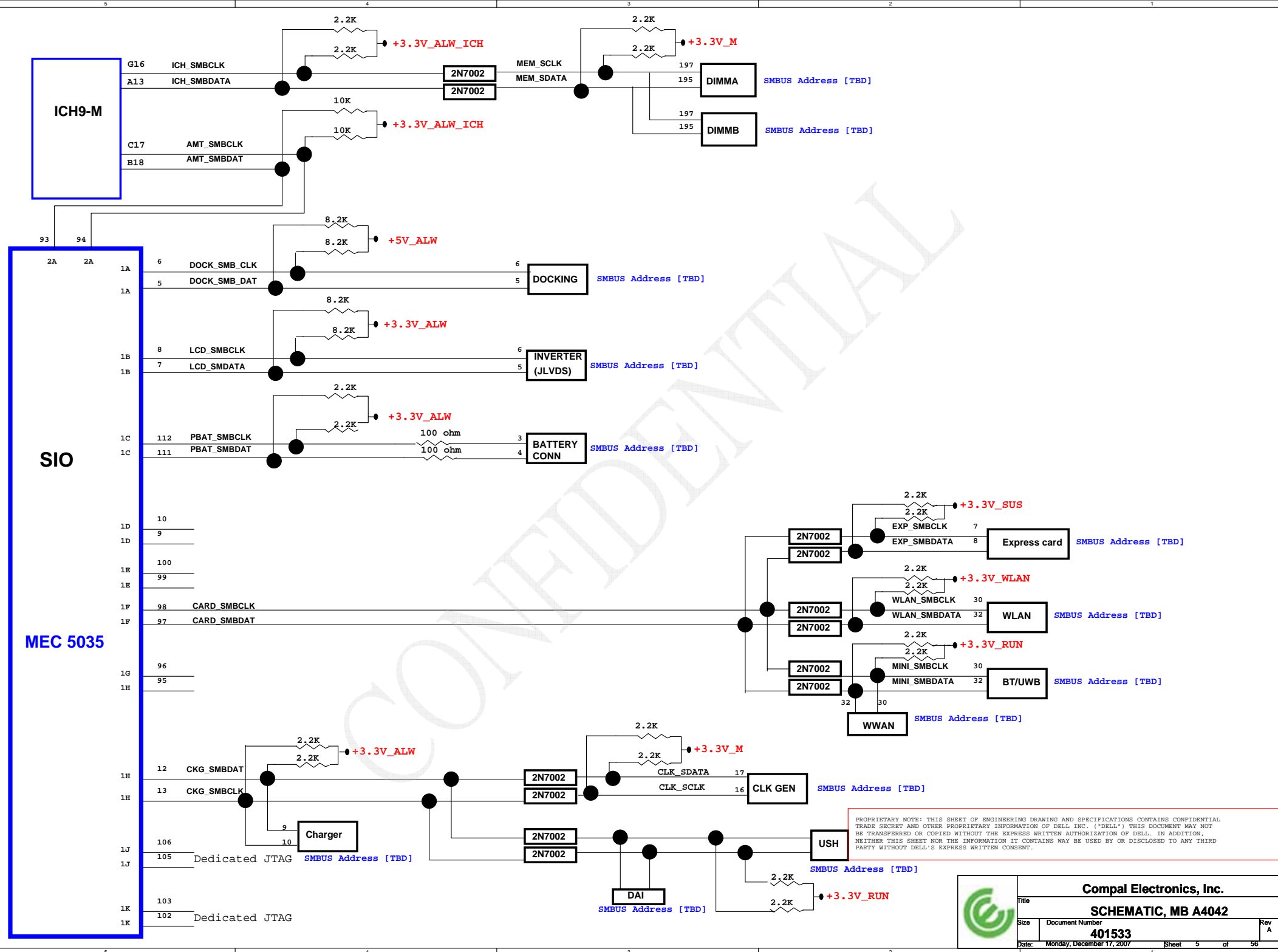
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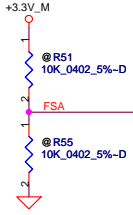


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FSC	FSB	FSA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz
0	0	0	266	100	33.3
0	0	1	133	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3
1	0	0	333	100	33.3
1	0	1	100	100	33.3
1	1	0	400	100	33.3



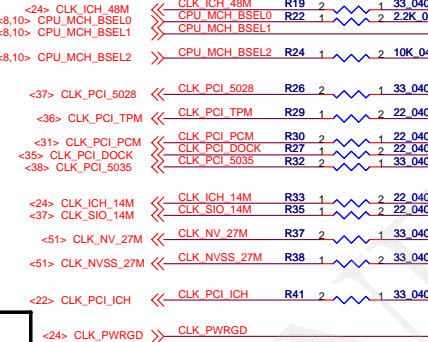
TME	PIN 32
0	overclocking enabled
1	overclocking disabled

ITP_EN	PIN 37
0	Pin 5/6 as SRC_10
1	Pin 5/6 as CPU_ITP

FCTSEL1	PIN43	PIN44	PIN47	PIN48
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1=DIS	27M_out	27M SSout	SRCT0	SRCC0

0=UMA  
1=Disc. GRFX down

Place crystal within 500 mils of CK505

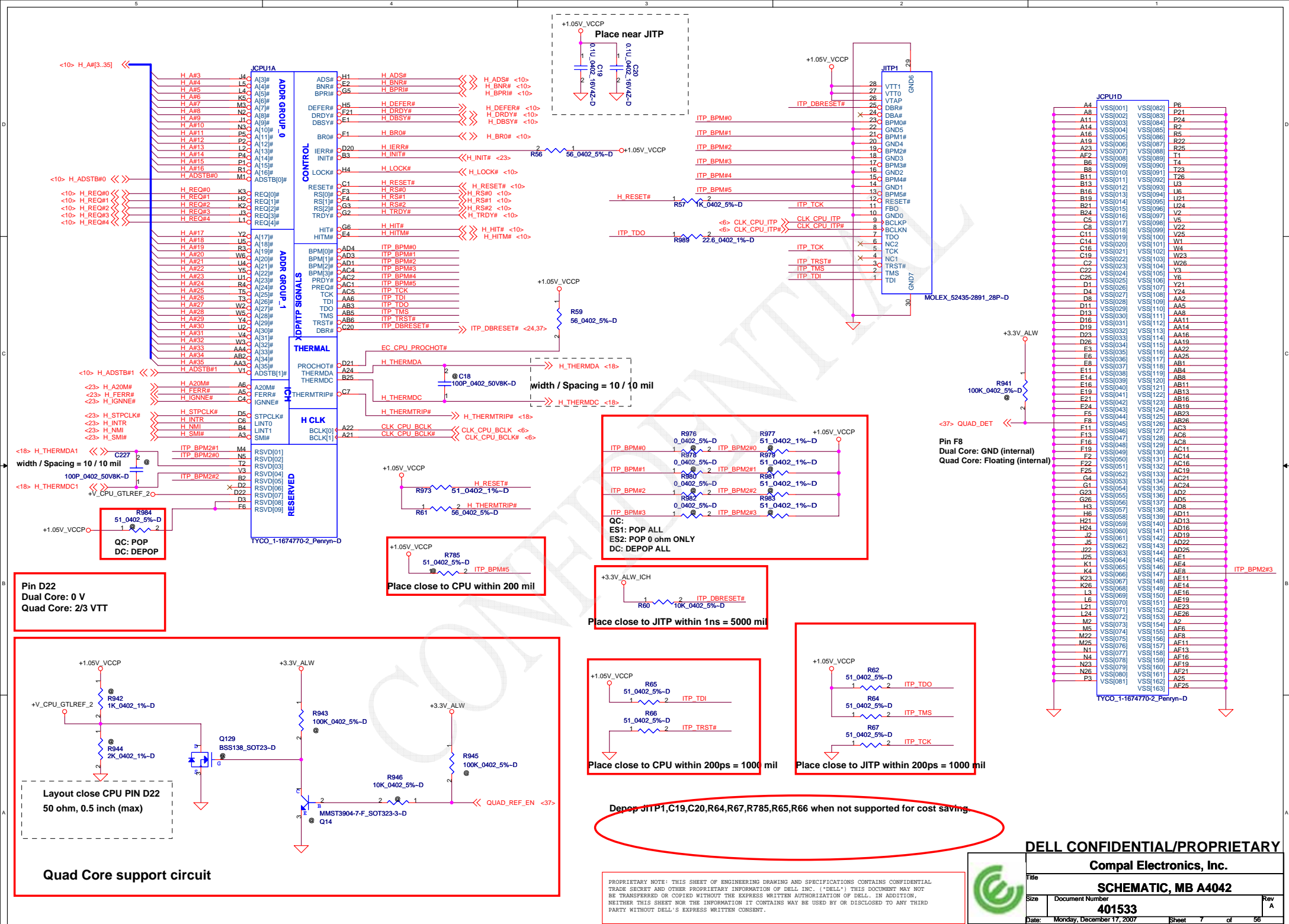


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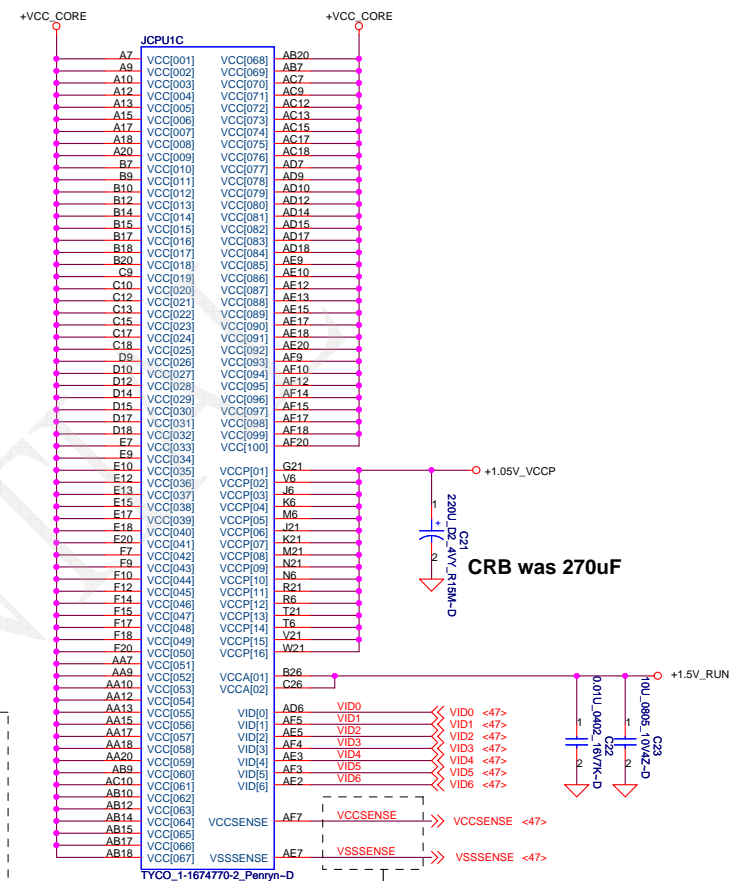


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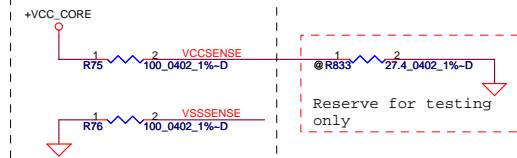






Length match within 25 mils,  $Z_0=27.4$  ohm

**Place R75 and R76 near CPU**



Route VCCSENSE and VSSSENSE trace at  
27.4 ohms, 7 mils spacing and the placement should be within 1 inch (max)

Layout close CPU PIN AD26  
50 ohm, 0.5 inch (max)

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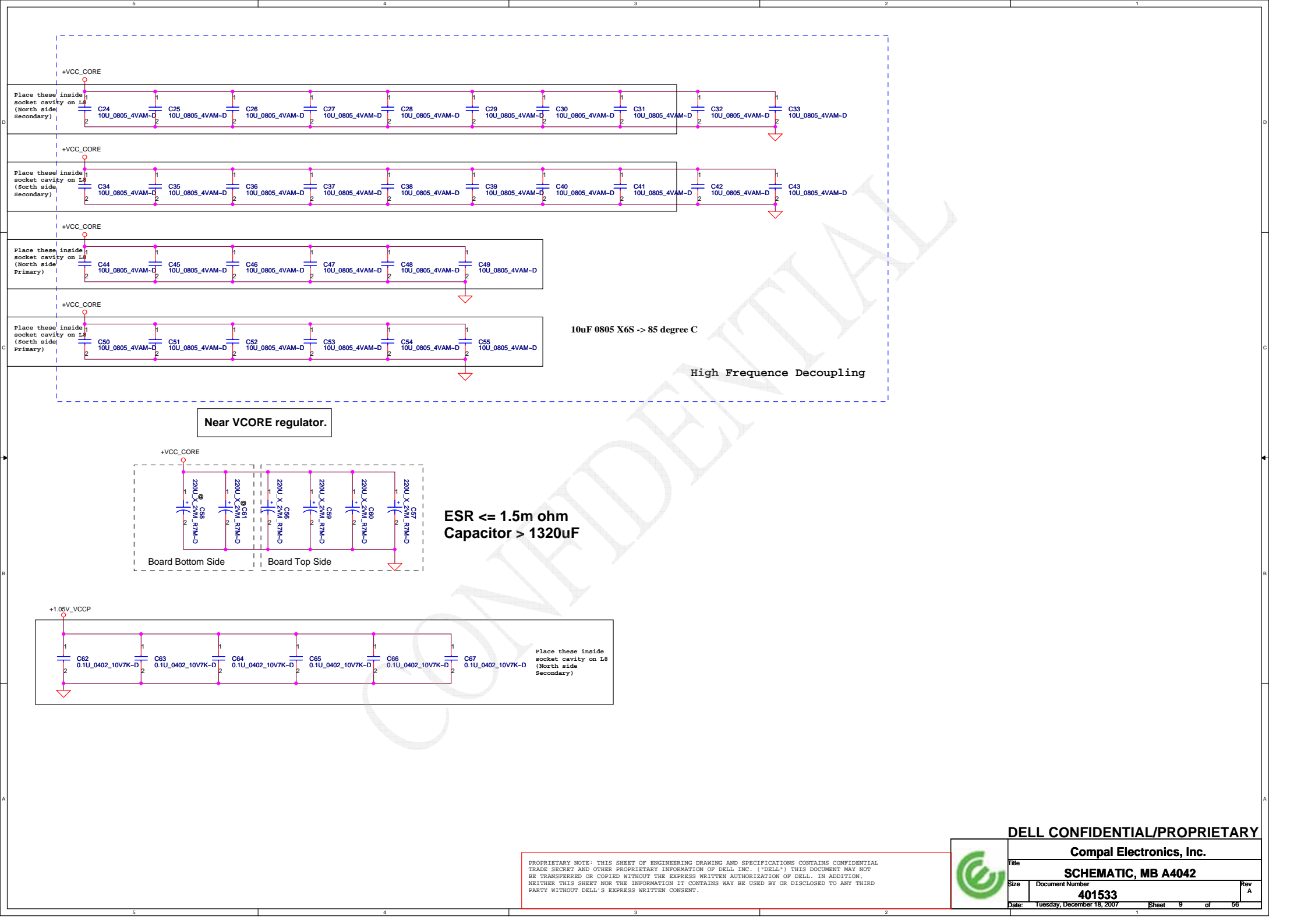
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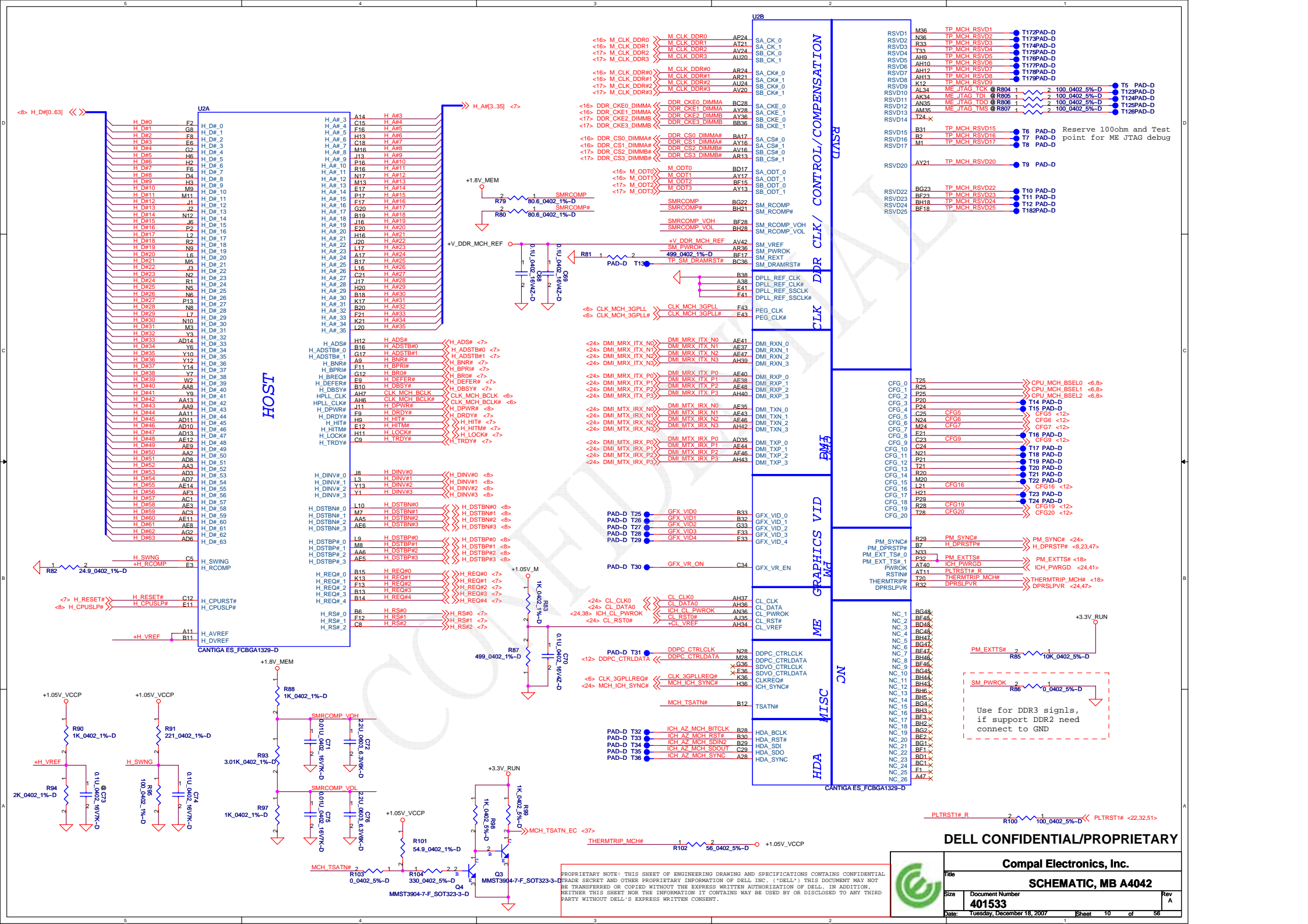
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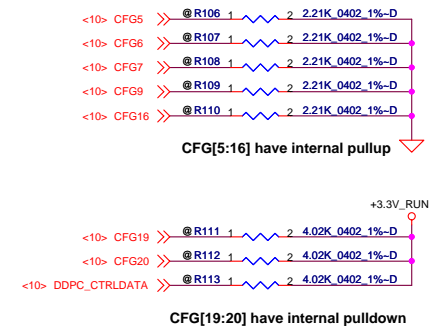
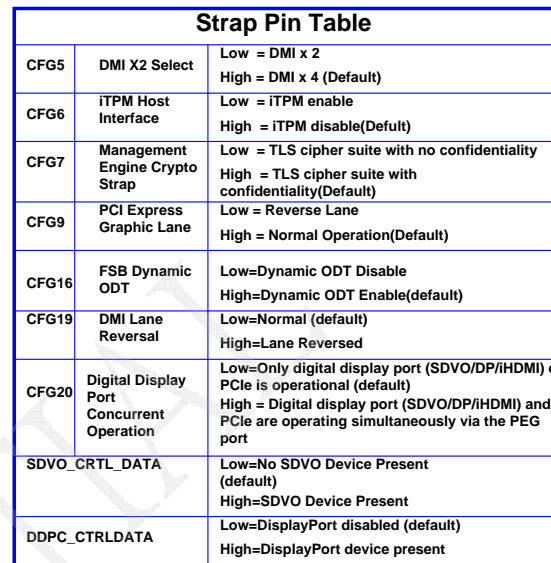
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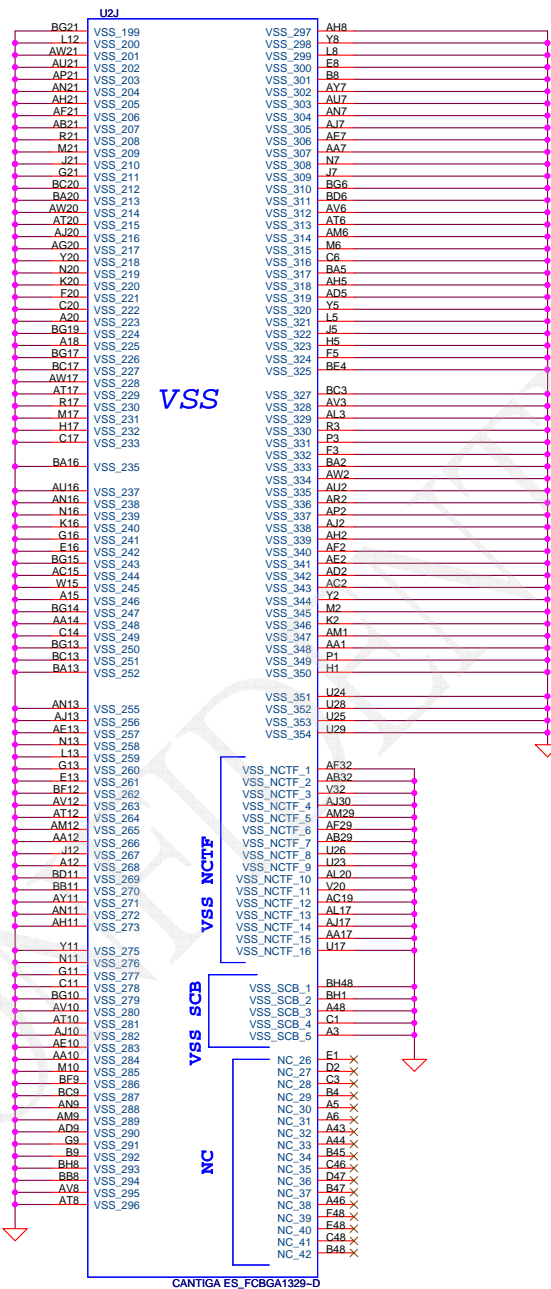
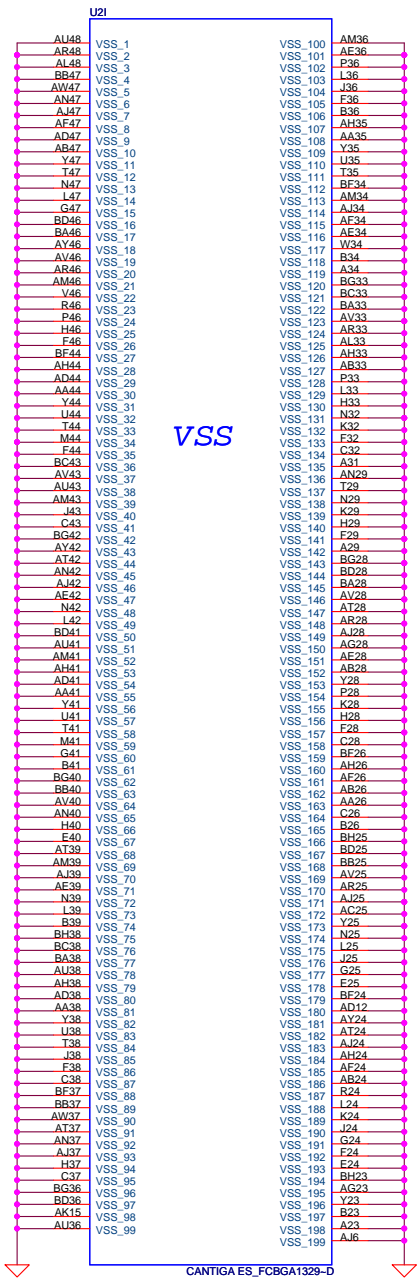












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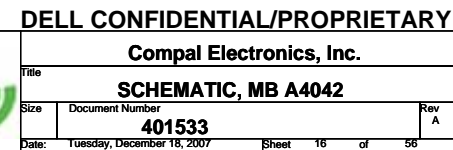
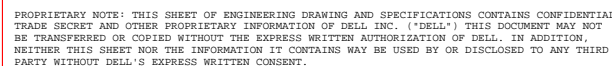
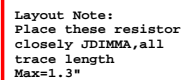
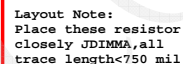
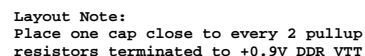
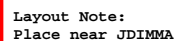
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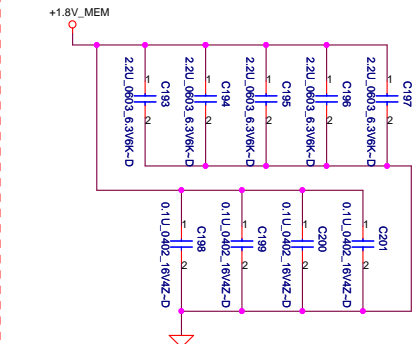
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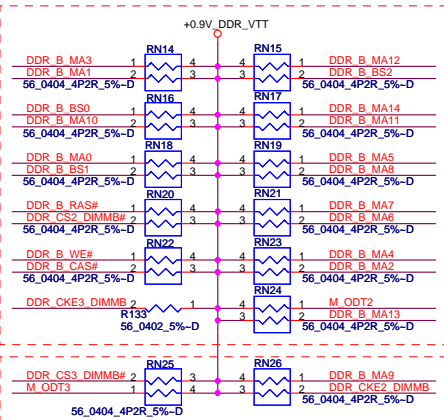
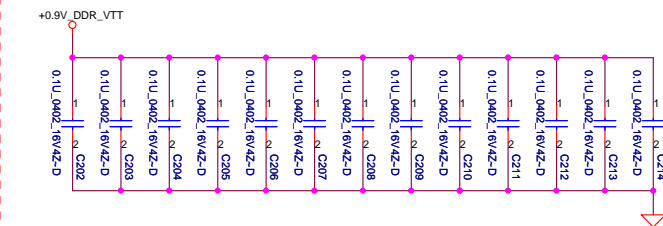


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<11> DDR\_B\_D[0..63] <<>>  
<11> DDR\_B\_DM[0..7] <<>>  
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<11> DDR\_B\_MA[0..14] <<>>

Layout Note:  
Place near JDIMMB

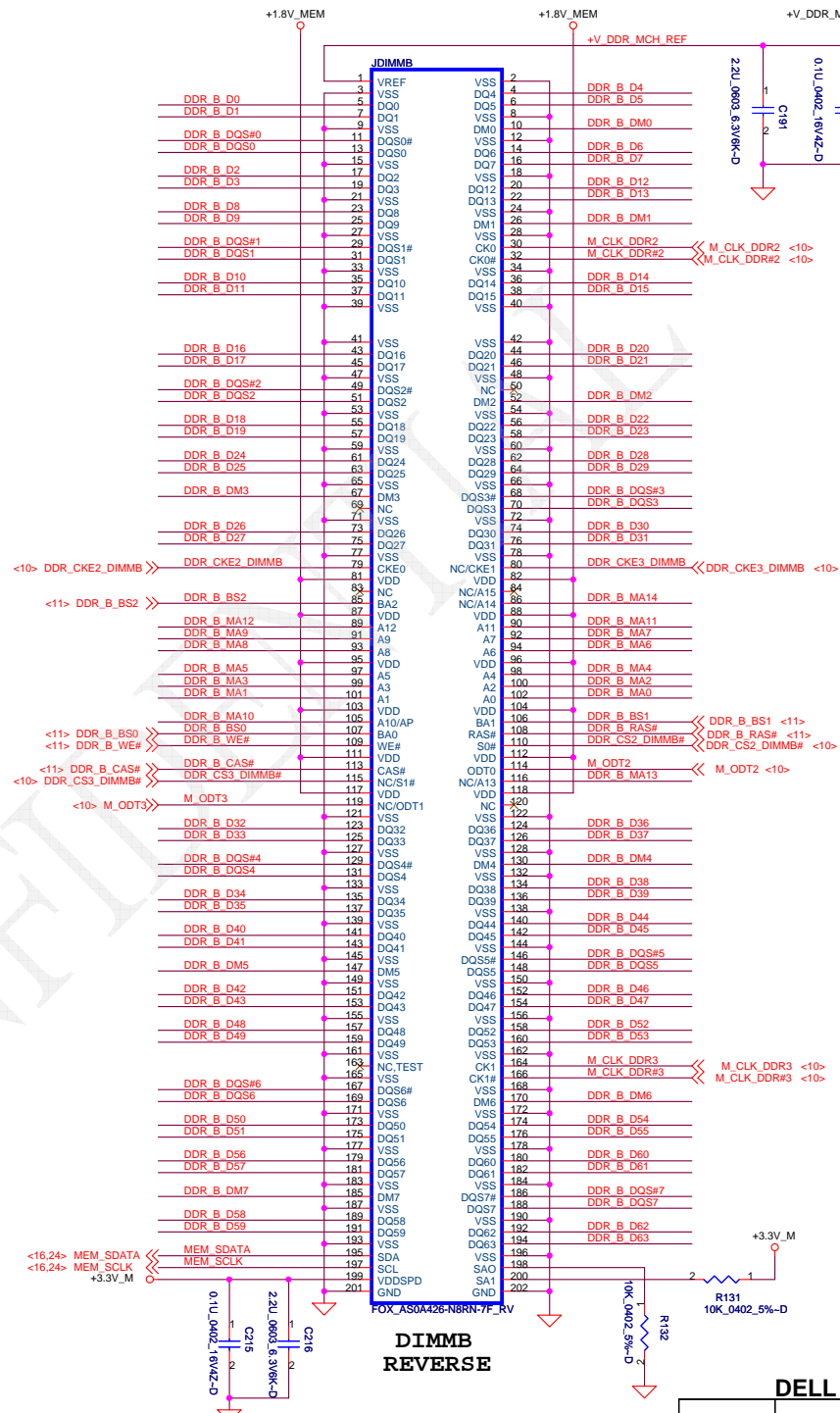


Layout Note:  
Place one cap close to every 2 pullup  
resistors terminated to +0.9V\_DDR\_VTT



Layout Note:  
Place these resistor  
closely JDIMMB, all  
trace length < 750 mil

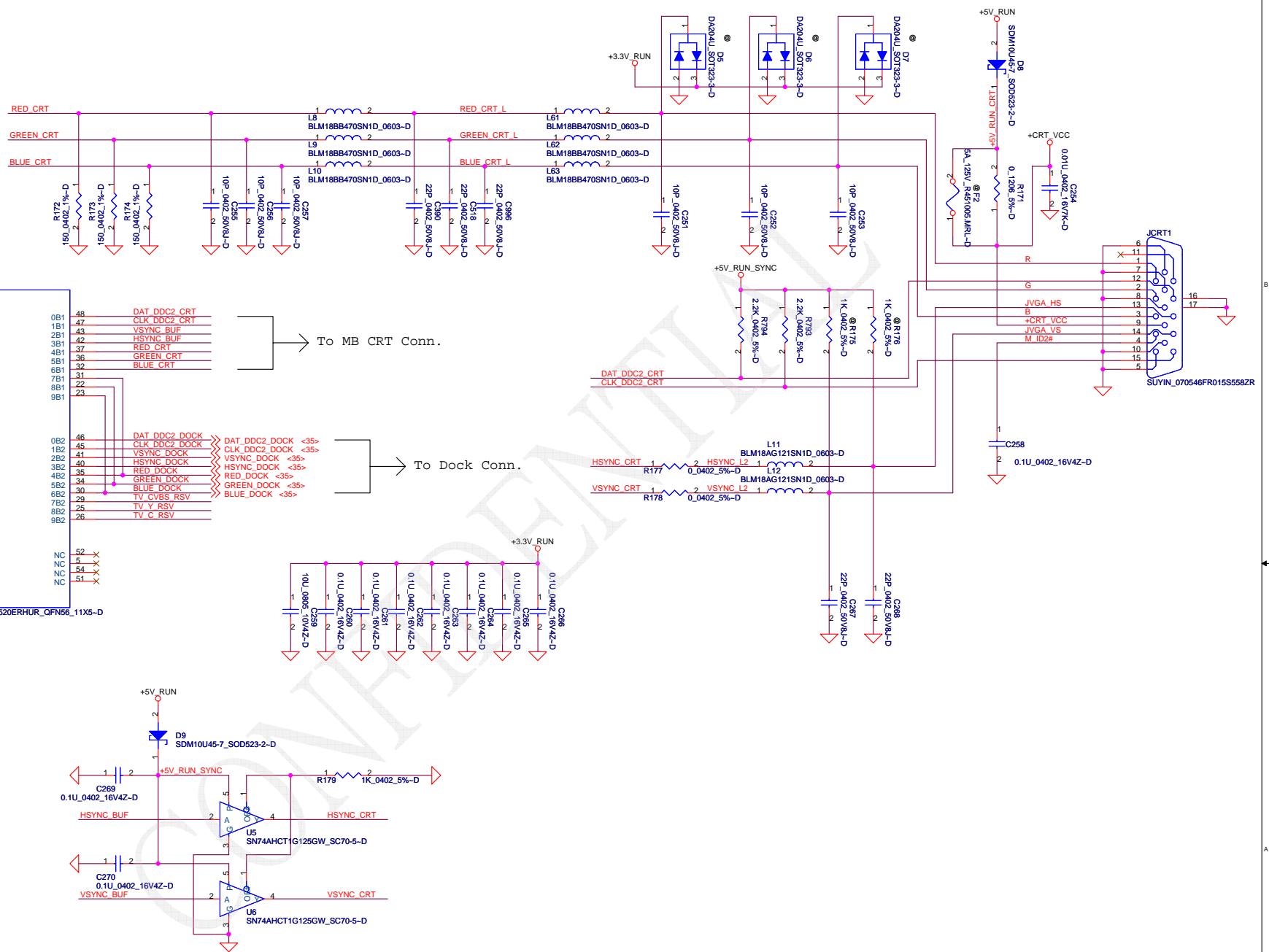
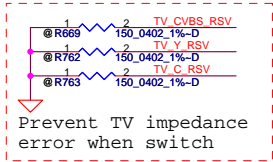
Layout Note:  
Place these resistor  
closely JDIMMB, all  
trace length  
Max=1.3"







SEL	CRT	TV
0	MB	LIO
1	APR/SPR	NA



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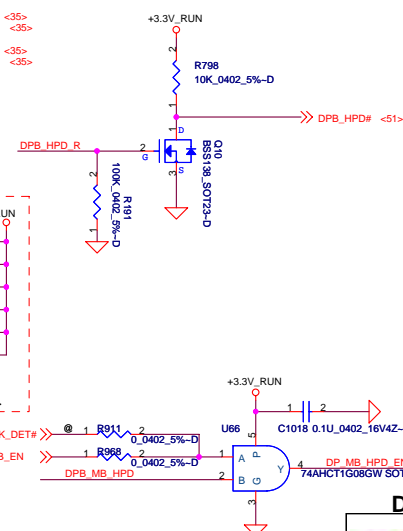
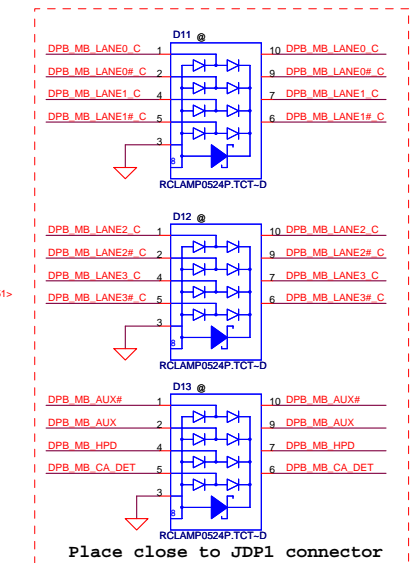
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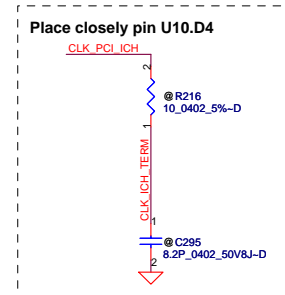
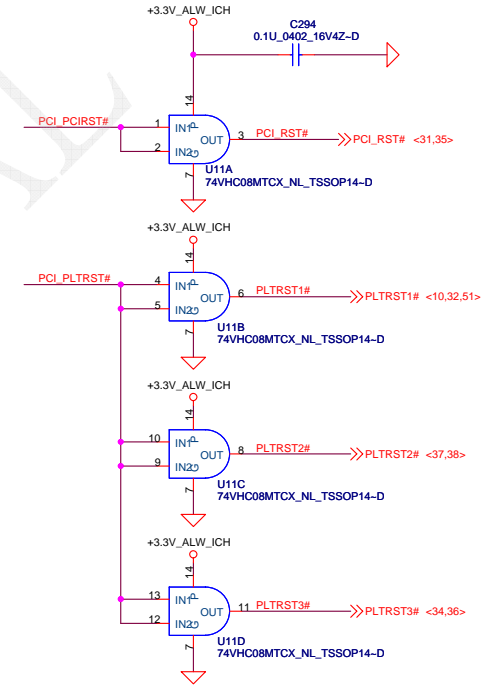
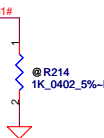
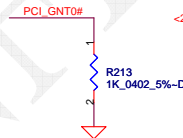
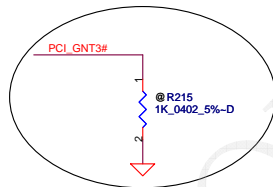
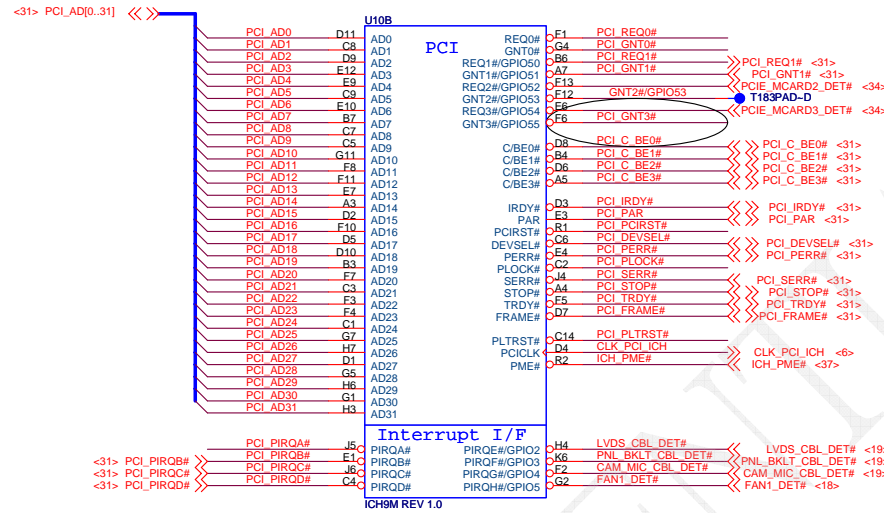
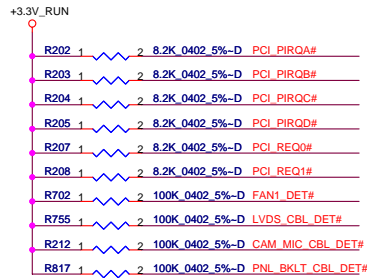
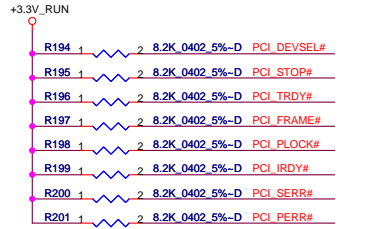
# SW for MB side

# SW for eDOCK side



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A16 away override strap.

PCI\_GNT3#/(MDC\_RST\_DIS#) Low = A16 swap override enabled. High = Default. pull up internal

Boot BIOS Strap

PCI_GNT0#	SPI_CS1#	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC

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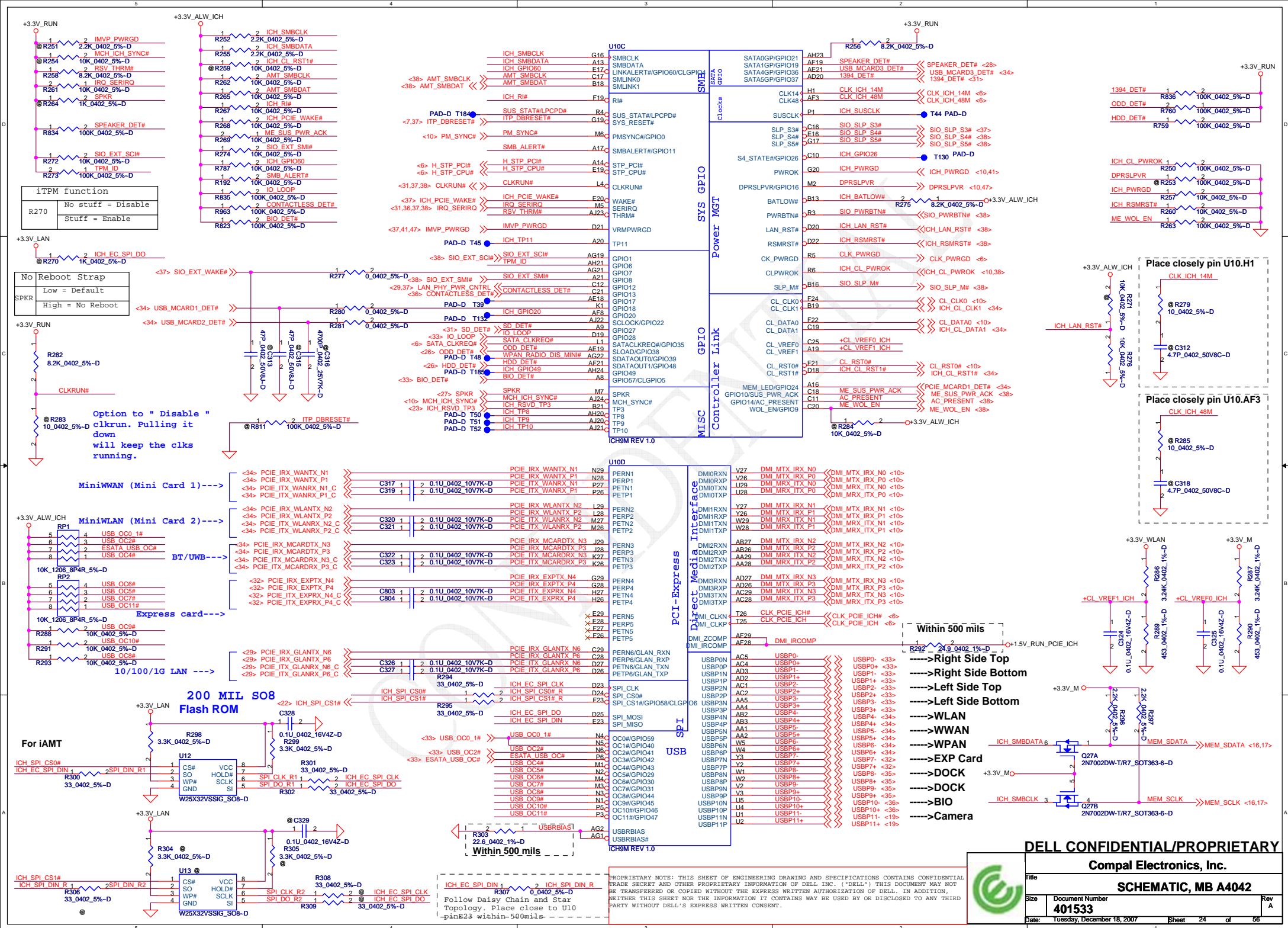
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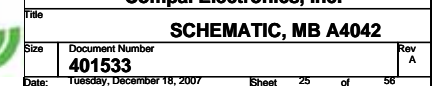
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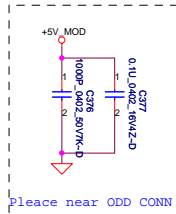
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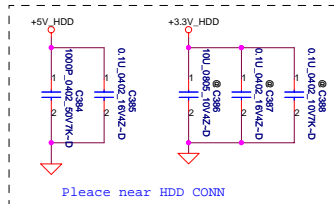
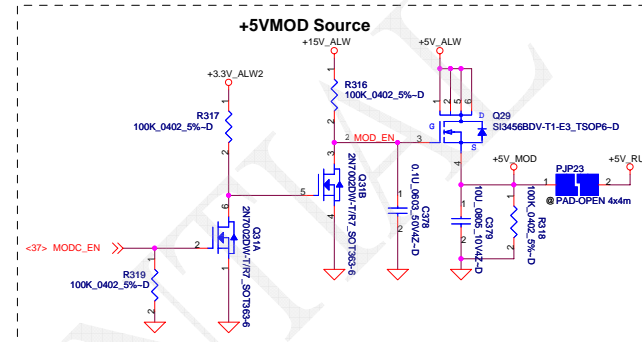
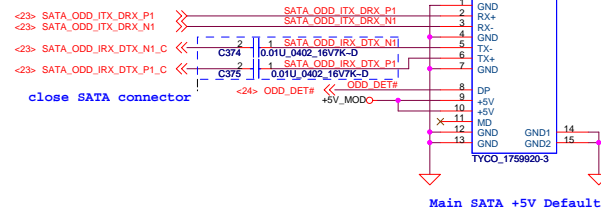




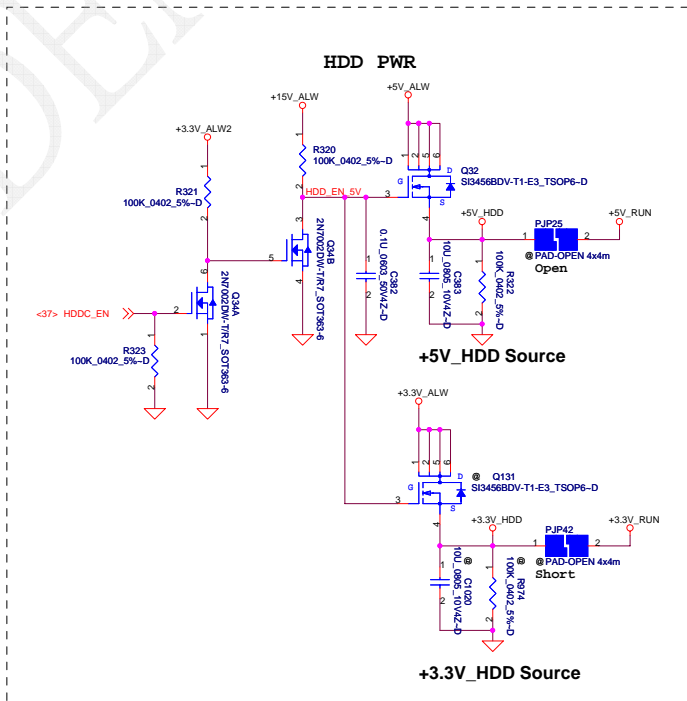
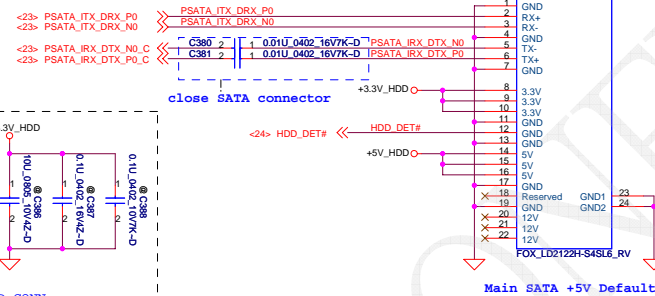




## For ODD



## For HDD



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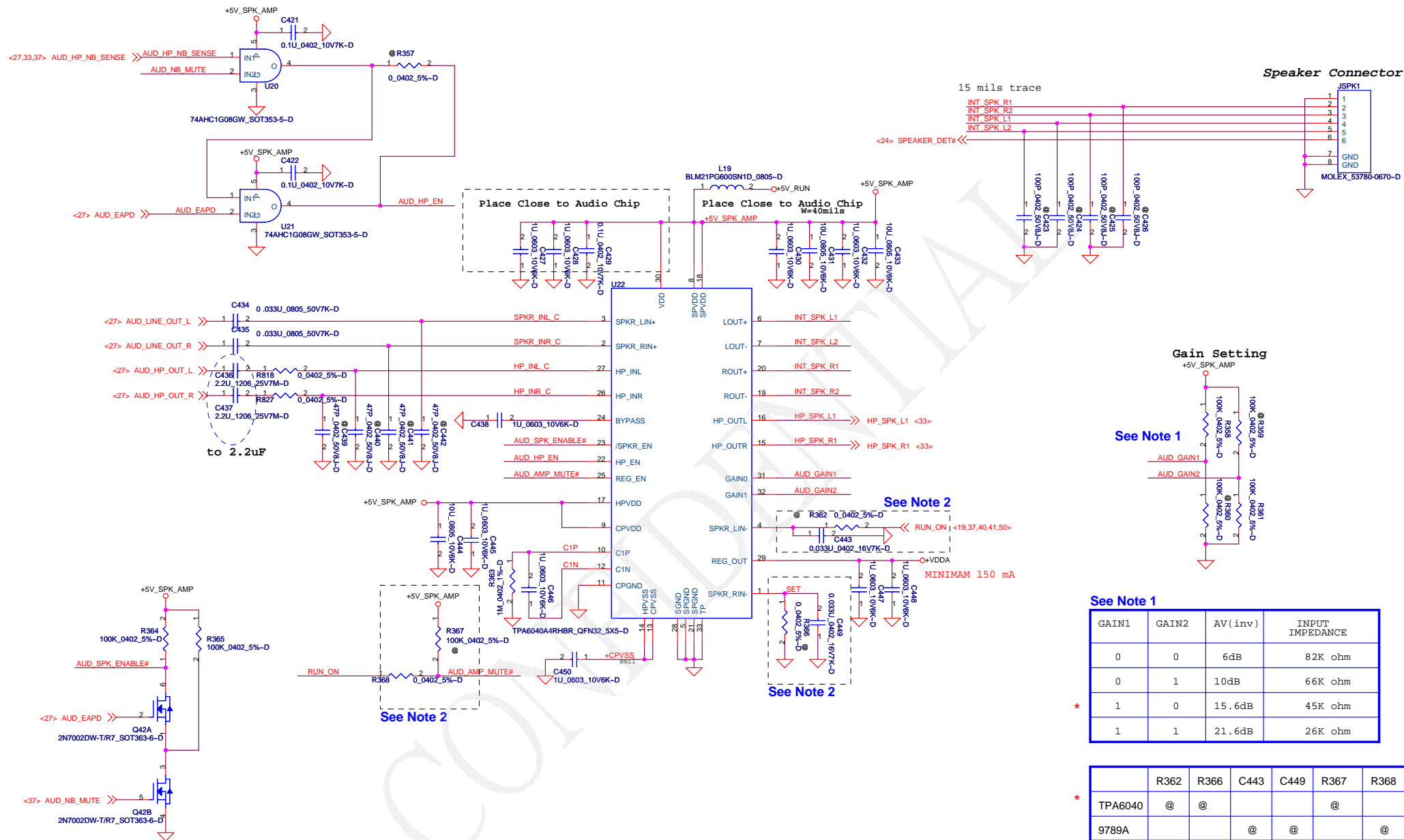
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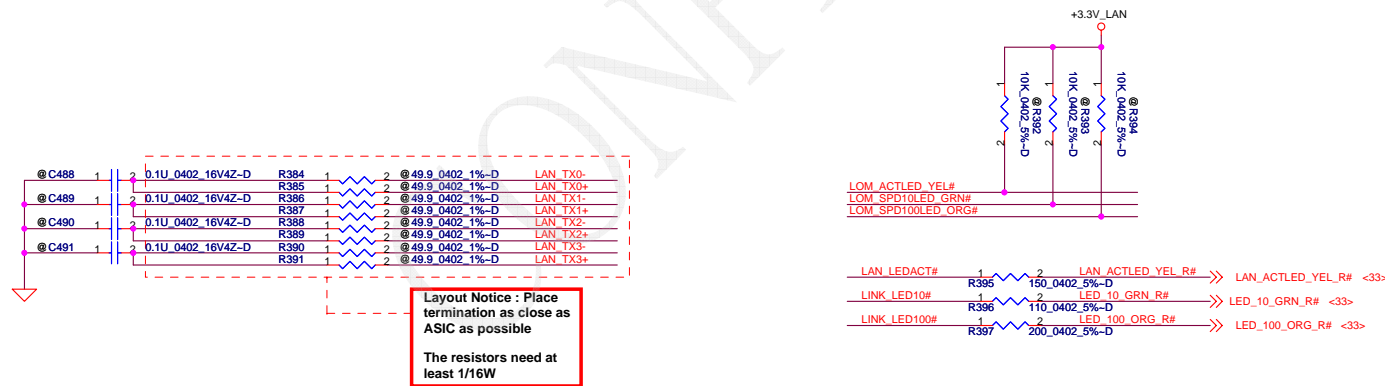
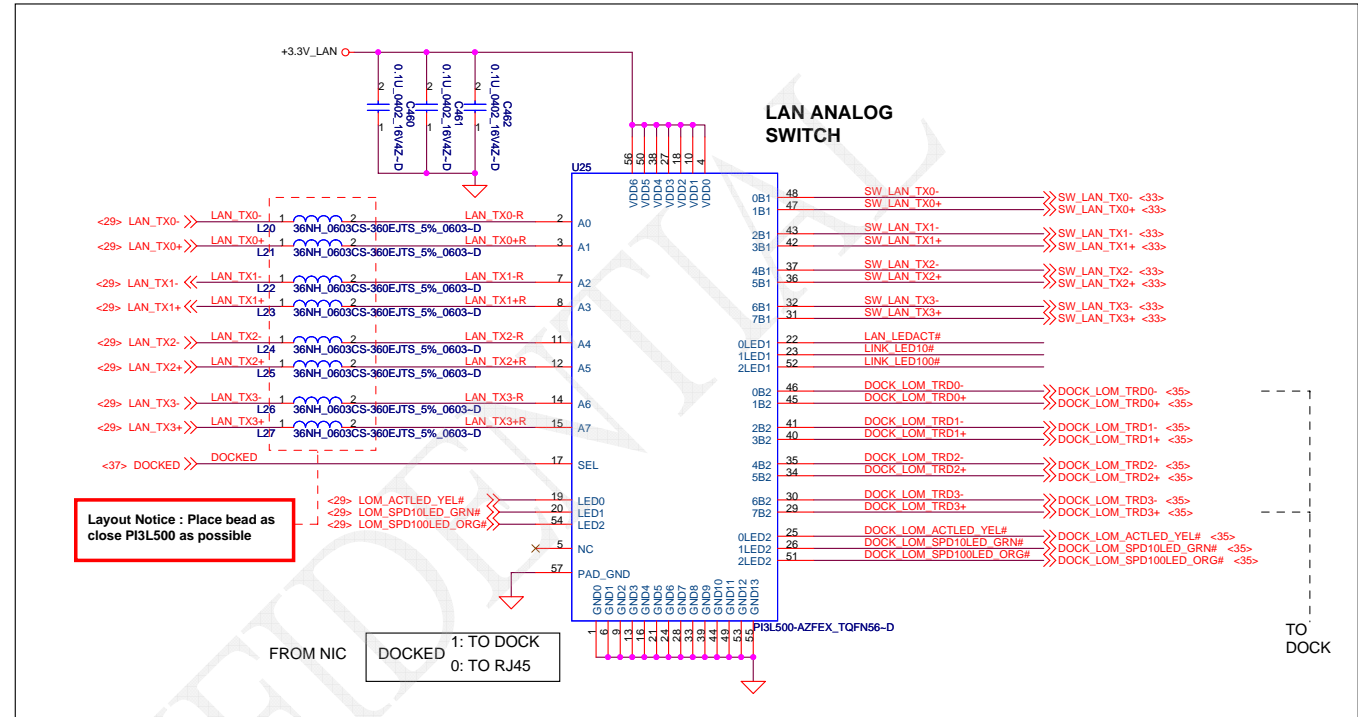
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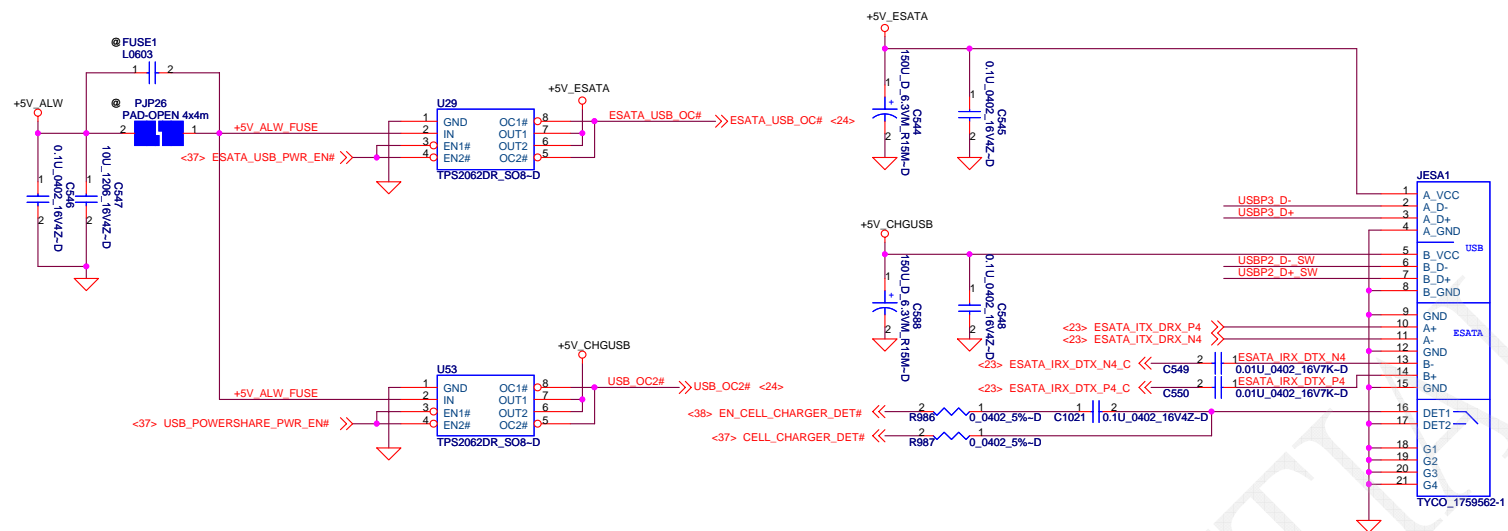
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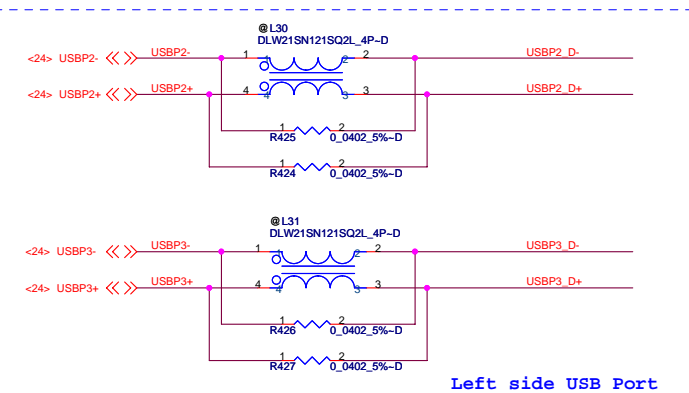
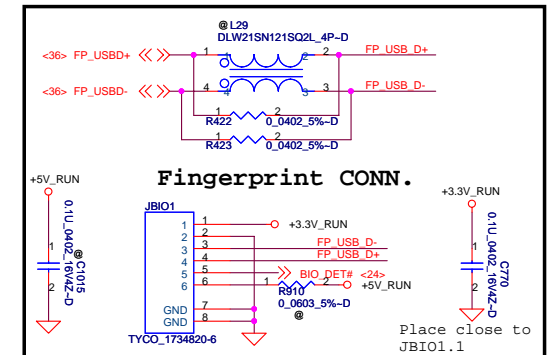


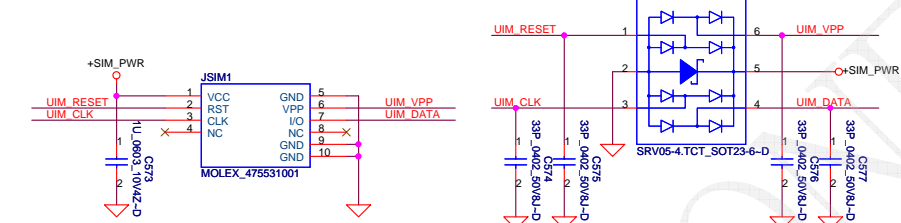
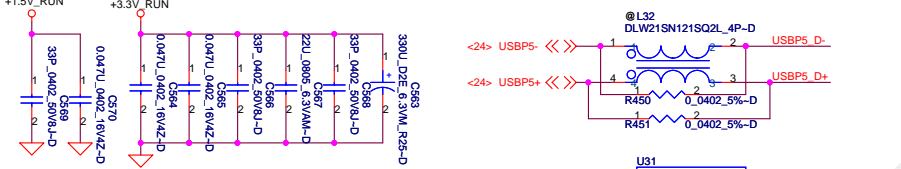
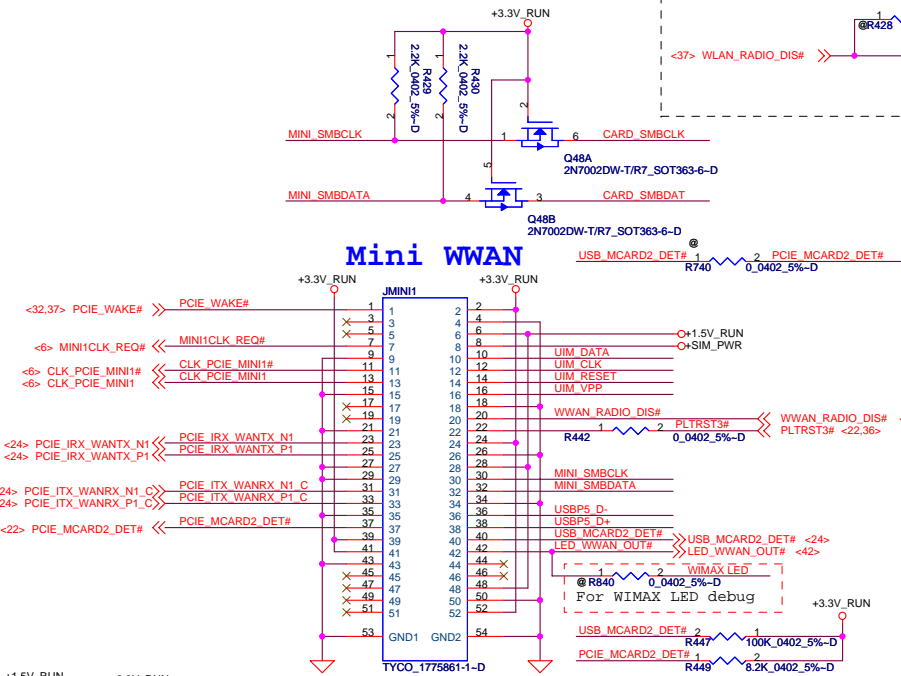




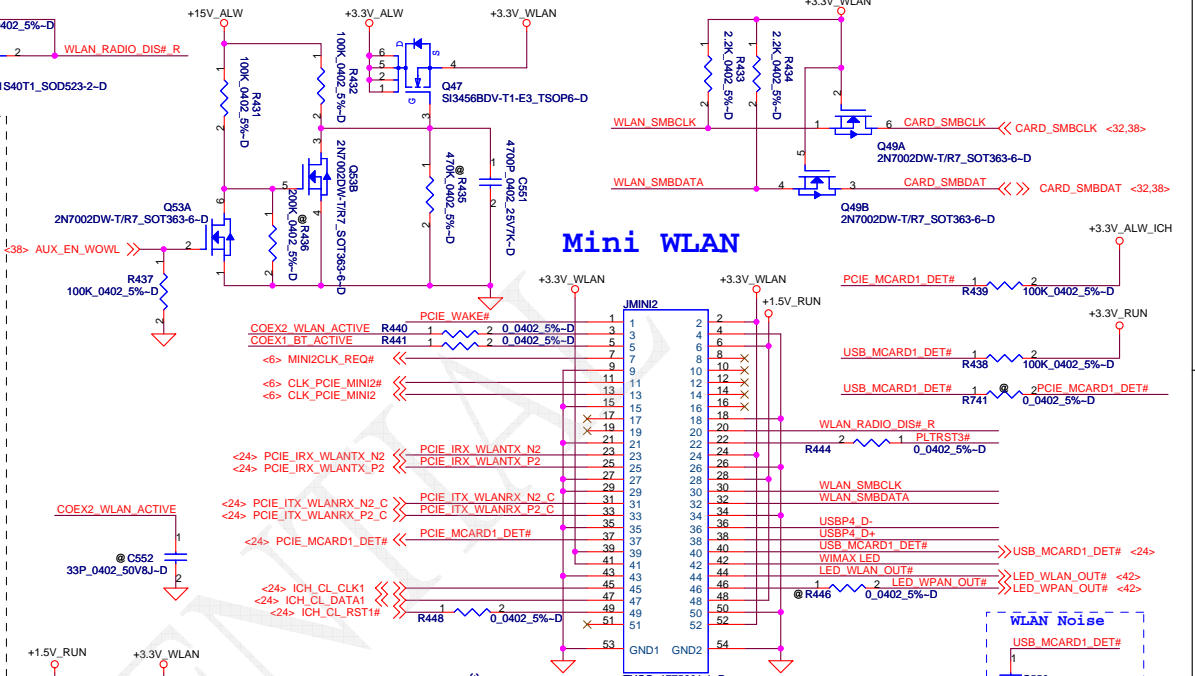


USB PORT#	DESTINATION
0	JUSB1 (Ext Right Side Top)
1	JUSB1 (Ext Right Side Bottom)
2	JESA1 (Ext Left Side Bottom)
3	JESA1 (Ext Left Side TOP)
4	WLAN
5	WWAN
6	WPAN
7	Express card
8	DOCKING
9	DOCKING
10	USH->BIO
11	Camera

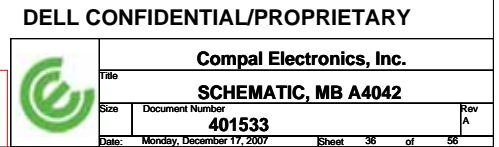




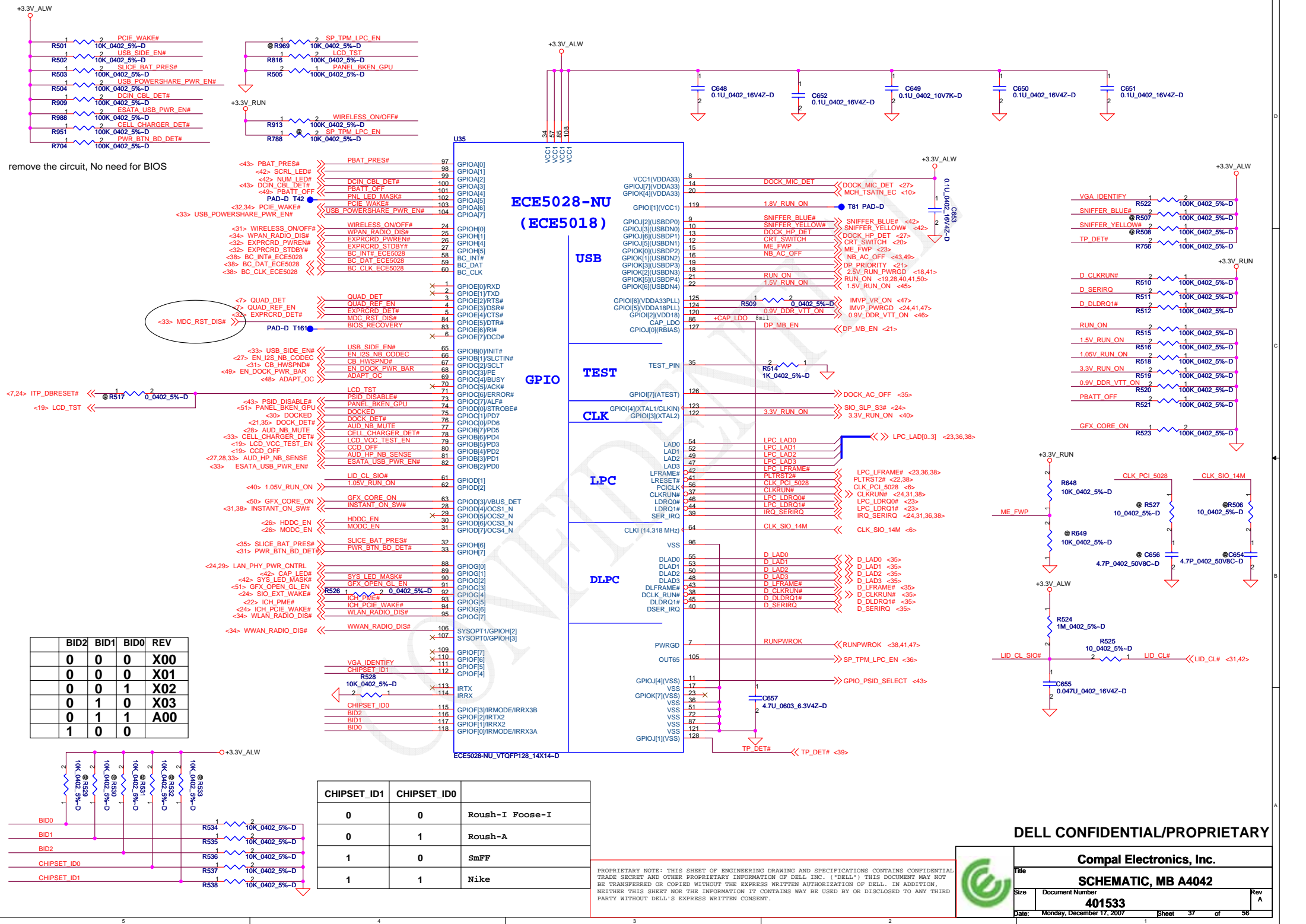
PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+-9%	1000	750	
+3.3Vaux	+-9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+-5%	500	375	NA











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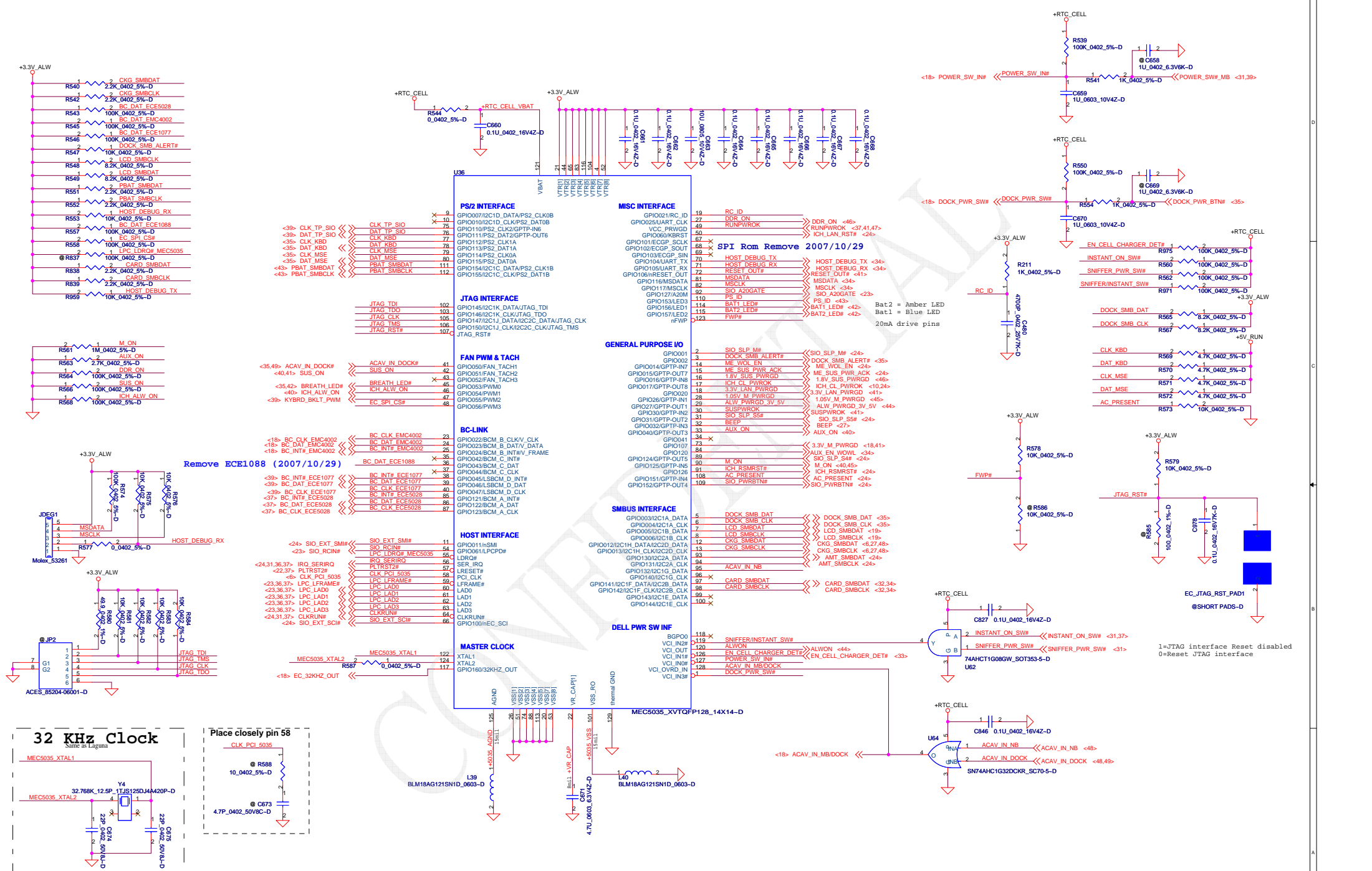
Compal Electronics, Inc.			
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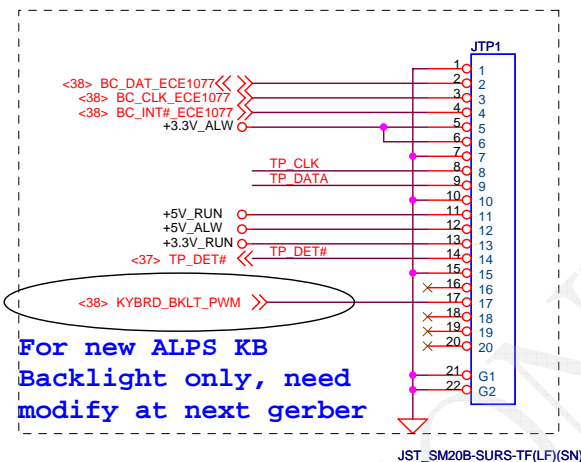
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CHIPSET_ID1	CHIPSET_ID0	
0	0	Roush-I Foose-I
0	1	Roush-A
1	0	SmFF
1	1	Nike

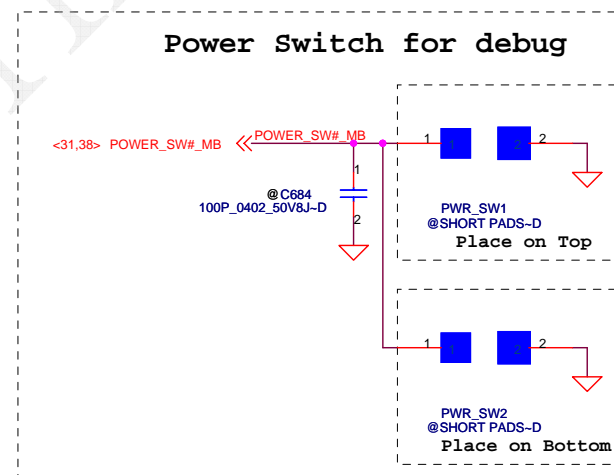
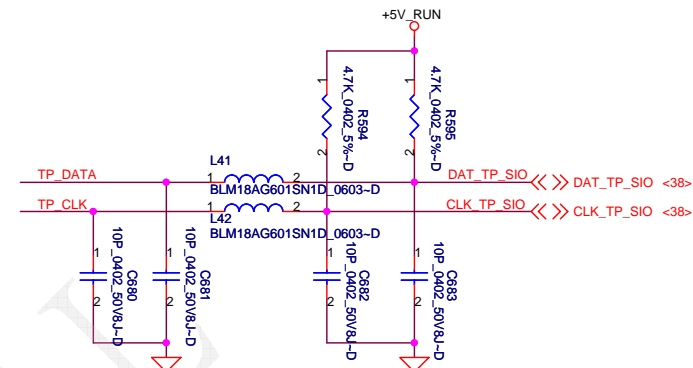
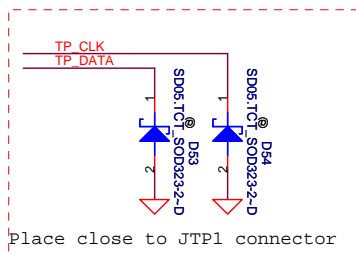
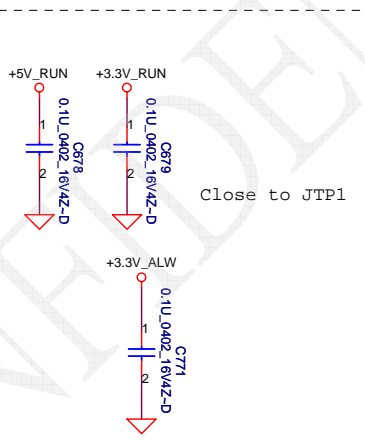
BID2	BID1	BID0	REV
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0	0	0	X01
0	0	1	X02
0	1	0	X03
0	1	1	A00
1	0	0	







JST\_SM20B-SURS-TF(LF)(SN)



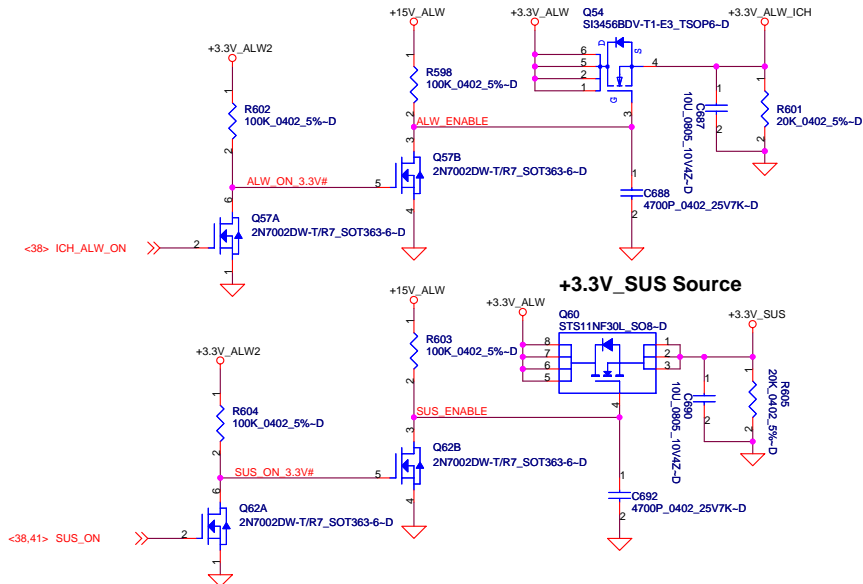
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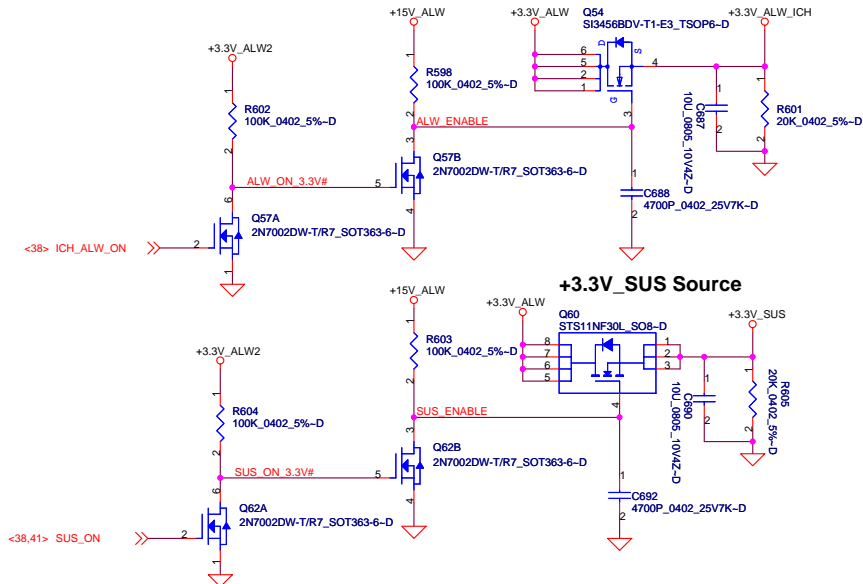
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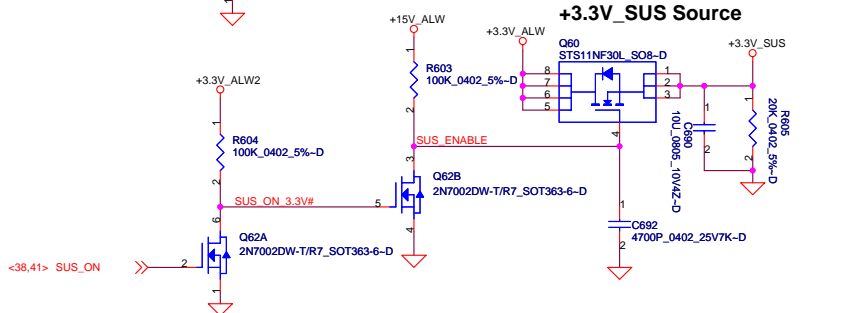
## DC/DC Interface



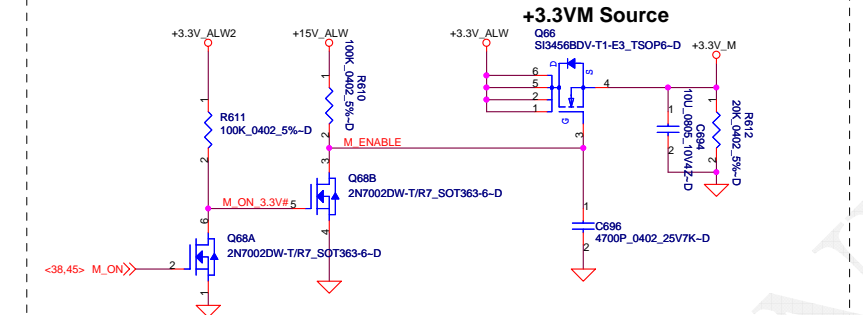
### +3.3V\_ALW\_ICH Source



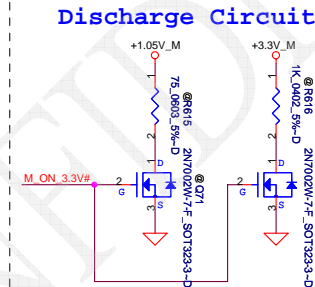
### +3.3V\_SUS Source



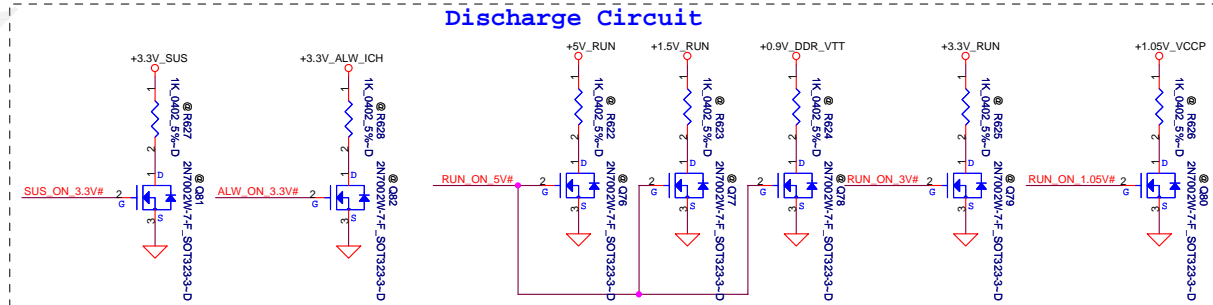
### +3.3VM Source



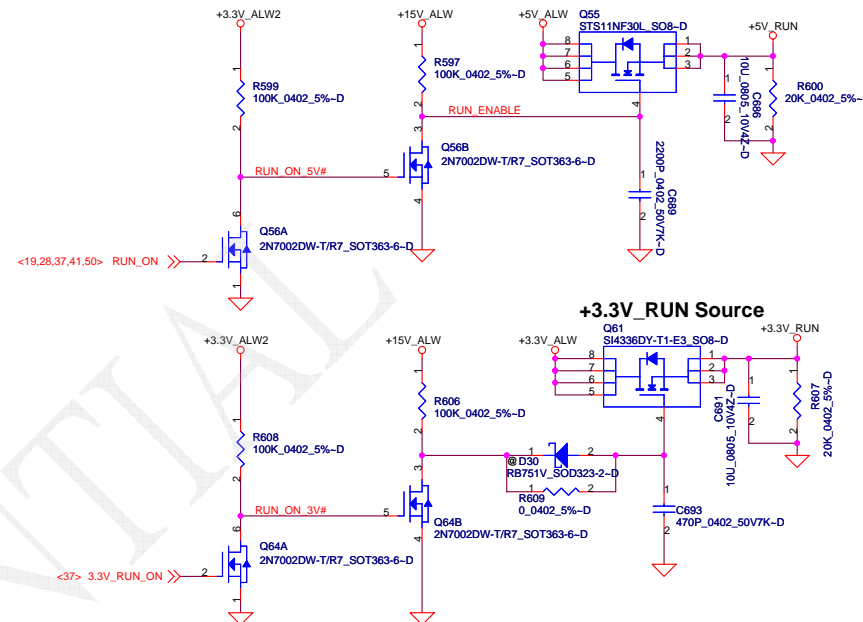
### Discharge Circuit



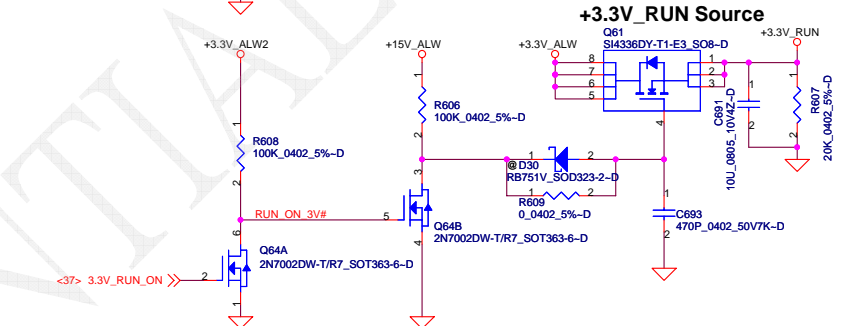
### Discharge Circuit



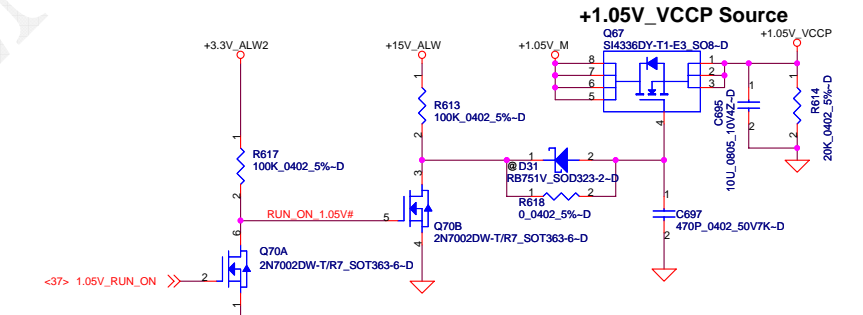
### +5V<sub>RUN</sub> Source



### +3.3V\_RUN Source



### +1.05V\_VCCP Source



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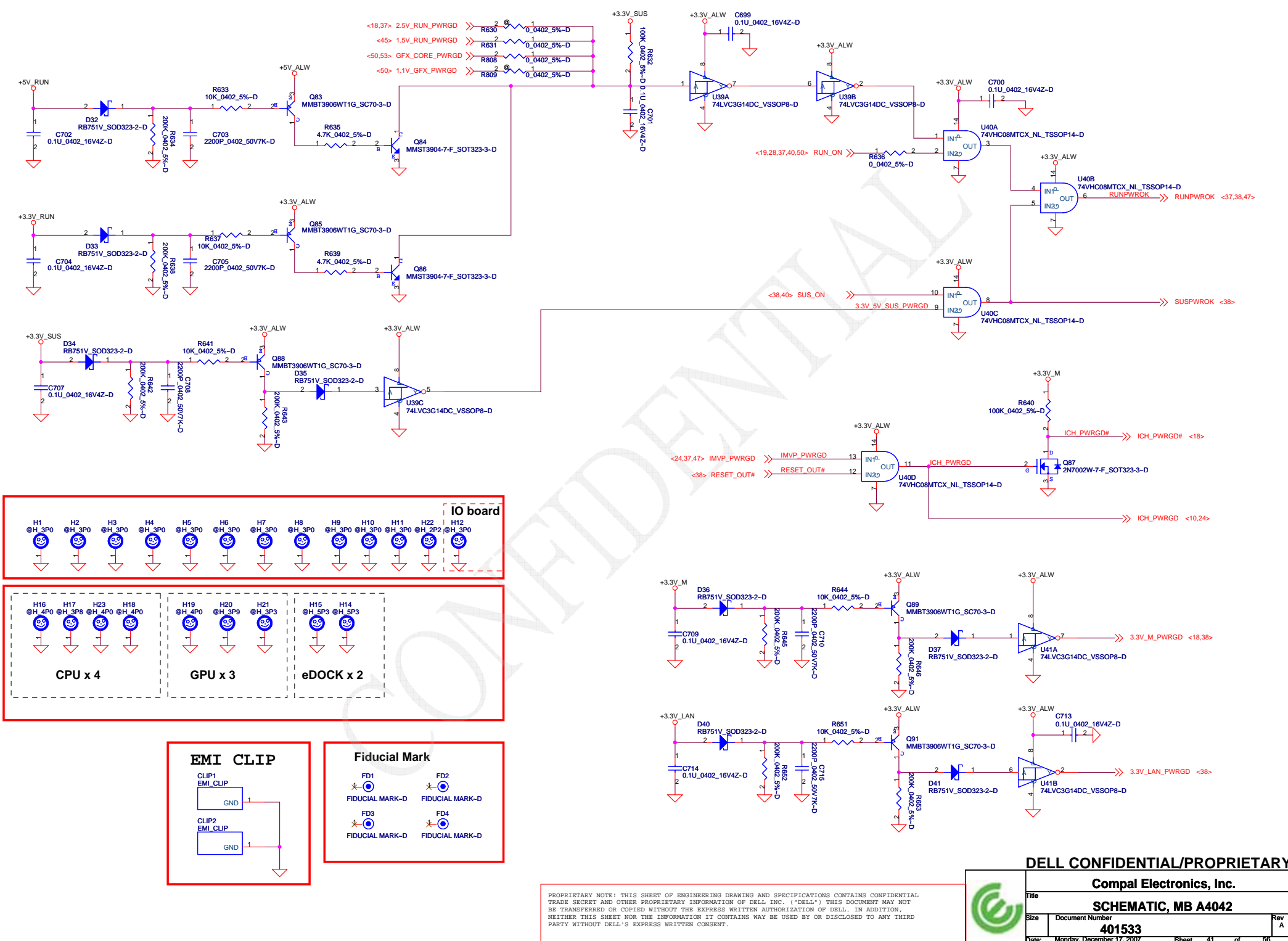
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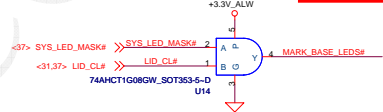
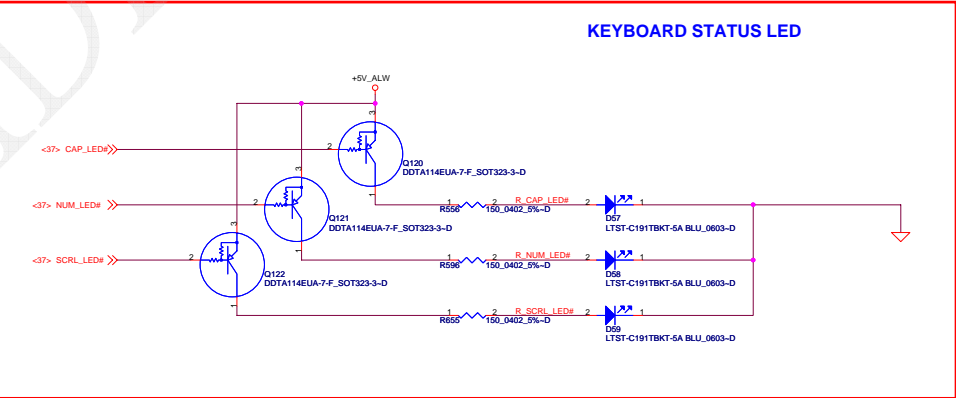
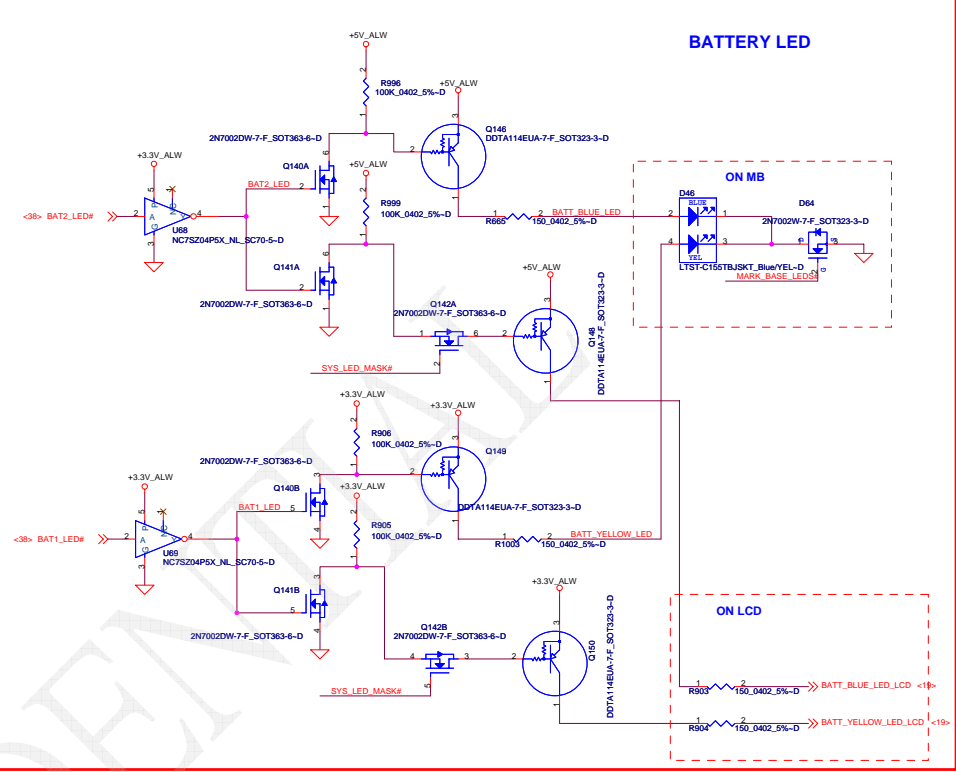
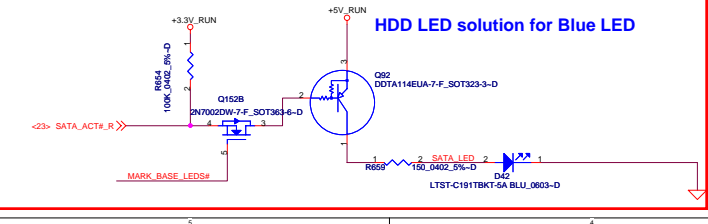
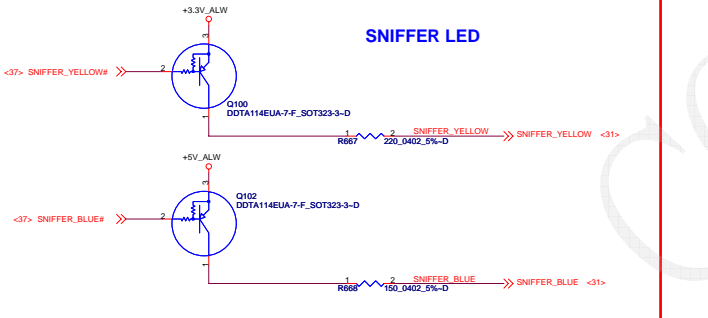
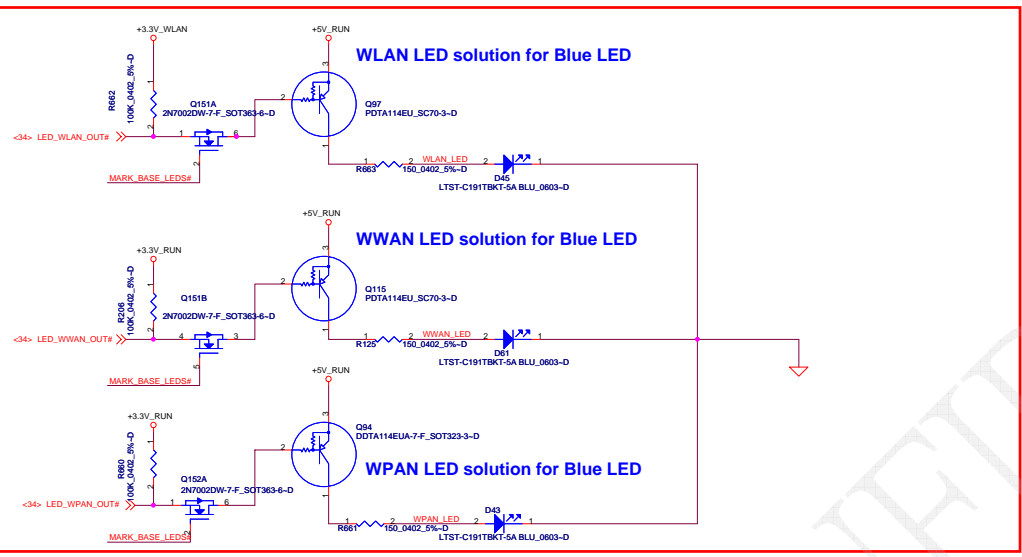
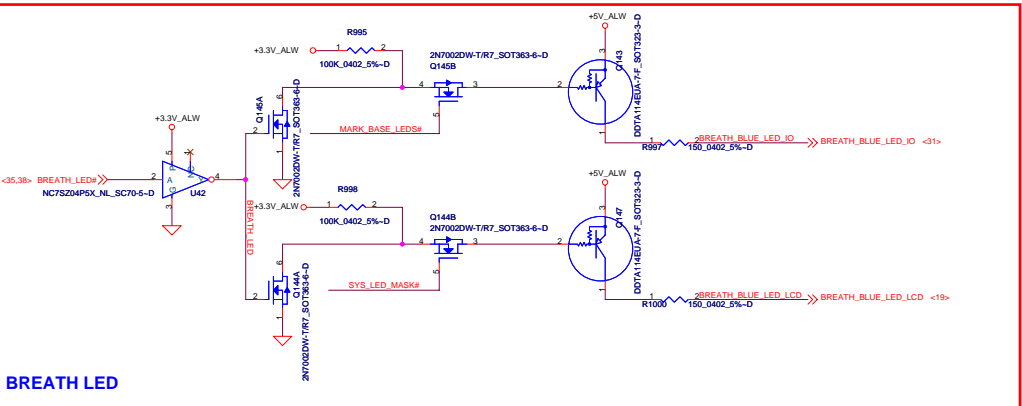
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BIOS GPIO Table for LED Control

	SYS_LED_MASK#	LID_CL#
MARK ALL LED (SNIFFER FUNCTION)	Low	X
MARK BASE MB LEDs (Lid Closed)	High	Low
Do Not Mark LEDs (Lid Opened)	High	High

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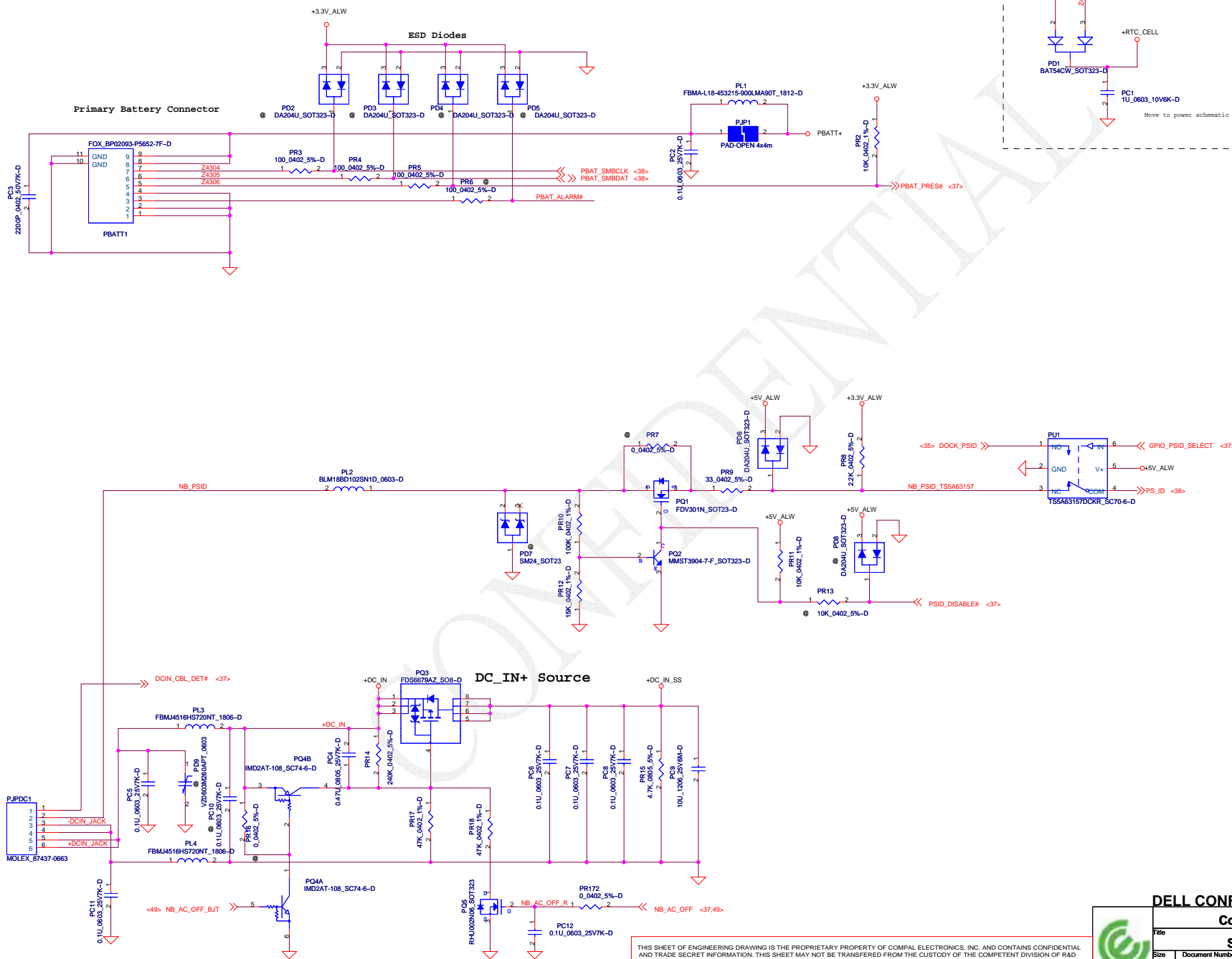
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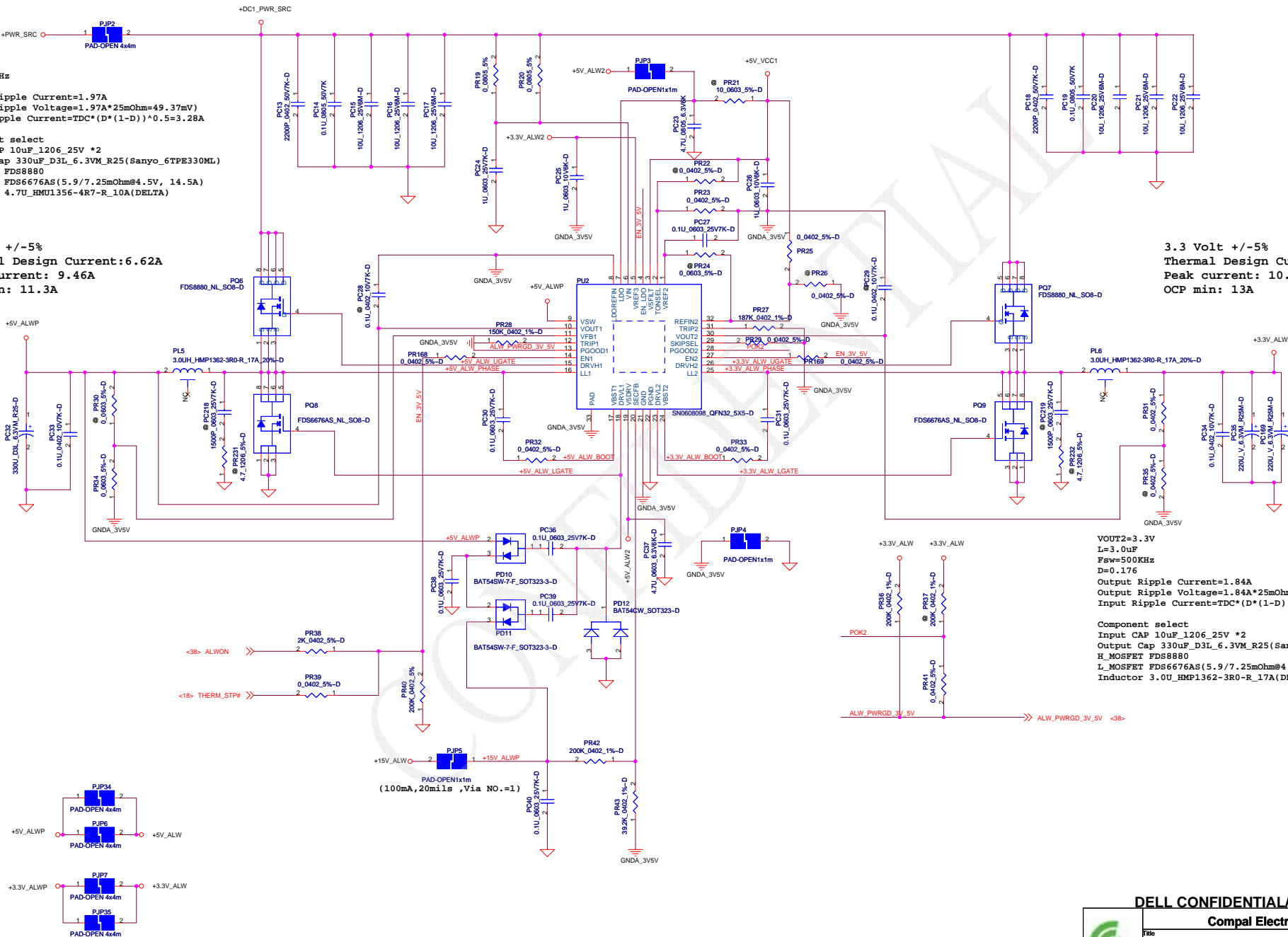
# +3.3V\_ALWP/ +5V\_ALWP/ +5V\_ALW2 / +15V\_ALWP

VOUT1=5V  
L=4.7uF  
Fsw=400KHz  
D=0.265  
Output Ripple Current=1.97A  
Output Ripple Voltage=1.97A\*25mOhm=49.37mV  
Input Ripple Current=TDC\*(D\*(1-D))^0.5=3.28A

Component select  
Input CAP 10uF\_1206\_25V \*2  
Output Cap 330uF\_D3L\_6.3VM\_R25(Sanyo\_6TPE330ML)  
H\_MOSFET FDS8880  
L\_MOSFET FDS6676AS(5.9/7.25mOhm@4.5V, 14.5A)  
Inductor 4.7U\_HMU1356-4R7-R\_10A(DELTA)

5 Volt +/-5%  
Thermal Design Current:6.62A  
Peak current: 9.46A  
OCP min: 11.3A

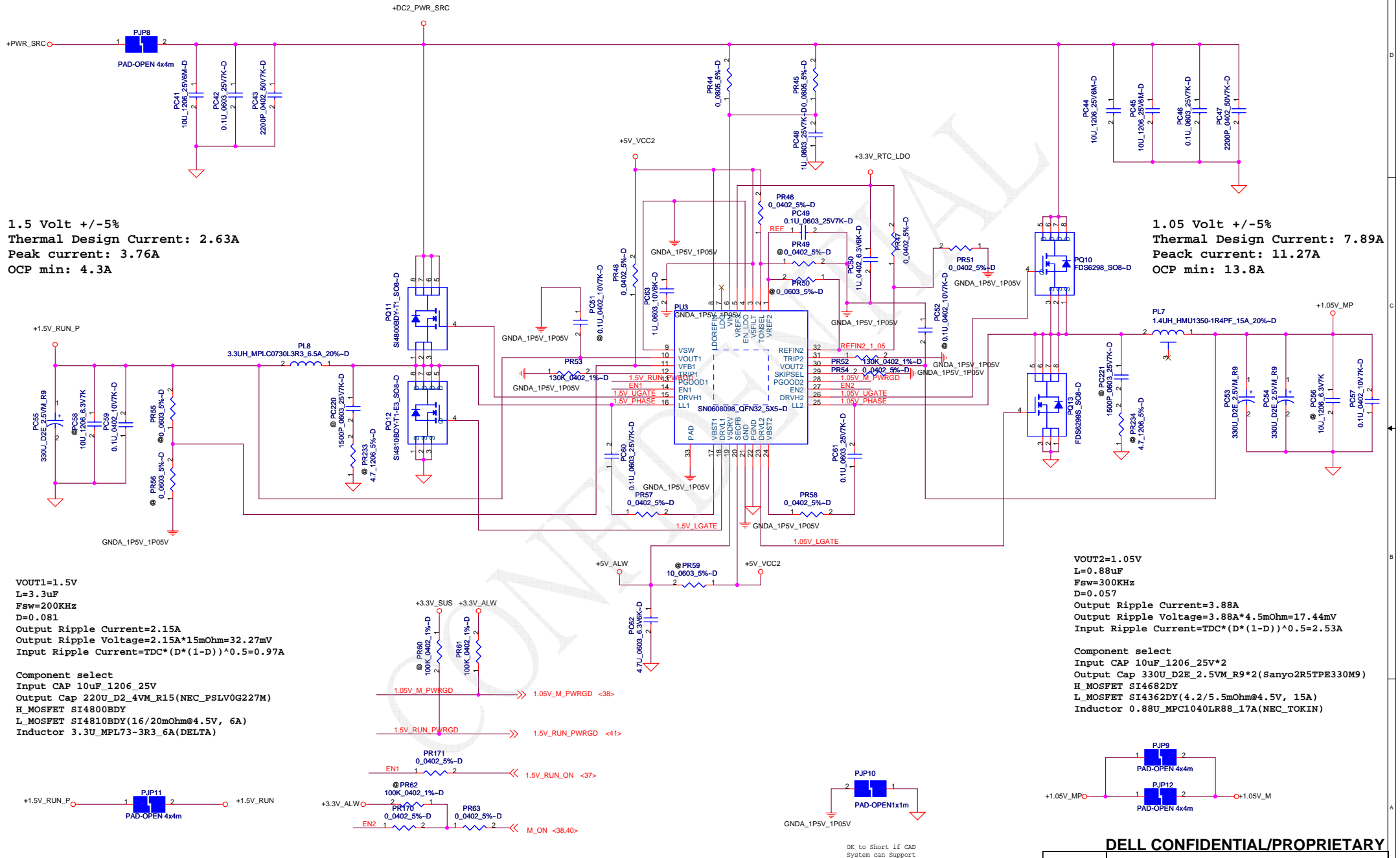
3.3 Volt +/-5%  
Thermal Design Current: 7.39A  
Peak current: 10.56A  
OCP min: 13A



+1.5V\_RUN / +1.05V\_M/ +3.3V\_RTC\_LDO

1.5 Volt +/-5%  
Thermal Design Current: 2.63A  
Peak current: 3.76A  
OCP min: 4.3A

1.05 Volt +/-5%  
Thermal Design Current: 7.89A  
Peak current: 11.27A  
OCP min: 13.8A



VOUT2=1.05V  
L=0.88uF  
Fsw=300KHz  
D=0.057  
Output Ripple Current=3.88A  
Output Ripple Voltage=3.88A\*4.5mOhm=17.44mV  
Input Ripple Current=TDC\*(D\*(1-D))^0.5=2.53A

Component select  
Input CAP 10uF\_1206\_25V  
Output Cap 330U\_D2E\_4VM\_R15(NEC\_PSLV0G227M)  
H\_MOSFET SI4800BDY  
L\_MOSFET SI4810BDY(16/20mOhm@4.5V, 6A)  
Inductor 3.3U\_MPL73-3R3\_6A(DELTA)

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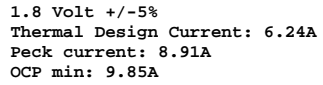
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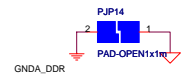
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## DDR2 Termination



Design current 0.7A for +0.9V\_DDR\_VTTP  
Peak current 1A for +0.9V\_DDR\_VTTP

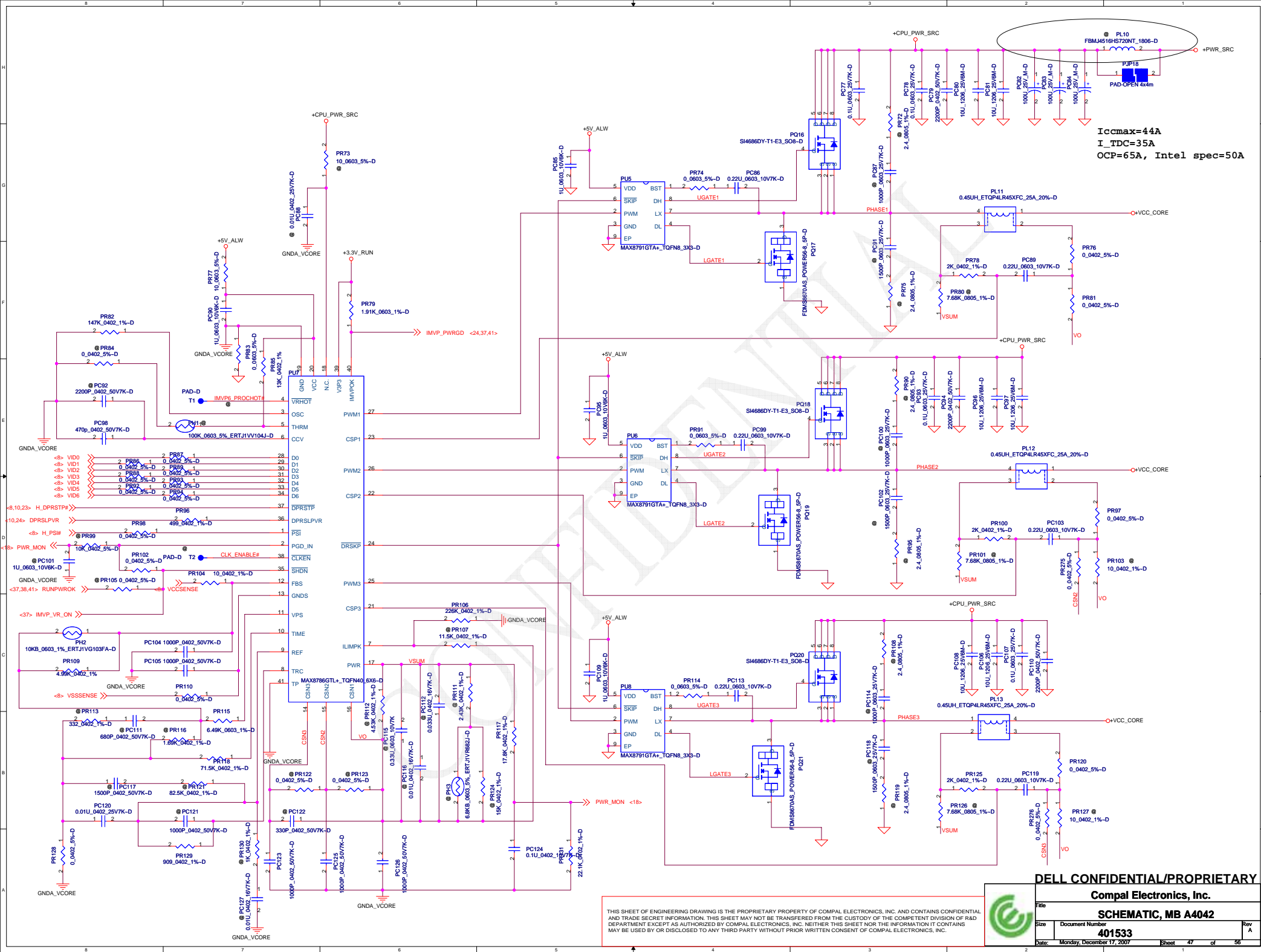


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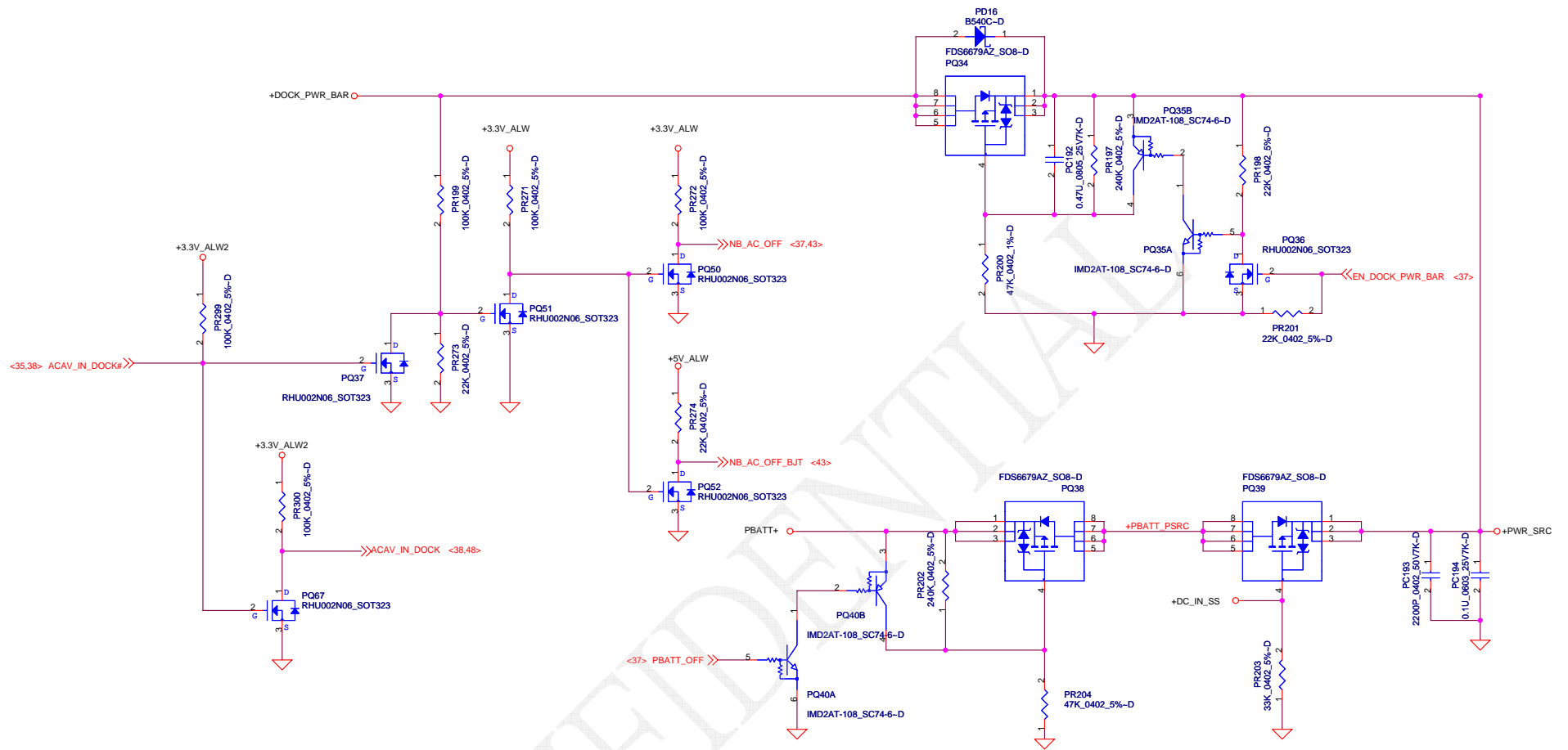
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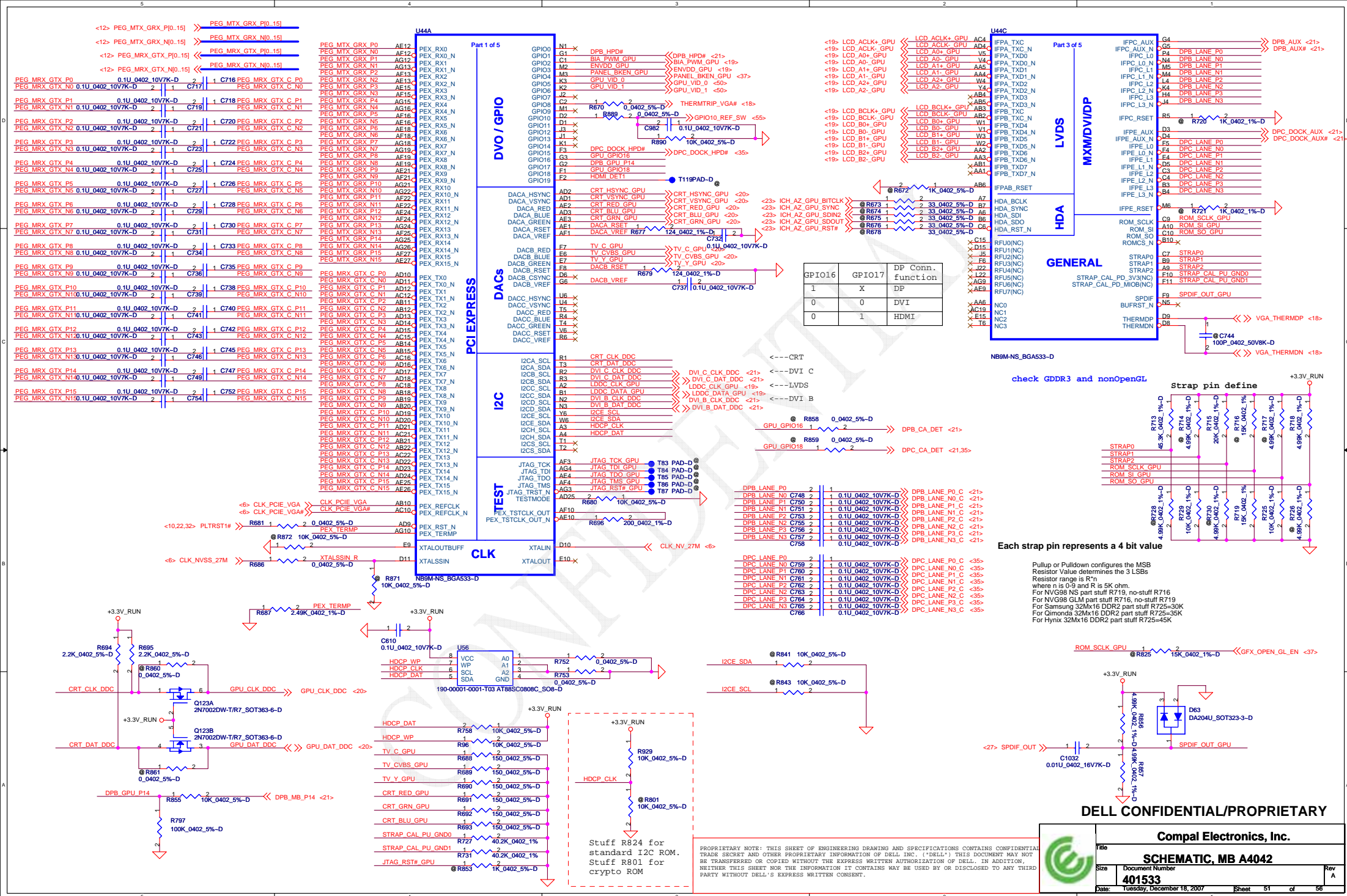
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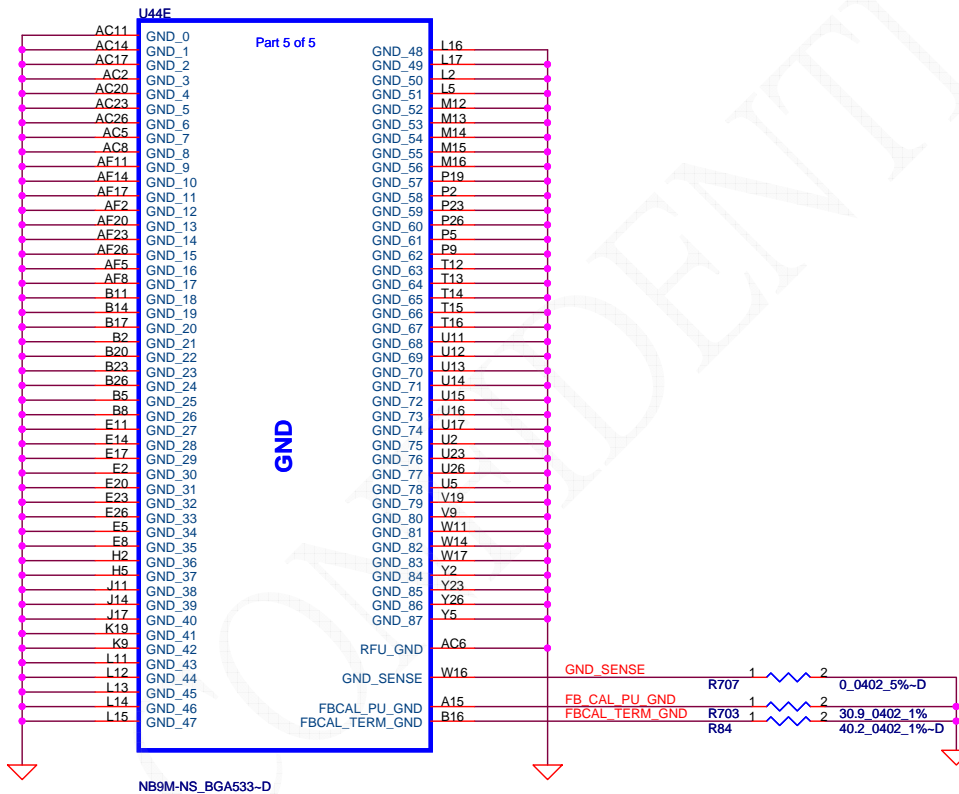












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## 32Mx32 GDDR3

## 32Mx32 GDDR3

FBAD[0..63] <<> FBAD[0..63] <52,56>  
 DQSA\_WP[0..7] <<> DQSA\_WP[0..7] <52,56>  
 DQSA\_RN[0..7] <<> DQSA\_RN[0..7] <52,56>  
 DQMA#[0..7] <<> DQMA#[0..7] <52,56>  
 FBA\_CMD[0..27] >>> FBA\_CMD[0..27] <52,56>

243 ohm for NB8P  
 475 ohm for NB9X  
 Place close to U57

243 ohm for NB8P  
 475 ohm for NB9X  
 Place close to U58

## Mirror U58

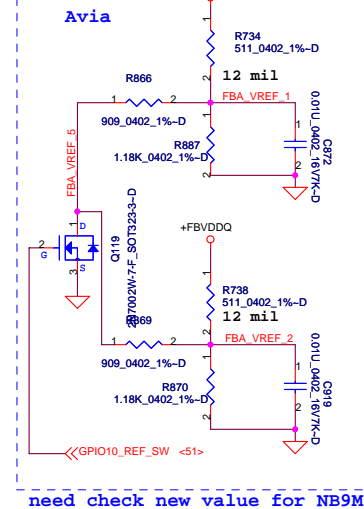
RAS# --> BA2  
 CAS# --> CS0#  
 WE# --> CKE  
 CS0# --> CAS#  
 A0 --> A4  
 A1 --> A5  
 A2 --> A6  
 A3 --> A9  
 A4 --> A0  
 A5 --> A1  
 A6 --> A2  
 A7 --> A11  
 A8 --> A10  
 A9 --> A3  
 A10 --> A8  
 A11 --> A7  
 A12 --> WE#  
 BA0 --> BA1  
 BA1 --> BA0  
 BA2 --> RAS#  
 NC/CS1# --> NV/CS1#

## U58 is Mirror

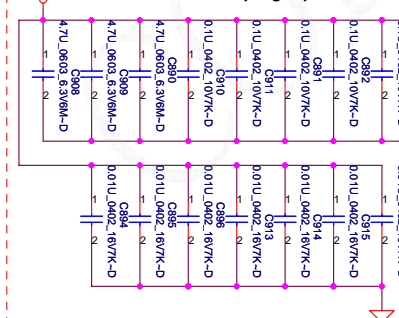
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 FBA\_VREF\_2 >>> FBA\_VREF\_2 <56>

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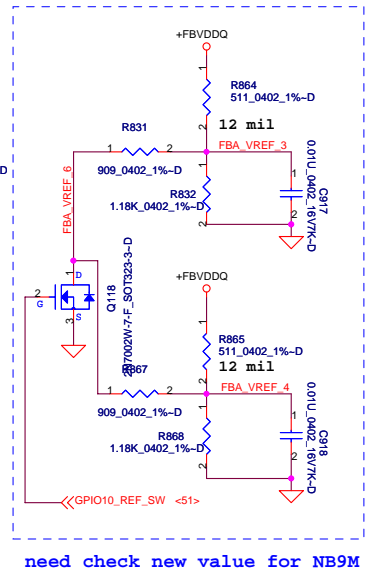
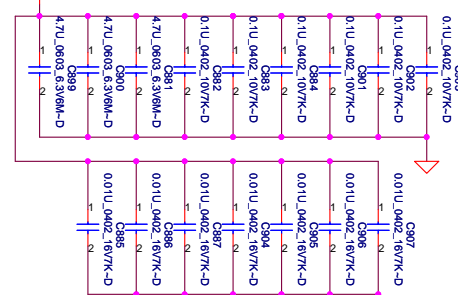
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 FBA\_VREF\_4 >>> FBA\_VREF\_4 <56>



## Place below decoupling caps close U57



## Place below decoupling caps close U58



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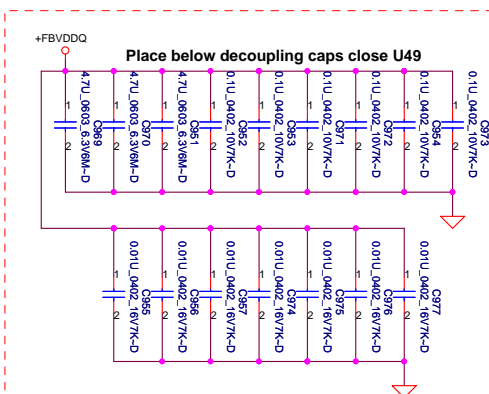
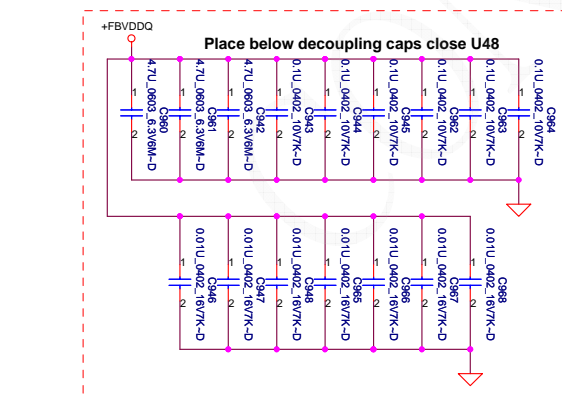
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