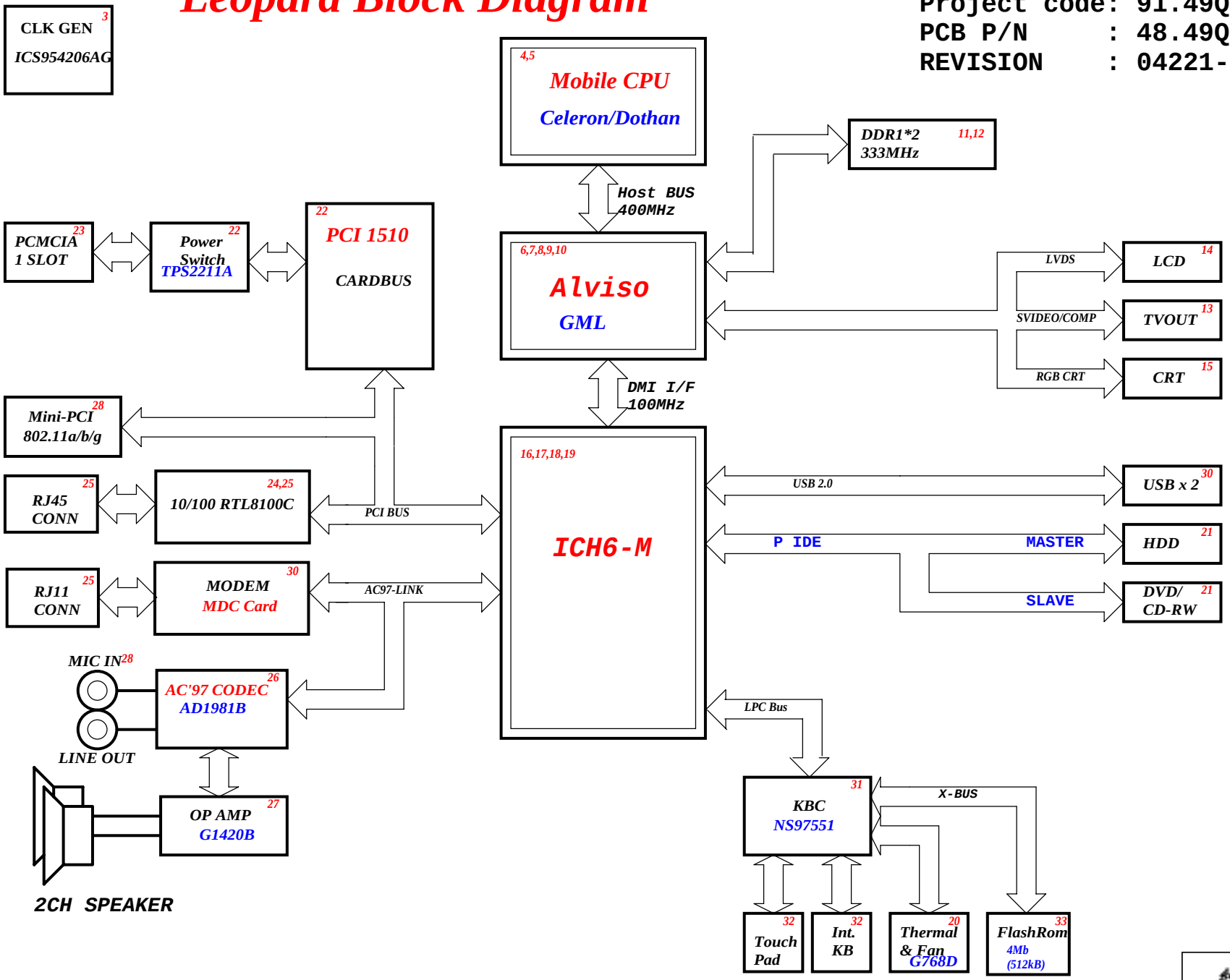
Leopard Block Diagram

Project code: 91.49Q01.001
PCB P/N : 48.49Q01.001
REVISION : 04221-2 DF



SYSTEM DC/DC 37 MAX1999	
INPUTS	OUTPUTS
DCBATOUT	5V_S3 3V_S5

SYSTEM DC/DC 38,39 TPS5130	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D2V_S0 2D5V_S3

MAXIM CHARGER 35 MAX8725	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A 5V 100mA

CPU DC/DC 36 MAX1907	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

PCB LAYER	
L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	VCC
L6:	Signal 4

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram

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ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, EE_CS, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

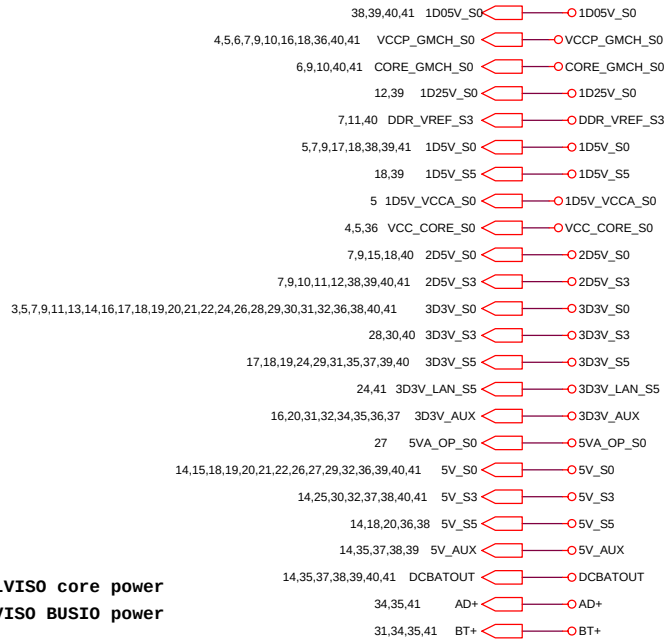
ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

Power name description

5V_S0= 5 Voltage power up on system work(S0 state)
5V_S3= 5 Voltage suspend to RAM(S3 state)
5V_S5= 5 Voltage soft off(S5 state)
3D3V_S0= 3.3 Voltage power up on system work(S0 state)
3D3V_S3= 3.3 Voltage suspend to RAM(S3 state)
3D3V_S5= 3.3 Voltage soft off(S5 state)
LVDDR_2D5V= 2.5 Voltage power up on system work(S0 state)
2D5V_S3= 2.5 Voltage suspend to RAM(S3 state)
2D5V_S0= 2.5 Voltage power up on system work(S0 state)

VCC_CORE_S0= CPU VID Voltage power up on system work(S0 state)
1D5V_VCCA_S0= 1.5 Voltage power up on system work(S0 state)
1D5V_S0= 1.5 Voltage power up on system work(S0 state)
1D5V_S5= 1.5 Voltage soft off(S5 state)
DDR_VREF_S3= 1.25 Voltage suspend to RAM(S3 state)
1D25V_S0= 1.25 Voltage power up on system work(S0 state)
1D2_VGA_S0= 1.2 Voltage power up on system work(S0 state) for VGA
1D05V_S0= 1.05 Voltage power up on system work(S0 state)
CORE_GMCH_S0= 1.05 Voltage power up on system work(S0 state) for ALVISO core power
VCCP_GMCH_S0= 1.05 Voltage power up on system work(S0 state)for ALVISO BUSIO power



PCI RESOURCE TABLE

DEVICE	IDSEL	PCI IRQ	REQ# / GNT#
Mini-PCI	AD21	P_INTE#	REQ0#/GNT0#
Cardbus Controller TI PCI1510	AD22	(CARBUS)P_INTG#	REQ1#/GNT1#
LAN	AD23	P_INTE#	REQ2#/GNT2#

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Title: *ITP*

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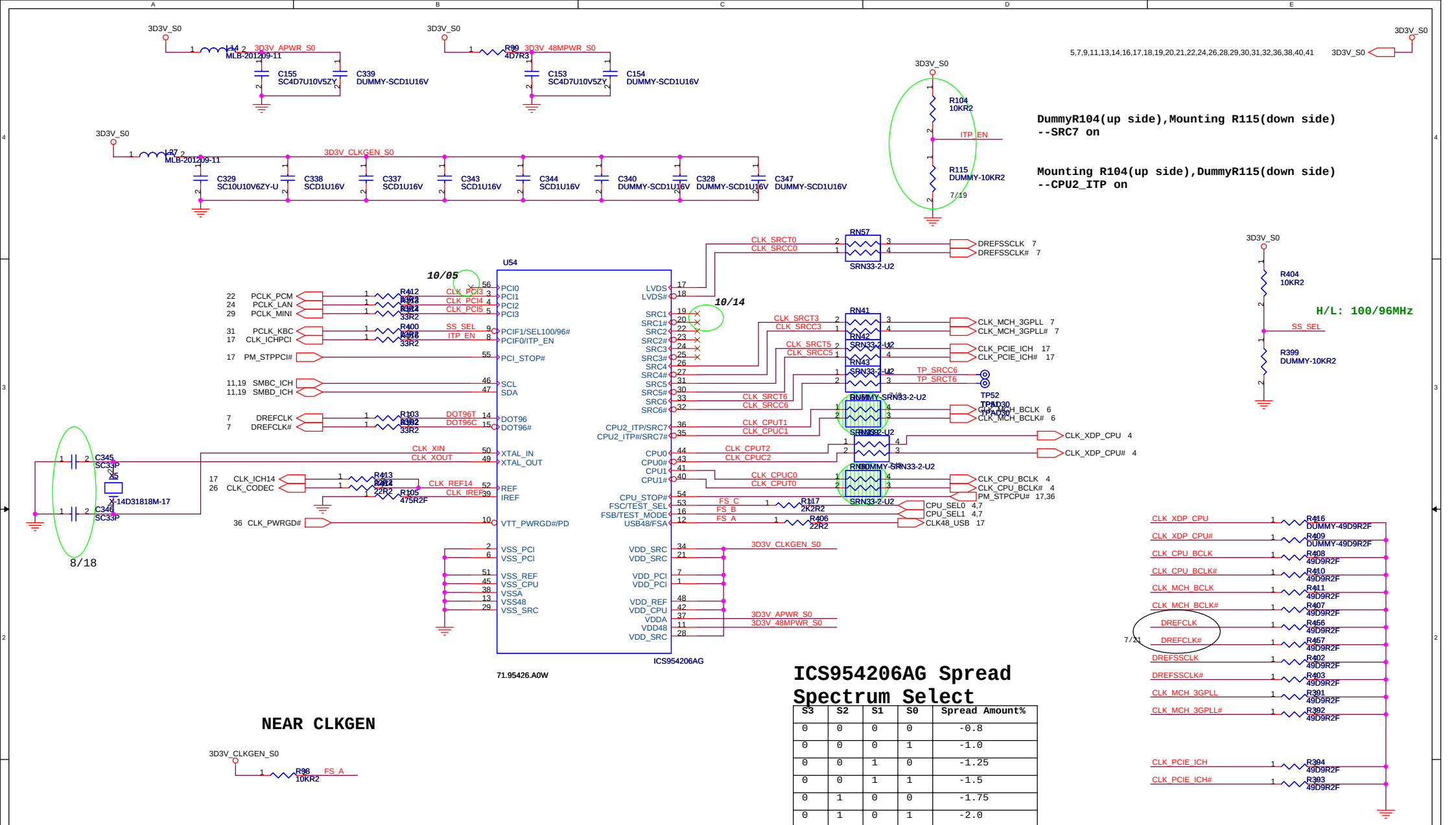
Date: Thursday, December 09, 2004 | Sheet 2 of 41



ICS954206AG Spread Spectrum Select

S3	S2	S1	S0	Spread Amount%
0	0	0	0	-0.8
0	0	0	1	-1.0
0	0	1	0	-1.25
0	0	1	1	-1.5
0	1	0	0	-1.75
0	1	0	1	-2.0
0	1	1	0	-2.5
0	1	1	1	-3.0
1	0	0	0	+/-0.3
1	0	0	1	+/-0.4
1	0	1	0	+/-0.5
1	0	1	1	+/-0.6
1	1	0	0	+/-0.8
1	1	0	1	+/-1.0
1	1	1	0	+/-1.25
1	1	1	1	+/-1.5

FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	Reserved

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Title: Clock Generator (ICS954206AG)

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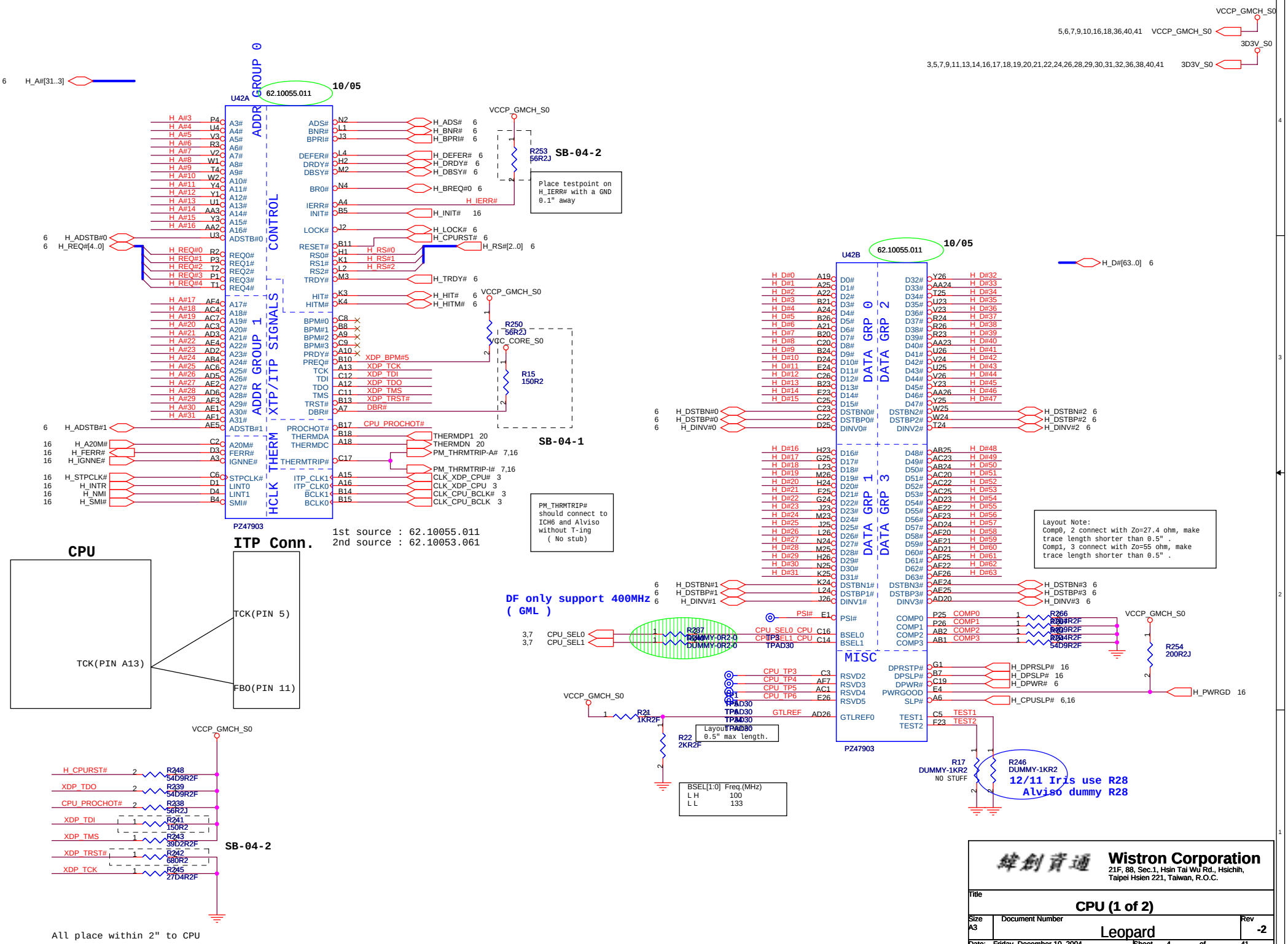
U42A
62.10055.011
10/05
ADDR GROUP 0
ADDR GROUP 1
XTP/ITP SIGNALS
CONTROL
THERM
HCLK
PZ47903
SB-04-2
SB-04-1
Place testpoint on H_IERR# with a GND 0.1" away
PM_THRMTRIP# should connect to ICH6 and Alviso without T-ing (No stub)
ITP Conn.
1st source : 62.10055.011
2nd source : 62.10053.061
CPU
TCK(PIN A13)
TCK(PIN 5)
FBO(PIN 11)
All place within 2" to CPU
U42B
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
DF only support 400MHz (GML)
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
Layout Note: 0.5" max length.
BSEL[1:0] Freq.(MHz)
L H 100
L L 133
12/11 Iris use R28
Alviso dummy R28
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Title
CPU (1 of 2)
Size A3
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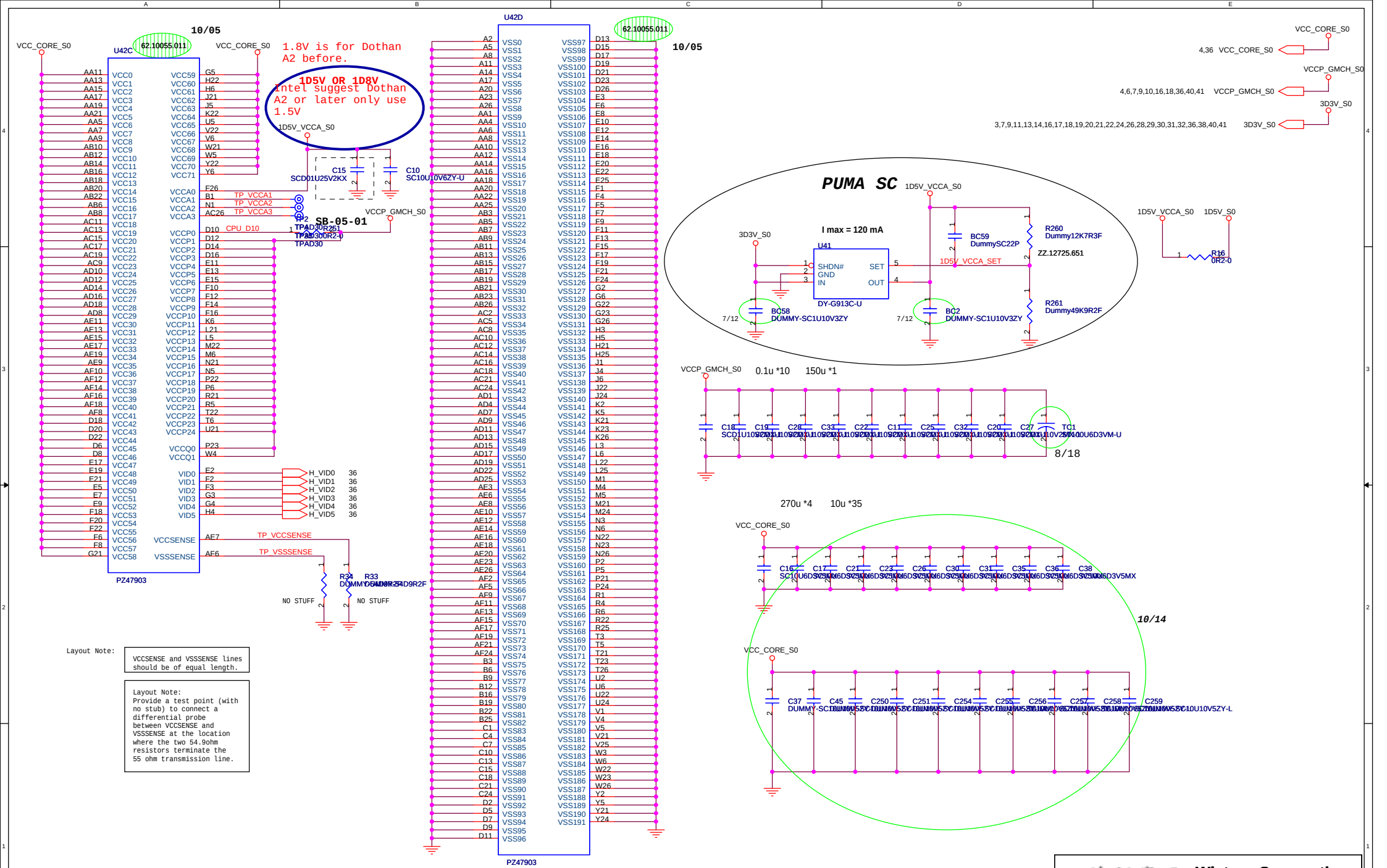

Layout Note:

VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

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Title	CPU (2 of 2)	
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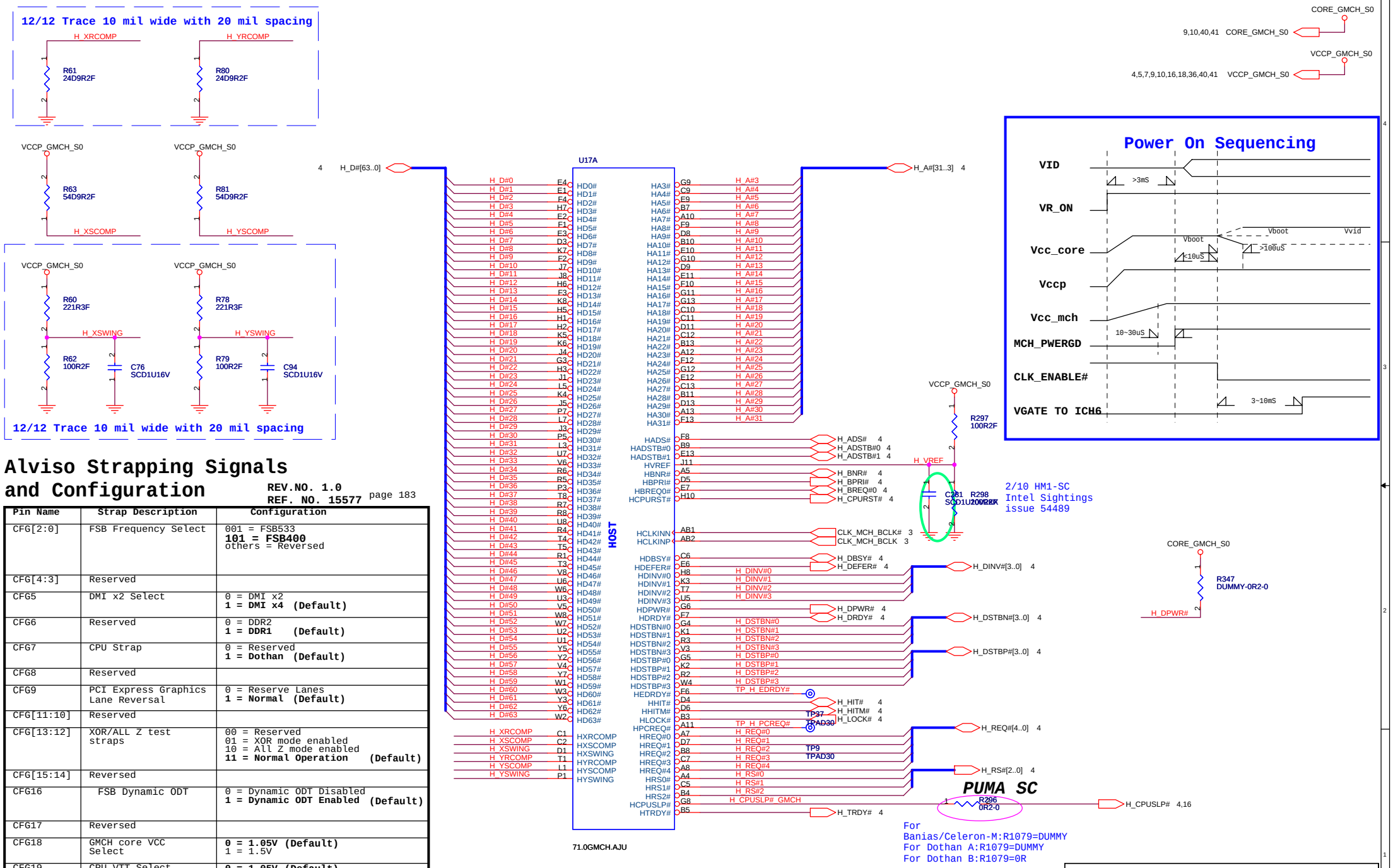

Alviso Strapping Signals and Configuration

REV.NO. 1.0
REF. NO. 15577 page 183

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 **101 = FSB400** others = Reversed
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	Reserved	0 = DDR2 **1 = DDR1 (Default)**
CFG7	CPU Strap	0 = Reserved **1 = Dothan (Default)**
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reserve Lanes **1 = Normal (Default)**
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation (Default)**
CFG[15:14]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG17	Reversed	
CFG18	GMCH core VCC Select	**0 = 1.05V (Default)** 1 = 1.5V
CFG19	CPU VTT Select	**0 = 1.05V (Default)** 1 = 1.2V
CFG20	Reversed	
SDVOCRTL_DATA	SDVO Present	**0 = No SDVO device present(Default)** 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

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Title: GMCH (1 of 5)
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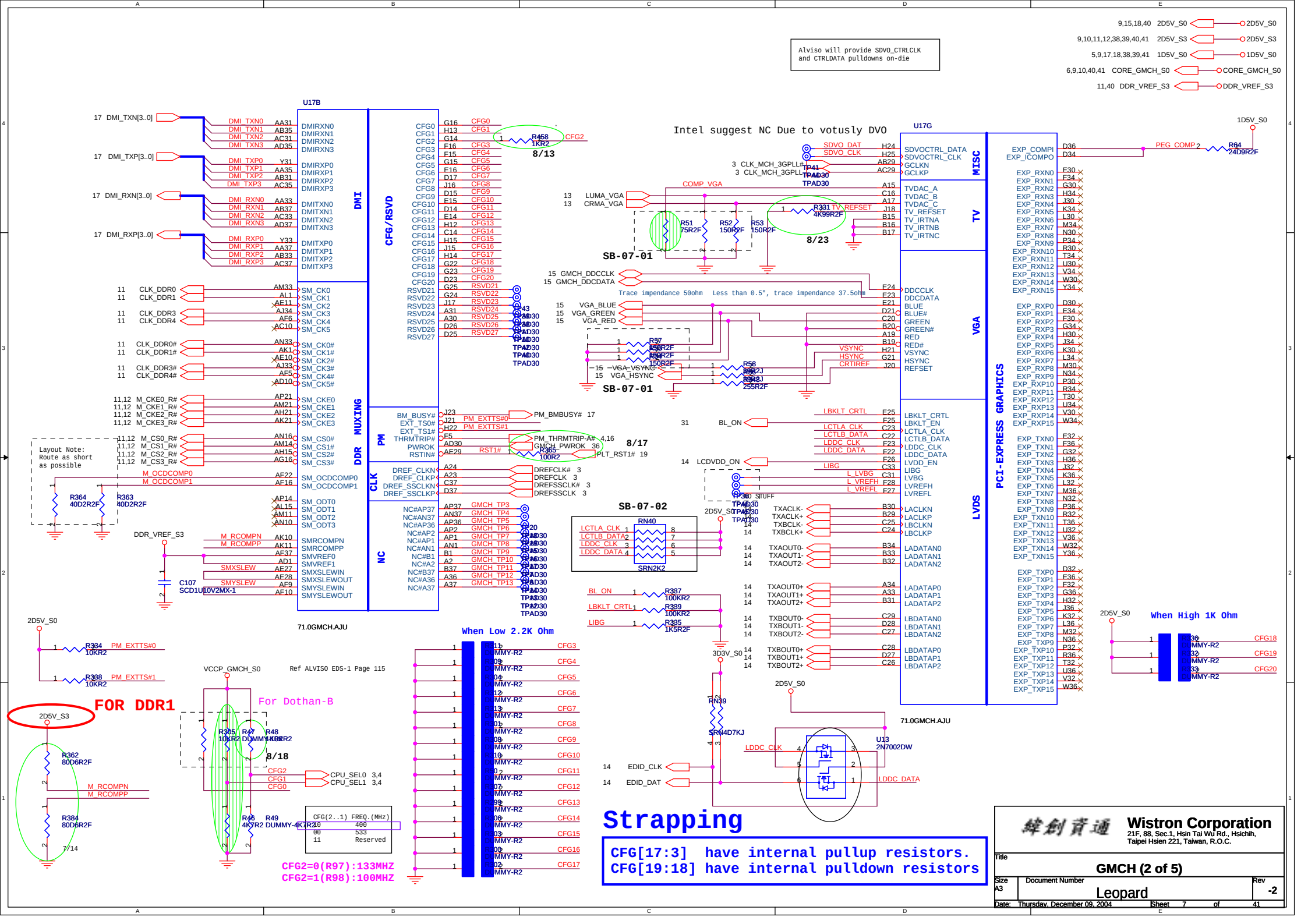
U17B
DMI
CFG/RSVD
DDR MUXING
PM
CLK
NC
71.0GMCH.AJU
U17G
MISC
TV
VGA
LVDS
PCI-EXPRESS GRAPHICS
Intel suggest NC Due to votusly DVO
Alviso will provide SDVO_CTRLCLK and CTRLDATA pulldowns on-die
SB-07-01
SB-07-02
8/13
8/23
8/17
8/18
7/14
Layout Note: Route as short as possible
Trace impendance 50ohm
Less than 0.5", trace impendance 37.5ohm
When Low 2.2K Ohm
When High 1K Ohm
FOR DDR1
For Dothan-B
Ref ALVISO EDS-1 Page 115
CFG2=0(R97):133MHZ
CFG2=1(R98):100MHZ
Strapping
CFG[17:3] have internal pullup resistors.
CFG[19:18] have internal pulldown resistors
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Title
GMCH (2 of 5)
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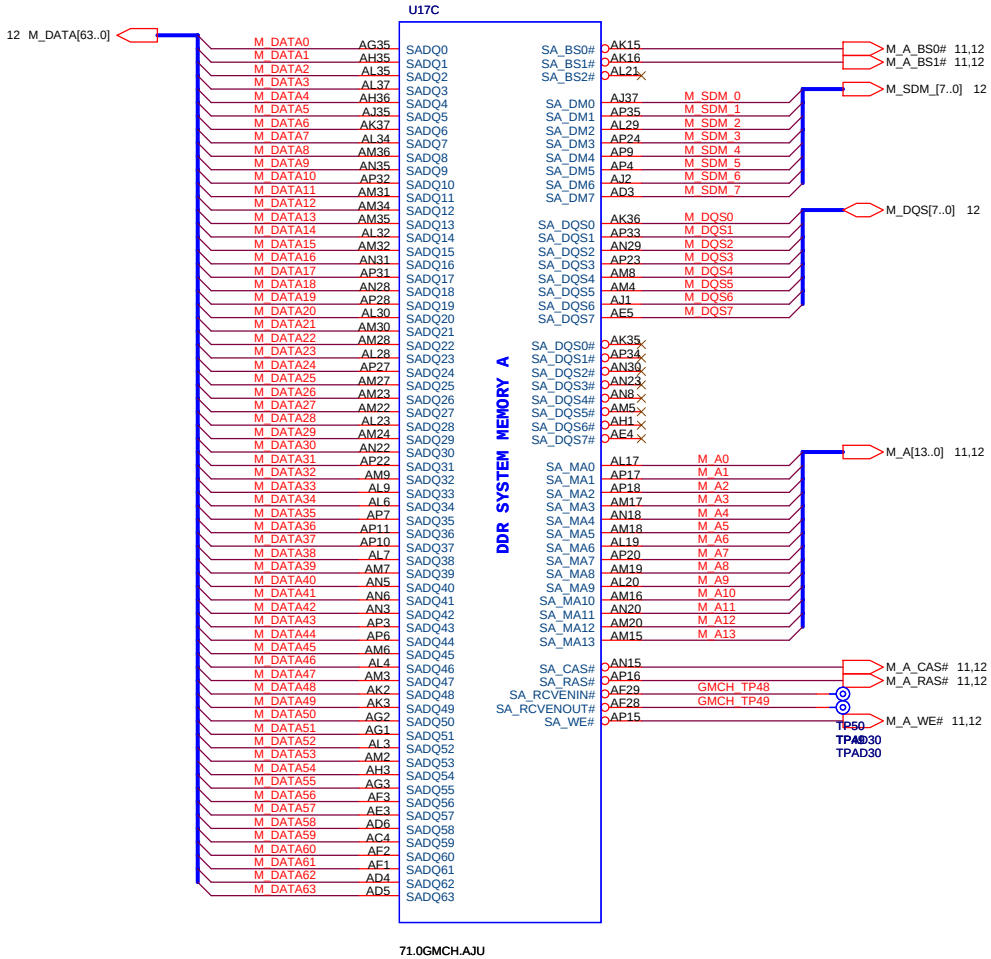
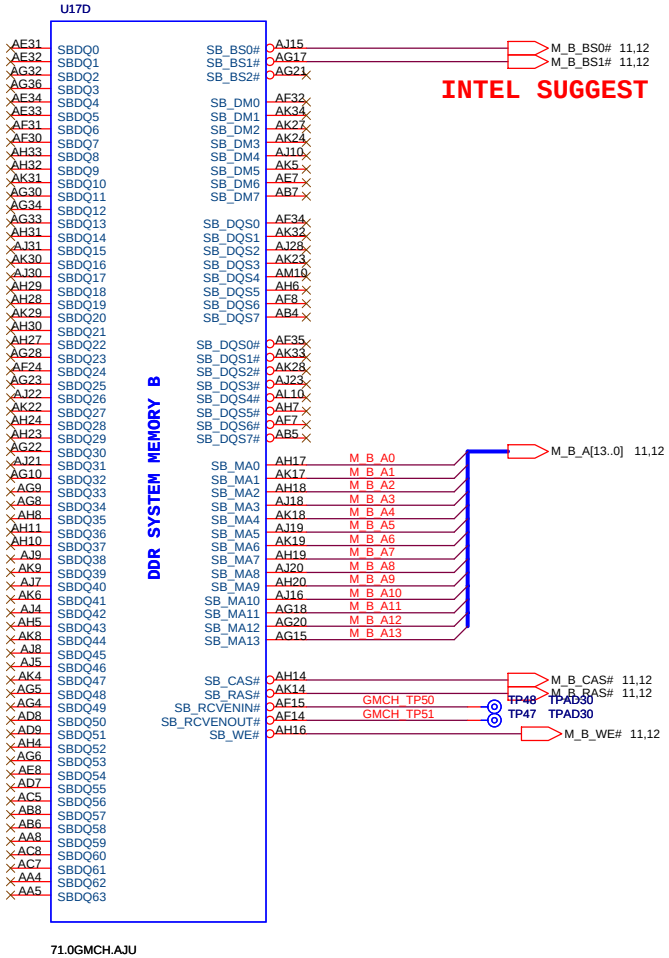
SUPPORT DDR333 ONLY





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Title: GMCH (3 of 5)

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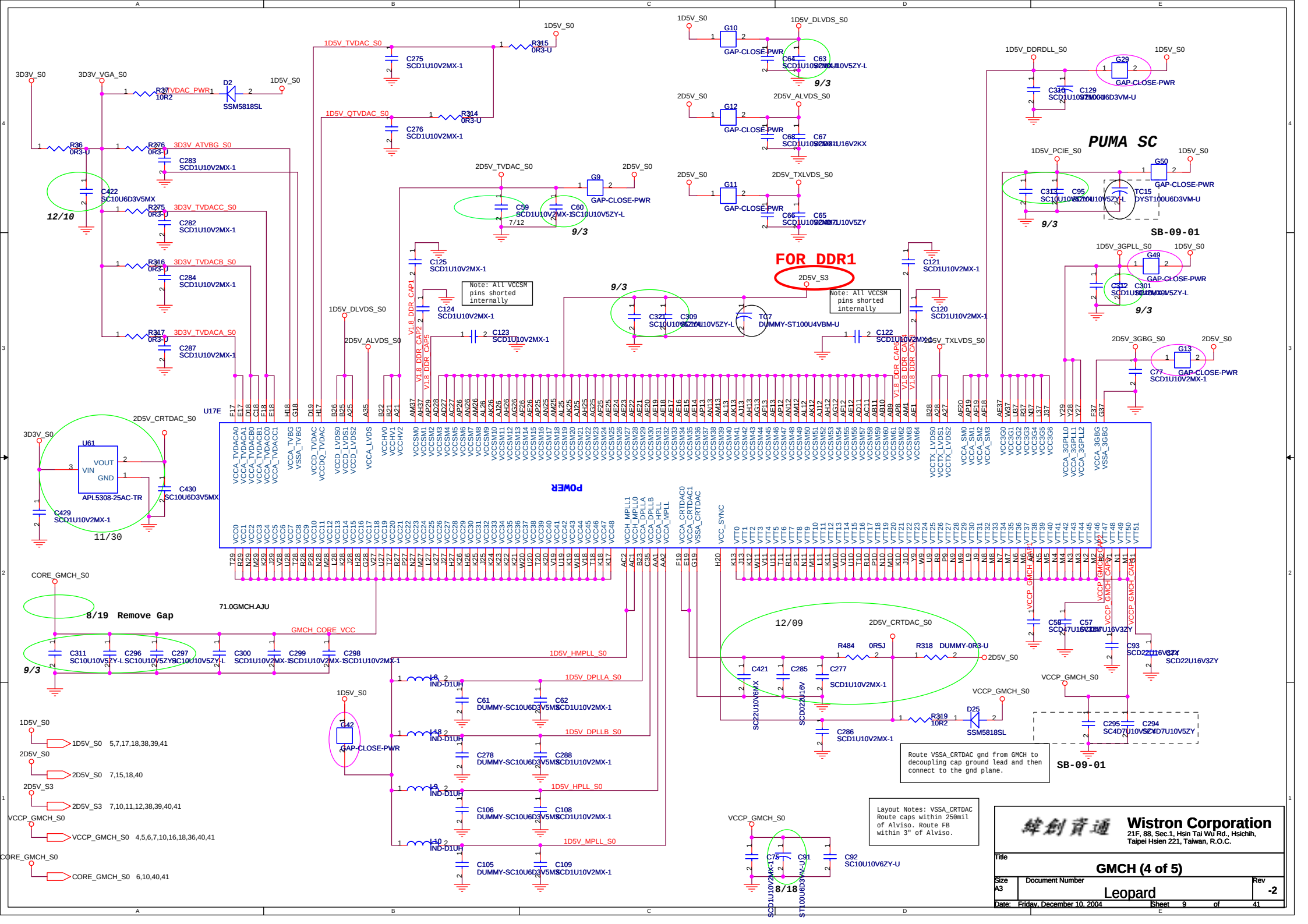

Layout Notes: VSSA_CRTDAC Route caps within 250mil of Alviso. Route FB within 3" of Alviso.

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Title: **GMCH (4 of 5)**

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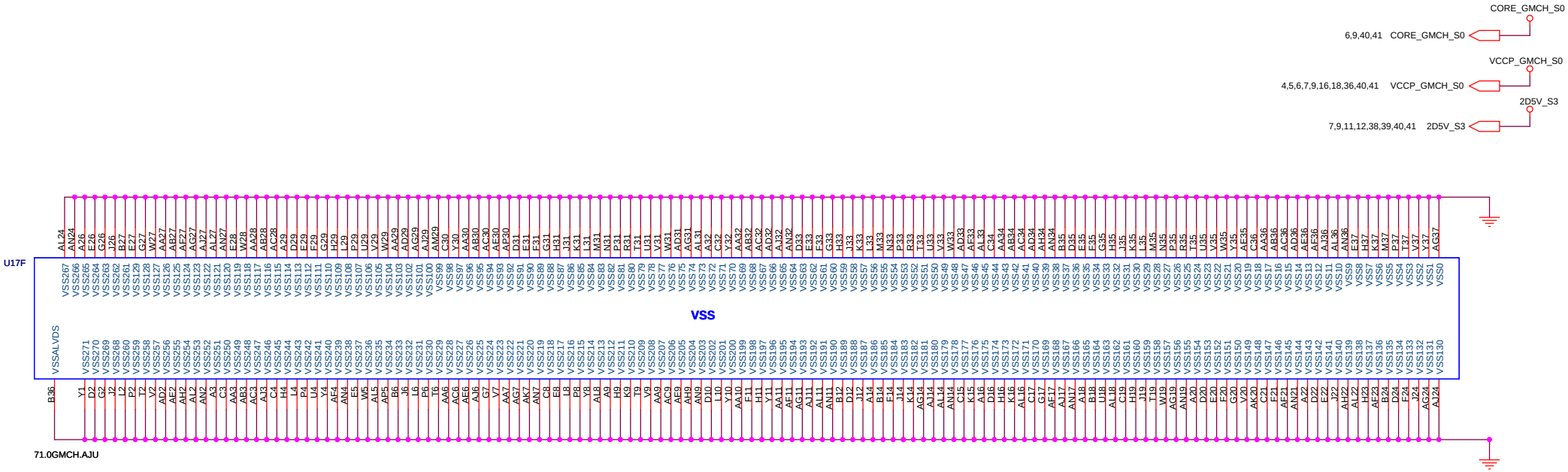

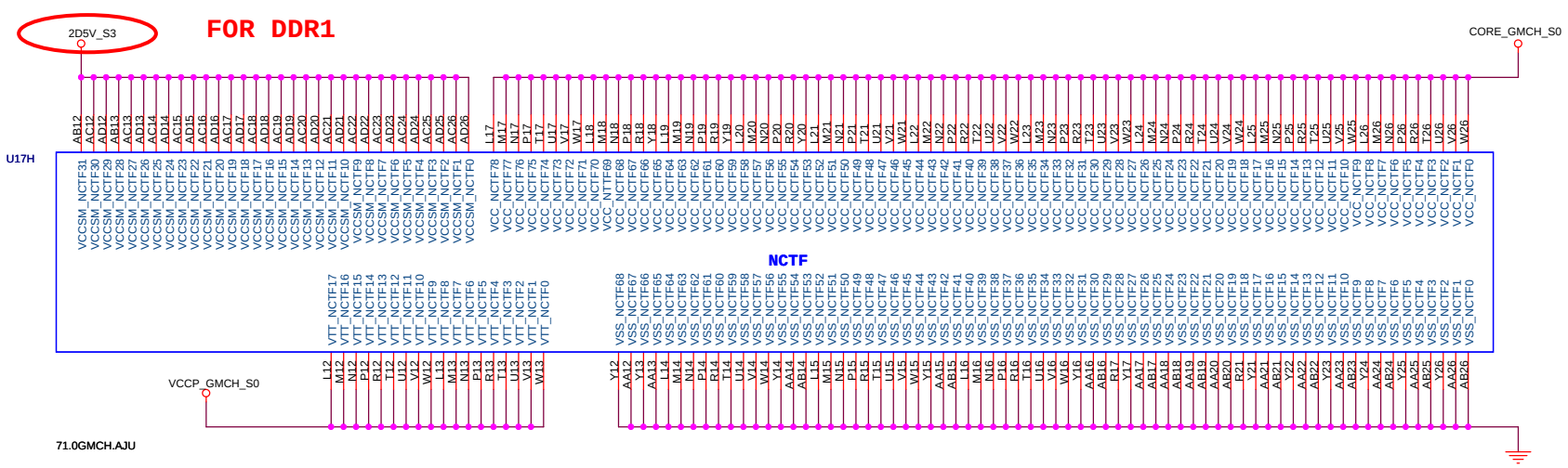

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**GMCH (5 of 5)**	
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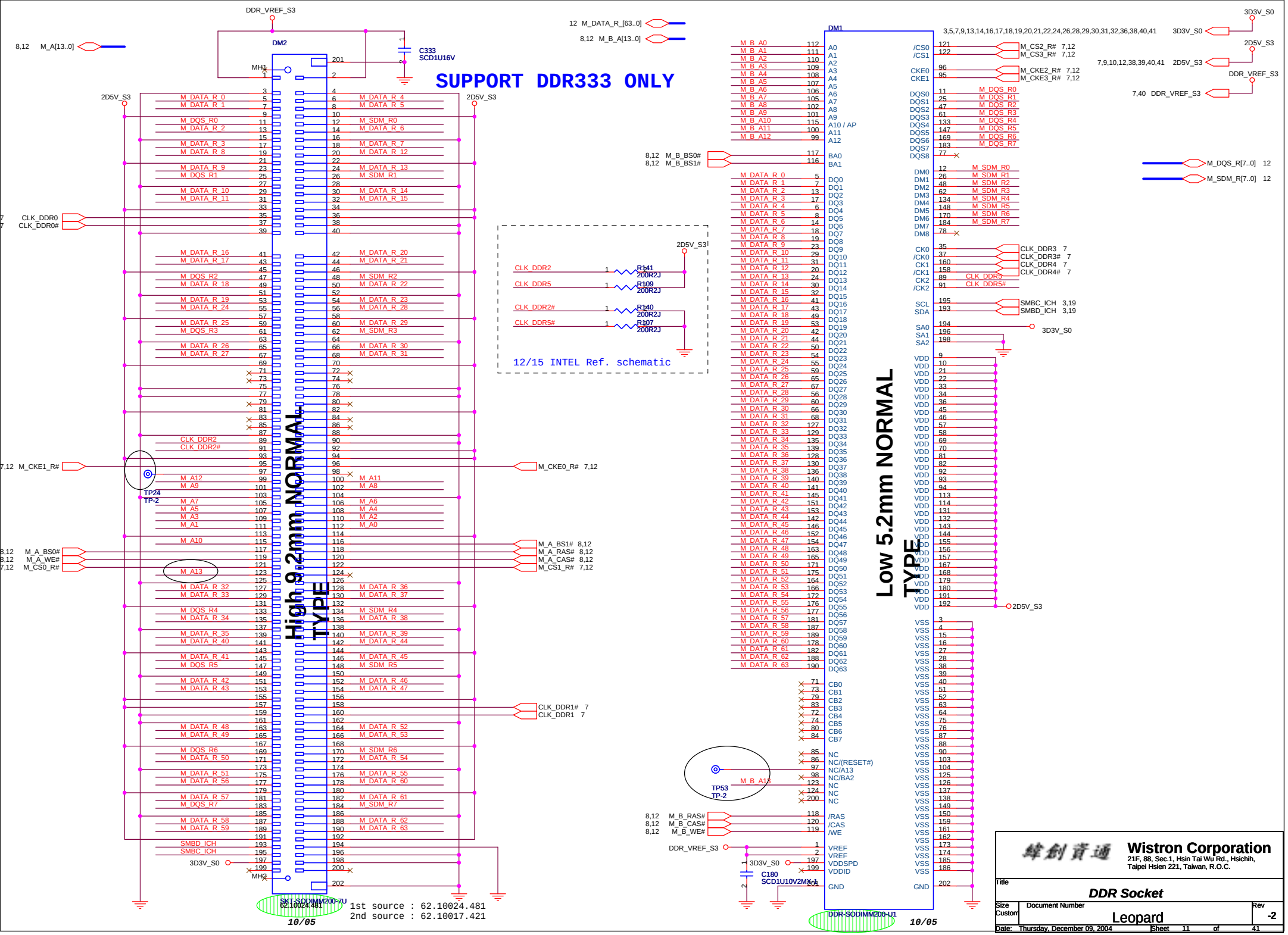
SUPPORT DDR333 ONLY
DM2
High 9.2mm NORMAL TYPE
DM1
Low 5.2mm NORMAL TYPE
DDR_VREF_S3
C333
SCD1U16V
2D5V_S3
3D3V_S0
M_A[13..0]
M_B_A[13..0]
M_DATA_R_[63..0]
M_DQS_R[7..0]
M_SDM_R[7..0]
CLK_DDR0
CLK_DDR0#
CLK_DDR2
CLK_DDR5
CLK_DDR2#
CLK_DDR5#
R141 200R2J
R109 200R2J
R140 200R2J
R107 200R2J
12/15 INTEL Ref. schematic
M_CKE1_R#
M_CKE0_R#
M_A_BS1#
M_A_RAS#
M_A_CAS#
M_CS1_R#
M_A_BS0#
M_A_WE#
M_CS0_R#
CLK_DDR1#
CLK_DDR1
M_B_BS0#
M_B_BS1#
M_B_RAS#
M_B_CAS#
M_B_WE#
M_CS2_R#
M_CS3_R#
M_CKE2_R#
M_CKE3_R#
CLK_DDR3
CLK_DDR3#
CLK_DDR4
CLK_DDR4#
CLK_DDR5
CLK_DDR5#
SMBC_ICH
SMBD_ICH
TP24
TP-2
TP53
TP-2
C180
SCD1U10V2MX-1
DDR-SODIMM200-7U
DDR-SODIMM200-U1
1st source : 62.10024.481
2nd source : 62.10017.421
10/05
10/05
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Title
DDR Socket
Size Custom
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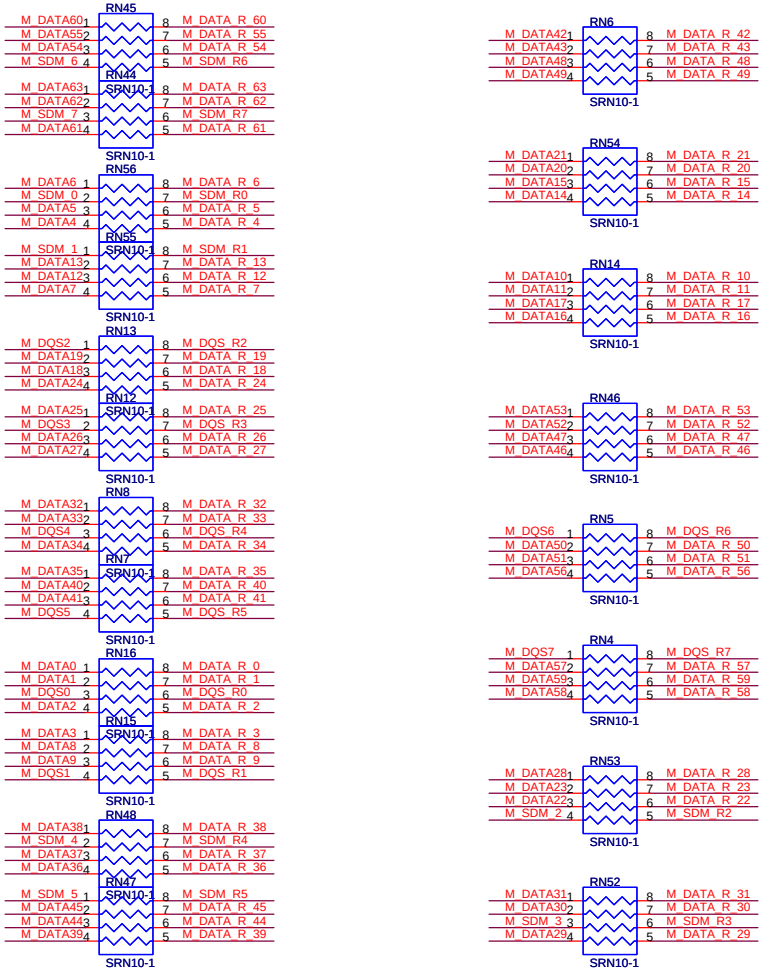
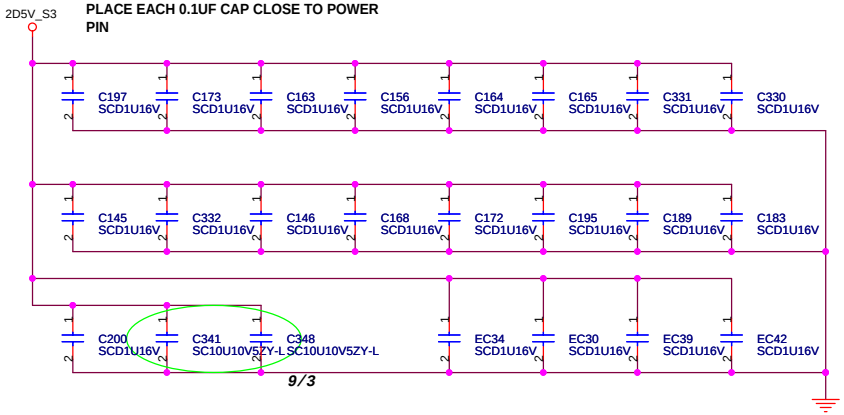
SERIES DAMPING

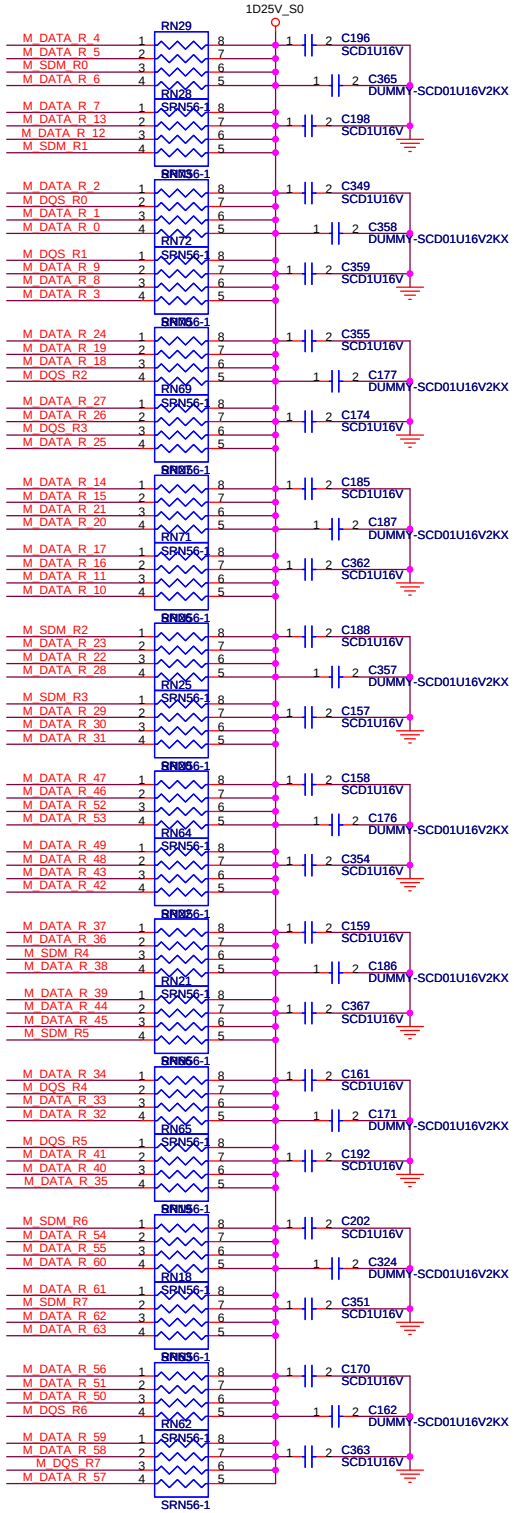
SC

Change RN to small size



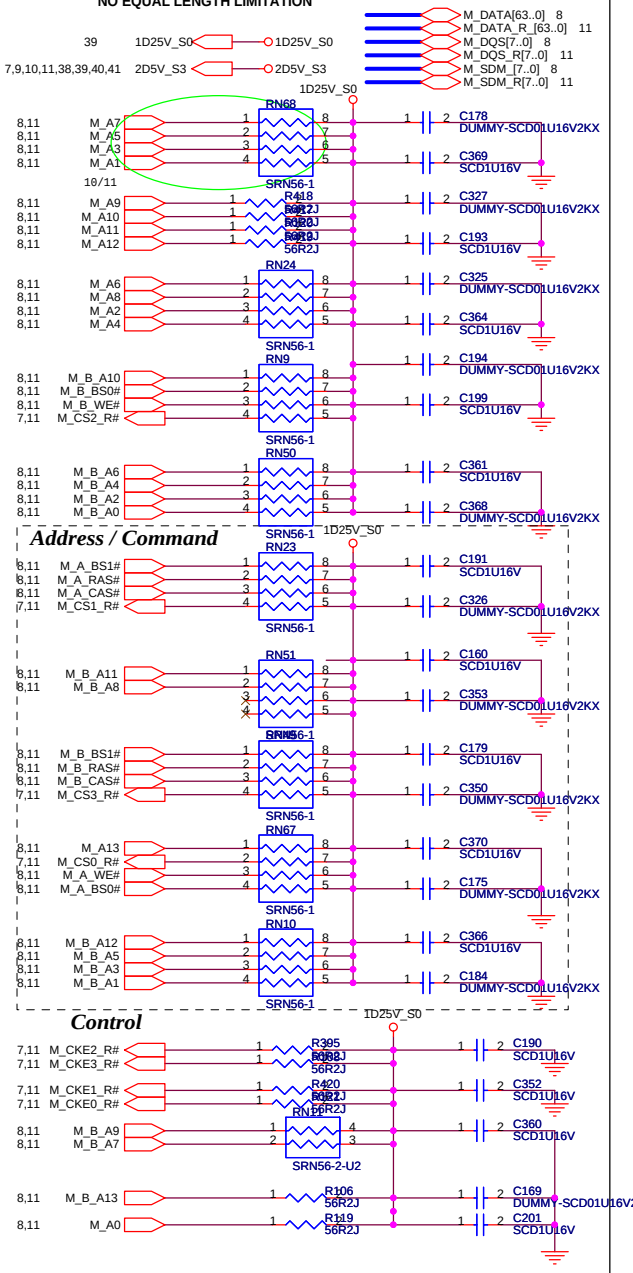
PLACE CAPS BETWEEN AND NEAR DDR SKTS
PLACE EACH 0.1UF CAP CLOSE TO POWER PIN





PARALLEL TERMINATION

PULL HIGH STUBS < 0.8", PLACE RPs CLOSE TO DM2
NO EQUAL LENGTH LIMITATION



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Title: **DDR Serial/Terminator Resistor**

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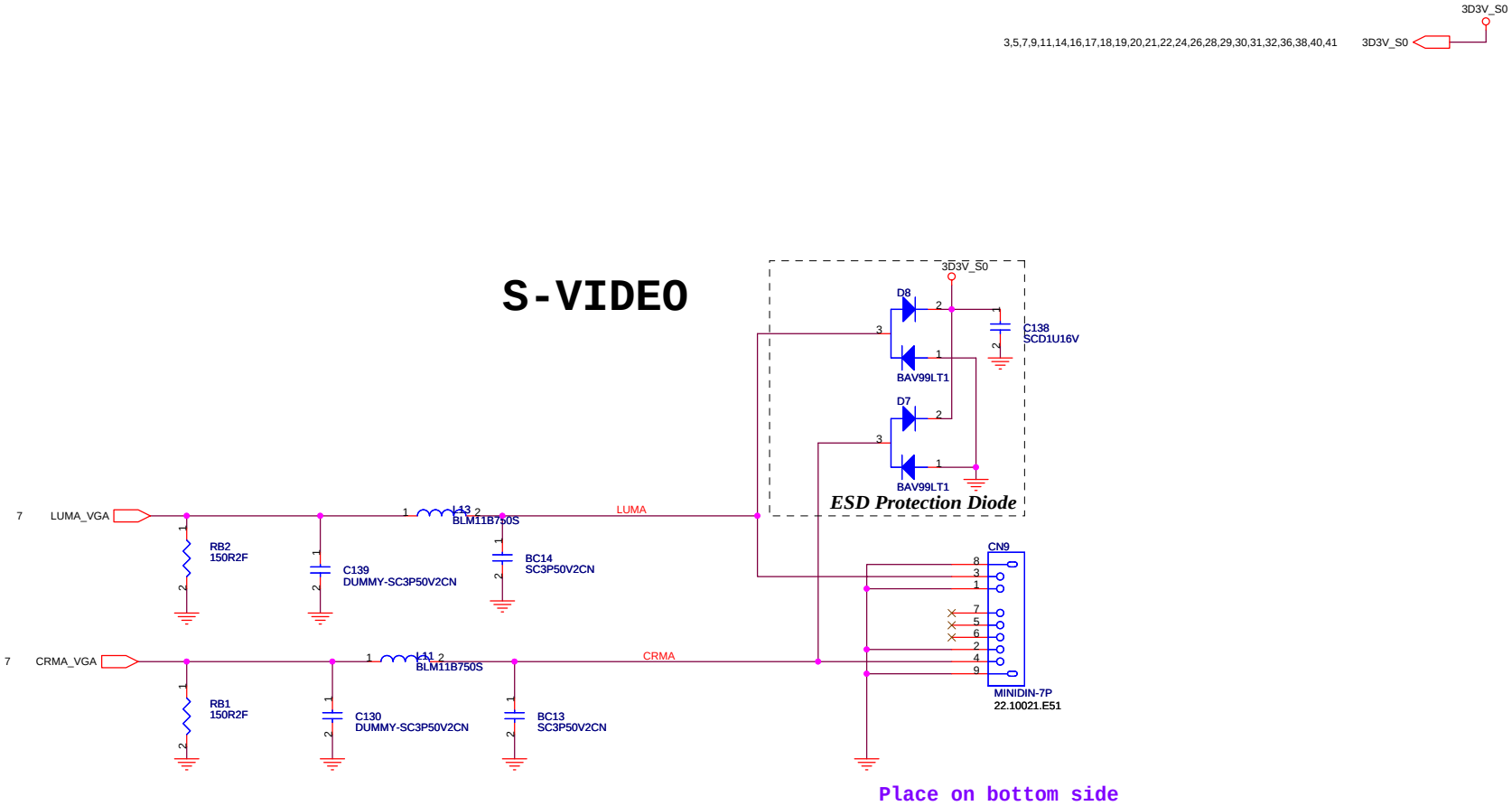

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Title	***S-VIDEO***	
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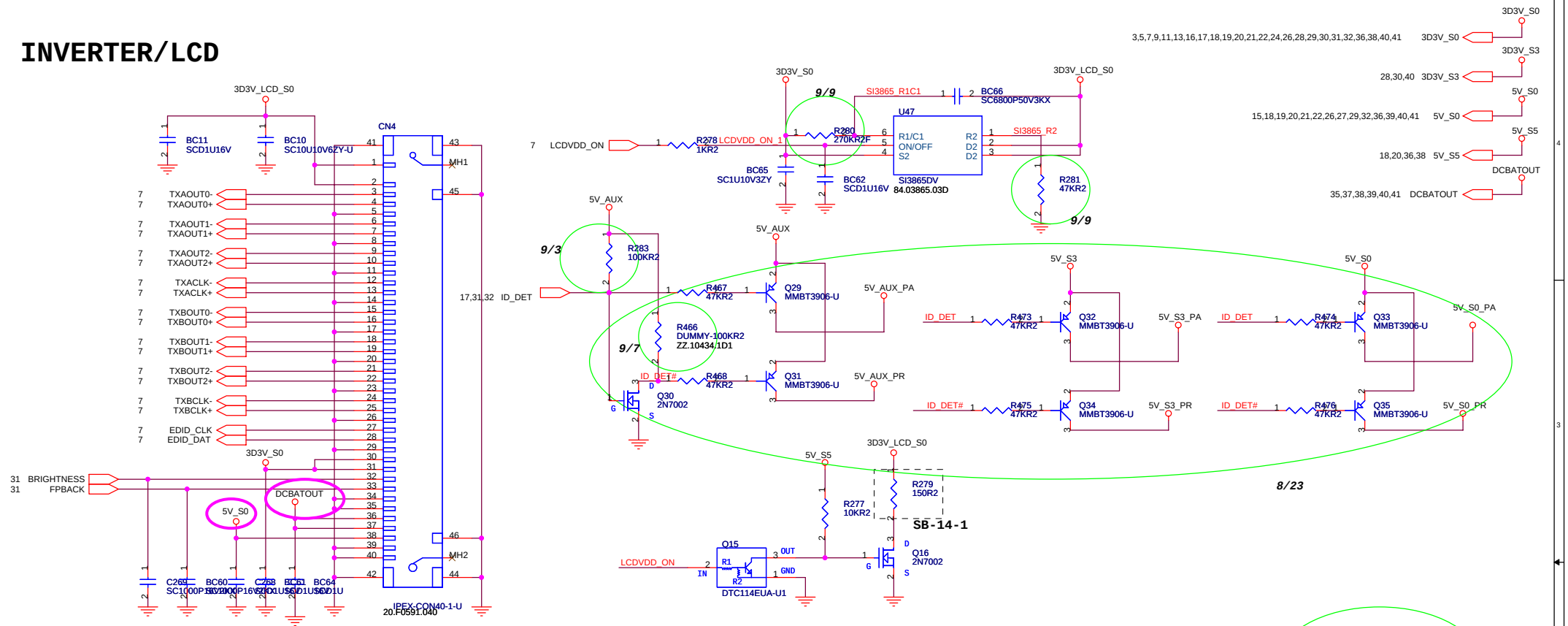
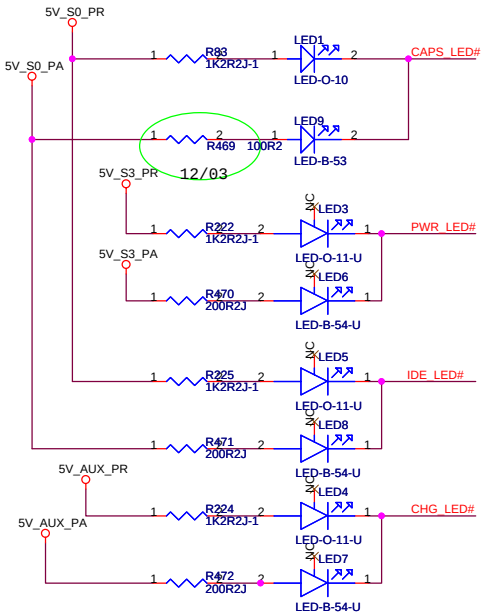
INVERTER/LCD

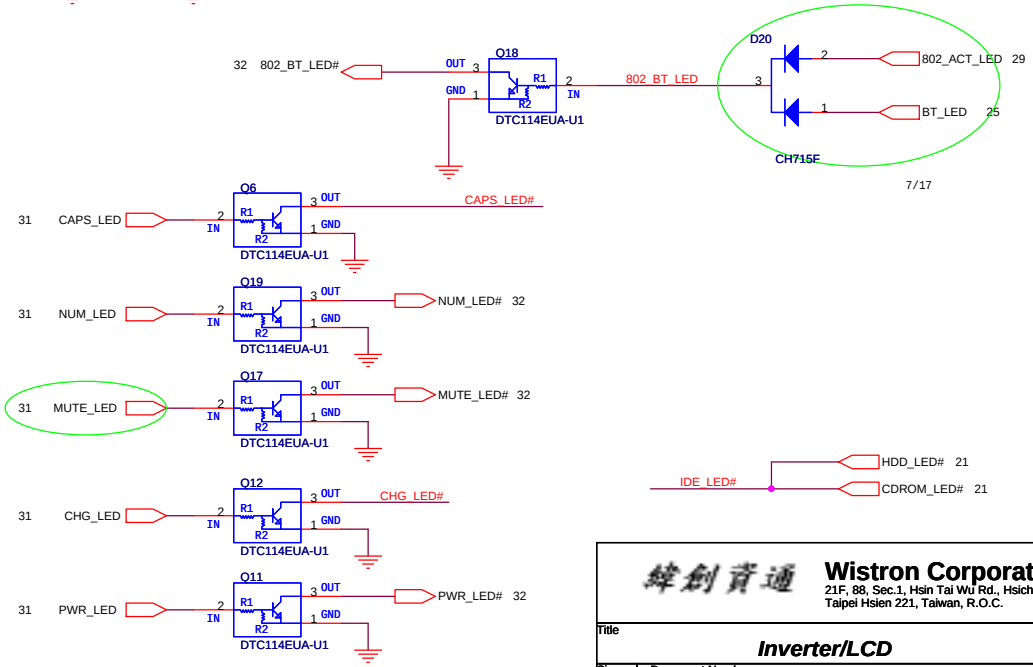




	PWR	CHR	HDD	IR	CAPS
PR Botton	Amber LED3	Amber LED4	Amber LED5	X	Amber LED1
PA Top	Blue LED6	Blue LED7	Blue LED8	X	Blue LED1

PA & PR diffent parts

	PA	PR
LED1	83.00190.Y70	83.00190.W70
LED3	Dummy	83.00110.D70
LED4	Dummy	83.00110.D70
LED5	Dummy	83.00110.D70
LED6	83.00110.E70	Dummy
LED7	83.00110.E70	Dummy
LED8	83.00110.E70	Dummy
R83	63.20134.1D1	63.10234.1D1
R222	63.20134.1D1	63.10234.1D1
R225	63.20134.1D1	63.10234.1D1
R224	63.20134.1D1	63.10234.1D1



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Title: Inverter/LCD

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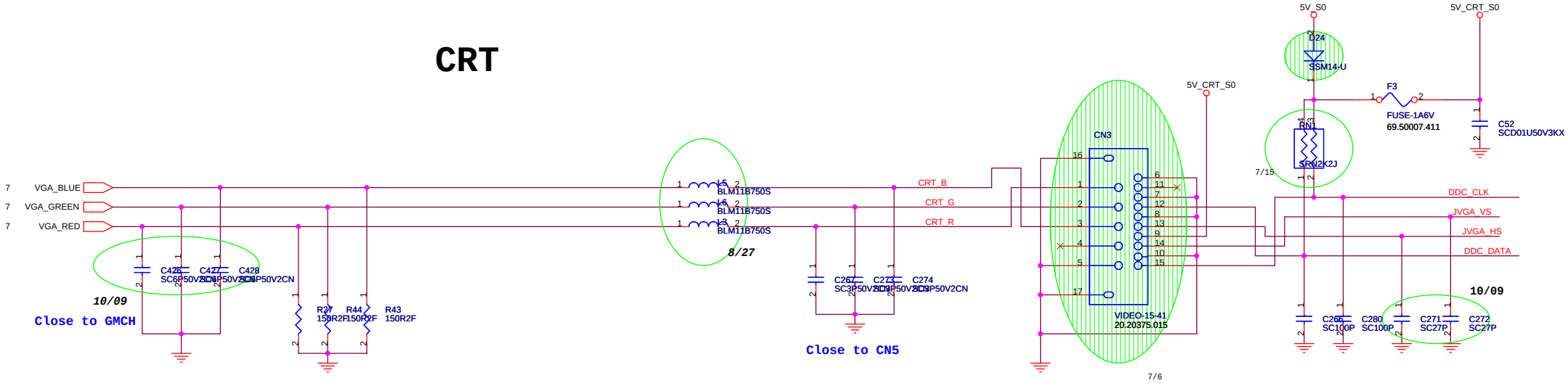
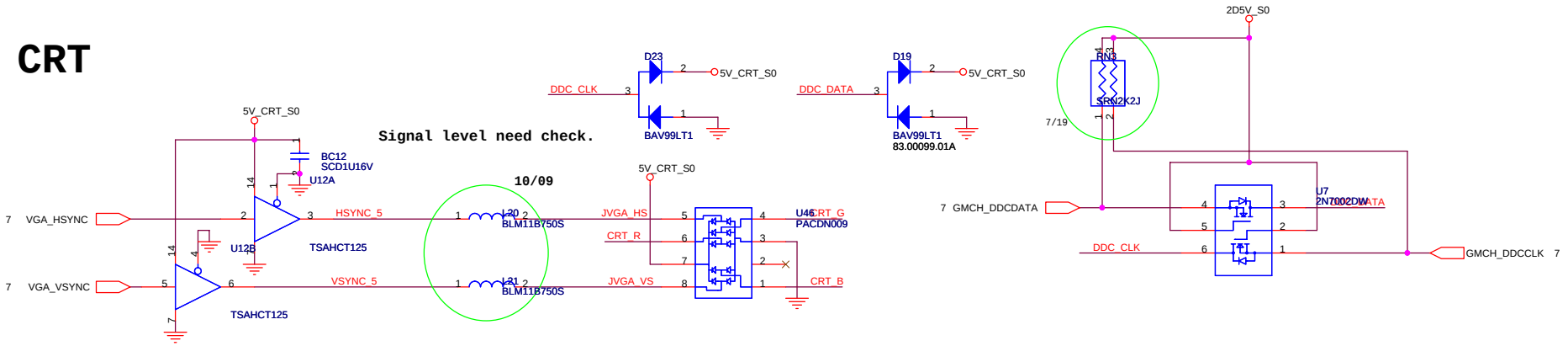
CRT CONN

CRT



CRT



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**CRT/ CIR**	
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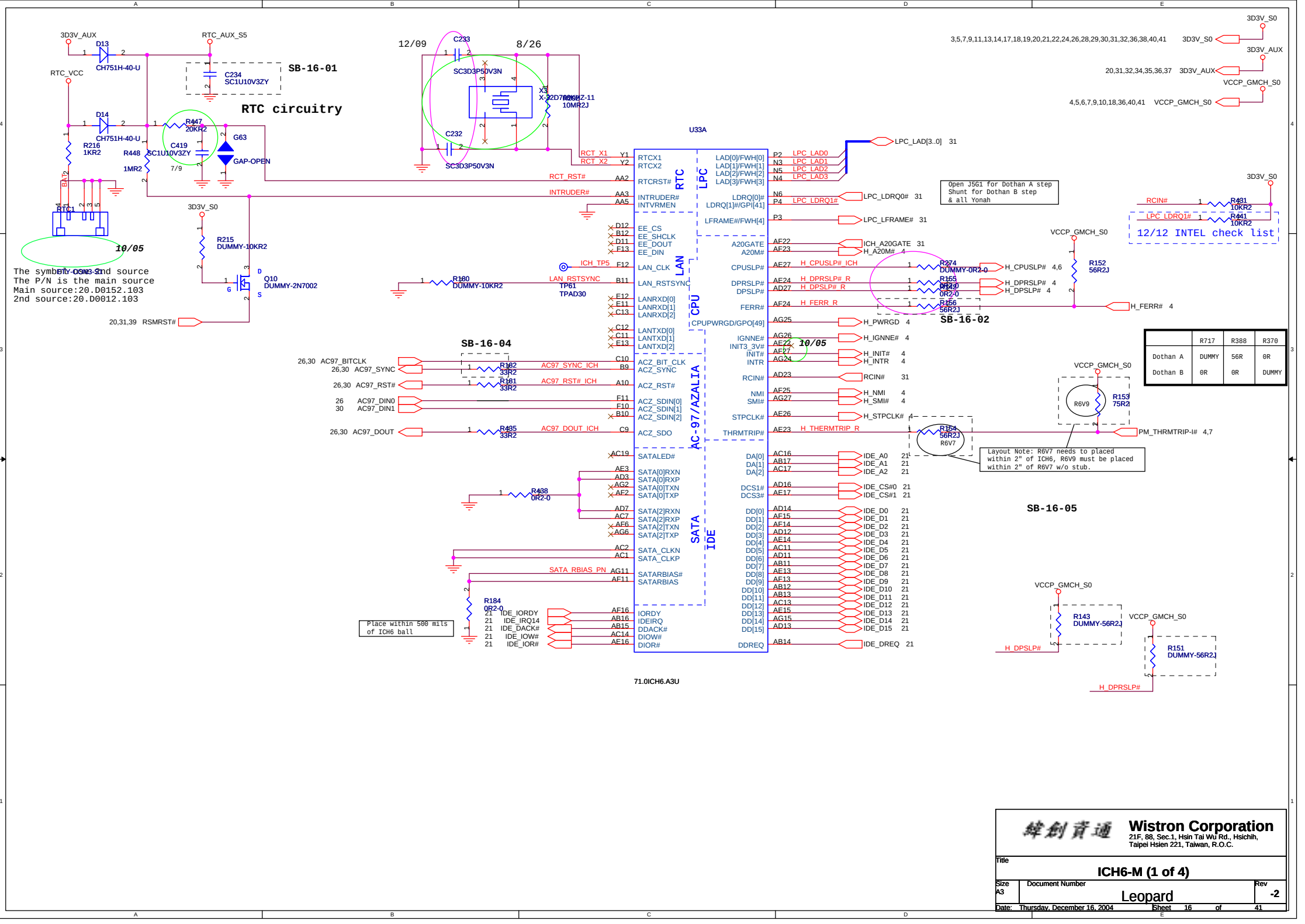

	R717	R388	R370
Dothan A	DUMMY	56R	0R
Dothan B	0R	0R	DUMMY

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Title: ICH6-M (1 of 4)

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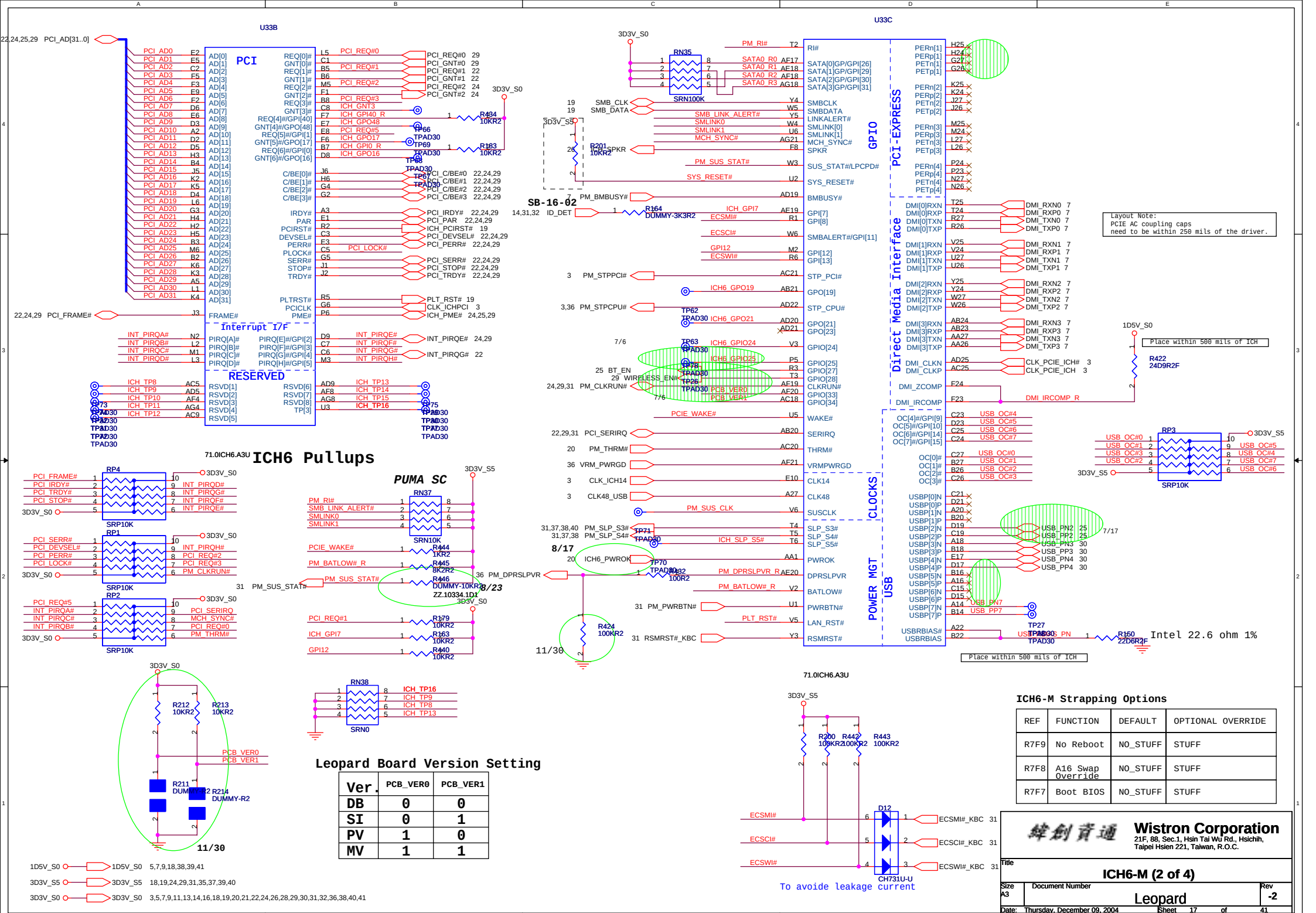
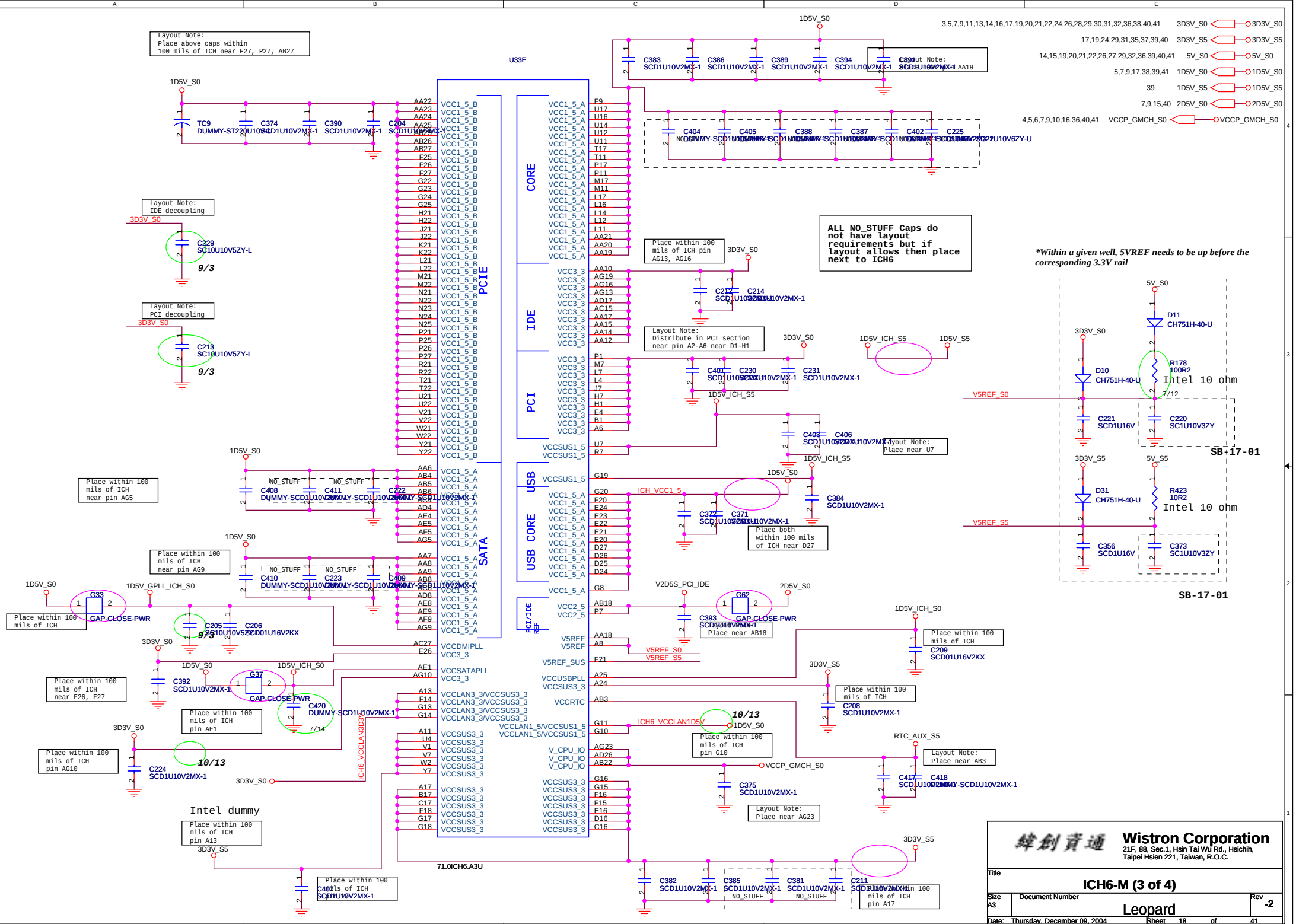
Date: Thursday, December 16, 2004 | Sheet 16 of 41



Ver.	PCB_VER0	PCB_VER1
DB	0	0
SI	0	1
PV	1	0
MV	1	1

REF	FUNCTION	DEFAULT	OPTIONAL OVERRIDE
R7F9	No Reboot	NO_STUFF	STUFF
R7F8	A16 Swap Override	NO_STUFF	STUFF
R7F7	Boot BIOS	NO_STUFF	STUFF


U33E
PCIE
SATA
CORE
IDE
PCI
USB
USB CORE
RCI/IDE REF
Layout Note: Place above caps within 100 mils of ICH near F27, P27, AB27
Layout Note: IDE decoupling
Layout Note: PCI decoupling
Place within 100 mils of ICH near pin AG5
Place within 100 mils of ICH near pin AG9
Place within 100 mils of ICH
Place within 100 mils of ICH near E26, E27
Place within 100 mils of ICH pin AE1
Place within 100 mils of ICH pin AG10
Intel dummy
Place within 100 mils of ICH pin A13
Place within 100 mils of ICH pin AG13, AG16
Layout Note: Distribute in PCI section near pin A2-A6 near D1-H1
Place both within 100 mils of ICH near D27
Place near AB18
Place within 100 mils of ICH pin G10
Layout Note: Place near AG23
Layout Note: Place near U7
Place within 100 mils of ICH pin A17
Layout Note: Place near AB3
ALL NO_STUFF Caps do not have layout requirements but if layout allows then place next to ICH6
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Intel 10 ohm
SB-17-01
71.0ICH6.A3U
Wistron Corporation
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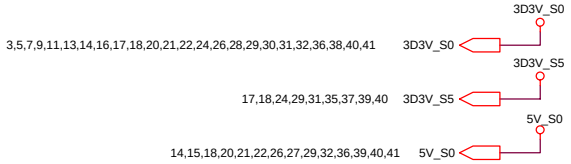
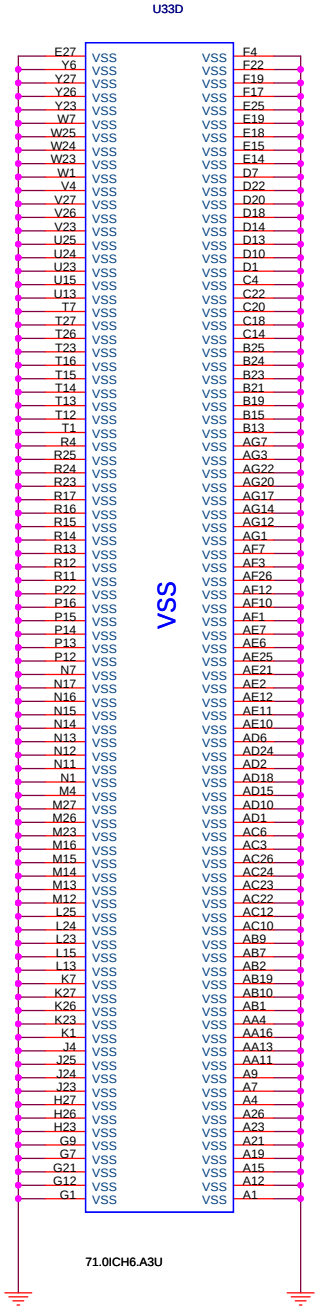
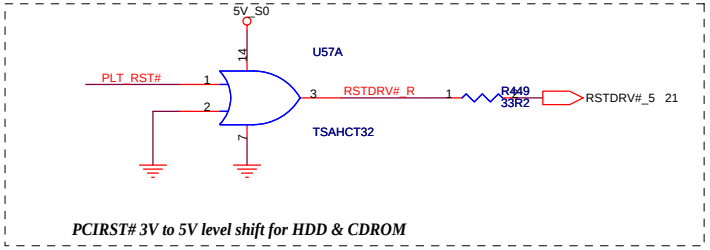
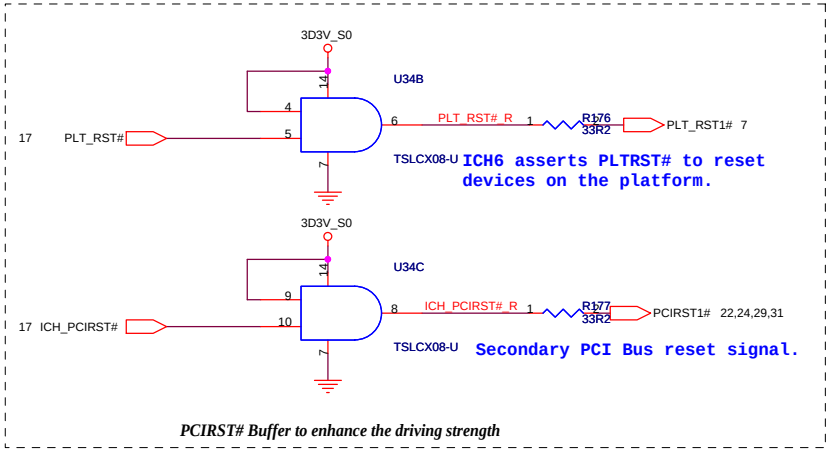
Title
ICH6-M (3 of 4)
Size A3
Document Number
Leopard
Rev -2
Date: Thursday, December 09, 2004
Sheet 18 of 41



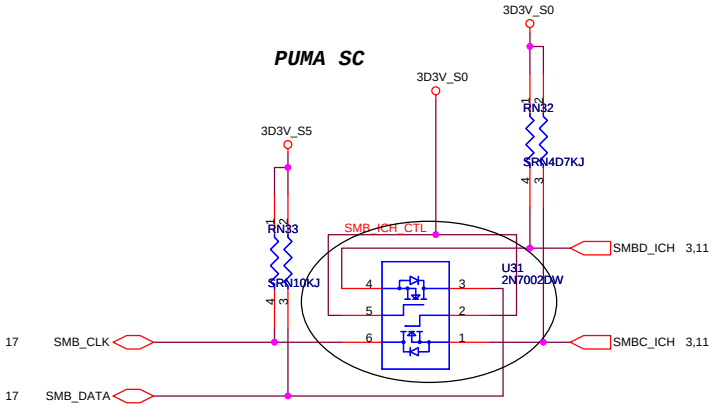


Cougar
SC





SMBUS(ICH6 ---> SODIMM,CLKGEN)



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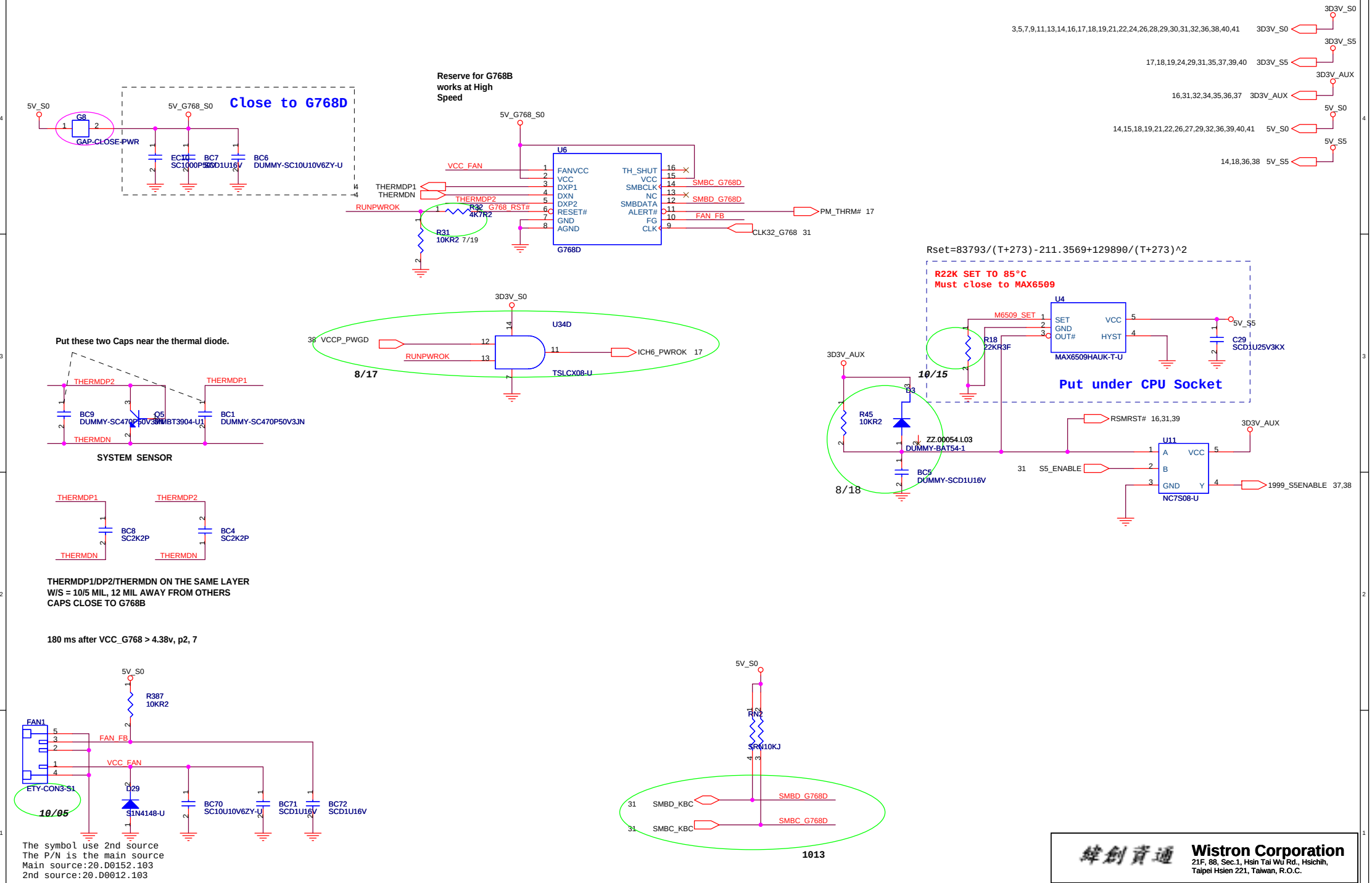
Title: ICH6-M (4 of 4)

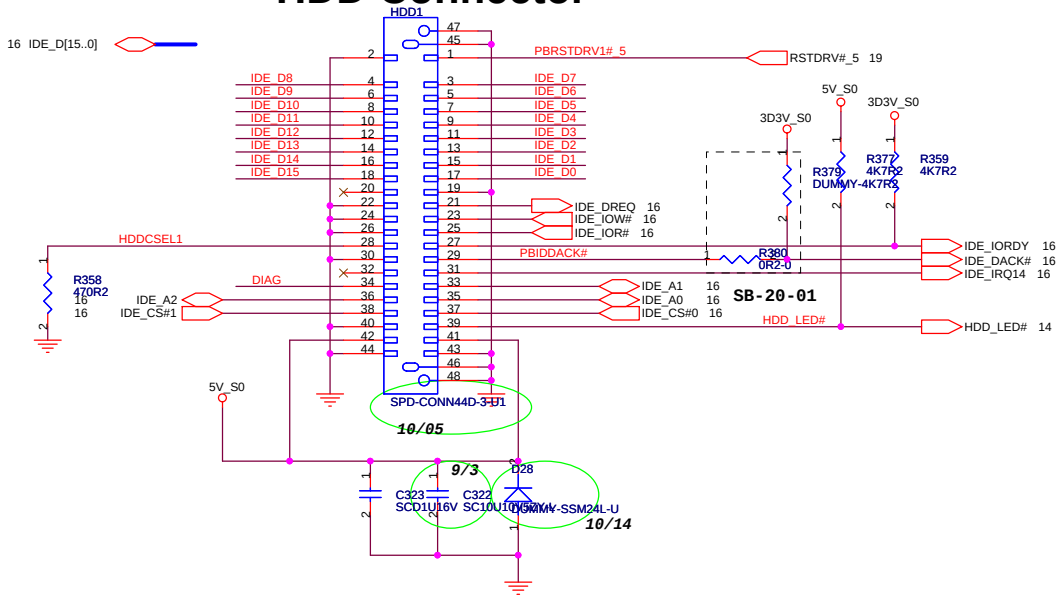
Size	Document Number	Rev
A3	Leopard	-2

Date: Thursday, December 09, 2004 Sheet 19 of 41

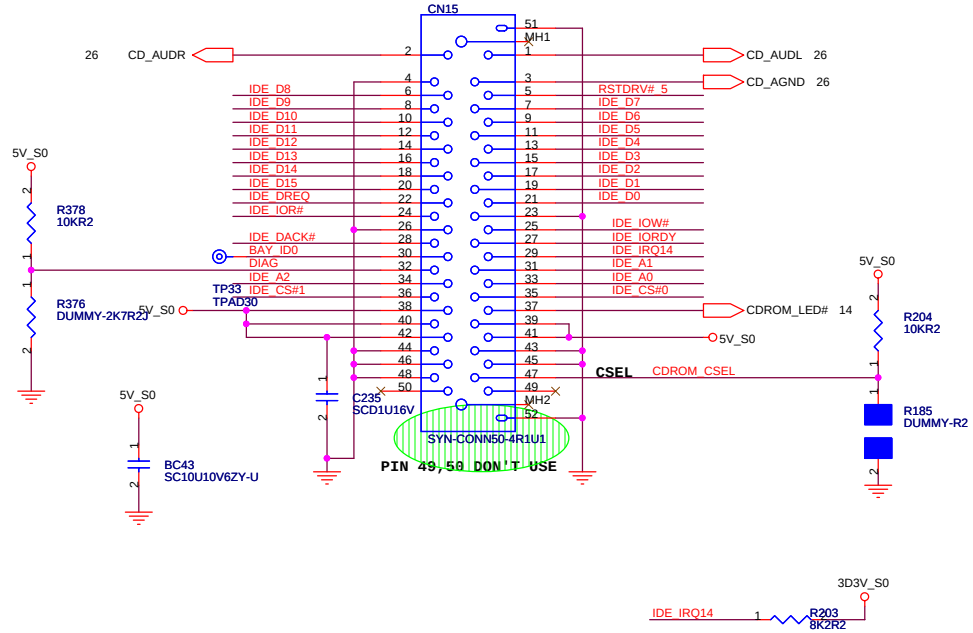


緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***G768D***	
Size A3	Document Number Leopard	Rev -2
Date: Thursday, December 09, 2004	Sheet 20 of 41	

HDD Connector



CDROM



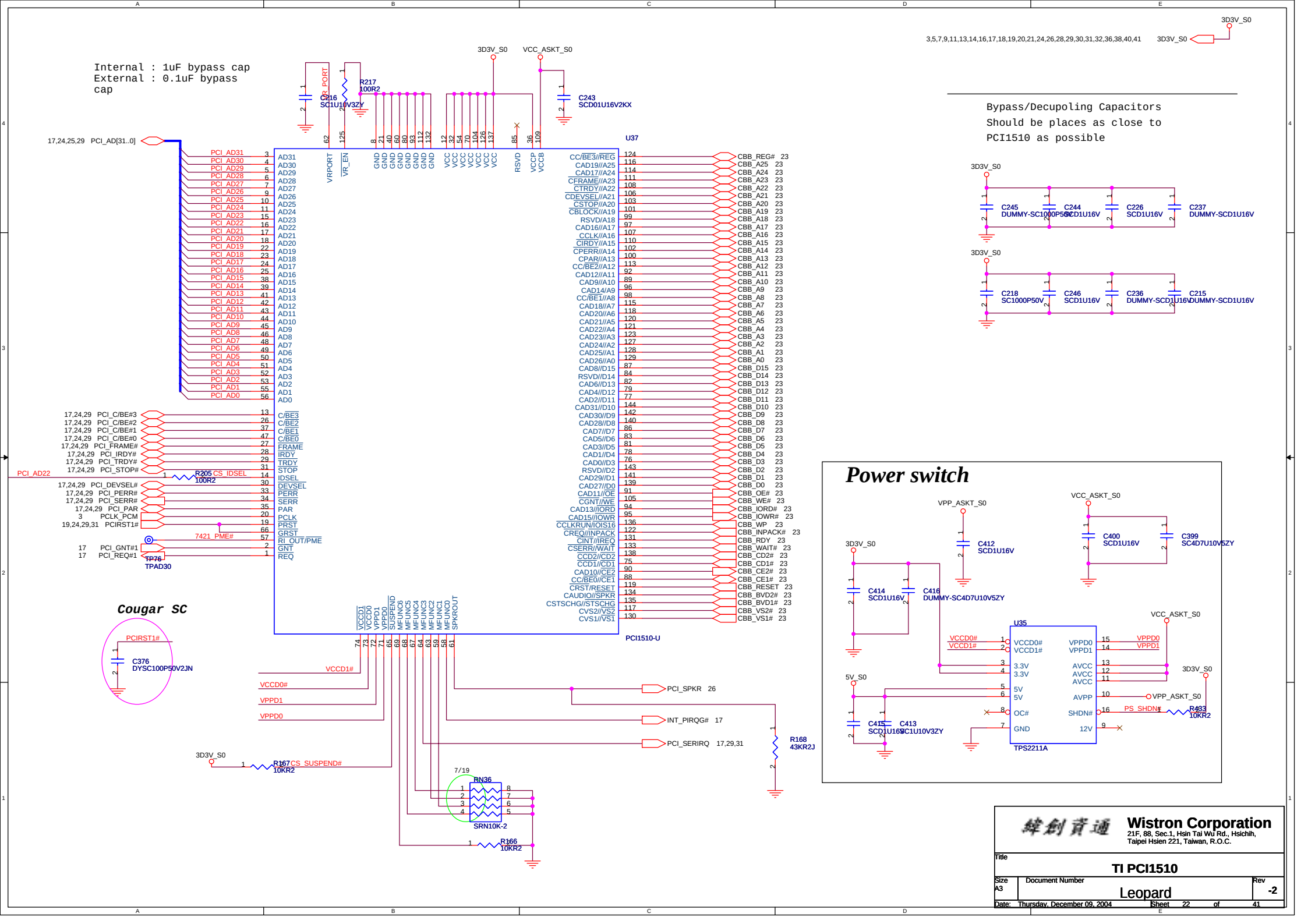
3,5,7,9,11,13,14,16,17,18,19,20,22,24,26,28,29,30,31,32,36,38,40,41 3D3V_S0 — 3D3V_S0

24,41 3D3V_LAN_S5 — 3D3V_LAN_S5

14,15,18,19,20,22,26,27,29,32,36,39,40,41 5V_S0 — 5V_S0

5,7,9,17,18,38,39,41 1D5V_S0 — 1D5V_S0

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***HDD / CDROM***	
Size A3	Document Number Leopard	Rev -2
Date: Thursday, December 09, 2004	Sheet 21 of 41	



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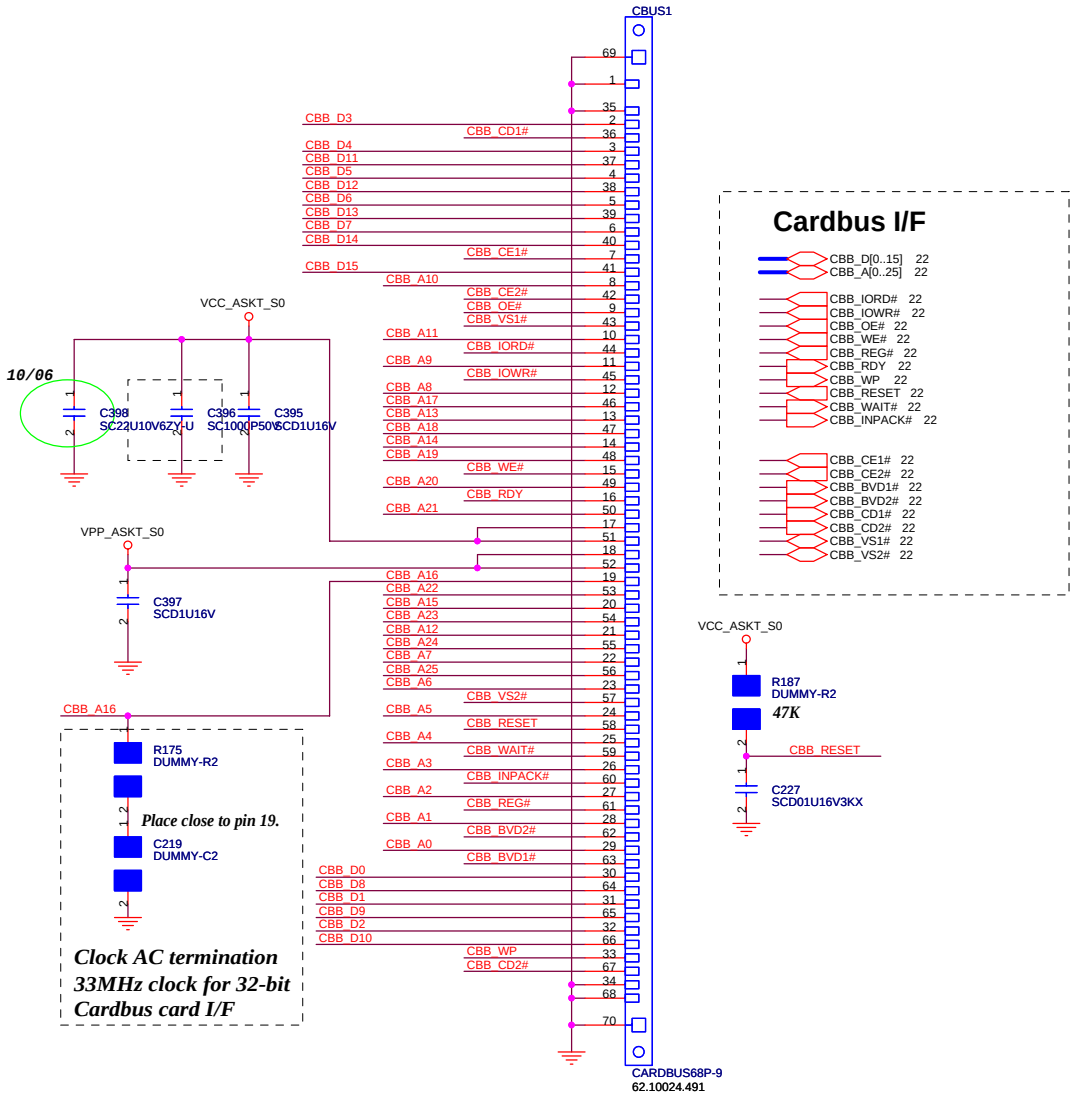
Title: TI PCI1510

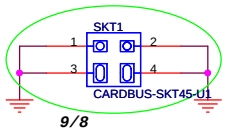
Size: A3 | Document Number: Leopard | Rev: -2

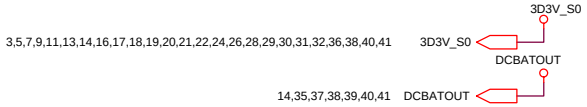
Date: Thursday, December 09, 2004 | Sheet 22 of 41

PCMCIA Socket



Cardbus I/F





Wistron Corporation
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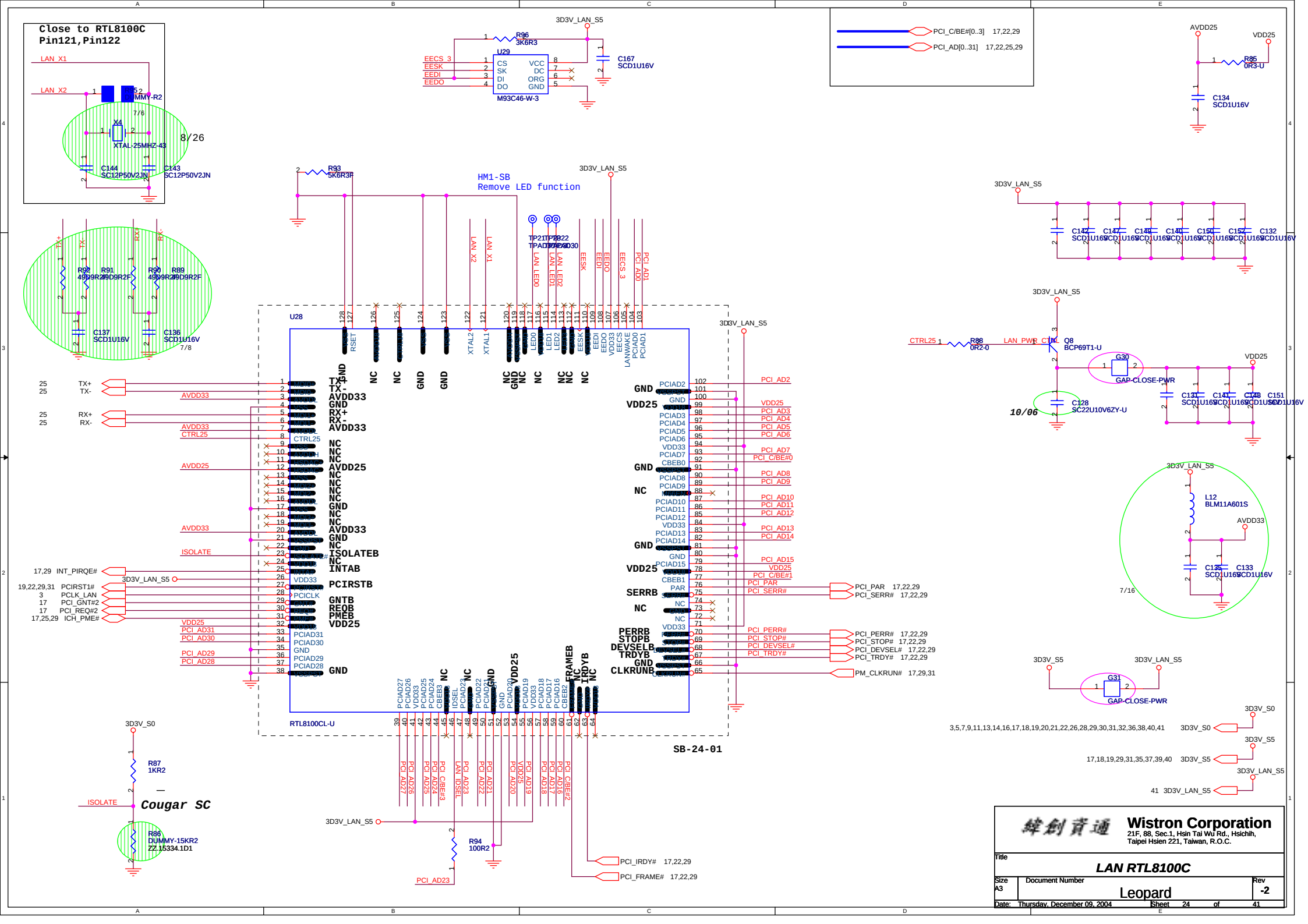
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCMCIA SLOT

Size	Document Number	Rev
A3	Leopard	-2

Date: Thursday, December 09, 2004 Sheet 23 of 41



Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN RTL8100C**

Size: A3 | Document Number: Leopard | Rev: -2

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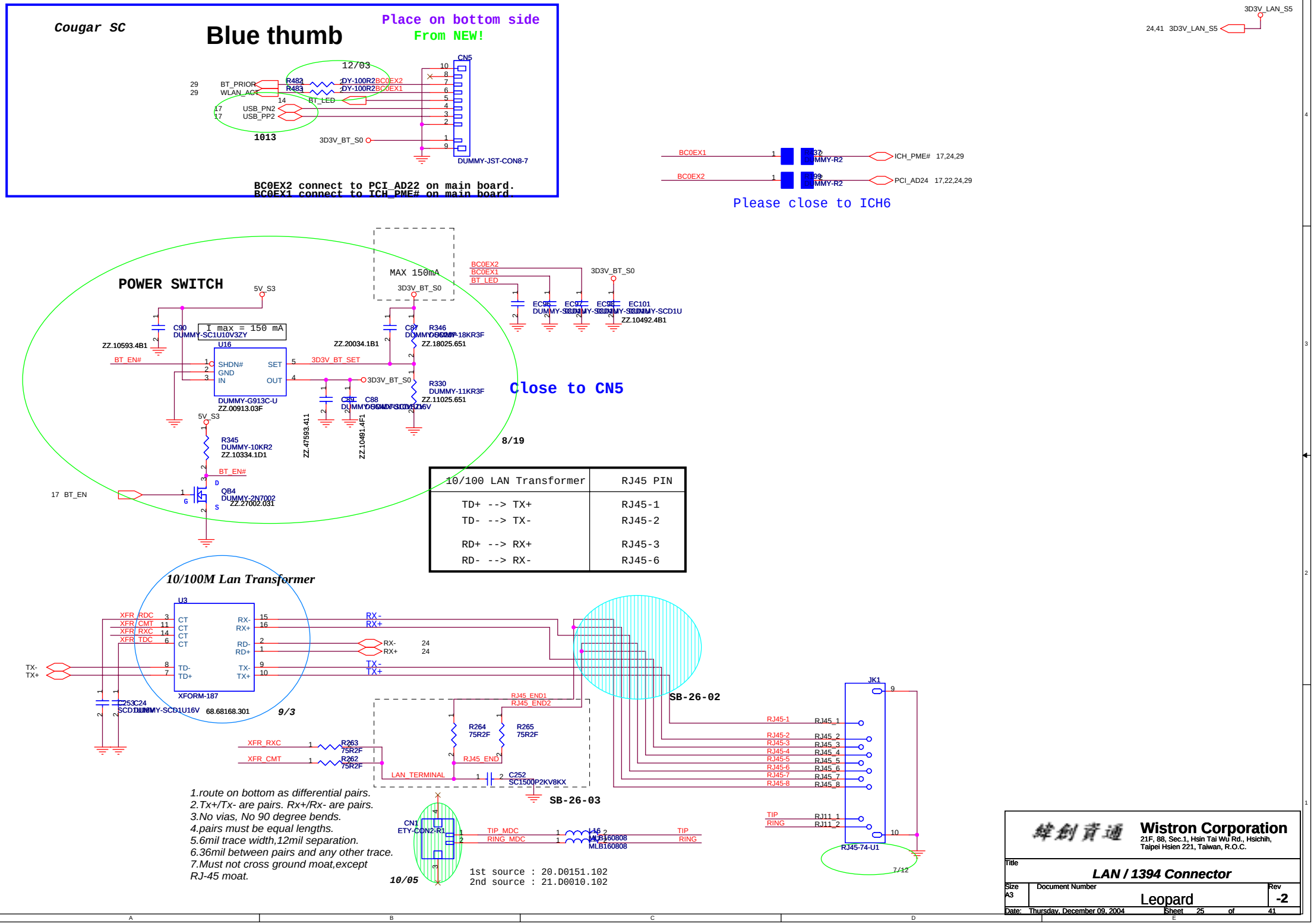
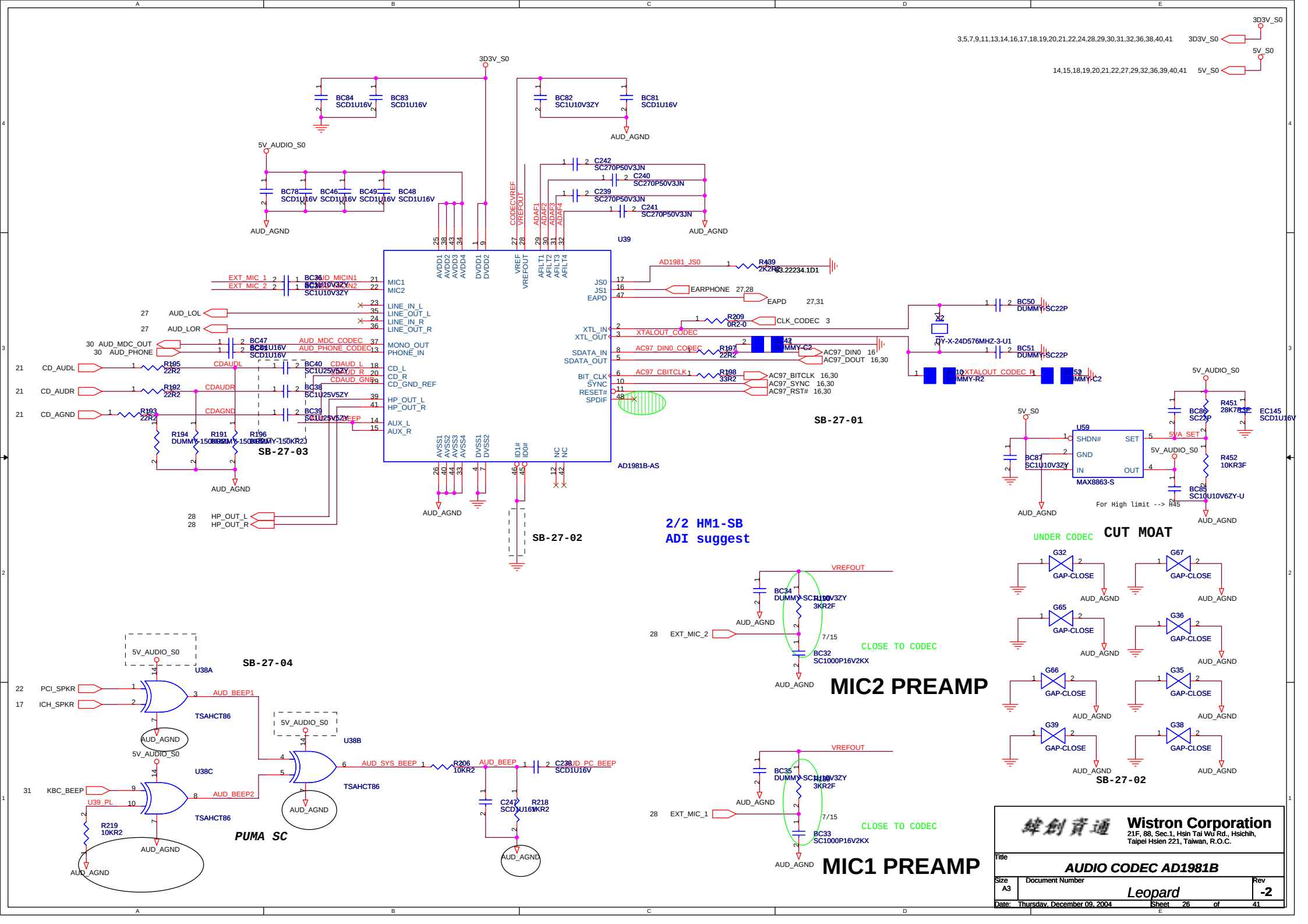
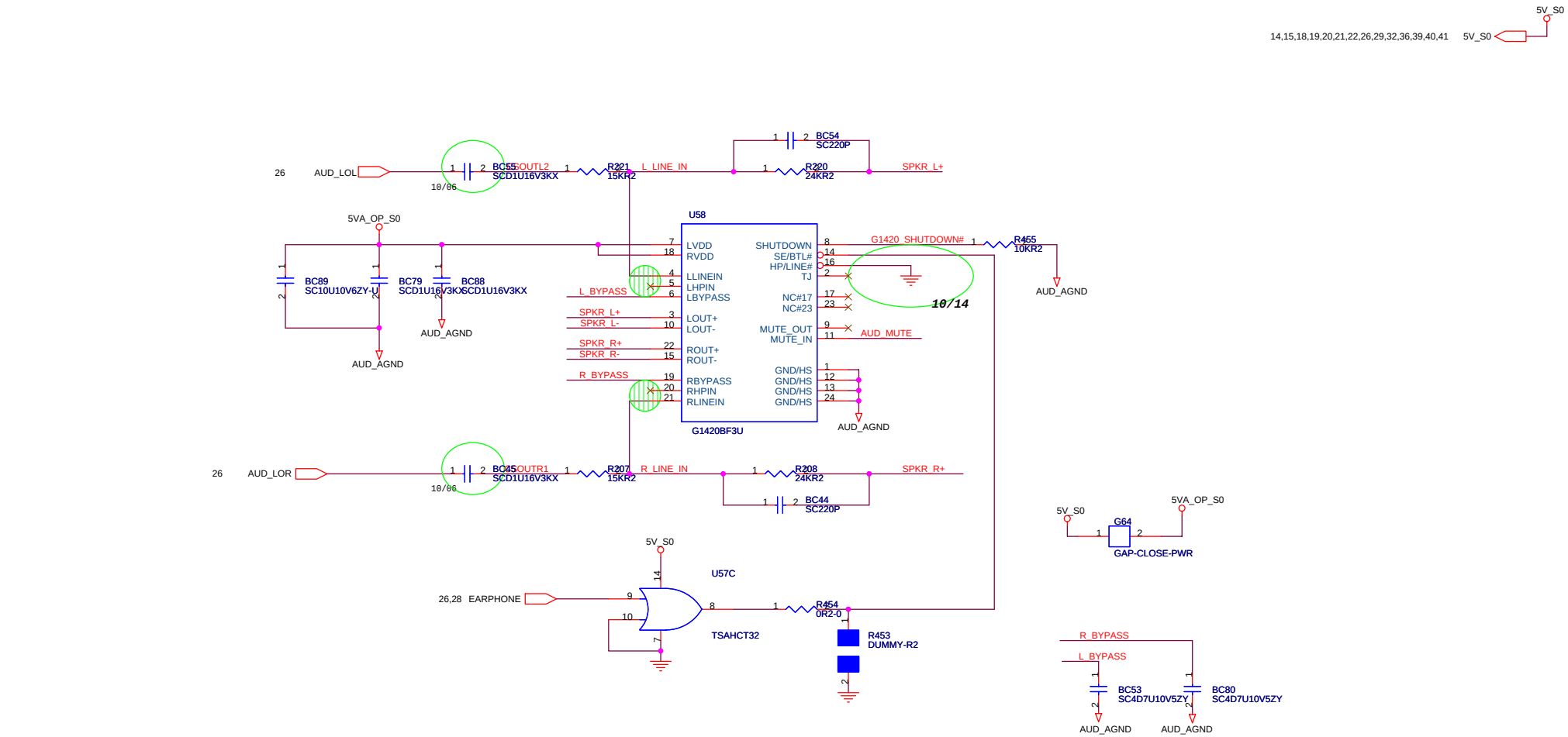


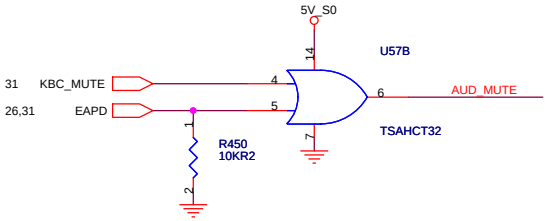
10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

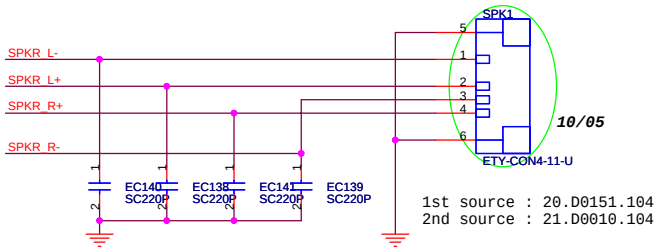
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.


3D3V_S0
5V_S0
5V_AUDIO_S0
AUD_AGND
U39
AD1981B-AS
SB-27-01
SB-27-02
SB-27-03
SB-27-04
2/2 HM1-SB
ADI suggest
CUT MOAT
UNDER CODEC
MIC2 PREAMP
MIC1 PREAMP
CLOSE TO CODEC
PUMA SC
U38A
U38B
U38C
TSAHCT86
U59
MAX8863-S
For High limit --> R45
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO CODEC AD1981B
Size
A3
Document Number
Leopard
Rev
-2
Date: Thursday, December 09, 2004
Sheet 26 of 41



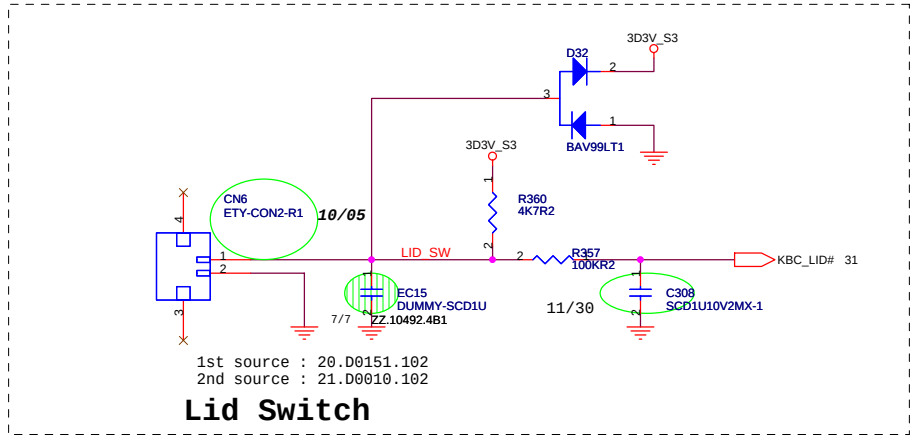
Speaker



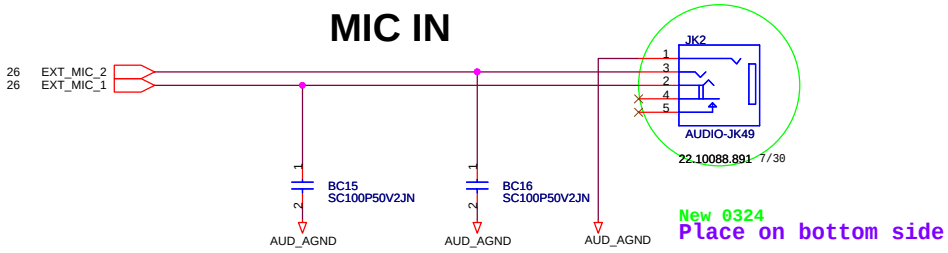


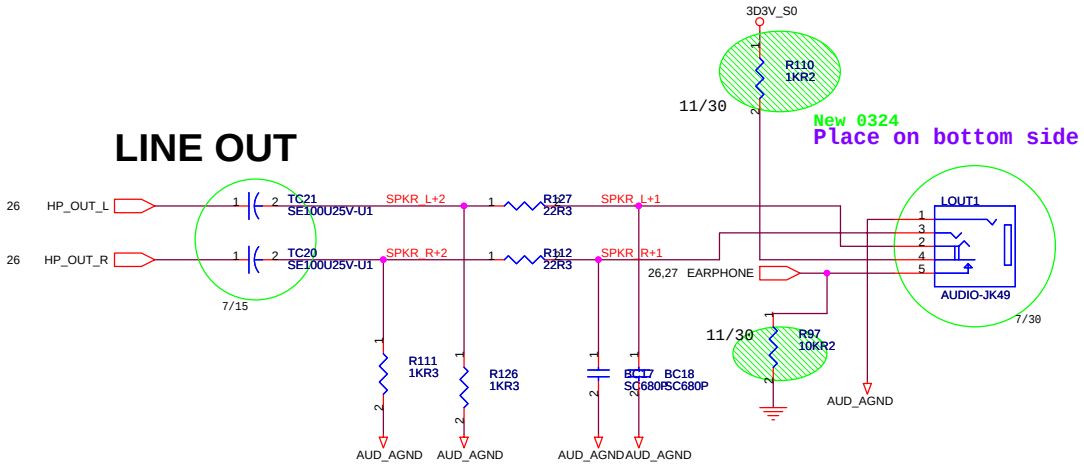
1st source : 20.D0151.104
2nd source : 21.D0010.104

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***AUDIO***	
Size A3	Document Number Leopard	Rev -2
Date: Thursday, December 09, 2004	Sheet 27 of 41	



3,5,7,9,11,13,14,16,17,18,19,20,21,22,24,26,29,30,31,32,36,38,40,41 3D3V_S0





緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**AUDIO CONN/LID switch**	
Size A3	Document Number Leopard	Rev -2
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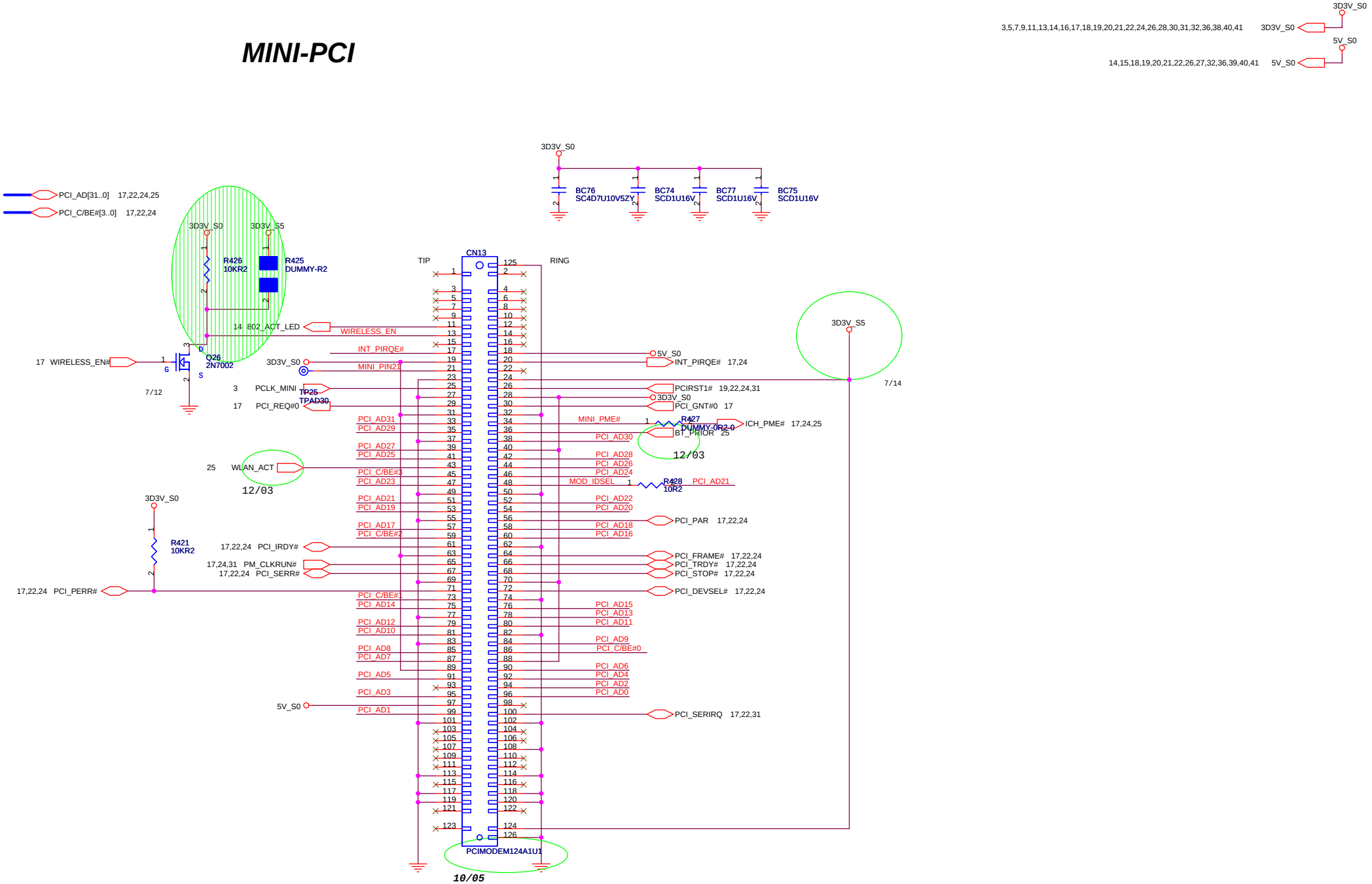
MINI-PCI



The symbol use 2nd source
The P/N is the main source
Main source:62.10032.001
2nd source:62.10032.031

Wistron Corporation
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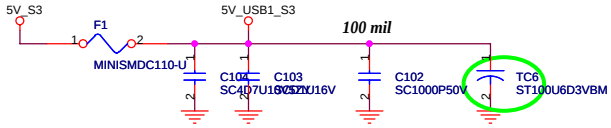
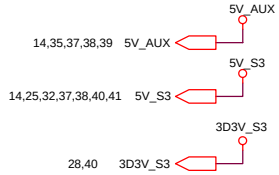
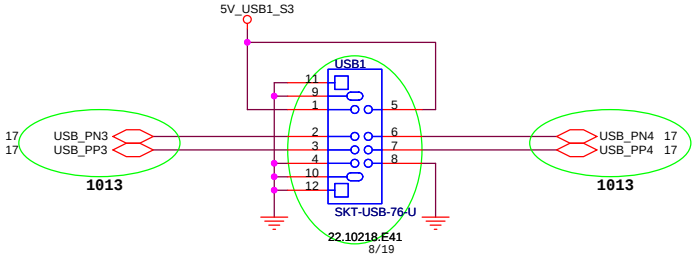
Taipei Hsien 221, Taiwan, R.O.C.

Title	MINI-PCI	
Size A3	Document Number Leopard	Rev -2
Date: Thursday, December 09, 2004	Sheet 29 of 41	

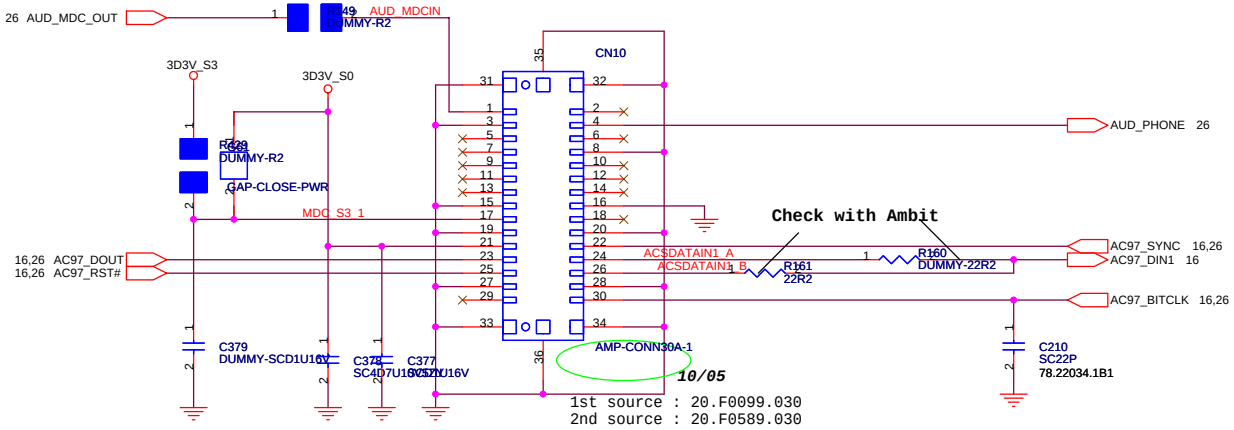
USB POWER



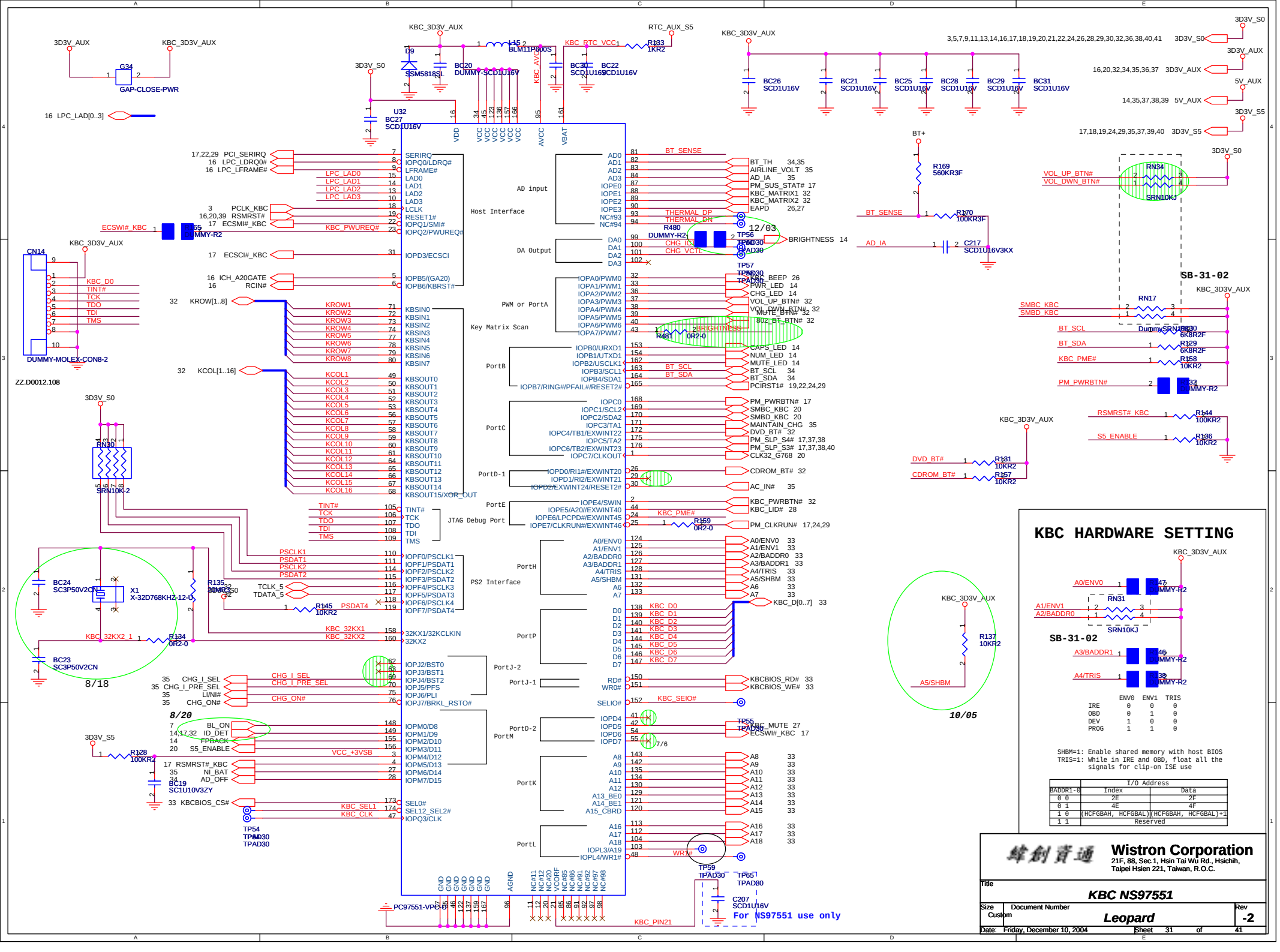




MDC Connector



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***USB / MDC CONN.***	
Size A3	Document Number Leopard	Rev -2
Date: Thursday, December 09, 2004	Sheet 30 of 41	



	ENV0	ENV1	TRIS
IRE	0	0	0
OBD	0	1	0
DEV	1	0	0
PROG	1	1	0

SHBM=1: Enable shared memory with host BIOS
TRIS=1: While in IRE and OBD, float all the signals for clip-on ISE use

	I/O Address	
BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1 1	Reserved	

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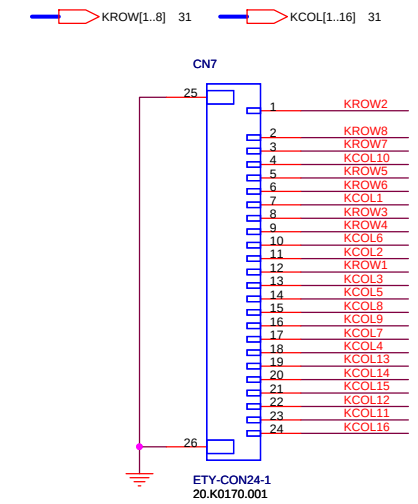
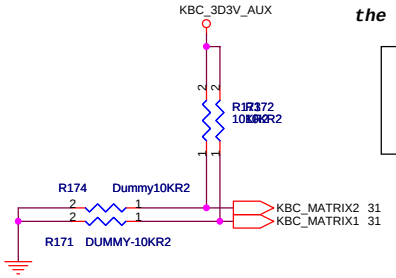
Title: **KBC NS97551**

Size: Custom | Document Number: **Leopard** | Rev: **-2**

Date: Friday, December 10, 2004 | Sheet 31 of 41

INTERNAL KEYBOARD CONNECTOR



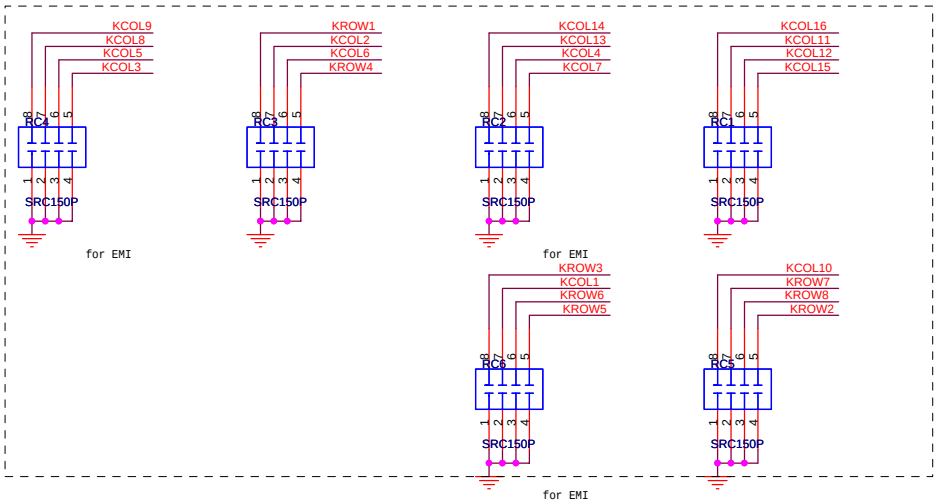


the matrix table for PCB

KBC_MATRIX2,KBC_MATRIX1

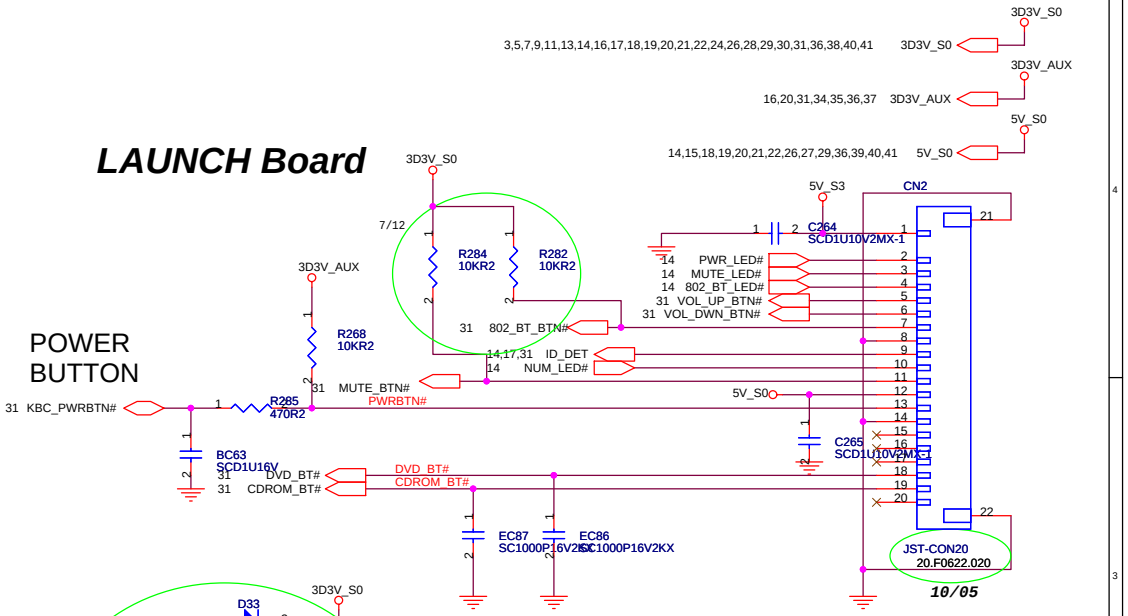
	PA	PR
FF	00	01
DF	10	11

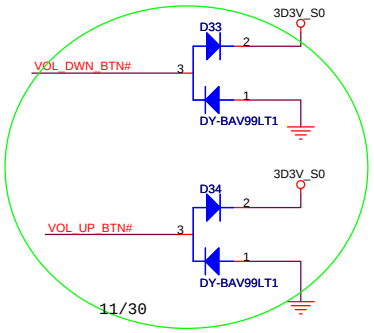
	NONE Quick Play	Quick Play
MATRIXID1#	0	1

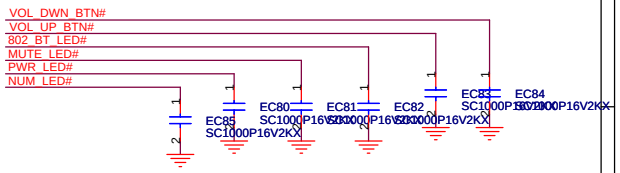


SB-32-01

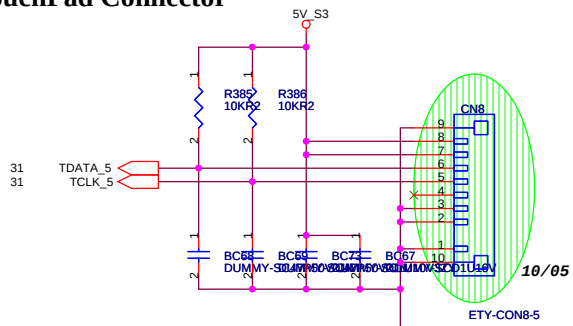
LAUNCH Board







TouchPad Connector



The symbol use 2nd source
The P/N is the main source
Main source:20.D0151.108
2nd source:21.D0010.108

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KEYBOARD/TOUCH PAD/Launch key

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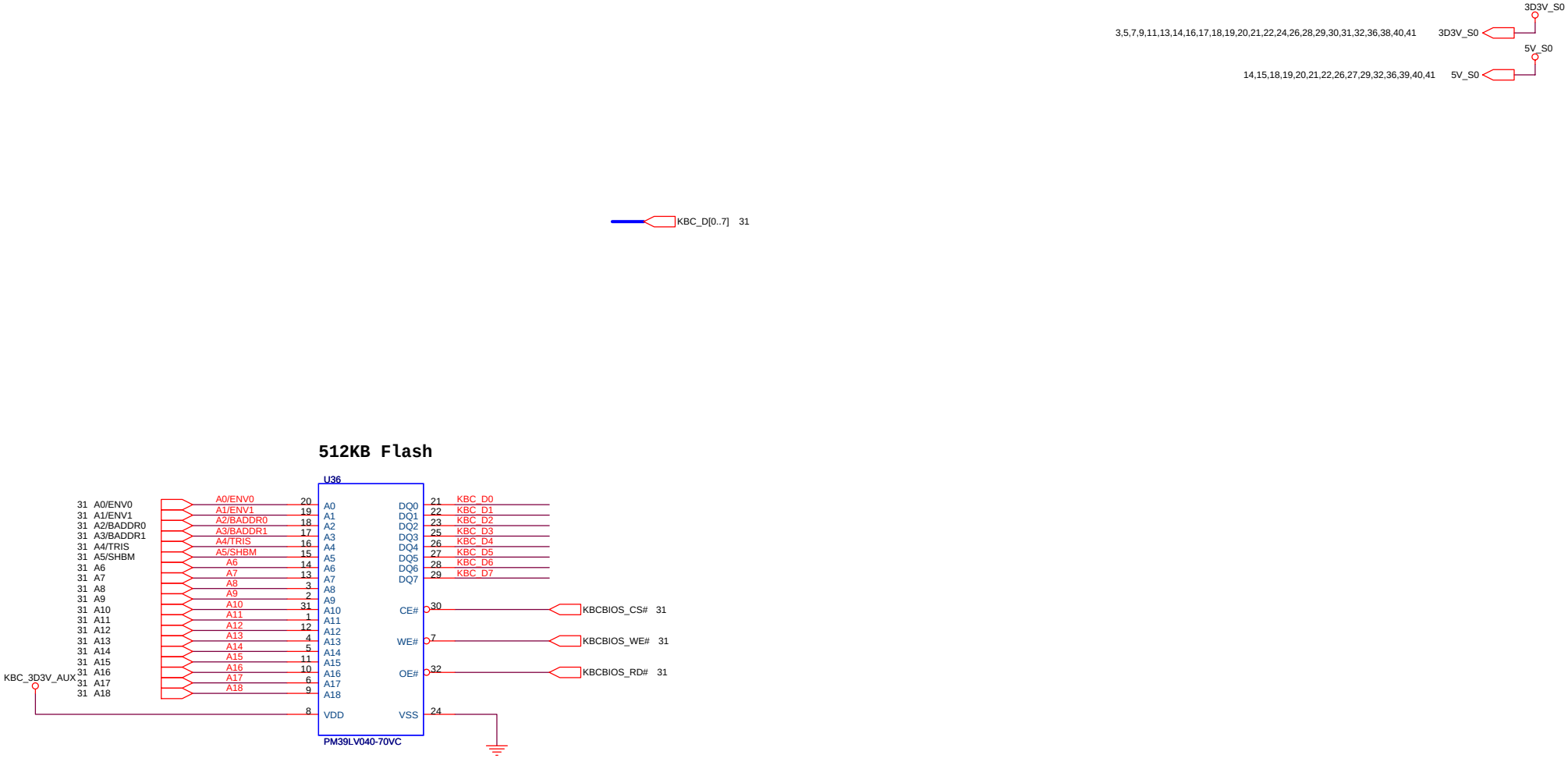

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***BIOS/GF***	
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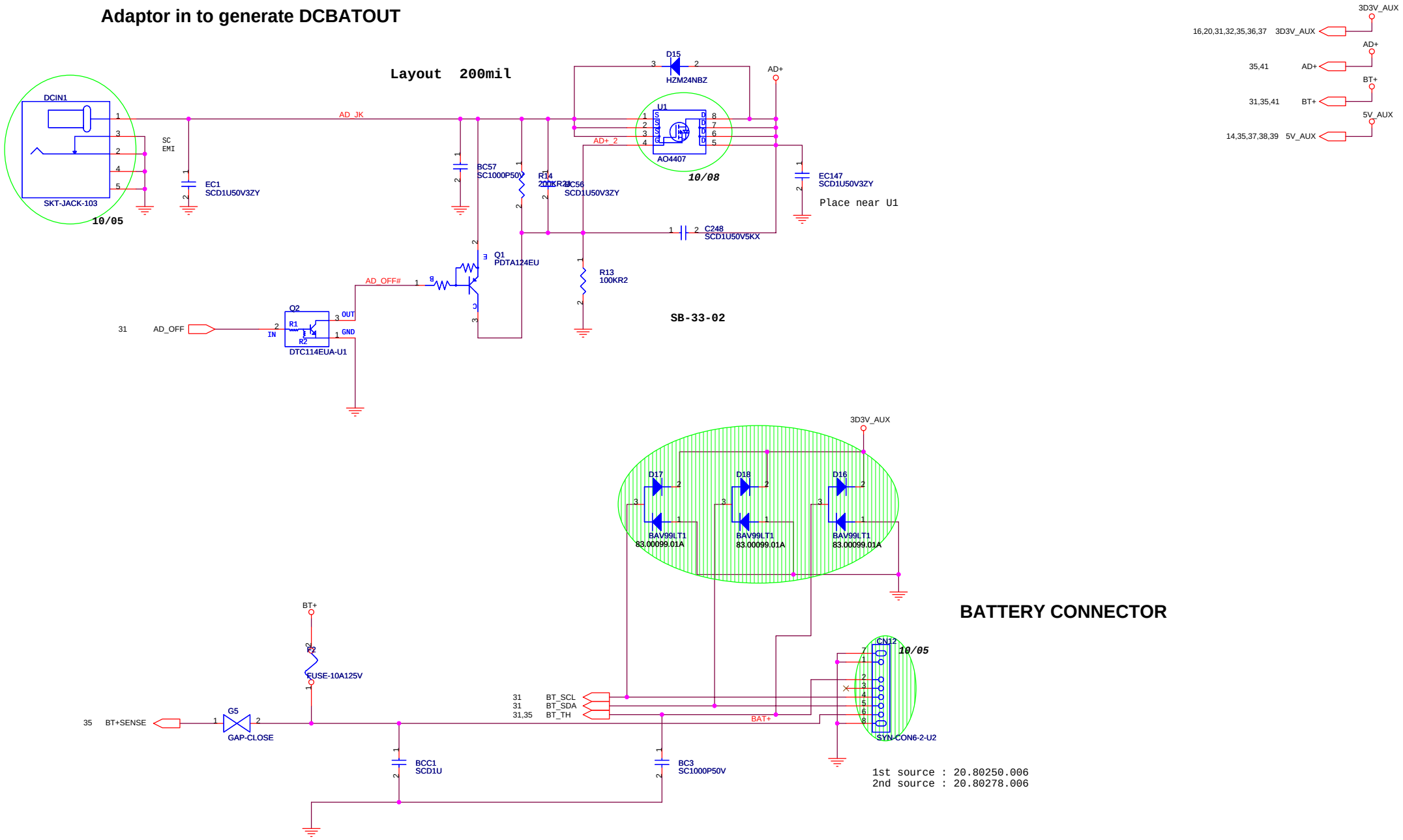
Adaptor in to generate DCBATOUT



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Title	***Adaptor/ Bettery conn.***	
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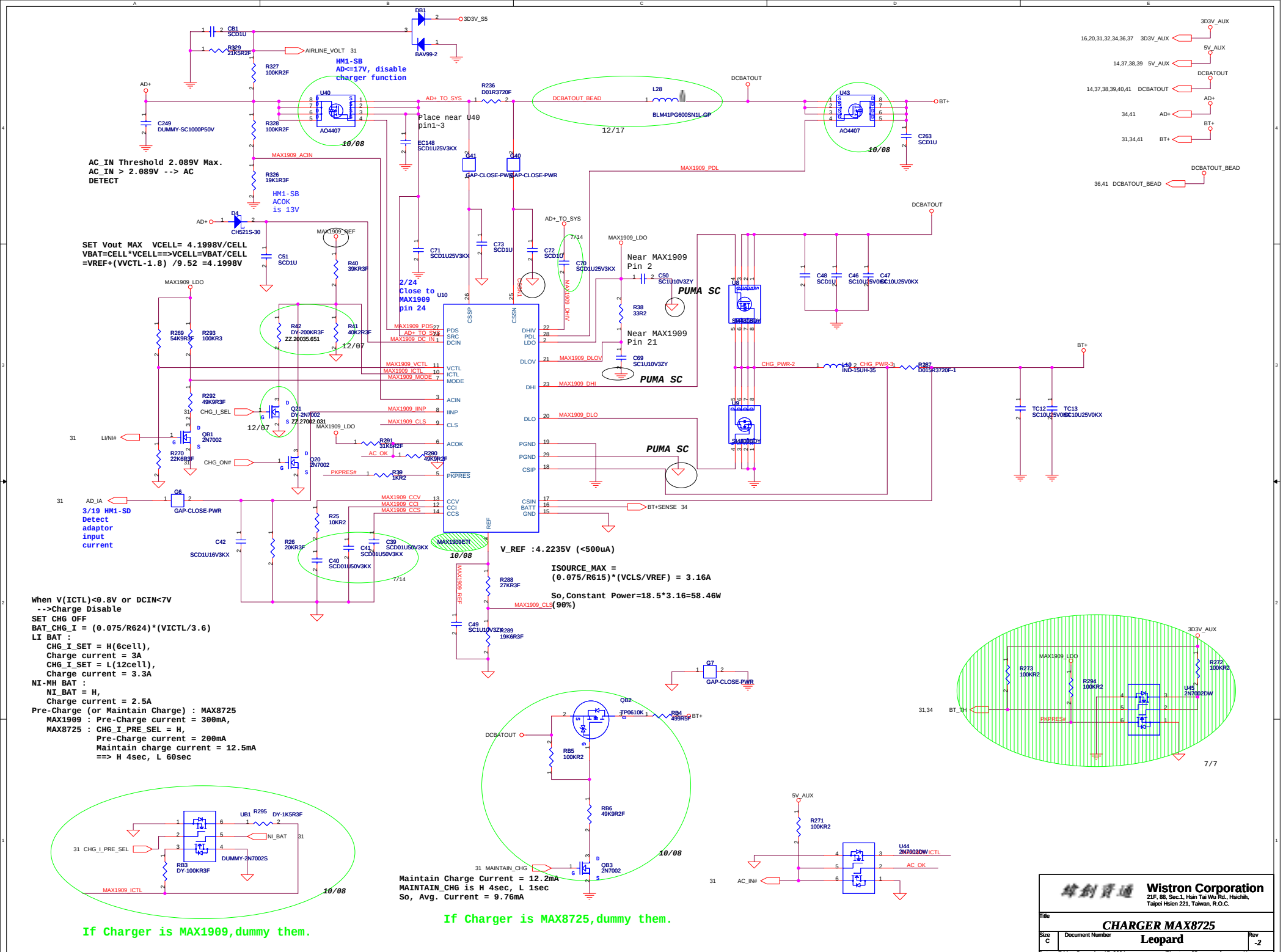
HM1-SB
AD<=17V, disable
charger function
AC_IN Threshold 2.089V Max.
AC_IN > 2.089V --> AC
DETECT
HM1-SB
ACOK
is 13V
SET Vout MAX VCELL= 4.1998V/CELL
VBAT=CELL*VCELL==>VCELL=VBAT/CELL
=VREF+(VVCTL-1.8) /9.52 =4.1998V
Place near U40
pin1~3
2/24
Close to
MAX1909
pin 24
Near MAX1909
Pin 2
Near MAX1909
Pin 21
PUMA SC
PUMA SC
PUMA SC
3/19 HM1-SD
Detect
adaptor
input
current
V_REF :4.2235V (<500uA)
ISOURCE_MAX =
(0.075/R615)*(VCLS/VREF) = 3.16A
So,Constant Power=18.5*3.16=58.46W
(90%)
When V(ICTL)<0.8V or DCIN<7V
-->Charge Disable
SET CHG OFF
BAT_CHG_I = (0.075/R624)*(VICTL/3.6)
LI BAT :
CHG_I_SET = H(6cell),
Charge current = 3A
CHG_I_SET = L(12cell),
Charge current = 3.3A
NI-MH BAT :
NI_BAT = H,
Charge current = 2.5A
Pre-Charge (or Maintain Charge) : MAX8725
MAX1909 : Pre-Charge current = 300mA,
MAX8725 : CHG_I_PRE_SEL = H,
Pre-Charge current = 200mA
Maintain charge current = 12.5mA
==> H 4sec, L 60sec
Maintain Charge Current = 12.2mA
MAINTAIN_CHG is H 4sec, L 1sec
So, Avg. Current = 9.76mA
If Charger is MAX1909,dummy them.
If Charger is MAX8725,dummy them.
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Title
CHARGER MAX8725
Size C
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Leopard
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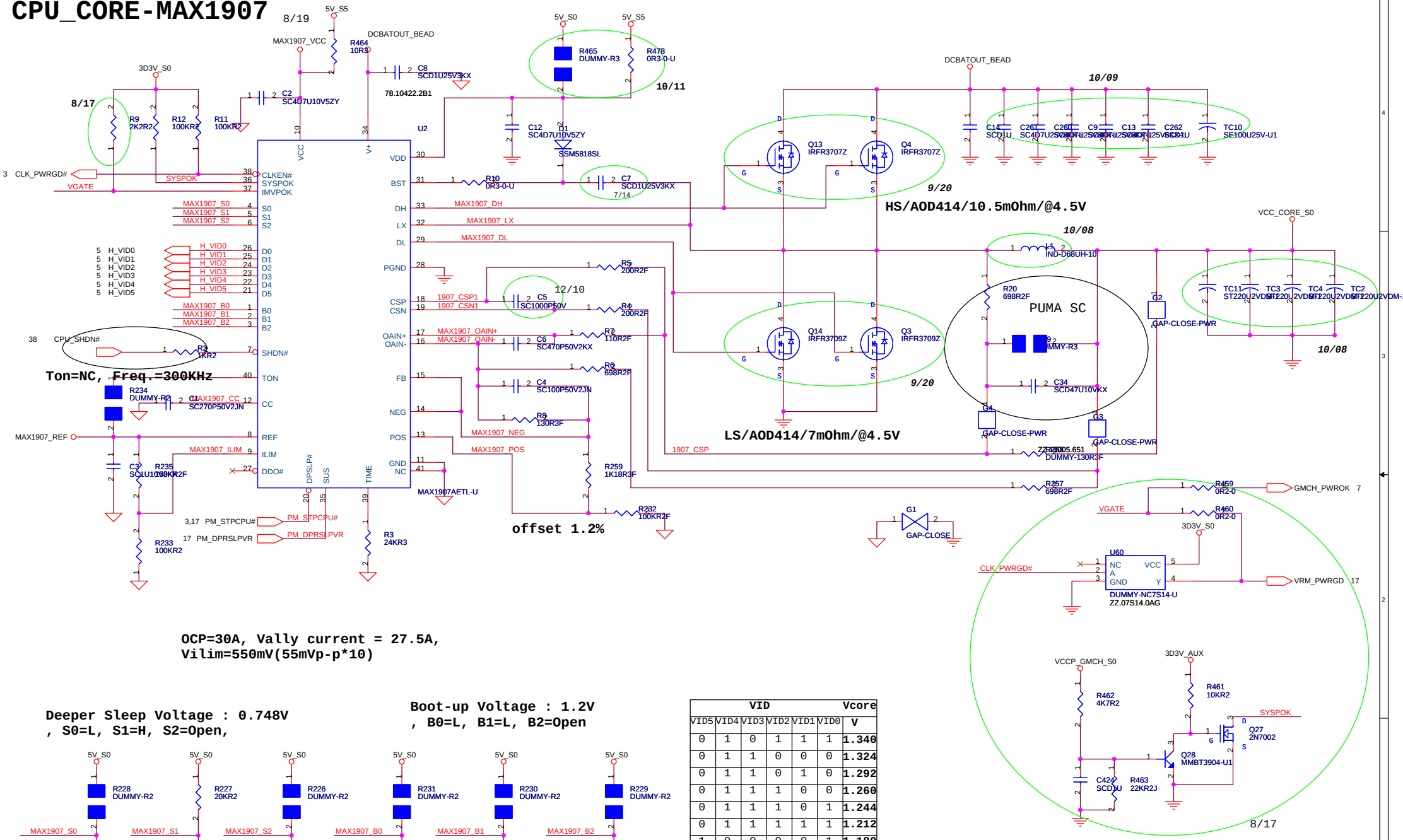
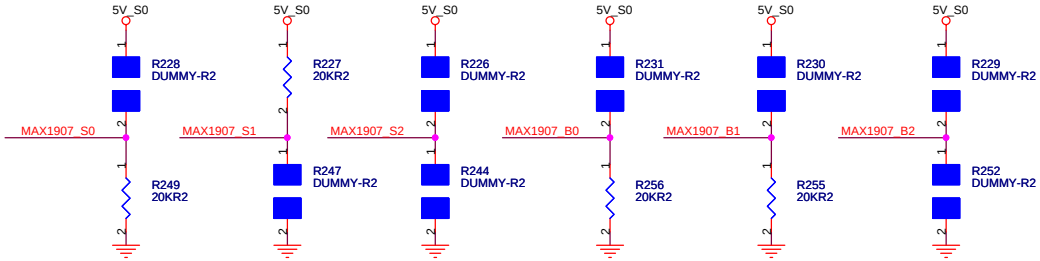
CPU_CORE-MAX1907



OCP=30A, Vally current = 27.5A,
Vilim=550mV(55mVp-p*10)

Deeper Sleep Voltage : 0.748V
, S0=L, S1=H, S2=Open,

Boot-up Voltage : 1.2V
, B0=L, B1=L, B2=Open



VID						Vcore
VID5	VID4	VID3	VID2	VID1	VID0	V
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	1	0	1.292
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	1	1.212
1	0	0	0	0	1	1.180
1	0	0	0	1	1	1.148
1	0	0	1	1	0	1.100
1	0	1	0	0	1	1.052
1	0	1	0	1	1	1.020
1	0	1	1	1	0	0.972
1	1	0	0	0	0	0.940

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Title: IMVP IV-CPU POWER-MAX1907

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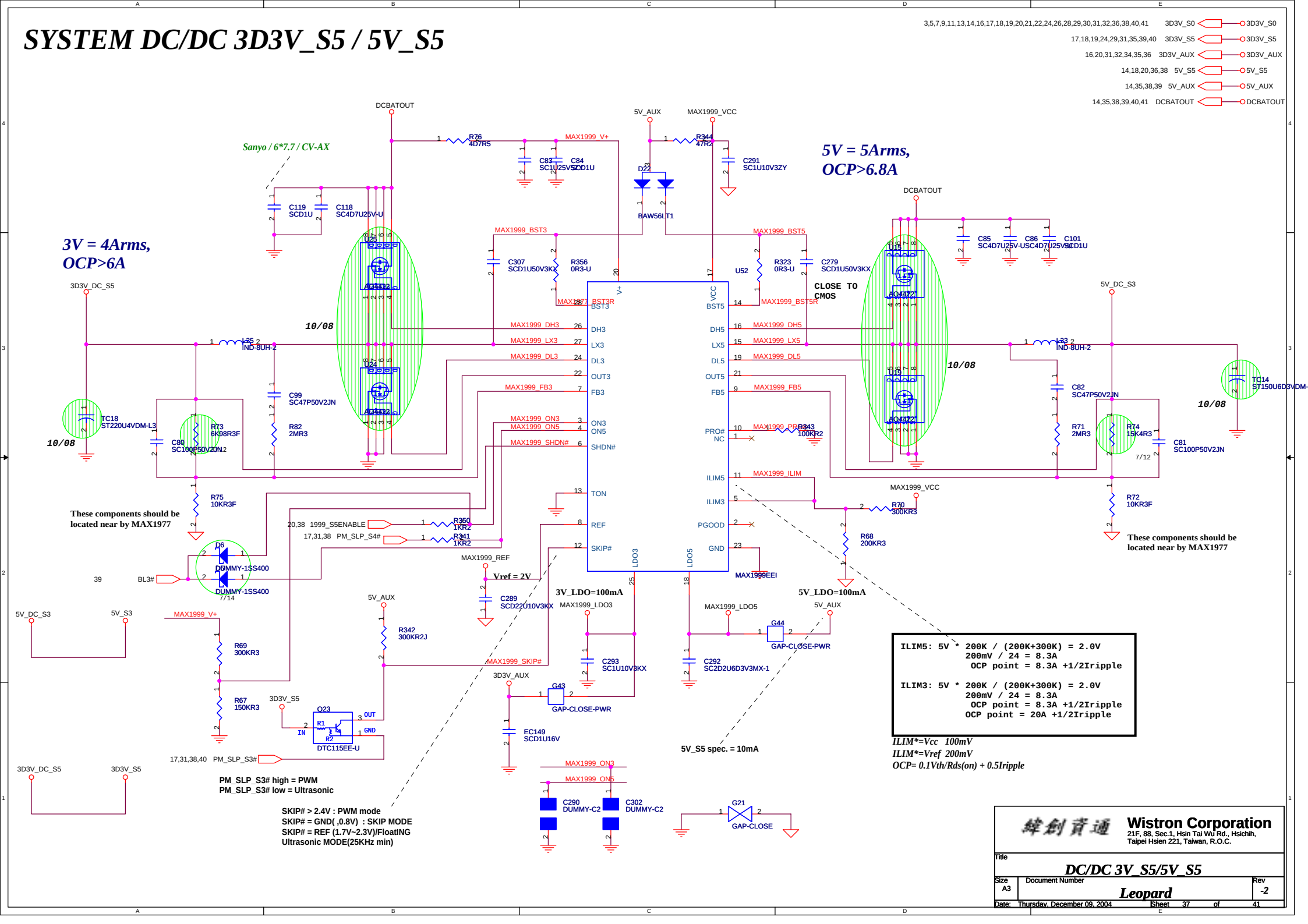
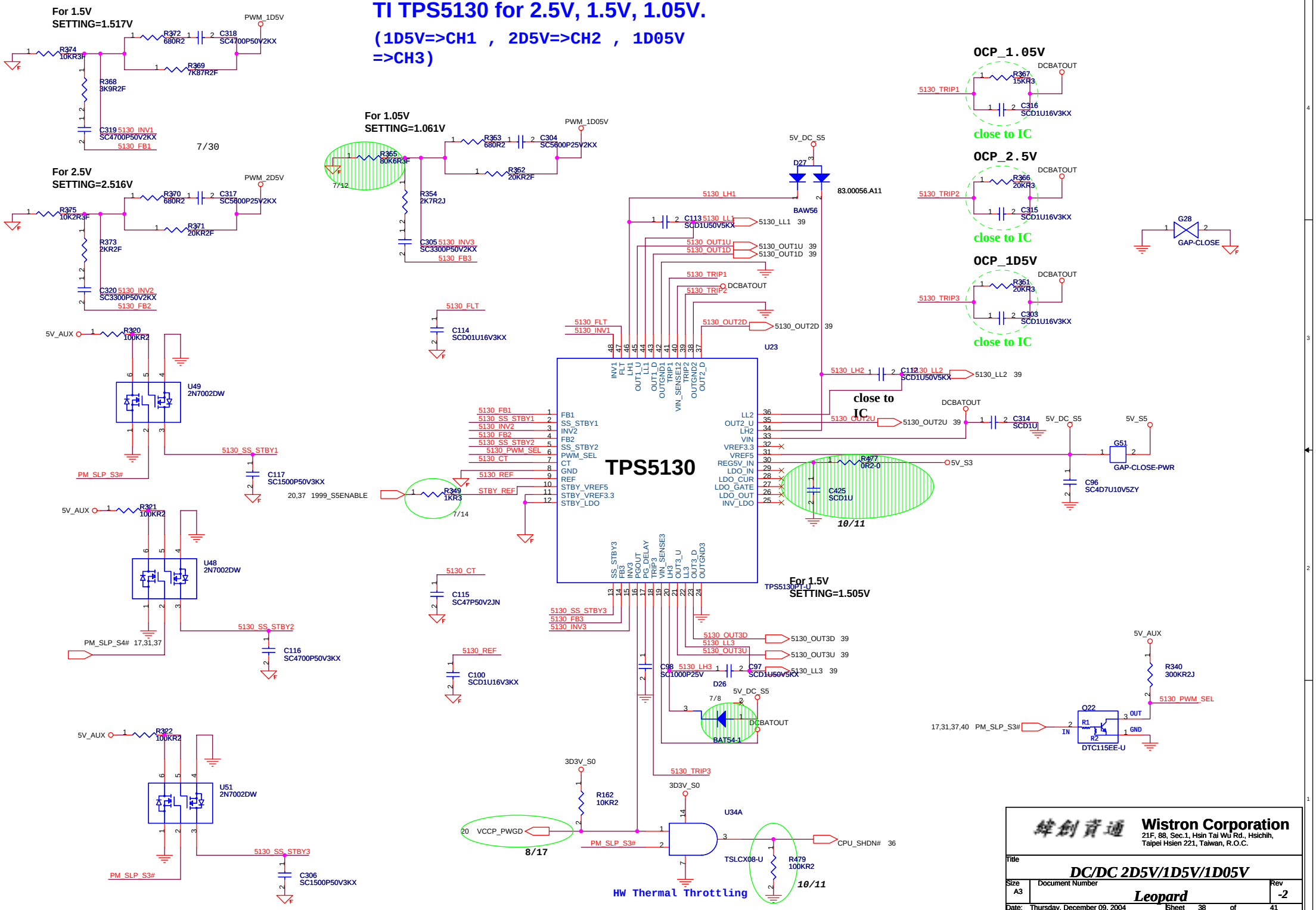
SYSTEM DC/DC 3D3V_S5 / 5V_S5



TI TPS5130 for 2.5V, 1.5V, 1.05V.

(1D5V=>CH1 , 2D5V=>CH2 , 1D05V =>CH3)



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Title	*DC/DC 2D5V/1D5V/1D05V*	
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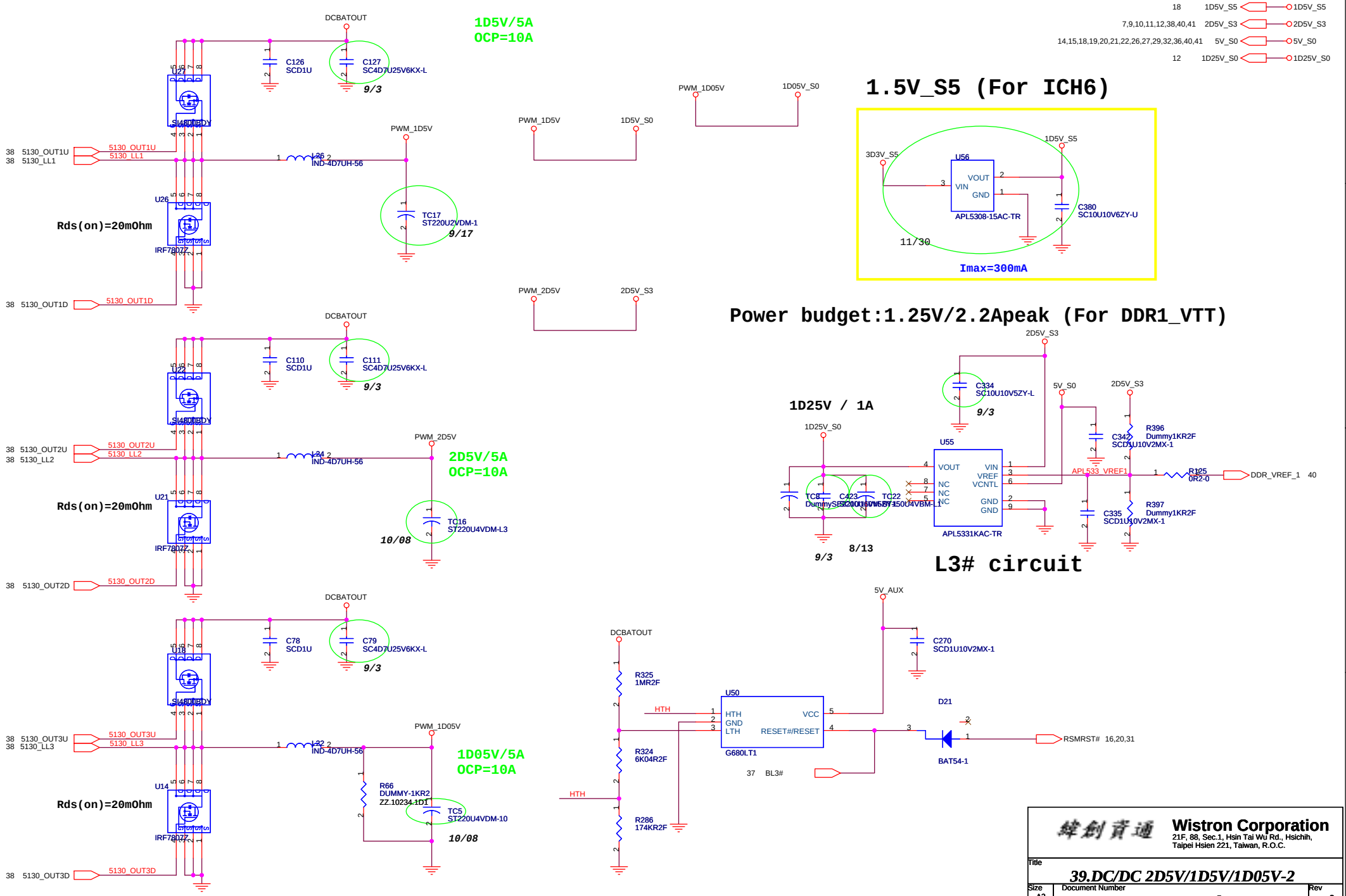
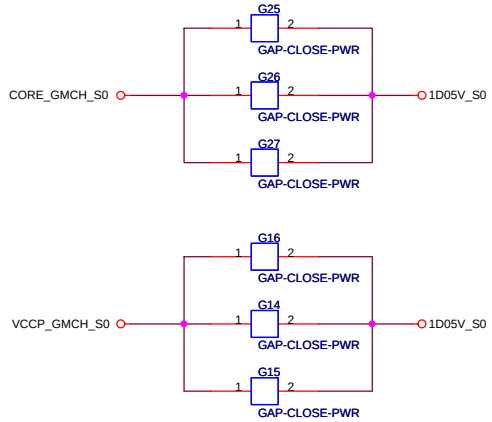
TI TPS5130 for 2.5V, 1.5V, 1.05V

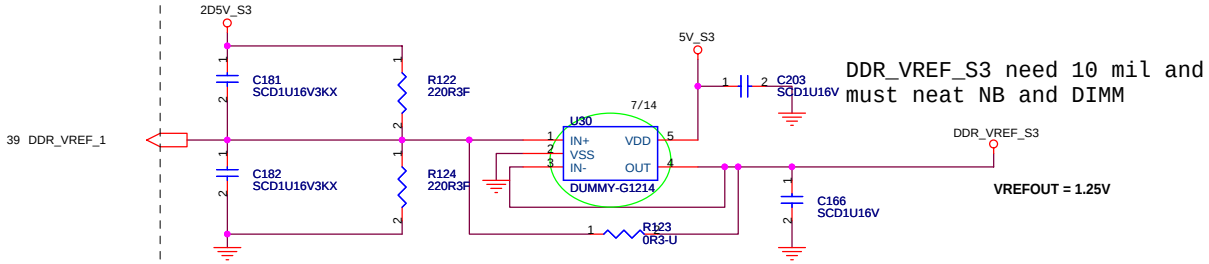
(2D5V=>CH1 , 3D3V=>CH2 , 5V =>CH3)



FOR GMCH Power



3,5,7,9,11,13,14,16,17,18,19,20,21,22,24,26,28,29,30,31,32,36,38,41 3D3V_S0 — 3D3V_S0
28,30 3D3V_S3 — 3D3V_S3
17,18,19,24,29,31,35,37,39 3D3V_S5 — 3D3V_S5
14,15,18,19,20,21,22,26,27,29,32,36,39,41 5V_S0 — 5V_S0
14,25,30,32,37,38,41 5V_S3 — 5V_S3
14,18,20,36,38 5V_S5 — 5V_S5
7,9,15,18 2D5V_S0 — 2D5V_S0
7,9,10,11,12,38,39,41 2D5V_S3 — 2D5V_S3
7,11 DDR_VREF_S3 — DDR_VREF_S3
14,35,37,38,39,41 DCBATOUT — DCBATOUT
38,39,41 1D05V_S0 — 1D05V_S0
4,5,6,7,9,10,16,18,36,41 VCCP_GMCH_S0 — VCCP_GMCH_S0
6,9,10,41 CORE_GMCH_S0 — CORE_GMCH_S0

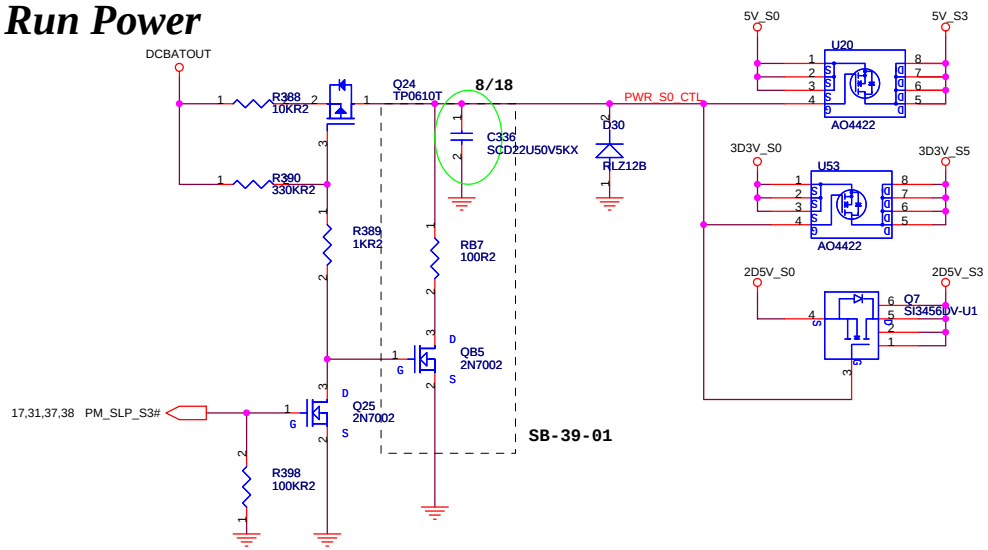


DDR_VREF_S3 need 10 mil and must neat NB and DIMM

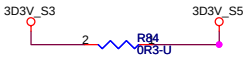
VREFOUT = 1.25V

FOR DDR Power

Run Power



Suspend Power



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Title: PWRPLANE&RESETLOGIC

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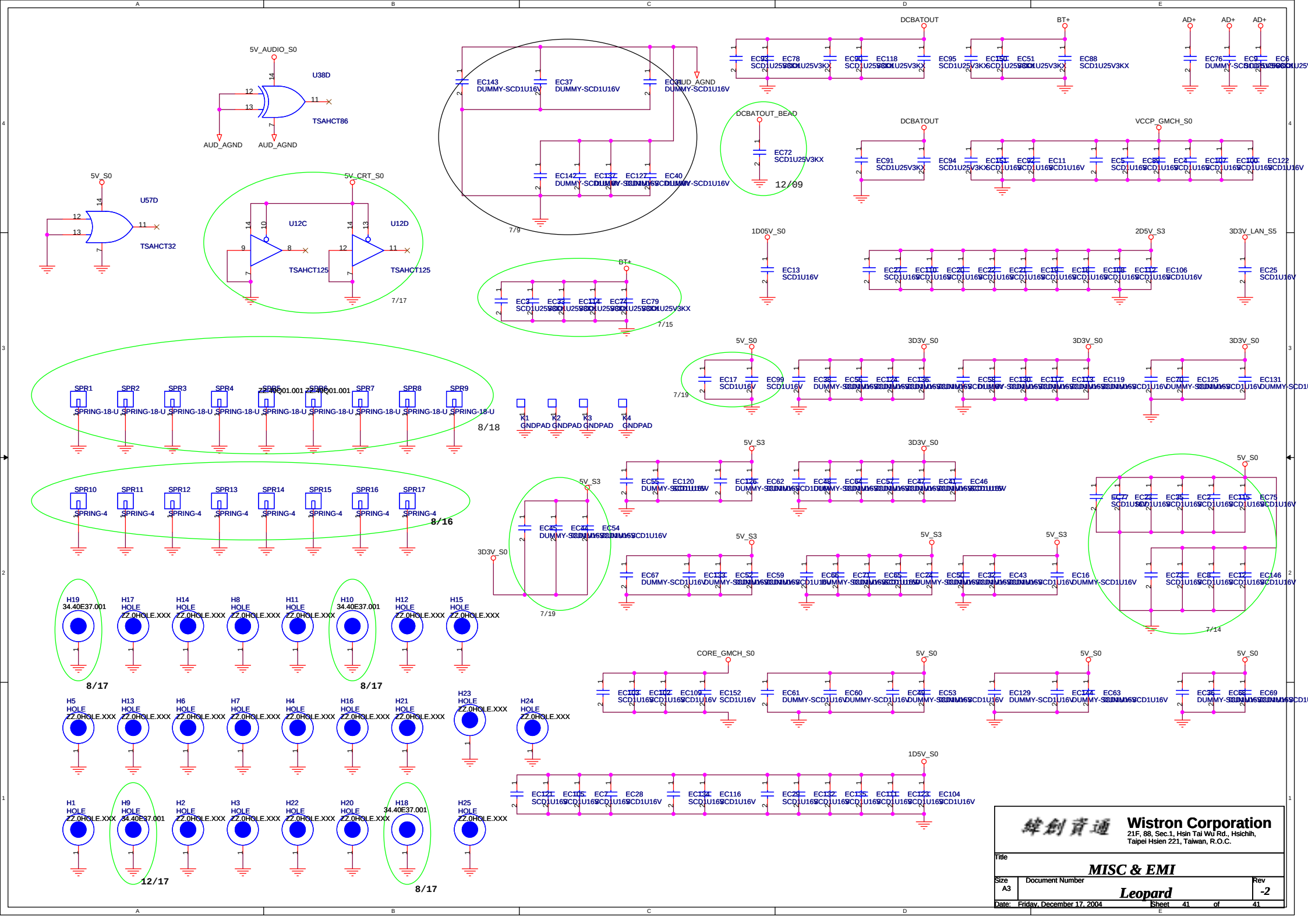
5V_AUDIO_S0
U38D
TSAHCT86
AUD_AGND
AUD_AGND
5V_S0
U57D
TSAHCT32
5V_CRT_S0
U12C
U12D
TSAHCT125
TSAHCT125
7/17
EC143 DUMMY-SCD1U16V
EC37 DUMMY-SCD1U16V
AUD_AGND
7/9
DCBATOUT
BT+
AD+
AD+
AD+
EC95 SCD1U25V3KX
EC88 SCD1U25V3KX
EC76 DUMMY-SCD1U16V
DCBATOUT_BEAD
EC72 SCD1U25V3KX
12/09
DCBATOUT
VCCP_GMCH_S0
EC91 SCD1U25V3KX
EC94 SCD1U25V3KX
EC122 SCD1U16V
1D05V_S0
EC13 SCD1U16V
2D5V_S3
EC106 SCD1U16V
3D3V_LAN_S5
EC25 SCD1U16V
BT+
EC79 SCD1U25V3KX
7/15
5V_S0
3D3V_S0
3D3V_S0
3D3V_S0
EC17 SCD1U16V
EC99 SCD1U16V
EC131
7/19
SPR1 SPR2 SPR3 SPR4 SPR5 SPR6 SPR7 SPR8 SPR9
SPRING-18-U
8/18
K1 K2 K3 K4
GNDPAD
5V_S3
3D3V_S0
EC46
5V_S0
EC75 SCD1U16V
SPR10 SPR11 SPR12 SPR13 SPR14 SPR15 SPR16 SPR17
SPRING-4
8/16
5V_S3
3D3V_S0
7/19
5V_S3
5V_S3
5V_S3
EC16 DUMMY-SCD1U16V
7/14
H19 34.40E37.001
H17 HOLE ZZ.0HOLE.XXX
H14 HOLE ZZ.0HOLE.XXX
H8 HOLE ZZ.0HOLE.XXX
H11 HOLE ZZ.0HOLE.XXX
H10 34.40E37.001
H12 HOLE ZZ.0HOLE.XXX
H15 HOLE ZZ.0HOLE.XXX
8/17
8/17
CORE_GMCH_S0
5V_S0
5V_S0
5V_S0
EC152 SCD1U16V
EC69
H5 HOLE ZZ.0HOLE.XXX
H13 HOLE ZZ.0HOLE.XXX
H6 HOLE ZZ.0HOLE.XXX
H7 HOLE ZZ.0HOLE.XXX
H4 HOLE ZZ.0HOLE.XXX
H16 HOLE ZZ.0HOLE.XXX
H21 HOLE ZZ.0HOLE.XXX
H23 HOLE ZZ.0HOLE.XXX
H24 HOLE ZZ.0HOLE.XXX
1D5V_S0
EC104 SCD1U16V
H1 HOLE ZZ.0HOLE.XXX
H9 HOLE 34.40E37.001
H2 HOLE ZZ.0HOLE.XXX
H3 HOLE ZZ.0HOLE.XXX
H22 HOLE ZZ.0HOLE.XXX
H20 HOLE ZZ.0HOLE.XXX
H18 34.40E37.001
H25 HOLE ZZ.0HOLE.XXX
12/17
8/17
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Title
MISC & EMI
Size A3
Document Number
Leopard
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