

Compal confidential

Schematics Document

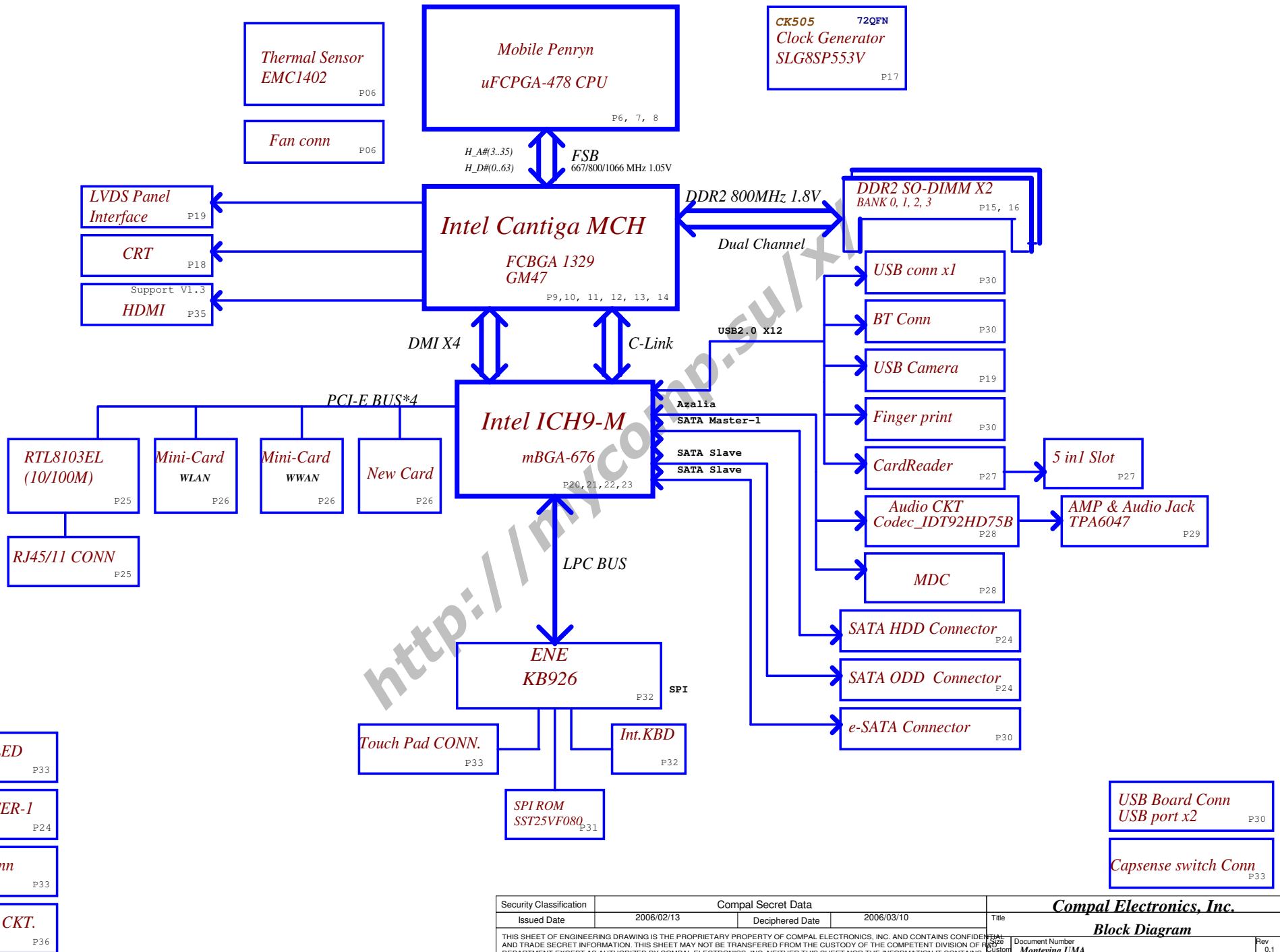
Mobile Penryn uFCPGA with Intel
Cantiga_GM+ICH9-M core logic

2009-02-16

REV:1.0

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	產出日期	
	解密日期	

Security Classification	Compal Secret Data			Title	
Issued Date	2007/08/28	Deciphered Date	2006/03/10	Cover Sheet	
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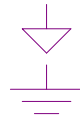


Voltage Rails

O MEANS ON X MEANS OFF

power plane State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +0.75V +VCCP +CPU_CORE +2.5VS +1.8V
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note:



: means Digital Ground



: means Analog Ground

@ :	means just reserve , no build
45@ :	means need be mounted when 45 level assy or rework stage.
DEBUG@ :	means just reserve for debug.
BATT @ :	means need be mounted when 45 level assy or rework stage.
CONN@ :	means ME part
ESATA @ :	means just reserve for ESATA
GS @ :	means just reserve for G sensor
FP @ :	means just reserve for Finger Print
Multi @ :	means just reserve for Multi Bay
NewC@ :	means just reserve for New card
Main@ :	means just reserve for Main stream
OPP@ :	means just reserve for OPP
2MiniC@ :	means just reserve for 2nd Mini card slot
PA @ :	means just reserve for PA
PR @ :	means just reserve for PR

USB assignment:

USB-0	Right side(with eSATA)
USB-1	Left side
USB-2	Left side
USB-3	Cardreader
USB-4	Camera
USB-5	WLAN
USB-6	Bluetooth
USB-7	Finger Printer
USB-8	MiniCard(WWAN/TV)
USB-9	Express card
USB-10	X
USB-11	X

PCIe assignment:

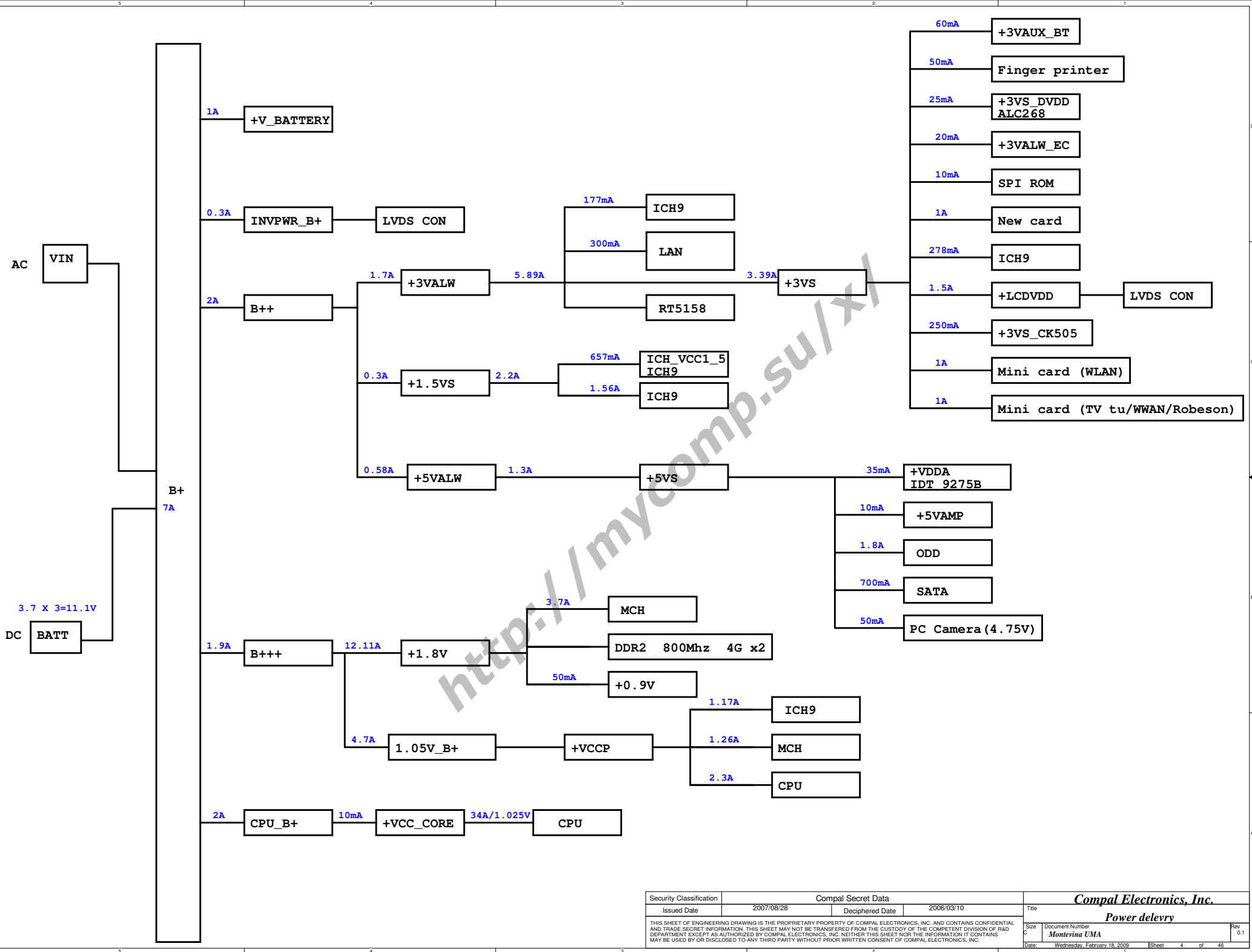
PCIe-1	WWAN
PCIe-2	X
PCIe-3	WLAN
PCIe-4	GLAN (Realtek)
PCIe-5	X
PCIe-6	New Card

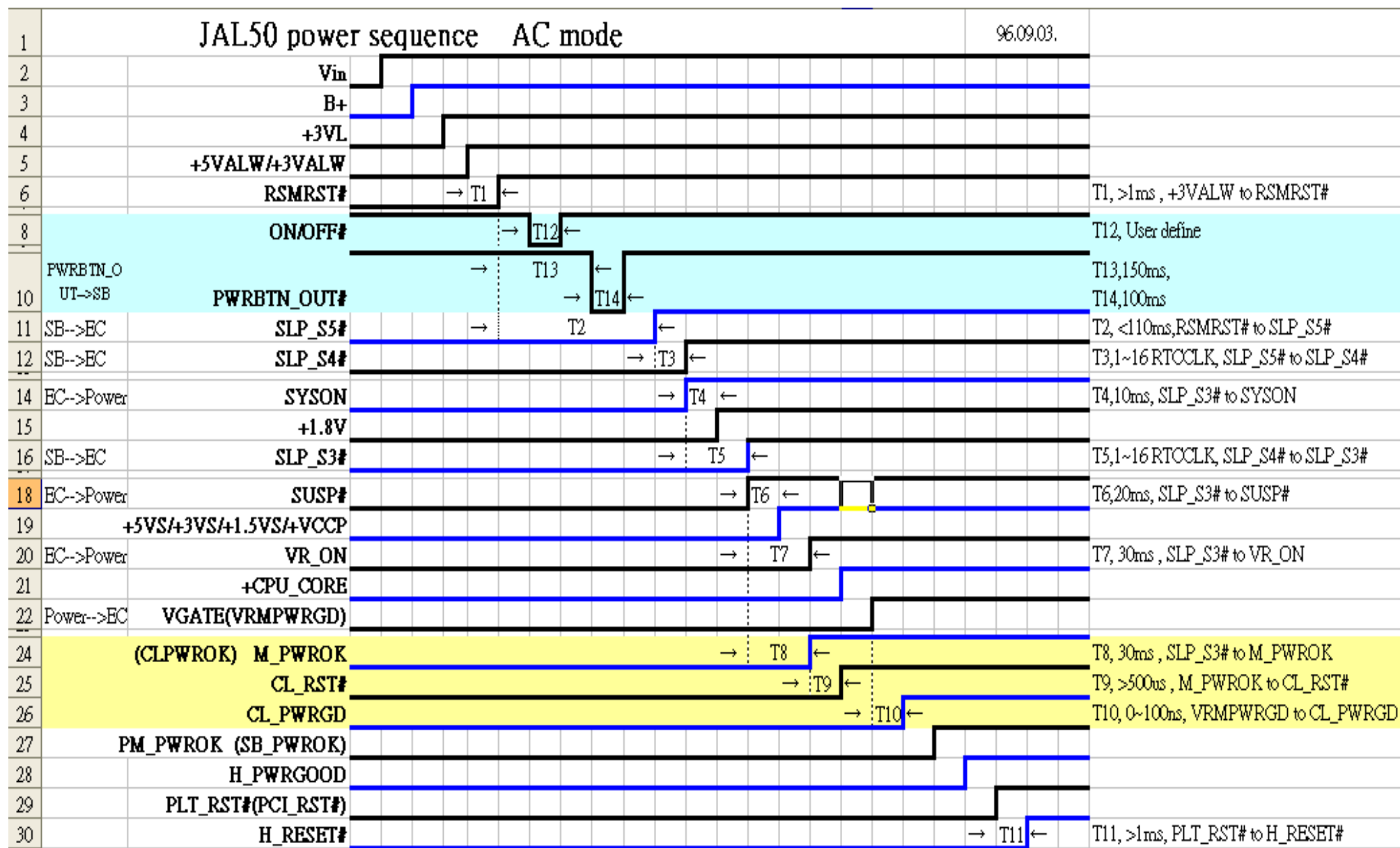
I2C / SMBUS ADDRESSING

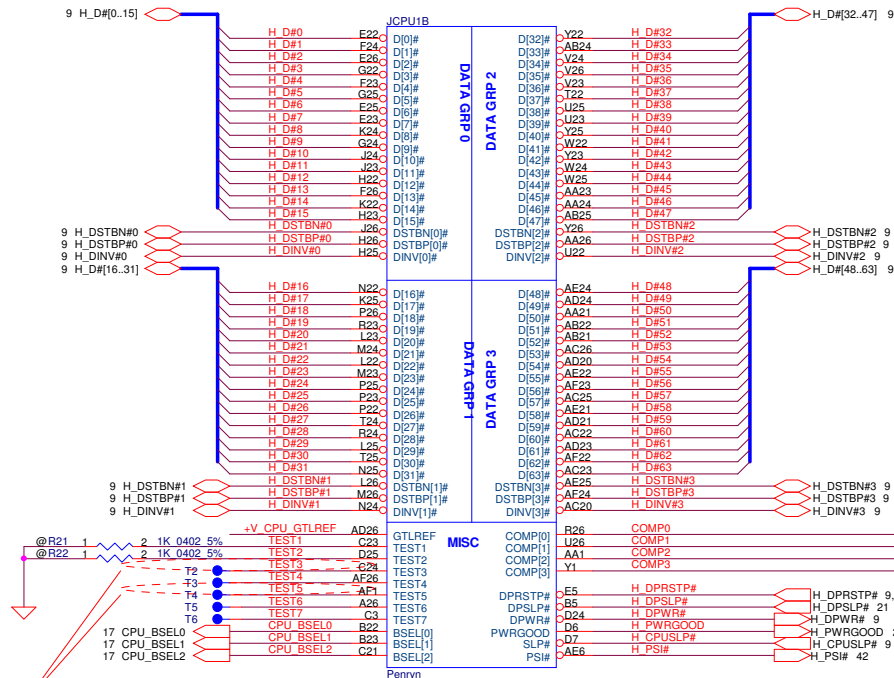
DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10 100 000
DDR SO-DIMM 1	A4	10 100 100
CLOCK GENERATOR (EXT.)	D2	11 010 010

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK CHIP	MINI CARD	LCD	Cap sensor board	NEW CARD	G sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	V	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X	X	V	V
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V	X	X	X

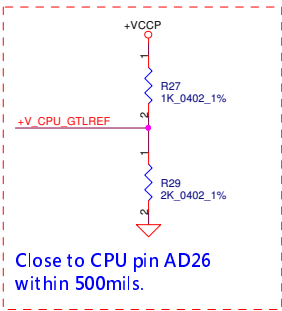




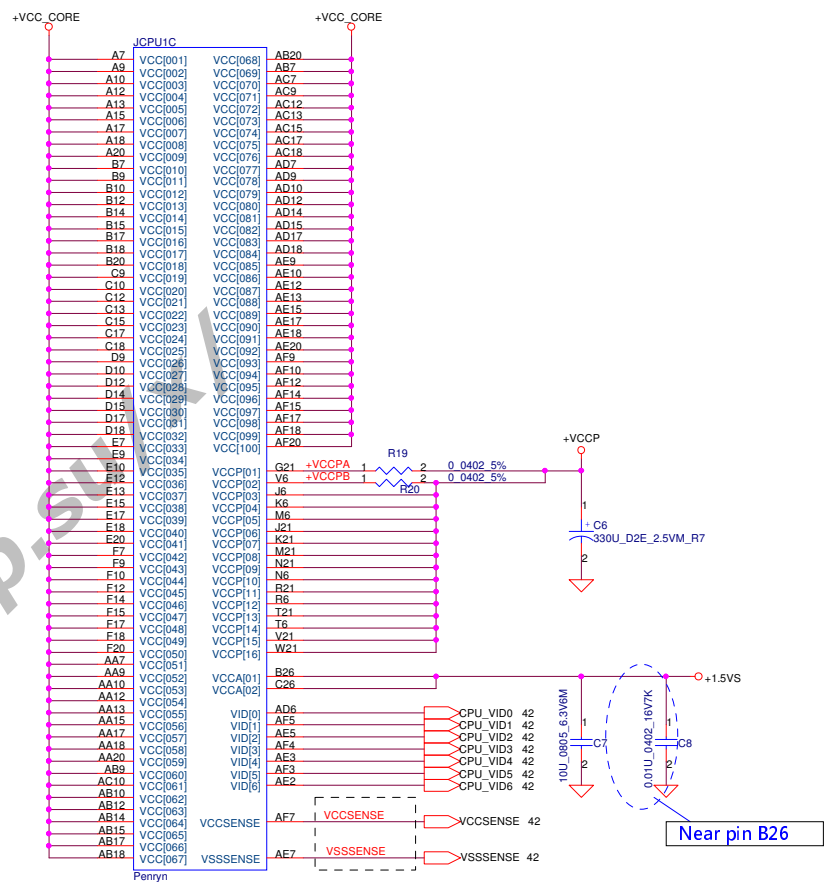


* Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

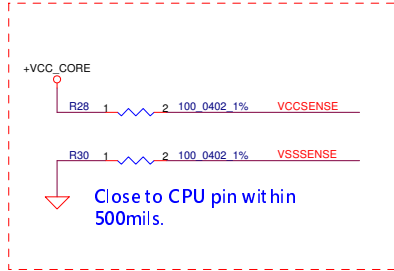
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



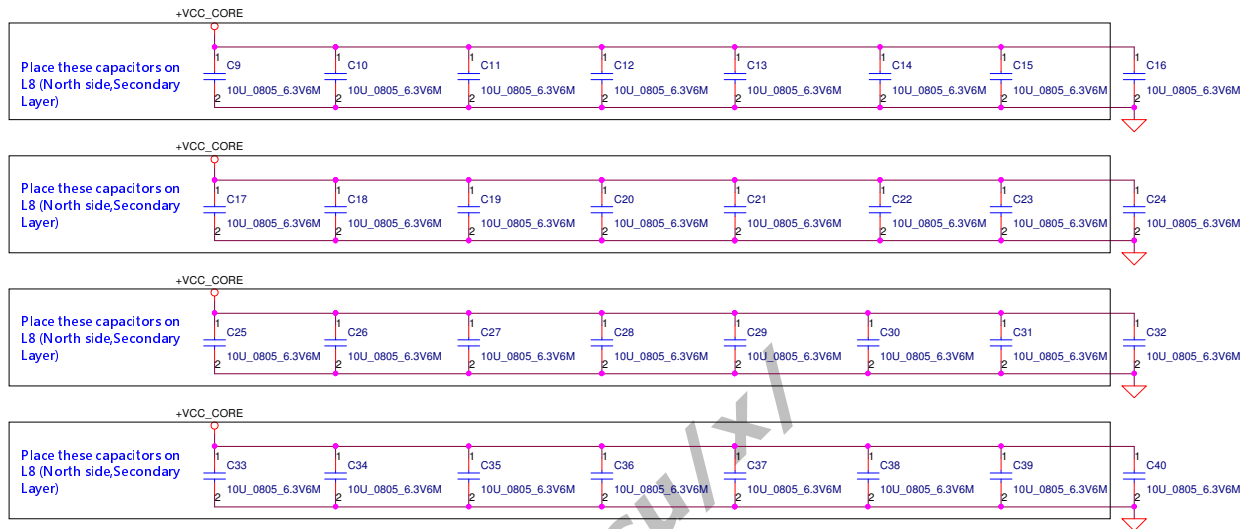
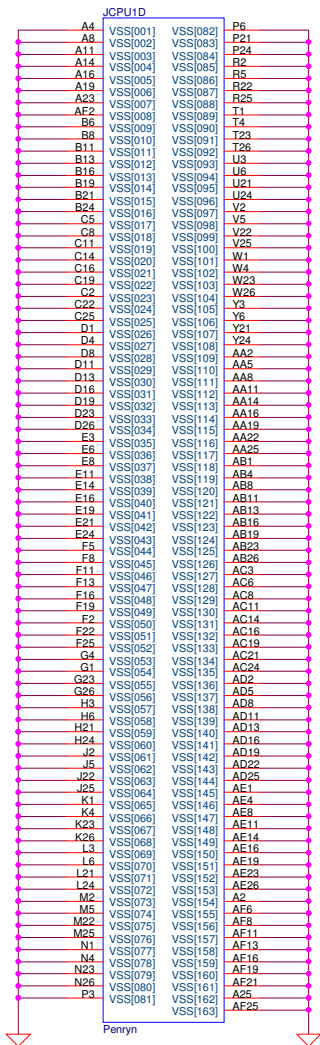
Close to CPU pin AD26 within 500mils.



Length match within 25 mils. The trace width/space/other is 20/7/25.



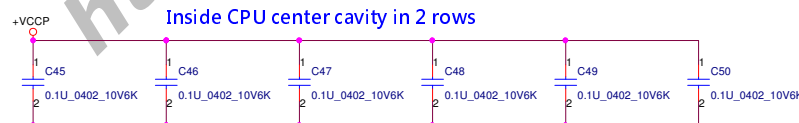
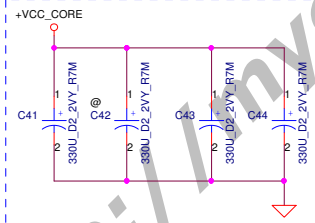
Close to CPU pin within 500mils.



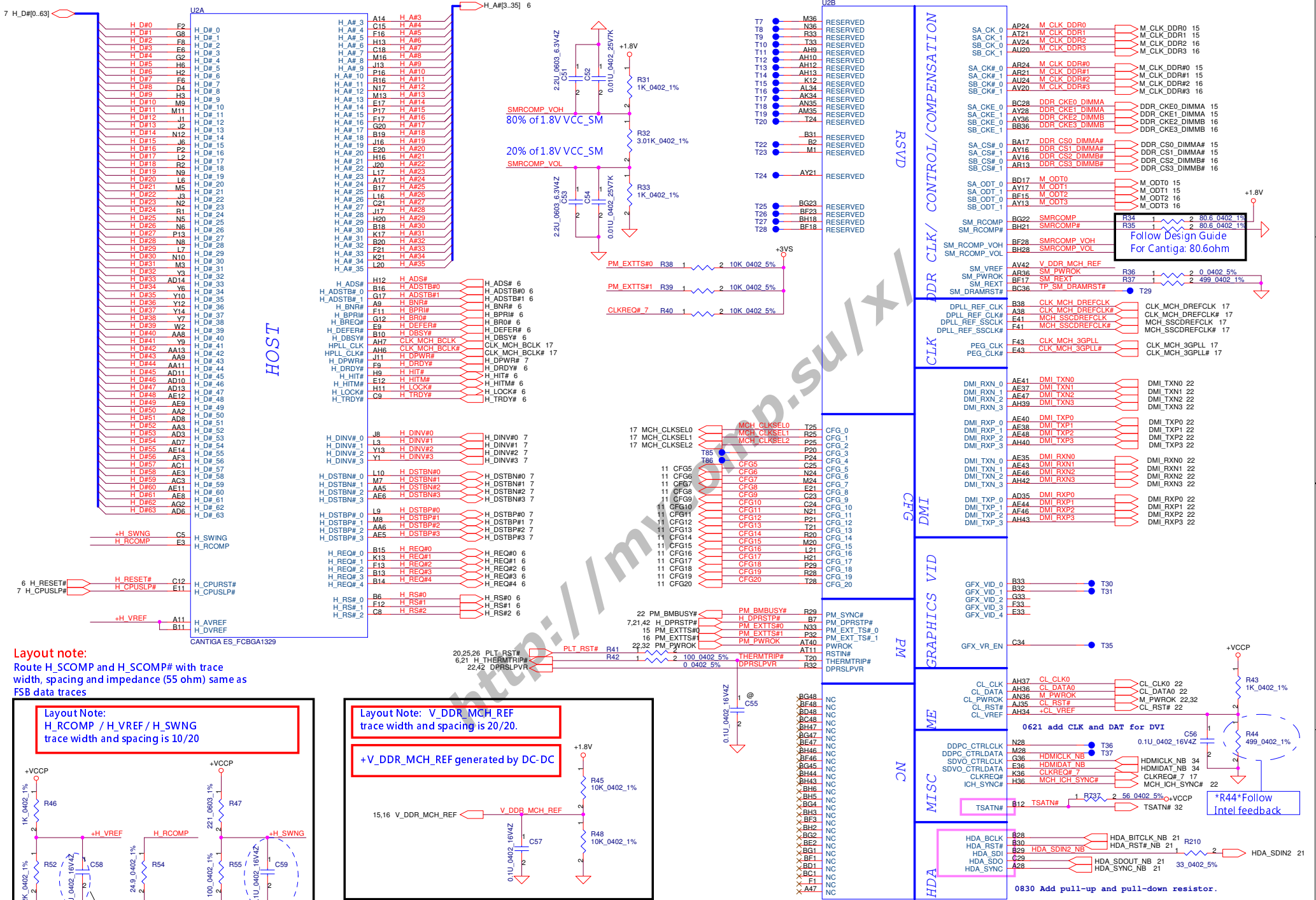
Mid Frequency Decoupling

Near CPU CORE regulator

ESR <= 1.5m ohm
Capacitor > 1980uF



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Layout note:
Route H_SCOMP and H_SCOMP# with trace
width, spacing and impedance (55 ohm) same as
FSB data traces

Layout Note:
H_RESET# / H_VREF / H_SWNG
trace width and spacing is 10/20

Layout Note: V_DDR_MCH_REF
trace width and spacing is 20/20.

+V_DDR_MCH_REF generated by DC-DC

Compal Secret Data

Compal Electronics, Inc.

Cantiga(1/6)-AGTL/DMI/DDR

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15 DDR_A_D[0..63]

U2D

DDR A D0 AJ38 SA_DQ_0
DDR A D1 AM41 SA_DQ_1
DDR A D2 AN38 SA_DQ_2
DDR A D3 AJ36 SA_DQ_3
DDR A D4 AJ36 SA_DQ_3
DDR A D5 AJ40 SA_DQ_4
DDR A D6 AM44 SA_DQ_6
DDR A D7 AM42 SA_DQ_7
DDR A D8 AM42 SA_DQ_7
DDR A D9 AN44 SA_DQ_8
DDR A D10 AU40 SA_DQ_10
DDR A D11 AT38 SA_DQ_11
DDR A D12 AN41 SA_DQ_11
DDR A D13 AN39 SA_DQ_12
DDR A D14 AU44 SA_DQ_14
DDR A D15 AU42 SA_DQ_15
DDR A D16 AV39 SA_DQ_17
DDR A D17 AY44 SA_DQ_16
DDR A D18 BA40 SA_DQ_18
DDR A D19 BD43 SA_DQ_19
DDR A D20 AV41 SA_DQ_20
DDR A D21 AV43 SA_DQ_21
DDR A D22 BB41 SA_DQ_22
DDR A D23 BC40 SA_DQ_23
DDR A D24 AV37 SA_DQ_24
DDR A D25 BD38 SA_DQ_25
DDR A D26 AV37 SA_DQ_26
DDR A D27 AT36 SA_DQ_27
DDR A D28 AV38 SA_DQ_28
DDR A D29 BB38 SA_DQ_29
DDR A D30 AV36 SA_DQ_30
DDR A D31 AW36 SA_DQ_31
DDR A D32 BD13 SA_DQ_32
DDR A D33 AU11 SA_DQ_34
DDR A D34 BC11 SA_DQ_35
DDR A D35 BA12 SA_DQ_36
DDR A D36 AU13 SA_DQ_37
DDR A D37 AV13 SA_DQ_38
DDR A D38 BD12 SA_DQ_39
DDR A D39 BC12 SA_DQ_40
DDR A D40 BB9 SA_DQ_41
DDR A D41 BA9 SA_DQ_42
DDR A D42 AU10 SA_DQ_43
DDR A D43 AV9 SA_DQ_44
DDR A D44 BA11 SA_DQ_45
DDR A D45 BD9 SA_DQ_46
DDR A D46 AV8 SA_DQ_47
DDR A D47 BA6 SA_DQ_48
DDR A D48 AV5 SA_DQ_49
DDR A D49 AT9 SA_DQ_50
DDR A D50 AT9 SA_DQ_51
DDR A D51 AN8 SA_DQ_52
DDR A D52 AU5 SA_DQ_53
DDR A D53 AU6 SA_DQ_54
DDR A D54 AT5 SA_DQ_55
DDR A D55 AN10 SA_DQ_56
DDR A D56 AM11 SA_DQ_57
DDR A D57 AM5 SA_DQ_58
DDR A D58 AJ9 SA_DQ_59
DDR A D59 AJ8 SA_DQ_60
DDR A D60 AN12 SA_DQ_61
DDR A D61 AM13 SA_DQ_62
DDR A D62 AJ11 SA_DQ_63
DDR A D63 AJ12 SA_DQ_63

DDR SYSTEM MEMORY A

CANTIGA ES_FCBGA1329

SA_BS_0
SA_BS_1
SA_BS_2
SA_RAS#
SA_CAS#
SA_WE#

SA_DM_0
SA_DM_1
SA_DM_2
SA_DM_3
SA_DM_4
SA_DM_5
SA_DM_6
SA_DM_7

SA_DQS_0
SA_DQS_1
SA_DQS_2
SA_DQS_3
SA_DQS_4
SA_DQS_5
SA_DQS_6
SA_DQS_7

SA_DQS#_0
SA_DQS#_1
SA_DQS#_2
SA_DQS#_3
SA_DQS#_4
SA_DQS#_5
SA_DQS#_6
SA_DQS#_7

SA_MA_0
SA_MA_1
SA_MA_2
SA_MA_3
SA_MA_4
SA_MA_5
SA_MA_6
SA_MA_7
SA_MA_8
SA_MA_9
SA_MA_10
SA_MA_11
SA_MA_12
SA_MA_13
SA_MA_14

BD21 DDR A BS0
BG18 DDR A BS1
AT25 DDR A BS2

BB20 DDR A RAS#
BD20 DDR A CAS#
AY20 DDR A WE#

AM37 DDR A DM0
AT41 DDR A DM1
AY41 DDR A DM2
AU39 DDR A DM3
BB12 DDR A DM4
AY6 DDR A DM5
AT7 DDR A DM6
AJ5 DDR A DM7

AJ44 DDR A DQS0
AT44 DDR A DQS1
BA43 DDR A DQS2
BC37 DDR A DQS3
AW12 DDR A DQS4
BC8 DDR A DQS5
AU8 DDR A DQS6
AM7 DDR A DQS7

AJ43 DDR A DQS#0
AT43 DDR A DQS#1
BA44 DDR A DQS#2
BD37 DDR A DQS#3
AY12 DDR A DQS#4
BD8 DDR A DQS#5
AU9 DDR A DQS#6
AM8 DDR A DQS#7

BA21 DDR A MA0
BC24 DDR A MA1
BG24 DDR A MA2
BH24 DDR A MA3
BG25 DDR A MA4
BA24 DDR A MA5
BD24 DDR A MA6
BG27 DDR A MA7
BF25 DDR A MA8
AW24 DDR A MA9
BC21 DDR A MA10
BG26 DDR A MA11
BH26 DDR A MA12
BH17 DDR A MA13
AY25 DDR A MA14

DDR A BS0 15
DDR A BS1 15
DDR A BS2 15

DDR A RAS# 15
DDR A CAS# 15
DDR A WE# 15

DDR_A_DM[0..7] 15

DDR_A_DQS[0..7] 15

DDR_A_DQS#[0..7] 15

DDR_A_MA[0..14] 15

16 DDR_B_D[0..63]

U2E

DDR B D0 AK47 SB_DQ_0
DDR B D1 AH46 SB_DQ_1
DDR B D2 AP47 SB_DQ_2
DDR B D3 AF46 SB_DQ_3
DDR B D4 AJ46 SB_DQ_3
DDR B D5 AJ48 SB_DQ_4
DDR B D6 AM48 SB_DQ_6
DDR B D7 AP48 SB_DQ_7
DDR B D8 AU47 SB_DQ_8
DDR B D9 AU46 SB_DQ_9
DDR B D10 BA48 SB_DQ_10
DDR B D11 AT47 SB_DQ_11
DDR B D12 AT47 SB_DQ_12
DDR B D13 AR47 SB_DQ_13
DDR B D14 BA47 SB_DQ_14
DDR B D15 BC47 SB_DQ_15
DDR B D16 BC46 SB_DQ_16
DDR B D17 BC44 SB_DQ_17
DDR B D18 BG43 SB_DQ_18
DDR B D19 BF43 SB_DQ_19
DDR B D20 BF45 SB_DQ_20
DDR B D21 BC41 SB_DQ_21
DDR B D22 BF40 SB_DQ_22
DDR B D23 BF41 SB_DQ_23
DDR B D24 BC38 SB_DQ_24
DDR B D25 BF38 SB_DQ_25
DDR B D26 BH35 SB_DQ_26
DDR B D27 BG35 SB_DQ_27
DDR B D28 BH40 SB_DQ_28
DDR B D29 BG39 SB_DQ_29
DDR B D30 BG34 SB_DQ_30
DDR B D31 BH34 SB_DQ_31
DDR B D32 BH14 SB_DQ_32
DDR B D33 BG12 SB_DQ_33
DDR B D34 BH11 SB_DQ_34
DDR B D35 BG8 SB_DQ_35
DDR B D36 BH12 SB_DQ_36
DDR B D37 BF11 SB_DQ_37
DDR B D38 BF8 SB_DQ_38
DDR B D39 BG7 SB_DQ_39
DDR B D40 BC5 SB_DQ_40
DDR B D41 BC6 SB_DQ_41
DDR B D42 AY3 SB_DQ_42
DDR B D43 AY1 SB_DQ_43
DDR B D44 BF6 SB_DQ_44
DDR B D45 BF5 SB_DQ_45
DDR B D46 BA1 SB_DQ_46
DDR B D47 BD3 SB_DQ_47
DDR B D48 AV2 SB_DQ_48
DDR B D49 AU3 SB_DQ_49
DDR B D50 AR3 SB_DQ_50
DDR B D51 AN2 SB_DQ_51
DDR B D52 AY2 SB_DQ_52
DDR B D53 AV1 SB_DQ_53
DDR B D54 AP3 SB_DQ_54
DDR B D55 AR1 SB_DQ_55
DDR B D56 AL1 SB_DQ_56
DDR B D57 AL2 SB_DQ_57
DDR B D58 AL2 SB_DQ_58
DDR B D59 AH1 SB_DQ_59
DDR B D60 AM2 SB_DQ_60
DDR B D61 AM3 SB_DQ_61
DDR B D62 AH3 SB_DQ_62
DDR B D63 AJ3 SB_DQ_63

DDR SYSTEM MEMORY B

CANTIGA ES_FCBGA1329

SB_BS_0
SB_BS_1
SB_BS_2
SB_RAS#
SB_CAS#
SB_WE#

SB_DM_0
SB_DM_1
SB_DM_2
SB_DM_3
SB_DM_4
SB_DM_5
SB_DM_6
SB_DM_7

SB_DQS_0
SB_DQS_1
SB_DQS_2
SB_DQS_3
SB_DQS_4
SB_DQS_5
SB_DQS_6
SB_DQS_7

SB_DQS#_0
SB_DQS#_1
SB_DQS#_2
SB_DQS#_3
SB_DQS#_4
SB_DQS#_5
SB_DQS#_6
SB_DQS#_7

SB_MA_0
SB_MA_1
SB_MA_2
SB_MA_3
SB_MA_4
SB_MA_5
SB_MA_6
SB_MA_7
SB_MA_8
SB_MA_9
SB_MA_10
SB_MA_11
SB_MA_12
SB_MA_13
SB_MA_14

BC16 DDR B BS0
BB17 DDR B BS1
BB33 DDR B BS2

AU17 DDR B RAS#
BG16 DDR B CAS#
BF14 DDR B WE#

AM47 DDR B DM0
AY47 DDR B DM1
BD40 DDR B DM2
BF35 DDR B DM3
BG11 DDR B DM4
BA3 DDR B DM5
AP1 DDR B DM6
AK2 DDR B DM7

AL47 DDR B DQS0
AV48 DDR B DQS1
BG41 DDR B DQS2
BG37 DDR B DQS3
BH9 DDR B DQS4
BB2 DDR B DQS5
AU1 DDR B DQS6
AN6 DDR B DQS7

AL46 DDR B DQS#0
AV47 DDR B DQS#1
BH41 DDR B DQS#2
BH37 DDR B DQS#3
BG9 DDR B DQS#4
BC2 DDR B DQS#5
AT2 DDR B DQS#6
AN5 DDR B DQS#7

AV17 DDR B MA0
BA25 DDR B MA1
BC25 DDR B MA2
AU25 DDR B MA3
AW25 DDR B MA4
BB28 DDR B MA5
AU28 DDR B MA6
AW28 DDR B MA7
AT38 DDR B MA8
BD33 DDR B MA9
BB16 DDR B MA10
AW33 DDR B MA11
AY33 DDR B MA12
BH15 DDR B MA13
AU33 DDR B MA14

DDR B BS0 16
DDR B BS1 16
DDR B BS2 16

DDR B RAS# 16
DDR B CAS# 16
DDR B WE# 16

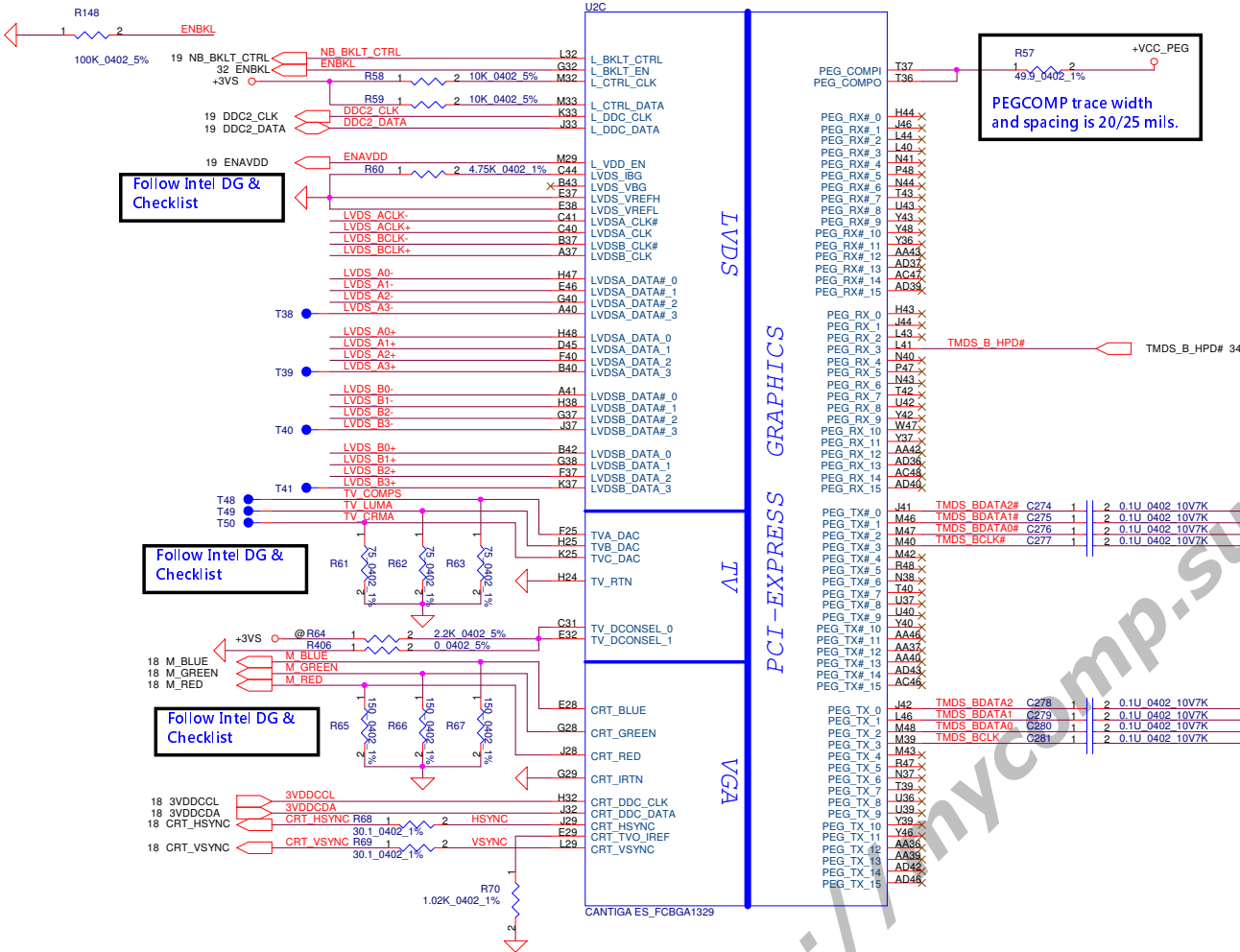
DDR_B_DM[0..7] 16

DDR_B_DQS[0..7] 16

DDR_B_DQS#[0..7] 16

DDR_B_MA[0..14] 16

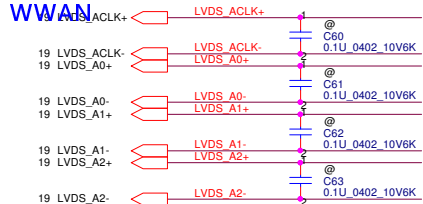
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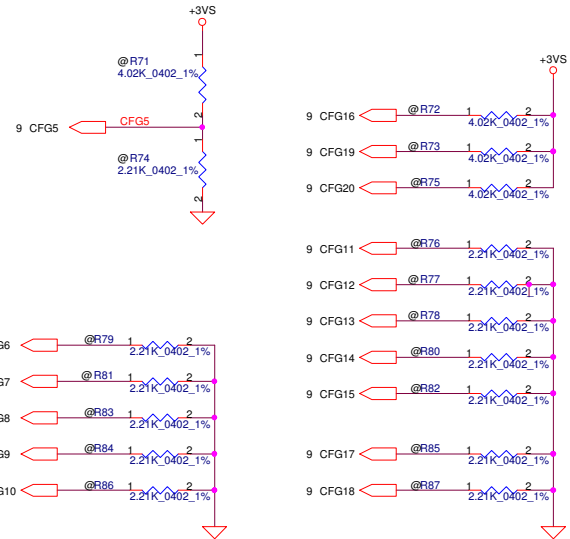
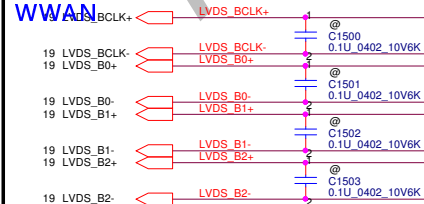
Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 800MHz 001 = FSB 800MHz 010 = FSB 800MHz 011 = FSB 800MHz 100 = FSB 800MHz 101 = FSB 800MHz 110 = FSB 800MHz 111 = FSB 800MHz
CFG[4:3]	Reserved Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4
CFG6	0 = The iTPM Host Interface is enabled 1 = The iTPM Host Interface is disabled
CFG7 (Intel Management Engine Crypto strap)	0 = (iTPM) chip suite with no confidentiality 1 = (iTPM) chip suite with confidentiality
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane, 15->0, 14->1, 13->2, 12->3, 11->4, 10->5, 9->6, 8->7, 7->8, 6->9, 5->10, 4->11, 3->12, 2->13, 1->14, 0->15 1 = Normal Operation, Lane Number in order
CFG10 (PCIe Lookback enable)	0 = Disabled 1 = Enabled
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode 10 = All Z Mode 11 = Normal (Default)
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operating 1 = PCIe/SDVO are operating simultaneously

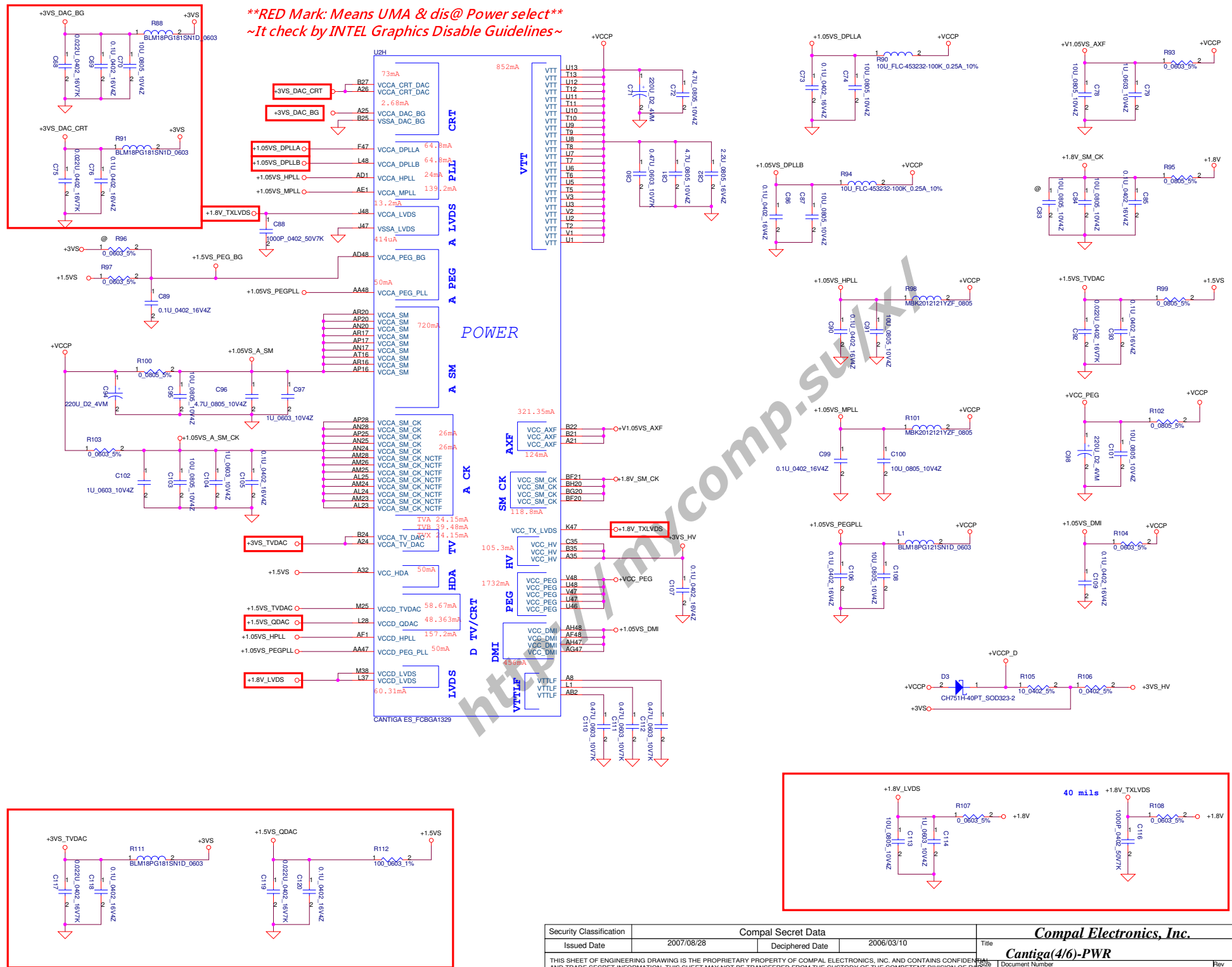
For 3G WWAN

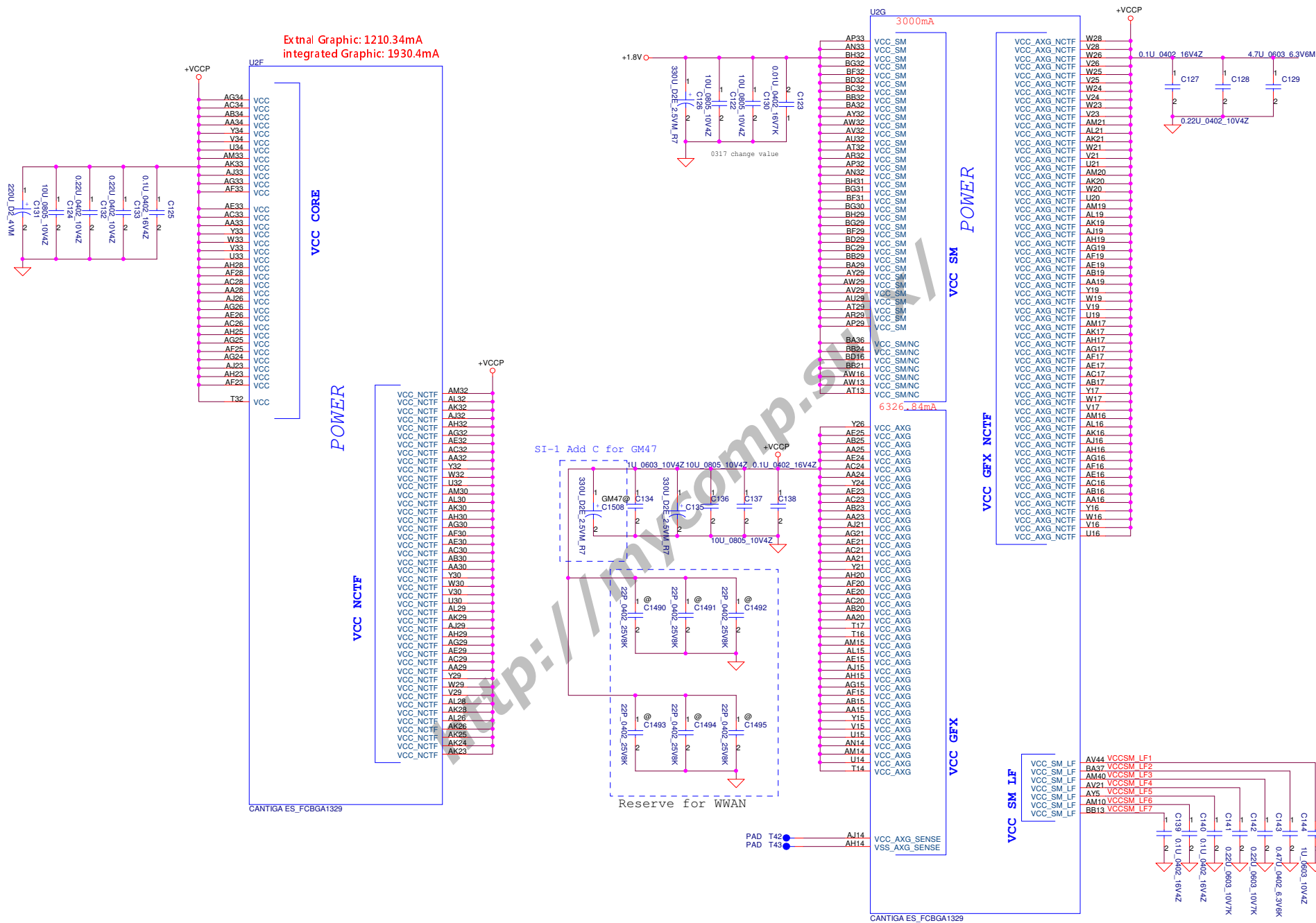


For 3G WWAN

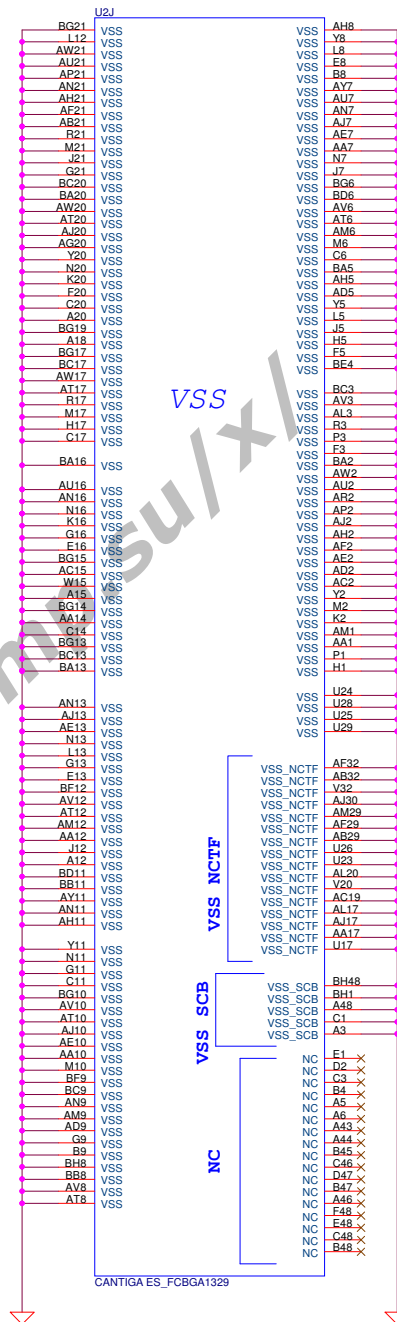
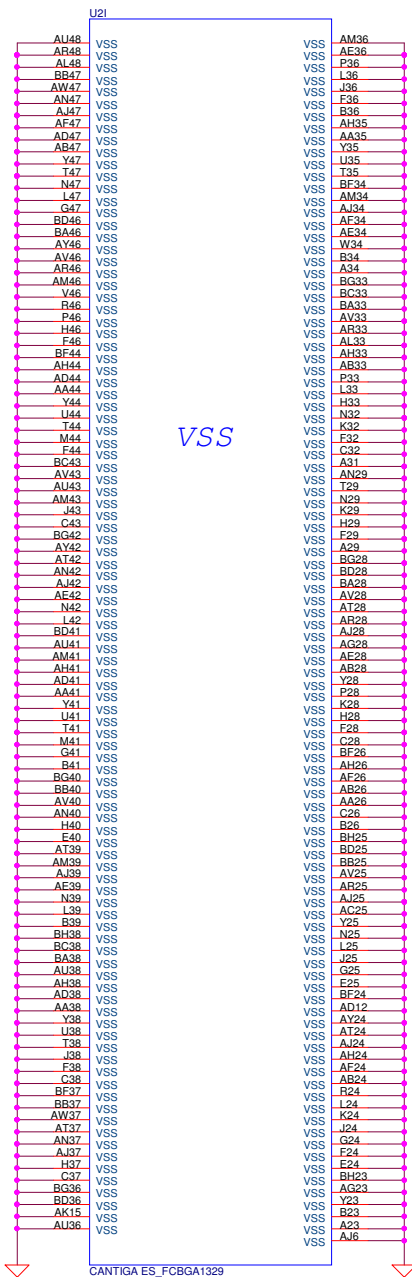


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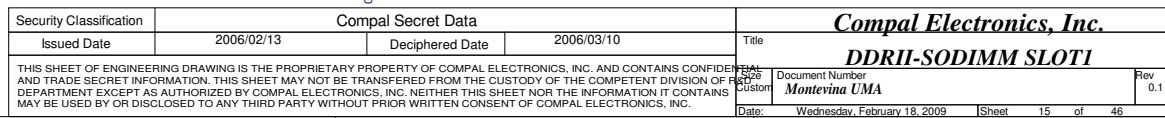
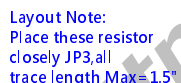
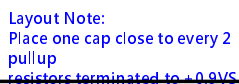
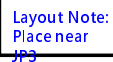


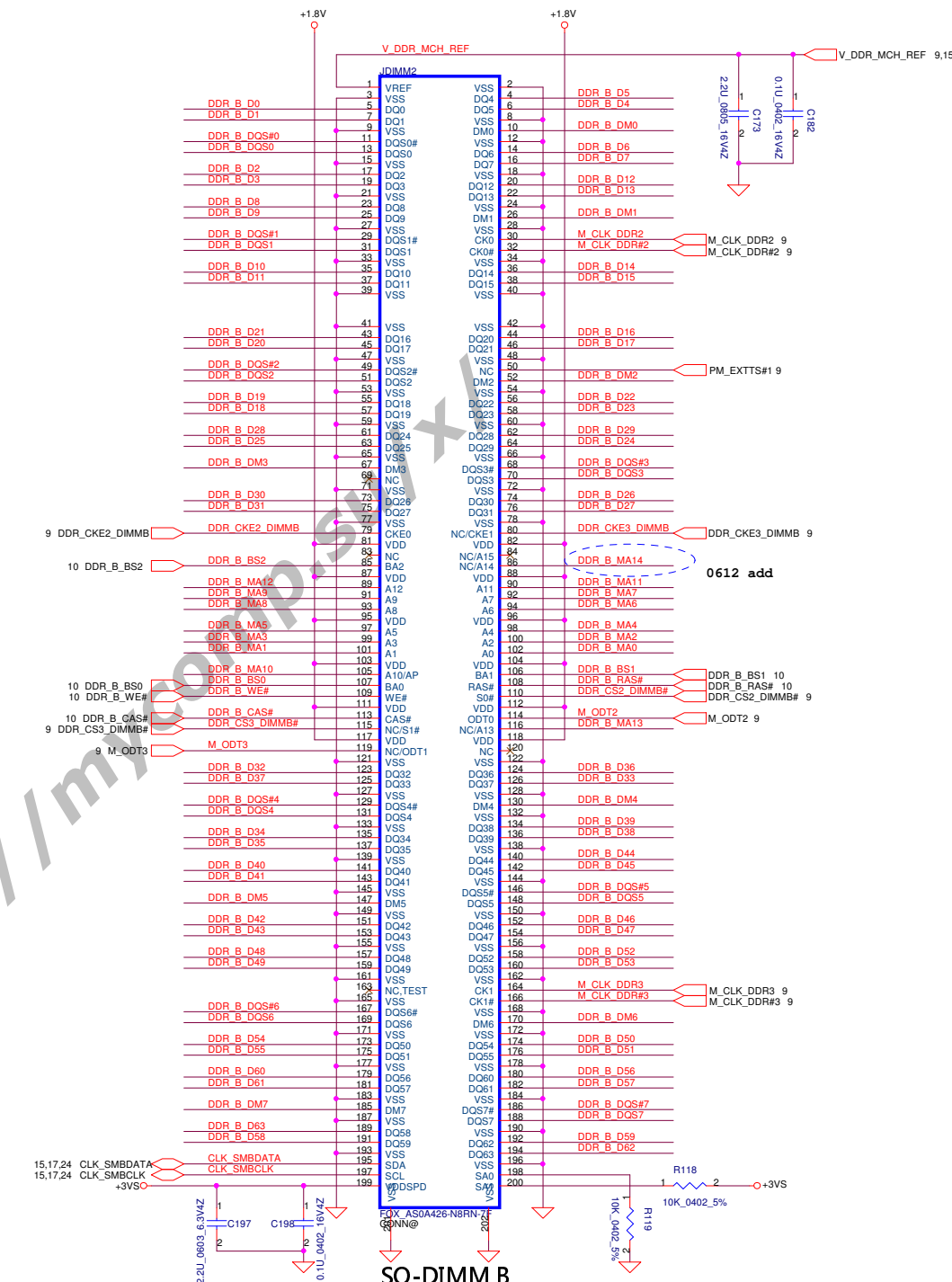
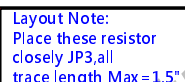
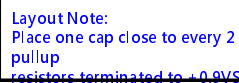
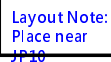


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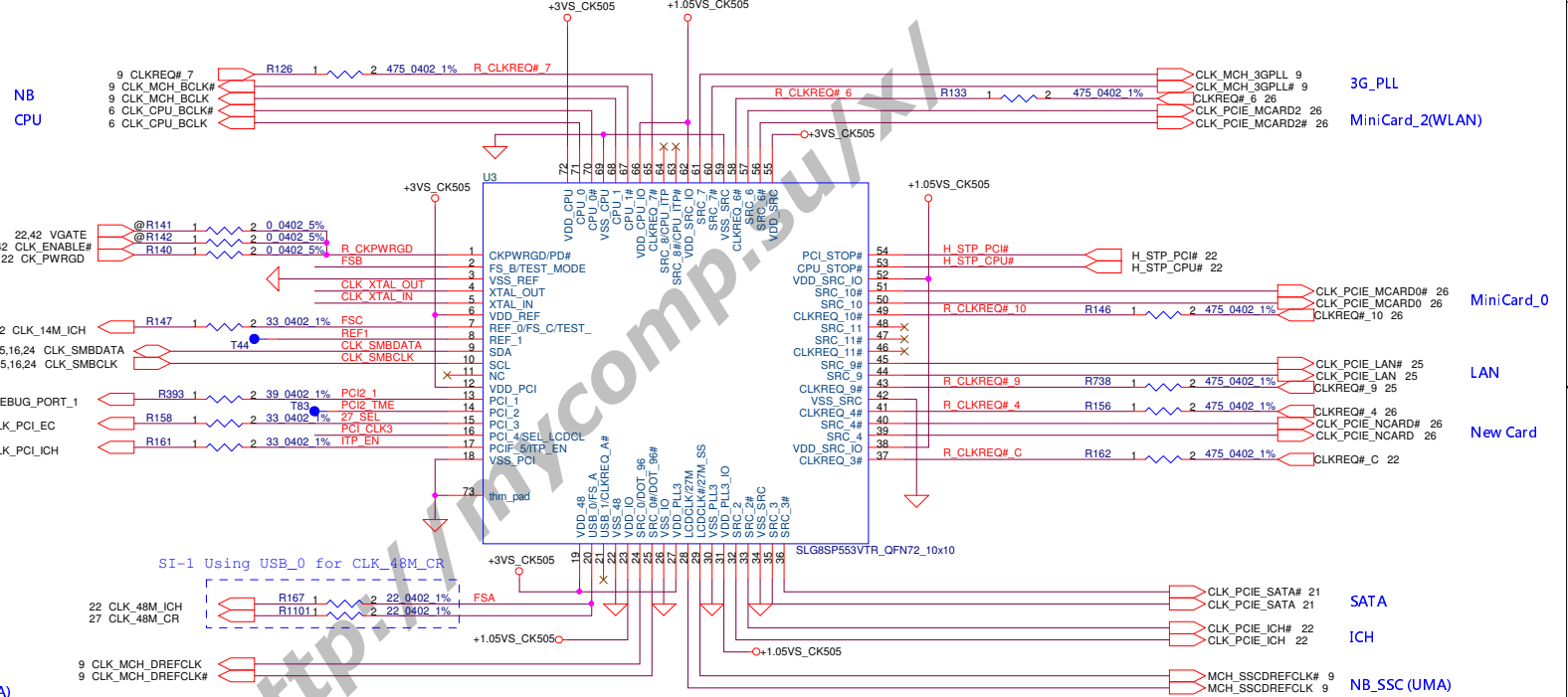
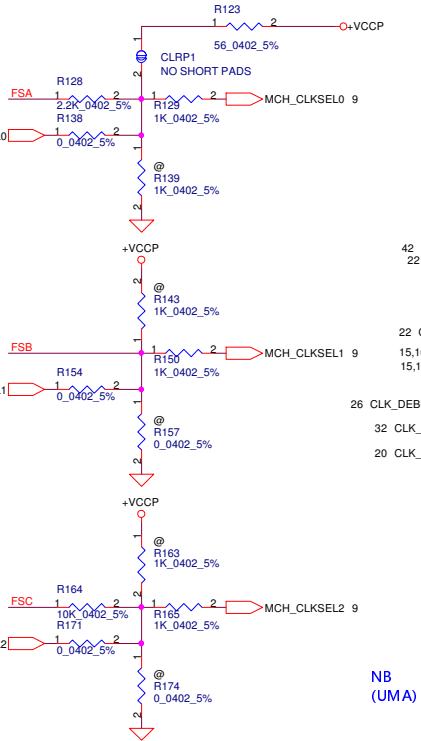
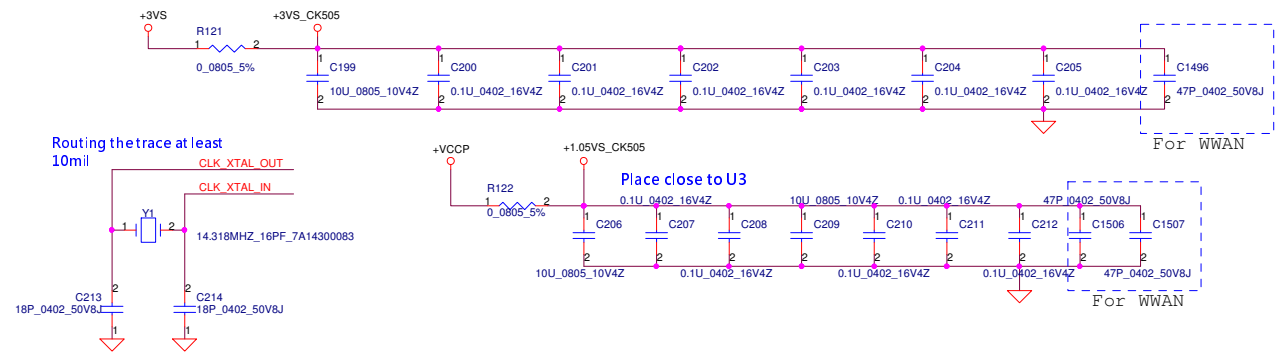
Security Classification		Compal Secret Data		Title	
Issued Date	2007/08/28	Deciphered Date	2006/03/10	Compal Electronics, Inc.	
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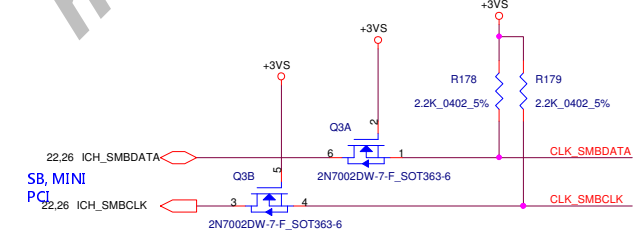
Security Classification		Compal Secret Data		Compal Electronics, Inc. DDRII-SODIMM SLOT2	
Issued Date	2006/02/13	Deciphered Date	2006/03/10	Title	
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FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					




ITP_EN	0 = \$RC8/SRC8#
PCI_CLK3	0 P/EP# \$RC10/MA\$RC0 & \$RC10/MA\$RC0 & 27MHz(DIS)

The diagram shows two circuit connections for signals ITP_EN and PCI_CLK3. Both signals are connected to a 3V5 supply through a pull-up resistor (R180 for ITP_EN, R181 for PCI_CLK3) and a pull-down resistor (R182 for ITP_EN, R183 for PCI_CLK3). The pull-up resistors are labeled 10K_0402_5% and the pull-down resistors are labeled 10K_0402_5%.



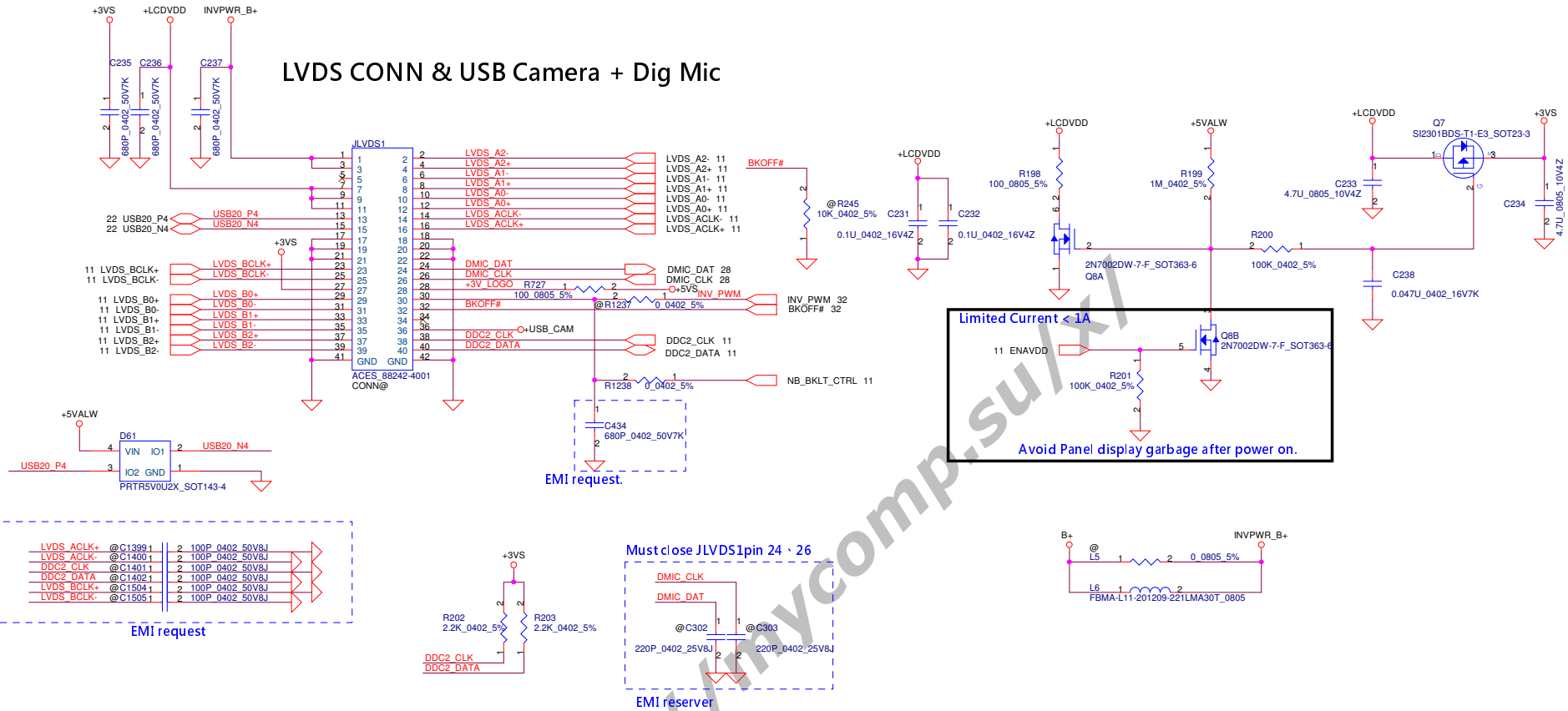
EMI

	@C1482	2	1	CLK 48M CR
	5P_0402_50V8C	2	1	CLK 48M ICH
	@C215	2	1	CLK 48M ICH
	5P_0402_50V8C	2	1	CLK 14M ICH
	C216	2	1	CLK 14M ICH
	12P_0402_50V8J	2	1	CLK PCI ICH
	@C217	2	1	CLK PCI ICH
	47P_0402_50V8J	2	1	CLK PCI EC
	@C218	2	1	CLK PCI EC
	47P_0402_50V8J	2	1	CLK DEBUG_PORT_1
@C219	2	1	CLK DEBUG_PORT_1	
47P_0402_50V8J	2	1	CLK DEBUG_PORT_1	

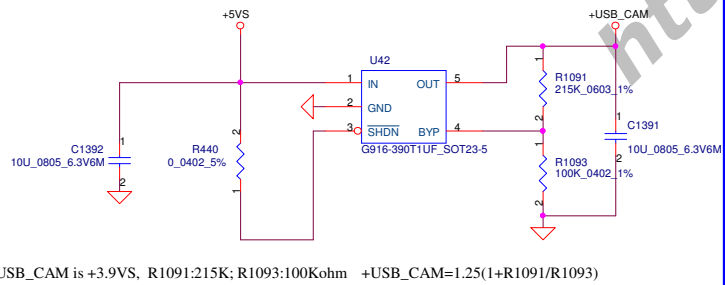
Install C217,C218,C219 for WWAN noise

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Issued Date	2007/08/28	Deciphered Date	2006/03/10	Title	
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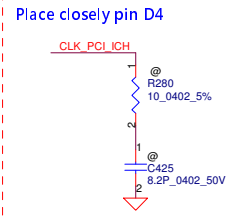
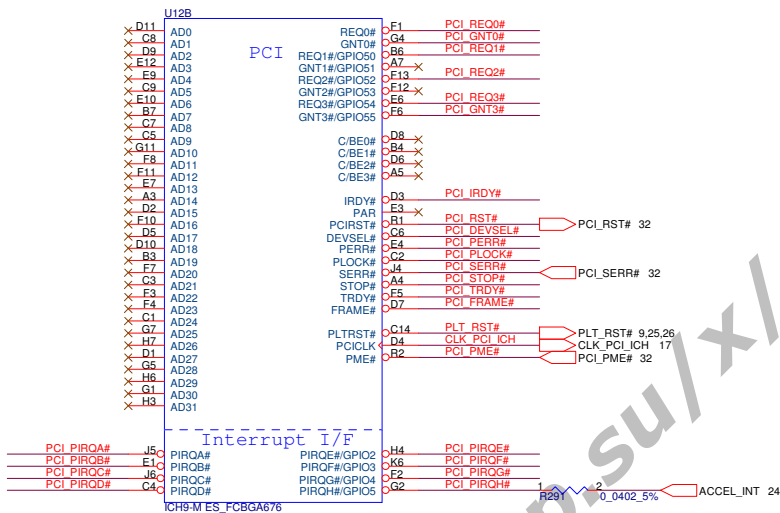
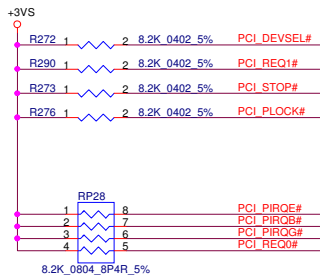
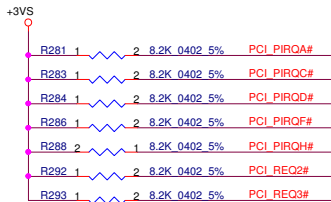
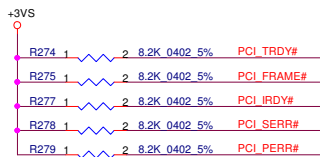
LVDS CONN & USB Camera + Dig Mic



USB Camera

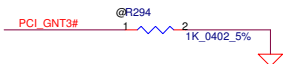


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Issued Date	2007/08/28	Deciphered Date	2006/07/26	LCD CONN.		
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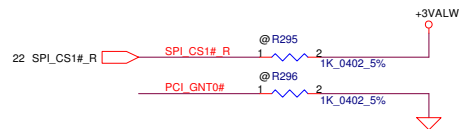
A16 swap override Strap

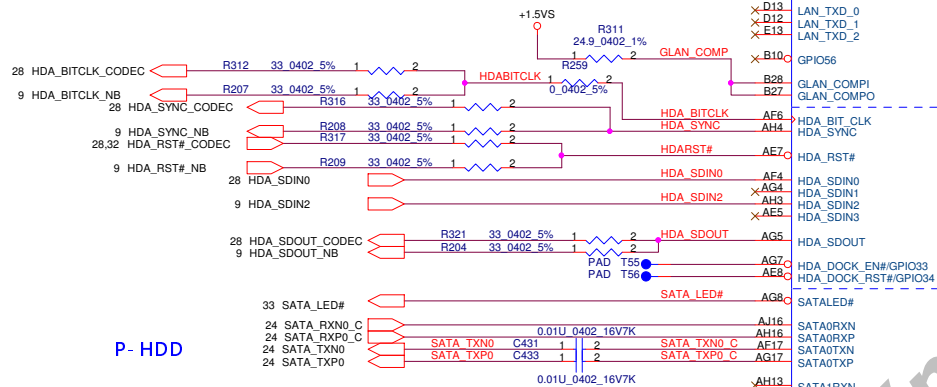
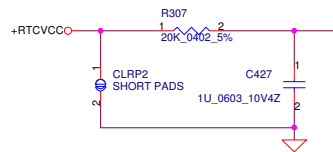
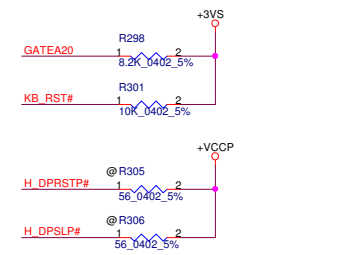
PCI_GNT3#	Low= A16 swap override Enble High= Default*
-----------	--



Boot BIOS Strap

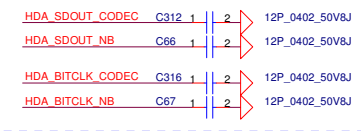
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



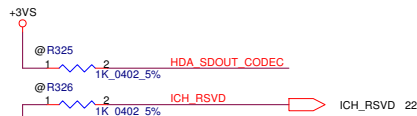


P- HDD

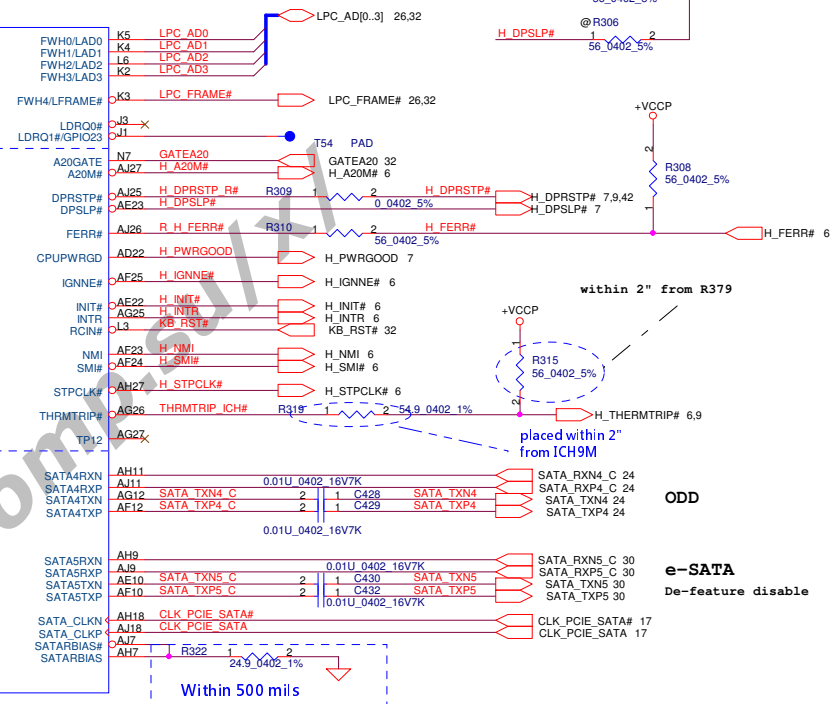
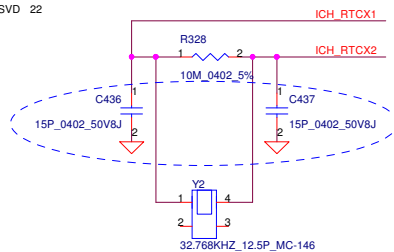
Add 12p on HDA_SDOUT and HDA_SDOUT
Add 12p on HDA_BITCLK_CODE and HDA_BITCLK_NB



XOR CHAIN ENTRANCE STRAP:RSVD



ICH_RSVD	HDA_SDOUT_CODEC	
0	0	
0	1	
1	0	
1	1	

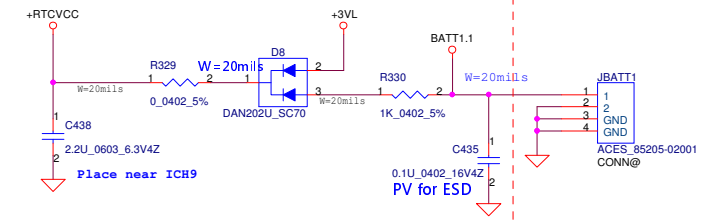


e-SATA
De-feature disable

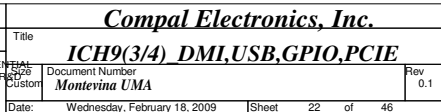
SI-1 Remove SSC

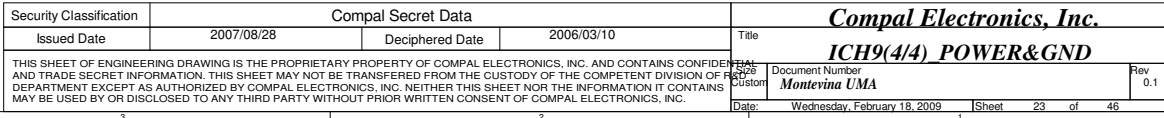
Reserve SSC for EMI

Reserve cap on HDA_BITCLK for WWAN noise issue

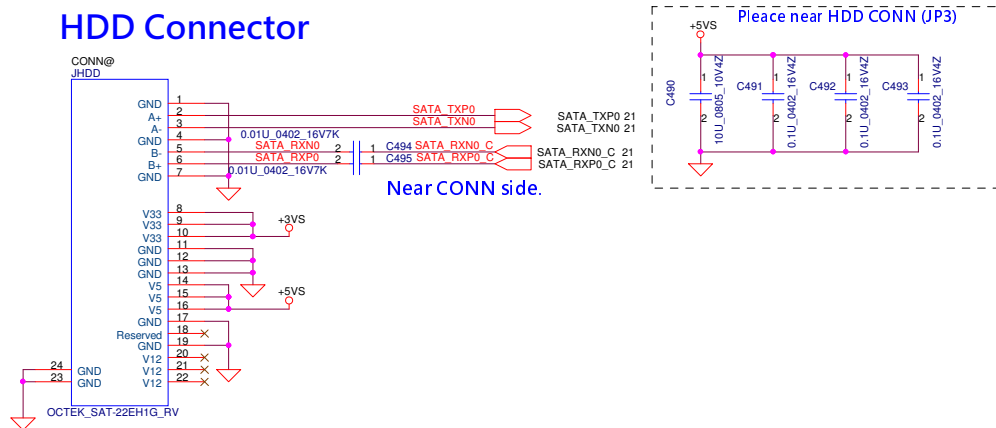


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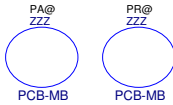
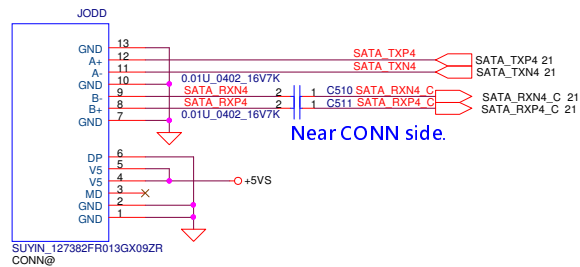




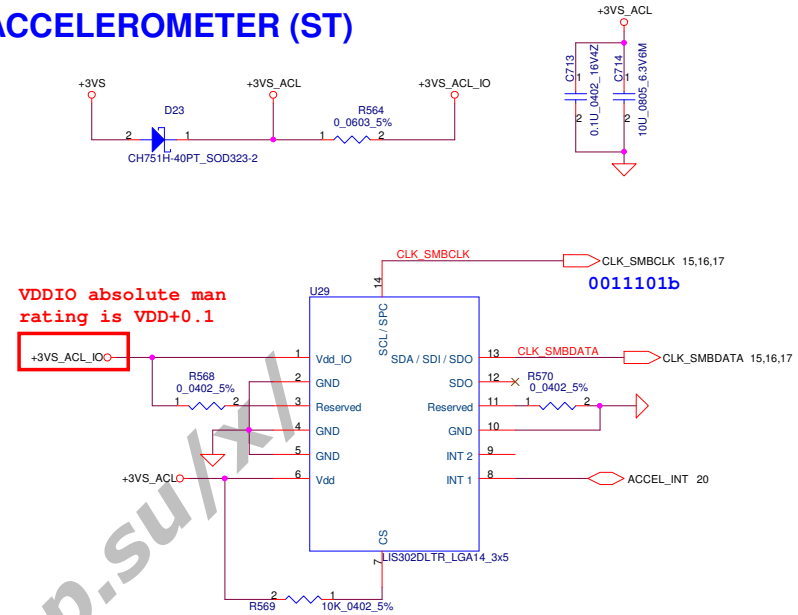
HDD Connector



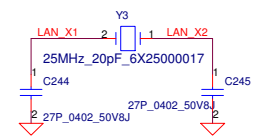
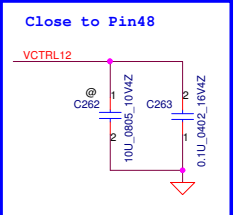
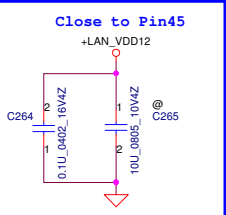
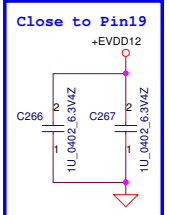
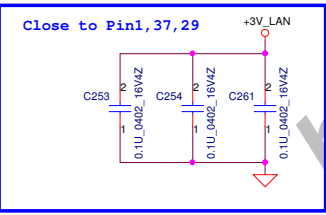
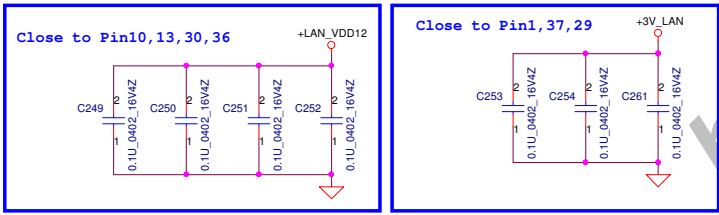
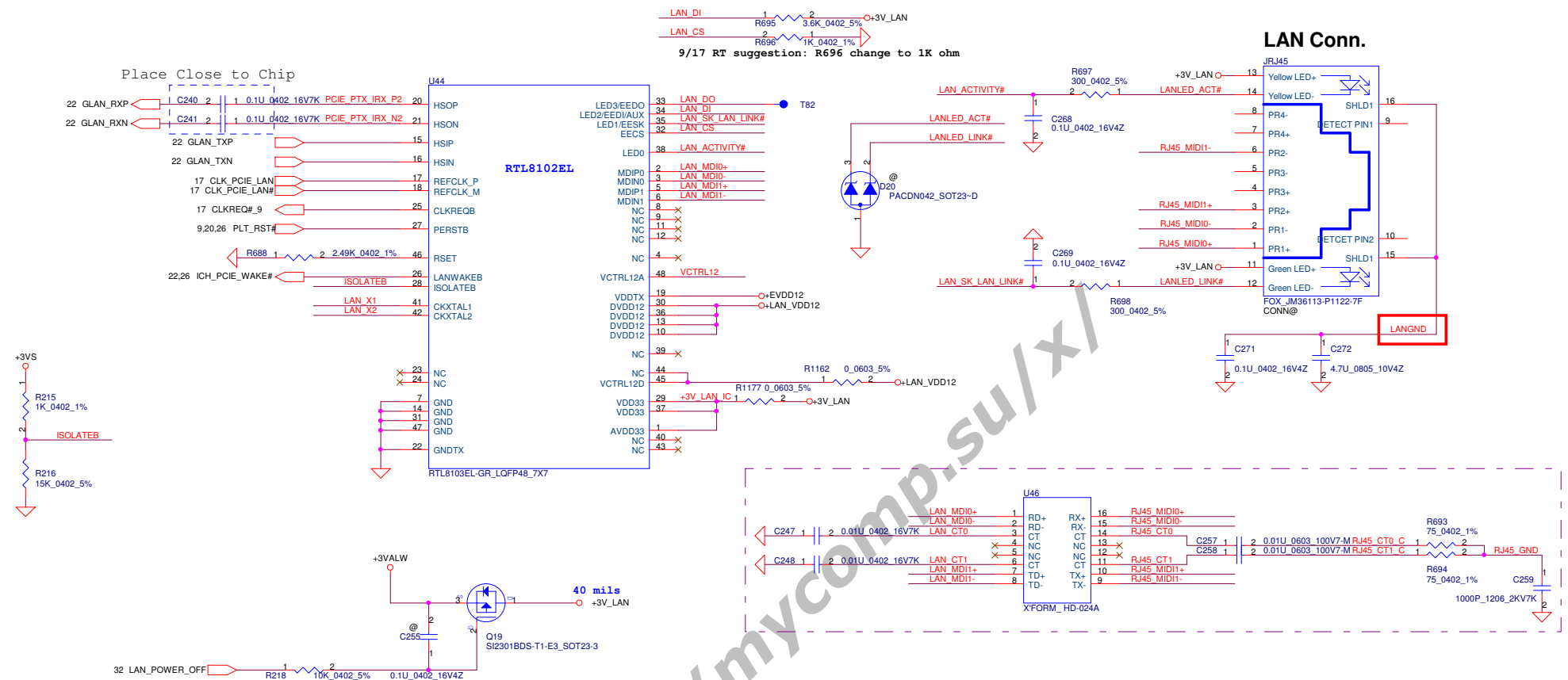
CD-ROM Connector



ACCELEROMETER (ST)



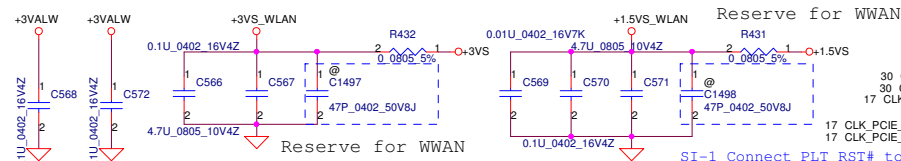
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Issued Date	2007/08/28	Deciphered Date	2006/03/10	HDD & CDROM	
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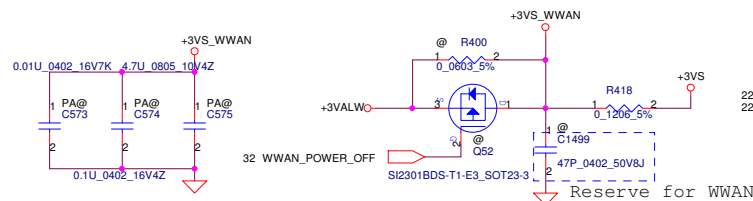
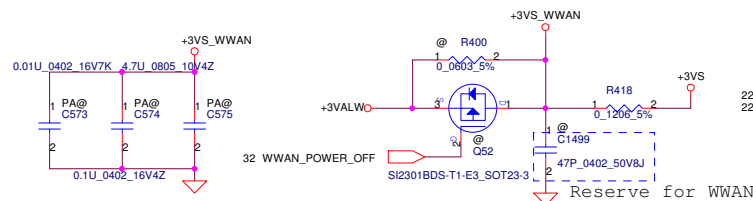
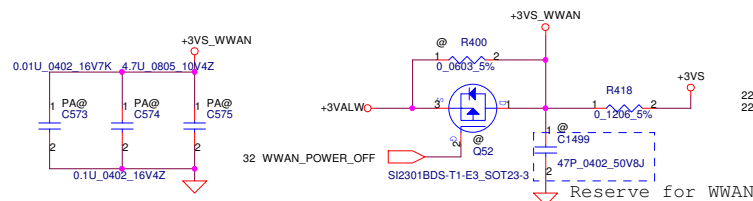
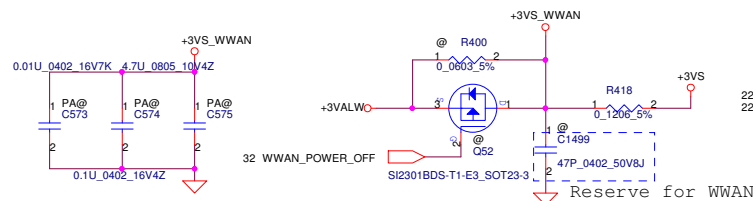
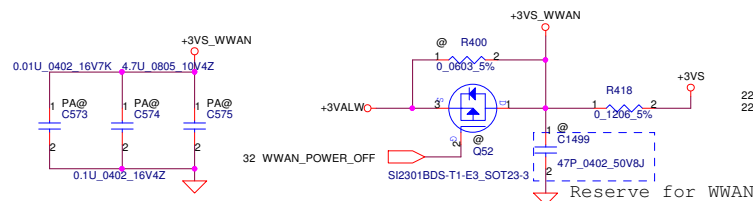
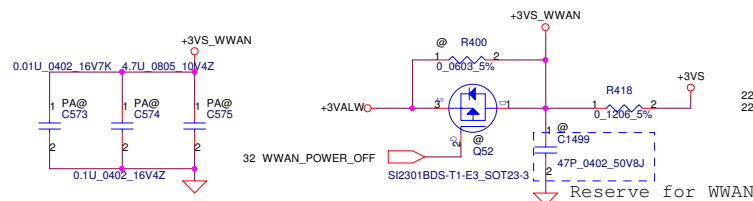
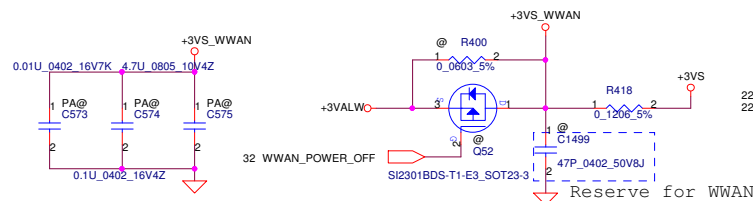
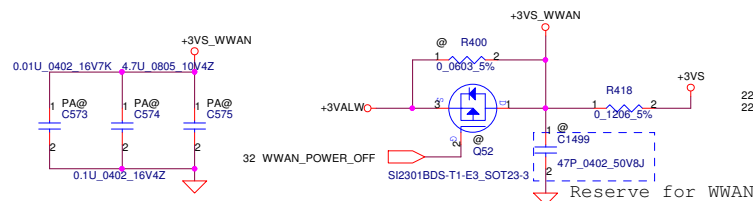
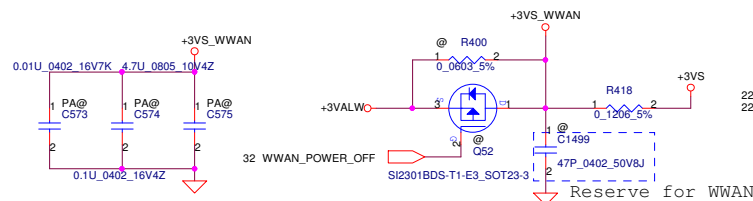
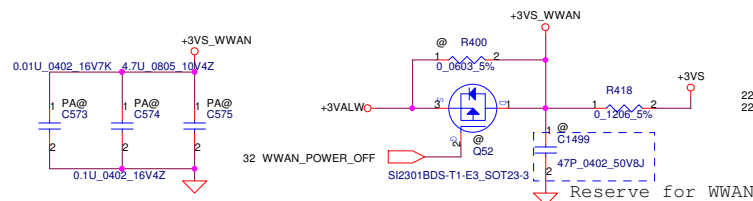
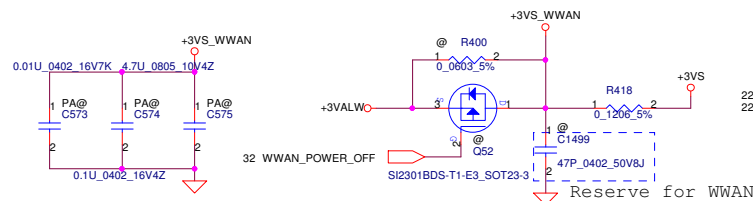
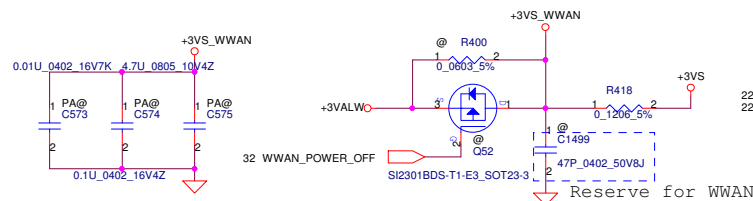
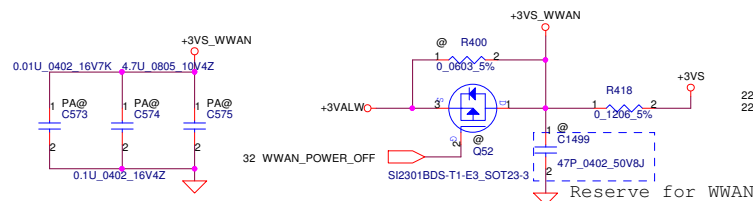
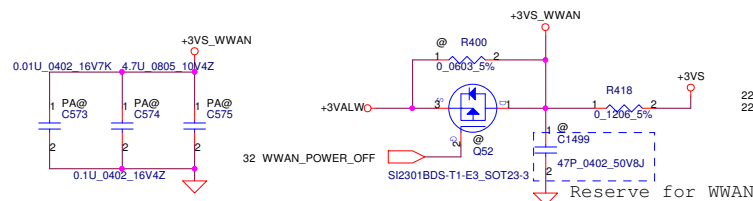
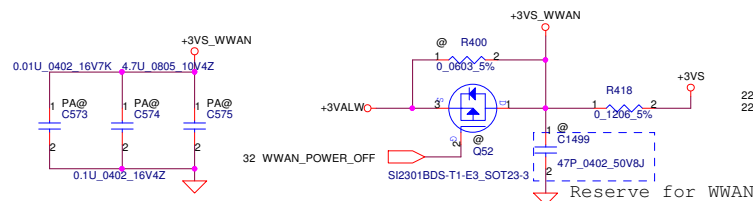
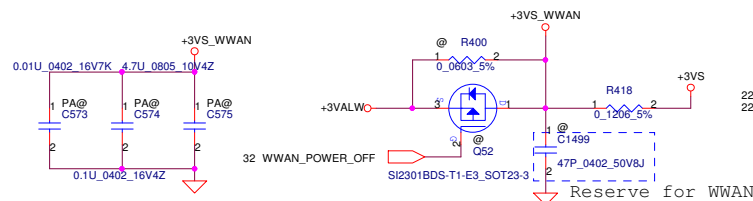
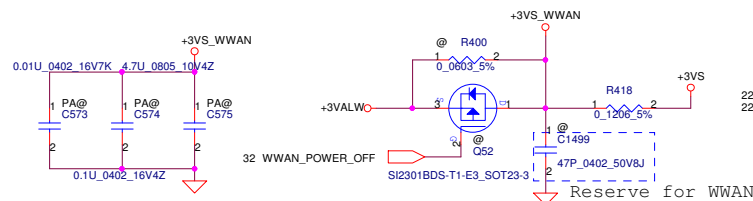
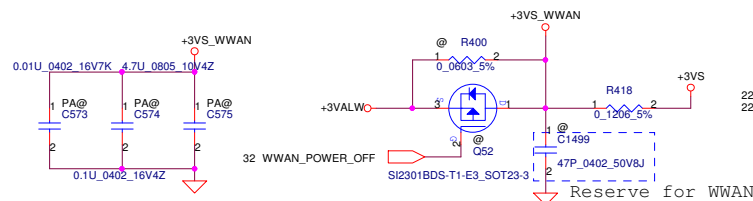
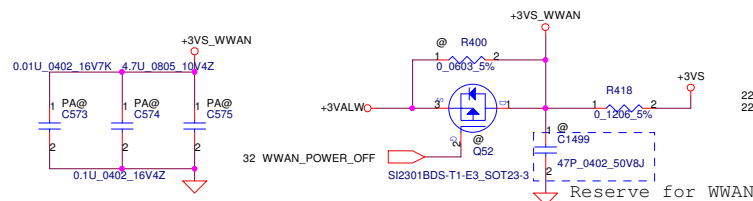
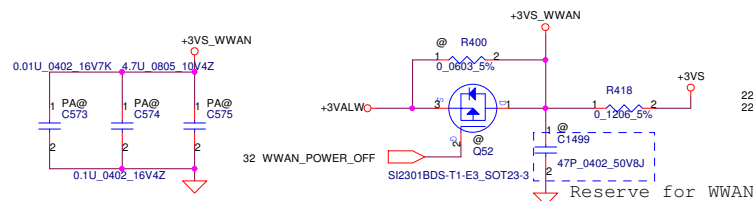
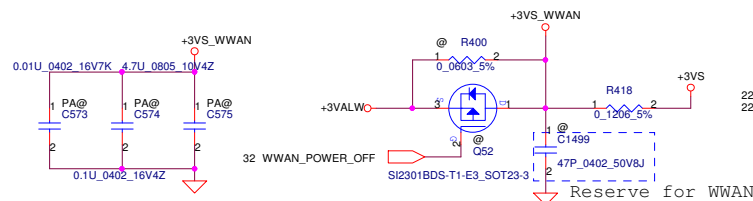
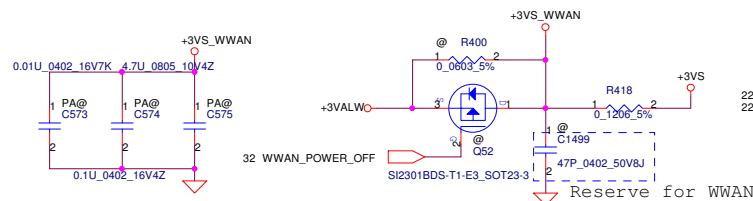
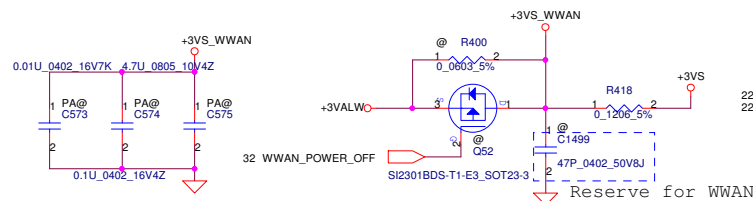
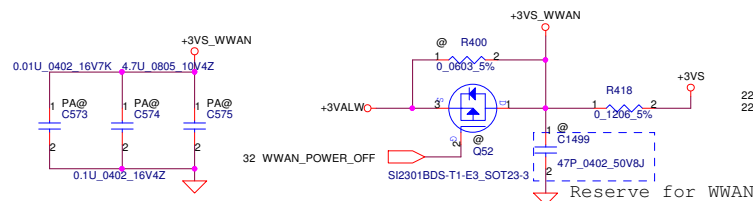
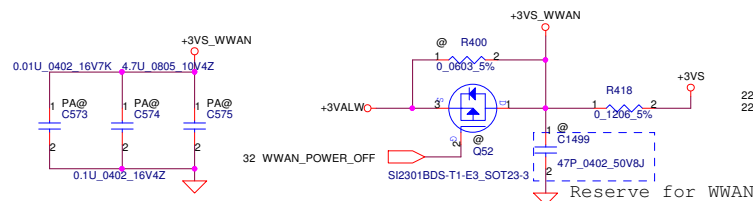
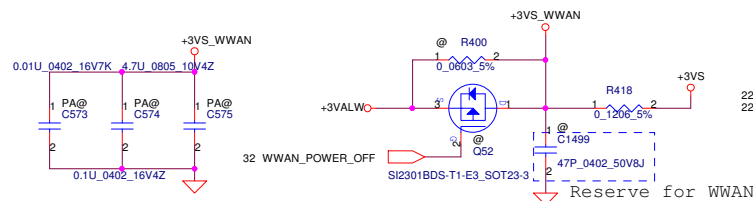
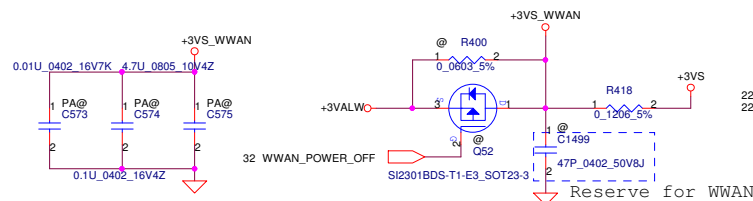
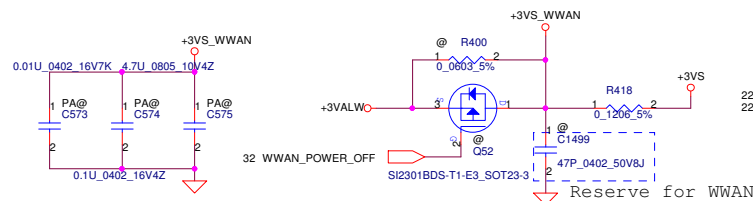
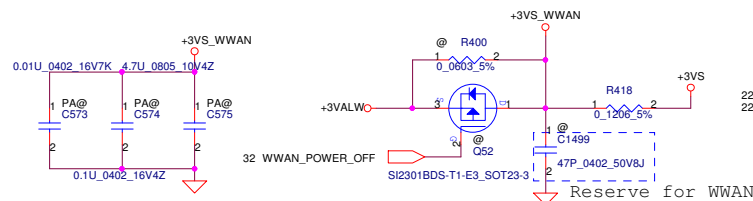
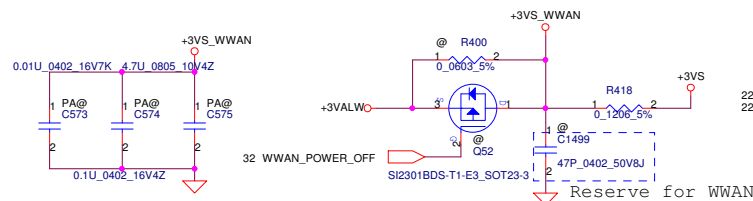
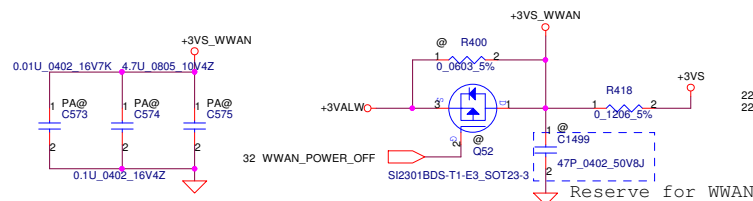
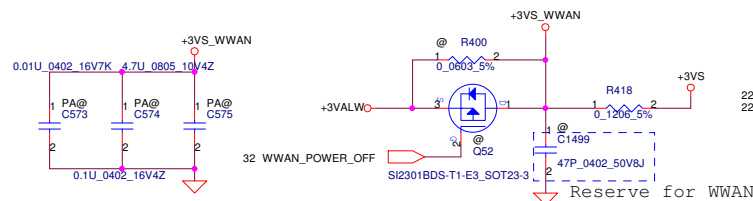
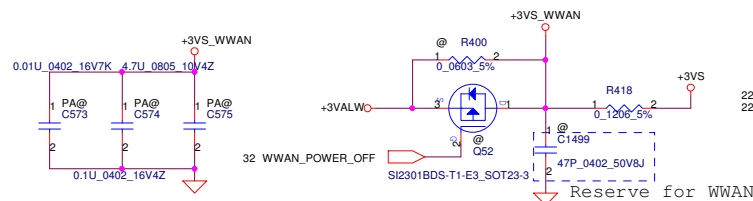
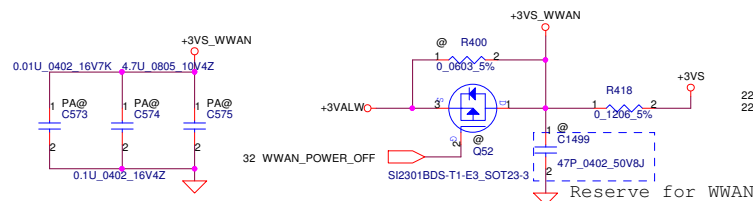
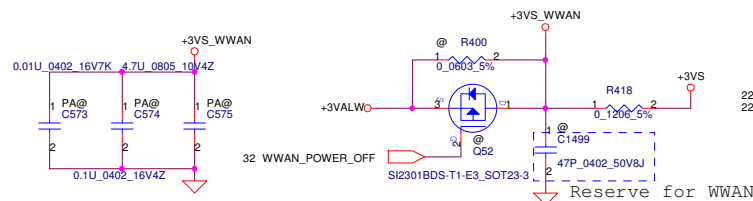
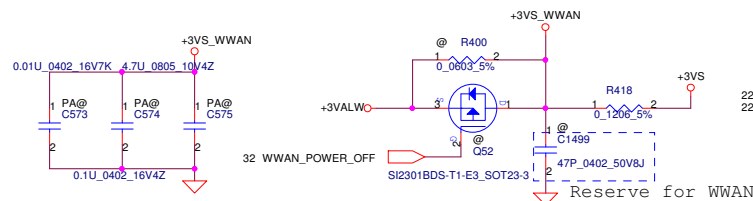
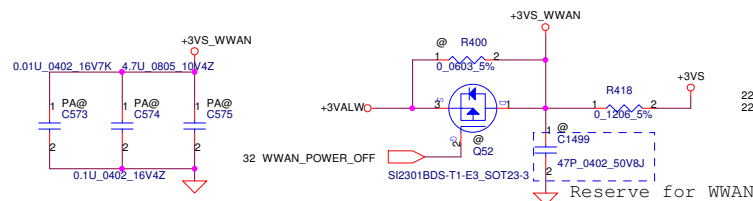
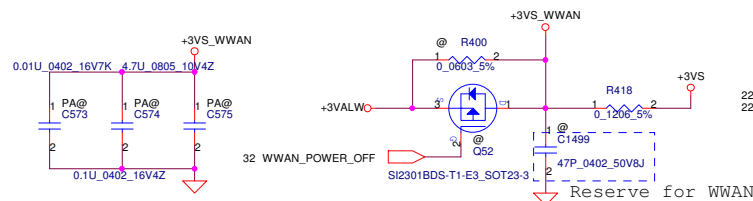
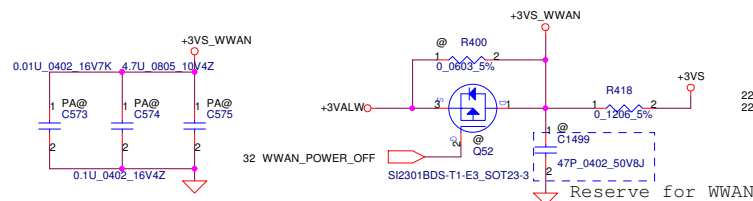
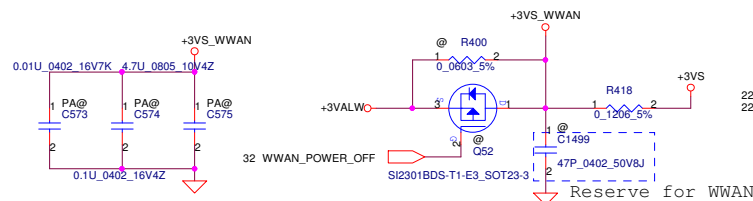
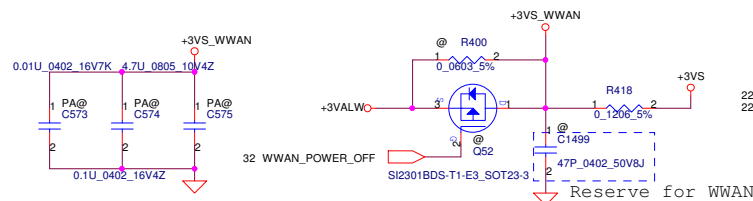
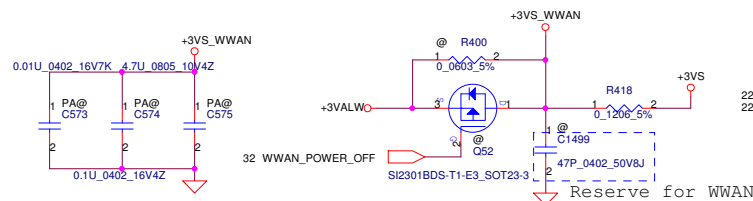
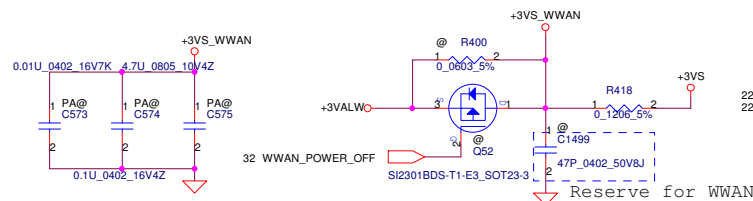
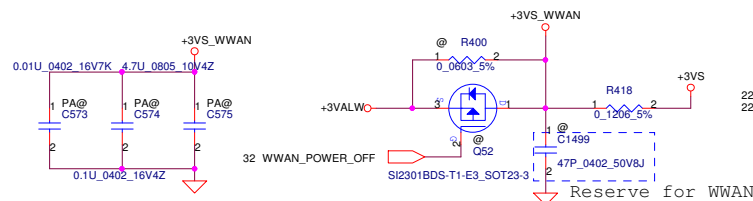
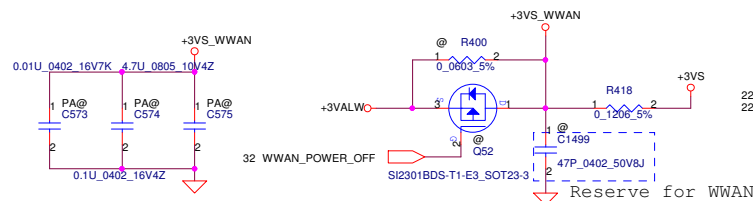
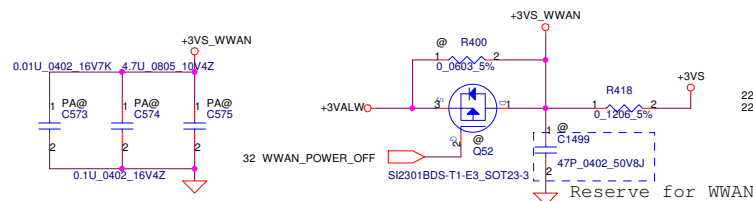
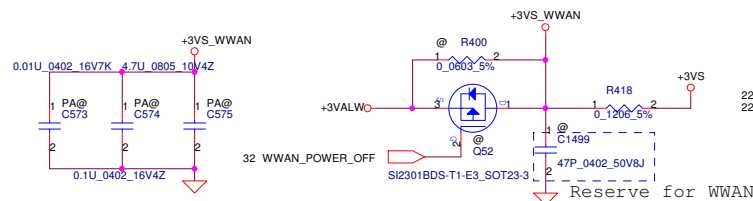
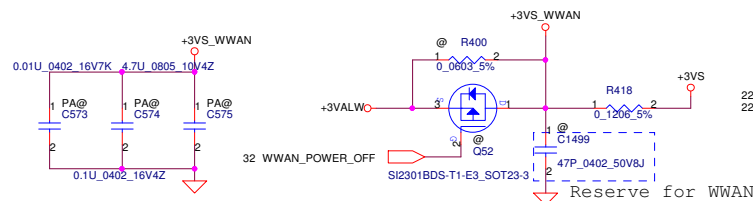
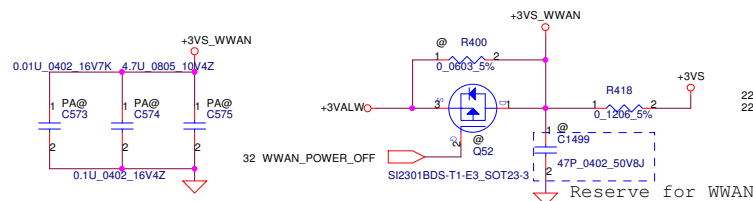
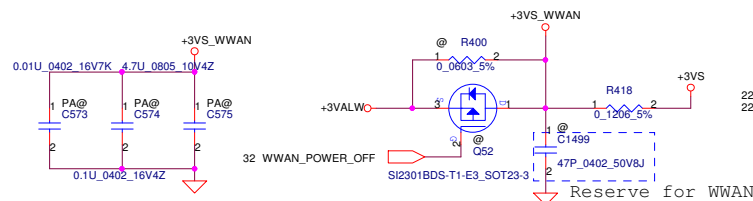
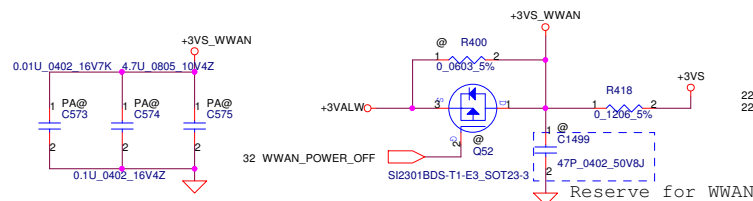
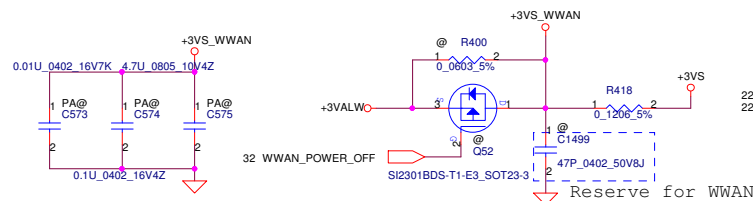
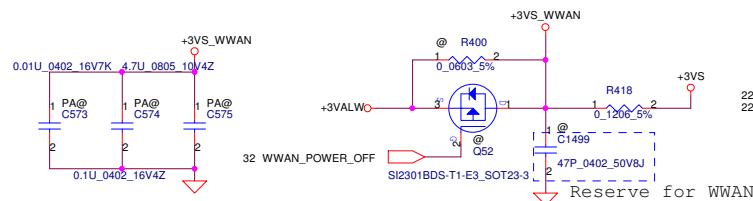
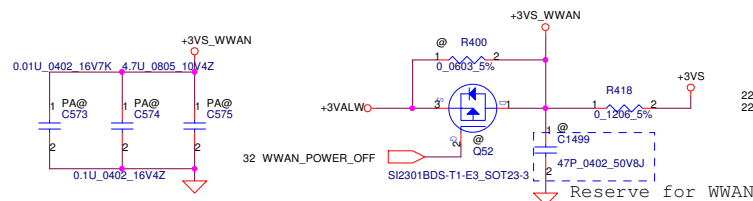
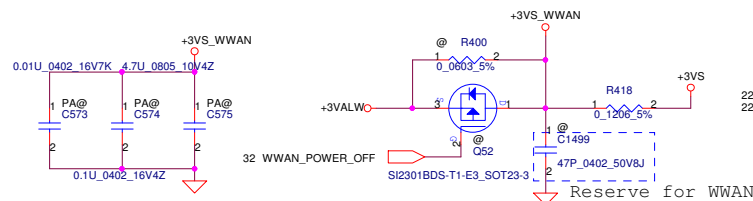
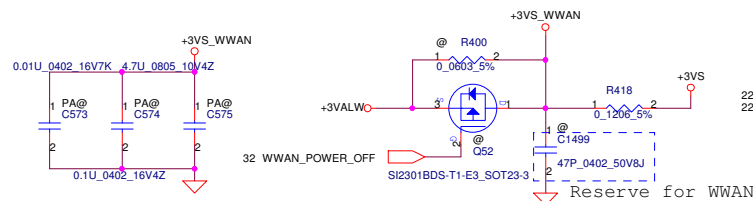
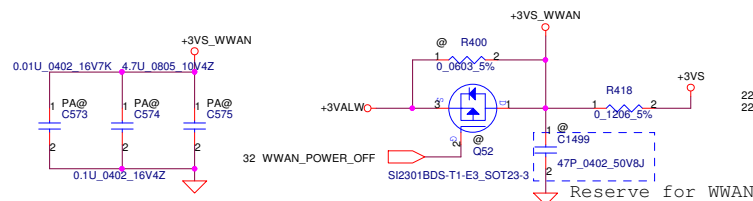
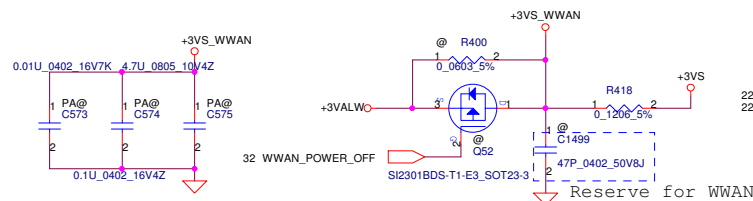
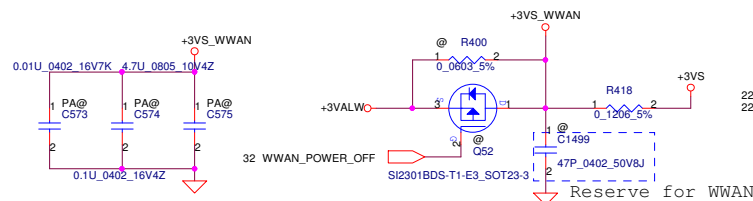
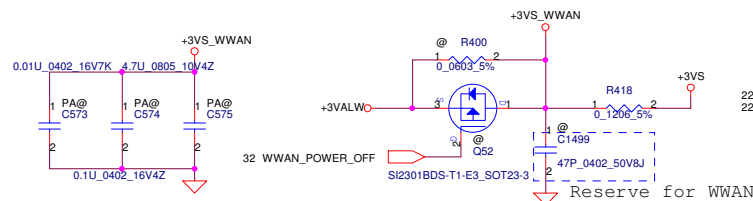
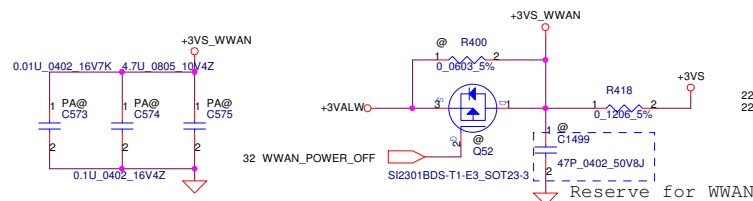
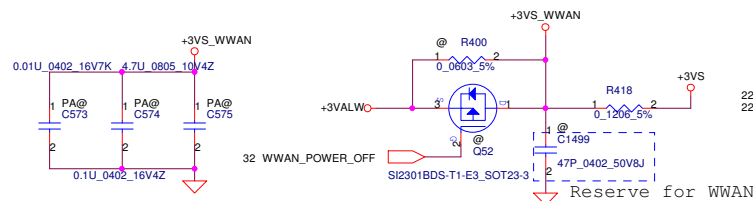
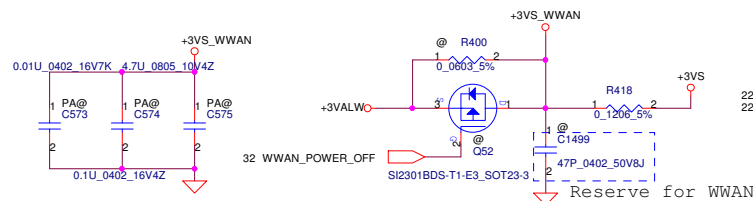
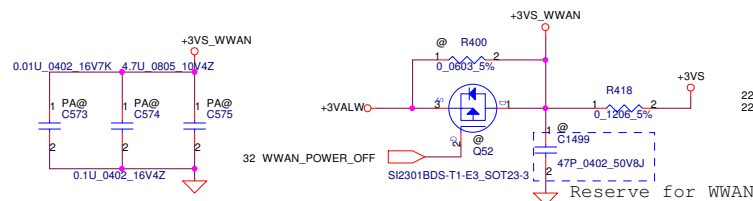
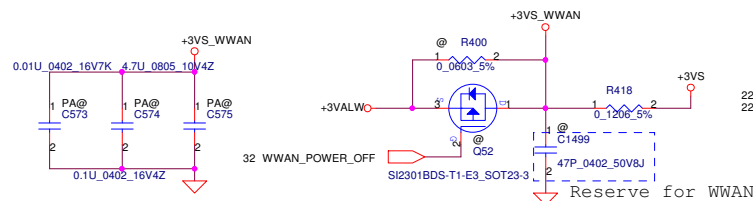
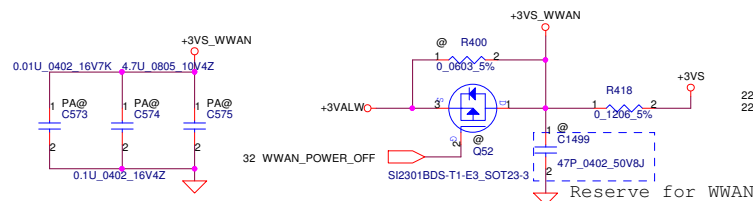
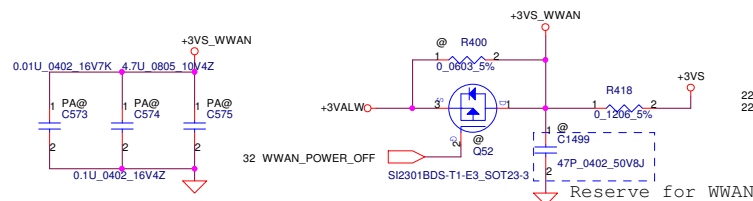
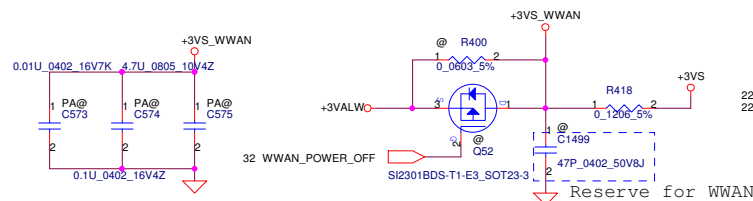
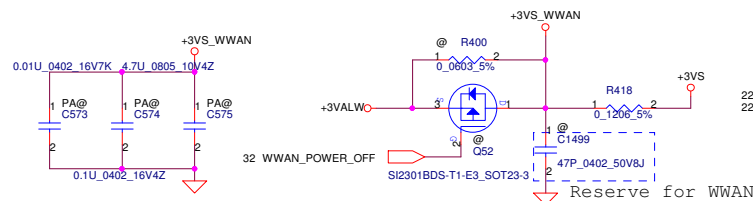
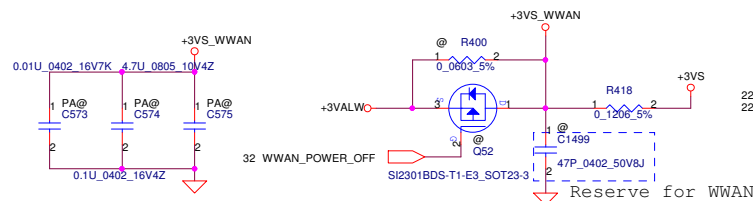
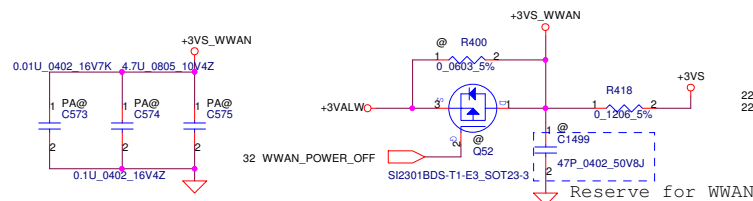
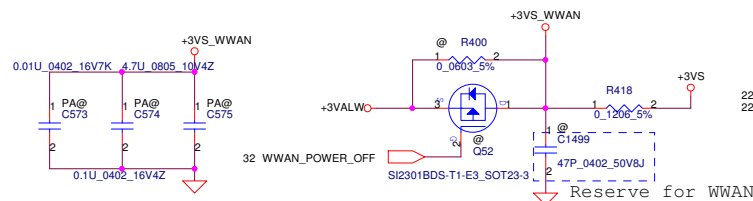
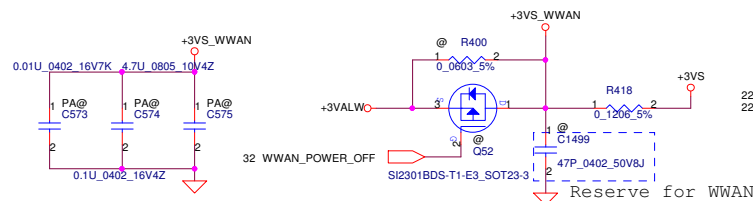
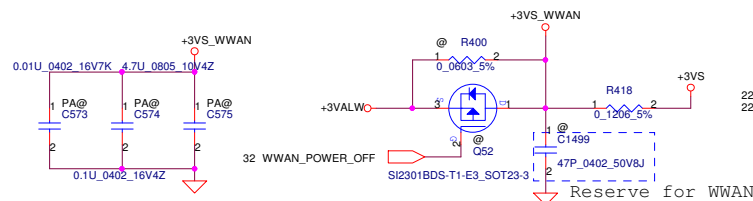
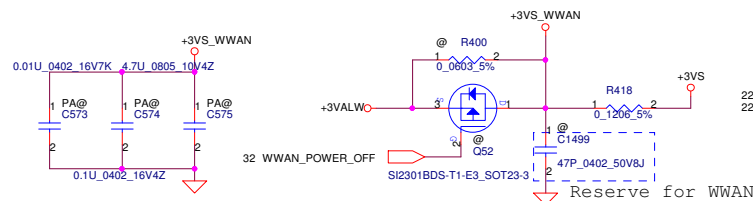
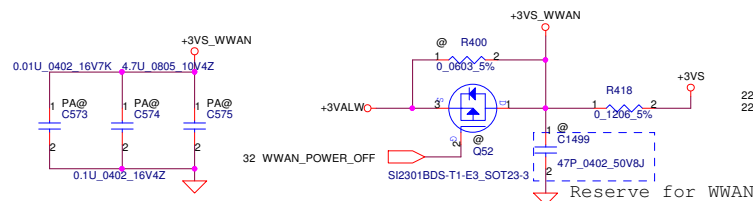
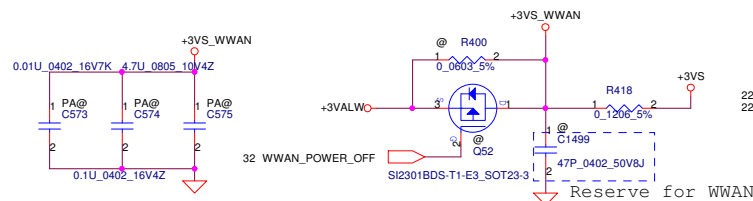
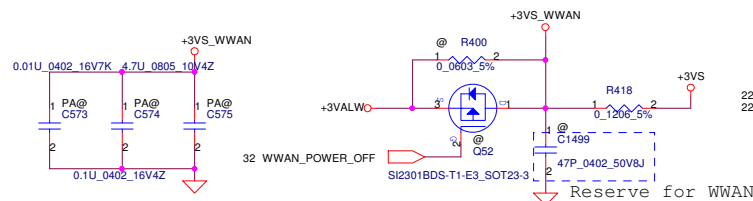
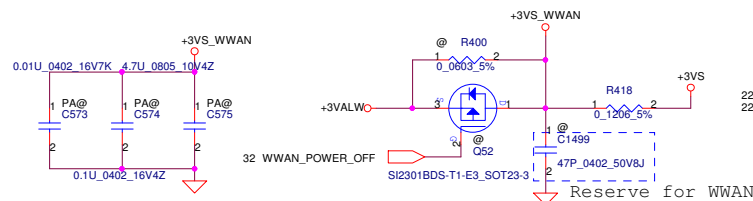
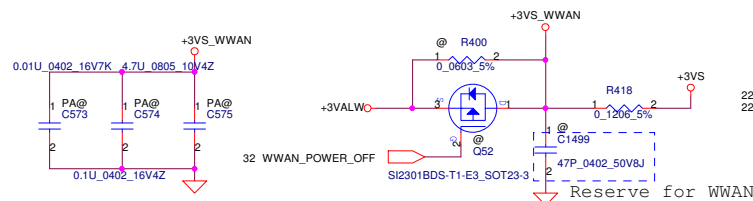
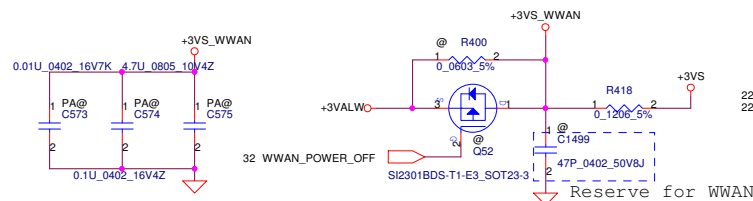
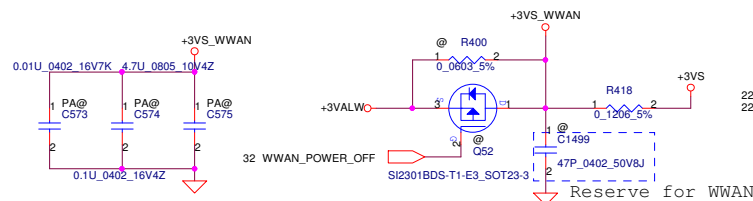
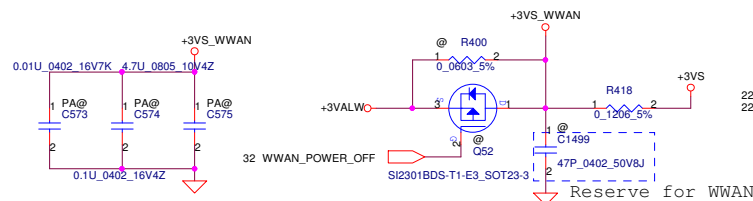
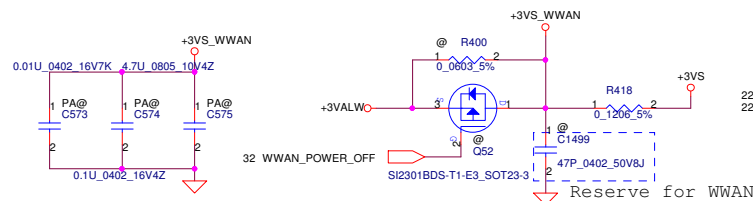
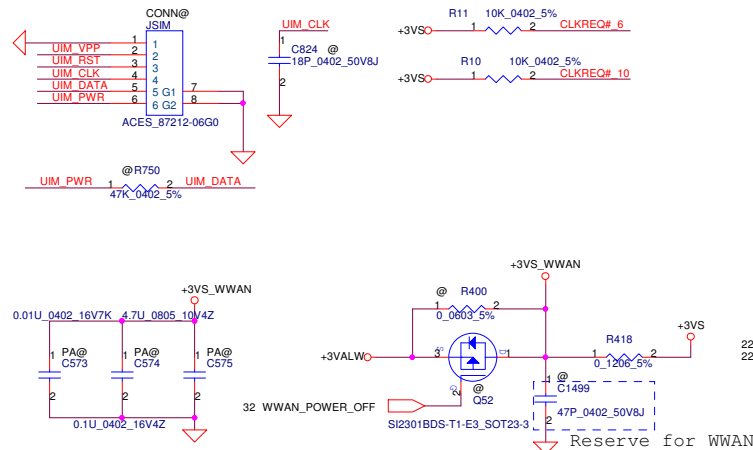
9/17 RT suggestion: C267 change to 1uF

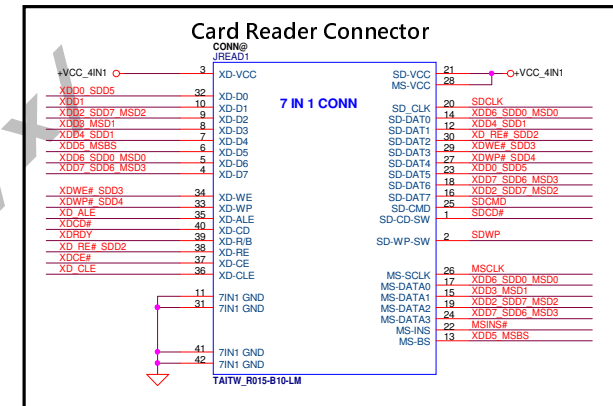
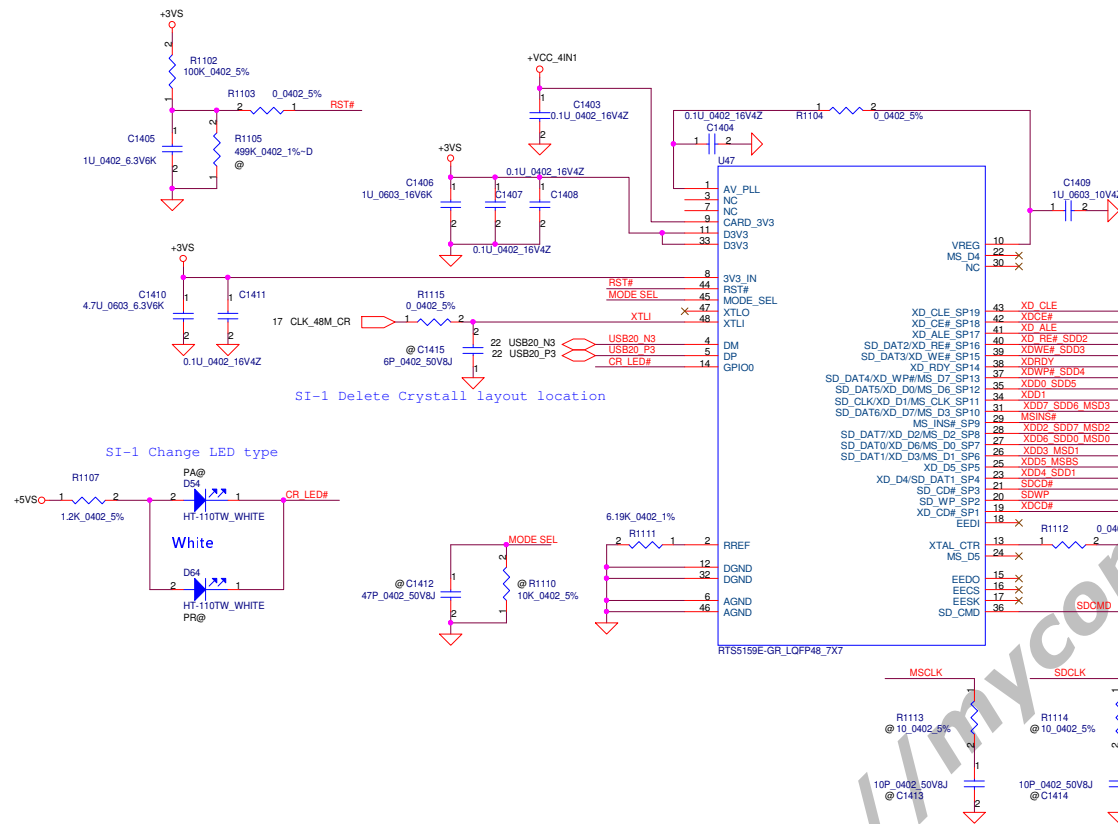
Security Classification		Compal Secret Data		Title	
Issued Date	2007/08/28	Deciphered Date	2007/06/30	RTL8102EL LAN	
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Date				Wednesday, February 18, 2009	Sheet 25 of 46

Mini Card Slot ---WLAN,WWAN



SIM card Connector





-1 Delete CODEC POWER IC

+VDDA_CODEC

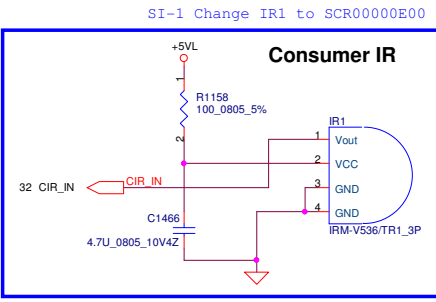
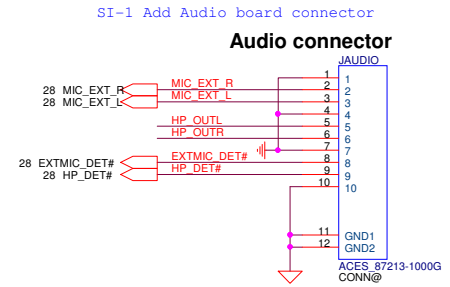
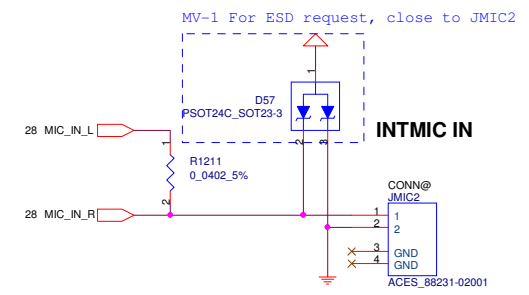
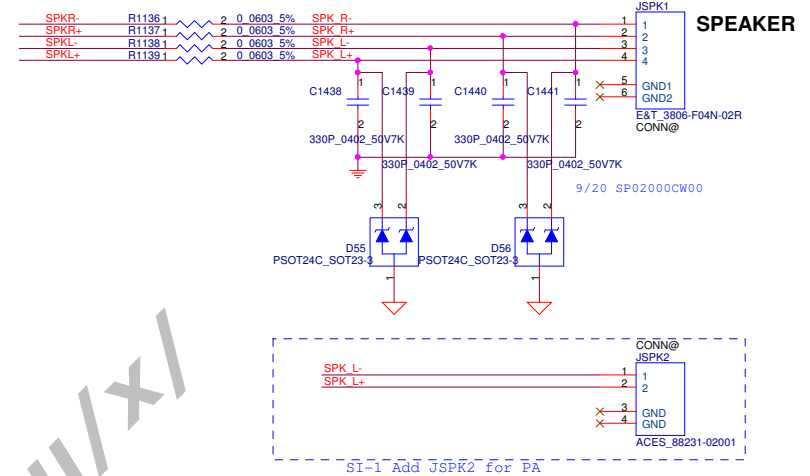
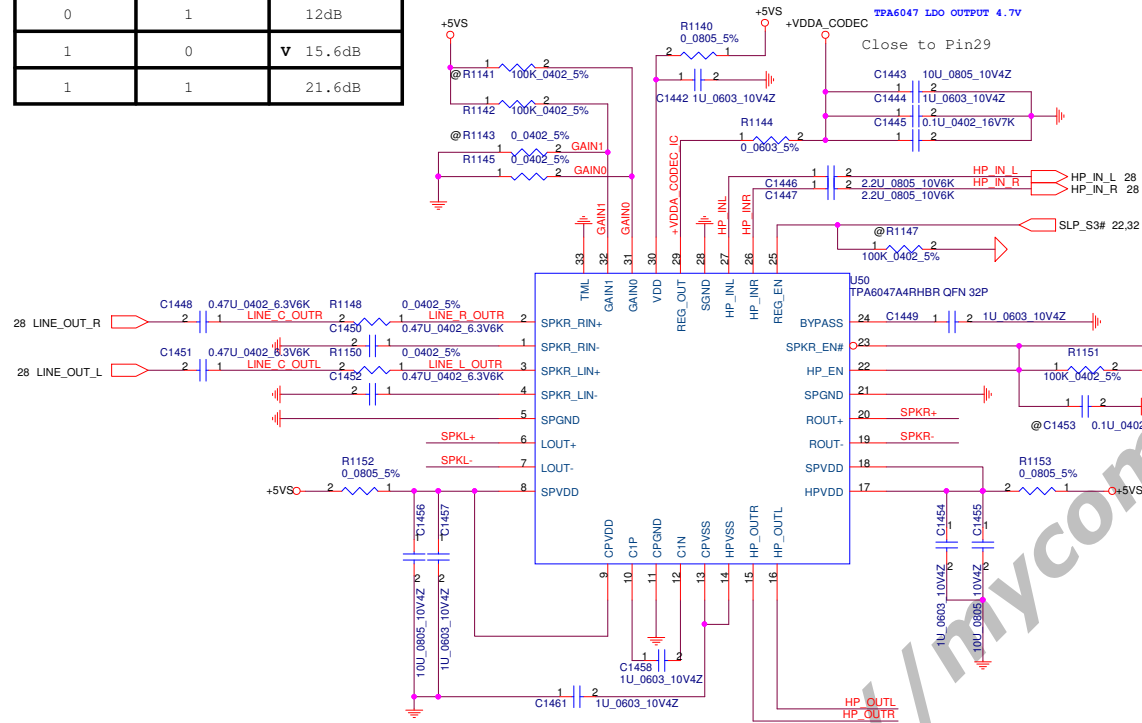
SI-1 Delete CODEC POWER IC



Security Classification	Compal Secret Data					
Issued Date	2007/08/28	Deciphered Date	2006/07/26	Title	Codex_IDT9275B	
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				Date:	Wednesday, February 18, 2009	Sheet 28 of 46

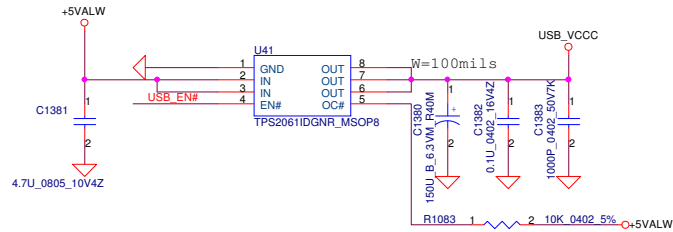
AMP. FOR INTERNAL SPEAKER

GAIN1	GAIN0	Av (inv)
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0	1	12dB
1	0	v 15.6dB
1	1	21.6dB

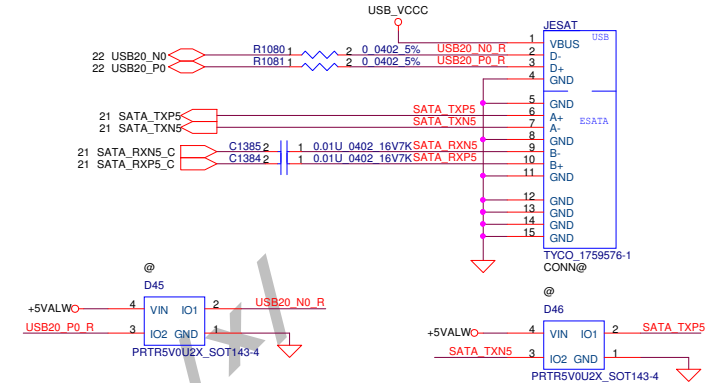


Security Classification	Compal Secret Data					
Issued Date	2007/08/28	Deciphered Date	2006/07/26	Title	AMP & Audio Jack	
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				Customer	Montevina UMA	0.1
				Date:	Wednesday, February 18, 2009	Sheet 29 of 46

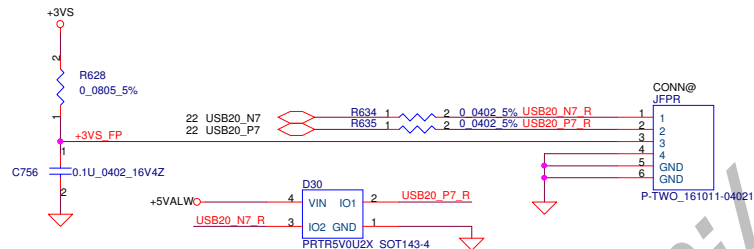
Right side USB Power Switch



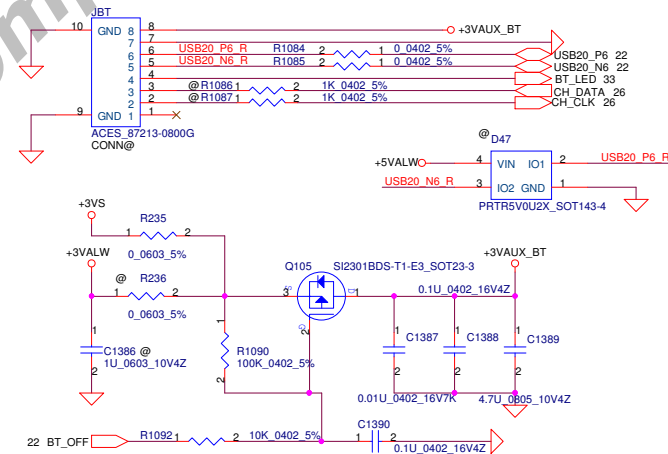
Right side ESATA/USB combination Connector



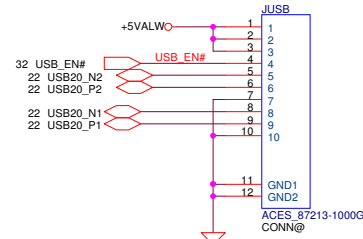
Finger printer



BT Connector

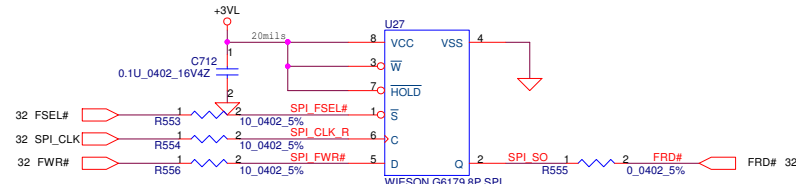


USB cable connector for Right side

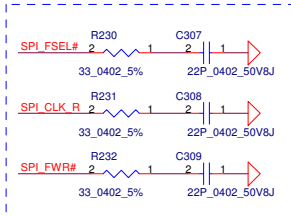


Security Classification	Compal Secret Data			Title	
Issued Date	2007/08/28	Deciphered Date	2006/07/26	USB, BT, eSATA	
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				Montevina UMA	0.1
				Date: Wednesday, February 18, 2009	Sheet 30 of 46

SPI ROM



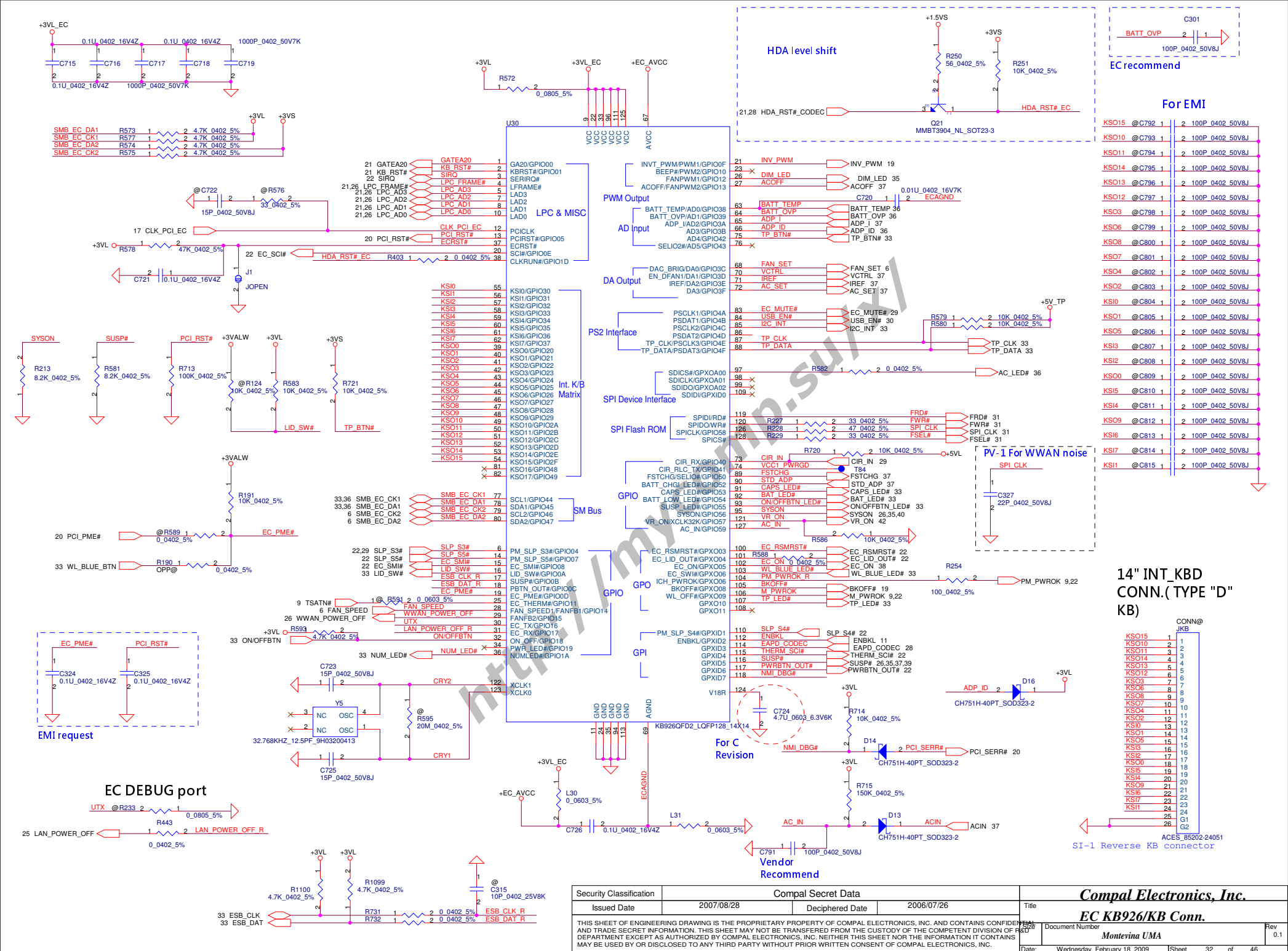
SP07000F500 S SOCKET WIESON G6179-100000 8P SPIFLASH
WIESO_G6179-100000_8P



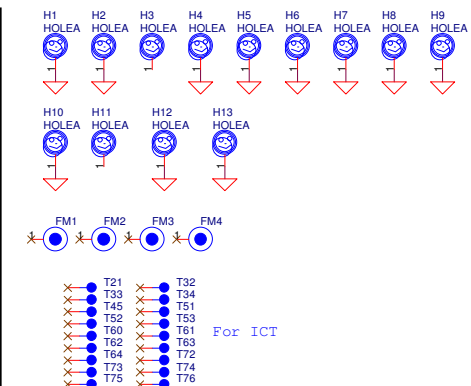
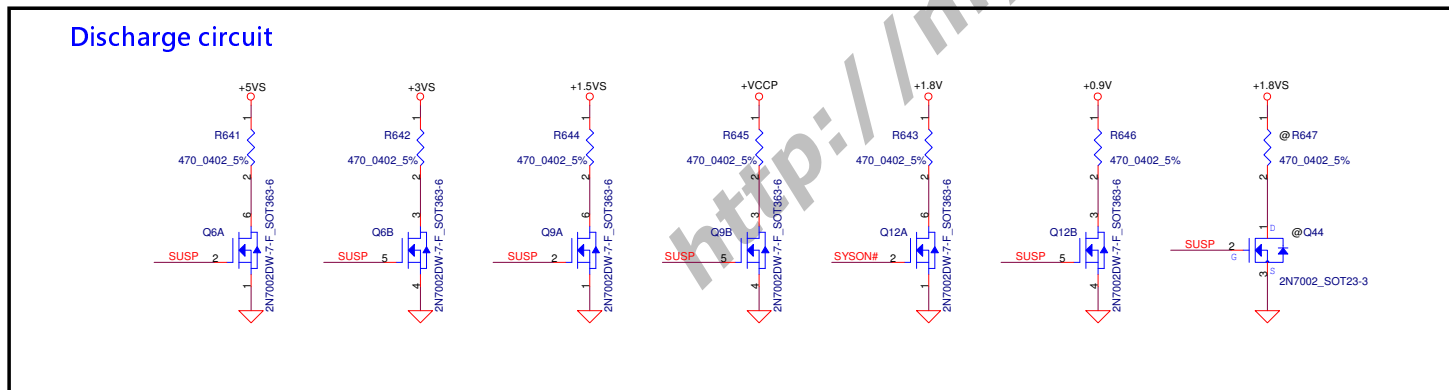
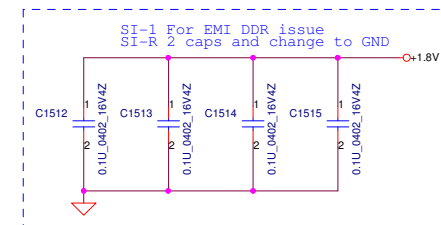
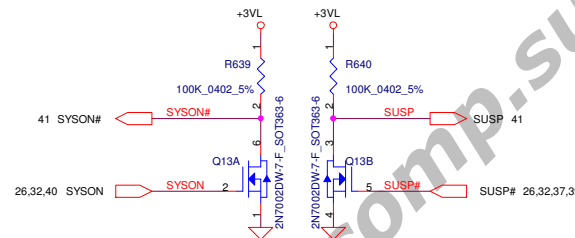
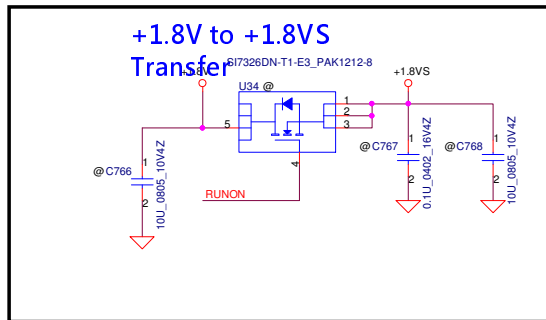
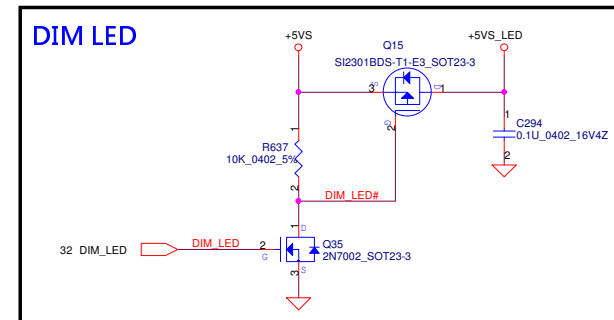
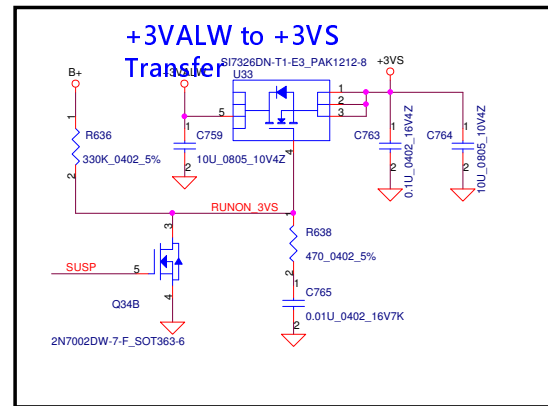
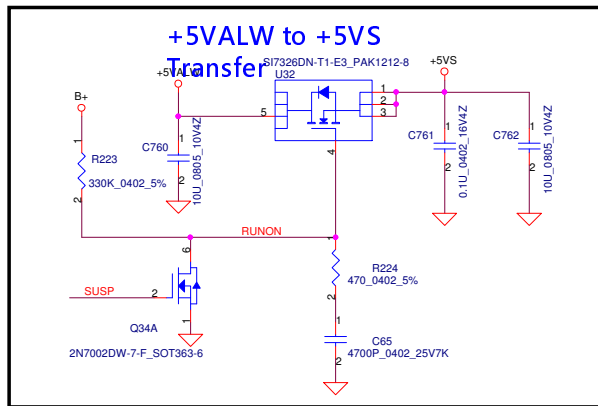
EMI request

<http://mycomp.su/x/>

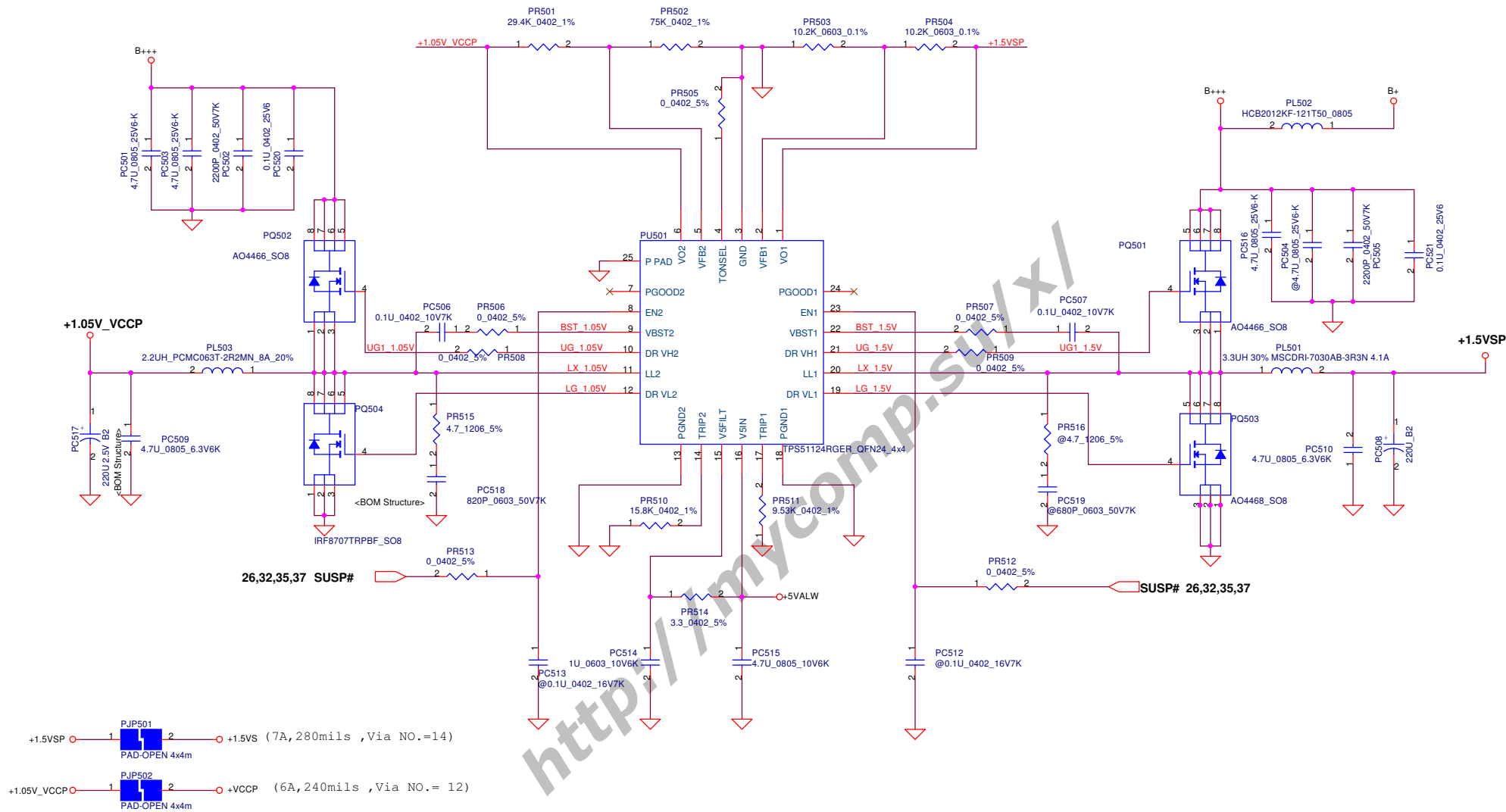
Security Classification	Compal Secret Data			Title	
Issued Date	2007/08/28	Deciphered Date	2006/07/26	BIOS ROM	
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				Montevina UMA	0.1
				Date: Wednesday, February 18, 2009	Sheet 31 of 46



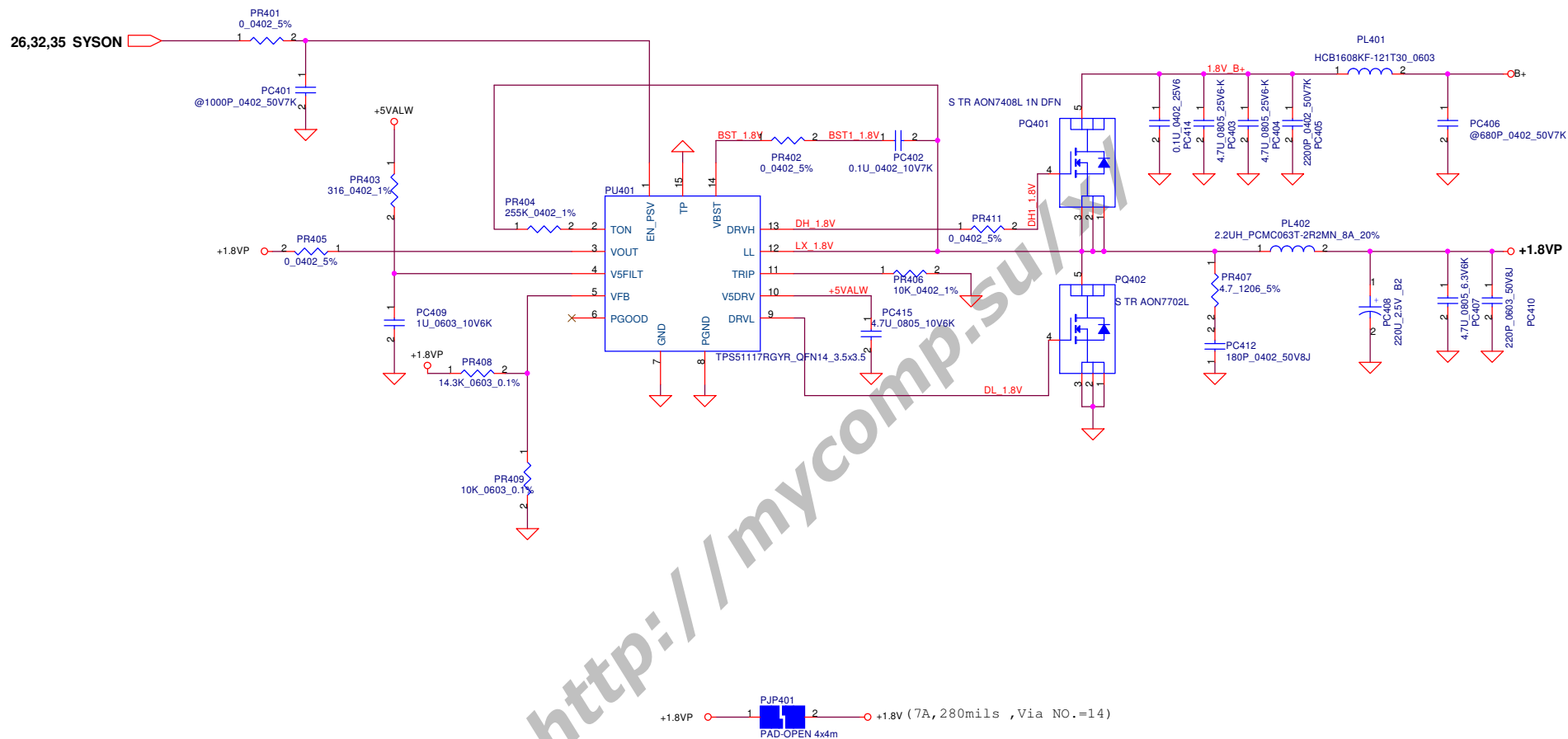
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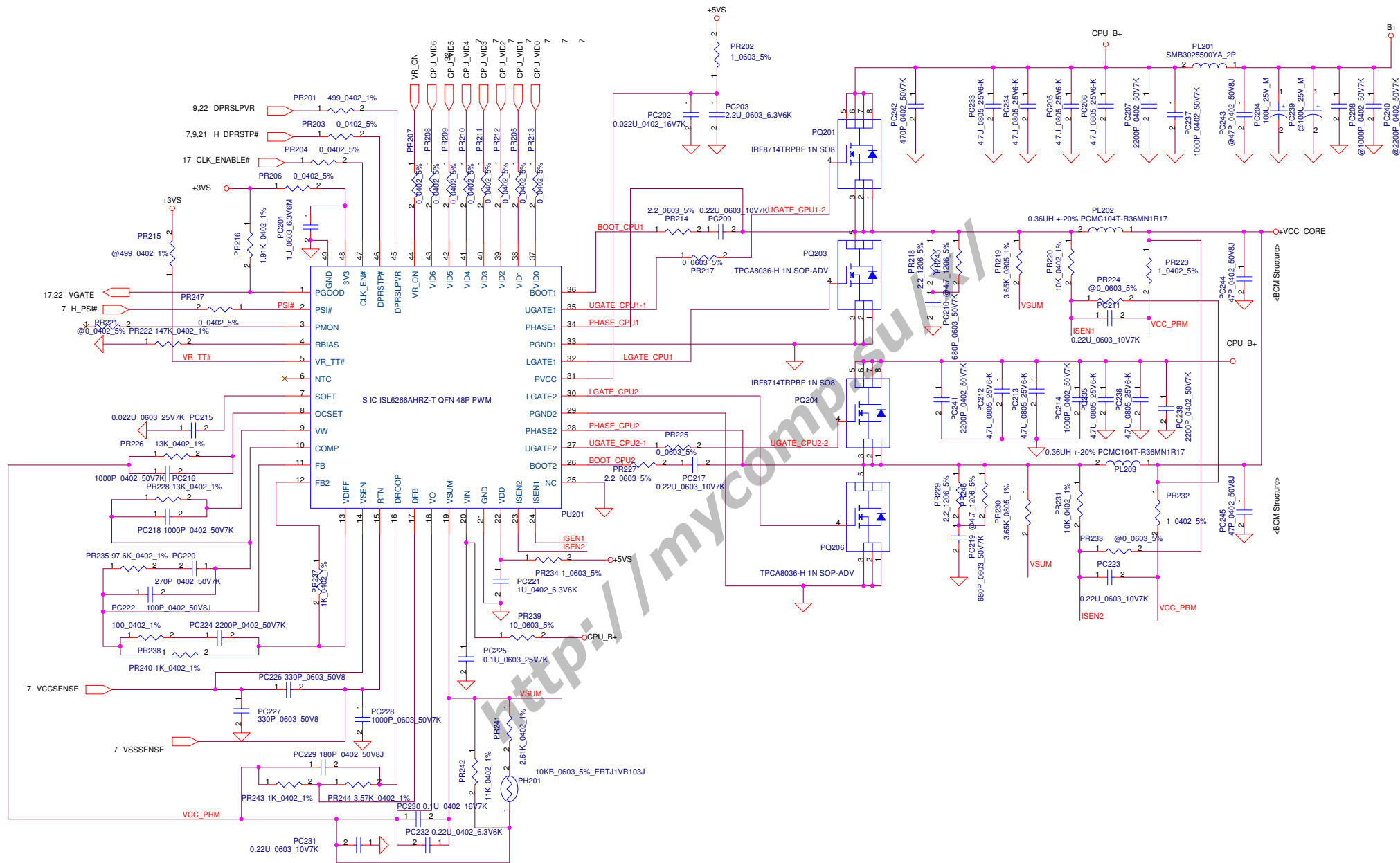
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Issued Date	2007/05/29	Deciphered Date	2008/05/29	Title	
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				Montevina Consumer Discrete	
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Issued Date	2007/05/29	Deciphered Date	2008/05/29	Title	
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				Date:	Wednesday, February 18, 2009
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Compal Electronics, Inc.

+CPU_CORE

Version Change List (P. I. R. List) for Power Circuit

[illegible]

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Issued Date	2007/08/02	Deciphered Date	2008/08/02	Title	
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Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	CardReader clock issue	17	Using USB_0 for CLK_48M_CR	2008/10/08	SI-1
2	Debug Card issue	26	Connect PLT_RST# to JP7.A17	2008/10/08	SI-1
3	SMT issue	29	Change IR1 to SCR00000E00	2008/10/08	SI-1
4	Add Audio board	29	Add JAUDIO for audio board	2008/10/08	SI-1
5	SW2 is for DB1 debug	33	Delete SW2	2008/10/08	SI-1
6	Cap board issue	33	Change Cap board power rail to +3VL	2008/10/08	SI-1
7	Support GM47	13	Add C1503 for GM47	2008/10/08	SI-1
8	Change FAN control circuit to voltage control	6	Add U51,D63	2008/10/08	SI-1
9	Delete HDA SSC	21	Remove U8 for layout spacing	2008/10/08	SI-1
10	For PR mini card connector	26	Add R1225 -- R1236	2008/10/08	SI-1
11	PA/PR CardReader LED	27	D54 for PA, D64 for PR	2008/10/08	SI-1
12	EMI request	28	Change R1132 to bead	2008/10/08	SI-1
13	Use audio board	29	Add audio board connector, change WIC to 2pin and add SPK connector	2008/10/08	SI-1
14	Change JFPR to 6 pin connector	30	Add Q109, C1518, R1210	2008/10/08	SI-1
15	EMI request	35	Add C1512 -- C1517	2008/10/08	SI-1
16	Change JFPR to 4 pin connector	30	Delete Q109, C1518, R1210	2008/11/21	SI-R
17	Delete resistor for Debug card	26	Delete R1220-R1224	2008/11/21	SI-R
18	EMI request	35	Delete C1516,C1517 and connect to GND	2008/11/21	SI-R
19	For Intel DPST	19	Add R1237,R1238	2008/11/25	SI-R
20	EMI and WWAN request	17 28	Install C217, C218, C219, C435, C312, C316, C66, C67, C1478, C1479, C1480, C1481, D58, C1516, R1239, C327	2008/12/18	PV-1
21	Audio board connector	29	Change pin define	2008/12/18	PV-1
22	ST and Parade level shift	34	Add R for Parade	2008/12/18	PV-1
23	ESD request	33	Add C1518,D65,D66,D67	2008/1/19	MV-1
24	ESD/ EMI request	17 38 35 32	C217-C219, D5-D7, D45-D47, D20, C792-C815 no stuff	2008/2/13	MV-1
25	AUDIO issue	29	C1446, C1447 change to 0805 size	2008/2/13	MV-1
26	PC Beep issue	28	change to analog GND and add separate diode	2008/2/13	MV-1
27					
28					

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Item	Fixed Issue	(Reason for change)	PAGE	Modify List	Date	Phase
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