

# Compal confidential

## JBK00 LA-4091P Schematics Document

Mobile AMD S1G2 CPU with ATI  
RS780M & SB700 core logic

2007-10-30

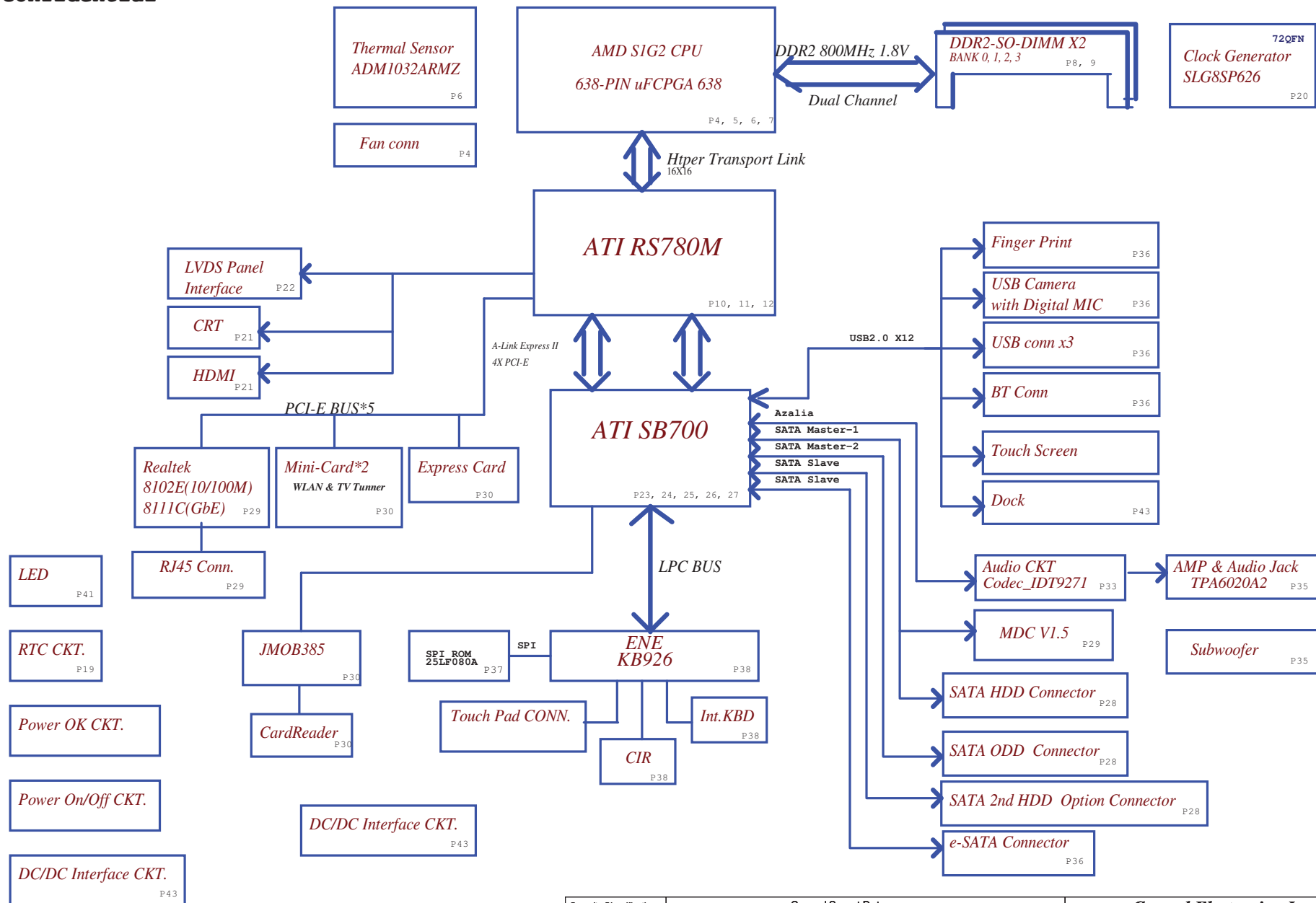
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	產出日期
	解密日期

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## Consumer AMD UMA 17"



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## Voltage Rails

○ MEANS ON X MEANS OFF

power plane State	+B +3VL	+5VALW +3VALW +1.2VALW	+1.8V +0.9V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +VGA_CORE +1.2V_HT +CPU_CORE_NB +CPU_CORE_0 +CPU_CORE_1
S0	○	○	○	○
S1	○	○	○	○
S3	○	○	○	X
S5 S4/AC	○	○	X	X
S5 S4/ Battery only	○	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

## Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build

DEBUG@ : means just reserve for debug.

 Layout Notes

UMA@ : means for RS780M.

## I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010
ACCELEROMETER	3A	00111010

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR CPU & ADM1032	SODIMM 1 / II	CLK CHIP	MINI_CARD Slot 2	LCD	HDMI	G-Sensor
SMB_EC_CK1	KB926	X	V	V	X	X	X	X	X	X	X
SMB_EC_DA1	KB926	X	X	X	V	X	X	X	X	X	X
SMB_EC_CK2	KB926	X	X	X	V	X	X	X	X	X	X
SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	X	X
I2C_CLK	RS780M	X	X	X	X	X	X	X	V	X	X
I2C_DATA	RS780M	X	X	X	X	X	X	X	X	V	X
DDC_CLK0	RS780M	X	X	X	X	X	X	X	X	V	X
DDC_DATA0	RS780M	X	X	X	X	X	X	X	X	V	X
DDC_CLK1	RS780M	X	X	X	X	X	X	X	X	X	X
DDC_DATA1	RS780M	X	X	X	X	X	X	X	X	X	X
SCL0	SB700	X	X	X	X	V	V	X	X	X	V
SDA0	SB700	X	X	X	X	X	X	V	X	X	X
SCL1	SB700	X	X	X	X	X	X	V	X	X	X
SDA1	SB700	X	X	X	X	X	X	V	X	X	X
SCL2	SB700	X	X	X	X	X	X	X	X	X	X
SDA2	SB700	X	X	X	X	X	X	X	X	X	X
SCL3	SB700	X	X	X	X	X	X	X	X	X	X
SDA3	SB700	X	X	X	X	X	X	X	X	X	X

## EC SM Bus1 address

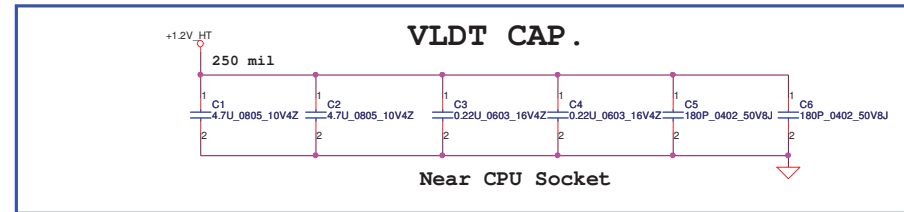
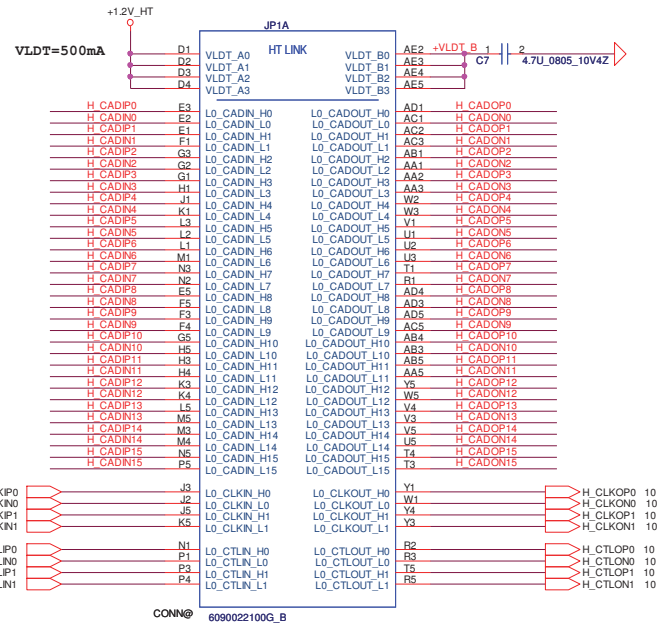
Device	HEX	Address
Smart Battery	16H	0001 011X b
24C16	A0H	1010 000X b
CPU SIC interface	98H	1001 100X b

## EC SM Bus2 address

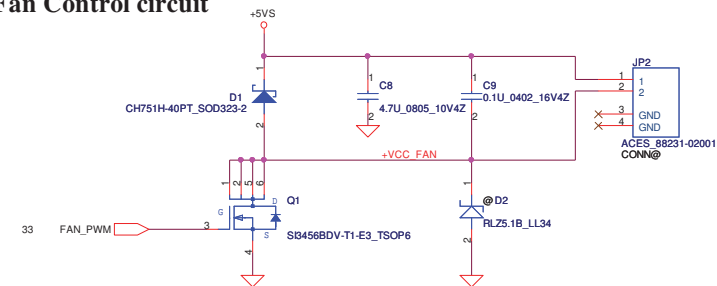
Device	HEX	Address
ADI1032-2 CPU	9AH	1001 101X b

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10 H\_CADIP[0..15] H\_CADIP[0..15] 10  
 10 H\_CADIN[0..15] H\_CADIN[0..15] 10

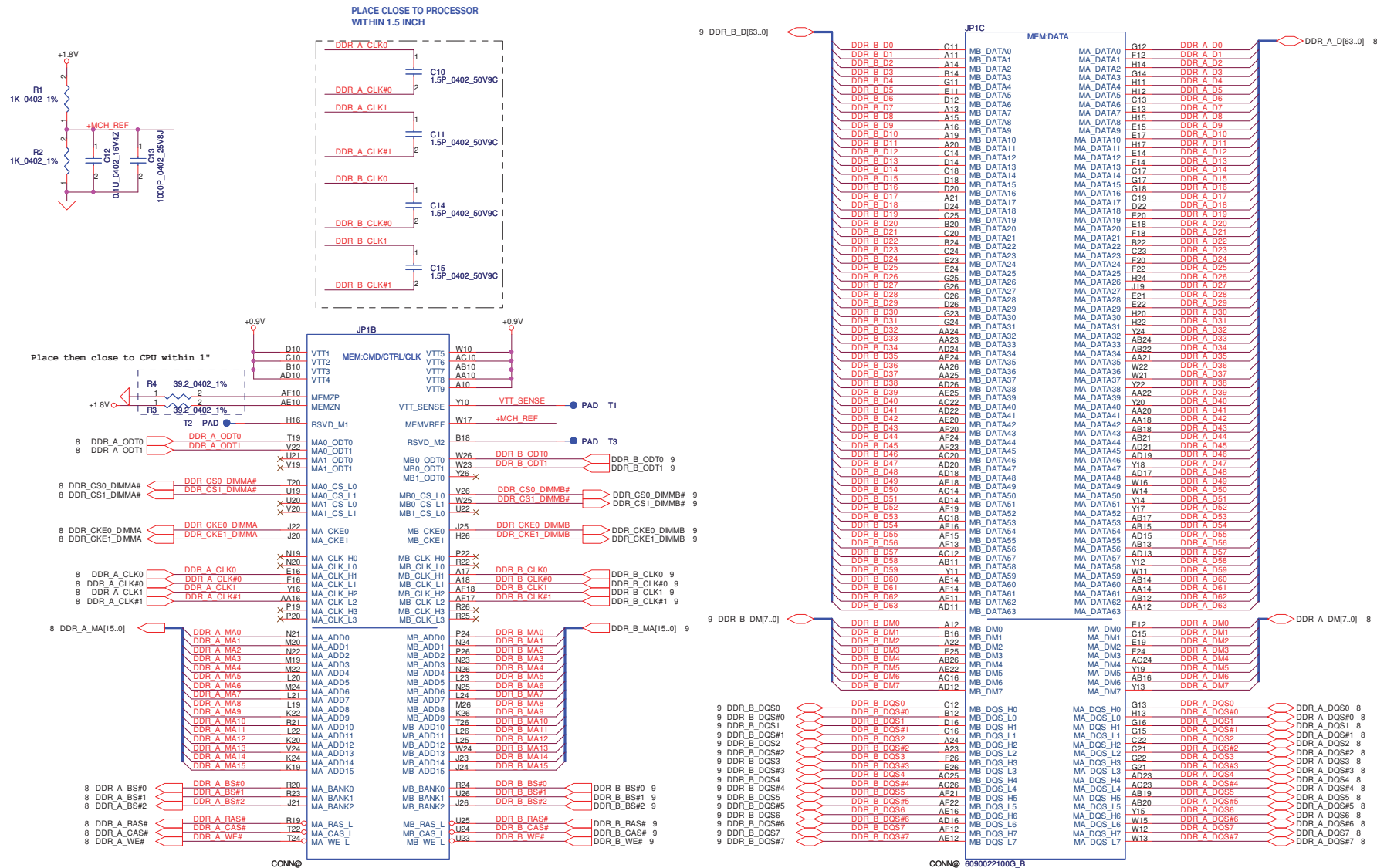


### PWM Fan Control circuit



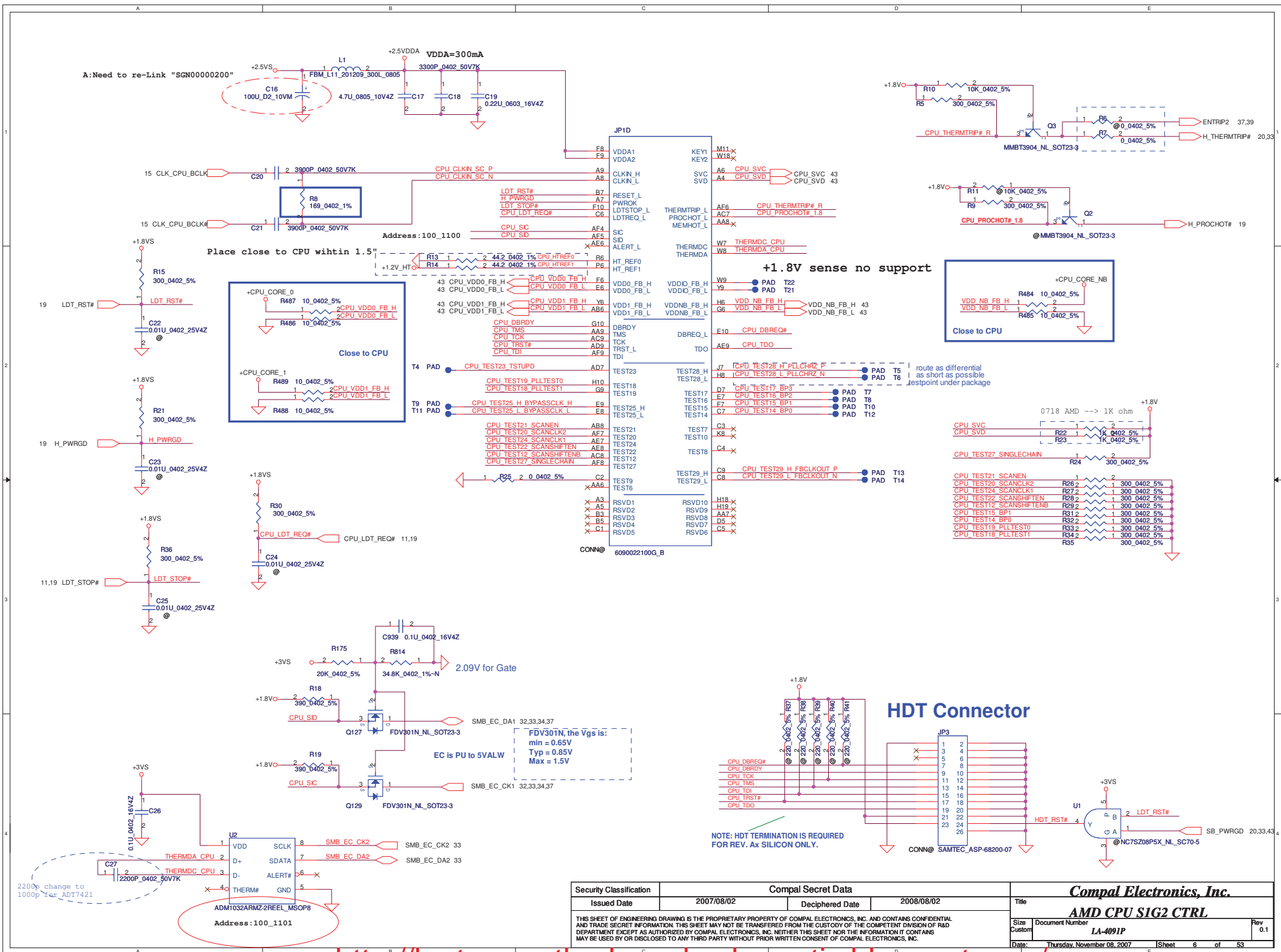
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# Processor DDR2 Memory Interface

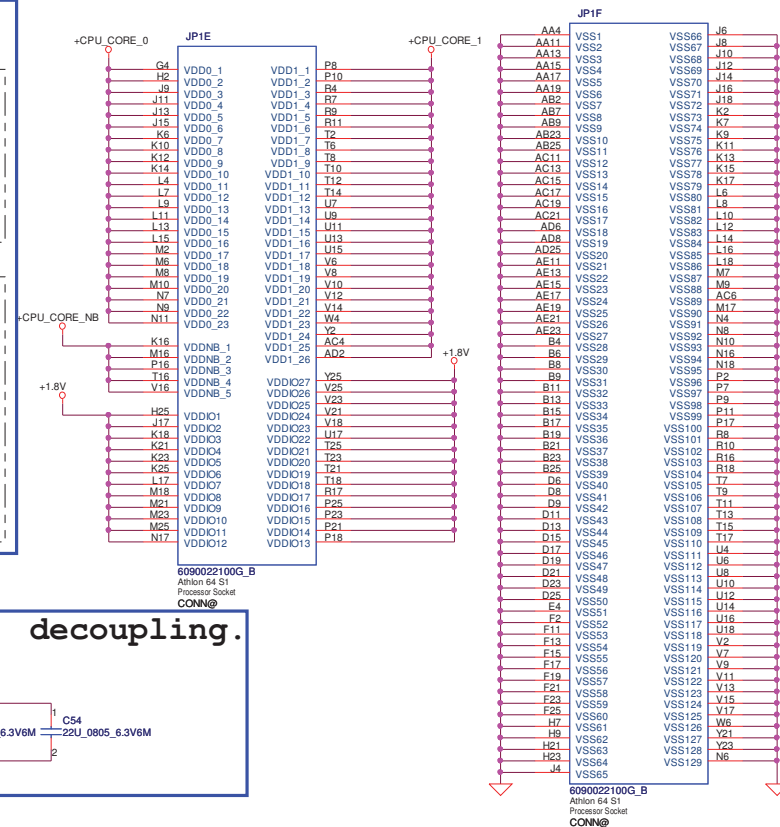
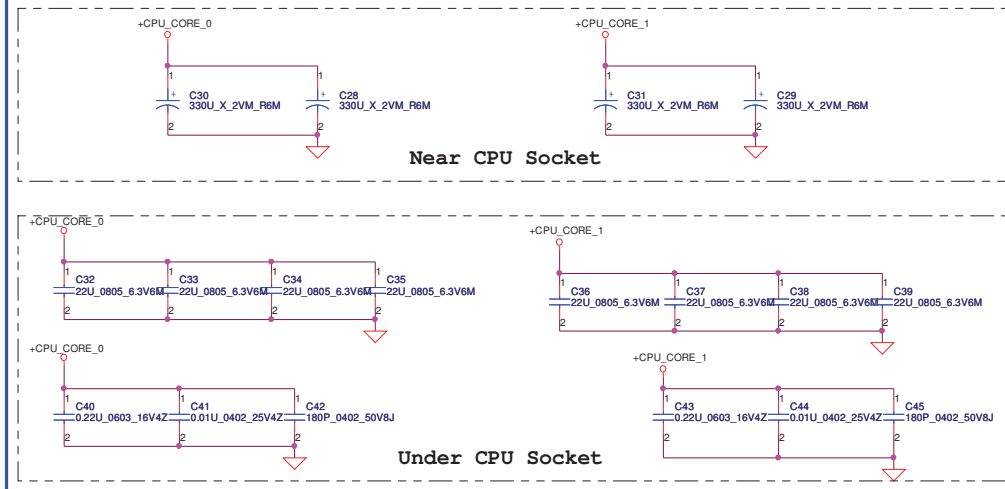


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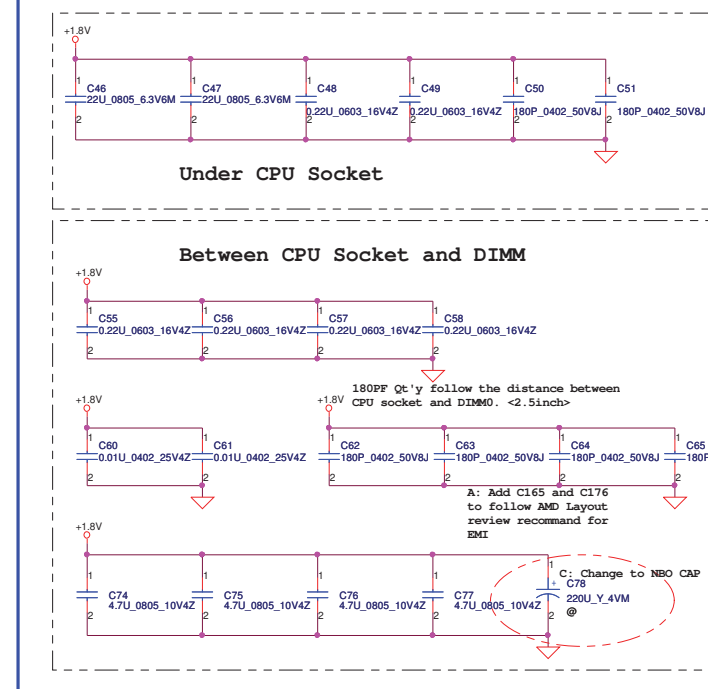
<http://laptop-motherboard-schematic.blogspot.com/>



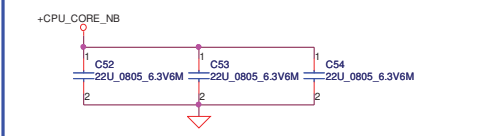
## VDD (+CPU\_CORE) decoupling.



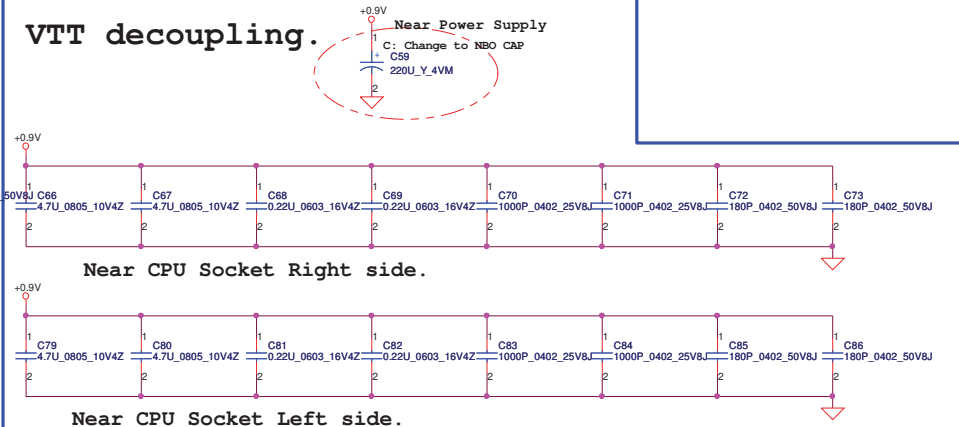
## VDDIO decoupling.



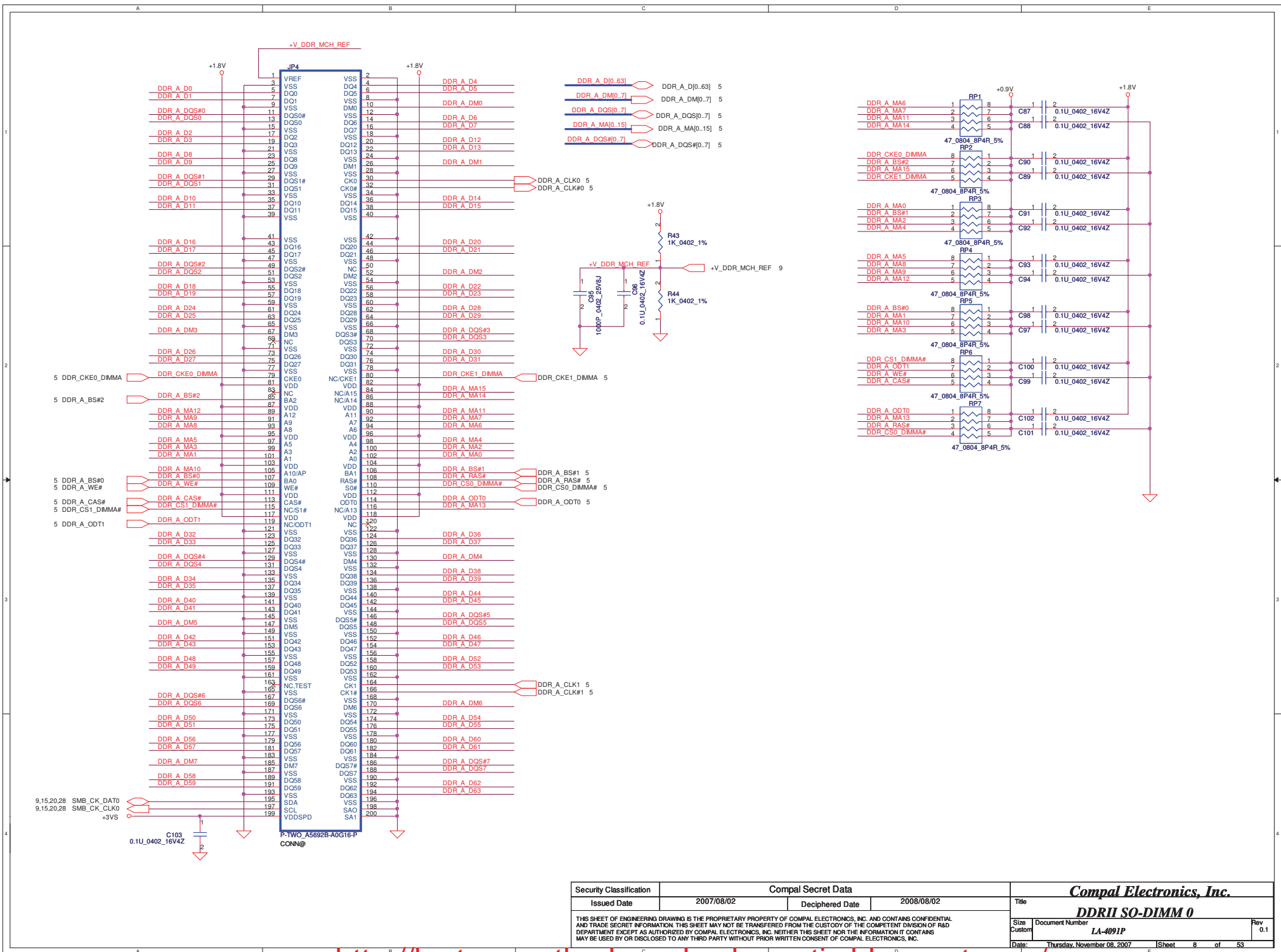
## +CPU\_CORE\_NB decoupling.



## VTT decoupling.



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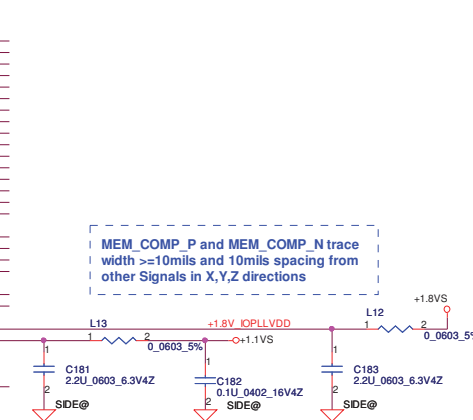
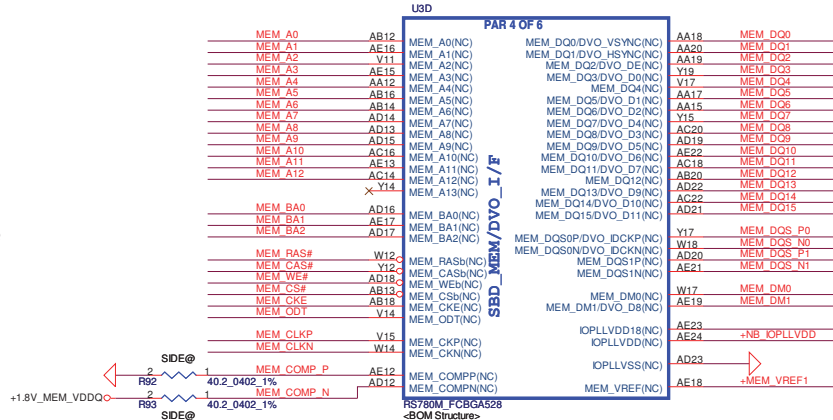
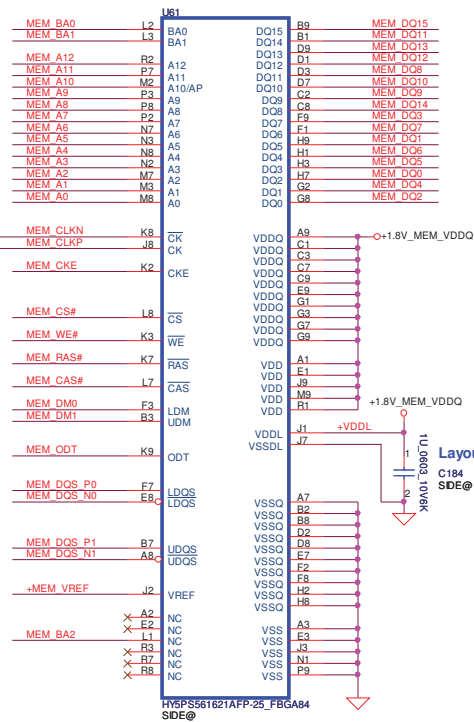




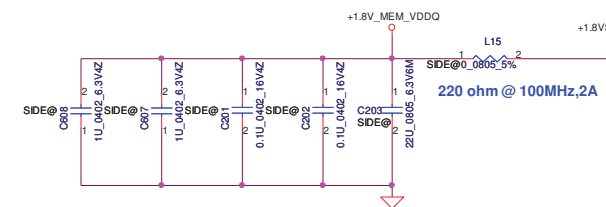
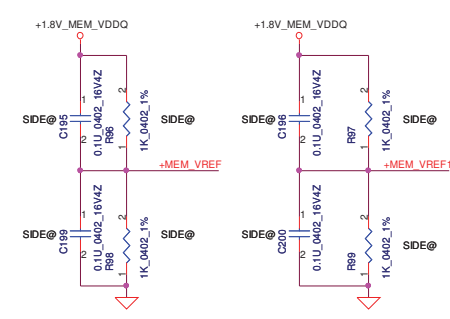






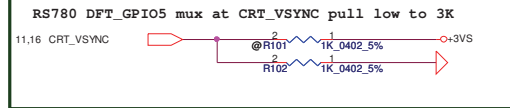


Layout Note: 50 mil for VSSDL



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**DFT\_GPIO5:STRAP\_DEBUG\_BUS\_GPIO\_ENABLEb**

Enables the Test Debug Bus using GPIO.

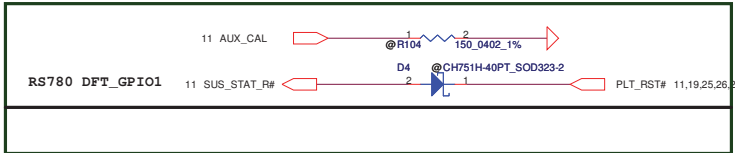
1 : Enable (RX780, RS780)  
0 : Disable (RX780, RS780)  
PIN: RS740-->RS780\_AUX\_CAL; RX780-->NB\_TV\_C; RS780--> VSYNC#

RS780 use register to control PCI-E configure

**DFT\_GPIO[4:2]: STRAP\_PCIE\_GPP\_CFG[2:0]**

These pin straps are used to configure PCI-E GPP mode.

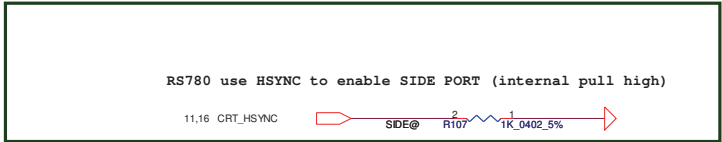
000 : 00001  
001 : 00010  
010 : 01011  
011 : 00100  
100 : 01010  
101 : 01100  
111 : 01011



**DFT\_GPIO1: LOAD\_EEPROM\_STRAPS**

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected  
RS740/RX780: DFT\_GPIO1 RS780:SUS\_STAT



**DFT\_GPIO0: STRAP\_DEBUG\_BUS\_PCIE\_ENABLEb**

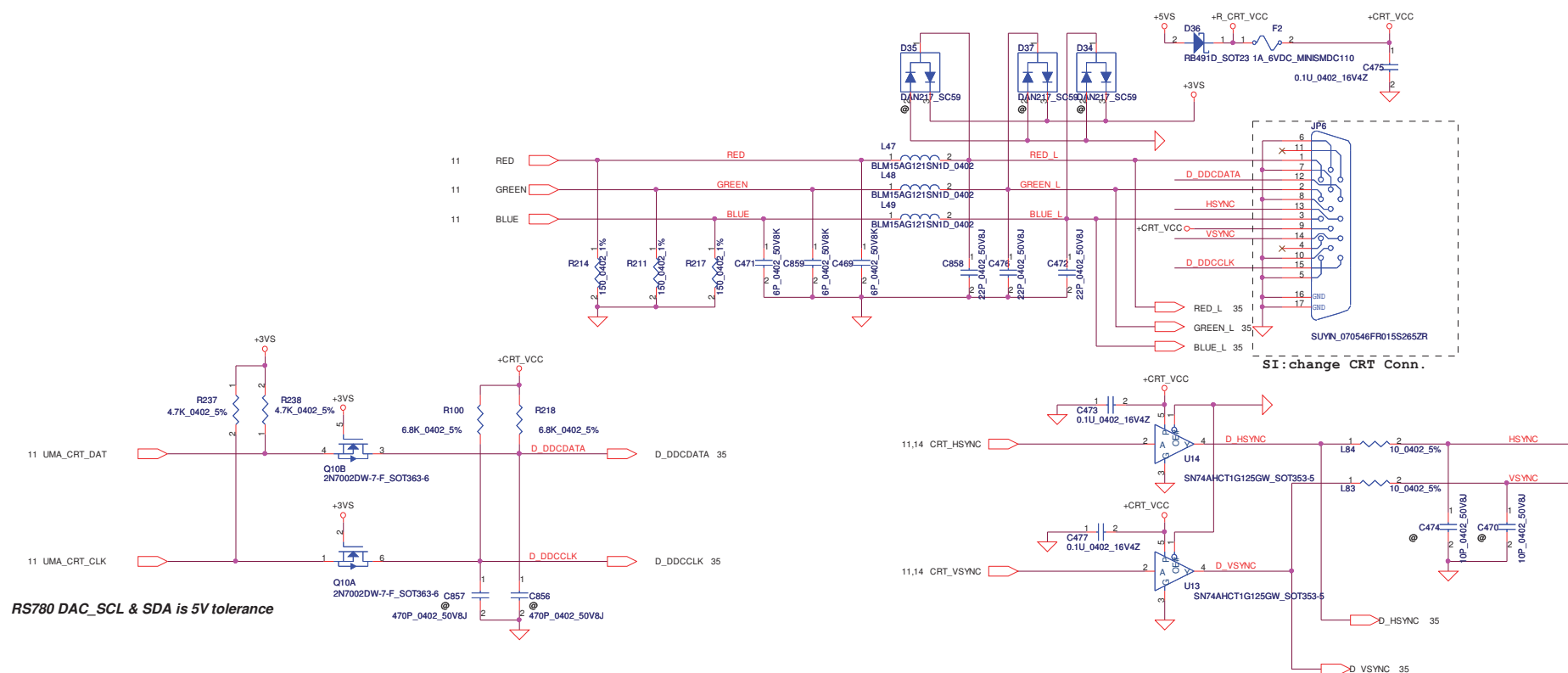
RX780: Enables the Test Debug Bus using PCIE bus  
1 : Disable ( Can still be enabled using nbcfg register access )  
0 : Enable

RS780: Enables Side port memory ( RS780 use HSYNC#)  
1. Disable (RS780)  
0 : Enable (RS780)

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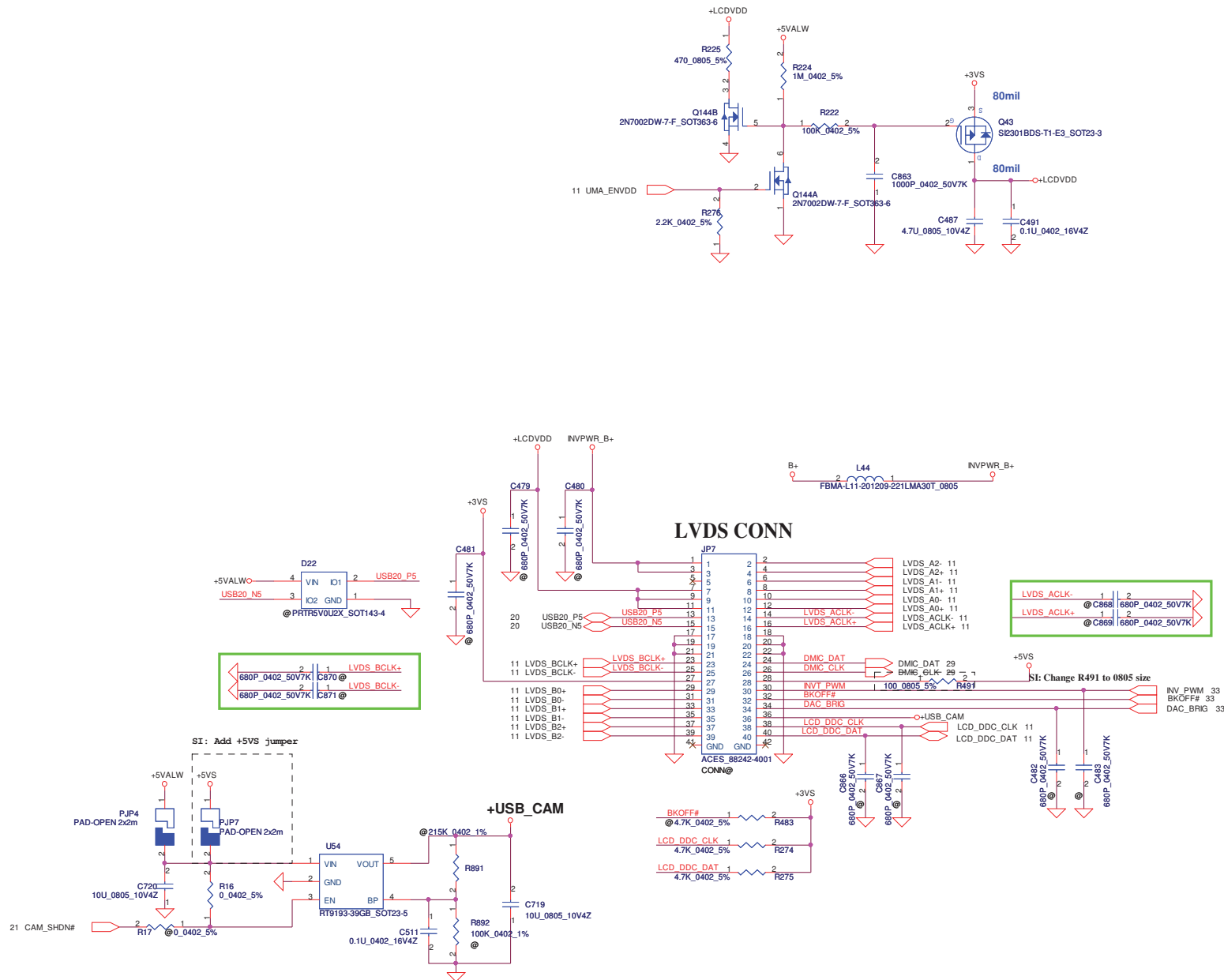


## CRT CONNECTOR

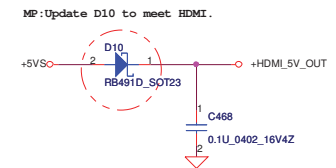
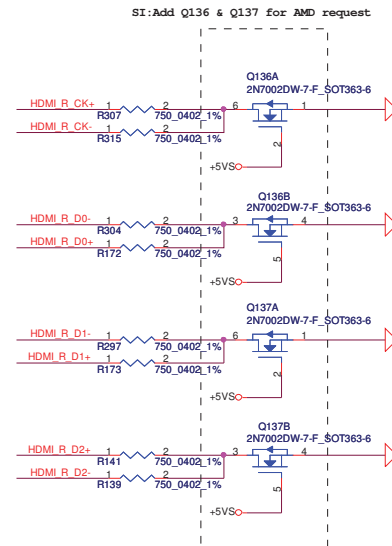
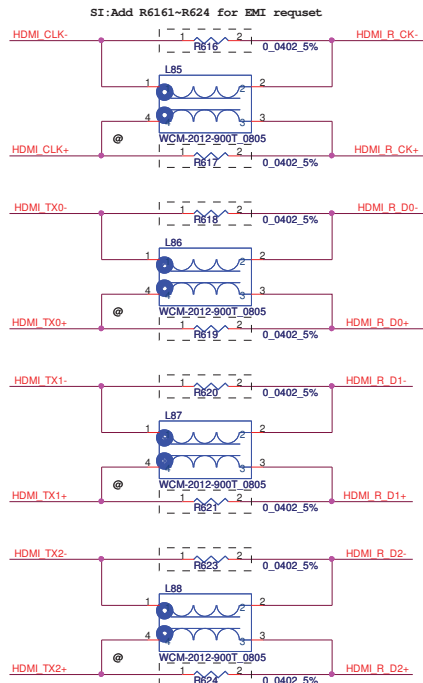
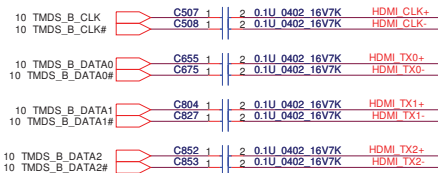
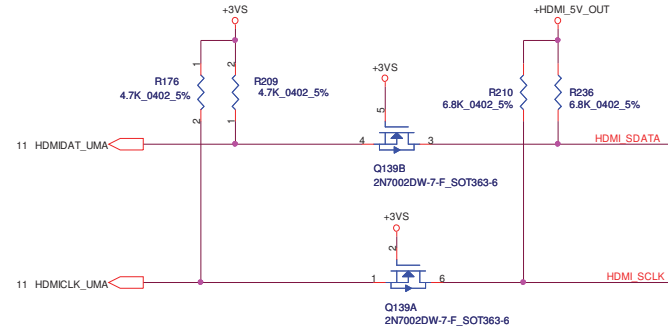
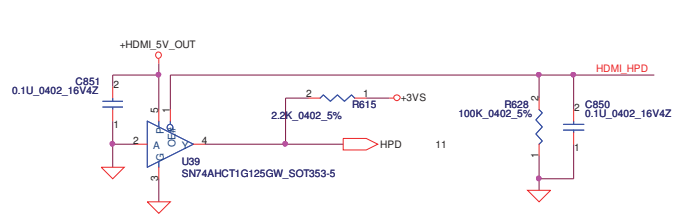


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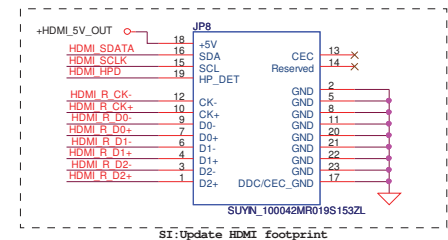




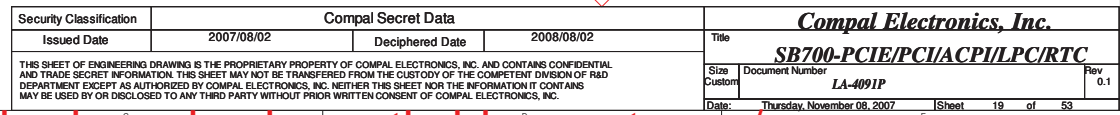
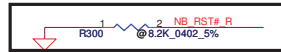
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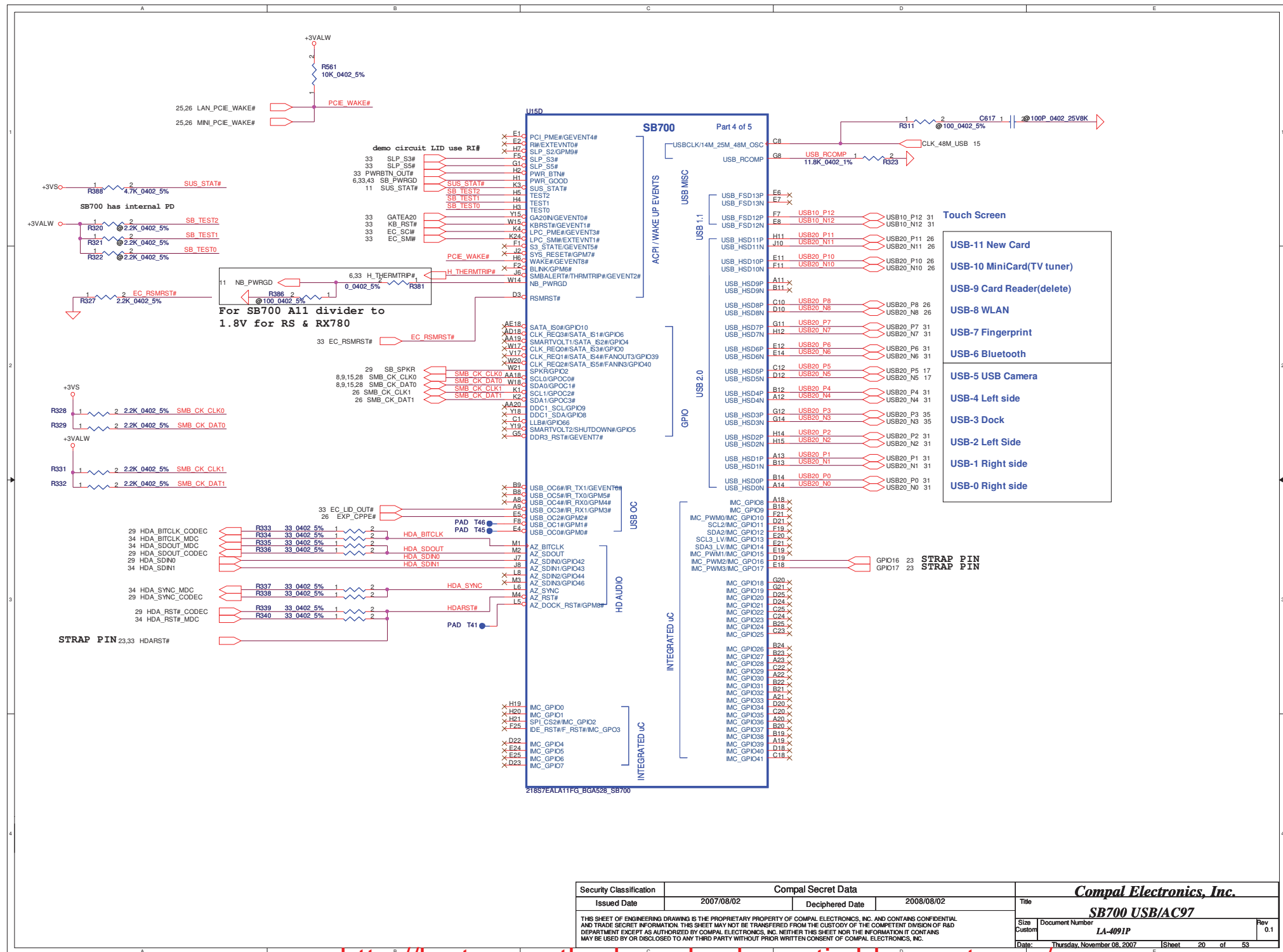


## HDMI Connector



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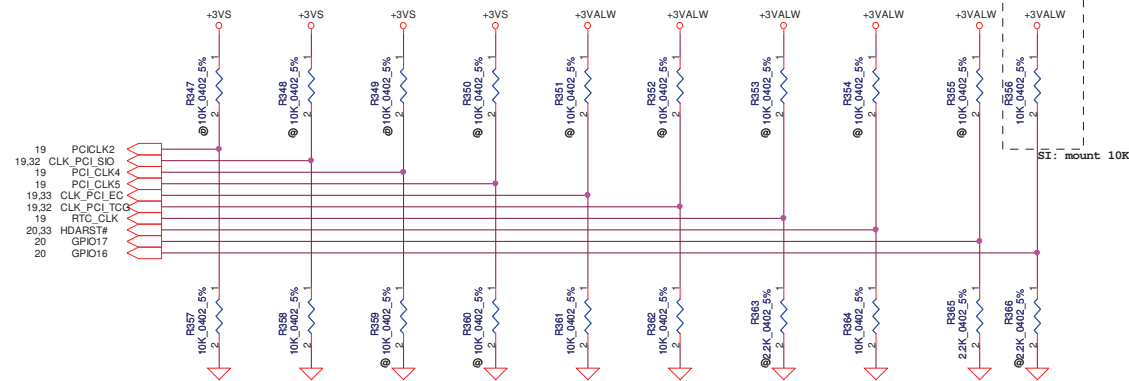




## REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC\_CLK

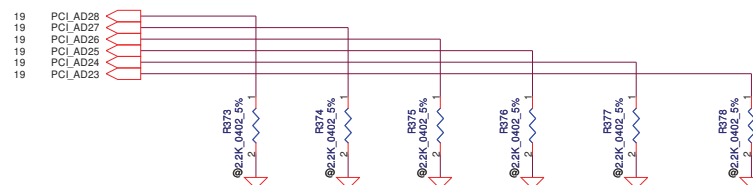
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
<b>PULL HIGH</b>	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC  DEFAULT	EC ENABLED	Internal pull up H,H = Reserved  H,L = SPI ROM	
<b>PULL LOW</b>	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM	



## DEBUG STRAPS

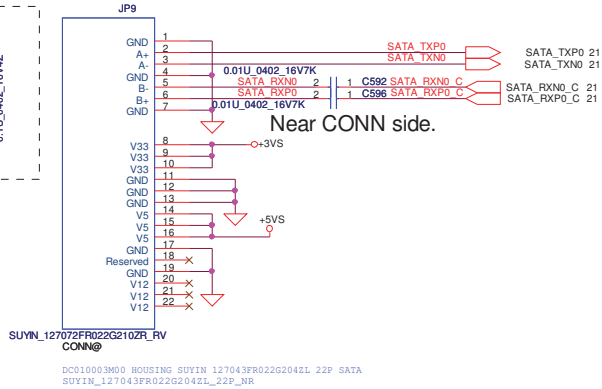
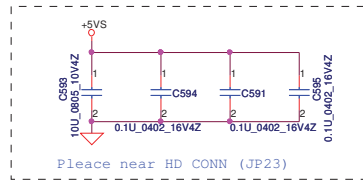
SB700 HAS 15K INTERNAL PU FOR PCI\_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
<b>PULL LOW</b>	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

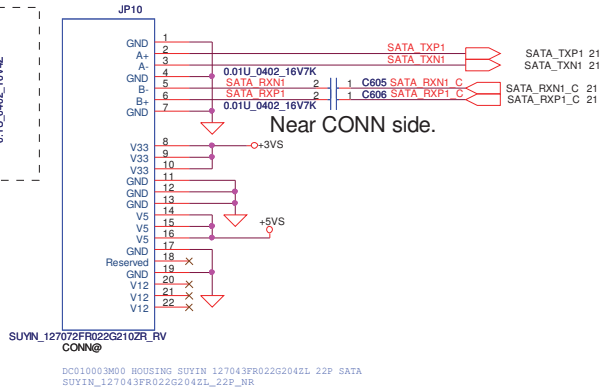
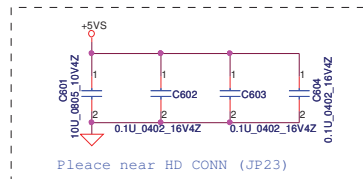


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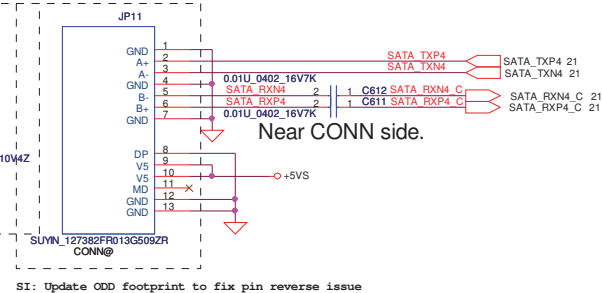
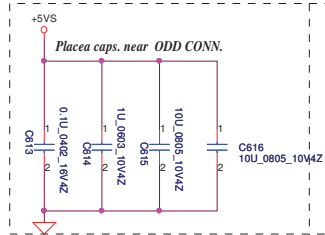
## HDD Connector



## 2nd HDD Connector-option

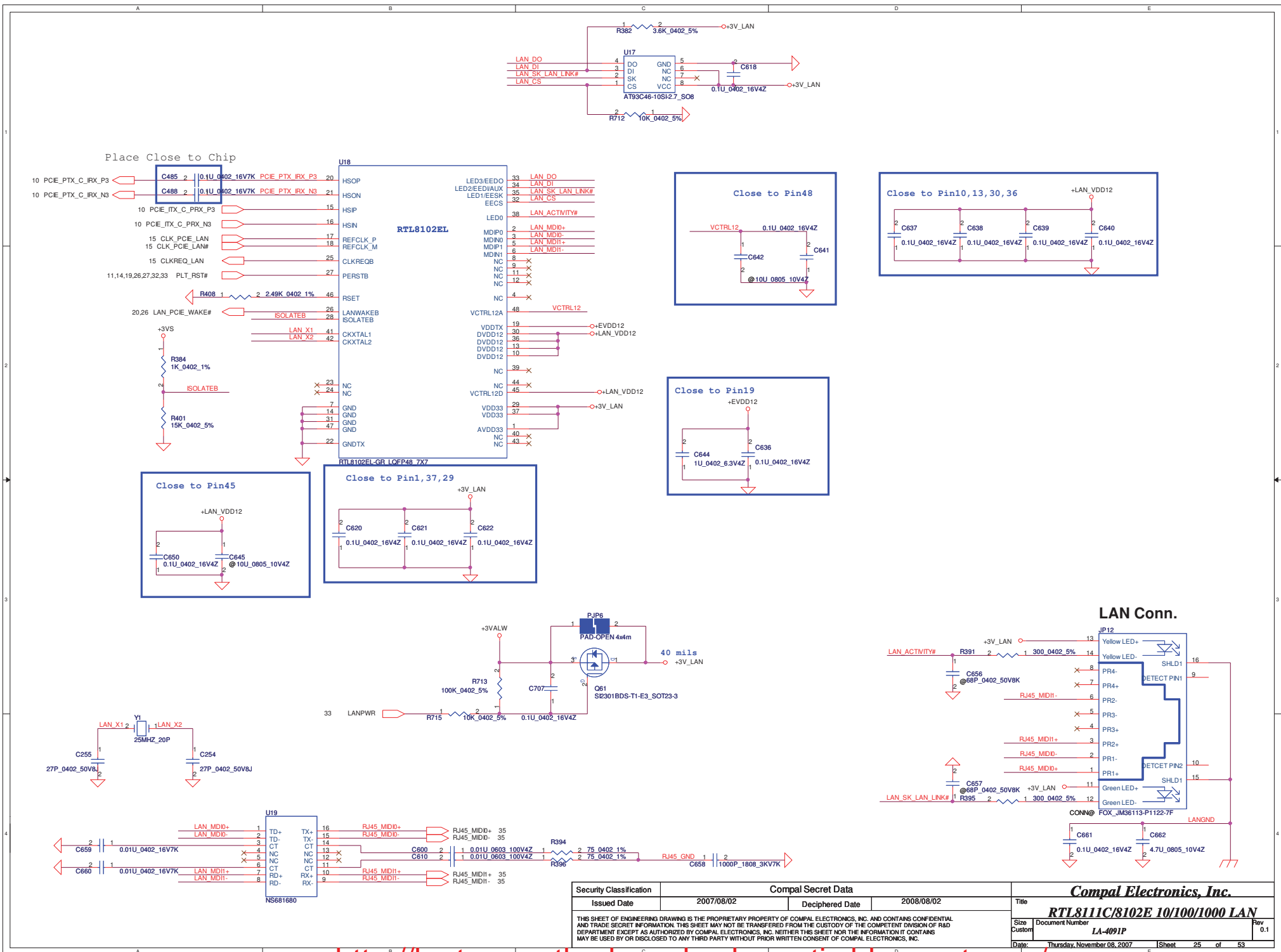


## CD-ROM Connector

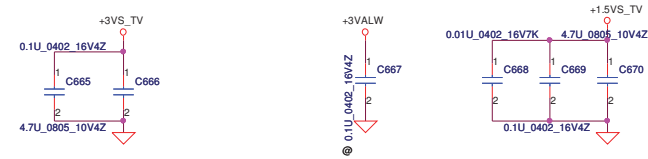


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				Custom	0.1
Date: Thursday, November 08, 2007				Sheet	24 of 53

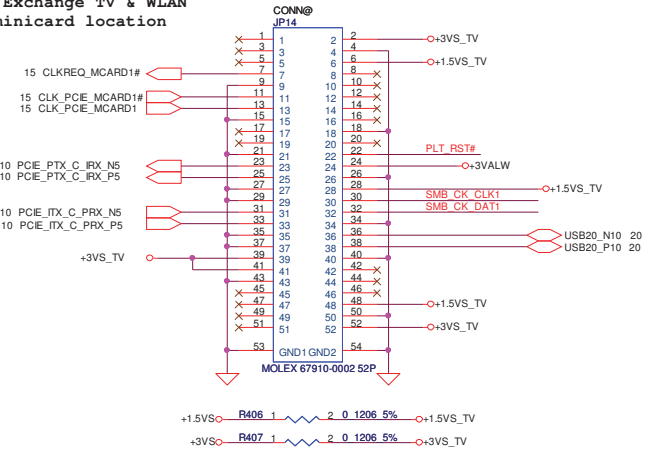




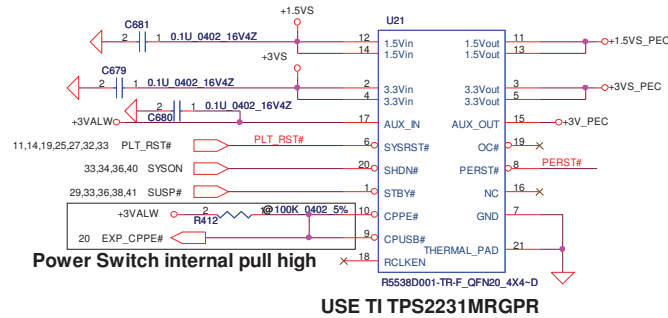
## Mini Card---TV tuner



SI: Exchange TV & WLAN  
minicard location

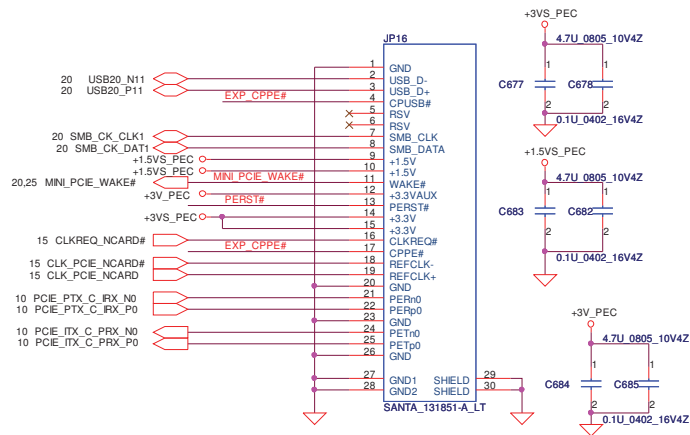


## New Card

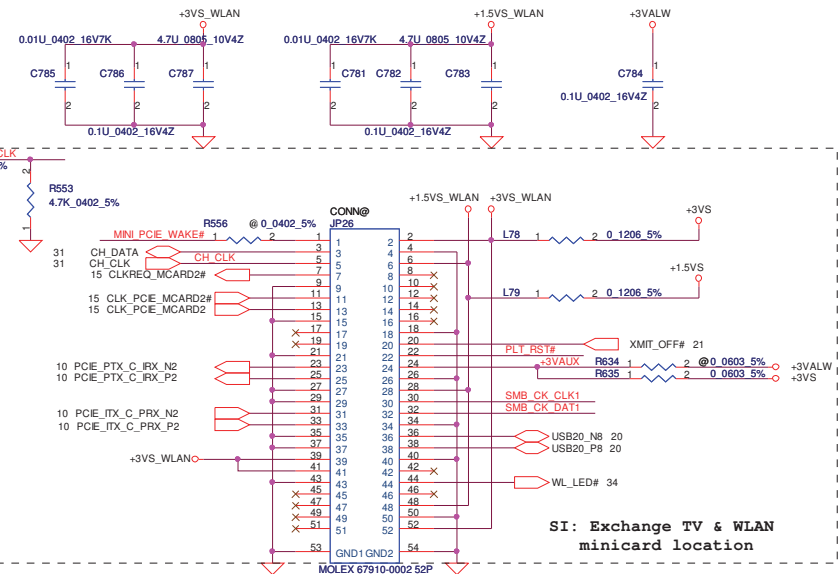


USE TI TPS2231MRGPR

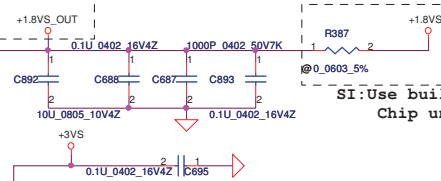
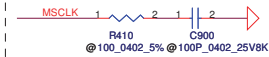
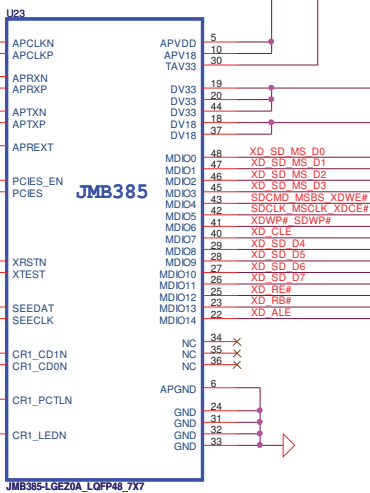
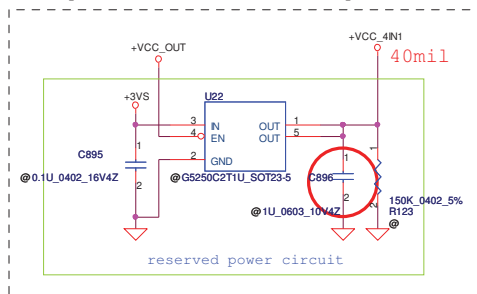
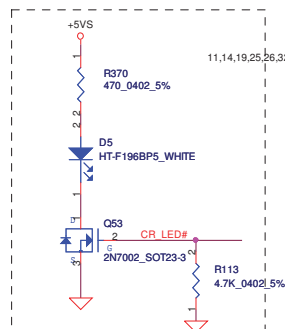
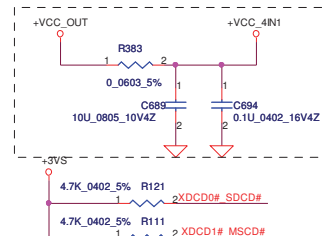
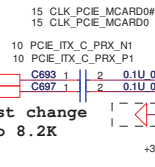
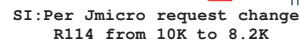
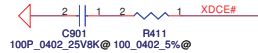
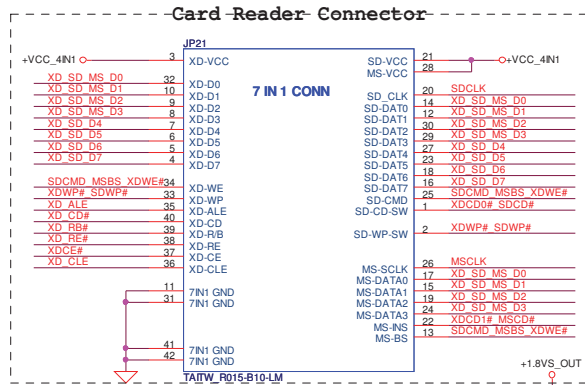
Near to Express Card slot.



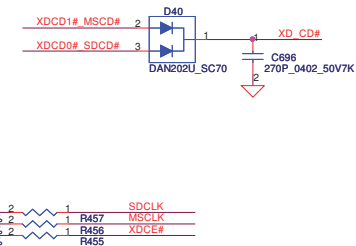
## Mini-Express Card---WLAN



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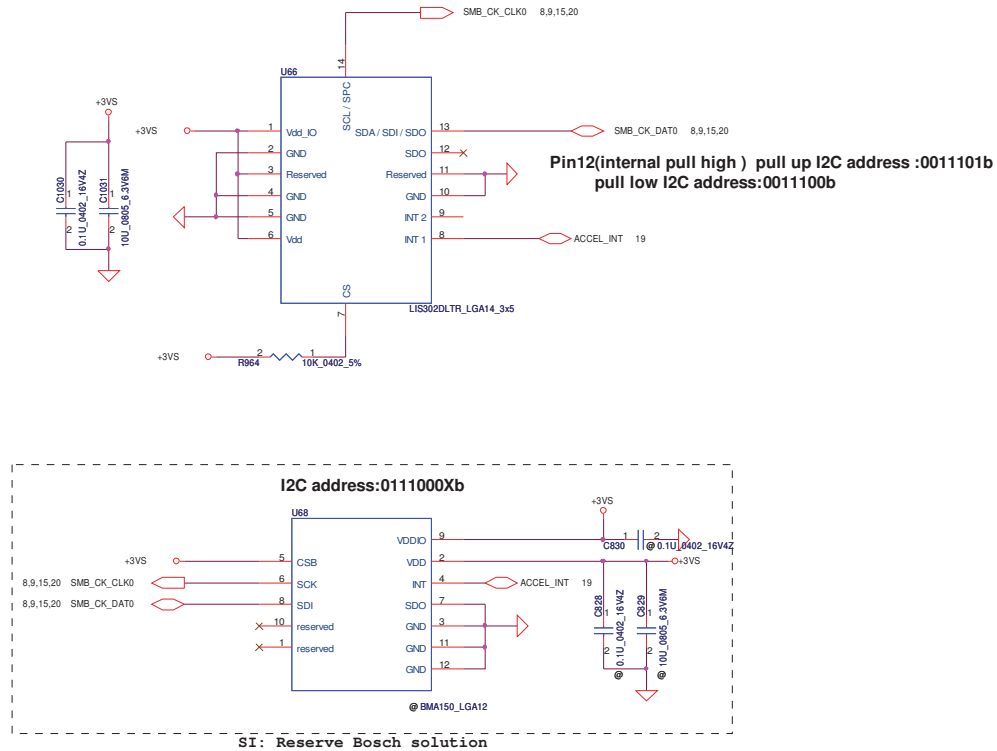


```
SI:Use build in Regulator
    Chip unmount R387
```

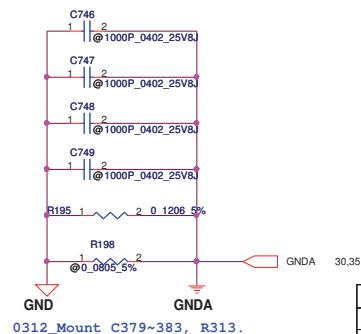
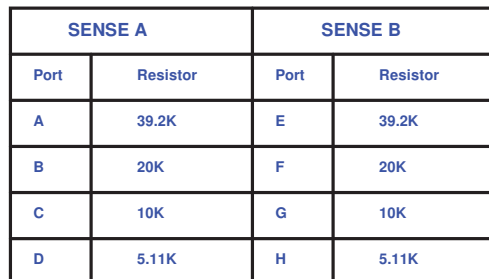
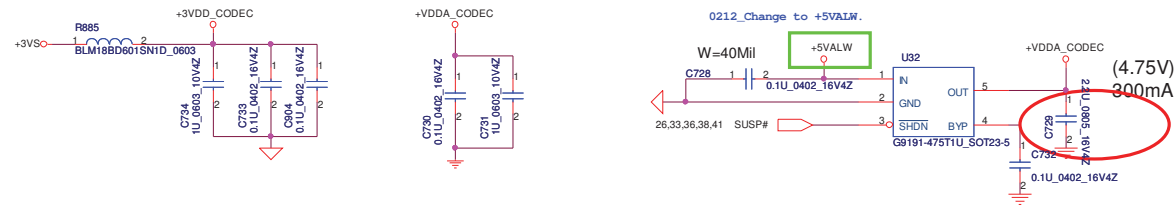


<http://laptop-motherboard-schematic.blogspot.com/>

## ACCELEROMETER



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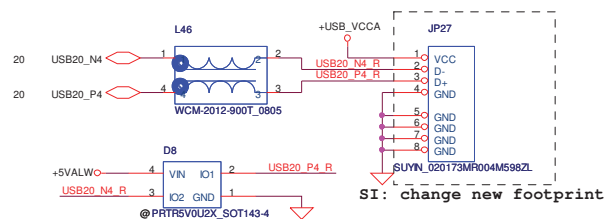
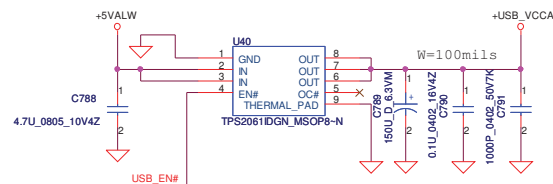


HP_DET#	MIC_DET	LINEOUT	PORT-A <Earphone OUT>	MIC	EQ
0 (LOW)	0 (LOW)	OFF	ON	ON	Disable
0 (LOW)	NC	OFF	ON	OFF	Disable
NC	0 (LOW)	ON	OFF	ON	Enable
NC	NC	ON	OFF	OFF	Enable

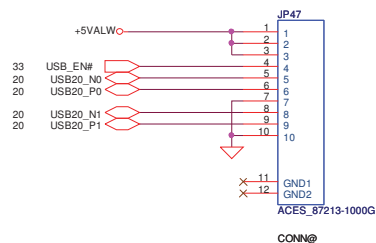
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Issued Date	2007/08/02	Deciphered Date	2008/08/02	Title	
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				Date: Thursday, November 08, 2007	Sheet 29 of 53



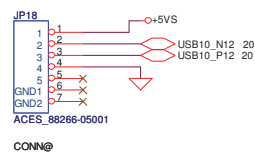
## Left side USB CONNECTOR 0



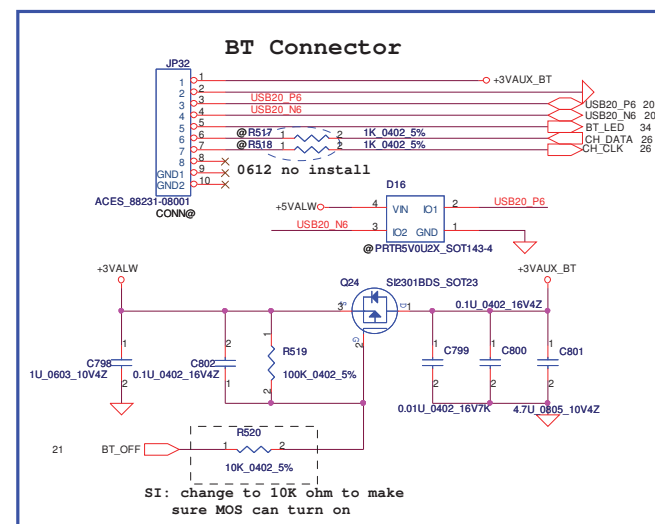
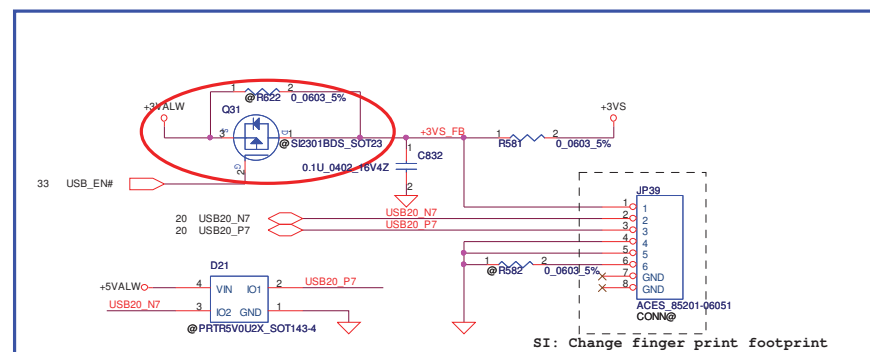
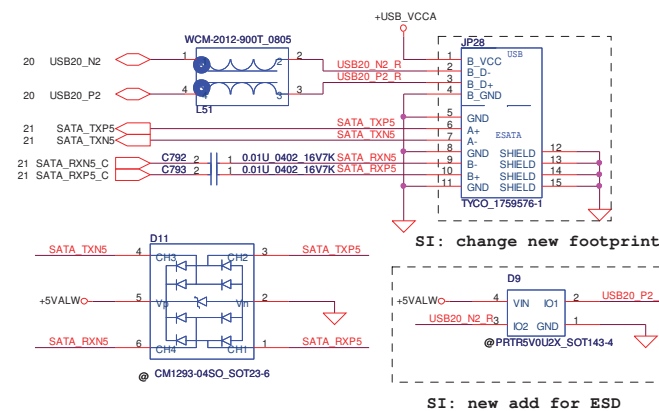
## USB Board Conn



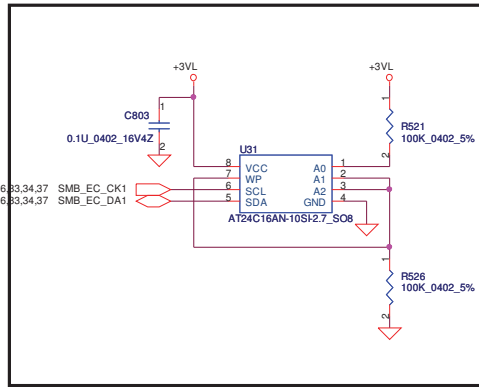
## Touch screen



Left side ESATA/USB combination Connector

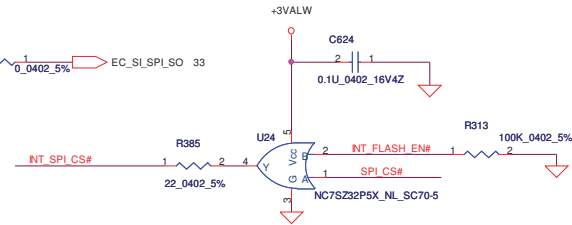
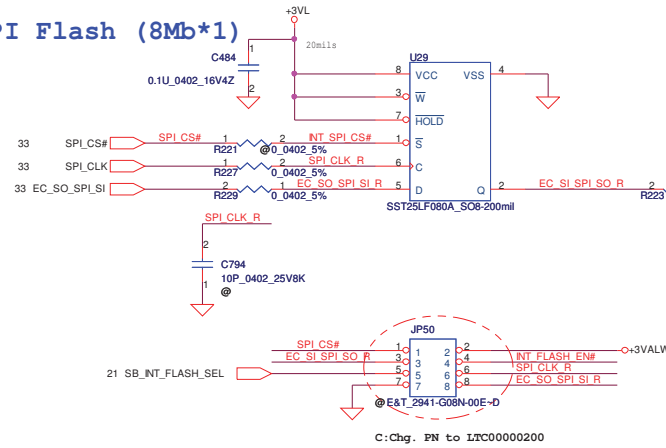


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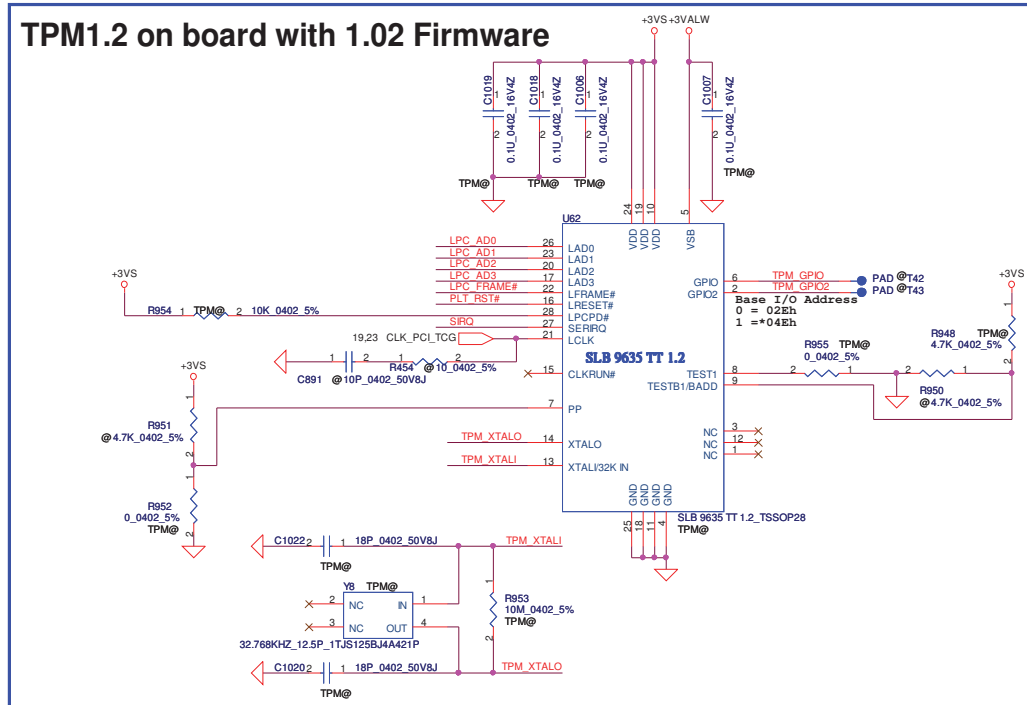


EEPROM need merge to BIOS ROM

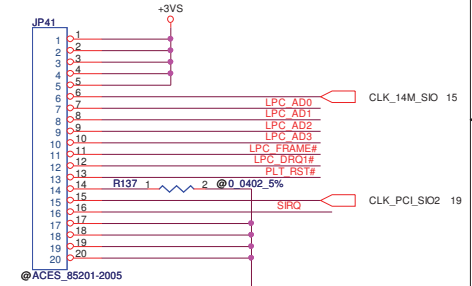
### SPI Flash (8Mb\*1)



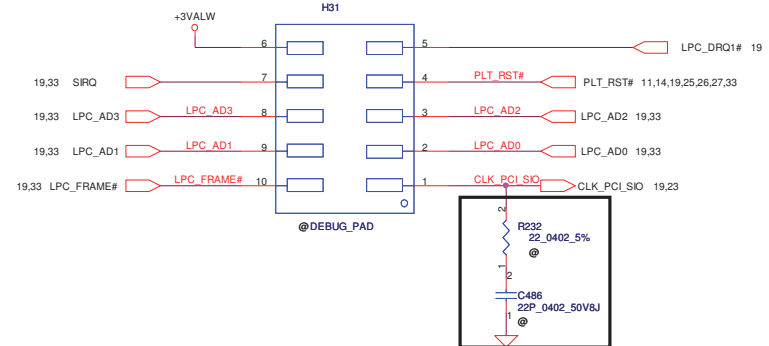
### TPM1.2 on board with 1.02 Firmware



### LPC Debug Port

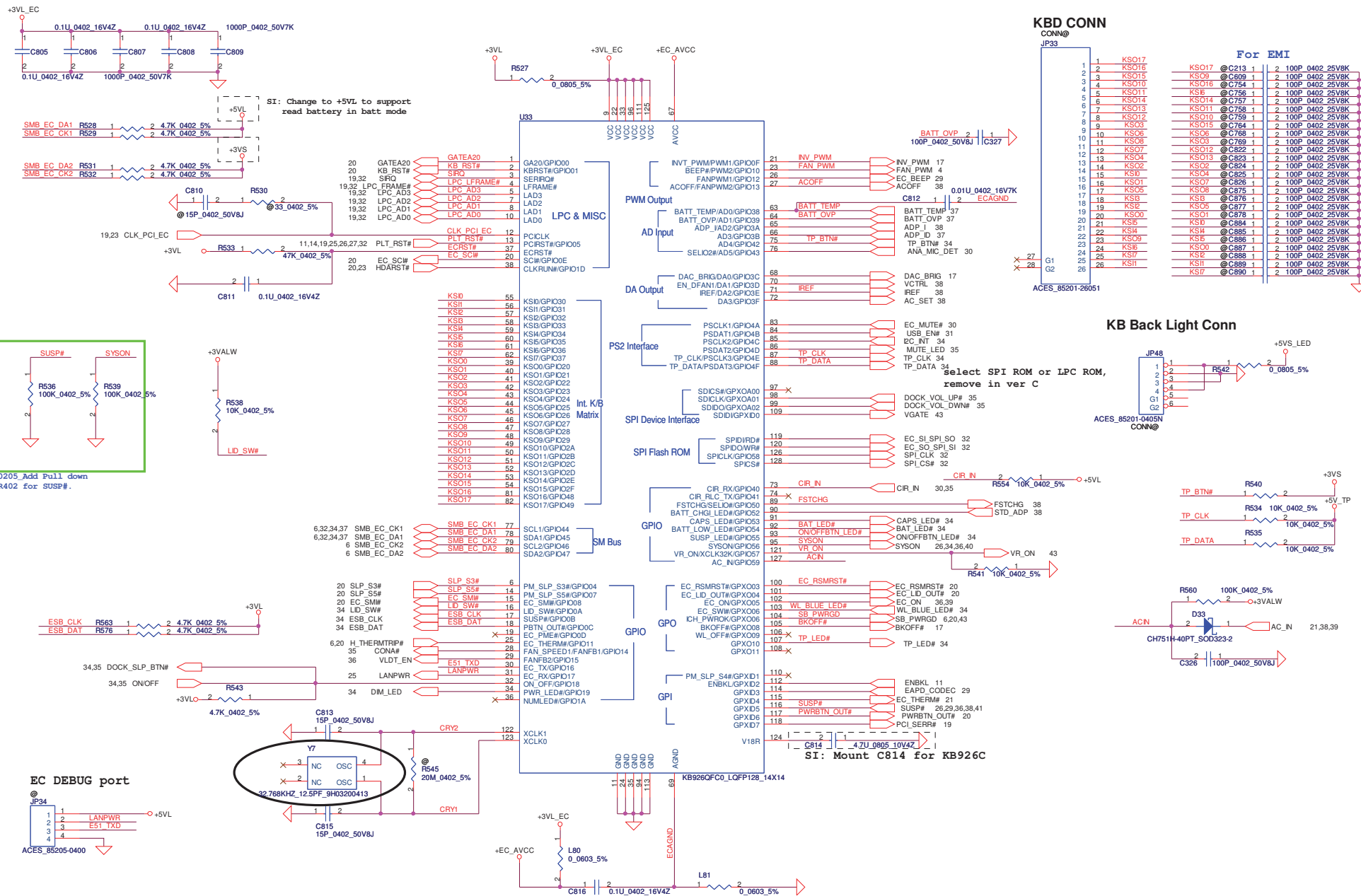


### LPC Debug Port



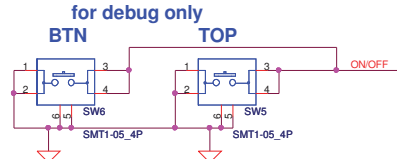
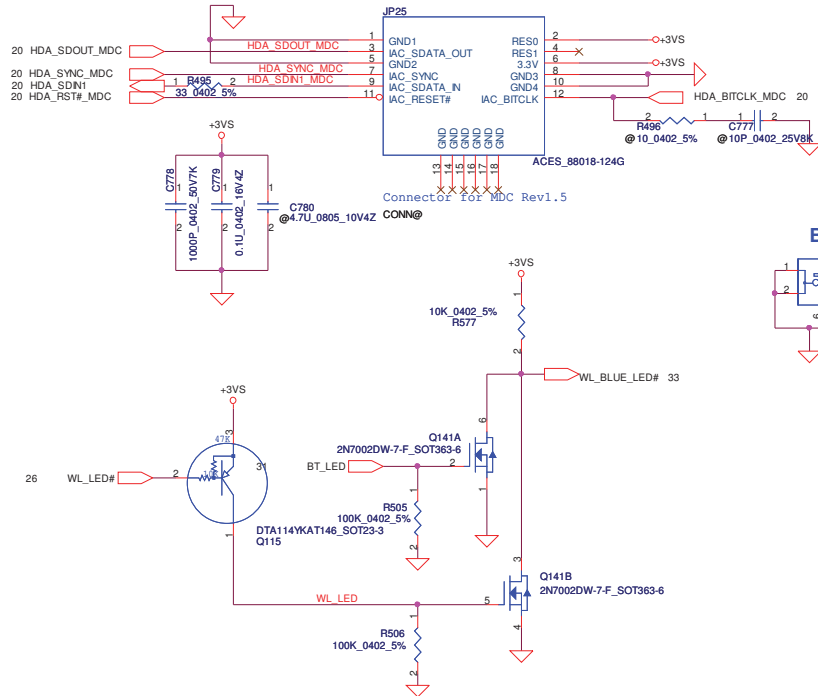
Security Classification		Compal Secret Data		Title	
Issued Date	2007/08/02	Deciphered Date	2008/08/02	TCG/BIOS ROM/PS2/LED/SW	
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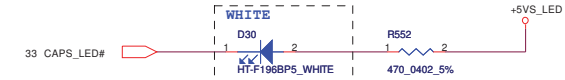
# MDC 1.5 Conn.

Change type 4/25

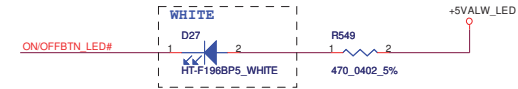


## CAPS LOCK LED

SI: Modify LED footprint



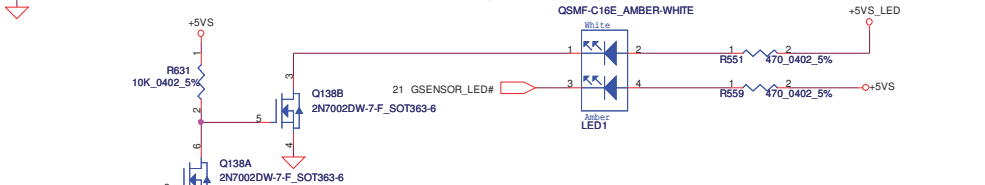
## POWER LED(Left 1)



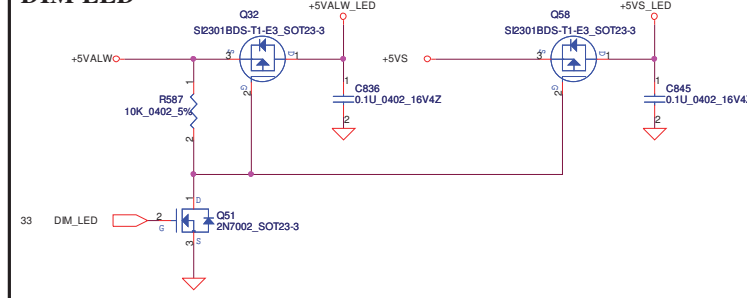
## Battery Charge LED(Left 2)



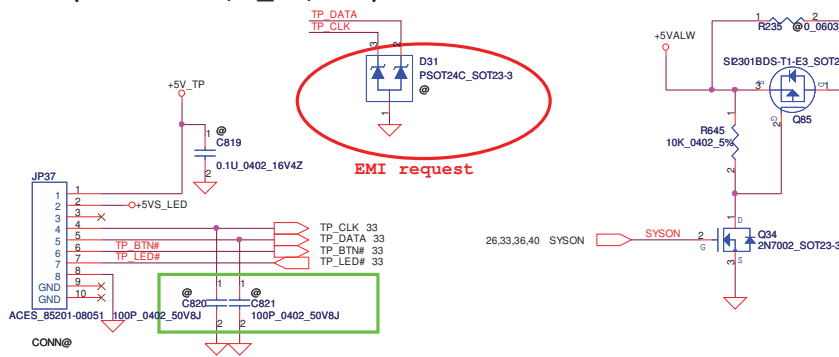
## HDD LED(Left 3)



## DIM LED

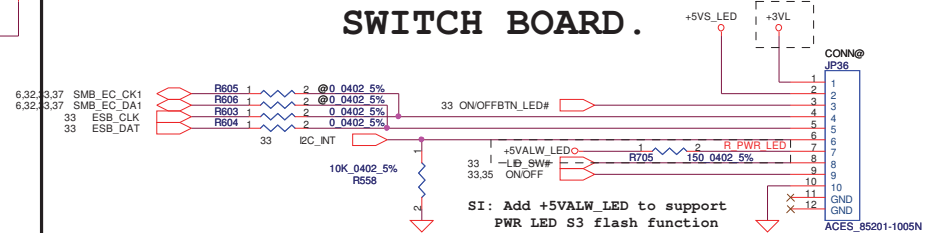


## T/P Board (Inculde T/P\_ON/OFF)



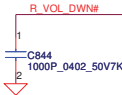
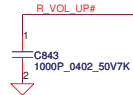
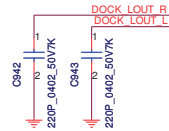
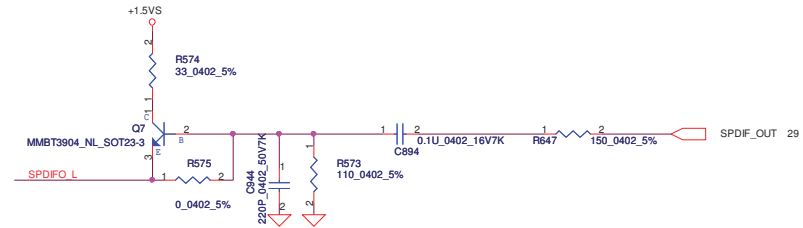
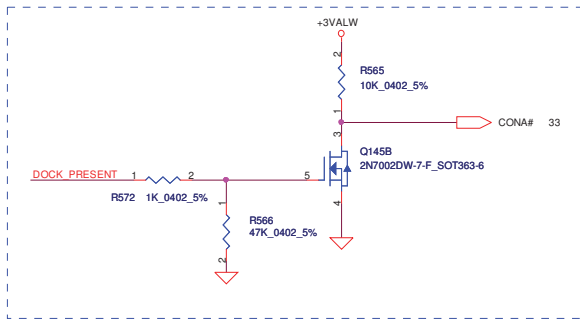
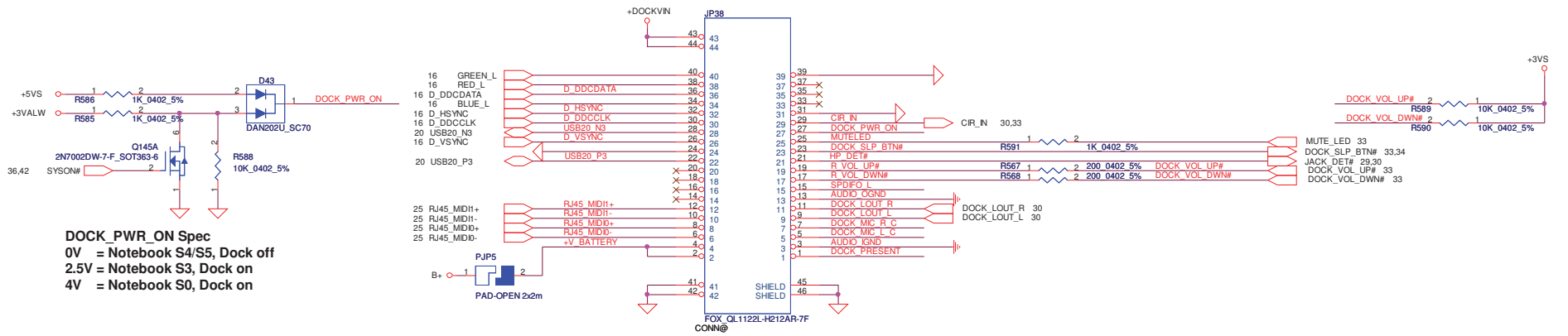
SI: Change to +3VL to support Qplay bottom boot in BATT mode

## SWITCH BOARD.



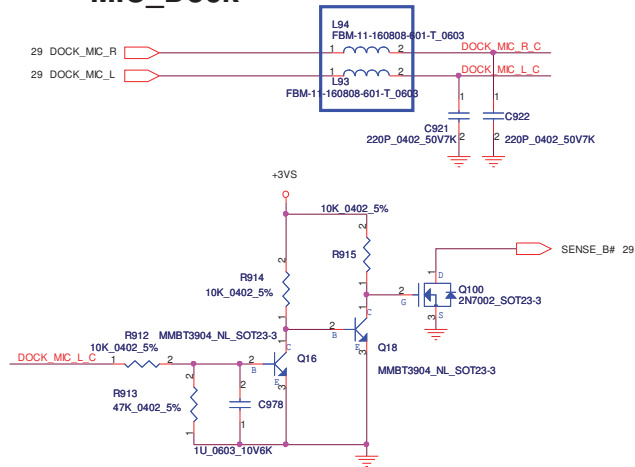
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# Atlas/ Saturn Dock



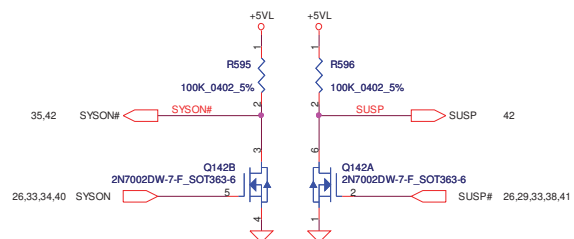
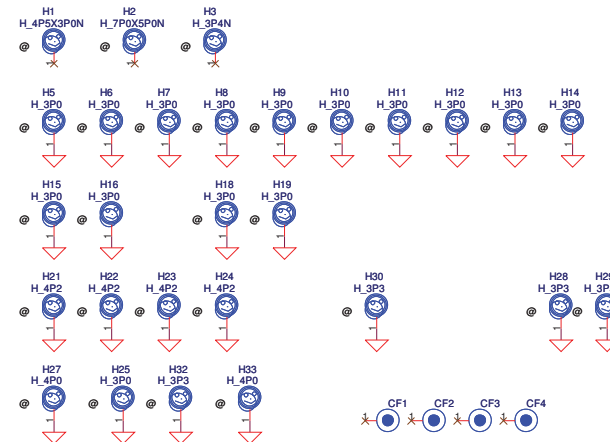
## MIC\_Dock

Need 600 Ohm 500 mA

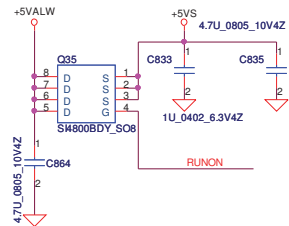


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				Date	Thursday, November 08, 2007
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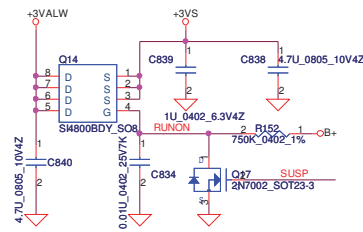
## Screw Hole



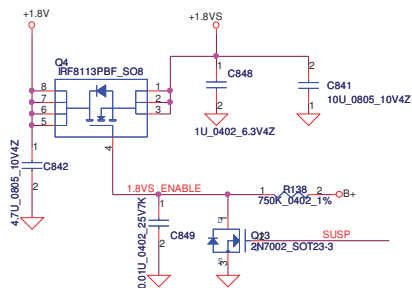
### +5VALW TO +5VS



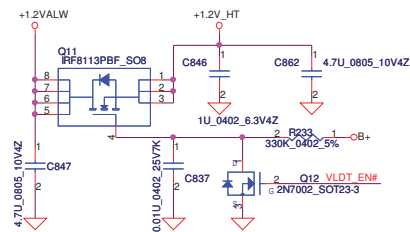
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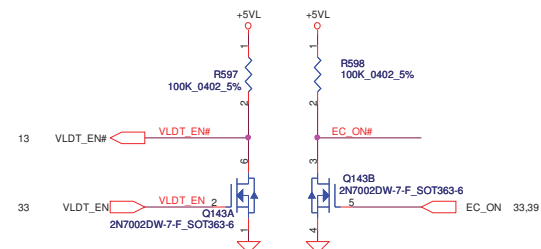
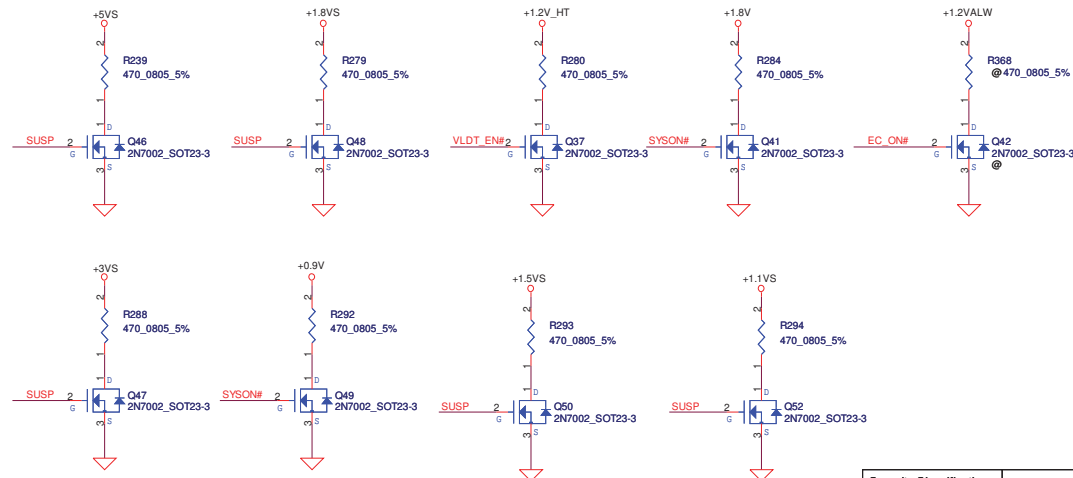
### +1.8V TO +1.8VS



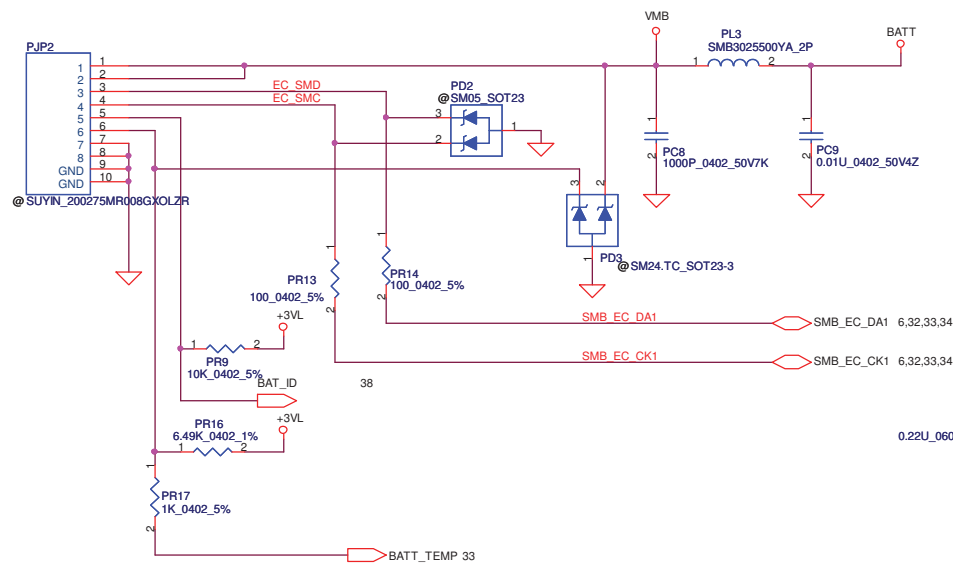
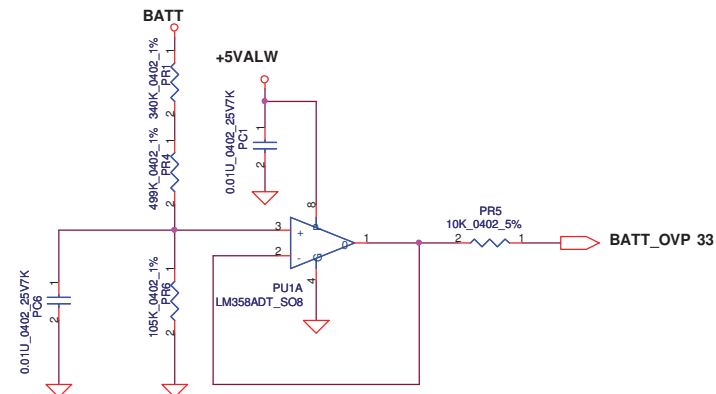
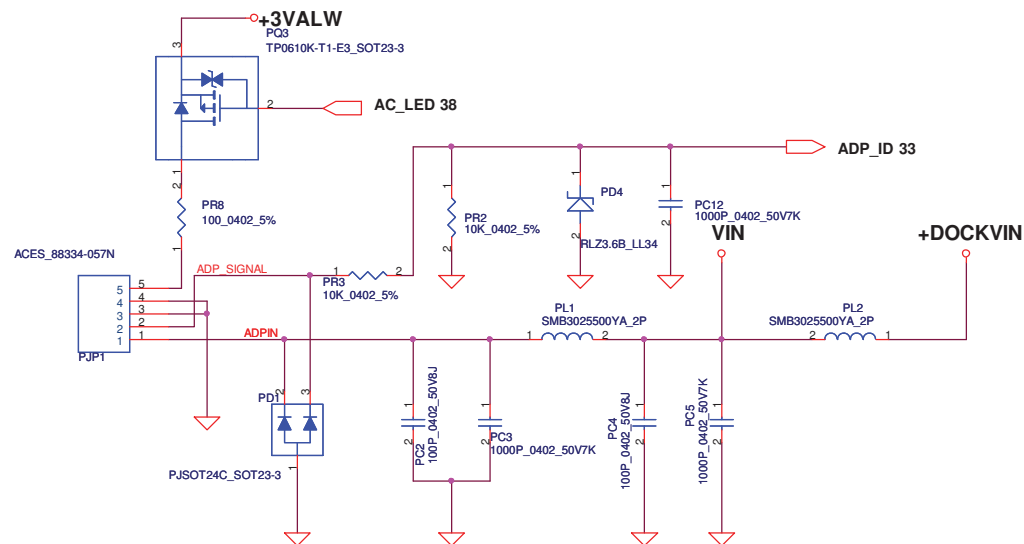
### +1.2VALW TO +1.2V\_HT



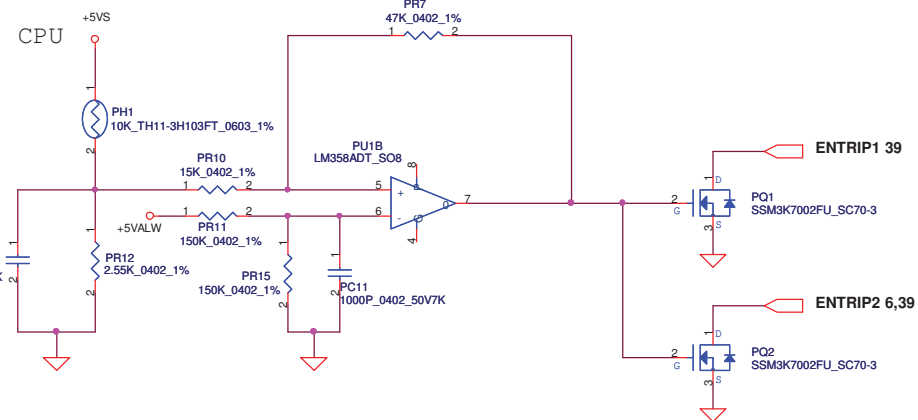
## Discharge circuit



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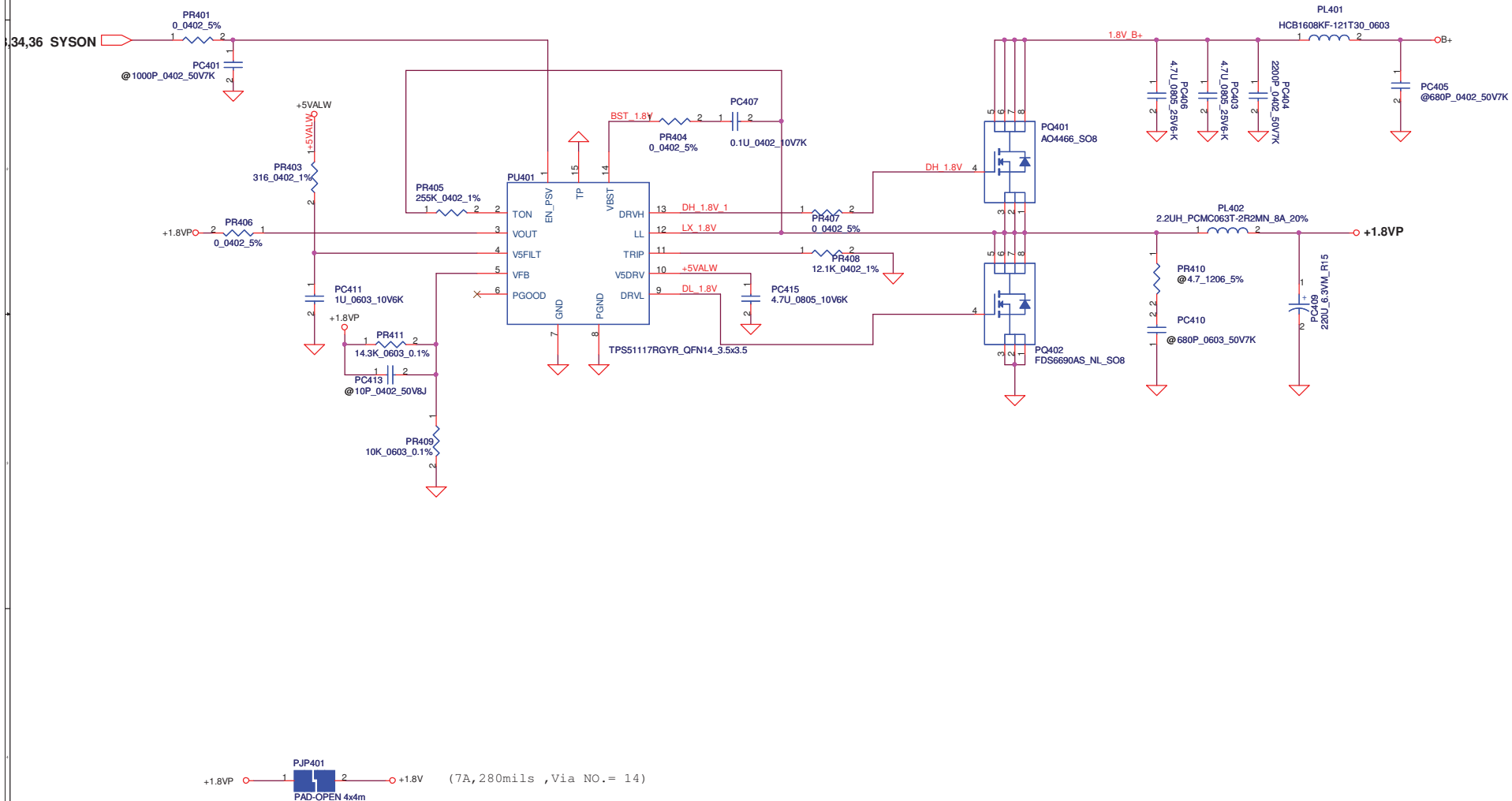
PH1 under CPU bottom side :  
CPU thermal protection at 90 +-3 degree C  
Recovery at 47 +-3 degree C



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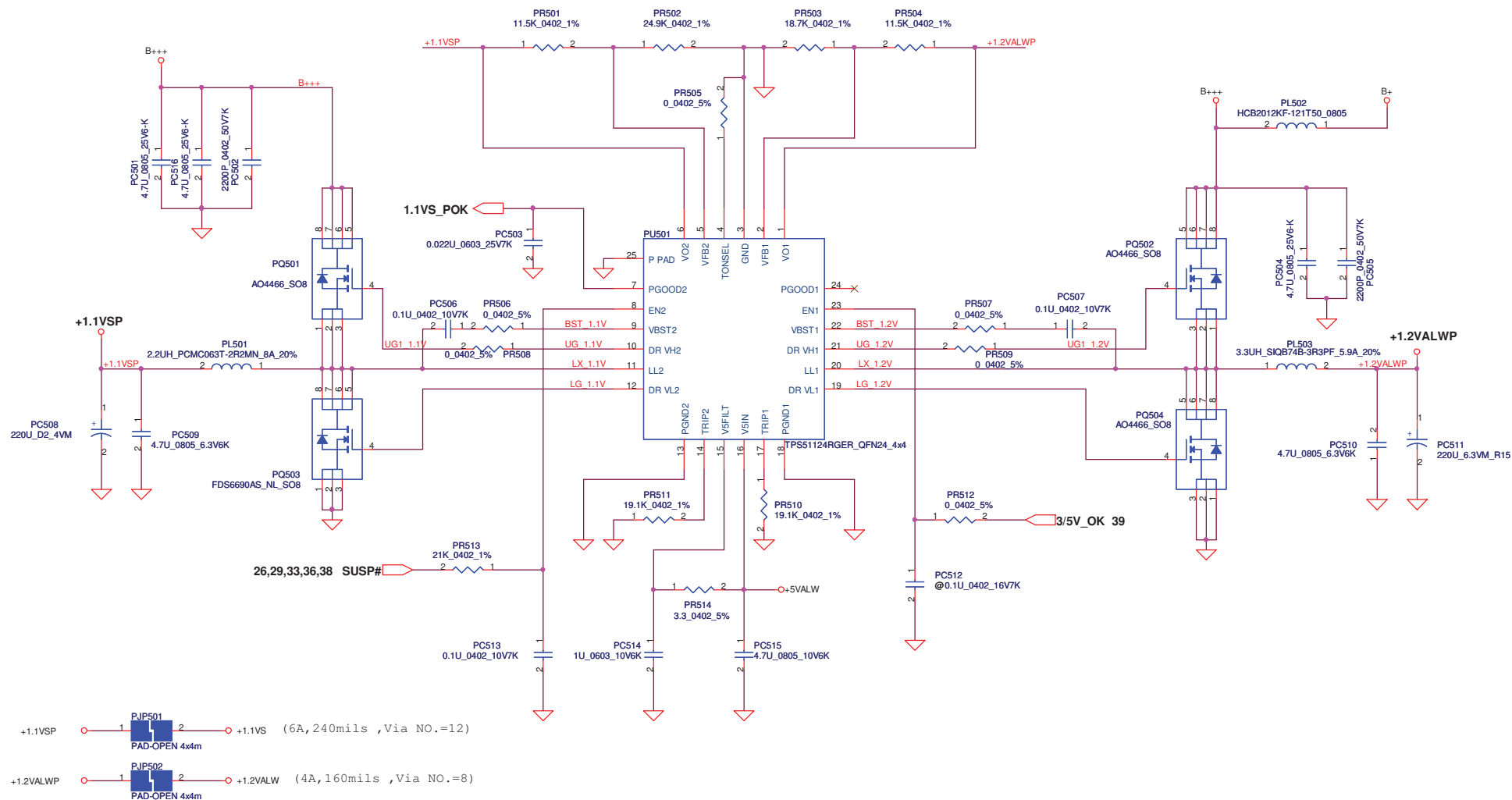




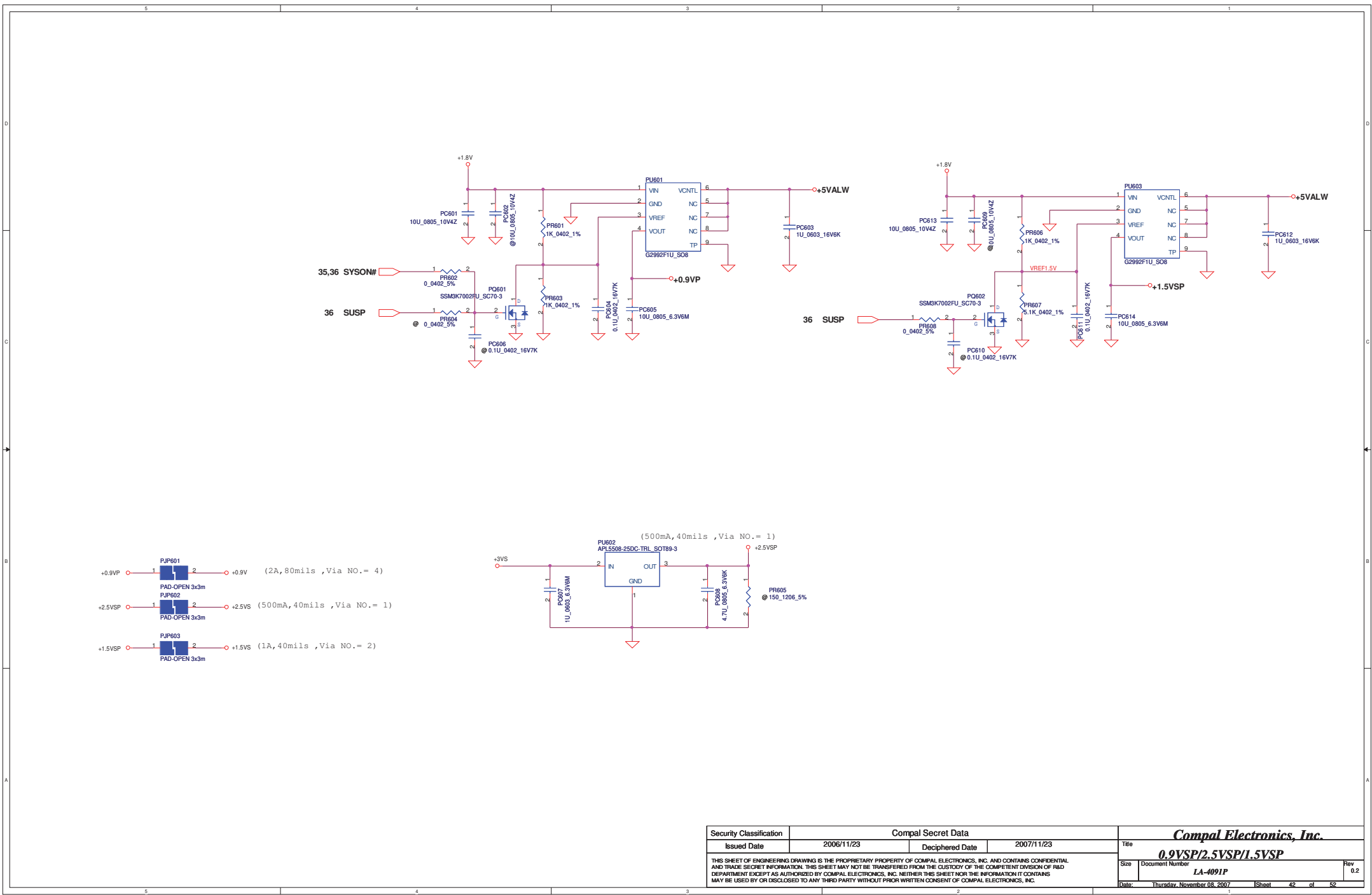


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								<b>1.1VSP/1.2VALWP</b>					
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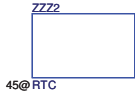


# Version Change List ( P. I. R. List )for Power Circuit

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	40	1.8VP	10/23	Compal	for power request	PU401 change the IC from "S IC RT8204PQW WQFN 16P" to "S IC TPS51117RGYR QFN 14P".	
2	38	Charger	10/30	Compal	for power request	PQ104 swap the PQ104 1,3 Pin	
3	39	3V/5V	10/30	Compal	for power request	Change PR301 to 13.7K modify output voltage	
4	39	3V/5V	10/30	Compal	for power request	Change PR305 to 180K modify OCP	
5	39	3V/5V	10/30	Compal	for power request	Change PR306 to 150K modify OCP	
6	39	3V/5V	10/30	Compal	for power request	Change PR311 to 620K	
7	39	3V/5V	10/30	Compal	for power request	Change PR315 to 604K modify sequence	
8	41	+1.1VSP	10/30	Compal	for power request	Change PR510 to 19.1K modify OCP	
9	41	+1.2VALWP	10/30	Compal	for power request	Change PR511 to 19.1K modify OCP	
10	38	Charger	10/30	Compal	for power request	Del PR119	
11	43	CPU_CORE	10/30	Compal	for power request	Change PC202 to B2 type for ME limit	
12	43	CPU_CORE	10/30	Compal	for power request	Change PR223 to 17.8K and PR224 to 100K modify OCP	
13	43	CPU_CORE	10/30	Compal	for power request	Change PR221,PR231 to 16.5K and PR217,PR233 to 4.02K for CPU_CORE compensation	
14	37	DC connector	10/30	Compal	for power request	Add PR3,PD4,PC12 for ADP_ID function	
15	39	3V/5V	10/30	Compal	for power request	Add PR317,PR318	
16	38	Charger	10/30	Compal	for power request	Change net from +3VLP to +3VL	
17	41	+1.1VSP	10/30	Compal	for power request	Change PR513 to 21K for HW power scquence.	

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# HW4 Product Improvement Record (P.I.R.)



RTC



PCB

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