AT3U BLOCK DIAGRAM

01

04-- 0402 footprint
06-- 0603 footprint
08-- 0805 footprint
12-- 1206 footprint
F-- 1% tolerance

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

CPU Merom
478P (uPGA)/35W
PAG 3,4

CPU THERMAL SENSOR
PAG 11

14.318MHz

CLOCK GEN
ICS9LPRS355AGLFT
64pinsTSSOP
PAG 2

CLK_CPU_BCLK, CLK_CPU_BCLK#
CLK_MCH_BCLK, CLK_MCH_BCLK#
DREFCLK, DREFCLK#
DREFSSCLK, DREFSSCLK#

NORTH BRIDGE
Crestline
PAG 5,6,7,8,9,10,11

DDRII-SODIMM1
PAG 12,13
DDRII 533,667 MHz

DDRII-SODIMM2
PAG 12,13
DDRII 533,667 MHz

TV_OUT
CRT_OUT
LVDS(2 Channel)

CRT/S-VIDEO
PAG 18

Panel Connector
PAG 19

Cable Docking
PAG 31
- TV_OUT
- VGA
- RJ-45
- CIR/Pwr btn
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

NBSRCCLK, NBSRCCLK#

DMI LINK

SOUTH BRIDGE
ICH-8M
PAG 14,15,16,17

USB2.0
5 | 0 | 3 | 4,6,7

Bluetooth PAG 27

USB2.0 I/O Ports X1 PAG 24

Camera X1 PAG 24

Mini PCI-E Card x1
Express Card x1
Cable Docking x1 PAG 31

PCI BUS / 33MHz
PCI-E
Azalia

SATA - HDD1 PAG 24 — *SATA2*
SATA - HDD2 PAG 27 — *SATA0*
PATA- CD-ROM PAG 24 — *PATA (66/100/133)*

LPC

Mini PCI-E Card
PCI Express Mini Card (Wireless LAN)
PAG 30

LAN
Realtek PCIE-LAN RTL8101 (10/100)
PAG 25,26

Express Card 34
(NEW CARD)
PAG 27

RICOH
RICOH 832
PAG 20,21

Realtek
ALC 268
PAG 22

Two-element microphone PAG 28

Audio Jacks (Phone/ MIC) PAG 22

RJ45 PAG 25

IEEE1394 CONN PAG 21

Memory CardReader PAG 20

ENE KBC
KB3926QF A2
PAG 32

Keyboard Touch Pad PAG 28
CIR PAG 22
Capacitive Sense SW PAG 28

AUDIO Amplifier PAG 23

Jack to Speaker PAG 28

FAN PAG 31

SPI PAG 32

SYSTEM CHARGER(MAX8724) PAG 33

SYSTEM POWER MAX8778 PAG 34

VCCP +1.5V AND GMCH 1.05V(MAX8717) PAG 35

CPU CORE MAX8771 PAG 36

DDR II SMDDR_VTERM 1.8V/1.8VSUS(TPS51116REGR) PAG 37

DISCHARGE/3VS/5VS/LANVCC PAG 38

PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD25	INTE#,INTF#	RICOH832
REQ1# / GNT1#	AD22	INTC#,INTD#	MINI PCI for debug

PROJECT : AT3U
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	2A

NB5/RD1/HW2

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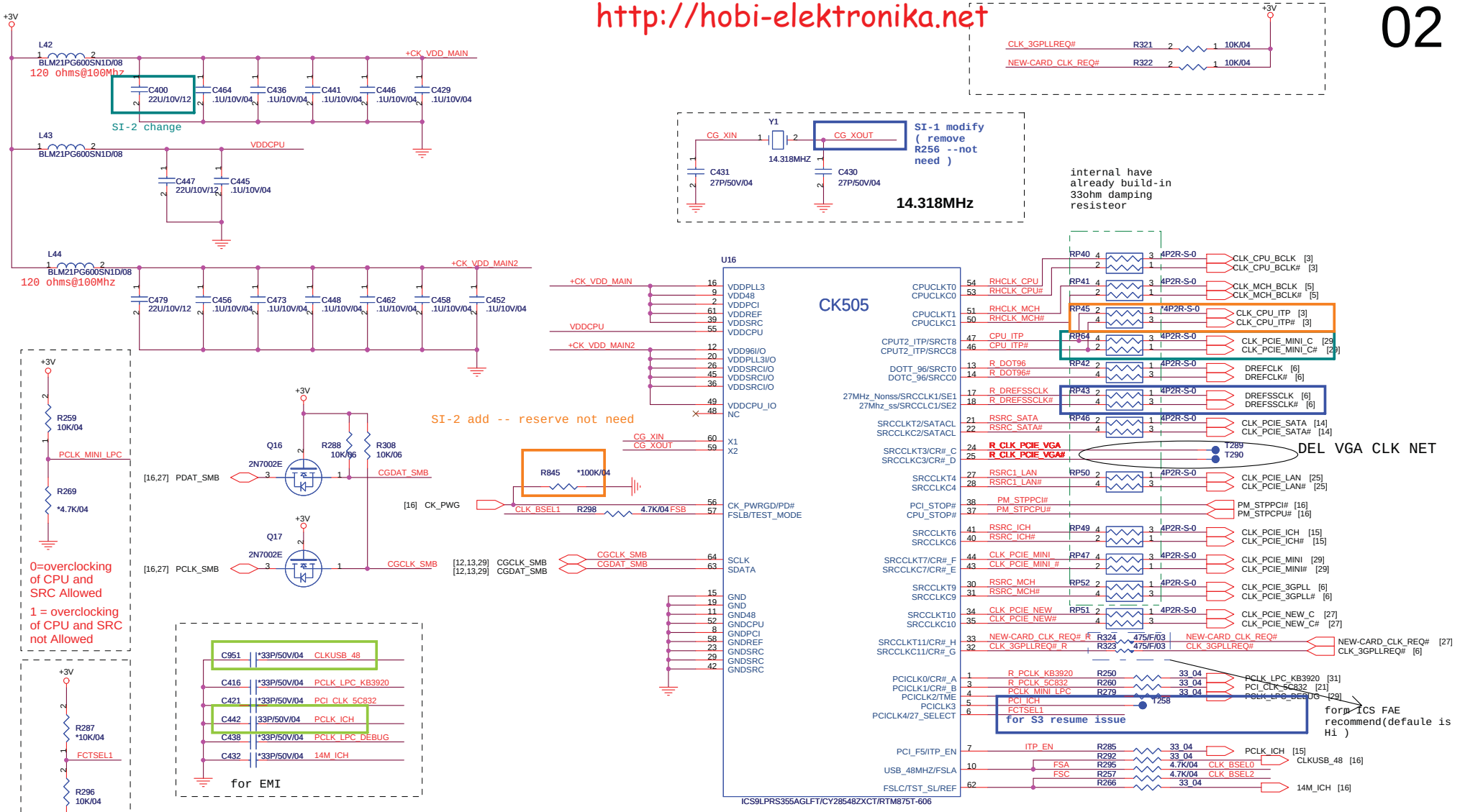

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

GCLK_SEL = FCTSEL1

FCTSEL1 (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

NB5/RD1/HW2

PROJECT : AT3U
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLOCK GENERATOR	2A

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for power noise

Layout Note: Place voltage divider within 0.5" of GTLREF pin

modified --remove R72

SI-2 modified for fix run TAT hang

Note: H_DPRSTP need to daisy chain from ICH8 to IMVP6 to CPU.

Reserved for EMI.

For the purpose of testability, route these signals through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

Place C close to the CPU_TEST4 pin. Make sure CPU_TEST4 routing is reference to GND and away from other noisy signal.

Comp0,2 connect with Zo=27.4ohm,Comp1,3 connect with Zo=55ohm, make those traces length shorter than 0.5".Trace should be at least 25 mils away from any other toggling signal.

Populate ITP700Flex for bringup

ITP debug signals

Layout Note: Place R8 close ITP.

Layout Note: Place R4,R361,R346 & R7 close to CPU.

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

ITP disable guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 1%	VTT	Within 2.0" of the ITP
TRST#	500-680ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 1%	GND	Within 2.0" of the ITP
TDO	150 ohm +/- 5%	VTT	Within 2.0" of the ITP

Note: Populate R5, R8, C372 & R430 when ITP connector is populated.

PROJECT : AT3U
Quanta Computer Inc.

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Custom	CLOCK GENERATOR	2A
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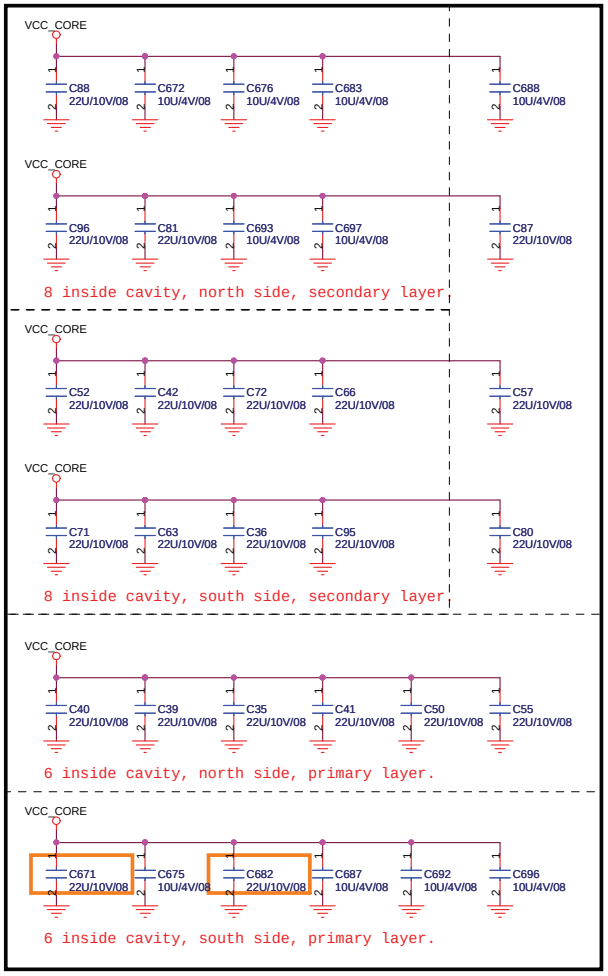
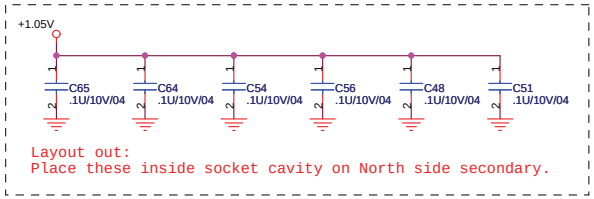
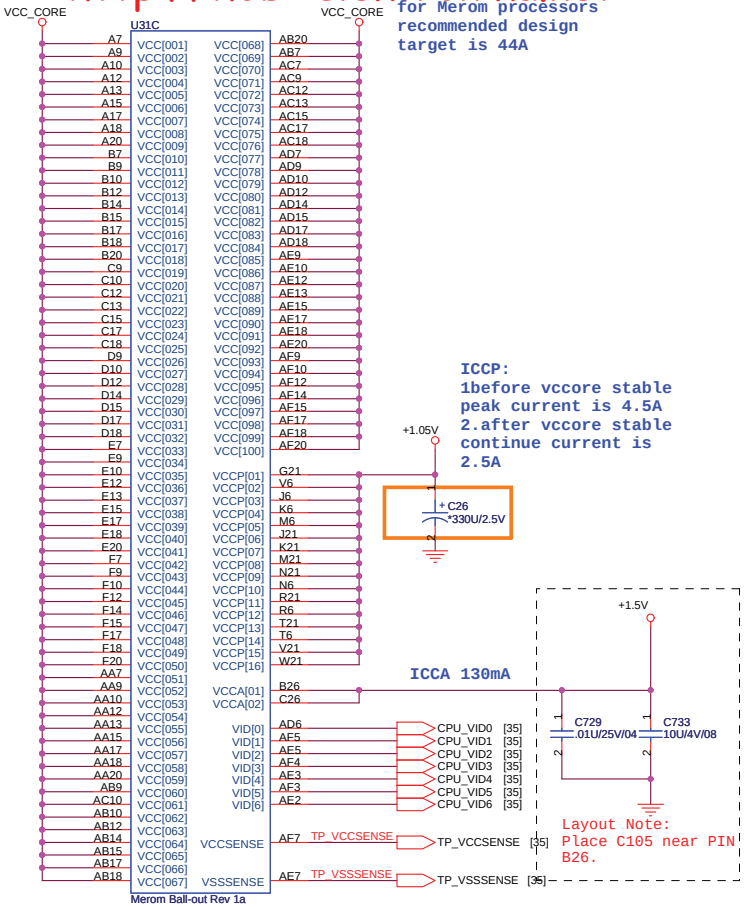
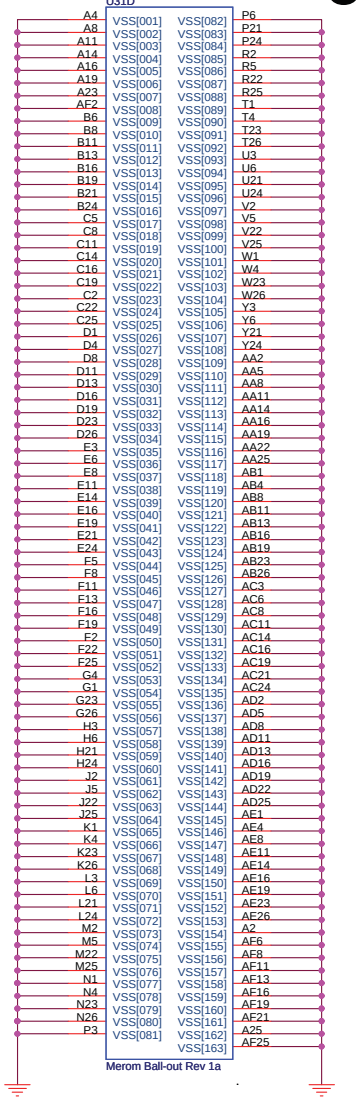
NB5/RD1/HW2









PROJECT : AT3U
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Merom Processor (POWER)	2A

NB5/RD1/HW2

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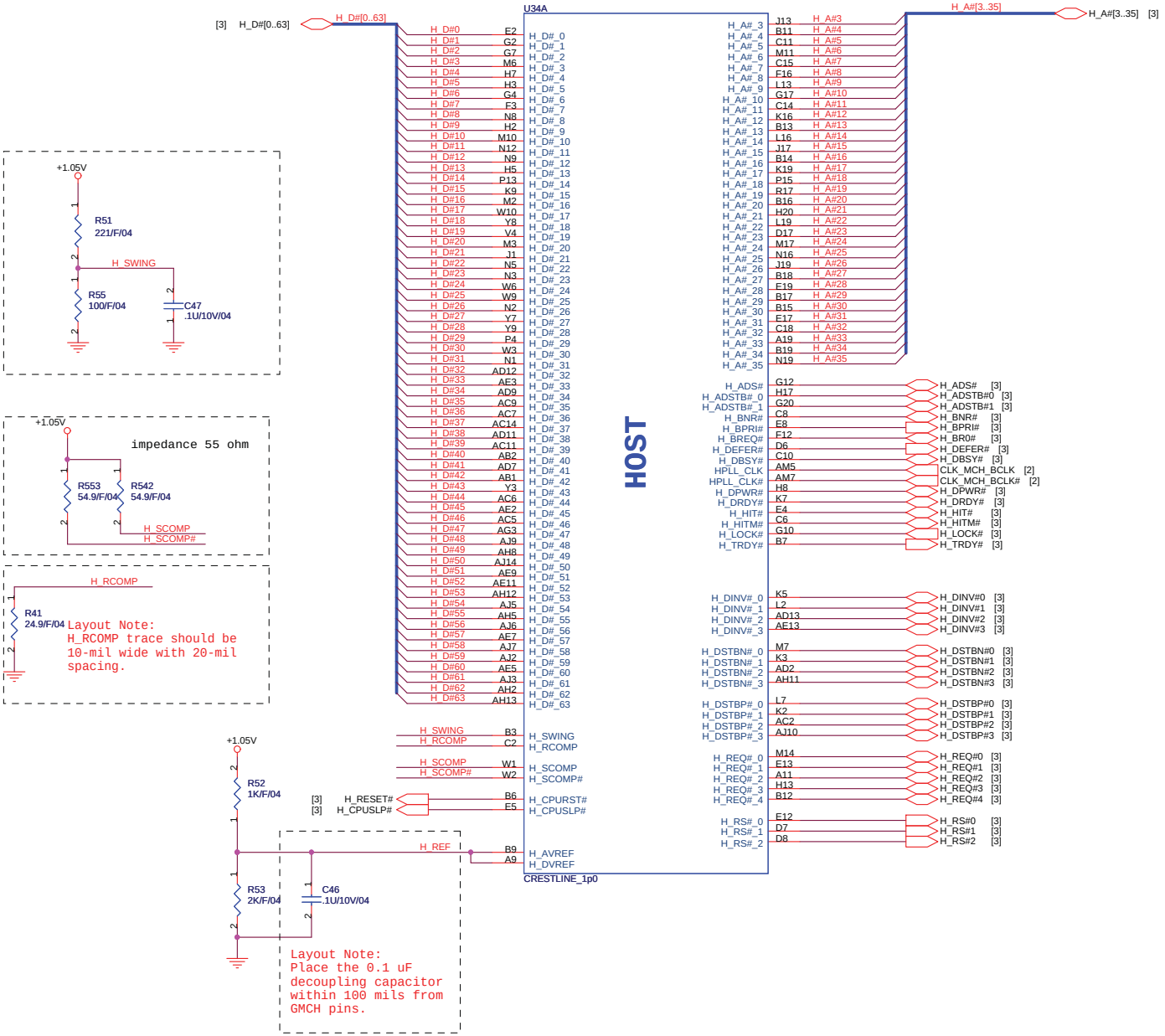

PROJECT : AT3U	
Quanta Computer Inc.	
Size: Custom	Document Number: Crestline (HOST)
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NB5/RD1/HW2	
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06

U34B

U34C

WW22 update --- MA14 needs to be routed if customers are planning on using 2Gb technology and width=8 (by 8) DIMMs

CRESTLINE new pin define

Layout Note:
Location of all MCH_CFG strap resistors needs to be close to minmize stub.

GMCH pwrok is 3.3v tolerant

<check list & CRB>
For Calero : 1.5K
For Cresstline:2.4K

modified add 470P

Dis/Enable setting

<FAE>
If no use can be NC

<check lisr & CRB>
For Calero : 255
For Cresstline:1.3K/F
For external VGA:0 ohm

<FAE> Flexible and safe

IV&EV Dis/Enable setting

<check list>
HSYNC/VSYNC serial R place close to NB

In Crestline EDS Rev.1.0, Render Standby Voltage is not finalized yet(TBD), 1.05V for Graphic Voltage range(VCC_AXG) is between 0.9975V(min.) and 1.1025V(max.). Vgfx max at 1.1025V @ 8A (estimated)

<FAE>
If no use DREFCLK PU and DREFCLK# PD

IV&EV Dis/Enable setting

only resever AT3/5 not support IAMT,but design line suggest to connection these pin ,do not NC

<design guide>
If no use
DREFCLK PU and
DREFCLK# PD

CLKREQ# (MCH drives CLK_REQ# to control the PCI-E diff clk input itself)

<check list>
For EV@
Connect to GND
CRT R/G/B
TV A/B/C
HSYNC/VSYNC

<check list>
For IV@
Connect to 150ohm
CRT R/G/B
TV A/B/C
Connect to 39ohm
HSYNC/VSYNC

SI-2 change

close to chip

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Quanta Computer Inc.	
Size: Custom	Document Number: Crestline (VGA,DMI)
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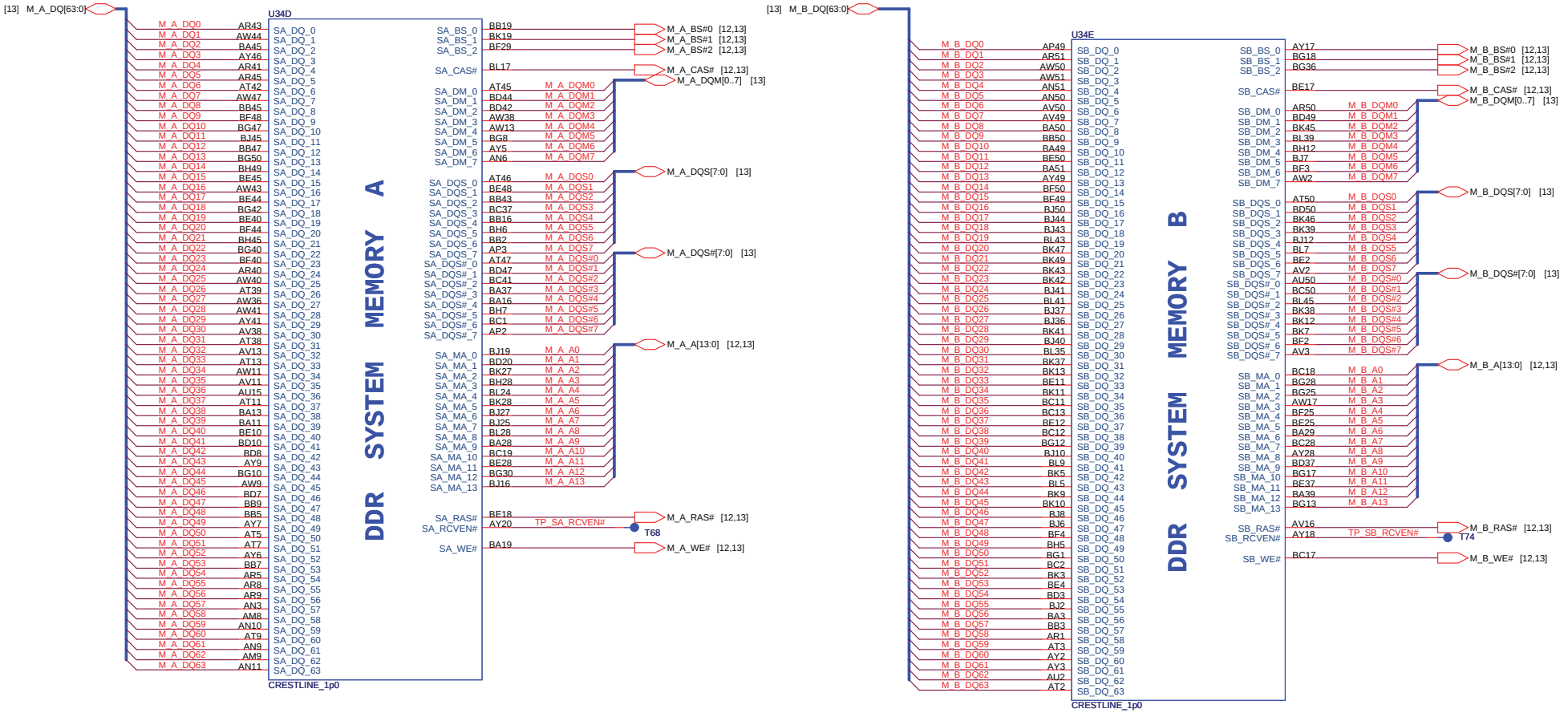
N85/RD1/HW2



NB5/RD1/HW2	PROJECT : AT3U Quanta Computer Inc.	
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POWER

U34G — CRESTLINE_1p0

VCC CORE: VCC_1 VCC_2 VCC_3 VCC_5 VCC_4 VCC_6 VCC_7 VCC_8 VCC_9 VCC_10 VCC_11 VCC_12 VCC_13

VCC SM: VCC_SM_1 VCC_SM_2 VCC_SM_3 VCC_SM_4 VCC_SM_5 VCC_SM_6 VCC_SM_7 VCC_SM_8 VCC_SM_9 VCC_SM_10 VCC_SM_11 VCC_SM_12 VCC_SM_13 VCC_SM_14 VCC_SM_15 VCC_SM_16 VCC_SM_17 VCC_SM_18 VCC_SM_19 VCC_SM_20 VCC_SM_21 VCC_SM_22 VCC_SM_23 VCC_SM_24 VCC_SM_25 VCC_SM_26 VCC_SM_27 VCC_SM_28 VCC_SM_29 VCC_SM_30 VCC_SM_31 VCC_SM_32 VCC_SM_33 VCC_SM_34 VCC_SM_35 VCC_SM_36

VCC GFX NCTF: VCC_AXG_NCTF_1 … VCC_AXG_NCTF_83

VCC GFX: VCC_AXG_1 … VCC_AXG_34

VCC SM LF: VCC_SM_LF1 … VCC_SM_LF7

IVCCSM supply current 1 channel 1.615A 2 channel 3.318A

+1.8VSUS_GMCH

+VCC_AXG +1.05V

Ivcc (External GFX 1.310 A, integrate 1.572 A)

+1.05V

C670 220U/2.5V

C663 22U/4V/08

C115 0.22U/10V/06

C90 0.22U/10V/06

C106 .1U/10V/04

Layout Note: 370 mils from edge.

Layout Note: Inside GMCH cavity.

Ivcc_AXG Graphics core supply current 7.7A

+VCC_AXG +1.05V

C91 *330U/6.3V

C108 *330U/6.3V

SI-2 modified --remove ~~C91&C108~~

Layout Note: 370 mils from edge.

Layout Note: Inside GMCH cavity for VCC_AXG.

C118 .1U/10V/04

C110 .1U/10V/04

C116 0.47U/10V/06

C79 1U/10V/06

C68 10U/6.3V/08

C73 22U/4V/08

GMCH 1.05V	current(A)	Remark
VCC Core	1.573	(1.3A for external GFX)
VCC_AXG	7.7	for integrated Gfx
VCC_AXD	0.2	
VTT	0.85	FSB VCCP
VCC_PEG	1.2	for PCIEG
VCC_AXM	0.54	for IAMT function
VCCR_RX_DMI	0.25	DMI
SUM	**12.313**	

for IAMT power if not support need to connection to S0 power

Ivcc_AXM Controller supply current 540mA

+1.05V

C105 .1U/10V/04

C94 .1U/10V/04

C113 .1U/10V/04

Layout Note: Inside GMCH cavity.

C124 22U/4V/08

C123 0.22U/10V/06

C99 0.22U/10V/06

Layout Note: Place close to GMCH edge.

U34F — CRESTLINE_1p0

VCC NCTF: VCC_NCTF_1 … VCC_NCTF_50

VSS NCTF: VSS_NCTF_1 … VSS_NCTF_21

VSS SCB: VSS_SCB1 … VSS_SCB6

VCC AXM NCTF: VCC_AXM_NCTF_1 … VCC_AXM_NCTF_19

VCC AXM: VCC_AXM_1 … VCC_AXM_7

+1.05V

1.8VSUS

C267 .1U/10V/04

C744 330U/6.3V

+1.8VSUS_GMCH

C265 22U/4V/08

C266 22U/4V/08

Layout Note: Place C901 where LVDS and DDR2 taps.

Layout Note: Place on the edge.

R500 10_04 +VCC_GMCH_L D32 CH751H-40PT +3V

CRT/TV Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT_DAC	3.3V	GND	VCCA_TVC_DAC	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TVDAC	1.5V	1.5V
VCCD_QDAC	1.5V	GND	VCCA_DAC_BG	3.3V	GND
VCCA_TVA_DAC	3.3V	GND	VSS_DAC_BG	GND	GND
VCCA_TVB_DAC	3.3V	GND	VCCSYNC	3.3V	GND

LVDS Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Signal	If SDVO Disable LVDS Disable	If LVDS enable
VCCD_LVDS	GND	1.8V
VCCA_LVDS	GND	1.8V
VCC_TX_LVDS	GND	1.8V

9

IV&EV Dis/Enable setting

<FAE>
INT VGA disable
VCCSYNC connect
to GND

FB_180ohm+-25%
_100mHz_1500mA
_0.09ohm DC

FB_120ohm+-25%_100mHz
_200mA_0.2ohm DC

10uH+-20%_100mA

0.1Caps should be placed 200 mils with in its pins.

SI-1 modify
(NET name
wrong)

POWER

Ivcc_VTT FSB supply current 0.85A

Place on the edge.

Reserved L81 pad for inductor.

Place caps close to VCC_AXD.

Ivcc_DMI supply current 100mA

Place caps close to VCC_AXF

Ivcca_PEG_BG supply current 100mA

Ivcc_PEG supply current 1.2A

SI-1 modified change

Ivcc_RX_DMI supply current 250mA

1uH+-20%_300mA

FB_220ohm+-25%_100MHz
_2A_0.1ohm DC

22nF & 0.1uF for VCC_TVDACA:C_R should be placed with in 250 mils from Crestline.

+3V_VCC_HV

40 mil wide

CRESTLINE_1p0

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Quanta Computer Inc.	
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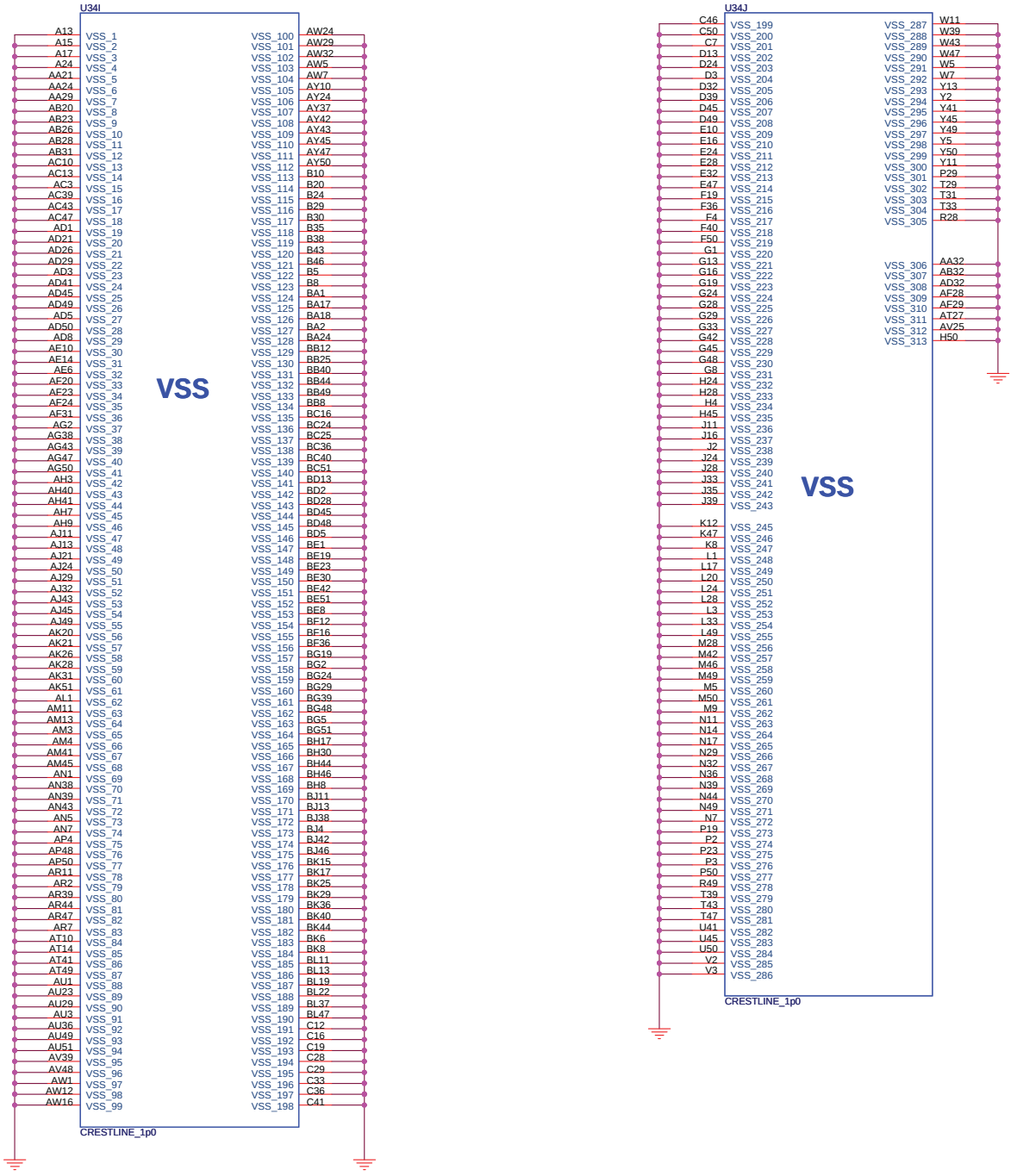
N85/RD1/HW2	



PROJECT : AT3U	
Quanta Computer Inc.	
NB5/RD1/HW2	
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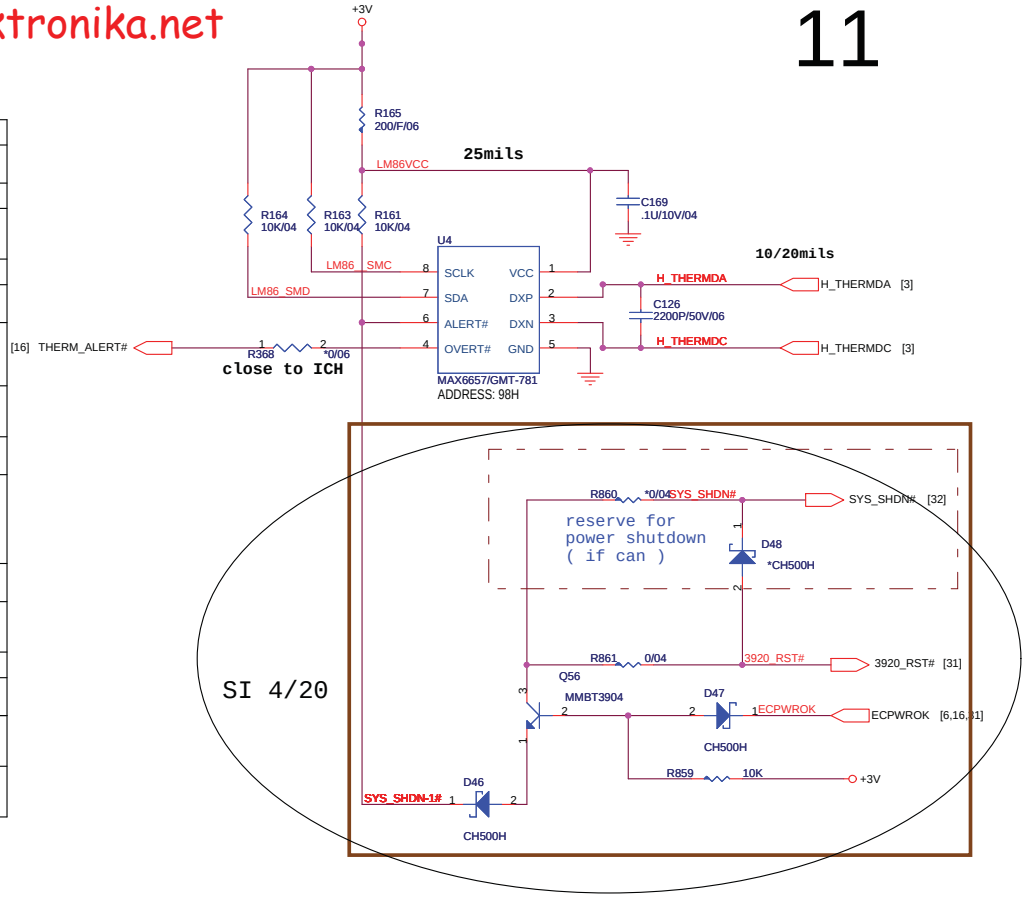
Strap table

All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) signal

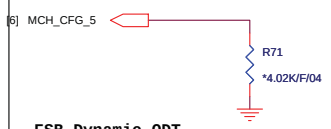
CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port



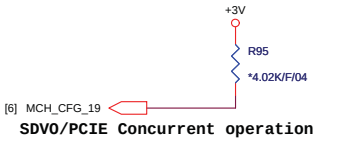
DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIX4(Default)



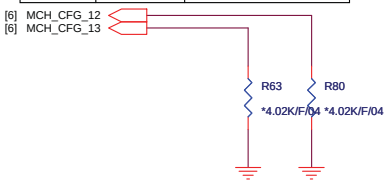
DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane



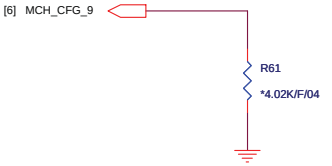
XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)



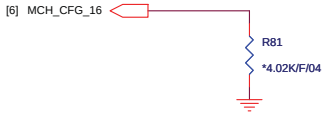
PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)



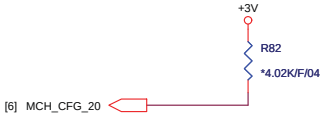
FSB Dynamic ODT

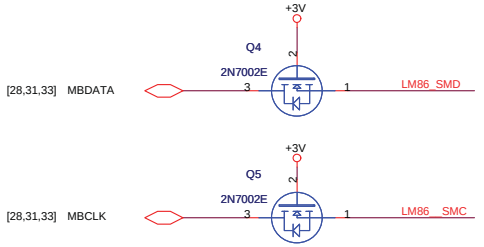
MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)



SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO andPCIE X1 are operating simultaneously via the PEG port





SDVO Present

Strap define at External DVI control page

NB5/RD1/HW2	PROJECT : AT3U Quanta Computer Inc.	
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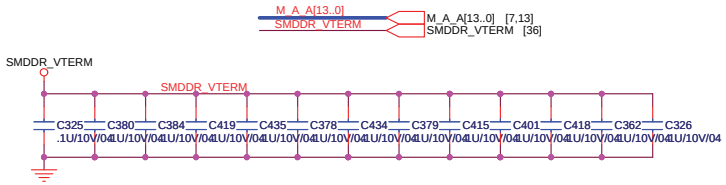
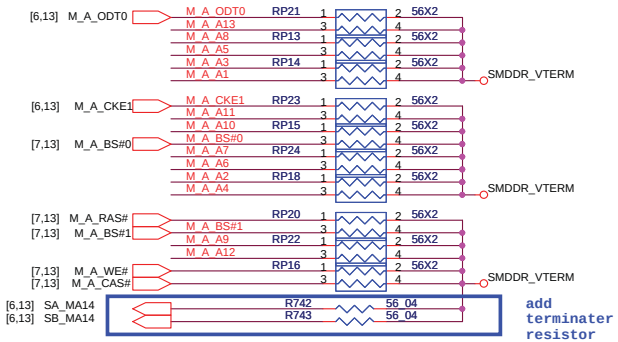
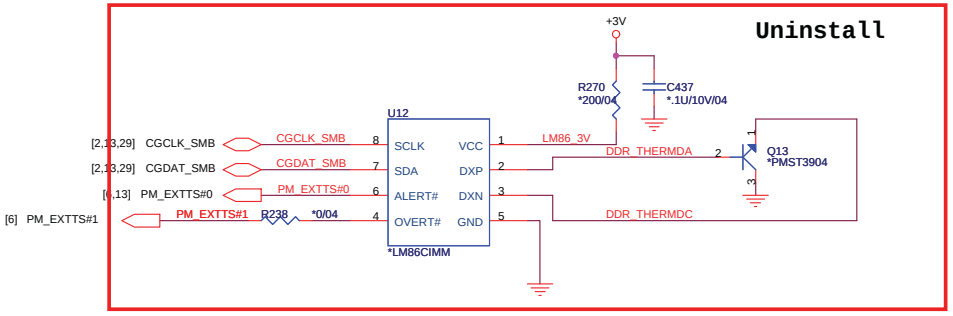
DDRII DUAL CHANNEL A,B.

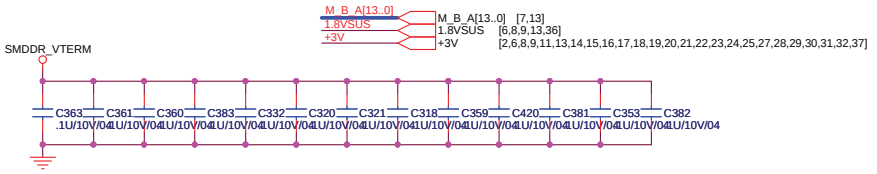
DDRII A CHANNEL



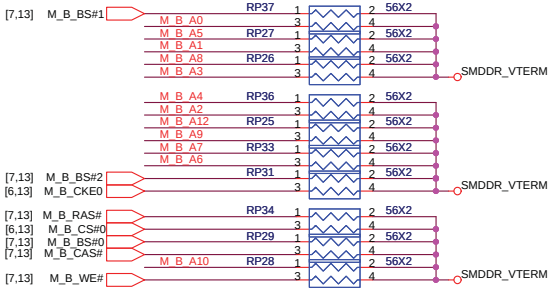


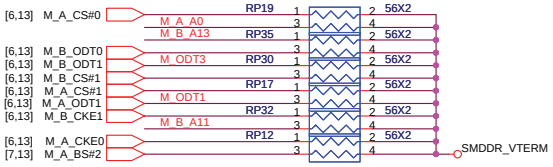


DDRII B CHANNEL



Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM





PROJECT : AT3U Quanta Computer Inc.		
NB5/RD1/HW2	Size: Custom Document Number: DDRII RES.ARRAY	Rev: 2A
	Date: Wednesday, May 02, 2007	Sheet 12 of 37

CGCLK_SMB
CGDAT_SMB
M_A_CKE[0..1]
M_A_CS#[0..1]
M_A_RAS#
M_A_CAS#
M_A_WE#
M_A_CLK0
M_A_CLK0#
M_A_CLK1
M_A_CLK1#
M_A_BS#[0..2]
M_A_ODT[0..1]
M_A_DQM[0..7]
M_A_DQ[0..63]
M_A_DQS[0..7]
M_A_DQS#[0..7]
M_A_A[13..0]
M_B_CKE[0..1]
M_B_CS#[0..1]
M_B_RAS#
M_B_CAS#
M_B_WE#
M_B_CLK0
M_B_CLK0#
M_B_CLK1
M_B_CLK1#
M_B_BS#[0..2]
M_B_ODT[0..1]
M_B_DQM[0..7]
M_B_DQ[0..63]
M_B_DQS[0..7]
M_B_DQS#[0..7]
M_B_A[13..0]
+3V
1.8VSUS

CKEA 0,1

H 9.2

FOX=AS0A426-M2S-TR
CN26A

PC2100 DDR2 SDRAM SO-DIMM (200P)

CKEB 0,1

H 5.2

FOX=AS0A426-MAS-TR
CN24A

PC2100 DDR2 SDRAM SO-DIMM (200P)

SMbus address A4

DIM2_SA0 R267 10K/04
DIM2_SA1 R268 10K/04

SMbus address A0

R216 10K/04 DIM1_SA0
R217 10K/04 DIM1_SA1

SMDDR_VREF_DIMM
SB_MA14
SA_MA14
PM_EXTTS#0
M_B_ODT0
M_B_ODT1
M_A_ODT0
M_A_ODT1

PC2100 DDR2 SDRAM SO-DIMM (200P)

FOX=AS0A426-M2S-TR
CN26B

FOX=AS0A426-MAS-TR
CN24B

C771 470P/50V/04
R226 0/06
R227
R603 *10K/F/06
*10K/F/06

SMDDR_VREF [6,36]

Place these Caps near So-Dimm1.

C773 2.2U/6.3V/06
C775 2.2U/6.3V/06
C785 2.2U/6.3V/06
C444 .1U/10V/04
C764 2.2U/6.3V/06
C770 .1U/10V/04
C788 .1U/10V/04
C439 .1U/10V/04
C433 .1U/10V/04
C769 .1U/10V/04
C767 .1U/10V/04

SMDDR_VREF_DIMM
C772 .1U/10V/04
C768 2.2U/6.3V/06
+3V
C317 2.2U/6.3V/06
C316 .1U/10V/04

SO-DIMM BYPASS PLACEMENT :

Place these Caps near So-Dimm1.

No Vias Between the Trace of PIN to CAP.

Place these Caps near So-Dimm2.

C774 2.2U/6.3V/06
C786 2.2U/6.3V/06
C784 2.2U/6.3V/06
C759 .1U/10V/04
C760 .1U/10V/04
C776 .1U/10V/04
C789 .1U/10V/04
C787 .1U/10V/04
C443 .1U/10V/04
C765 .1U/10V/04
C766 .1U/10V/04

SMDDR_VREF_DIMM
C371 .1U/10V/04
C373 2.2U/6.3V/06
+3V
C372 2.2U/6.3V/06
C385 .1U/10V/04

SO-DIMM BYPASS PLACEMENT :

Place these Caps near So-Dimm2

No Vias Between the Trace of PIN to CAP.

NB5/RD1/HW2

PROJECT : AT3U
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDRII SO-DIMM(200P)	2A

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RTC

Place near to Mini-door

CKL:C1/C2: 18pF -> CL:12.5pF
C1/C: 10pF -> CL Value = 8.5pF

VCCRTC
3VPCU
C804 1U/16V/06
D41 SDM10K45
D42 SDM10K45
R638 20K/06
VCCRTC_2
R635 1K/06
R637 1M/F/06
C811 1U/16V/06
G2 *SHORT_PAD1
C820 15P/50V/04
C817 15P/50V/04
Y6 32.768KHZ
R663 10M/06
CLK_32KX1
CLK_32KX2
RTCRST#
SM_INTRUDER#
ICH_INTVRMEN
LAN100_SLP
CN30 CWY020-B0G1Z
change to battery conn

5VPCU
20MIL 20MIL
R625 *1.2K/06 VCCRTC_1
R628 *1K/06 VCCRTC_3
Q42 *MMBT3904
R626 *4.7K/06
R629 *15K/06
add RTC Bat rechargeable circuit

U42A

RTCX1 AG25
RTCX2 AF24
RTCRST# AF23
INTRUDER# AD22
INTVRMEN AF25
LAN100_SLP AD21

RTC / LPC

LAN_JCLK T234 B24 GLAN_CLK
LAN_RSTSYNC T102 D22 LAN_RSTSYNC
LAN_RXD0 T104 C21 LAN_RXD0
LAN_RXD1 T233 B21 LAN_RXD1
LAN_RXD2 T226 C22 LAN_RXD2
LAN_TXD0 T105 D21 LAN_TXD0
LAN_TXD1 T112 E20 LAN_TXD1
LAN_TXD2 T99 C20 LAN_TXD2
+1.5V_PCIE R334 24.9/F/04 GLAN_COMP_SB
AH21 GLAN_DOCK#/GPIO13
D25 GLAN_COMPI
C25 GLAN_COMPO

LAN / GLAN

ACZ_BCLK AJ16 HDA_BIT_CLK
ACZ_SYNC AJ15 HDA_SYNC
ACZ_RST# AE14 HDA_RST#
[22] ACZ_SDIN0 ACZ_SDIN0 AJ17 HDA_SDIN0
ACZ_SDIN1 AH17 HDA_SDIN1
ACZ_SDIN2 AH15 HDA_SDIN2
ACZ_SDIN3 AD13 HDA_SDIN3
ACZ_SDOUT AE13 HDA_SDOUT
[25] LAN_DISABLE# AE10 HDA_DOCK_EN#/GPIO33
AG14 HDA_DOCK_RST#/GPIO34
+3V R691 10K/06 T143
[28] SATA_LED# SATA_LED# AF10 SATALED#

CPU

FWH0/LAD0 E5 LAD0 [29,31]
FWH1/LAD1 F5 LAD1 [29,31]
FWH2/LAD2 G8 LAD2 [29,31]
FWH3/LAD3 F6 LAD3 [29,31]
FWH4/LFRAME# C4 LFRAME# [29,31]
LDRQ0# G9 LDRQ#0 T116
LDRQ1#/GPIO23 E6 LDRQ#1 T230
A20GATE AF13 GATEA20 [31]
A20M# AG26 H_A20M# [3]
DPRSTP# AF26 H_DPRSTP#_R
DPSLP# AE26 H_DPSLP#_R
FERR# AD24
CPUPWRGD/GPIO49 AG29 R432 0/06 H_PWRGD [3]
IGNNE# AF27 H_IGNNE# [3]
INIT# AE24 H_INIT# [3]
INTR AC20 H_INTR [3]
RCIN# AH14 RCIN# RCIN# [31]
NMI AD23 H_NMI [3]
SMI# AG28 H_SMI#_R R425 0/06 H_SMI# [3]
STPCLK# AA24 H_STPCLK# [3]
THRMTRIP# AE27 H_THERMTRIP_R
TP8 AA23 T127 PDD[15:0] [24]

IHDA

SATA0RXN AF6 SATA_RXN2_C
SATA0RXP AF5 SATA_RXP2_C
SATA0TXN AH5 SATA_TXN2_C
SATA0TXP AH6 SATA_TXP2_C
SATA1RXN AG3
SATA1RXP AG4
SATA1TXN AJ4
SATA1TXP AJ3
SATA2RXN AF2 SATA_RXN0_C
SATA2RXP AF1 SATA_RXP0_C
SATA2TXN AE4 SATA_TXN0_C
SATA2TXP AE3 SATA_TXP0_C
SATA_CLKN AB7 [2] CLK_PCIE_SATA#
SATA_CLKP AC6 [2] CLK_PCIE_SATA
SATARBIAS# AG1 R655 24.9/F/06 SATA_BIAS
SATARBIAS AG2

SATA

DD0 V1 PDD0
DD1 U2 PDD1
DD2 V3 PDD2
DD3 T1 PDD3
DD4 V4 PDD4
DD5 T5 PDD5
DD6 AB2 PDD6
DD7 T6 PDD7
DD8 T3 PDD8
DD9 R2 PDD9
DD10 T4 PDD10
DD11 V6 PDD11
DD12 V5 PDD12
DD13 U1 PDD13
DD14 V2 PDD14
DD15 U6 PDD15
DA0 AA4 PDA0
DA1 AA1 PDA1
DA2 AB3 PDA2
DCS1# Y6 PDCS1# [24]
DCS3# Y5 PDCS3# [24]
DIOR# W4 PDIOR# [24]
DIOW# W3 PDIOW# [24]
DDACK# Y2 PDDACK# [24]
IDEIRQ Y3 IRQ14 IRQ14 [24]
IORDY Y1 PDIORDY PDIORDY [24]
DDREQ W5 PDDREQ [24]

IDE

ICH8M REV 1.0

[24] SATA_RXN0 C597 3900P/25V/04 SATA_RXN0_C
[24] SATA_RXP0 C600 3900P/25V/04 SATA_RXP0_C
[24] SATA_TXN0 C606 3900P/25V/04 SATA_TXN0_C
[24] SATA_TXP0 C609 3900P/25V/04 SATA_TXP0_C
CKL:1n ~ 20nF

[27] SATA_RXN2 C576 3900P/25V/04 SATA_RXN2_C
[27] SATA_RXP2 C577 3900P/25V/04 SATA_RXP2_C
[27] SATA_TXN2 C587 3900P/25V/04 SATA_TXN2_C
[27] SATA_TXP2 C590 3900P/25V/04 SATA_TXP2_C
CKL:1n ~ 20nF

Place within 500 mils of ICH7
25mils/15mils

+3V R447 10K/06 R648 10K/06
RCIN# GATEA20
+1.05V R409 *56/F/06 R449 *56/F/06
+1.05V R442 56/F/06
R439 0/06 H_DPRSTP# [3,6,35] H_DPSLP# [3]
H_FERR# [3]
+1.05V R849 56_04
for fix ESD issue
R406 24.9/F/06 PM_THRMTRIP# [3,6]
Should be 2" close ICH7
C560 *SFI0603-050E101NP/06

ACZ_SDOUT R654 33_04 ACZ_SDOUT_AUDIO [22] C814 *10P/50V/04
ACZ_SYNC R649 33_04 ACZ_SYNC_AUDIO [22] C816 *10P/50V/04
ACZ_BCLK R653 33_04 BIT_CLK_AUDIO [22] C813 *10P/50V/04
ACZ_RST# R646 33_04 ACZ_RST#_AUDIO [22]
intel check list define to stuff 33ohm

SB Strap

ICH8-M Internal VR Enable strap (Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

VCCRTC
R443 332K/F/06
ICH_INTVRMEN
R417 *0

ICH8-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

VCCRTC
R444 332K/F/06
LAN100_SLP
R414 *0

XOR Chain Entrance Strap

ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

+3V
R644 *1K/06
ACZ_SDOUT
ICH_TP3 [16]
R428 *1K

NB5/RD1/HW2	PROJECT : AT3U Quanta Computer Inc.	
	Size: Custom Document Number: ICH7-M HOST(1/4)	Rev: 2A
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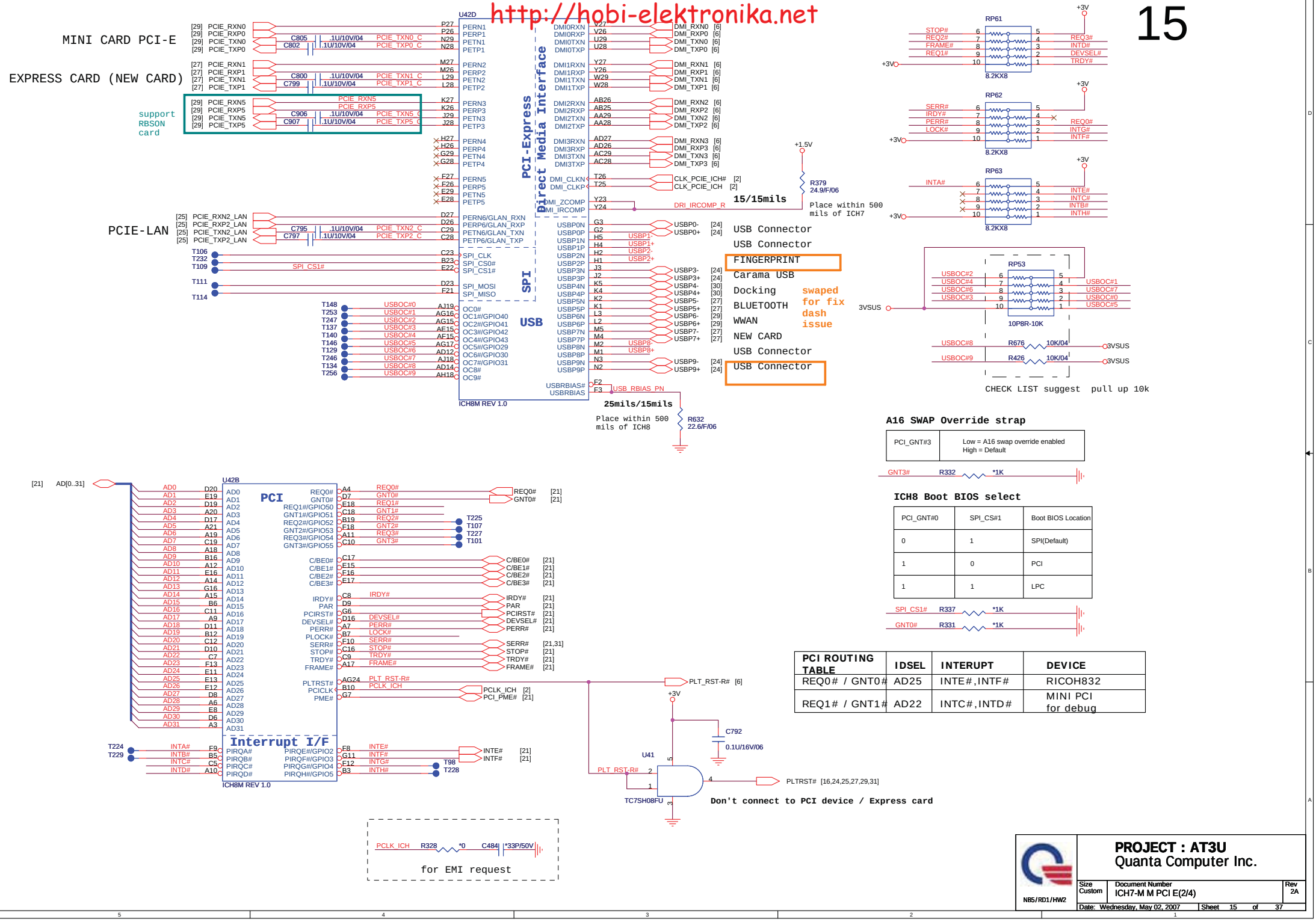

PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD25	INTE#,INTF#	RICOH832
REQ1# / GNT1#	AD22	INTC#,INTD#	MINI PCI for debug

PROJECT : AT3U
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH7-M M PCI E(2/4)	2A

NB5/RD1/HW2

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fix re-boot fail

R833 2K/F/04

[35] VR_PWRGD_CK410#

U26 NL17SZ14DFT2G

C608 1U/16V/04

VR_PWRGD_CK410

R809 100K/04

PCLK_SMB R617 2.2K/06
PDAT_SMB R272 2.2K/06
PCIE_WAKE# R399 1K/06
PM_BATLOW#_R R387 8.2K/06

SMB_LINK_ALERT# R621 10K/06
SMLINK0 R619 10K/06
SMLINK1 R618 10K/06

R624 8.2K/06
DNBSWON# R271 10K/06
SYS_RST#-1 R615 10K/06
SMB_ALERT# R273 10K/06

KBSMI#_R R281 10K/06

SWI#_R R280 10K/06

CLKRUN# R433 8.2K/06
SERIRQ R656 8.2K/06
SCI#_R R662 10K/06

PM_RSMRST#_R R658 10K/06

these pin if unused require 8.2k to 10k pull-up to +3v

SI-1 add

U42C ICH8M REV 1.0

SMB: SMBCLK, SMBDATA, LINKALERT#, SMLINK0, SMLINK1

SATA GPIO: SATA0GP/GPIO21, SATA1GP/GPIO19, SATA2GP/GPIO36, SATA3GP/GPIO37

Clocks: RI#, SUS_STAT#/LPCPD#, SYS_RESET#, SUSCLK

SYS GPIO: BMBUSY#/GPIO0, SMBALERT#/GPIO11, STP_PCI#/GPIO15, STP_CPU#/GPIO25, CLKRUN#/GPIO32, WAKE#, SERIRQ, THRM#, VRMPWRGD, TP7

Power MGT: SLP_S3#, SLP_S4#, SLP_S5#, S4_STATE#/GPIO26, PWROK, DPRSLPVR/GPIO16, BATLOW#, PWRBTN#, LAN_RST#, RSMRST#, CK_PWRGD, CLPWROK, SLP_M#

GPIO: TACH1/GPIO1, TACH2/GPIO6, TACH3/GPIO7, GPIO8, GPIO12, TACH0/GPIO17, GPIO18, GPIO20, SCLOCK/GPIO22, QRT_STATE0/GPIO27, QRT_STATE1/GPIO28, SATACLKREQ#/GPIO35, SLOAD/GPIO38, SDATAOUT0/GPIO39, SDATAOUT1/GPIO48, SPKR

Controller Link: CL_CLK0, CL_CLK1, CL_DATA0, CL_DATA1, CL_VREF0, CL_VREF1, CL_RST#

MISC: MCH_SYNC#, MEM_LED/GPIO24, ME_EC_ALERT/GPIO10, EC_ME_ALERT/GPIO14, WOL_EN/GPIO9

[2,27] PCLK_SMB R816 0/04
[2,27] PDAT_SMB R817 0/04
SMB_LINK_ALERT#
SMLINK0
SMLINK1
RI#
SYS_RST# R614 0/04 SYS_RST#-1
R682 0/04
SMB_ALERT#
PM_STPPCI_ICH# R402 0/06
PM_STPCPU_ICH# R436 0/06
CLKRUN#
PCIE_WAKE# [25,27,29]
SERIRQ [21,31]
VR_PWRGD_CK410
R364 8.2K/06
T245
T254
KBSMI# R405 0/04 KBSMI#_R
SCI# R386 0/04 SCI#_R
SWI# R611 0/04 SWI#_R
T128
T248
T252
LCD_BK [19]
BOARD_ID2
R687 0/04
R671 0/04
R420 0/04
WAN_OFF# [29]
RF_OFF# [29]
BTLED [28]
AMPBEEP_EN [23]
R768 10K/04
R769 10K/04
R770 10K/04
ACZ_SPKR [23]
R427 0/04
MCH_ICH_SYNC#_R
ICH_TP3 [14]
R435 *10K

3/22

R450 *10K/F/06
R315 *10K/F/06
SYS_RST# [2]
PM_BMBUSY# [6]
PM_STPPCI# [2]
PM_STPCPU# [2]
THERM_ALERT# [11]
MCH_ICH_SYNC# [6]

SATA0GP/GPIO21 AJ12 BOARD_ID1
SATA1GP/GPIO19 AJ10 BOARD_ID0
SATA2GP/GPIO36 AF11 BOARD_ID3
SATA3GP/GPIO37 AG11 BOARD_ID4

CLK14 AG9 14M_ICH [2]
CLK48 G5 CLKUSB_48 [2]
SUSCLK D3 T108

SLP_S3# AG23 R616 100/F/06 SUSB# [31]
SLP_S4# AF21 R326 100/F/06 SUSC# [31]
SLP_S5# AD18 T130

S4_STATE#/GPIO26 AH27 T249 R677 *100K/04

PWROK AE23 ICH_PWROK

DPRSLPVR/GPIO16 AJ14 DPRSLPVR-ICH R620 499/F DPRSLPVR → DPRSLPVR [6,35]

BATLOW# AE21 PM_BATLOW#_R R642 0/04 → PM_BATLOW# [31]
DNBSWON# → DNBSWON# [31]

PWRBTN# C2 C819 *1U/16V/04
R665 *100/F/06
LAN_RST# AH20 PLTRST_LAN# R666 100/F/06 → LAN_REST [25,31] PLTRST# [15,24,25,27,29,31]

RSMRST# AG27 PM_RSMRST#_R R659 100/F/06 RSMRST# → RSMRST# [31]

CK_PWRGD E1 R623 0/04 → CK_PWG [2]

CLPWROK E3 R622 0/04 → ECPWROK [6,11,31]

SLP_M# AJ25 SUSM# T251

CL_CLK0 F23 → CL_CLK0 [6]
CL_CLK1 AE18 → ICH_CL_CLK1 [29]

CL_DATA0 F22 → CL_DATA0 [6]
CL_DATA1 AF19 → ICH_CL_DATA1 [29]

CL_VREF0 D24 CL_VREF0_SB
CL_VREF1 AH23 CL_VREF1_SB

CL_RST# AJ23 → CL_RST#0 [6,29]

MEM_LED/GPIO24 AJ27 R284 0/04 → BT_OFF# [27]
ME_EC_ALERT/GPIO10 AJ24 ME_SMC_ALERT#
EC_ME_ALERT/GPIO14 AF22 T250
WOL_EN/GPIO9 AG19 T141 T144

100ohm to 499 ohm check list -- series 500ohm to IMVP6+

LAN_RST pin : 1.if used pci LAN please tie to PLTRST# 2.if used PHY LAN please tie to RSMRST#

R819 10K/04 → 3VSUS

ADD (ww36 request)

3V_S5
R631 3.24K/F/06
R633 453/F/04
C798 1U/10V/04

Controller Link 1 VREF for IAMT support only

+3V
R338 3.24K/F/06
R344 453/F/04
C511 1U/10V/04

Controller Link 0 VREF for IAMT support only

14M_ICH R856 *33/04
CLKUSB_48 R857 33_04
C953 10P/04
C952 *10P/04

No Reboot strap

HDA_SPKR	Low = Default High = No Reboot

ACZ_SPKR R411 *10K

SI-2 Change

CRB STUFF 2K%1
R657 2K/F/04
C818 .047U/10V/04
[6,35] DELAY_VR_PWRGOOD
ECPWROK
R661 100K/06
U43 TC7SH08FU
ICH_PWROK
R667 10K/06

Board ID	15 " AT3U 965GM DUAL HDD (0:0:1:1:1) BOARD ID 7	
ID0	R692 Stuff	R693 not Stuff
ID1	R688 Stuff	R448 not Stuff
ID2	R690 Stuff	R689 not Stuff
ID3	R760 Stuff	R660 not Stuff
ID4	R761 Stuff	R652 not Stuff

R660 *10K/06 BOARD_ID3 R760 10K/06
R652 *10K/06 BOARD_ID4 R761 10K/06
R692 10K/06 BOARD_ID0 R693 *10K/06
R688 10K/06 BOARD_ID1 R448 *10K/06
R690 10K/06 BOARD_ID2 R689 *10K/06

NB5/RD1/HW2

PROJECT : AT3U
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH7-M GPIO(3/4)	2A

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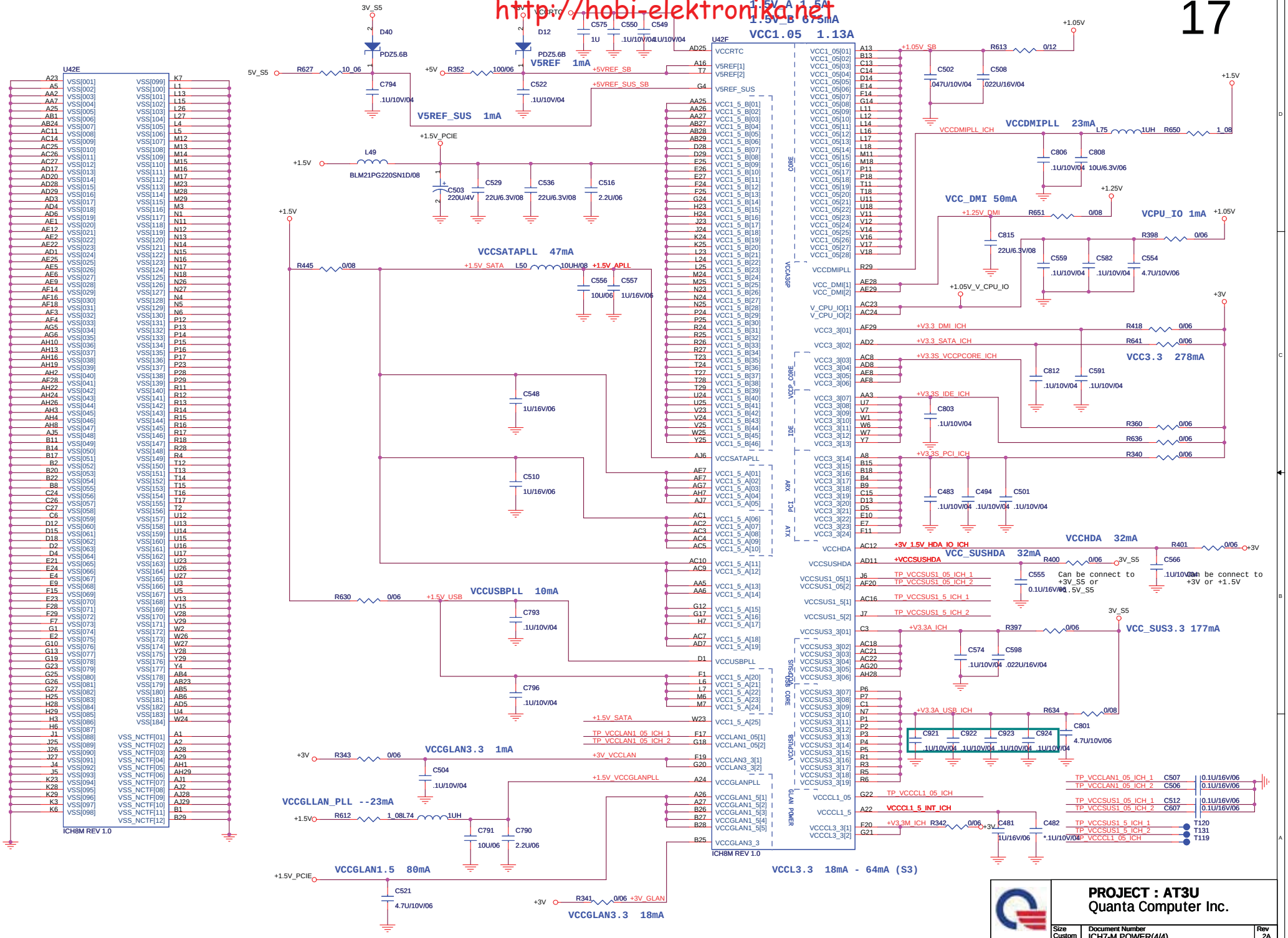
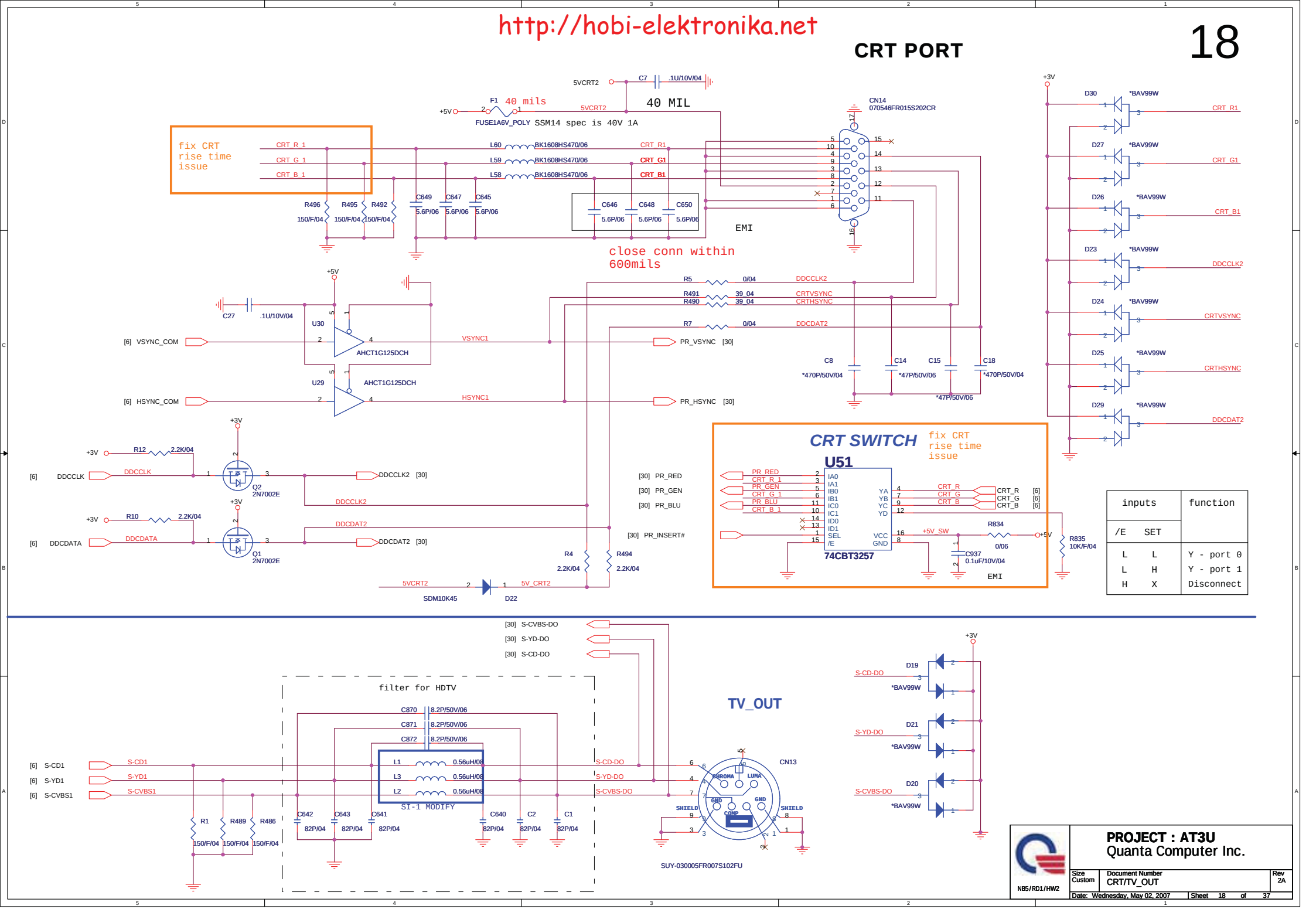
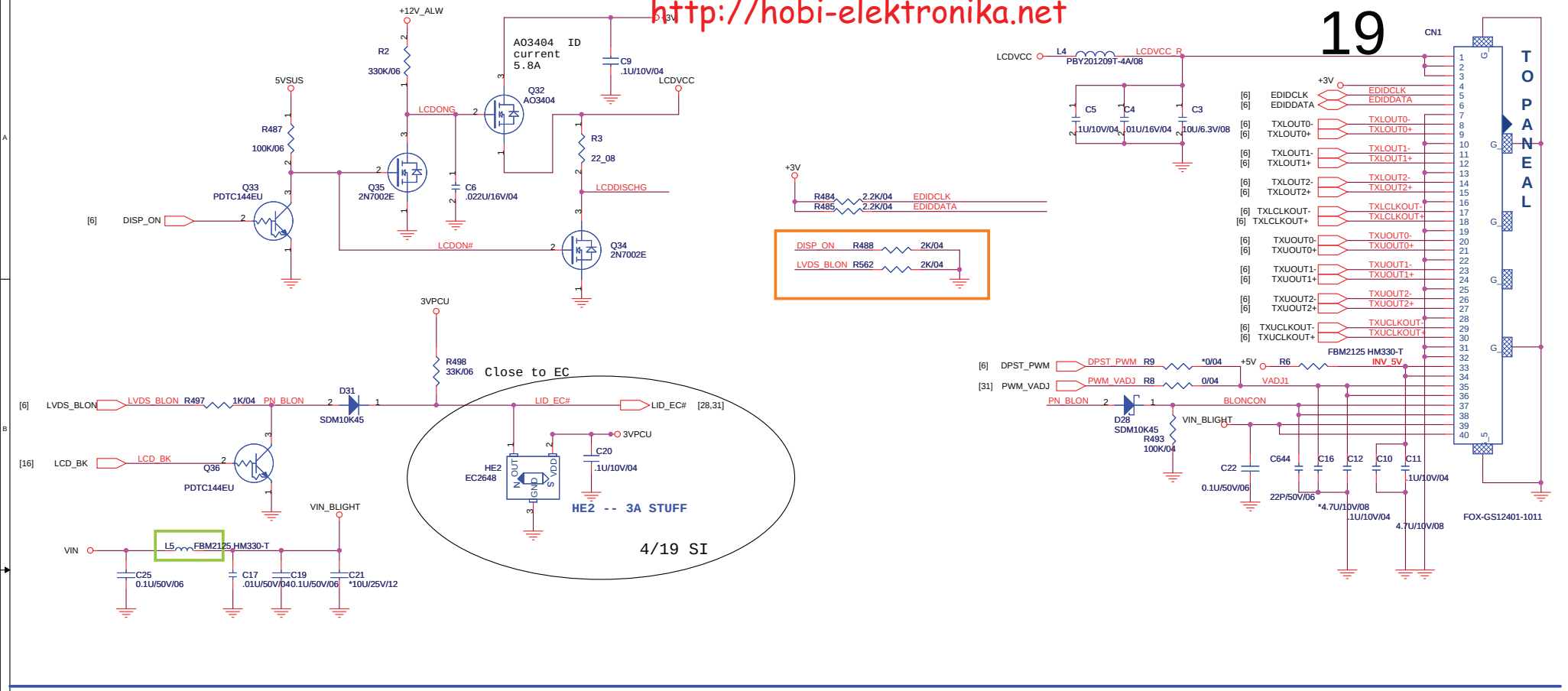


CRT PORT



PROJECT : AT3U		
Quanta Computer Inc.		
Size: Custom	Document Number: CRT/TV_OUT	Rev: 2A
NB5/RD1/HW2	Date: Wednesday, May 02, 2007	Sheet 18 of 37



PROJECT : AT3U
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN	2A

NB5/RD1/HW2

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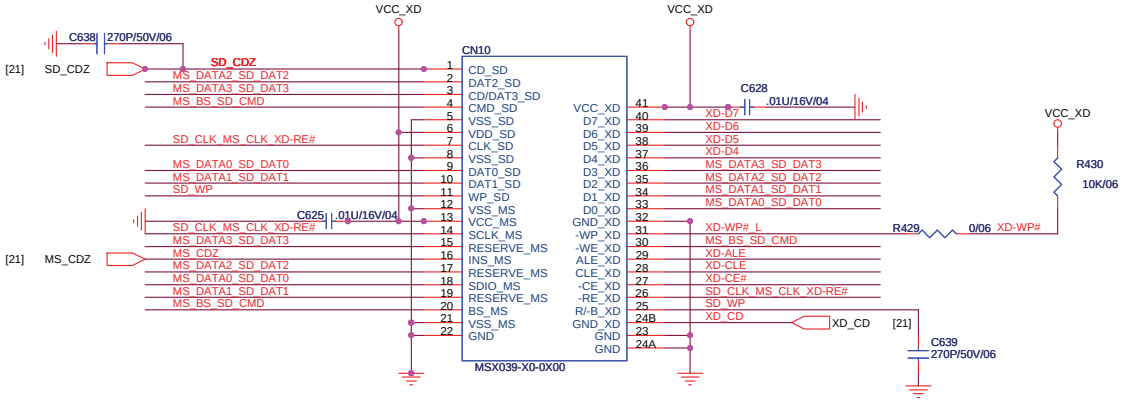
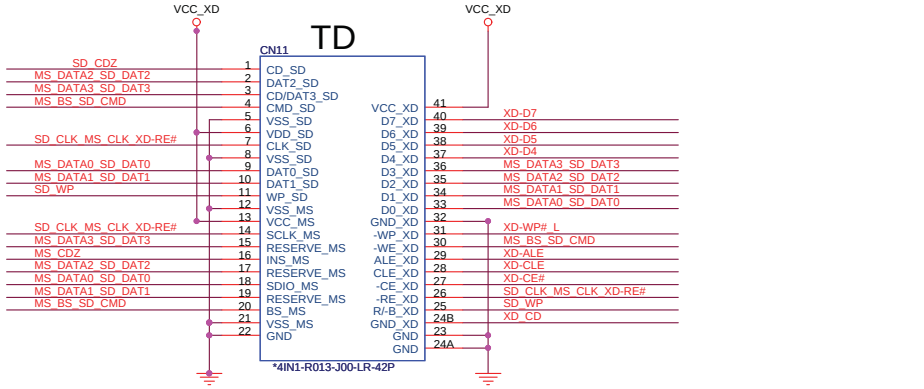
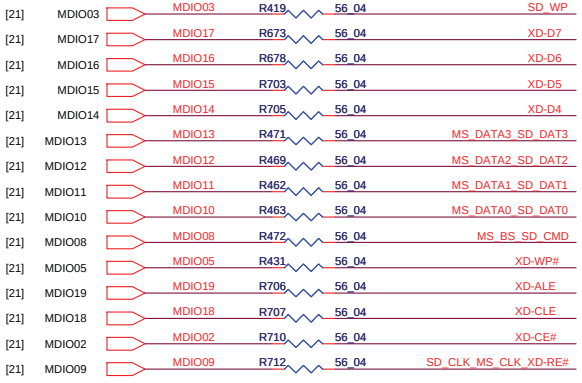
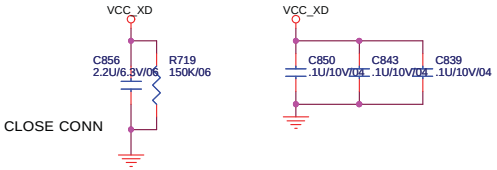
5 IN1 CARD READER
XD,MMC/SD,MS/MSP

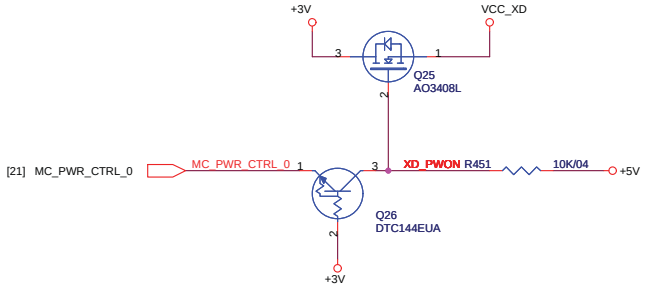




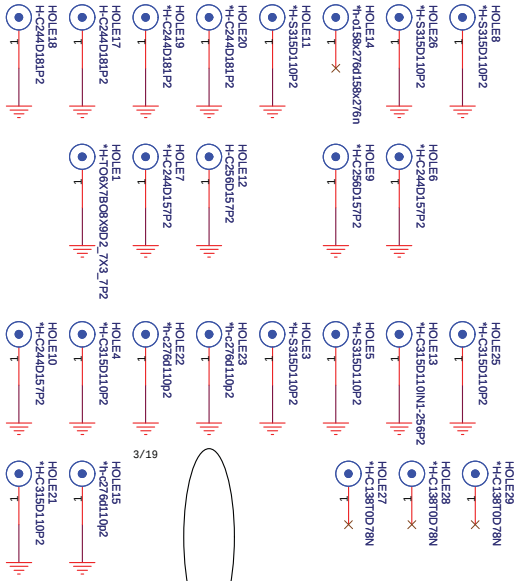
bom create 2'nd source







SCREW HOLE

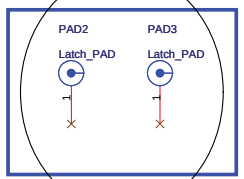


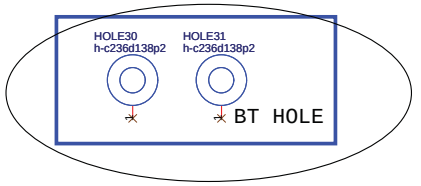
3/19

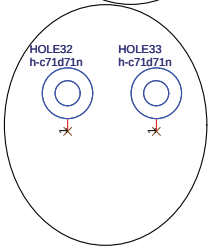
SI 4/20 del hole16

SI 4/30 del PAD1,9,10,13,16

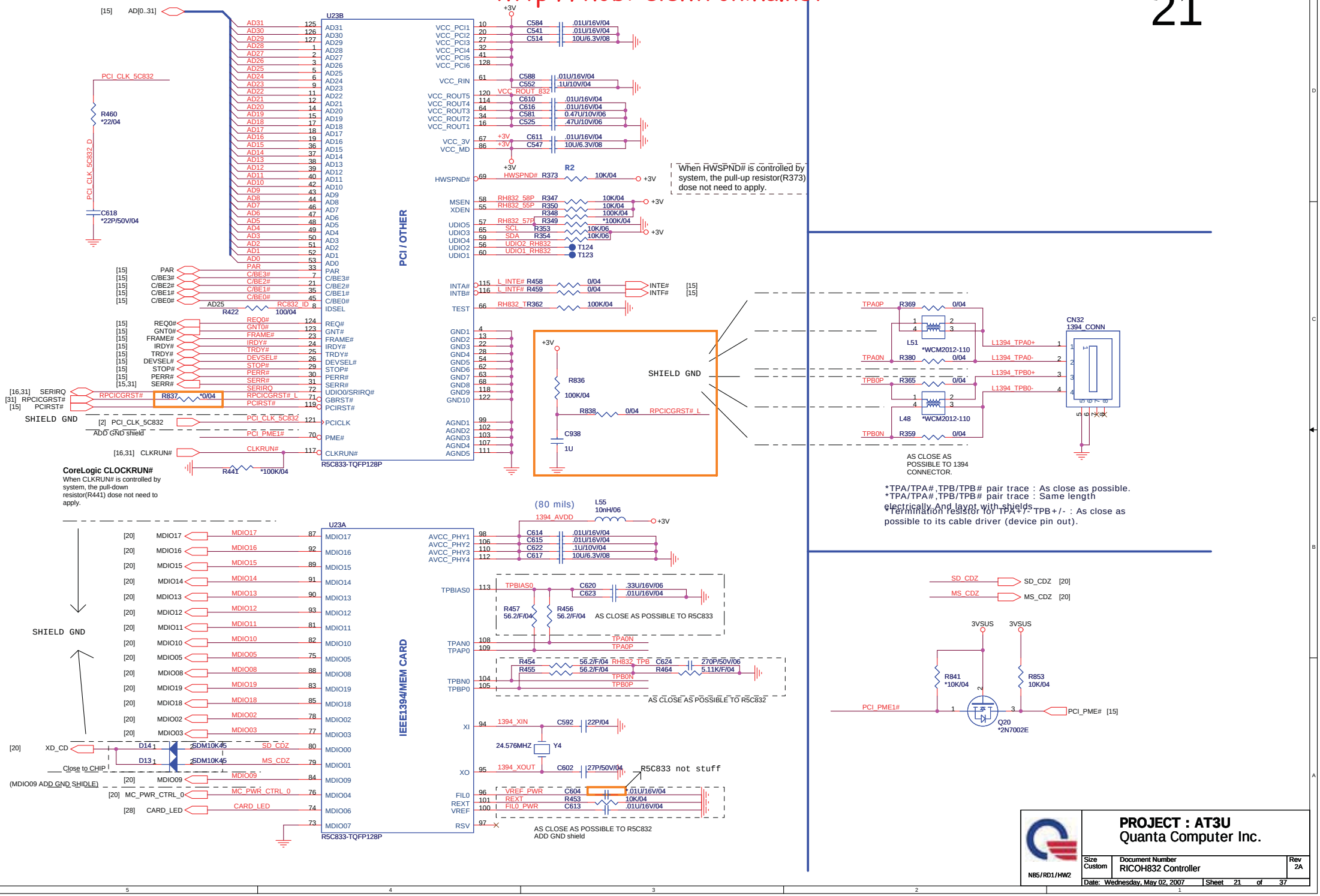
BT PAD

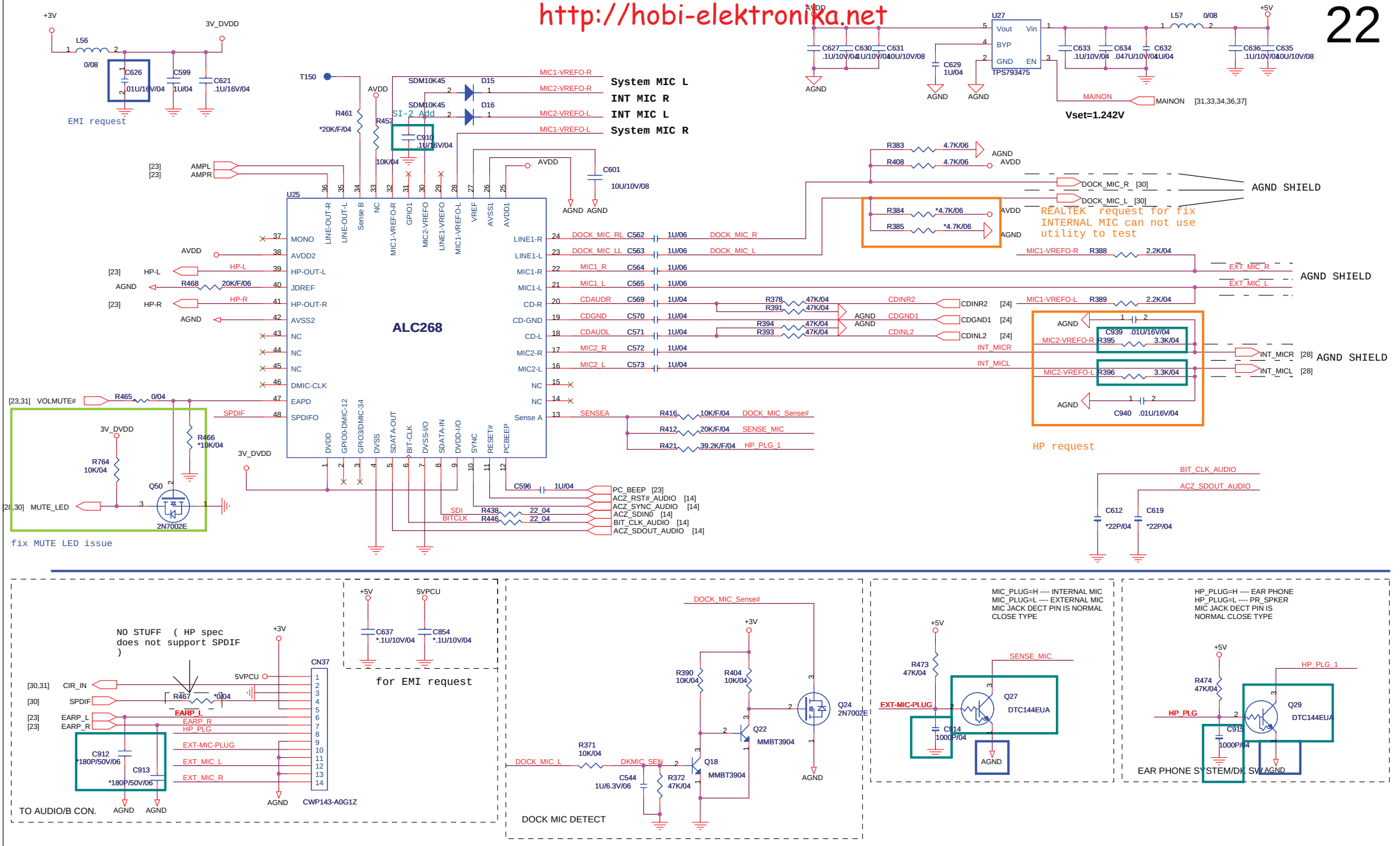






PROJECT : AT3U Quanta Computer Inc.		
NB5/RD1/HW2	Size: Custom Document Number: CARD READER/HOLE	Rev: 1A
	Date: Wednesday, May 02, 2007	Sheet 20 of 37





PROJECT : AT3U
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Azalia CONEXANT20549-12	2A

NB5/RD1/HW2

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AUDIO AMPLIFIER

0312 Gain Table

GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	**0**	**0**	**15.6dB**
1	1	0	21.6dB
x	x	1	4.1dB

remove r739 ,r731 from realtek request for fix BO voice when audio jack unplug

TPA0312 PWP24

EMI request

INT. SPEAKER

EMI requests change footprint
EMI request

PCSPK BEEP

TO CODE

TO AMP

SI-1 add R765 and remove * part

SI-1 add R807 and remove *part

(AMP BEEP ENABLE AT SYSTEM BOOT)
H=ENABLE
L=DISABLE

LINE OUT Amplifier

LINE OUT Amplifier

U46 MAX4411

QFN20-4X4-5-25P

MAX4411 EP can NOT be connected to GND. Please leave EP pins floating.

HP recommend

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Quanta Computer Inc.	
Size: Custom	Document Number: JACK/AMP_TAP0312
Rev: 2A	
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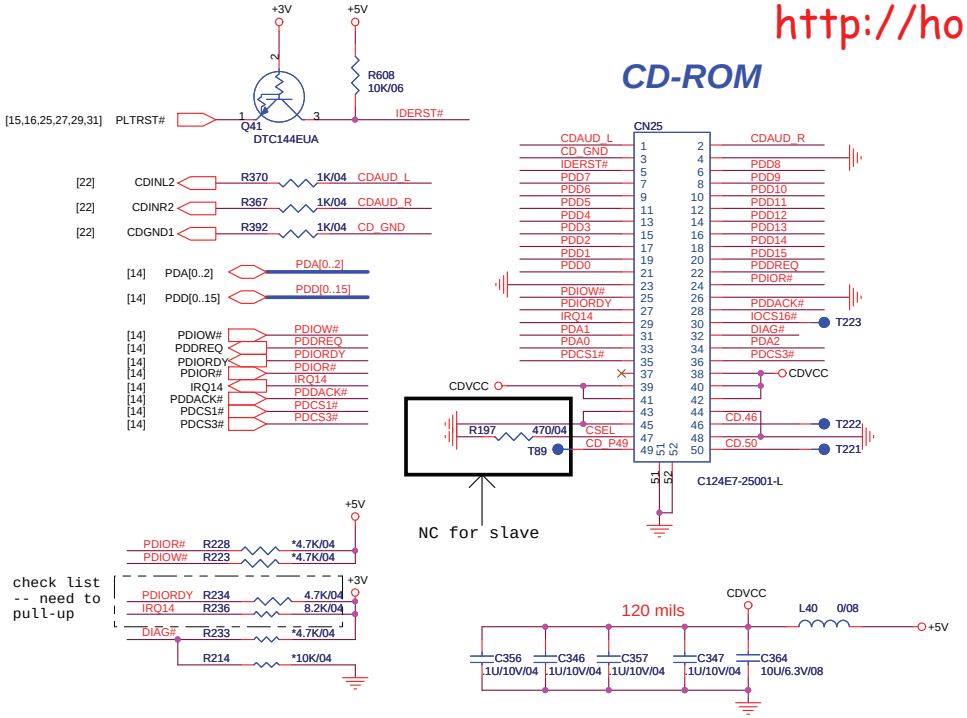
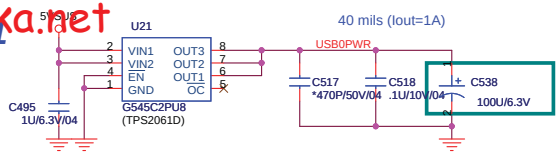
NB5/RD1/HW2

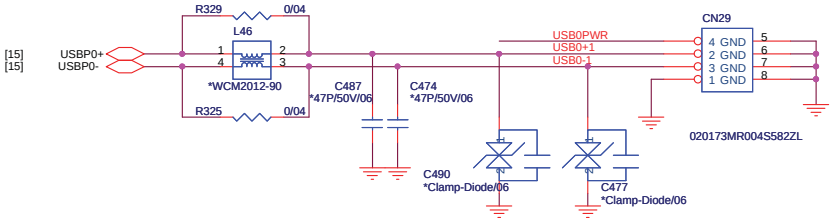
CD-ROM



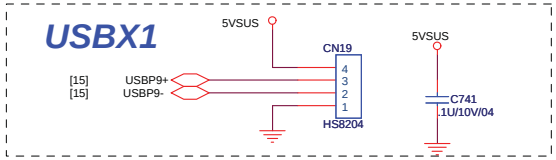
USBX1



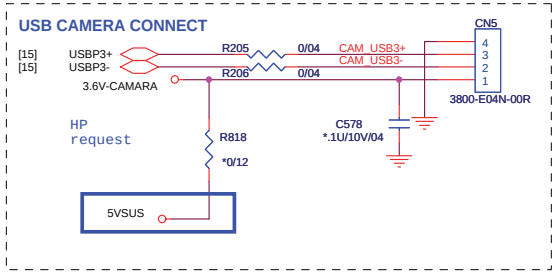
USB 0

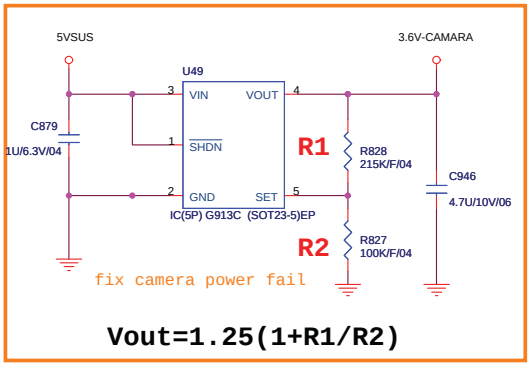


USBX1

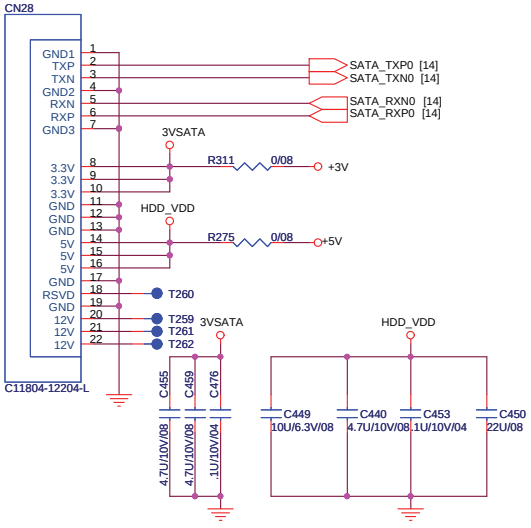


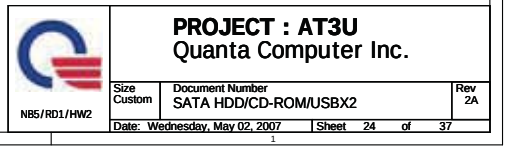
USB CAMERA CONNECT





SATA_2 CONNECTOR





fix 10/100 LAN LED issue

E : Stuffed for 8101E(10/100)

R21 value should be 2.49K (1%) for 8111B/8111C application. R21 should be 2.0K(1%) for 8101E application

BLOCK A is only for RTL8101E application.

Block A

SI 4/20

SI 4/20

SI 4/20

for 93C56 used. NC if 93C46 is used.

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

Remove R70 for 8111B and 8111C

close U6

NS892405:10/100

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Size: Custom	Document Number: RTL8101E	Rev: 2A
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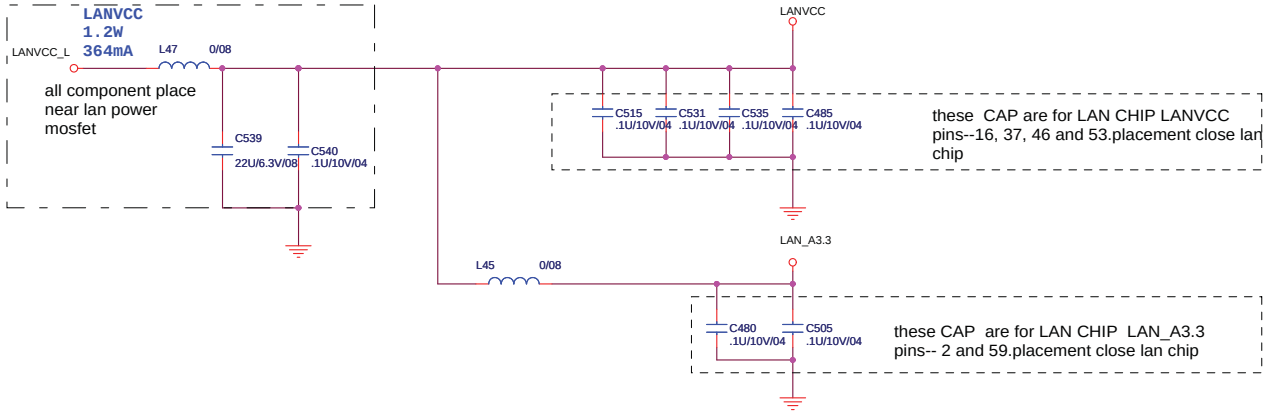
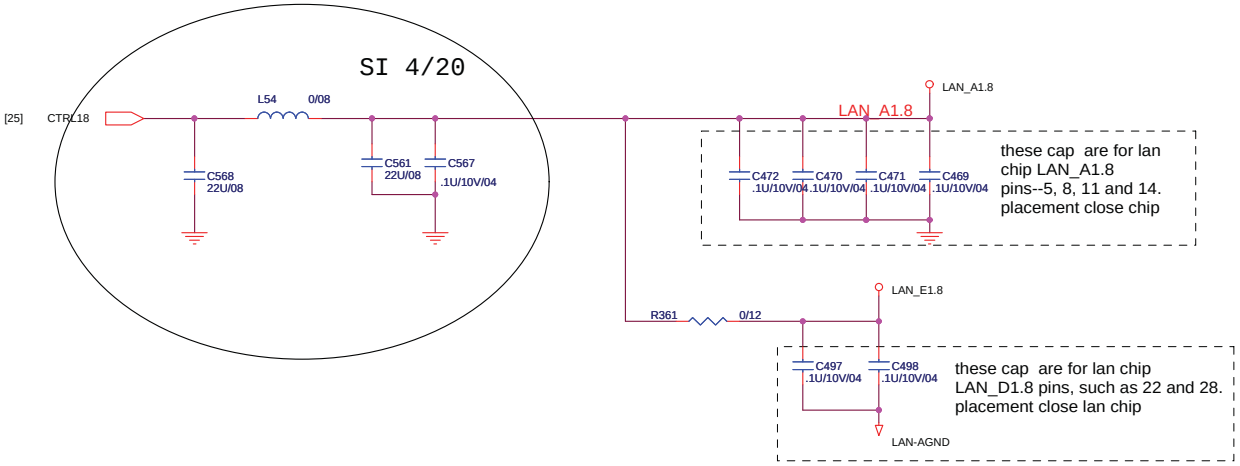
E : Stuffed for 8101E(10/100)

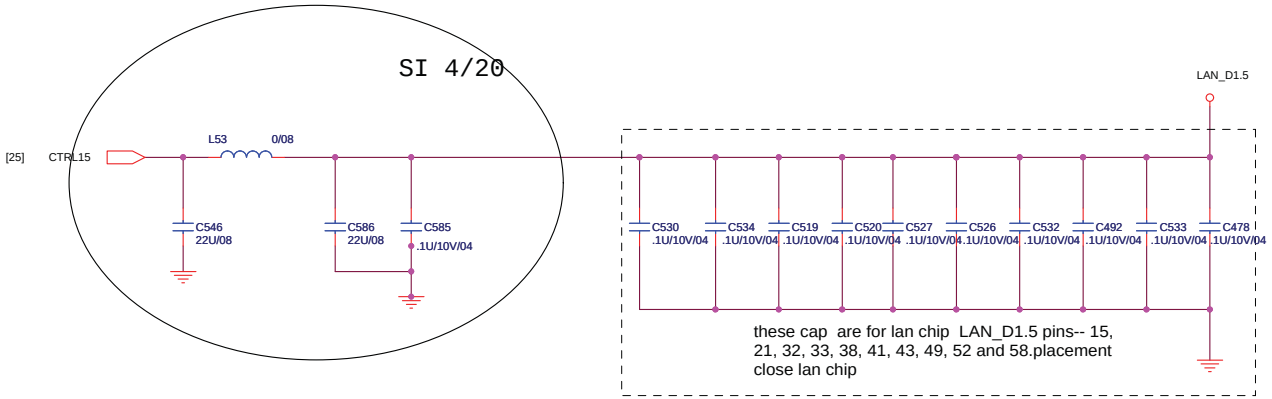




Power domain chart

	RTL8111B / RTL8101E	
LANVCC	*3.3V*	
LAN_D1.8	*1.8V*	
LAN_A1.8	*1.8V*	
LAN_D1.5	*1.5V*	

	Q19	Q21
RTL8111B	*Need*	*Need*
RTL8101E	*N/A*	*N/A*



NB5/RD1/HW2

PROJECT : AT3U
Quanta Computer Inc.

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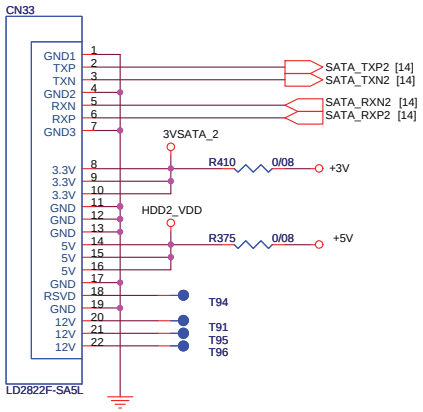
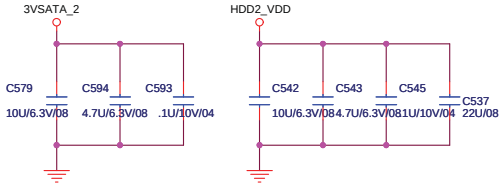
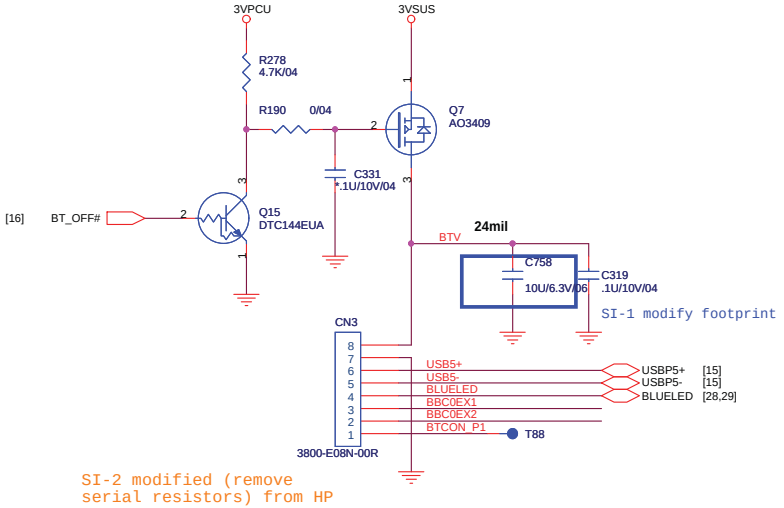
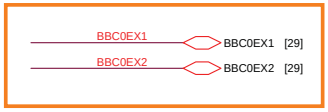
SATA_1 CONNECTOR





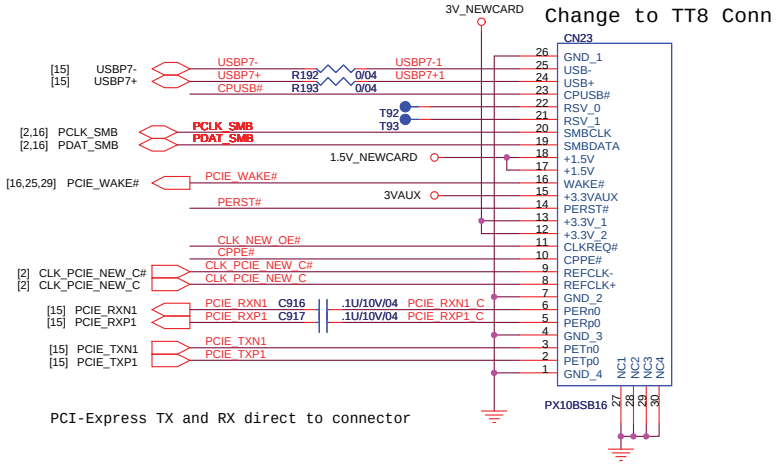
BLUETOOTH



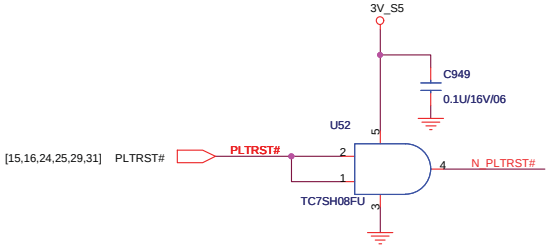


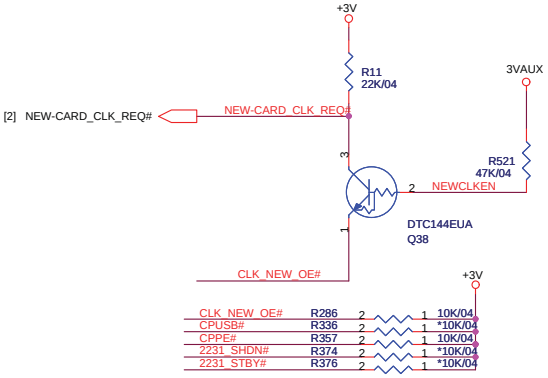
NEWCARD

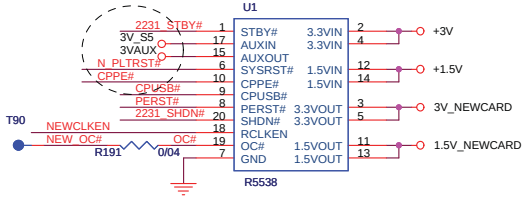
Change to TT8 Conn

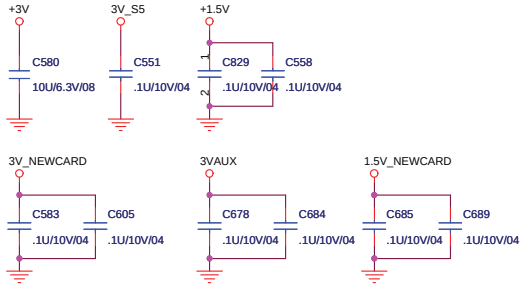


PCI-Express TX and RX direct to connector









PROJECT : AT3U
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NEW CARD/BT	2A

NB5/RD1/HW2

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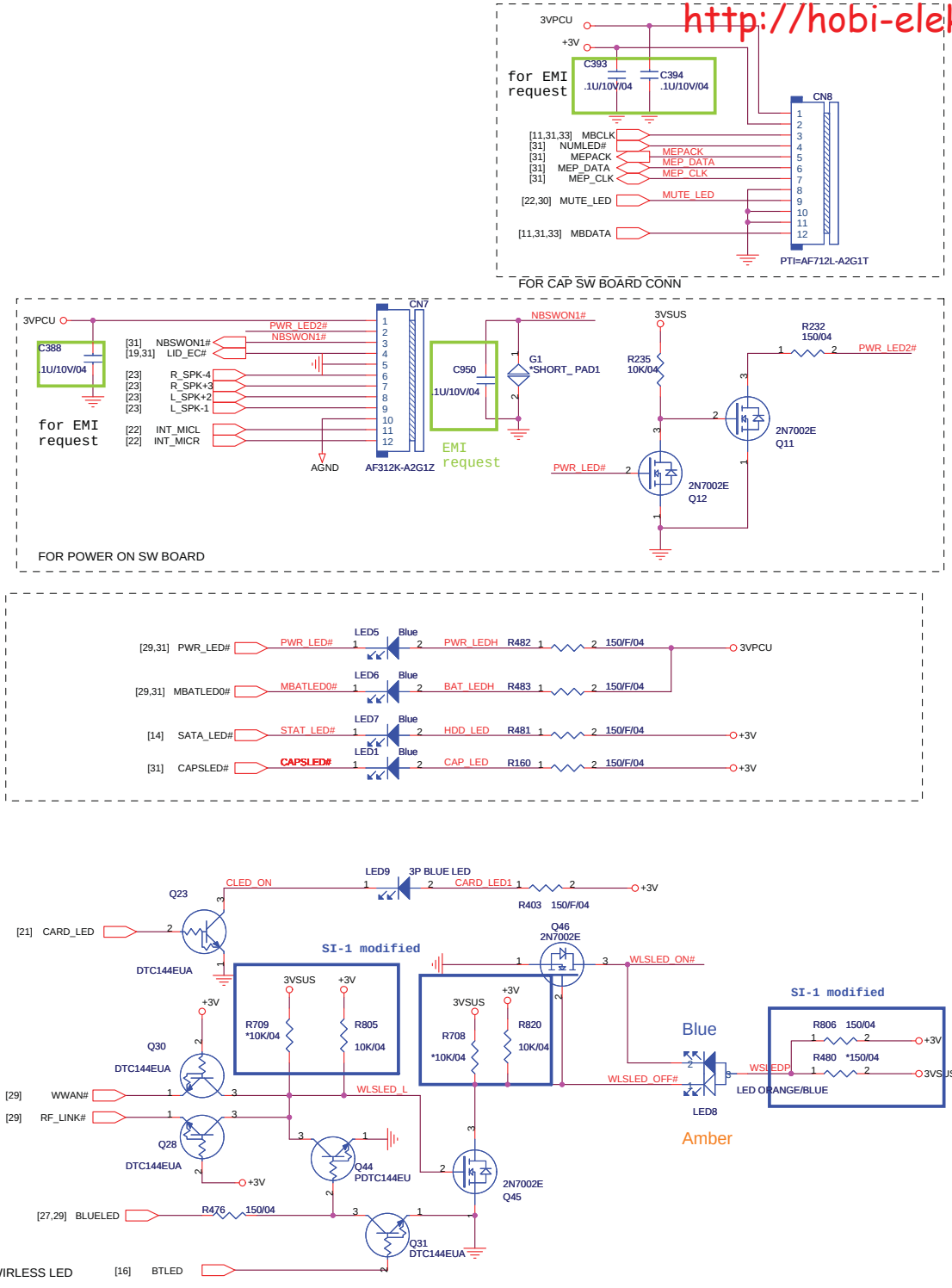
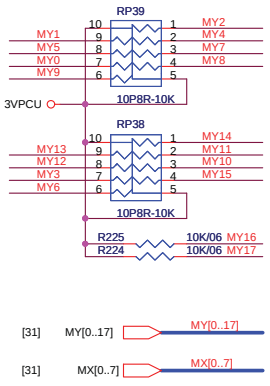


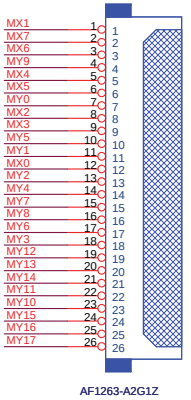
MY5 C423 220P/50V/06
MY6 C410 220P/50V/06
MY3 C409 220P/50V/06
MY7 C412 220P/50V/06
MY8 C411 220P/50V/06
MY9 C377 220P/50V/06
MY10 C404 220P/50V/06
MY11 C405 220P/50V/06

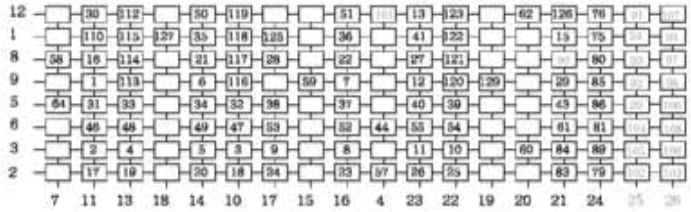
MY1 C422 220P/50V/06
MY2 C414 220P/50V/06
MY4 C413 220P/50V/06
MY0 C424 220P/50V/06
MX4 C426 220P/50V/06
MX6 C374 220P/50V/06
MX3 C367 220P/50V/06
MX2 C368 220P/50V/06

MX7 C376 220P/50V/06
MX0 C366 220P/50V/06
MX5 C425 220P/50V/06
MX1 C375 220P/50V/06
MY12 C408 220P/50V/06
MY13 C407 220P/50V/06
MY14 C406 220P/50V/06
MY15 C403 220P/50V/06
MY16 C370 220P/50V/06
MY17 C369 220P/50V/06

KEYBOARD PULL-UP







12	30	112		50	119			51	103	13	123		62	126	76	97	107							
1	110	113	127	35	118	125		36		41	122			15	75		91							
8	58	16	114		21	117	28		22		27	121				97	80		90	87				
9		1	111		6	116		59	7		12	120	29		20	85								
5	54	31	33		34	32	38		37		40	39			43	86		89						
6		46	48		49	47	53		52	44	55	54			61	81		101	106					
3		3	4		5	8	9		8		11	10		60	84	69		102	105					
2		17	19		20	18	24		23	57	26	25		83	79			103						
	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	75	26						

PROJECT : AT3U
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LED/KEYBOARD/SW	2A
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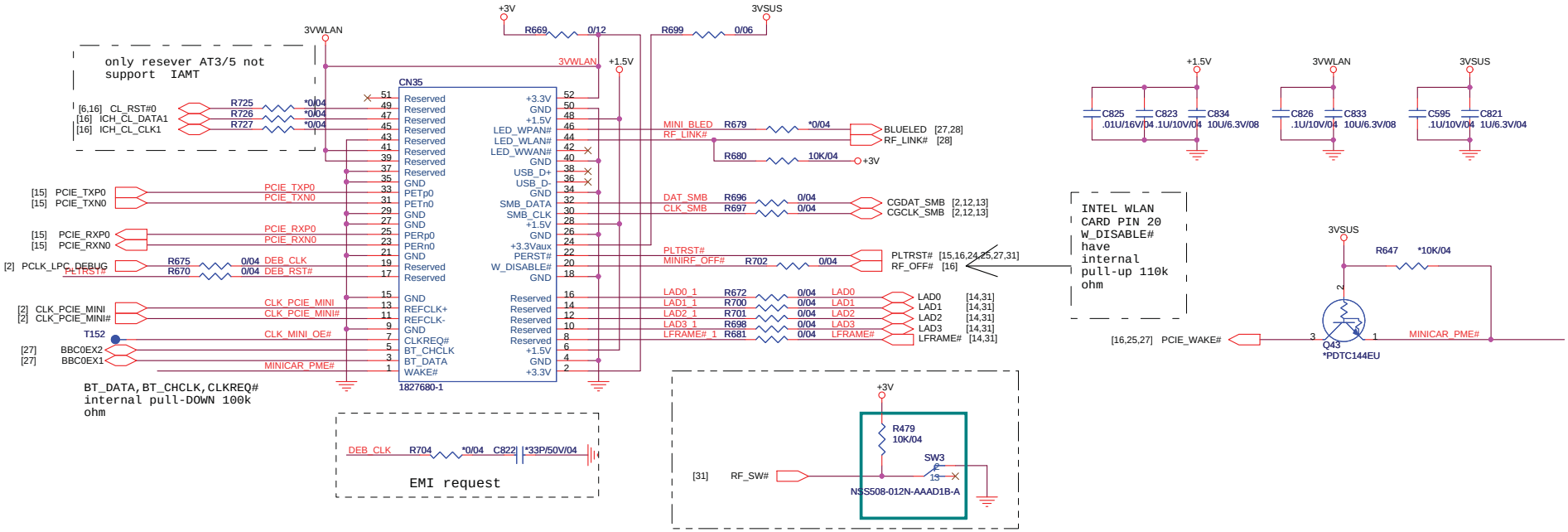
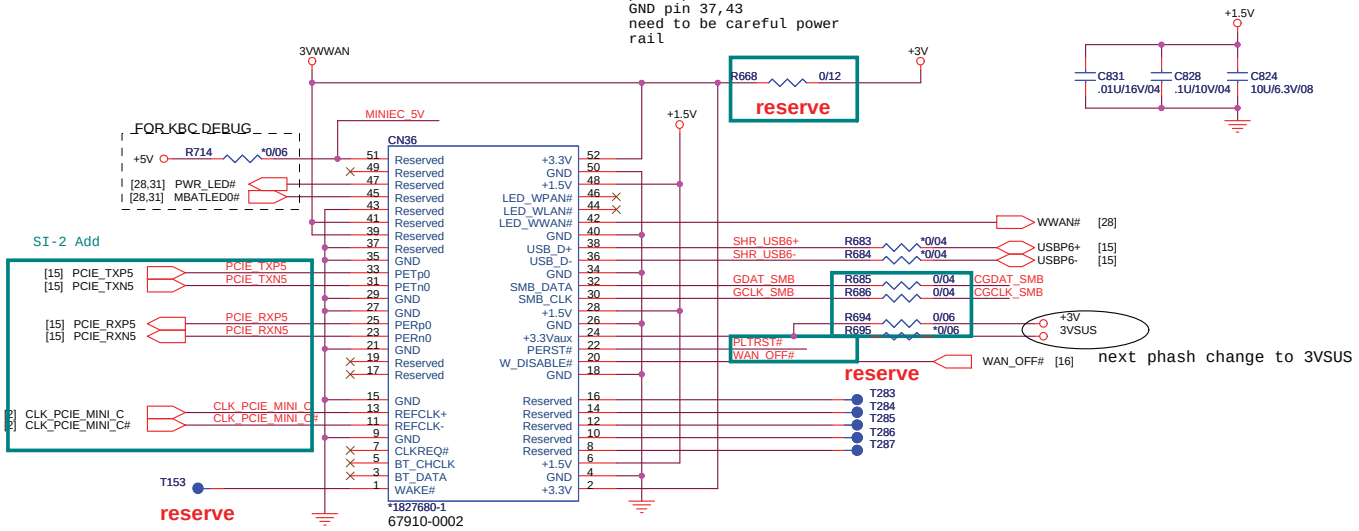
Mini PCI-E Card 1
WLAN



Mini PCI-E Card 2

WWAN -- have 2.8A 7W power consumption
power pin 24.39.41
GND pin 37,43
need to be careful power rail



NB5/RD1/HW2	PROJECT : AT3U Quanta Computer Inc.	
	Size: Custom Document Number: MINI CARD X2	Rev: 2A
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CABLE DOCK

support docking
SPIDF

+1.5V
R522 33_04
C883 .1U/10V/04
SPDDK_V
Q37 MMBT3904
[22] SPDIF
R531 510/F/04
SPDIF_DK
R525 510/F/04
C681 68P/50V/04
L68 0/06
SPD_DK
SPDIF_DOCK

DOCK_VA
[33] DOCK_VA
L61 FBMJ3216HS480NT/12
VA_P
C658 0.1U/50V/06
C651 0.1U/50V/06

SI change EMI request
[18] PR_GEN
[18] PR_RED
[18] DDCDAT2
[18] PR_BLU
[18] PR_HSYNC
[18] DDCCLK2
[18] PR_VSYNC
R45 BK1608LL680/06
R38 BK1608LL680/06
R54 BK1608LL680/06
R811 0/06
R812 0/06
CRT_GDK
CRT_RDK
CRT_BDK
PR_HSYNC_D
PR_VSYNC_D
USB4-1
USB4+1
EMI request

CN18
VA_P
VDD
VSS
S-YD-DO-PR R510 0/04 S-YD-DO [18]
S-CD-DO-PR R516 0/04 S-CD-DO [18]
S-CVBS-DO-PR R518 0/04 S-CVBS-DO [18]
CIR_IN [22,31]
PWR_ON
MUTE_LED [22,28]
SLP_BTN# [31]
JACK_DETECT# [23]
VOLME_UP# [31]
VOLME_DN# [31]
SPDIF_DOCK
RSPK_DK C60 100U/6.3V AGND
LSPK_DK C75 100U/6.3V DOCK_RSPK+ [23]
DOCK_LSPK+ [23]
DOCK_MIC_R [22]
DOCK_MIC_L [22]
AGND
DOCK_PRESENT
QL1122L-H212AR-7F

[25] +LAN_MX1_PR
[25] -LAN_MX1_PR
[25] +LAN_MX0_PR
[25] -LAN_MX0_PR
VIN
C894 0.1U/50V/06
EMI request

R528 0/04
[15] USBP4-
[15] USBP4+
L67 *CMM211T-900M-S
R526 0/04
USB4-1
USB4+1

PR_HSYNC_D
PR_VSYNC_D
C892 *47P/50V/06
C893 *47P/50V/06
EMI request

+3V
3VPCU
R844 100K/04
R548 *100K/04
PR_INSERT#
PR_INSERT# [18]
docking insert is HI voltage
DOCK_PRESENT
R579
DKPR#
1K/04
Q40 2N7002E
R573 2K/F/06

+5V
5VSUS
R520 10K/04
DK_PWRON
D33 1N4148
D34 1N4148
PWR_ON
R527 15K/04
S0: 4V
S3: 2.5V
S4/S5: 0V
*Check voltage on DB

DOCK_MIC_R
DOCK_MIC_L
RSPK_DK
LSPK_DK
JACK_DETECT#
VOLME_DN#
CIR_IN
C673 *120P/50V/04
C677 *120P/50V/04
C674 270P/25V/04
C897 180P/50V/04
C898 180P/50V/04
C902 180P/50V/04
C903 180P/50V/04
EMI request

PR_GEN
PR_RED
PR_BLU
CRT_GDK
CRT_RDK
CRT_BDK
C918 5.6P/06
C919 5.6P/06
C920 5.6P/06
C941 5.6P/06
C942 5.6P/06
C943 5.6P/06
fix docking R.G.B signals measure fail
R56 150/F/04
R30 150/F/04
R39 150/F/04

S-YD-DO-PR
S-CD-DO-PR
S-CVBS-DO-PR
R519 *150/F/04
R517 *150/F/04
R506 *150/F/04

FAN

CPU FAN
D39 *SSM34PT L-F
CN22
20 mil
L73 0/08
+5V
C749 2.2U/6.3V/06
C748 1U/10V/04
[31]
FAN1ON
5VFAN1
PTI=CWP043-A0G1T
R594 4.7K/06
FAN1SIG
FAN1SIG [31]

FAN1 PWM CONNECTOR

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	Size: Custom Document Number: CABLE DOCKING/FAN	Rev: 2A
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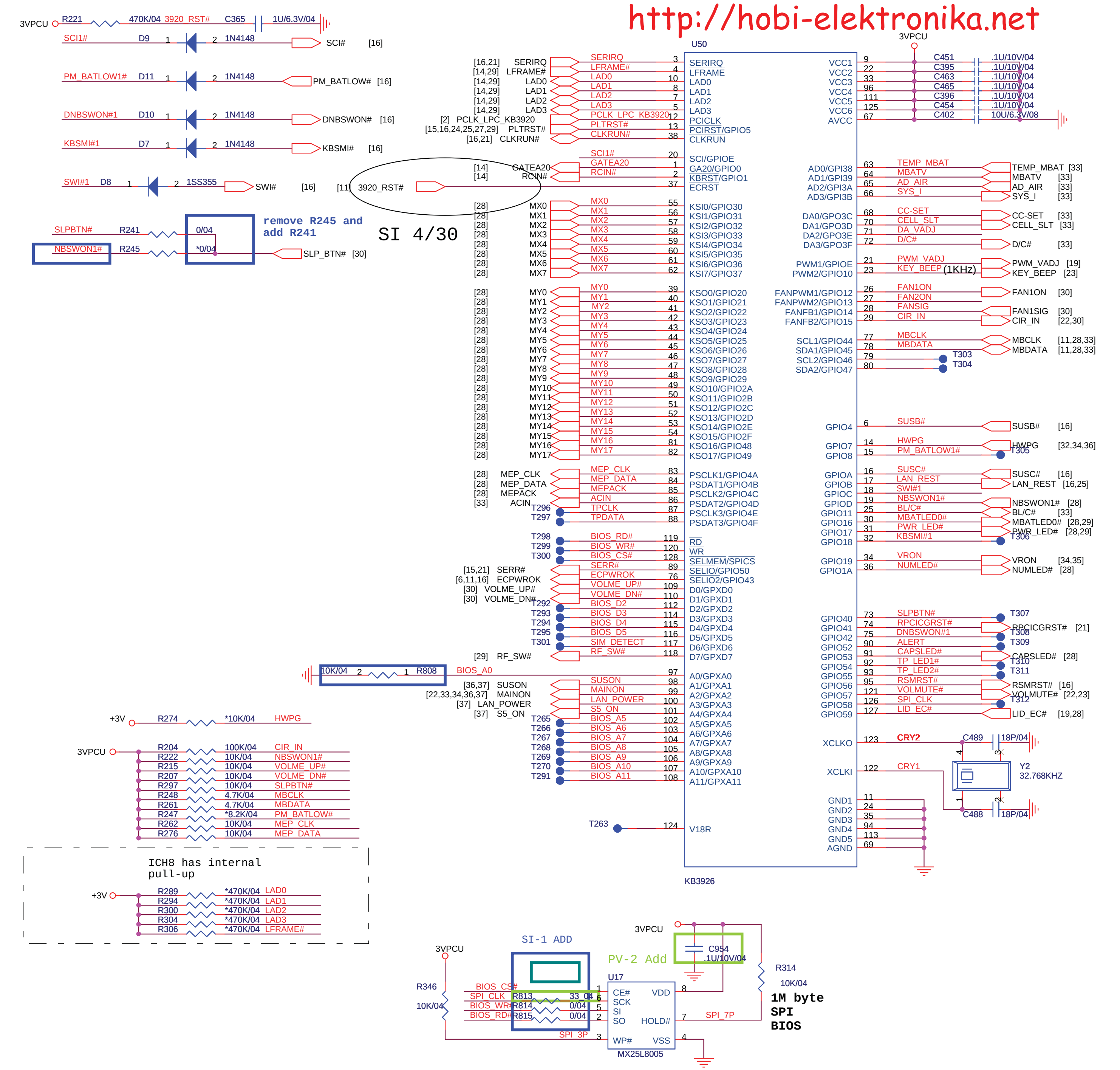
http://hobi-elektronika.net



U50
KB3926
3VPCU
R221 470K/04 3920_RST# C365 1U/6.3V/04
SCI1# D9 1N4148 SCI# [16]
PM_BATLOW1# D11 1N4148 PM_BATLOW# [16]
DNBSWON#1 D10 1N4148 DNBSWON# [16]
KBSMI#1 D7 1N4148 KBSMI# [16]
SWI#1 D8 1SS355 SWI# [16]
[11] 3920_RST#
SLPBTN# R241 0/04
NBSWON1# R245 *0/04 SLP_BTN# [30]
remove R245 and add R241
SI 4/30
SERIRQ LFRAME LAD0 LAD1 LAD2 LAD3 PCICLK PCIRST/GPIO5 CLKRUN
SCI/GPIOE GA20/GPIO0 KBRST/GPIO1 ECRST
KSI0/GPIO30 … KSI7/GPIO37
KSO0/GPIO20 … KSO17/GPIO49
PSCLK1/GPIO4A PSDAT1/GPIO4B PSCLK2/GPIO4C PSDAT2/GPIO4D PSCLK3/GPIO4E PSDAT3/GPIO4F
RD WR SELMEM/SPICS SELIO/GPIO50 SELIO2/GPIO43
D0/GPXD0 … D7/GPXD7
A0/GPXA0 … A11/GPXA11
V18R
VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 AVCC
C451 C395 C463 C465 C396 C454 .1U/10V/04 C402 10U/6.3V/08
AD0/GPI38 AD1/GPI39 AD2/GPI3A AD3/GPI3B
TEMP_MBAT [33] MBATV [33] AD_AIR [33] SYS_I [33]
DA0/GPO3C DA1/GPO3D DA2/GPO3E DA3/GPO3F
CC-SET [33] CELL_SLT [33] D/C# [33]
PWM1/GPIOE PWM2/GPIO10 PWM_VADJ [19] KEY_BEEP (1KHz) [23]
FANPWM1/GPIO12 FANPWM2/GPIO13 FANFB1/GPIO14 FANFB2/GPIO15
FAN1ON [30] FAN1SIG [30] CIR_IN [22,30]
SCL1/GPIO44 SDA1/GPIO45 SCL2/GPIO46 SDA2/GPIO47
MBCLK [11,28,33] MBDATA [11,28,33] T303 T304
GPIO4 SUSB# [16]
GPIO7 GPIO8 HWPG PM_BATLOW1# [32,34,36] T305
GPIOA GPIOB GPIOC GPIOD GPIO11 GPIO16 GPIO17 GPIO18
SUSC# [16] LAN_REST [16,25] SWI#1 NBSWON1# [28] BL/C# [33] MBATLED0# [28,29] PWR_LED# [28,29] KBSMI#1 T306
GPIO19 GPIO1A VRON [34,35] NUMLED# [28]
GPIO40 … GPIO59
SLPBTN# T307 RPCICGRST# [21] T308 DNBSWON#1 ALERT T309 CAPSLED# [28] T310 TP_LED1# TP_LED2# T311 RSMRST# [16] VOLMUTE# [22,23] SPI_CLK T312 LID_EC# [19,28]
XCLKO XCLKI CRY2 CRY1 C489 18P/04 C488 18P/04 Y2 32.768KHZ
GND1 GND2 GND3 GND4 GND5 AGND
10K/04 R808 BIOS_A0
[36,37] SUSON [22,33,34,36,37] MAINON [37] LAN_POWER [37] S5_ON
+3V R274 *10K/04 HWPG
3VPCU R204 100K/04 CIR_IN; R222 10K/04 NBSWON1#; R215 10K/04 VOLME_UP#; R207 10K/04 VOLME_DN#; R297 10K/04 SLPBTN#; R248 4.7K/04 MBCLK; R261 4.7K/04 MBDATA; R247 *8.2K/04 PM_BATLOW#; R262 10K/04 MEP_CLK; R276 10K/04 MEP_DATA
ICH8 has internal pull-up
+3V R289 *470K/04 LAD0; R294 *470K/04 LAD1; R300 *470K/04 LAD2; R304 *470K/04 LAD3; R306 *470K/04 LFRAME#
SI-1 ADD
PV-2 Add
3VPCU C954 .1U/10V/04 R314 10K/04
U17 MX25L8005 CE# SCK SI SO WP# VDD HOLD# VSS
R346 10K/04 BIOS_CS# SPI_CLK R813 33_04 BIOS_WR# R814 0/04 BIOS_RD# R815 0/04 SPI_3P SPI_7P
1M byte SPI BIOS

STRAP PIN

MY2	49	TP_SPI: Default flash access Low: Boot from SPI flash part HIGH: Boot from ISA flash part
MY3	50	TP_ISP: In System Programming Mode Low: ISP mode HIGH: Normal Mode

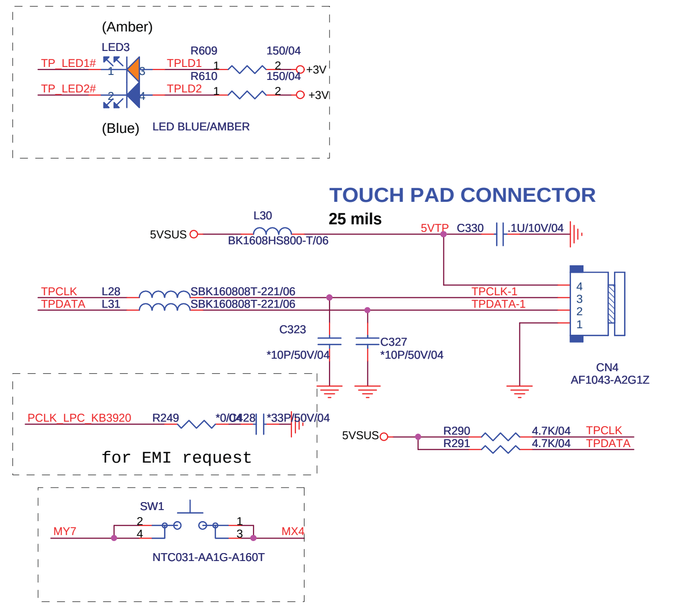
DEL R209,R210,R218,R219,R220
MY2 R208 *10K/04
MY3 R212 *0/04

All hardware straps default internal pull-up, so don't need pull-UP outside.
A TEST need try
--andrew ????

SELECT KBC TPYE

PIN NAME	USE KBC3920	USE KBC3926
MY2	R208	REMOVE R208
BIOS_A0	REMOVE R808	R808

TOUCH PAD CONNECTOR



(Amber)
LED3 R609 150/04 TP_LED1# TPLD1 +3V
R610 150/04 TP_LED2# TPLD2 +3V
(Blue) LED BLUE/AMBER
25 mils
5VSUS L30 BK1608HS800-T/06 5VTP C330 .1U/10V/04
TPCLK L28 SBK160808T-221/06 TPCLK-1
TPDATA L31 SBK160808T-221/06 TPDATA-1
C323 *10P/50V/04 C327 *10P/50V/04
CN4 AF1043-A2G1Z
PCLK_LPC_KB3920 R249 *0/04 C428 *33P/50V/04
for EMI request
5VSUS R290 4.7K/04 TPCLK R291 4.7K/04 TPDATA
SW1 MY7 MX4 NTC031-AA1G-A160T

PROJECT : AT3U
Quanta Computer Inc.
NB5/RD1/HW2

Size	Document Number	Rev
Custom	KB3920/ROM/TP	2A

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+12V_ALW

Place these CAPs close to FETs

Place these CAPs close to FETs

5 Volt +/- 5%
Countinue current:8A
Peak current:11A
OCP minimum 13A

3.3 Volt +/- 5%
Countinue current:5A
Peak current:7.5A
OCP minimum 10A

VIN
5V_AL
+5V_VCC1
5VPCU
3VPCU
5V_DH
5V_LX
5V_DL
3V_LX
3V_DH
PGOOD1
PGOOD2
Rds(on) 13m ohm
Rds(on) 15m ohm
+12V_ALW
[11] SYS_SHDN#
[37] MAIND
[37] SUSD
HWPG [31,34,36]
3.8A
3.4A
5.92A
2A
SI-1 MODIFY
3VSUS [15,16,17,27,28,29,34,37]

PR174 390K/04
PR175 150K/04
PR73 *47/06
PC120 1U/10V/06
PC106 10U/25V/X6S/12
PC104 1000P/04
PC105 0.1U/50V/06
PR75 0/08
PR74 0/08
PC193 0.1U/50V/06
PR177 *0/04
PR173 *0/04
PC194 *.1U/10V/04
PC190 .1U/10V/04
PC192 1U/10V/06
PR172 0/04
PC191 *.1U/10V/04
PC189 *.1U/10V/04
PR186 0/04
PR170 402K/F/04
PC87 0.1U/50V/06
PC89 1000P/04
PC86 10U/25V/X6S/12
PQ50 Si4800BDY
PL12 2.2uH_MPL73-2R2
PR50 *2.2/08
PC100 *1500P/04
PR166 0/04
PR168 *0/04
PQ48 ME4410
PC171 0.1U/50V/06
PC175 150U/6.3V/ESR18
PQ55 Si4800BDY
PL14 1.5uH_MPL73-1R5
PC184 150U/6.3V/ESR18
PC187 0.1U/50V/06
PR171 *0/04
PR169 0/04
PR160 *2.2/08
PC185 *1500P/04
PQ59 SI4420DY
PC119 0.1U/50V/06
PR72 1_06
PR167 309K/F/04
PU10 ISL6236IRZA-T
PC186 0.1U/50V/06
PR164 1_06
PR161 *SHORT-1A
PC111 0.1U/50V/06
PC110 0.1U/50V/06
PC188 4.7U/10V/08
PD8
PD7
BAT54S
BAT54S
PC116 0.1U/50V/06
PC117 0.1U/50V/06
PR162 200K/F/04
PC207 *10P/04
PR165 39K/F/04
PR178 100K/F/04
PR176 0/04
PC94 .1U/10V/04
PQ63 ME3424
PQ49 ME4410
PC170 .1U/10V/04
PC169 .1U/10V/04
PC183 .1U/10V/04
PQ56 ME4410
PC176 .1U/10V/04
PC174 .1U/10V/04
PC172 .1U/10V/04
PQ60 ME4410
PC182 .1U/10V/04
PC179 .1U/10V/04

PROJECT : AT3U	
Quanta Computer Inc.	
N85/RD1/HW2	Size: Custom; Document Number: 3v/5v; Rev: 2A
	Date: Wednesday, May 02, 2007; Sheet 32 of 37

C30: Add PD22 for 12cell patent issue

TOP DC_JACK
65W/90W

SI-1-2 Add

SI-2 modify

SI-2 ADD

SI power

Setting the Vin min to 8V

SI-1-2 MODIFY

SI-2 ADD

Battery Low = 8V

Iinput=Vcls/Vref * 0.075/RS1
Vref=4.096V,RS1=10m-ohm

ADP TYPE	VALUE	P/N
65W	39.2K/F	CS33922FB15
90W	20K/F	CS32002FB29

CELL_SLT = 1 → 3 S
CELL_SLT = 0 → 4 S

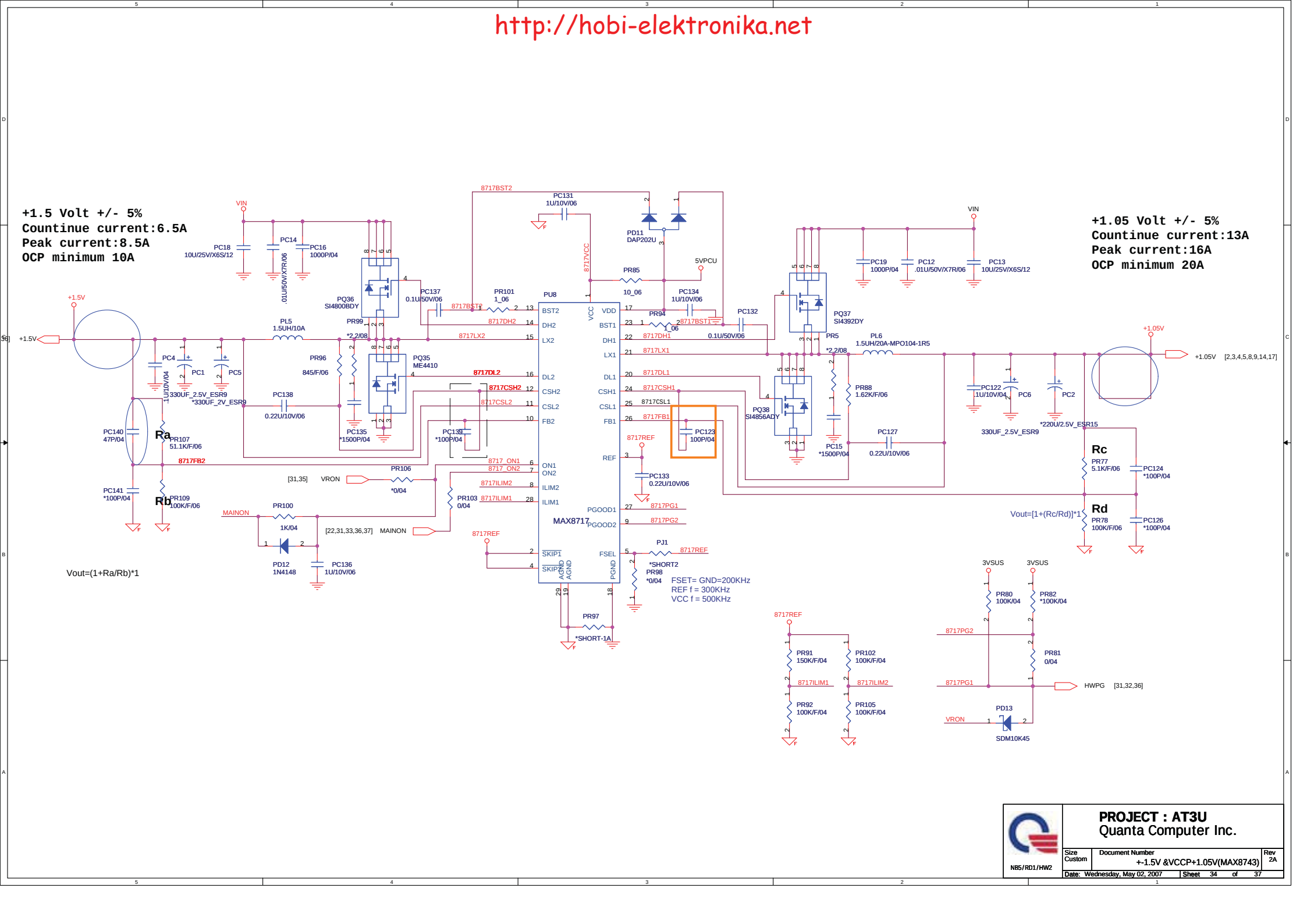
BL/C#	D/C#	M/A#	Status
0	0	0	Chareg A batt
0	0	1	Charge M batt
0	1	0	Discharge A batt
0	1	1	Discharge M batt
1	0	0	Free Dicharge
1	0	1	Free Dicharge
1	1	0	Free Dicharge
1	1	1	Free Dicharge

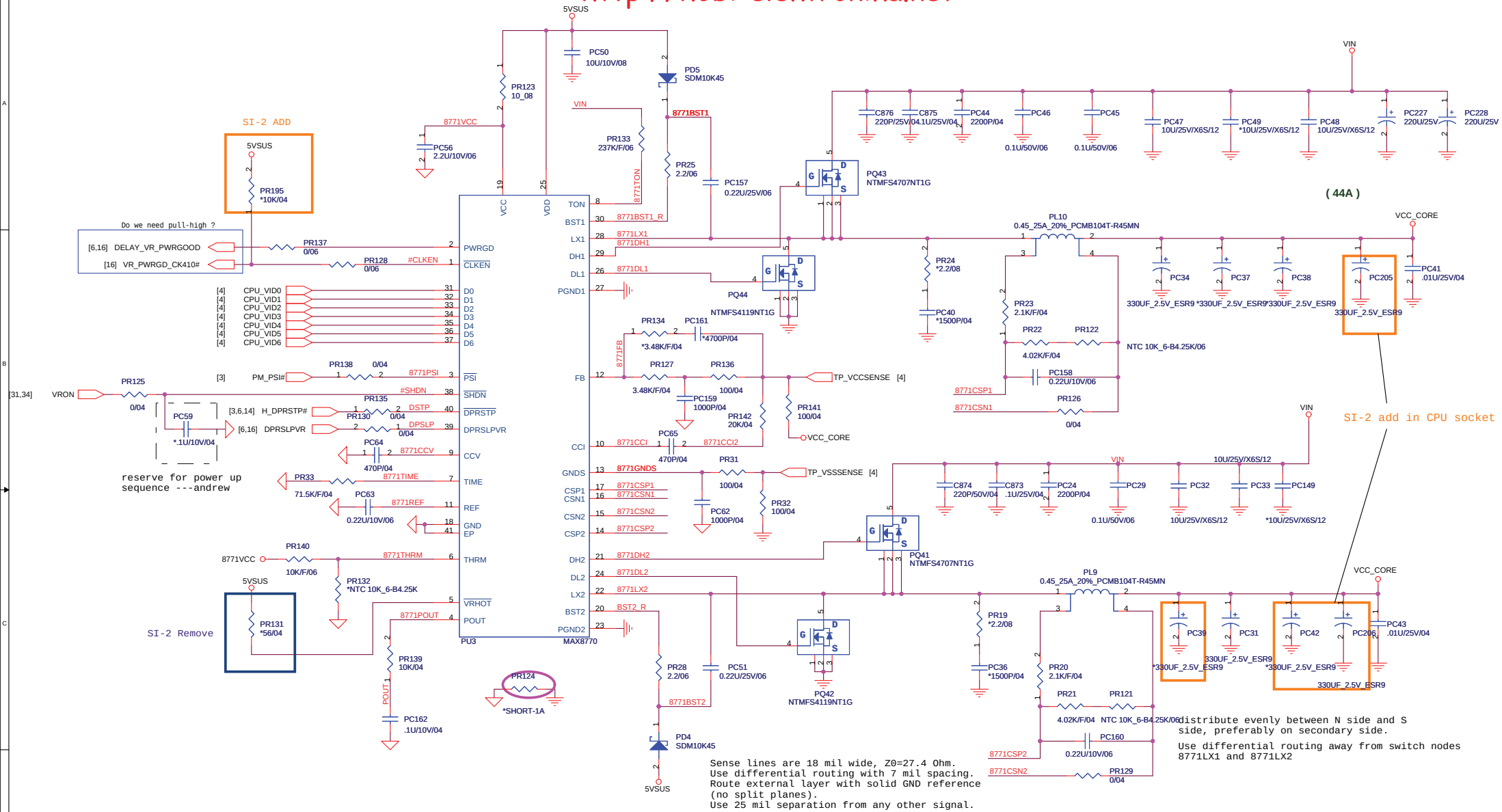
PROJECT : AT3U
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SYSTEM CHARGER(MAX8724)	2A

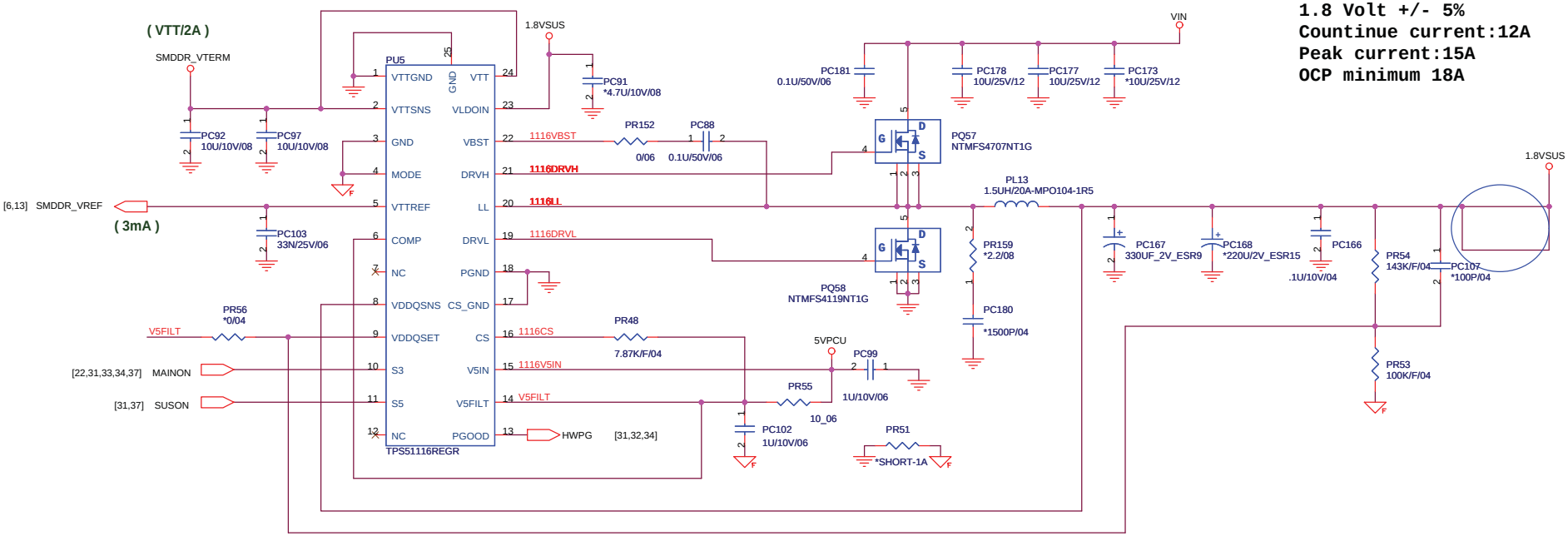
NB5/RD1/HW2

Date: Wednesday, May 02, 2007 | Sheet 33 of 37

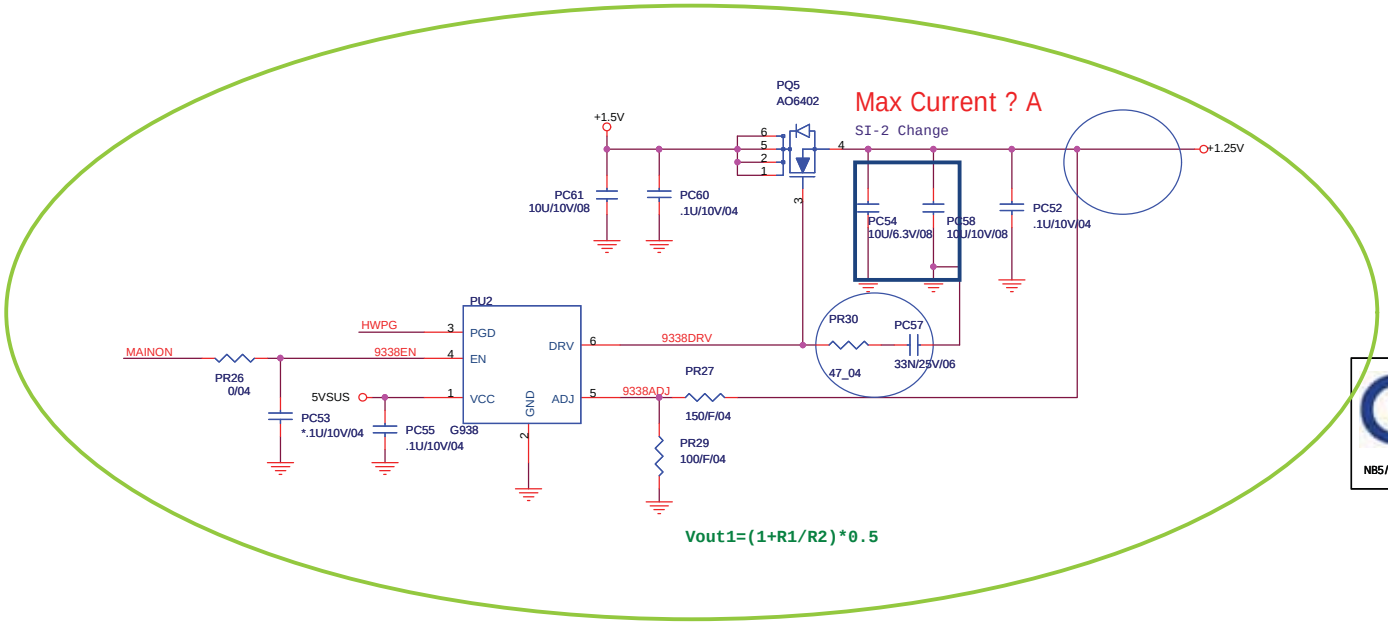




NB5/RD1/HW2	PROJECT : AT3U Quanta Computer Inc.	
Size: Custom	Document Number: CPU_CORE(MAX8771)	Rev: 2A
Date: Wednesday, May 02, 2007	Sheet 35 of 37	



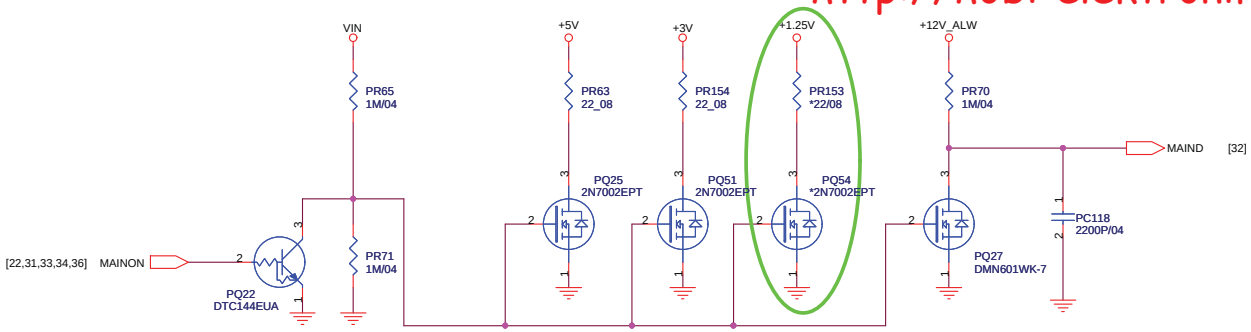
1.8 Volt +/- 5%
Countinue current:12A
Peak current:15A
OCP minimum 18A

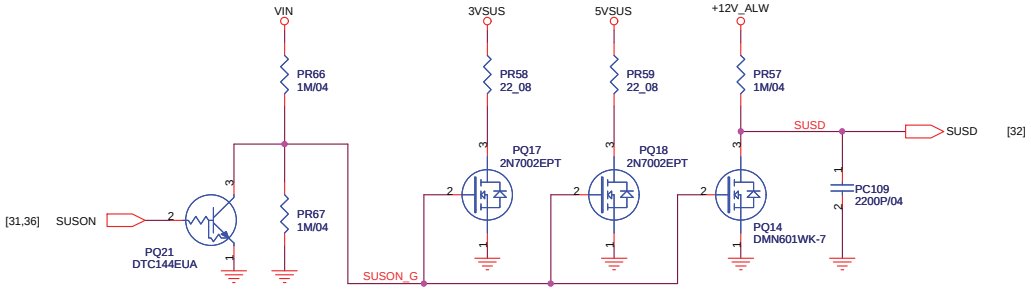


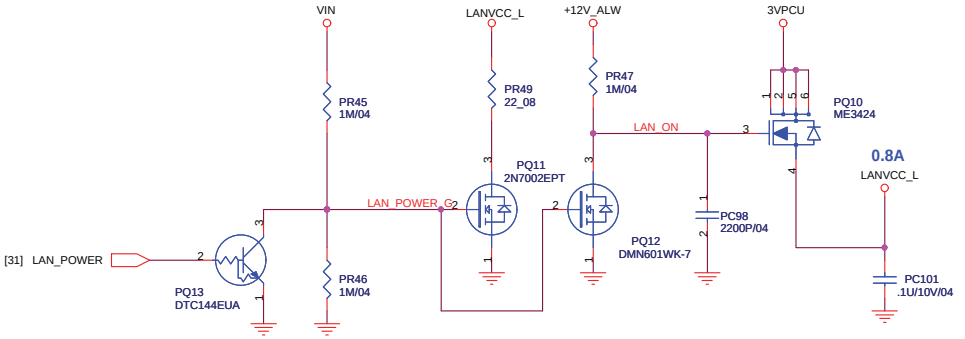
NB5/RD1/HW2

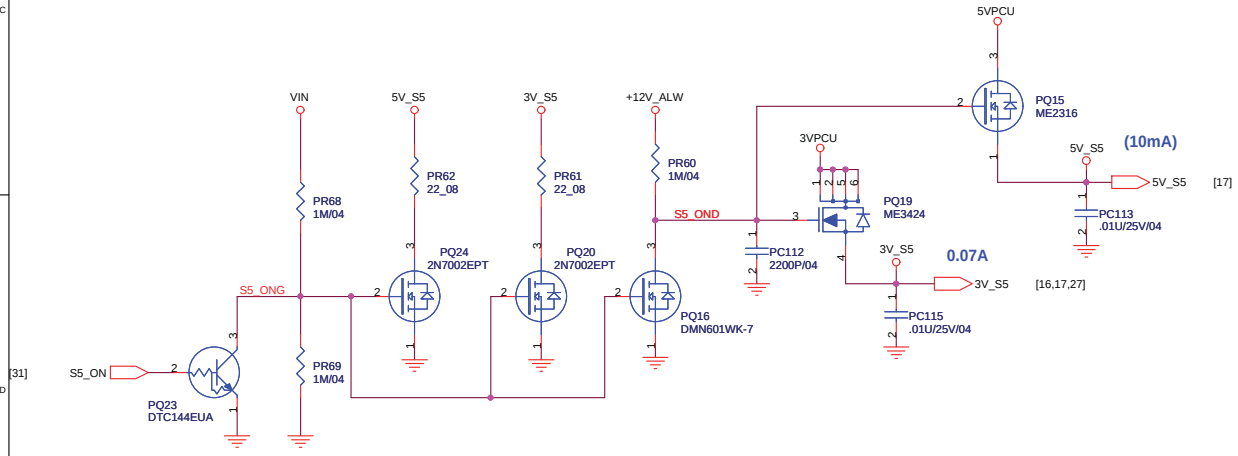
PROJECT : AT3U
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDRII 1.8VSUS/SMDDR_VTERM	2A
Date: Wednesday, May 02, 2007	Sheet 36 of 37	









NB5/RD1/HW2	**PROJECT : AT3U** Quanta Computer Inc.	
	Size: Custom — Document Number: DISCHARGE	Rev: 2A
	Date: Wednesday, May 02, 2007 — Sheet 37 of 37	