

UM7 UMA SYSTEM DIAGRAM

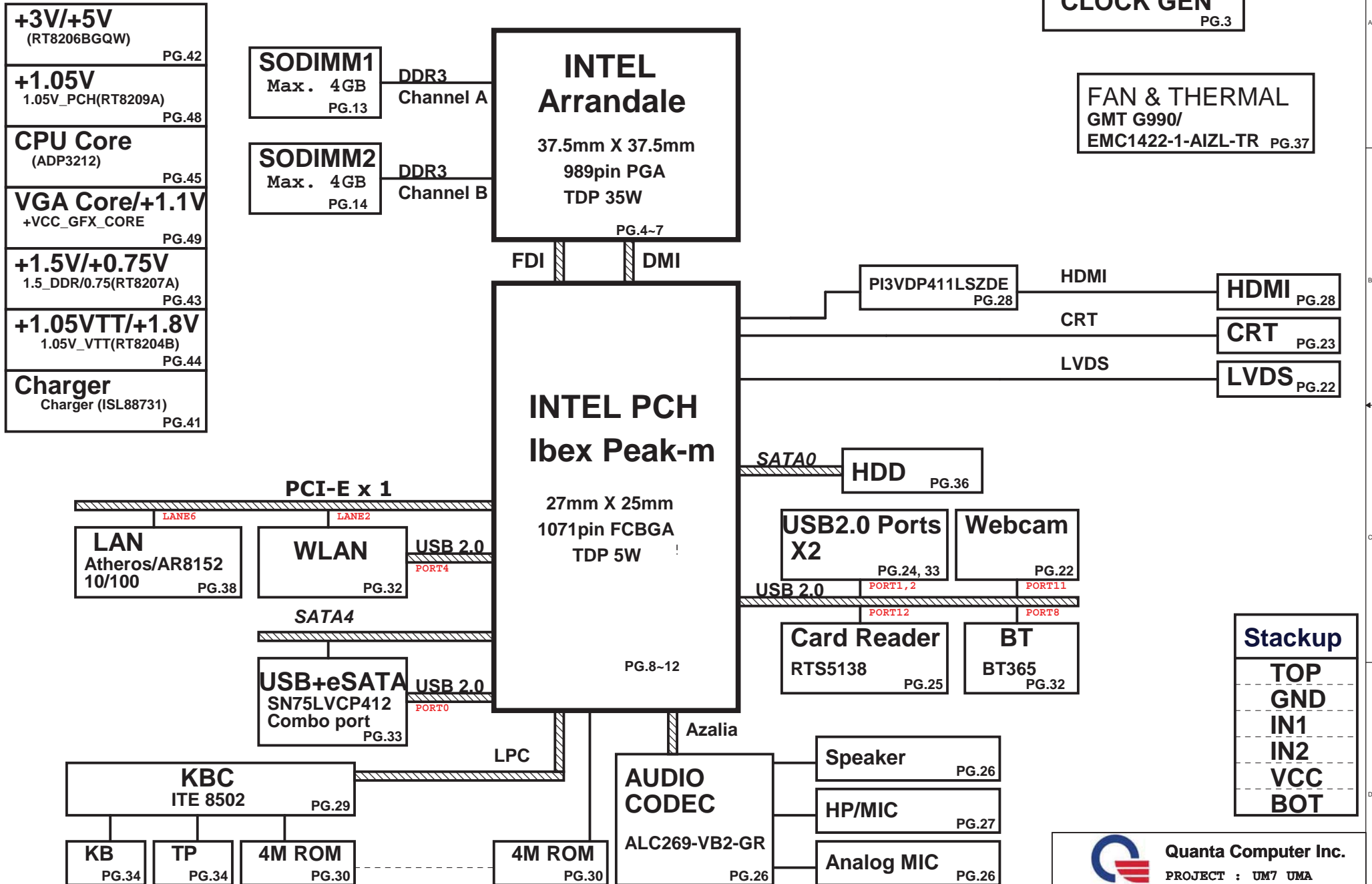



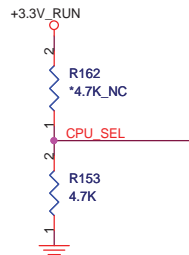
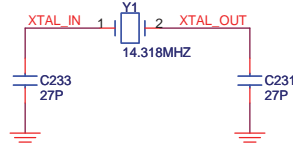
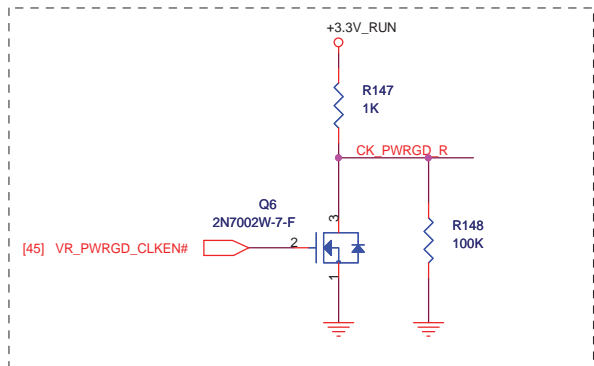
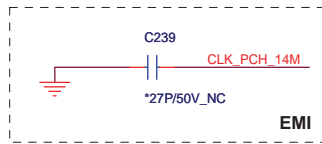
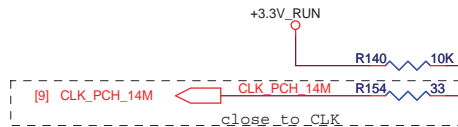
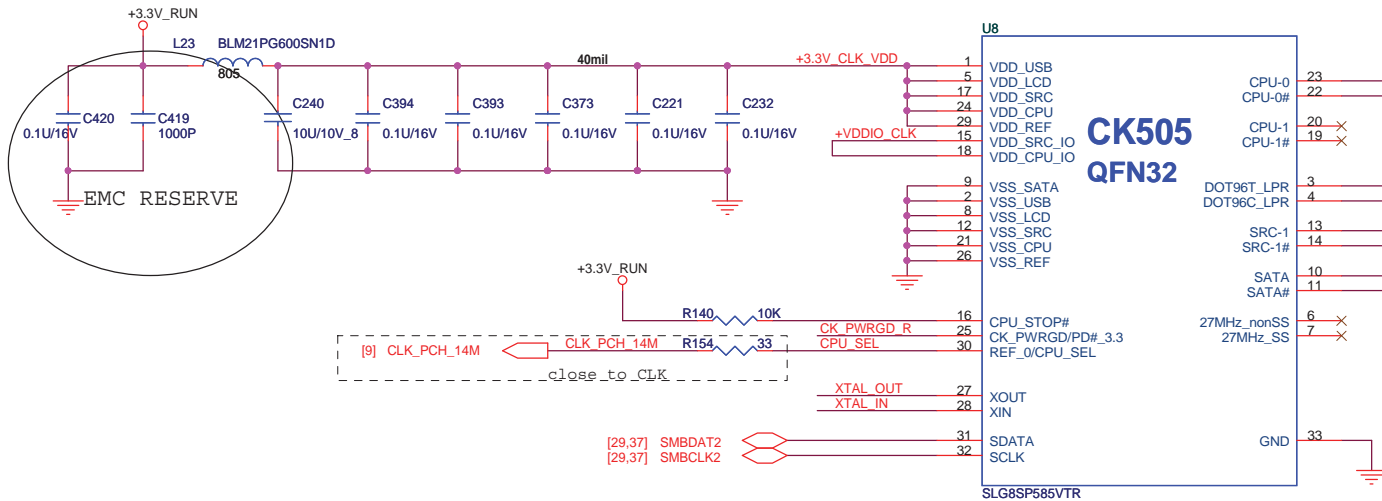
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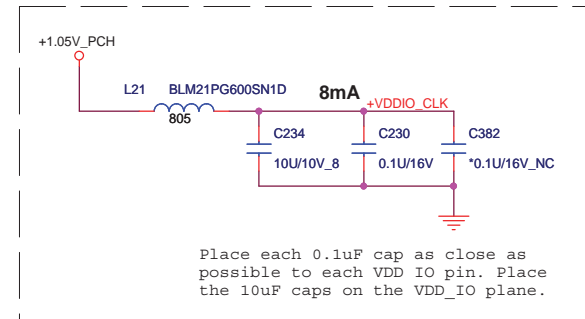
Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	23,42,43,44,45,46,49,50	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	09,12,30,31	RTC		S0~S5
+5V_ALW	+5V	37,43,44,47,48	LARGE POWER	ALW_ON	S0~S5
+3.3V_ALW	+3.3V	30,31,37,42,43,45,47,48	8051 POWER	3.3V_ALW_ON	S0~S5
+5V_SUS	+5V	12,25,34,37,43,44,45,46,47,49,50	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	03,08,09,10,11,12,23,35,37,39,41,46,47,50	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.5V	04,06,14,15,44,47	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	14,15,44	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	08,12,23,24,27,28,29,35,36,37,38,47	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,4,8,9,10,11,12,14,15,23,24,26,27,28,29,30,31,33,34,36,37,38,39,41,47	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	6,12,45	SDVO POWER	RUN_ON	
+1.05V_VTT	+1.1V	4,6,11,12,45,46	CPU POWER	RUN_ON	
+1.5V_RUN	+1.5V	12,33,47	PCH/Min Card	RUN_ON	
+1.05V_PCH	+1.05V	3,8,9,10,12,49	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	6,46	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	23	LCD Power	LCDVCC_TST_EN & ENVDD	

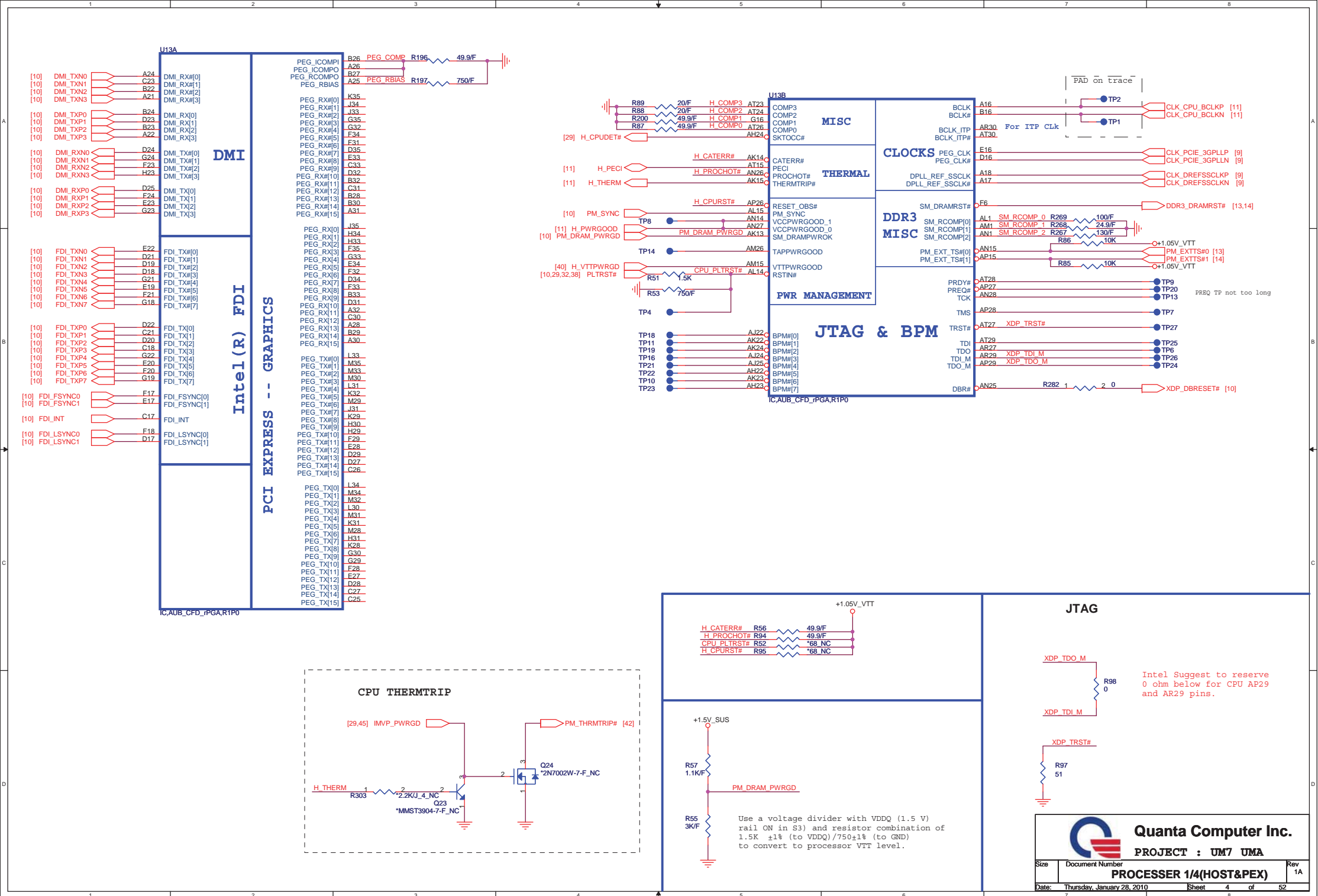
GND PLANE	PAGE	DESCRIPTION
 GND	ALL	



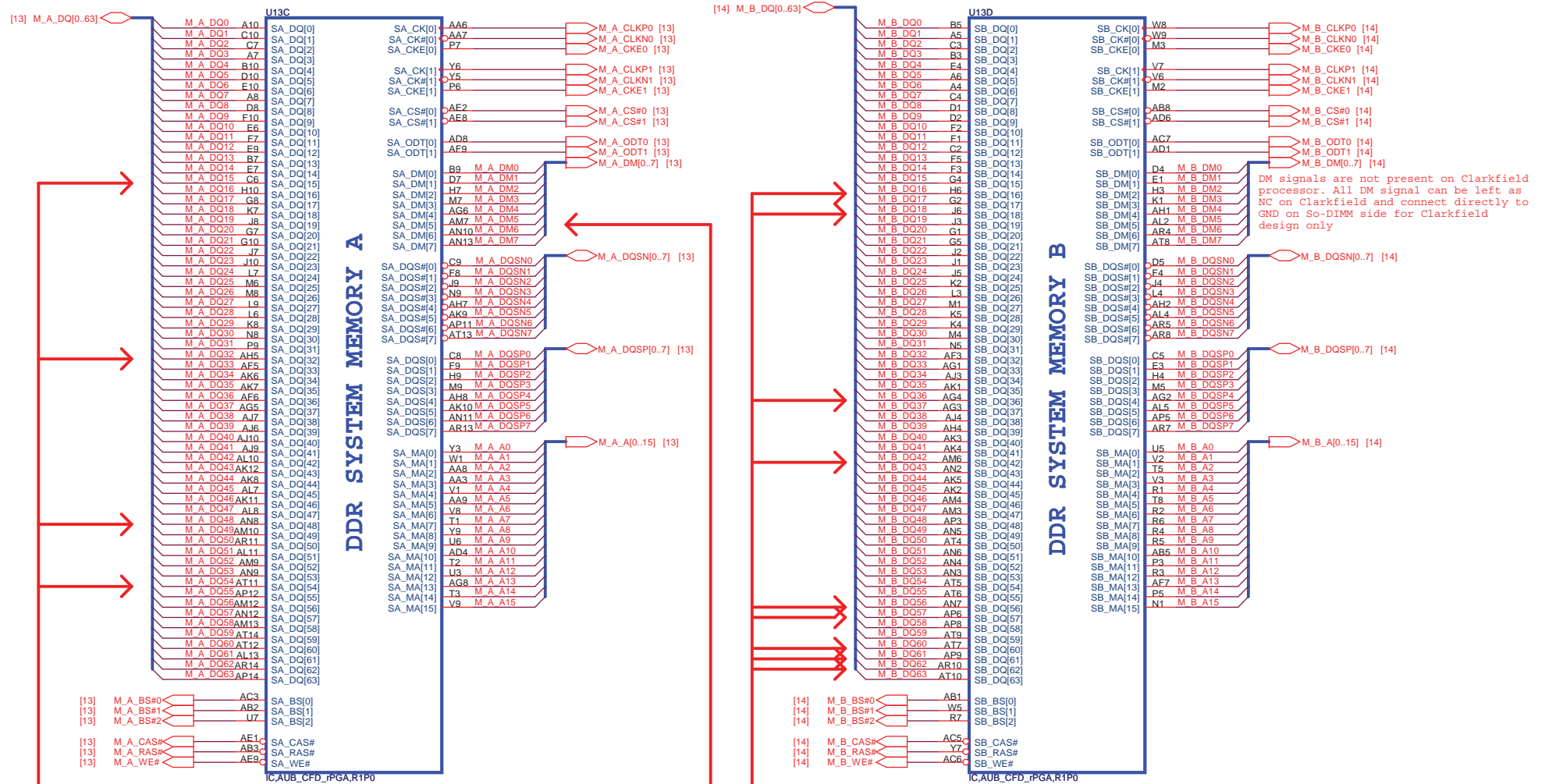
PIN 30	CPU_0	CPU_1
0 (default)	133MHz	133MHz
1 (0.7V-1.5V)	100MHz	100MHz



<http://hobi-elektronika.net>

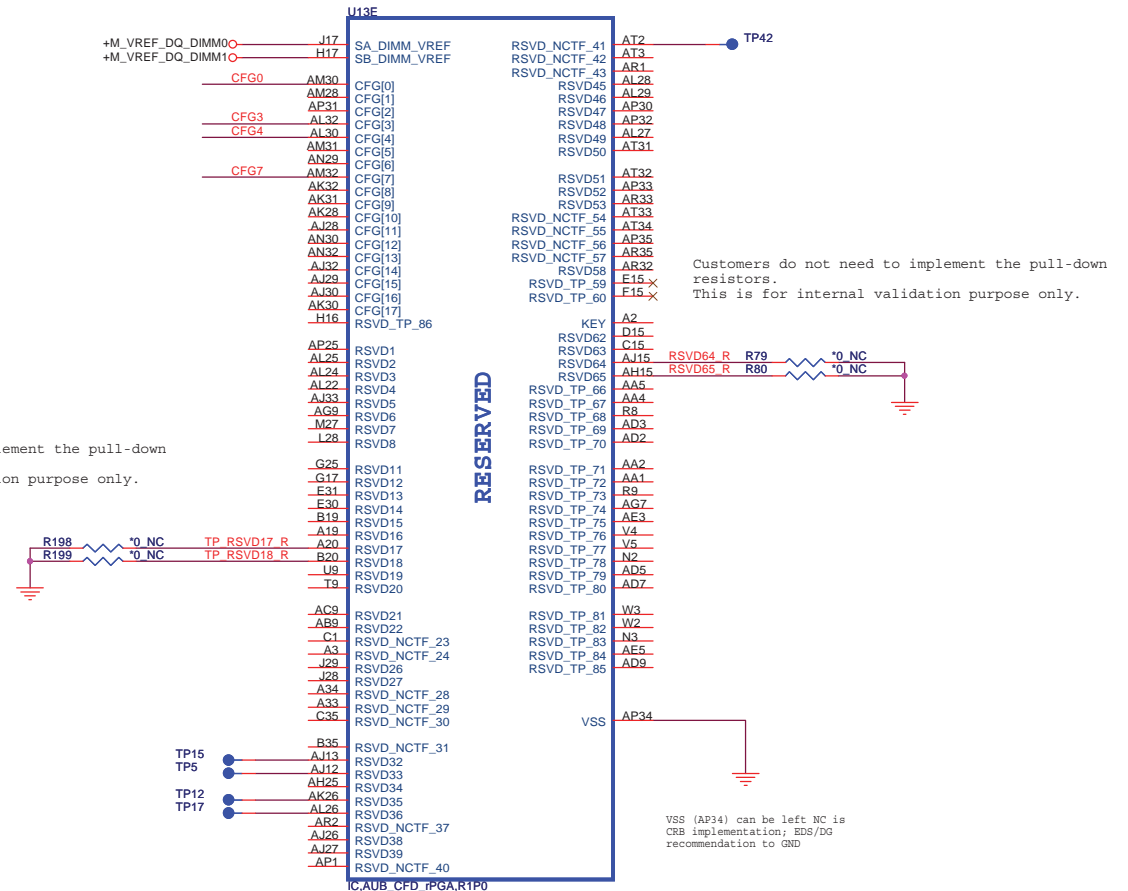
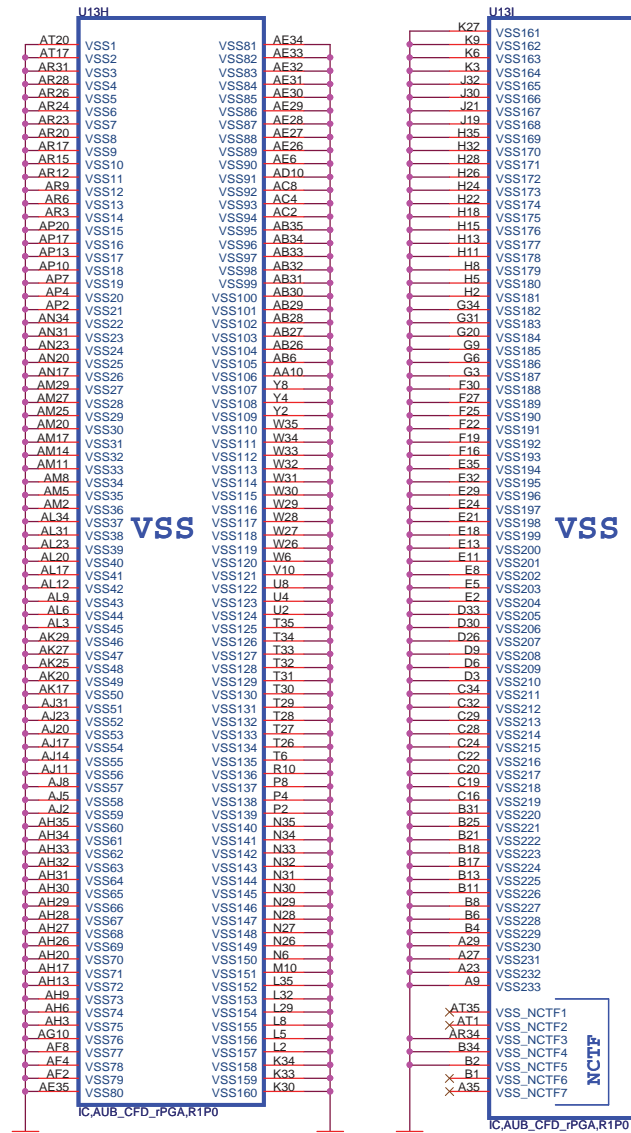


AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Arrandale PROCESSOR (GND)

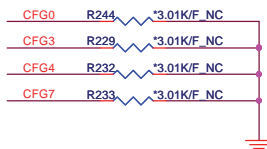
Arrandale PROCESSOR(RESERVED, CFG)



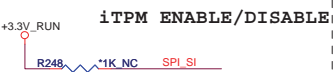
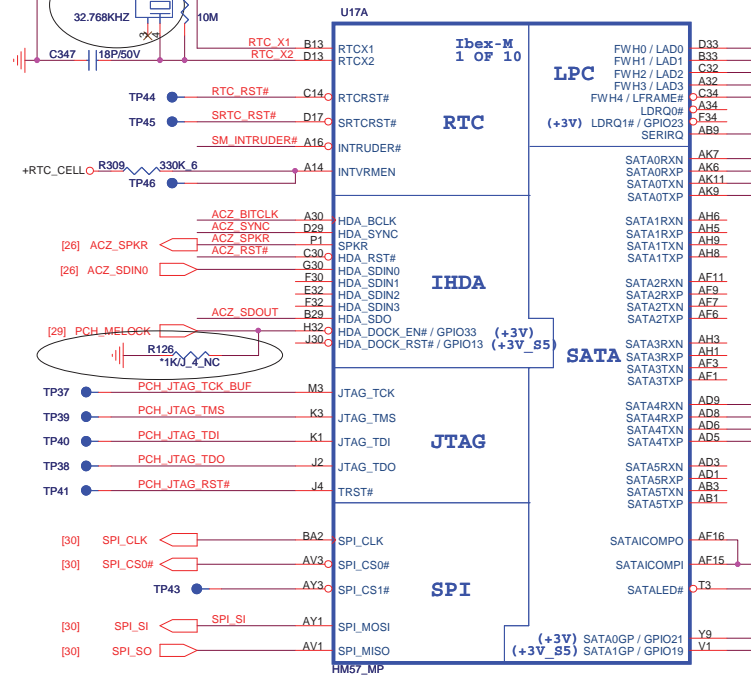
Customers do not need to implement the pull-down resistors.
This is for internal validation purpose only.

Customers do not need to implement the pull-down resistors.
This is for internal validation purpose only.

VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND

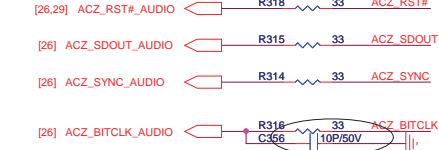


	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed



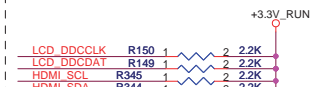
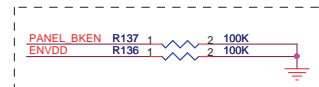
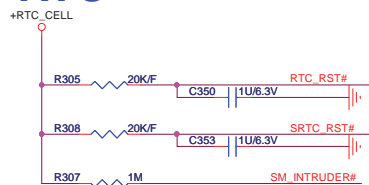
TPM Function	
Enable	Mount
Disable	NC (Default)

For AUDIO



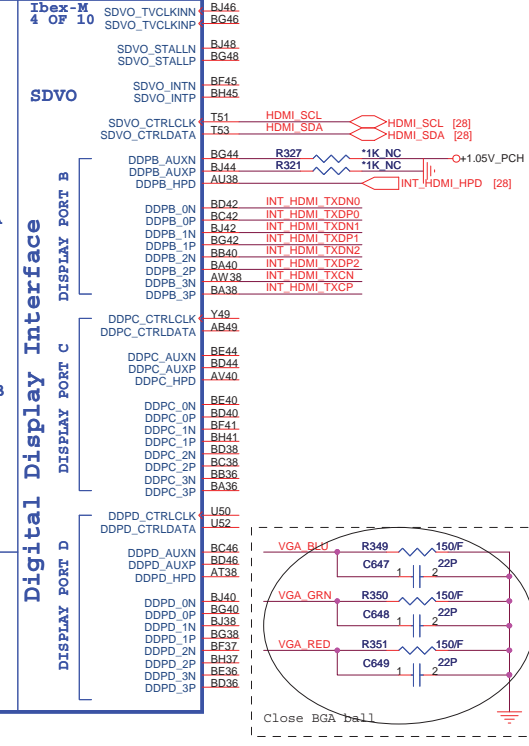
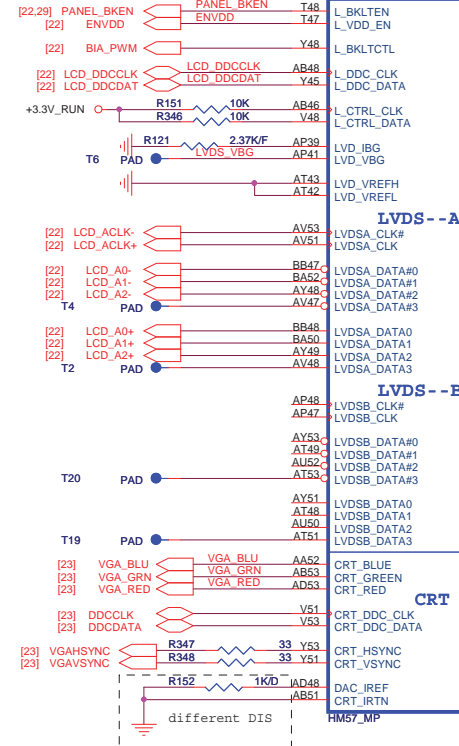
No Reboot strap.

SPKR	Low = Default. High = No Reboot.
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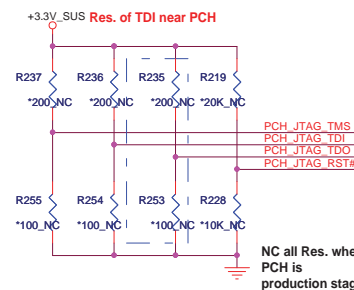


IBEX PEAK-M (LVDS,DDI)

U17D



Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.



NC all Res. when PCH is production stage.	Res. of TDO PCH ES1 stage : NC PCH ES2 stage : pop
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For UMA HDMI Function

INT_HDMI_TXD0N0	C334	0.1U/16V	INT_HDMI_TXD0N2_C	[28]
INT_HDMI_TXDP0	C337	0.1U/16V	INT_HDMI_TXDP2_C	[28]
INT_HDMI_TXD1N1	C329	0.1U/16V	INT_HDMI_TXD1N1_C	[28]
INT_HDMI_TXDP1	C331	0.1U/16V	INT_HDMI_TXDP1_C	[28]
INT_HDMI_TXD2N2	C324	0.1U/16V	INT_HDMI_TXD0N0_C	[28]
INT_HDMI_TXDP2	C327	0.1U/16V	INT_HDMI_TXDP0_C	[28]
INT_HDMI_TXCN	C320	0.1U/16V	INT_HDMI_TXCN_C	[28]
INT_HDMI_TXCP	C323	0.1U/16V	INT_HDMI_TXCP_C	[28]

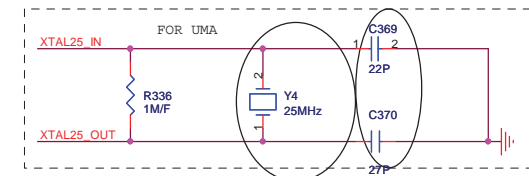


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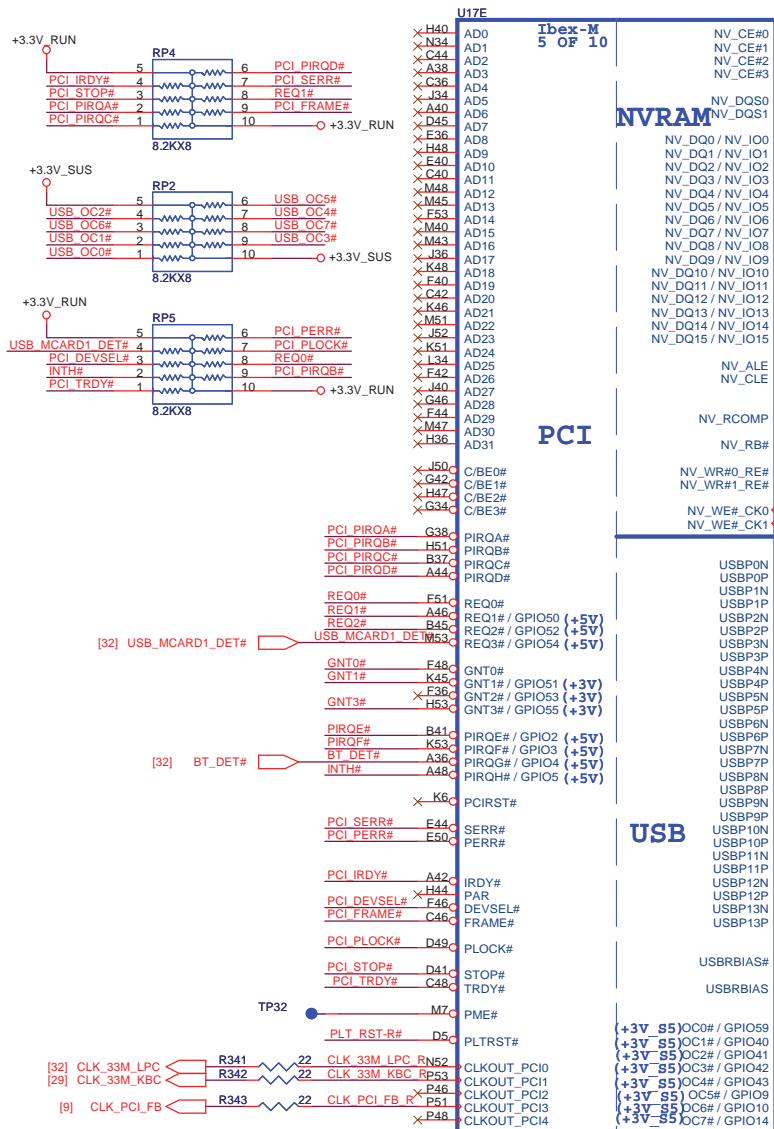
PROJECT : UM7 UMA

Size	Document Number	Rev
	PCH 1/5 (SATA,HDA,LPC)	1.
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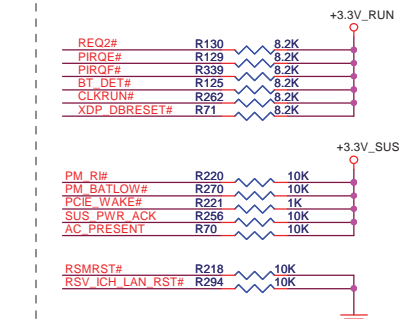
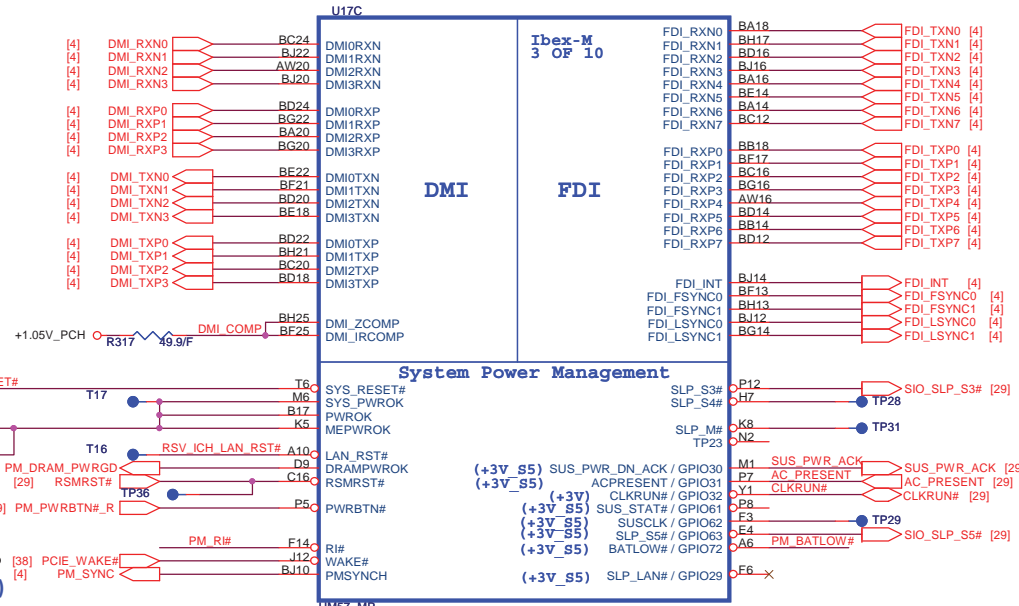
A17	B5S	VSS159	VSS259	H49
B11	B5S	VSS160	VSS260	H51
B15	B5S	VSS161	VSS261	J24
B19	B5S	VSS162	VSS262	K11
B23	B5S	VSS163	VSS263	K43
B31	B5S	VSS163	VSS263	K47
B35	B5S	VSS164	VSS264	K7
B39	B5S	VSS165	VSS265	K14
B43	B5S	VSS166	VSS266	L17
B47	B5S	VSS167	VSS267	L18
B51	B5S	VSS168	VSS268	L22
B55	B5S	VSS169	VSS269	L23
BC12	B5S	VSS170	VSS270	L36
BB16	B5S	VSS171	VSS271	L40
BB20	B5S	VSS172	VSS272	L52
BB24	B5S	VSS174	VSS274	M12
BB30	B5S	VSS175	VSS275	M16
BB38	B5S	VSS176	VSS276	M38
BB42	B5S	VSS177	VSS277	M34
BB49	B5S	VSS178	VSS278	M38
BB5	B5S	VSS179	VSS279	M46
BC10	B5S	VSS180	VSS280	M42
BC14	B5S	VSS181	VSS281	M49
BC18	B5S	VSS182	VSS282	M5
BC2	B5S	VSS183	VSS283	M6
BC22	B5S	VSS184	VSS284	N24
BC32	B5S	VSS185	VSS285	P11
BC36	B5S	VSS186	VSS286	AD15
BC40	B5S	VSS187	VSS287	P22
BC44	B5S	VSS188	VSS288	P20
BC52	B5S	VSS189	VSS289	P32
BH9	B5S	VSS190	VSS290	P34
BD48	B5S	VSS191	VSS291	P42
BD49	B5S	VSS192	VSS292	P47
BD5	B5S	VSS193	VSS293	P45
BE12	B5S	VSS194	VSS294	R2
BE16	B5S	VSS195	VSS295	S52
BE20	B5S	VSS196	VSS296	T12
BE24	B5S	VSS197	VSS297	T41
BE30	B5S	VSS198	VSS298	T46
BE34	B5S	VSS199	VSS299	T49
BE38	B5S	VSS200	VSS300	T5
BE42	B5S	VSS201	VSS301	T8
BE46	B5S	VSS202	VSS302	U30
BE48	B5S	VSS203	VSS303	U31
BE50	B5S	VSS204	VSS304	U32
BE6	B5S	VSS205	VSS305	U34
BE8	B5S	VSS206	VSS306	P38
BF3	B5S	VSS207	VSS307	V11
BF40	B5S	VSS208	VSS308	V19
BF51	B5S	VSS209	VSS309	V19
BG18	B5S	VSS210	VSS310	Y20
BG24	B5S	VSS211	VSS311	Y21
BG4	B5S	VSS212	VSS312	Y22
BG50	B5S	VSS213	VSS313	V30
BH1	B5S	VSS214	VSS314	V32
BH15	B5S	VSS215	VSS315	V34
BH19	B5S	VSS216	VSS316	V35
BH23	B5S	VSS217	VSS317	V38
BH31	B5S	VSS218	VSS318	V43
BH35	B5S	VSS219	VSS319	V45
BH39	B5S	VSS220	VSS320	V46
BH43	B5S	VSS221	VSS321	V47
BH47	B5S	VSS222	VSS322	V49
BH7	B5S	VSS223	VSS323	V5
C12	B5S	VSS224	VSS324	V7
C50	B5S	VSS225	VSS325	V8
D51	B5S	VSS226	VSS326	V8
E12	B5S	VSS227	VSS327	W52
E16	B5S	VSS228	VSS328	Y11
E20	B5S	VSS229	VSS329	Y12
E24	B5S	VSS230	VSS330	Y15
E30	B5S	VSS231	VSS331	Y19
E34	B5S	VSS232	VSS332	Y23
E38	B5S	VSS233	VSS333	Y28
E42	B5S	VSS234	VSS334	Y30
E46	B5S	VSS235	VSS335	Y31
E48	B5S	VSS236	VSS336	Y32
E52	B5S	VSS237	VSS337	Y33
E6	B5S	VSS238	VSS338	Y38
E8	B5S	VSS239	VSS339	Y43
F49	B5S	VSS240	VSS340	Y46
F5	B5S	VSS241	VSS341	Y49
G10	B5S	VSS242	VSS342	Y51
G14	B5S	VSS243	VSS343	Y8
G18	B5S	VSS244	VSS344	Y8
G2	B5S	VSS245	VSS345	P24
G22	B5S	VSS246	VSS346	T43
G32	B5S	VSS247	VSS347	AD51
G36	B5S	VSS248	VSS348	AT8
G40	B5S	VSS249	VSS349	AD47
G44	B5S	VSS250	VSS350	Y47
G52	B5S	VSS251	VSS351	AT12
AF39	B5S	VSS252	VSS352	AT

[illegible]

IBEX PEAK-M (PCI,USB,NVRAM)



IBEX PEAK-M (DMI,FDI,GPIO)



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PROJECT : UM7 UMA

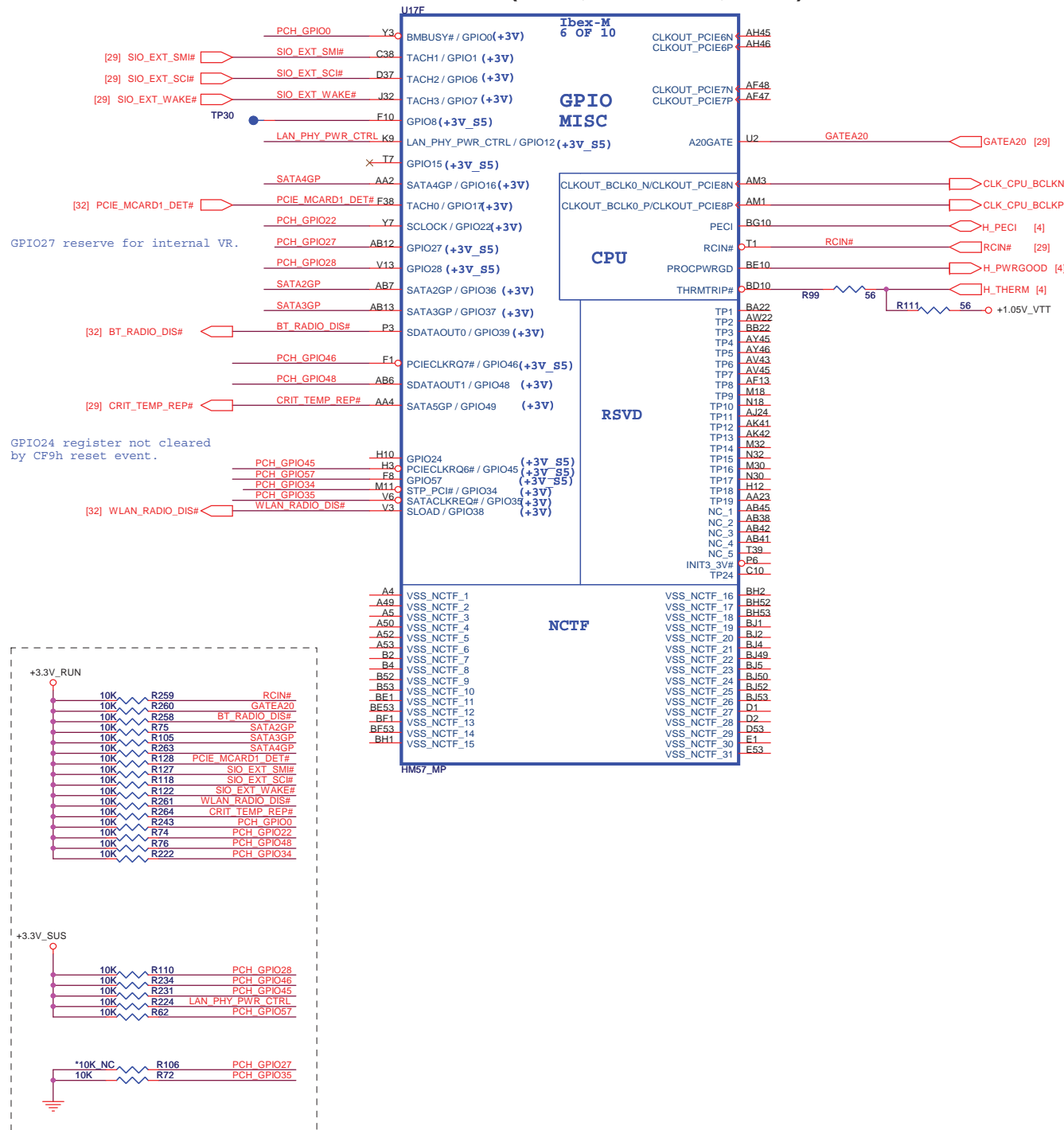
PCH 3/5 (PCI,ONFI,USB,DMI)

Rev 1A

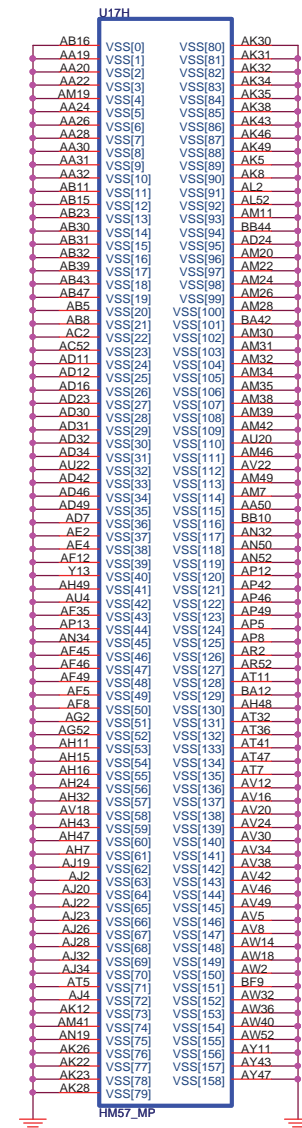
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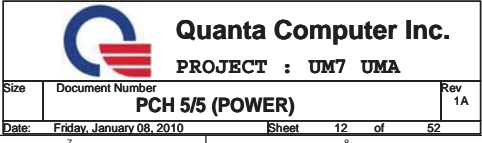
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IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



IBEX PEAK-M (GND)





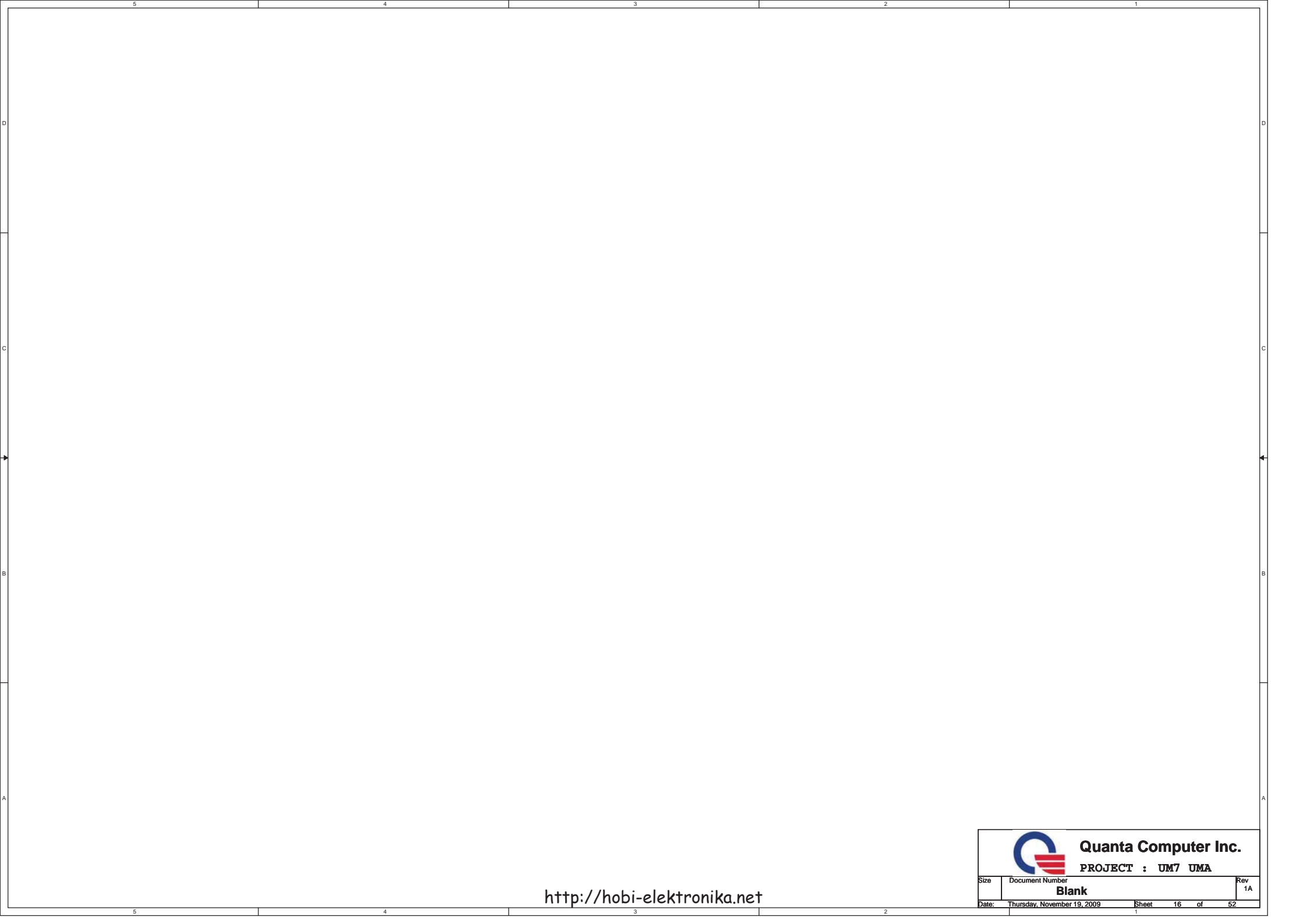
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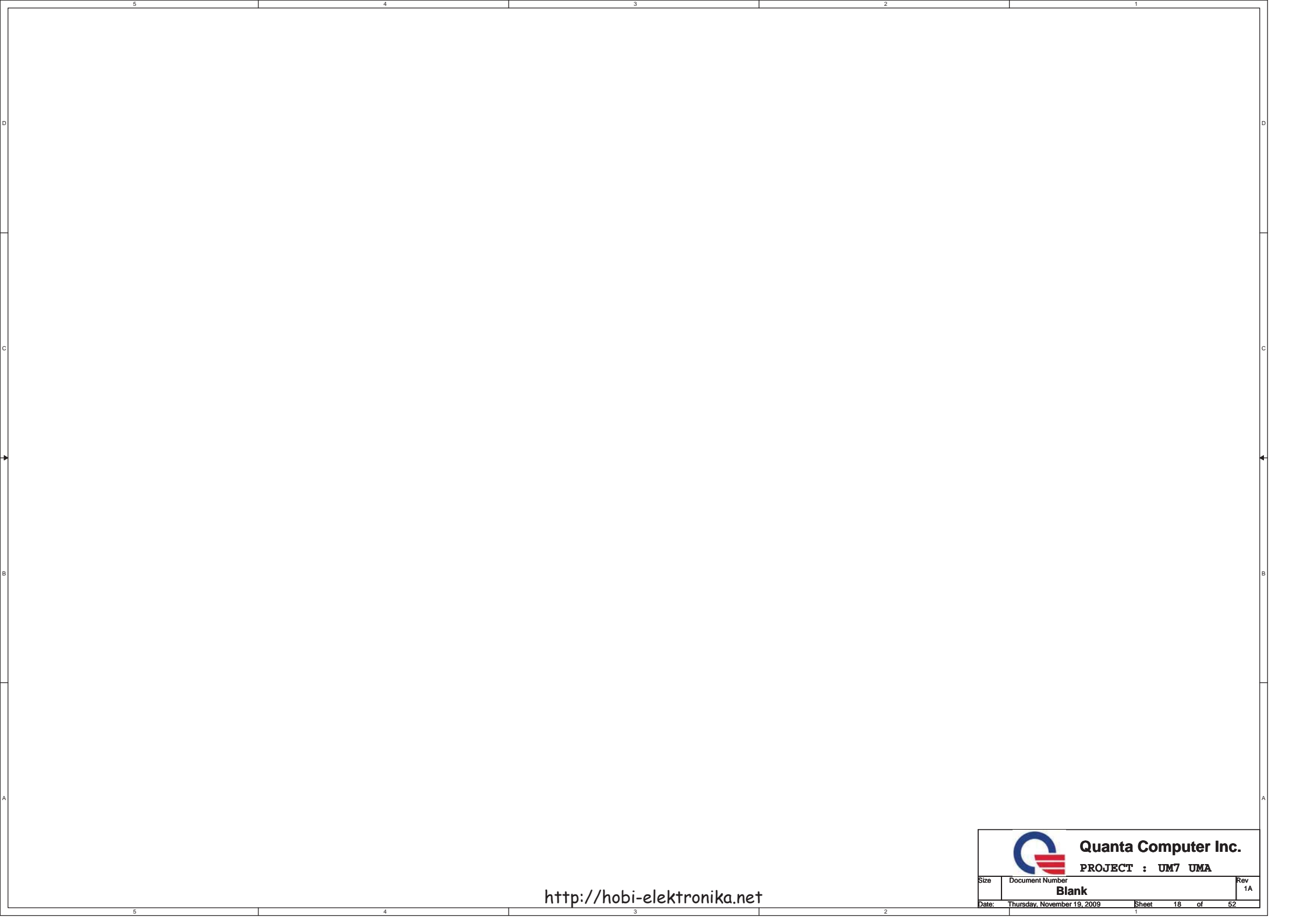
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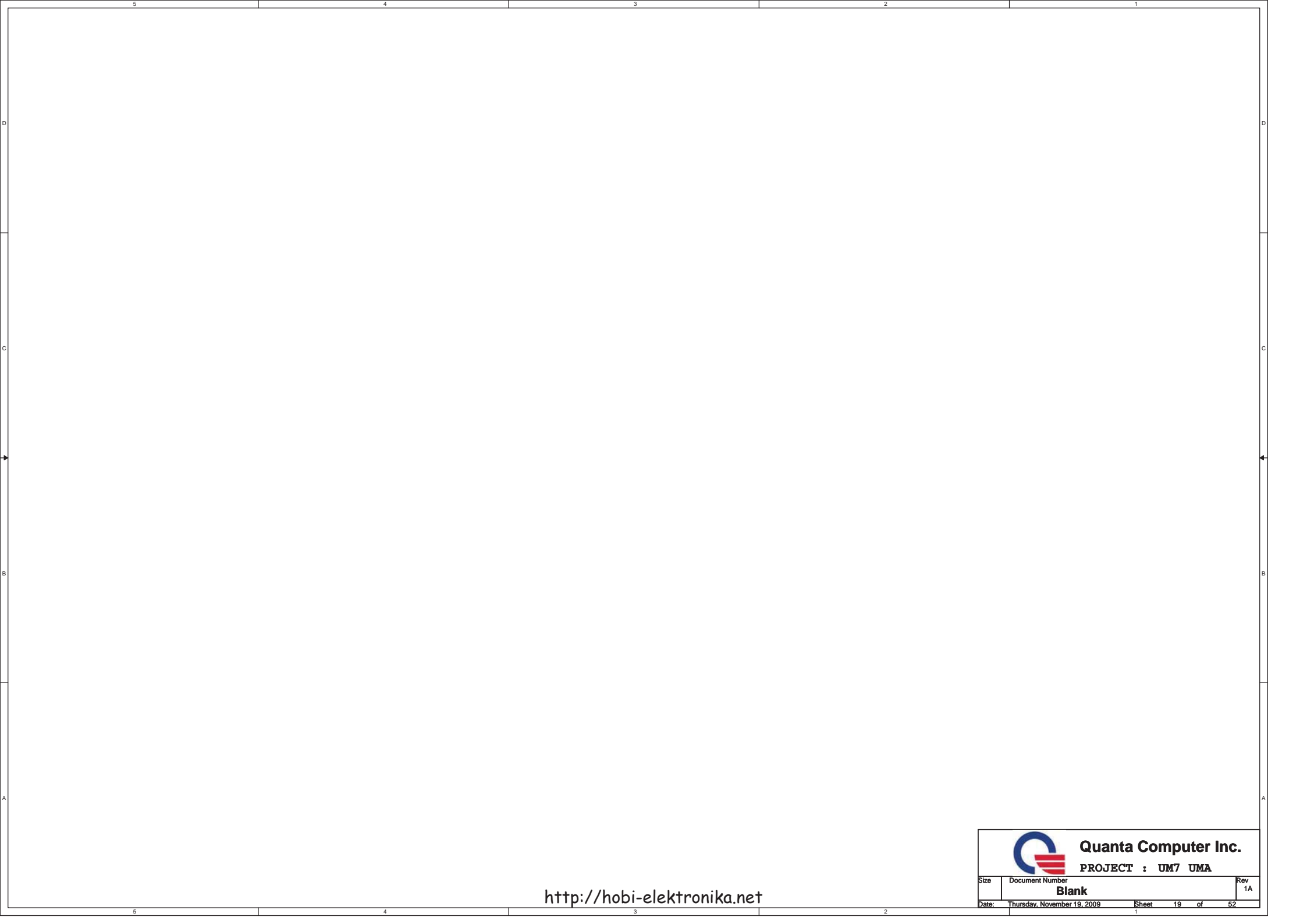
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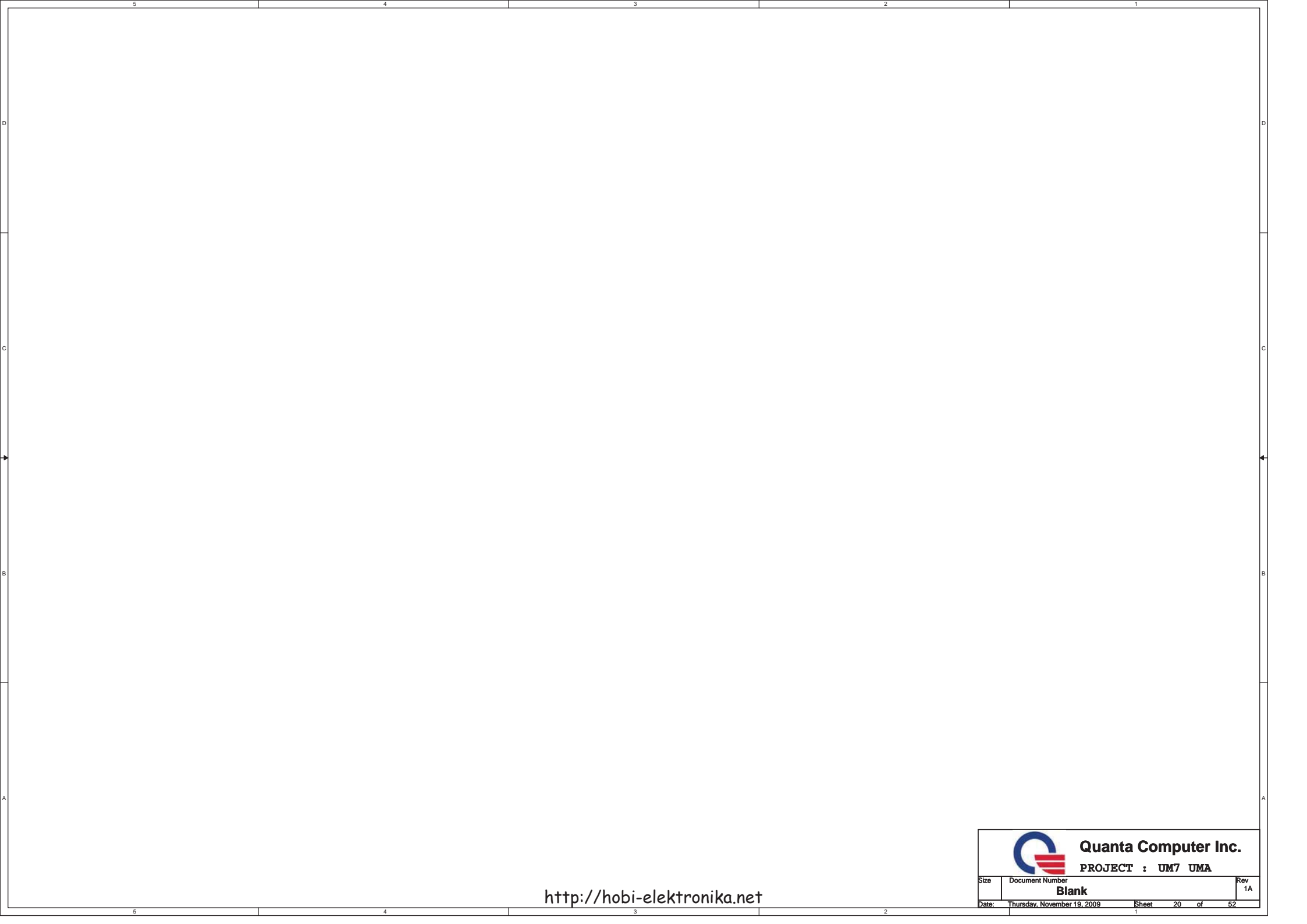
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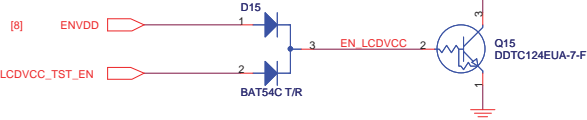




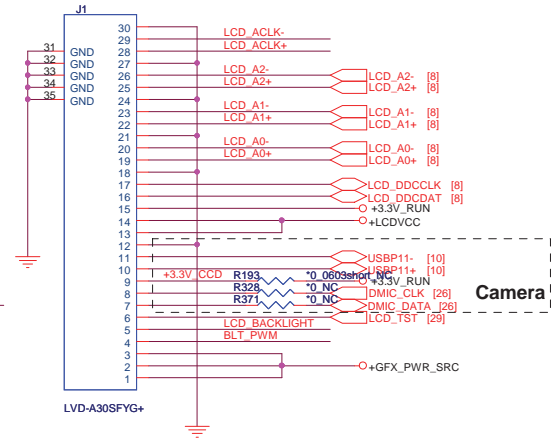
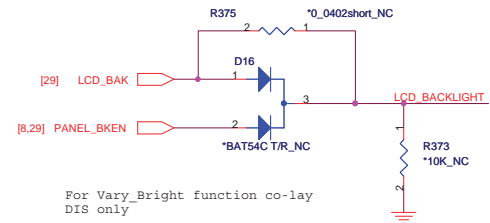
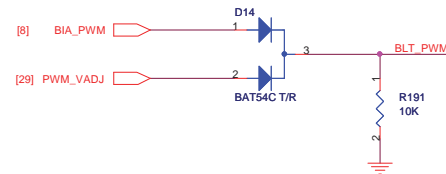
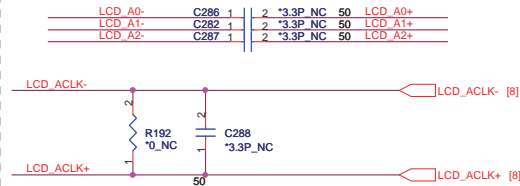


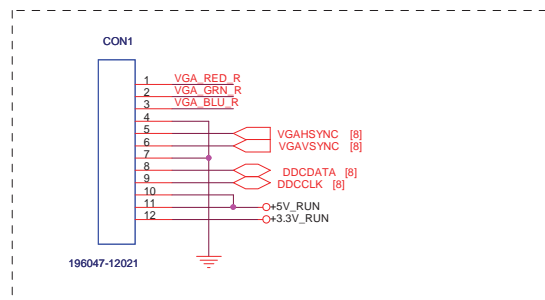
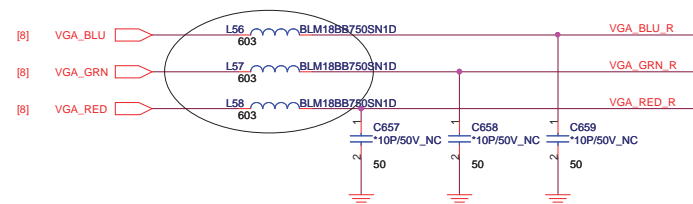


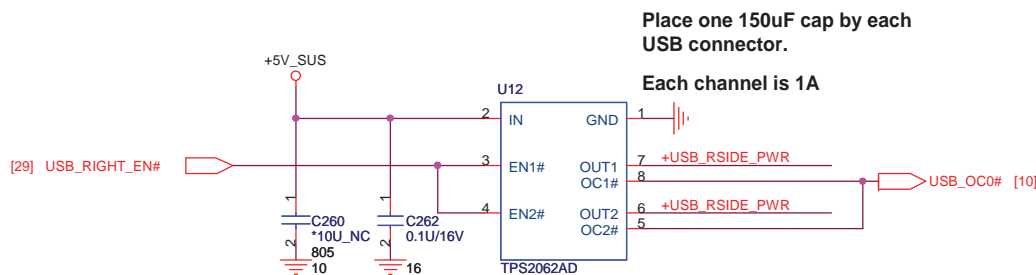
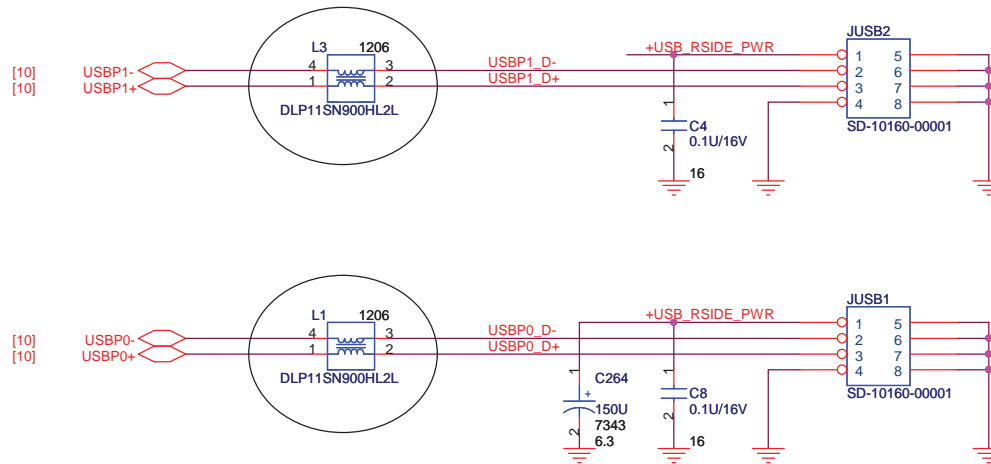
Support the new imbedded diagnostics.



Shunt capacitors on LVDS for improving WWAN.





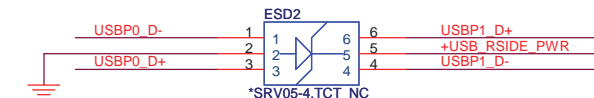


Place one 150uF cap by each USB connector.

Each channel is 1A

Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

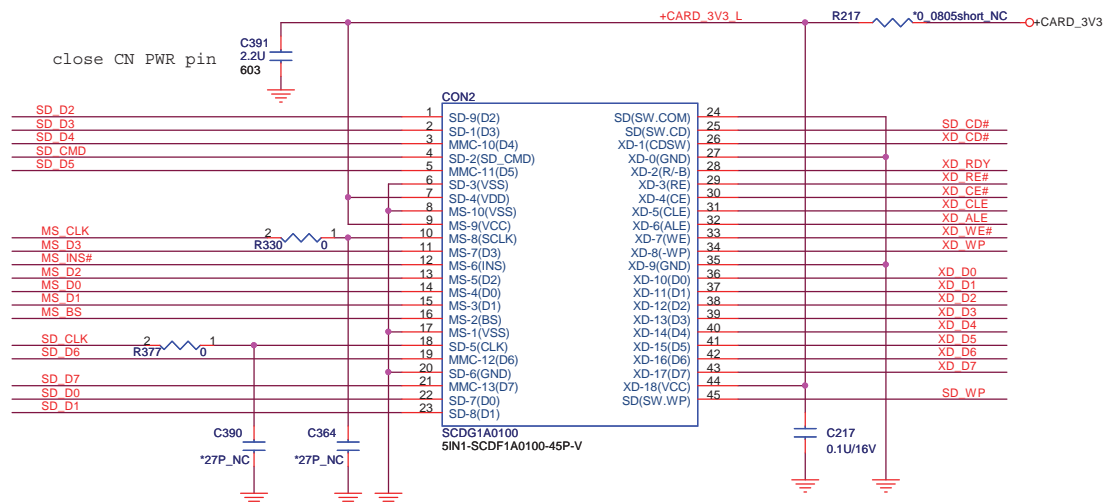
Place ESD diodes as close as USB connector.



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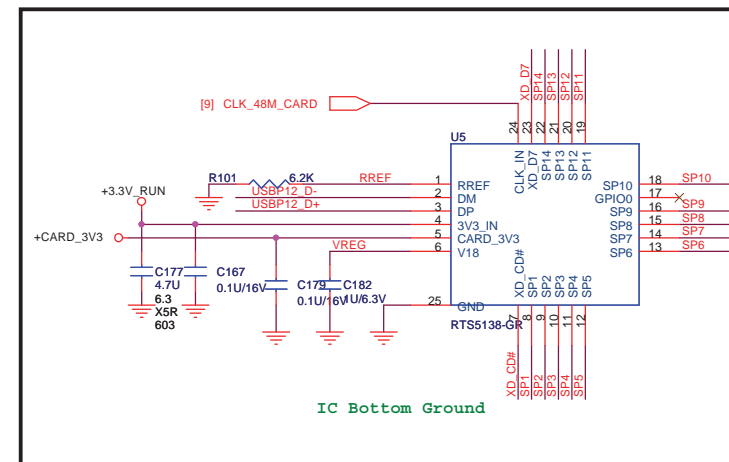
PROJECT : UM7 UMA

Size	Document Number	Rev
	Right USB	1A
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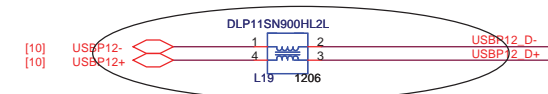


SP1	XD RDY	SD WP	MS CLK
SP2	XD RE#		MS INS#
SP3	XD CE#	SD D1	
SP4	XD CLE	SD D0	MS D7
SP5	XD ALE	SD D7	MS D3
SP6	XD WE#	SD CD#	
SP7	XD WP	SD D6	MS D6
SP8	XD D0	SD CLK	MS D2
SP9	XD D1	SD D5	MS D0
SP10	XD D2	SD CMD	
SP11	XD D3	SD D4	MS D4
SP12	XD D4	SD D3	MS D1
SP13	XD D5	SD D2	MS D5
SP14	XD D6		MS BS

Share Pin



RTS5138-QFN24

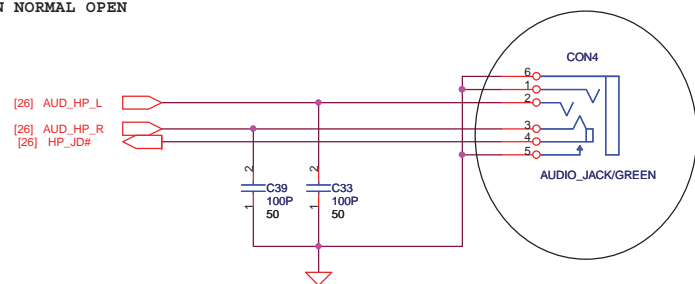


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Size	Document Number	Rev
	Card Reader(RST5138)	1A
Date:	Tuesday, February 02, 2010	Sheet 25 of 52

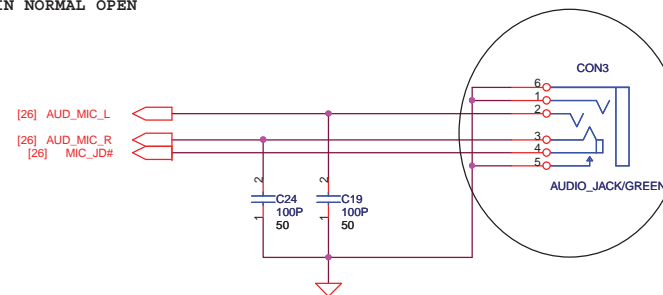
HP JACKN

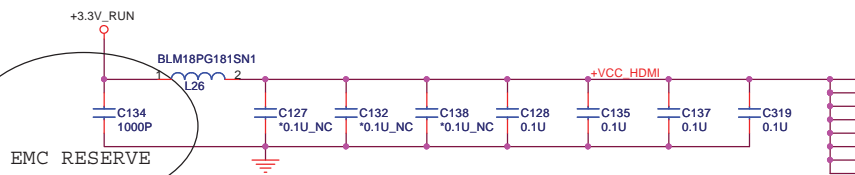
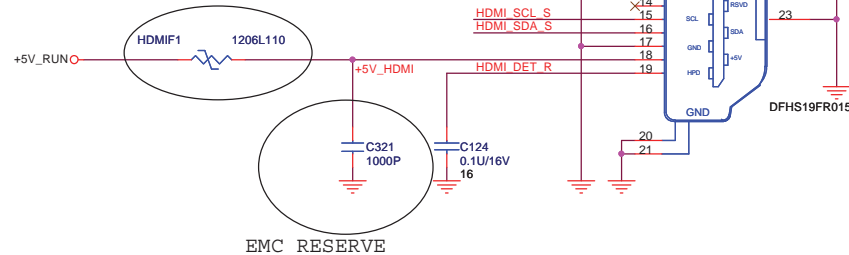
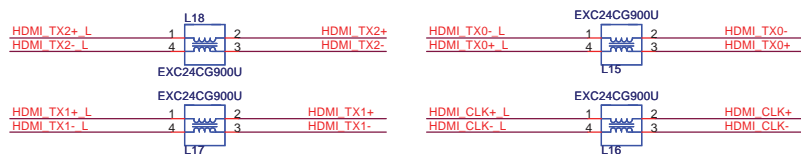
SUYIN NORMAL OPEN



MIC JACK

SUYIN NORMAL OPEN

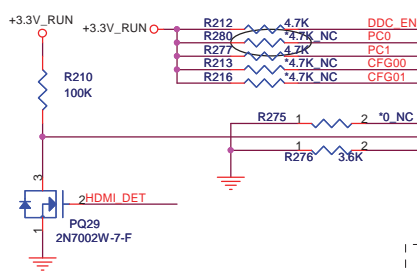
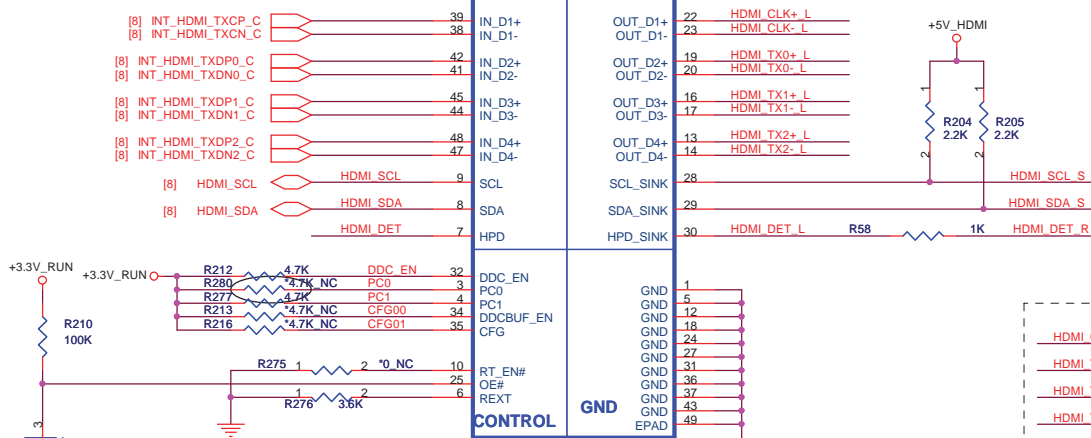
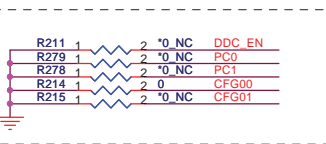




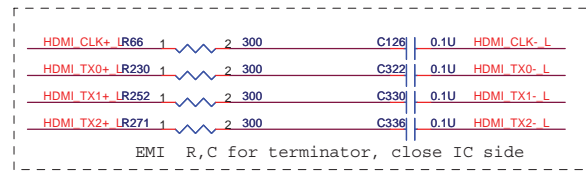
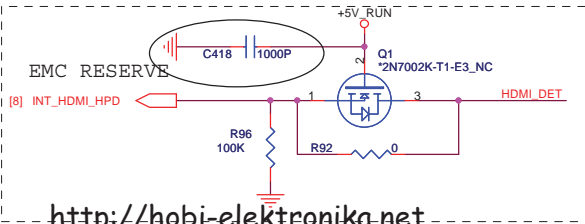
EQUALIZATION SETTING
 PC1:PC0=0:0 8dB
 PC1:PC0=0:1 4dB Recommended
 PC1:PC0=1:0 12dB
 PC1:PC0=1:1 0dB

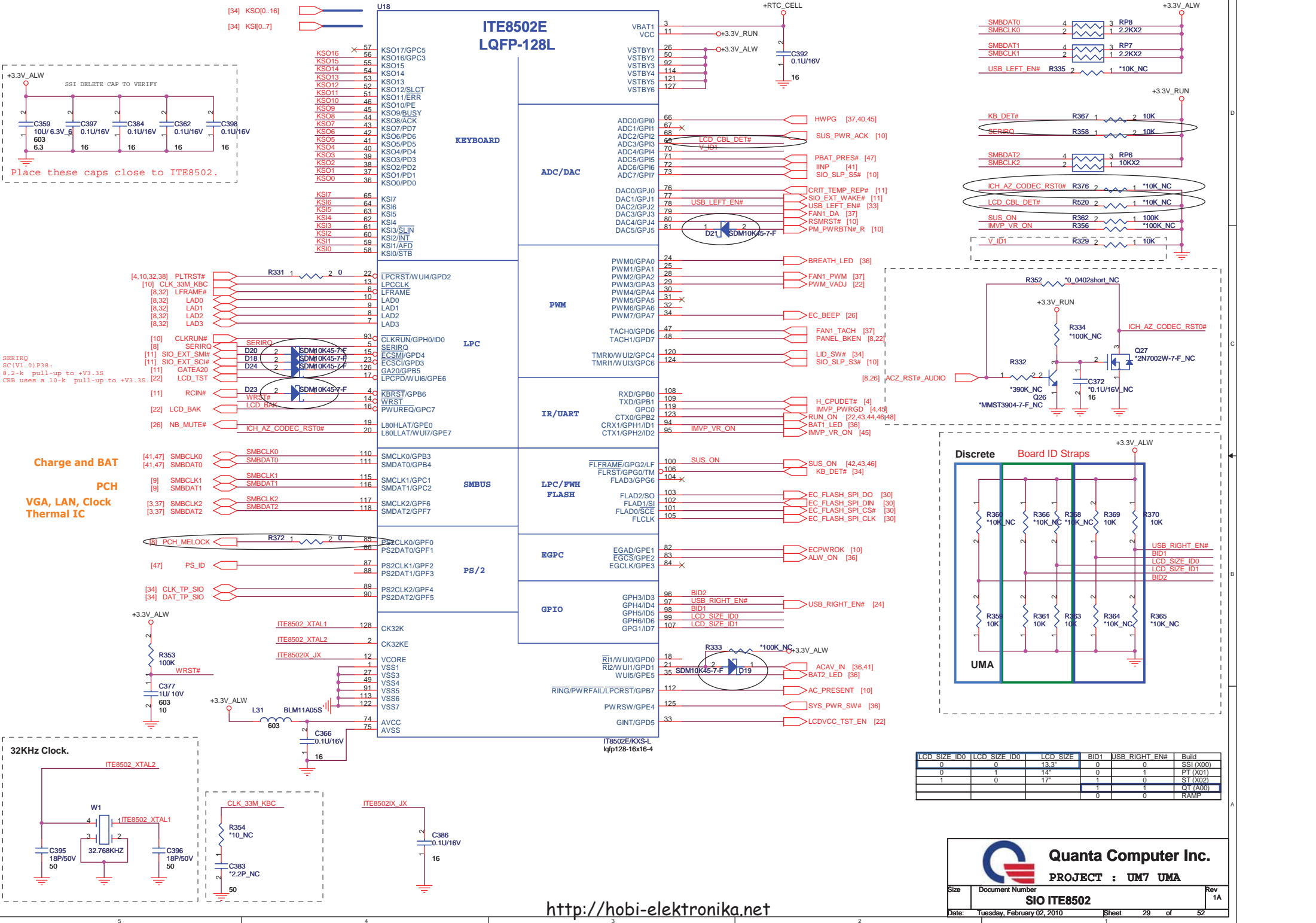
SCL/SDA Low-level input/output Voltage
 CFG01:CFG00=0:0 VIL:<0.4V VOL:0.6V (Default)
 CGF01:CGF00=0:1 VIL:<0.36V VOL:0.55V
 CGF01:CGF00=1:0 VIL:<0.44V VOL:0.65V
 CGF01:CGF00=1:1 VIL:<0.36V VOL:0.6V

HDMI_PWR_CTRL
 0 is Enable
 1 is Disable



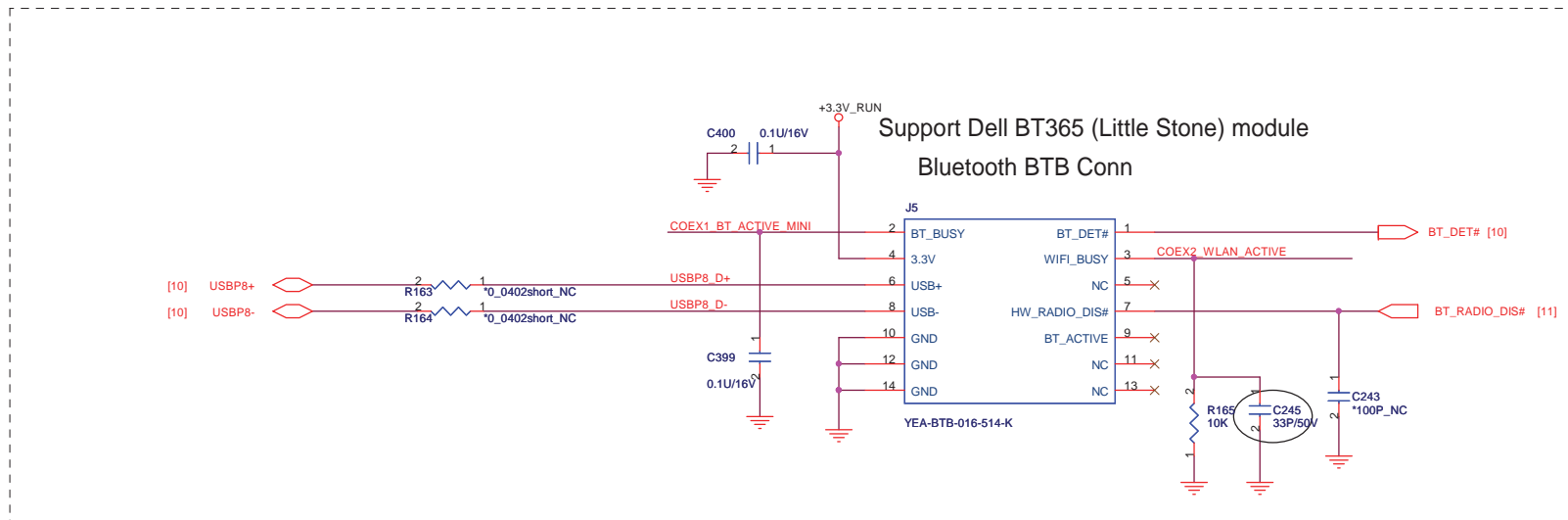
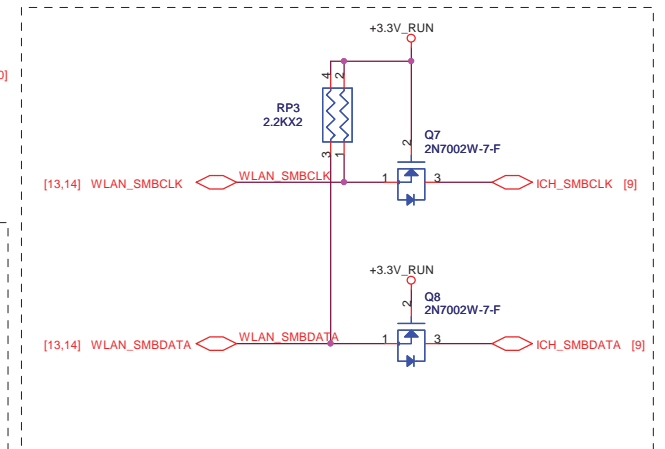
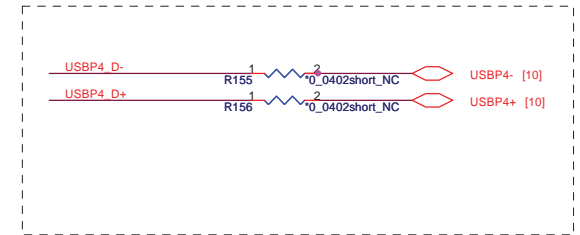
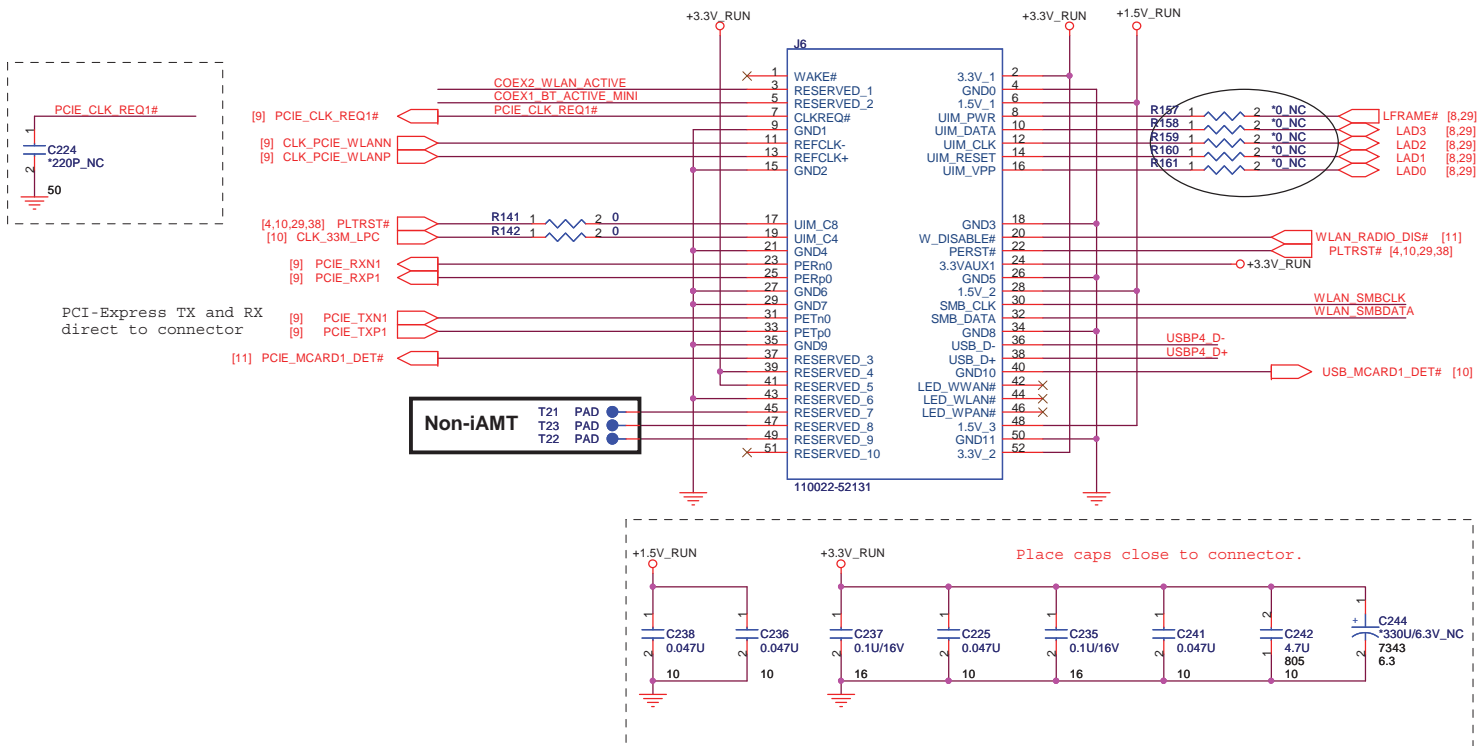
SN75DP139RGZR



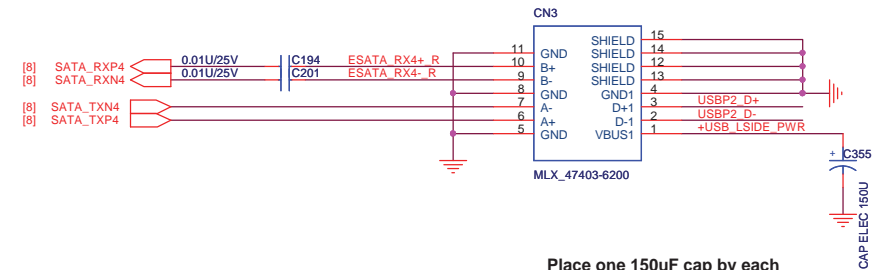




MiniCard WLAN connector

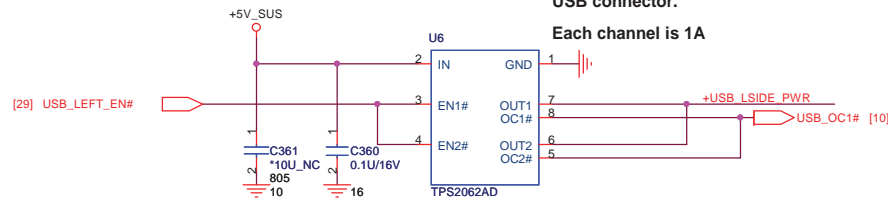


USB and eSATA Conn.

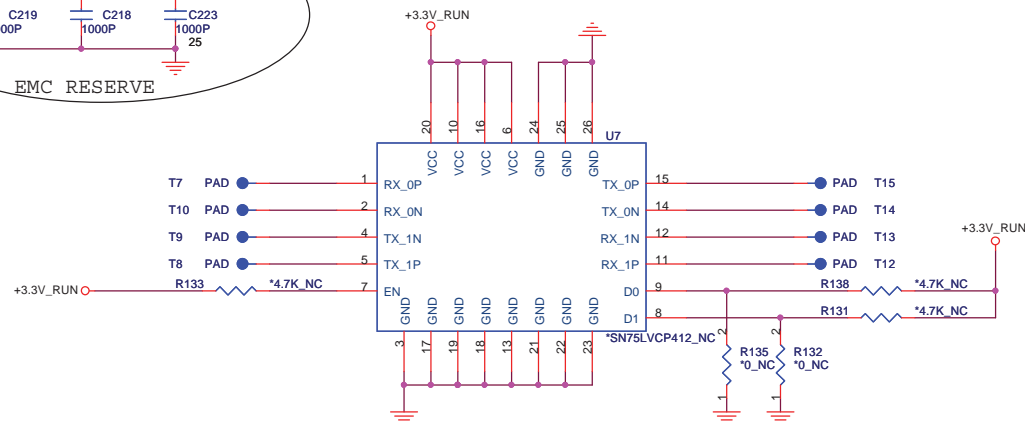
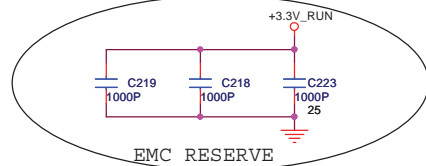


Place one 150uF cap by each USB connector.

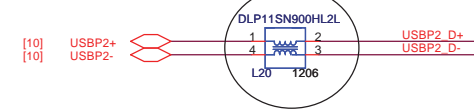
Each channel is 1A



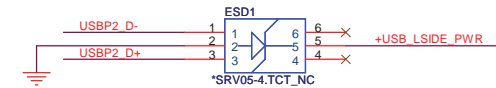
E-SATA Re-driver



Platforms should put in PADS for the USB chokes if they have the room. Chokes should be ~~NOPOP~~.

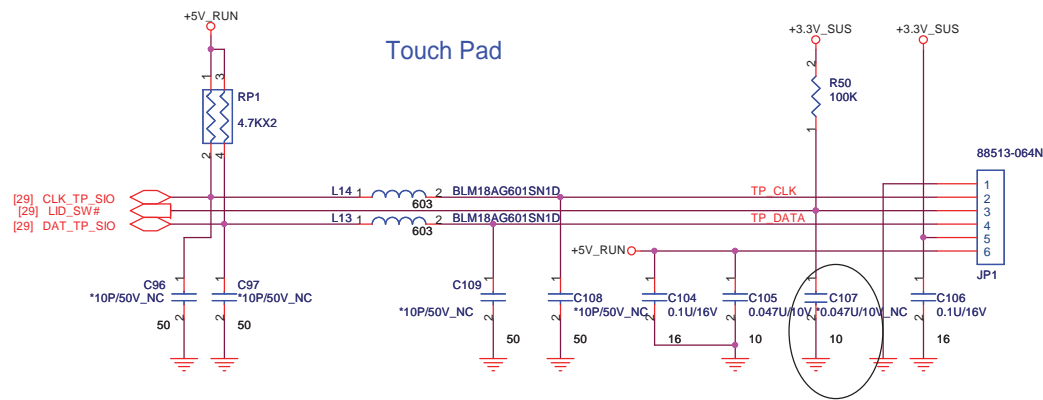


Place ESD diodes as close as USB connector.



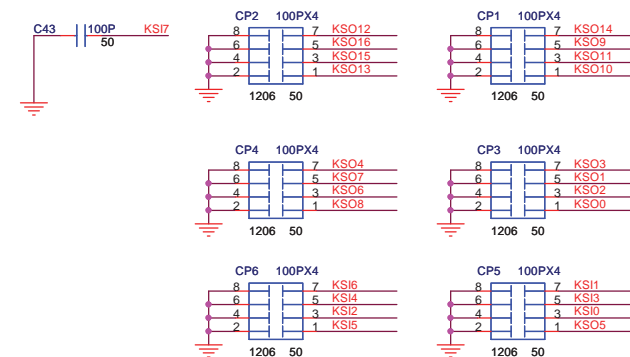
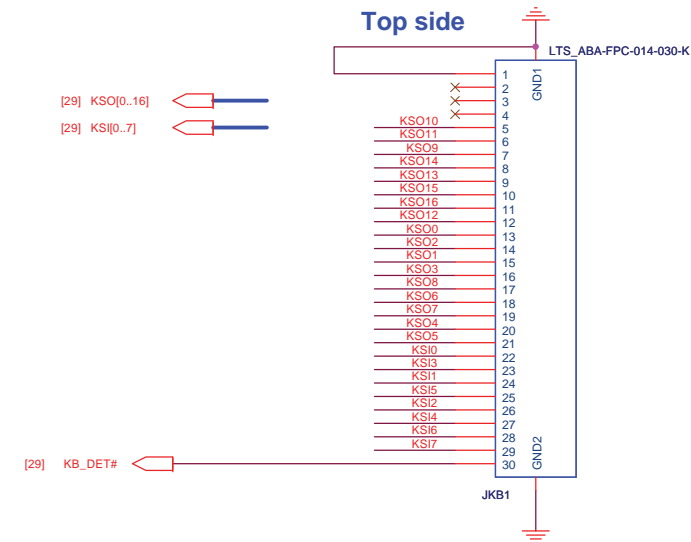
Note: Boost:5dB, Standard SATA:0dB

EN	D0	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost



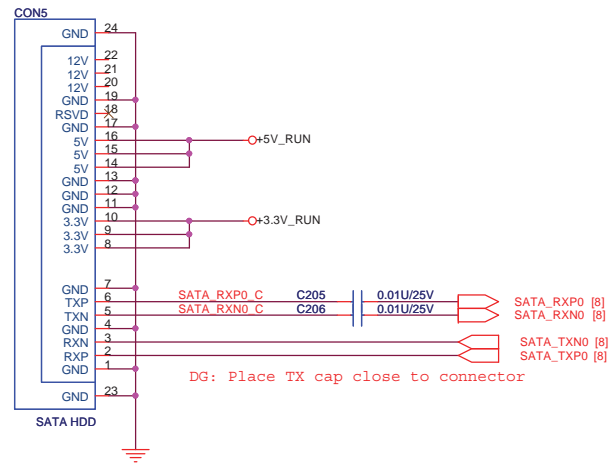
KEYBOARD CONNECTOR

Top side

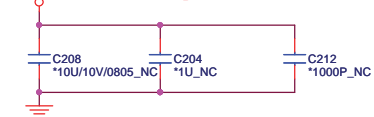


100P CAPS CLOSE TO JKB1

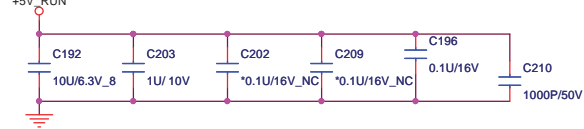
SATA Connector.



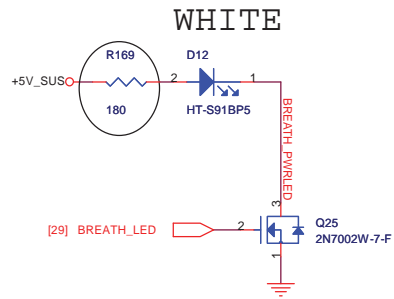
+3.3V_RUN Place caps close to connector.



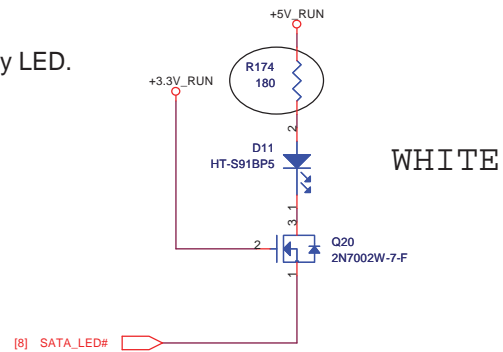
+5V_RUN Place caps close to connector.



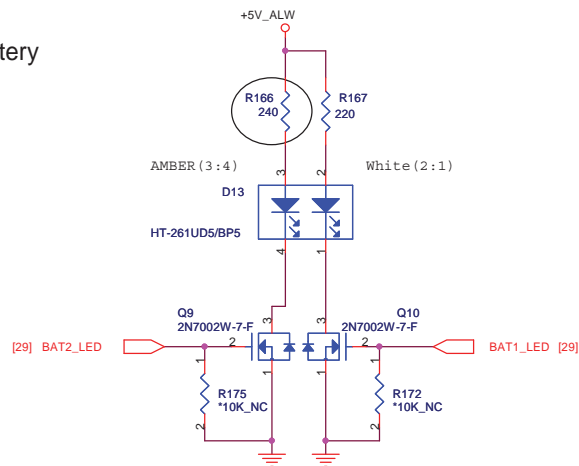
Power



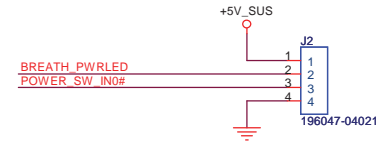
HDD activity LED.



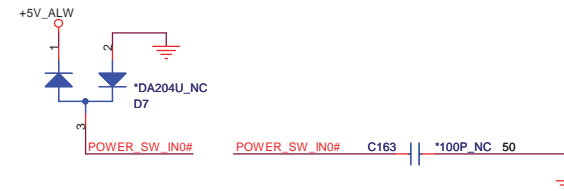
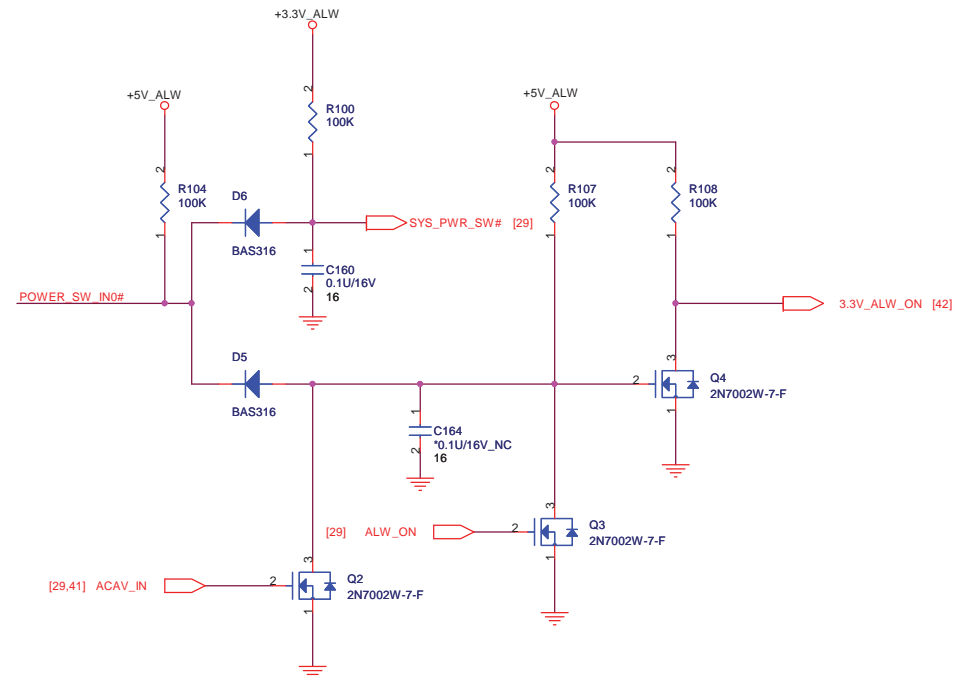
Battery



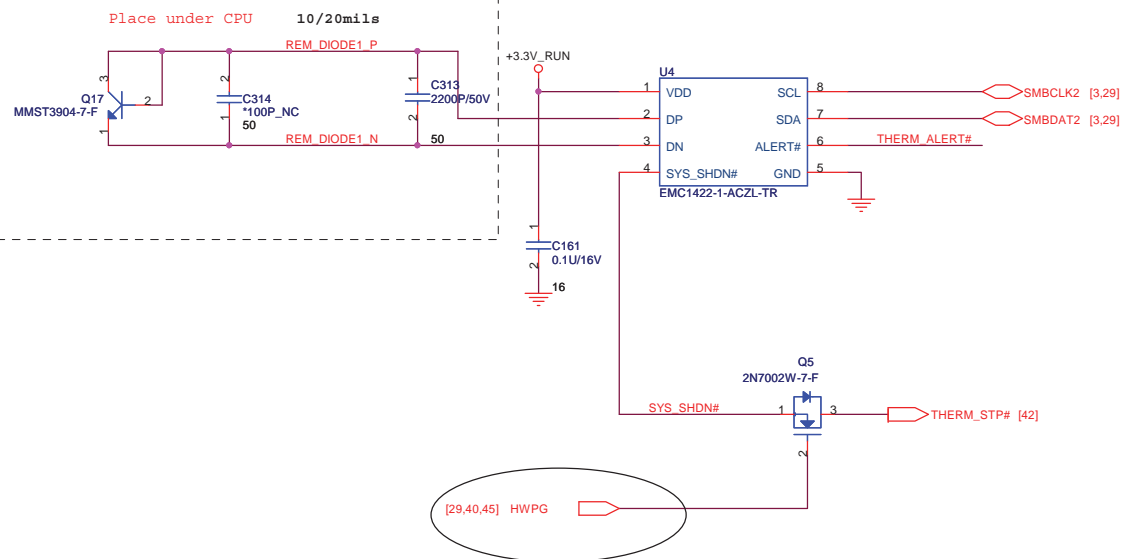
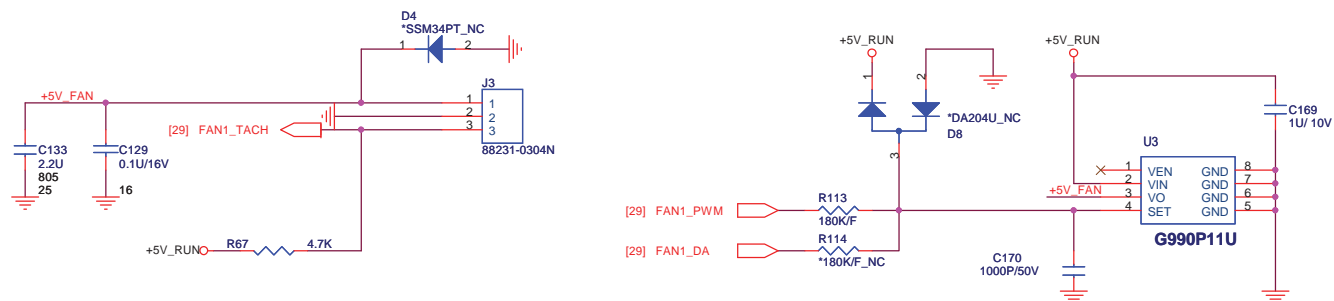
Power button Cable



3VALW ON POWER LOGIC

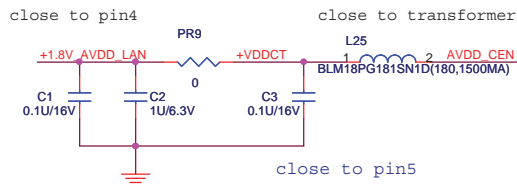
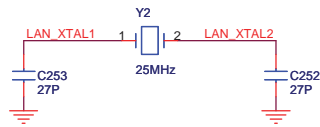


FAN CONTROL



OTP 85 degree C

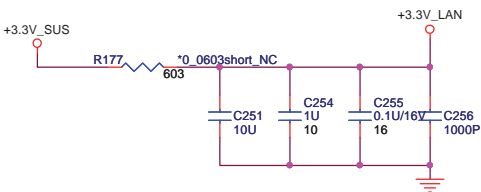
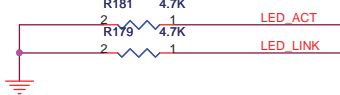




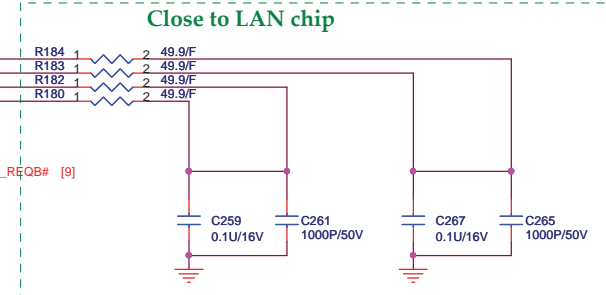
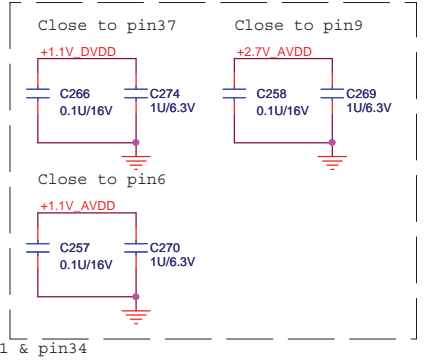
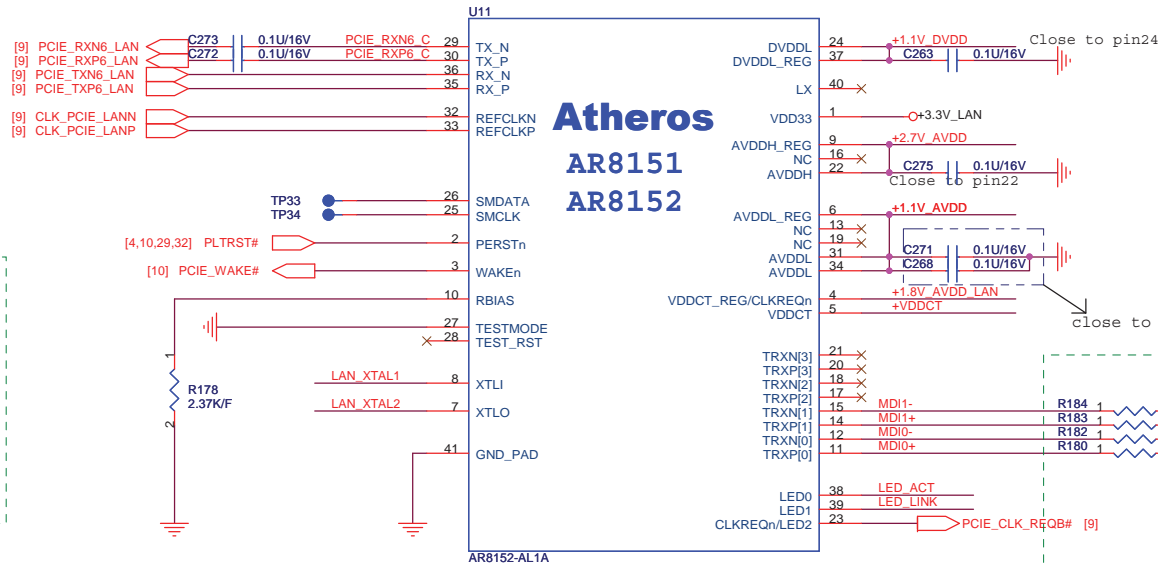
LDO MODE

PWR-ON-STRAPPING

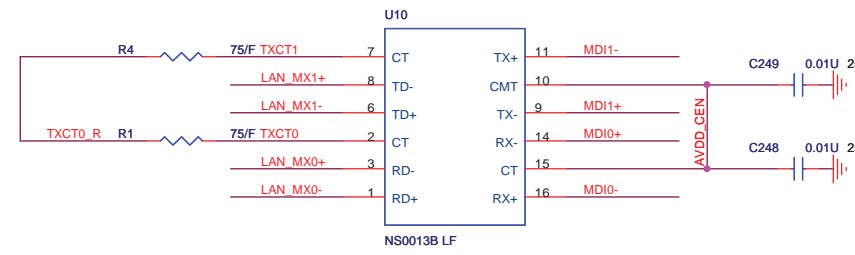
	SWR	LDO
LED_LINK	1	0
LED_ACT	0/C	NO/C
	1	0



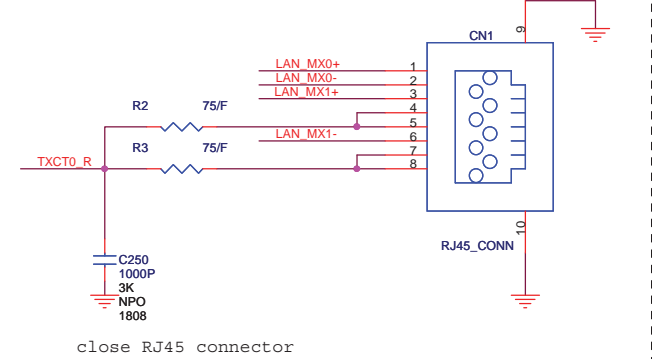
These Caps close LAN Chip VDD33 pins



TRANSFORMER



RJ45



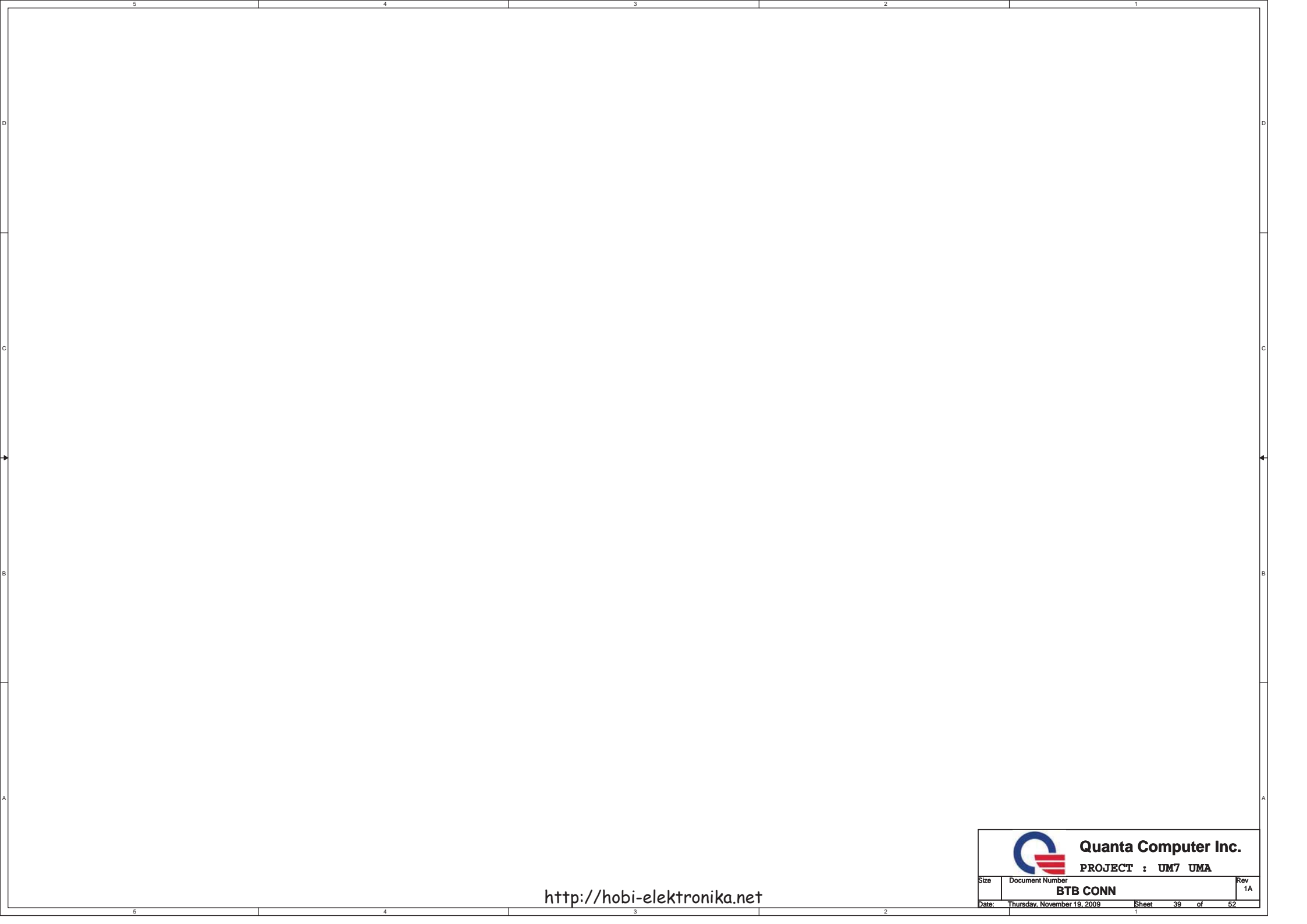
close RJ45 connector

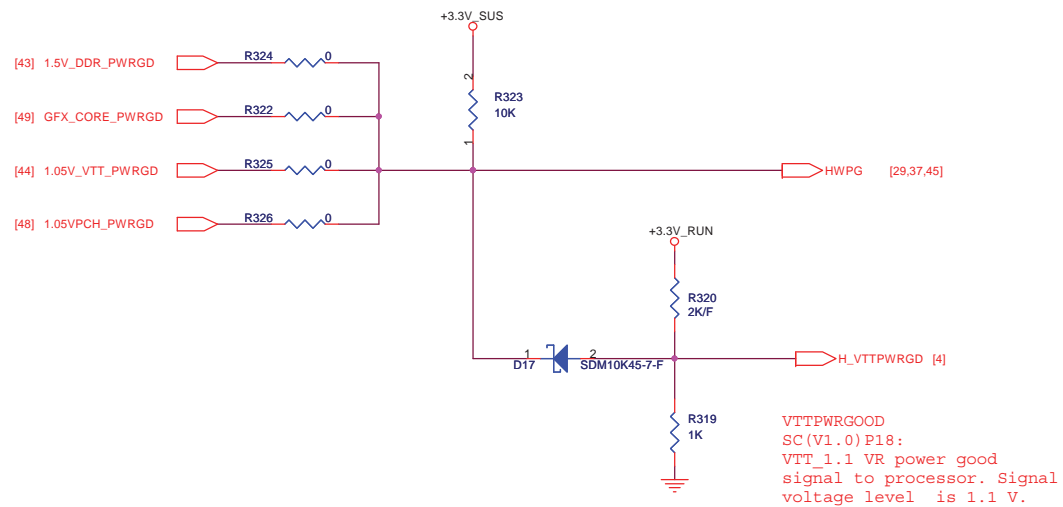


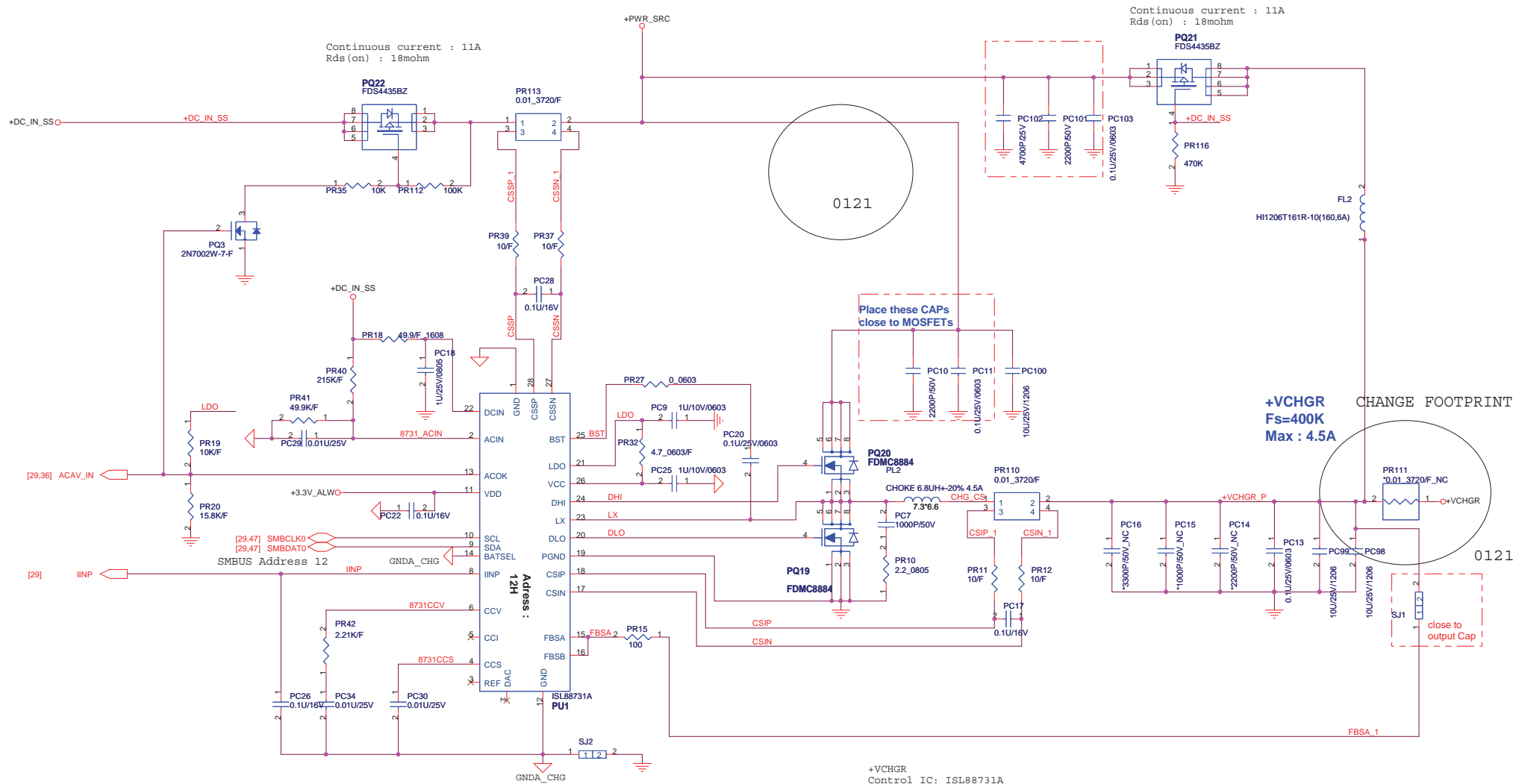
Quanta Computer Inc.

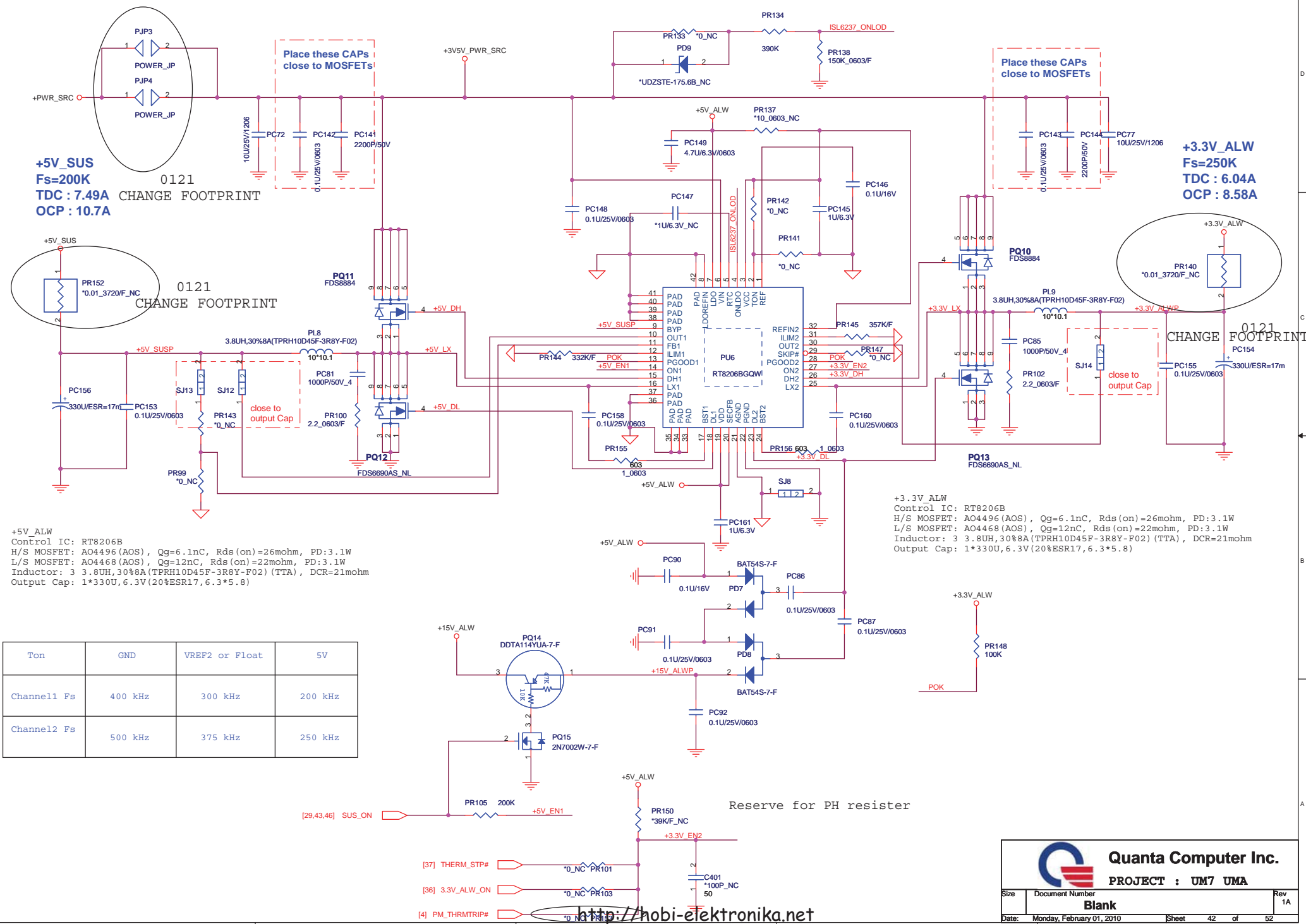
PROJECT : UM7 UMA

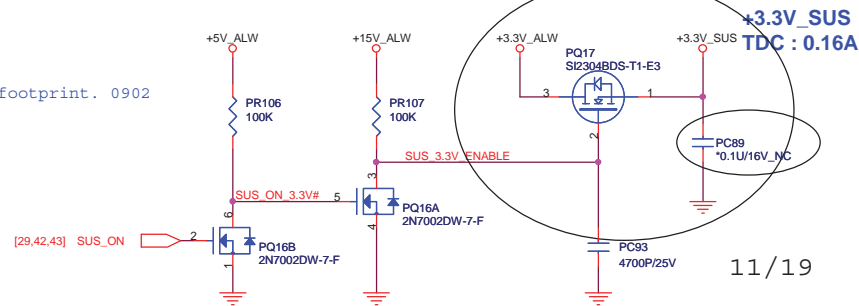
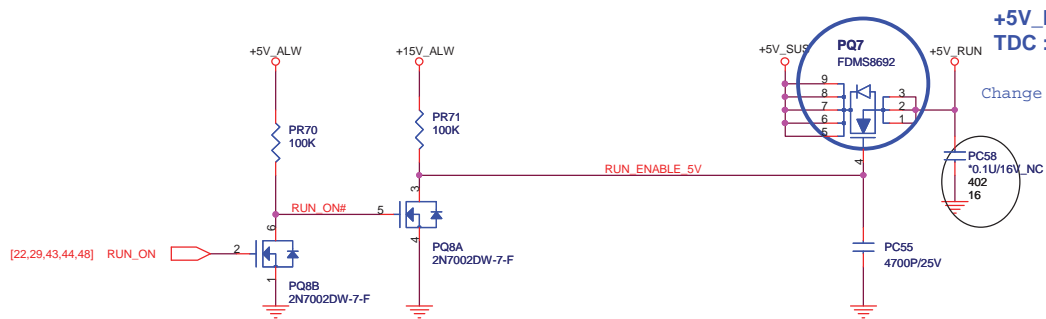
LAN(AR8152/RJ-45)



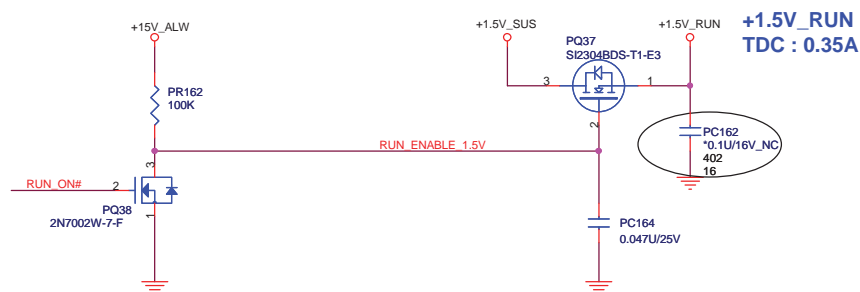




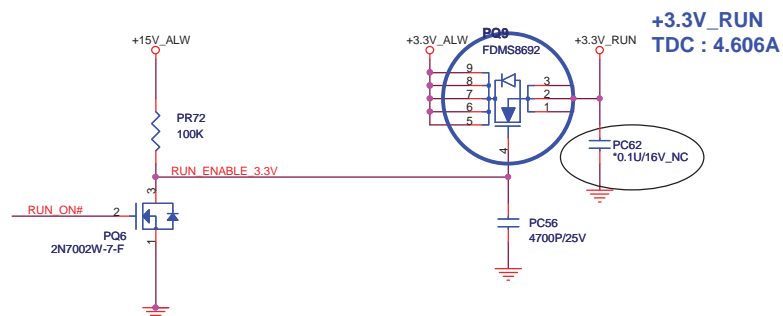




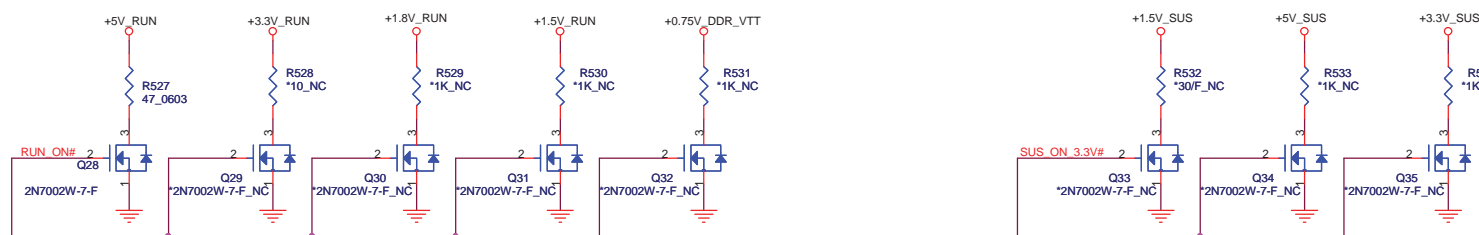
11/19



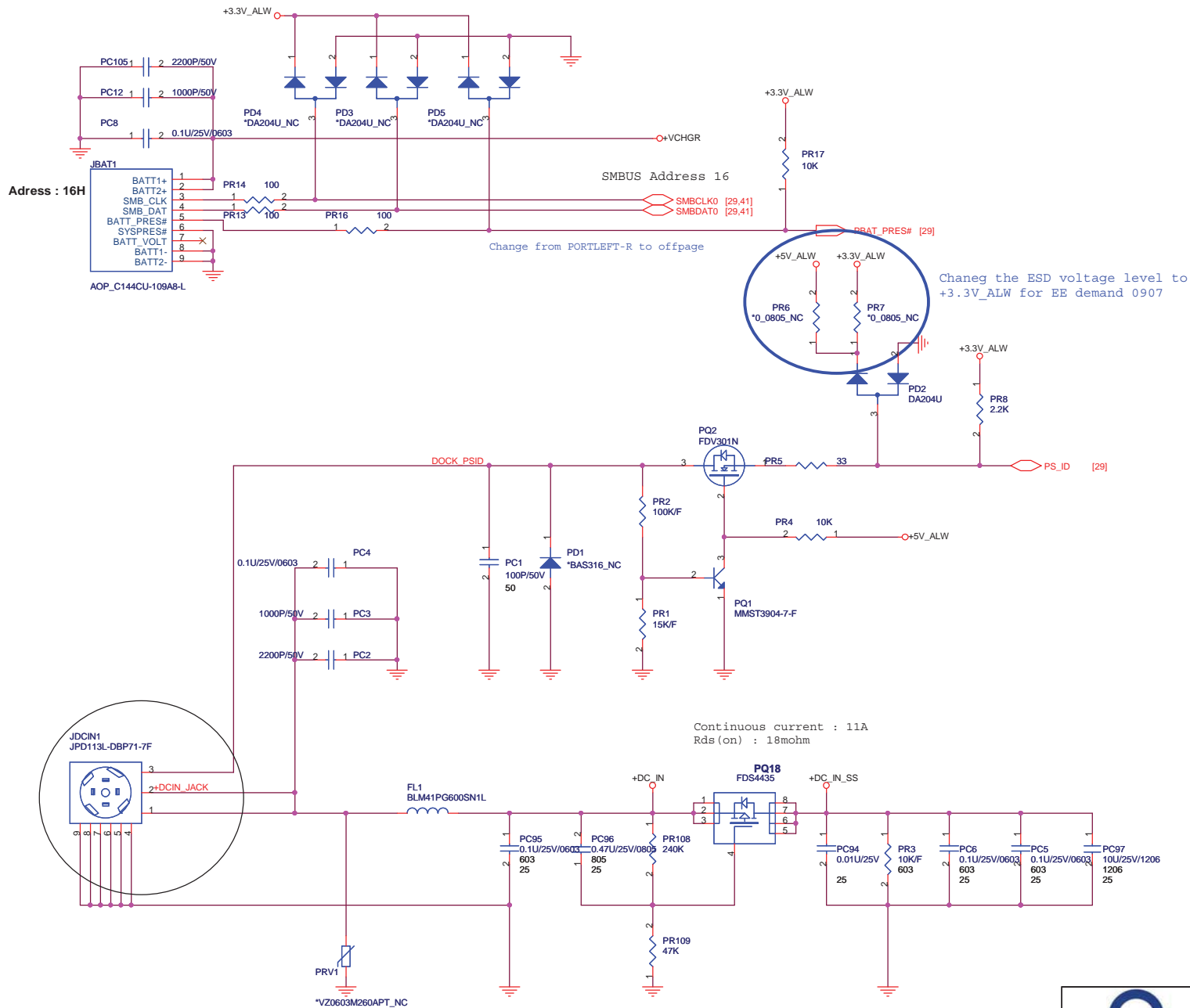
Change component from IRF8707 to.FDMS8692 0902

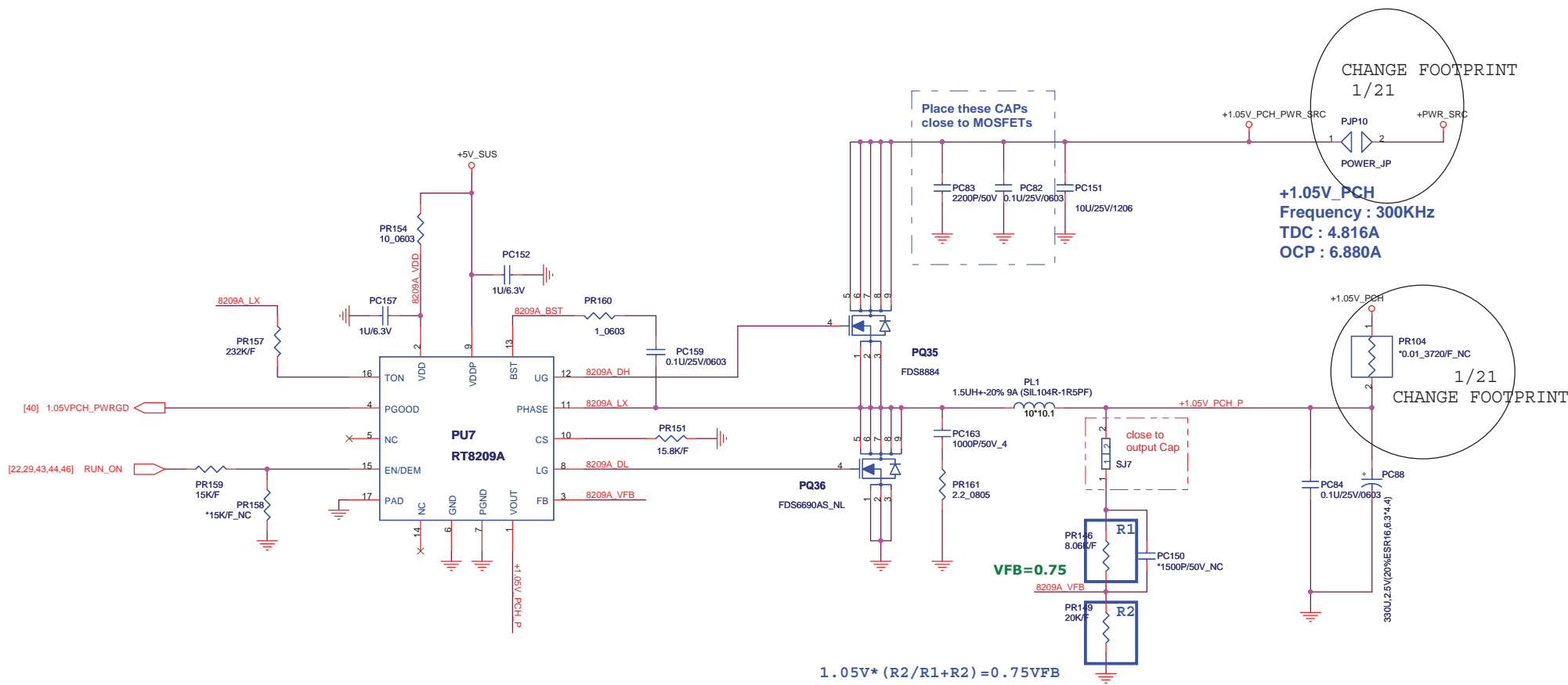


Reserve discharge path

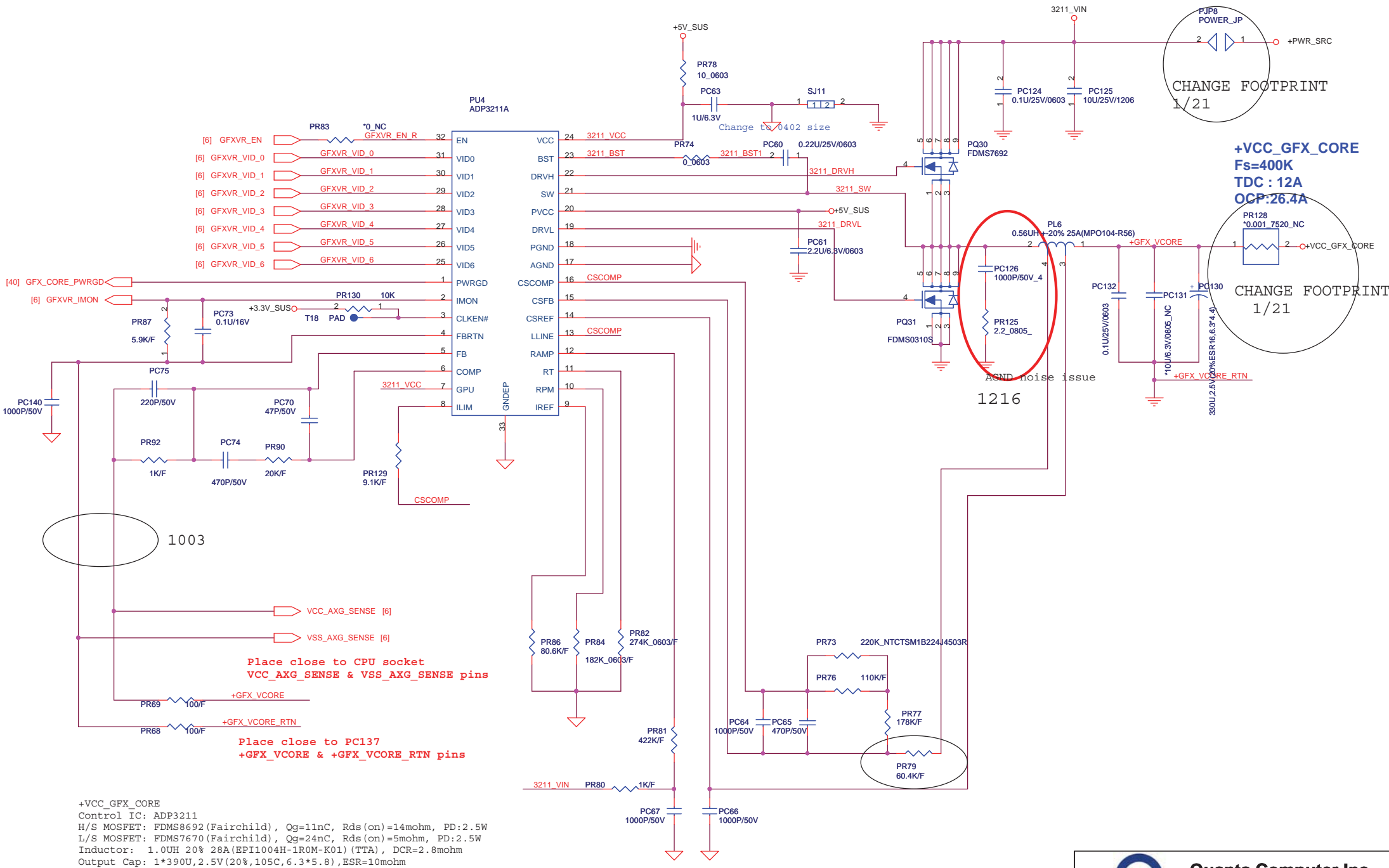


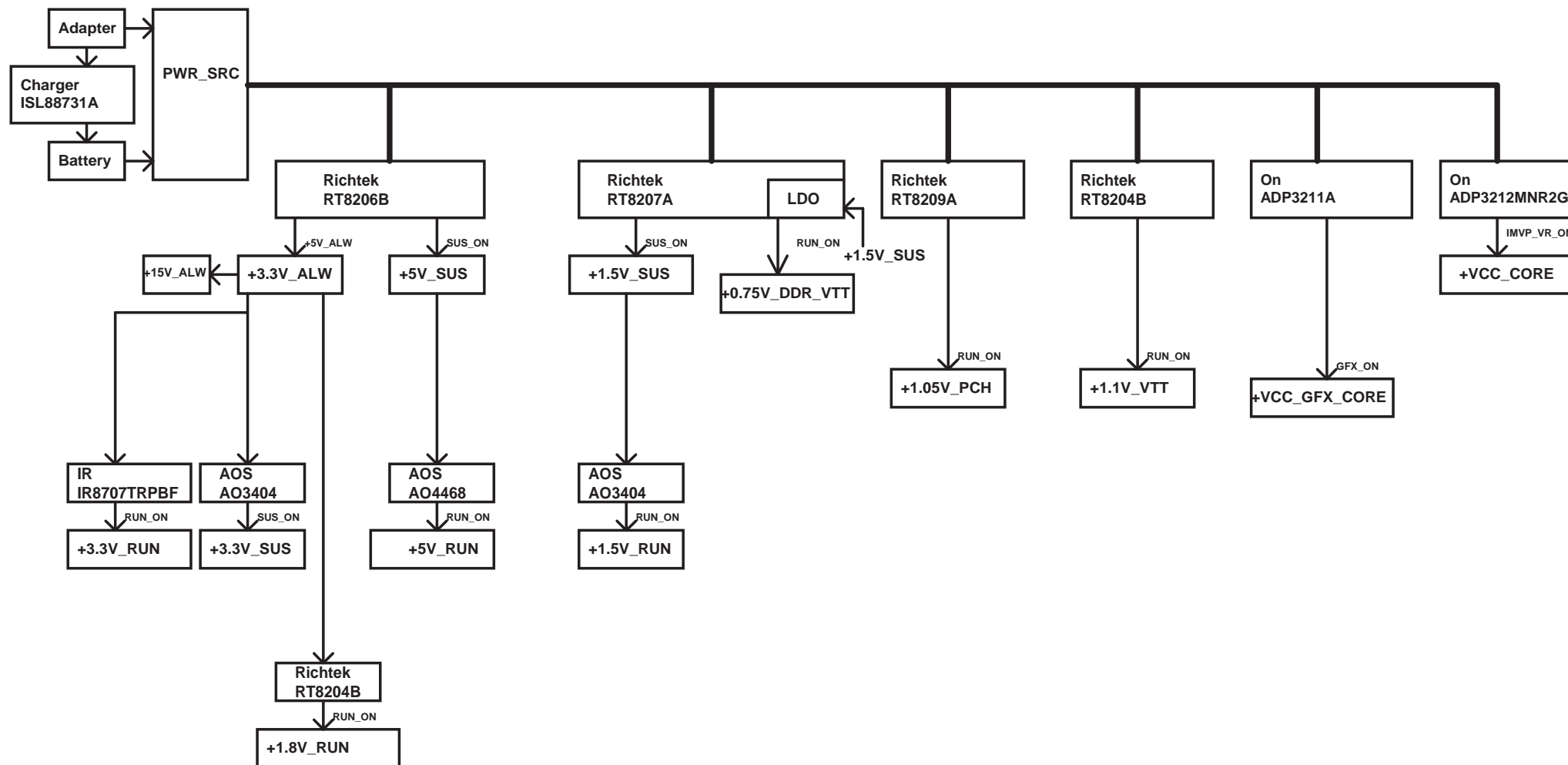
<http://hobi-elektronika.net>





+1.05V_PCH
Control IC: RT8209A
H/S MOSFET: AO4496 (AOS), Qg=6.1nC, Rds(on)=26mohm, PD:3.1W
L/S MOSFET: AO4468 (AOS), Qg=12nC, Rds(on)=22mohm, PD:3.1W
Inductor: 1.5uH+-20% 9A (10D40F-1R5M) (TTA), DCR=10.5mohm
Output Cap: 1*390u, 2.5V (20%, 105C, 6.3*5.8), ESR=10mohm





Power Design Block Diagram 2009/08/24

