

**Enrico Caruso 14**  
**Muxless/UMA Schematics Document**  
**Sandy Bridge**  
**Intel PCH**  
**2011-04-07**  
**REV : A00**

*DY : None Installed*  
*UMA: UMA ONLY installed*  
*PSL: KBC795 PSL circuit for 10mW solution installed.*  
*10mW: External circuit for 10mW solution installed.*  
*DIS: MUXLESS solution installed.*  
*Surge: For GO Rural config stuff.*  
*GIGA: For GIGA LAN config stuff.*  
*HDMI: For HDMI config stuff.*  
*DIS\_CRT: Pure DIS install*

<Core Design>



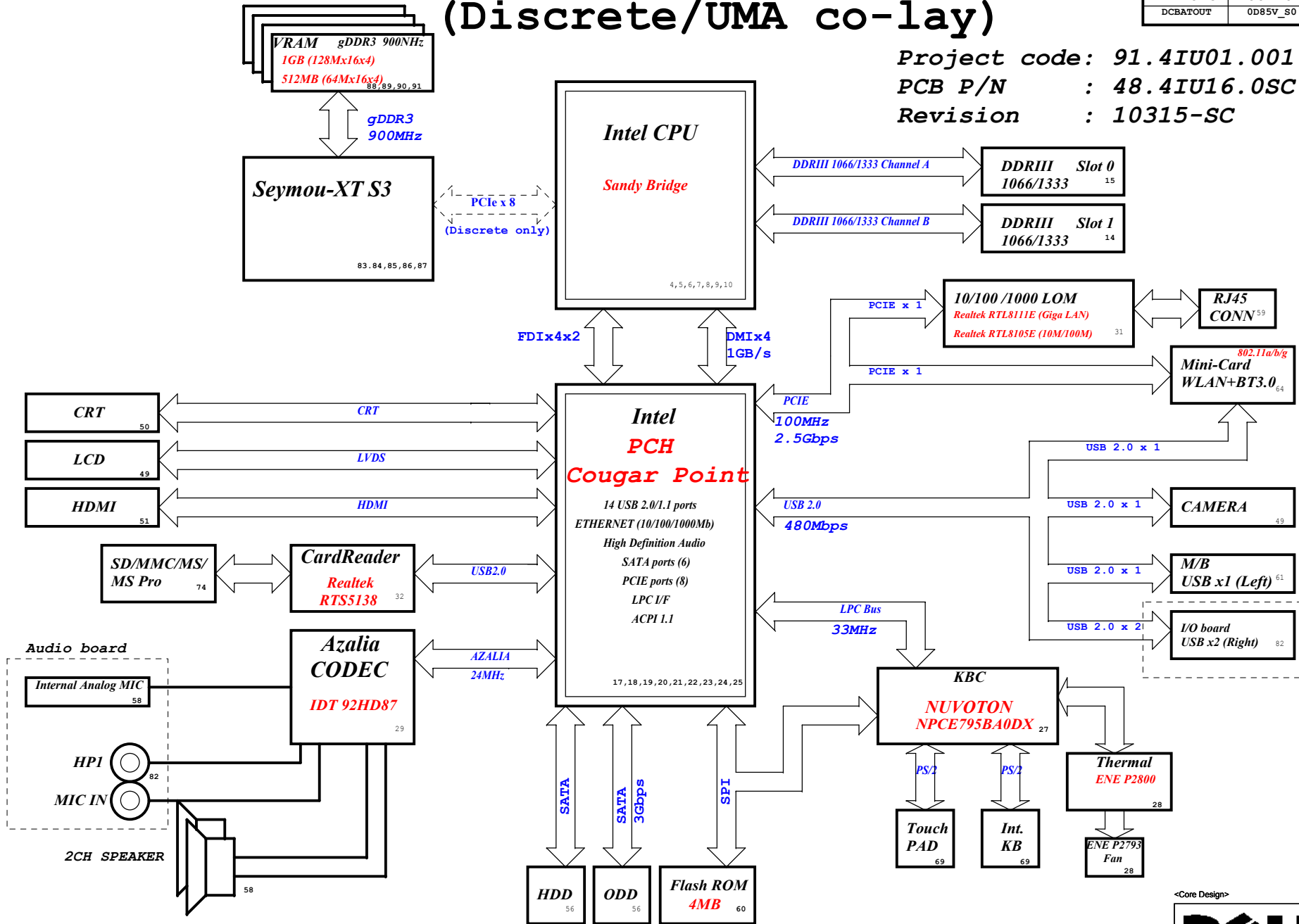
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Cover Page		
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##OnMainBoard

# Block Diagram (Discrete/UMA co-lay)

Project code: 91.4IU01.001  
PCB P/N : 48.4IU16.0SC  
Revision : 10315-SC

SYSTEM DC/DC APL5916 48		CPU DC/DC VT1316+1314 42~44	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
DCBATOUT	0D85V_S0	DCBATOUT	VCC_CORE
SYSTEM DC/DC TPS51218 45		SYSTEM DC/DC TPS51125 41	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT	DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5 15V_S5
SYSTEM DC/DC TPS51216R 46		SYSTEM DC/DC TPS51216R 46	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3	DCBATOUT	VCC_GFXCORE
GFX DC/DC VT1316+1317 44		VGA RT8208B 92	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE	DCBATOUT	VGA_CORE
TI CHARGER BQ24707 40		SYSTEM DC/DC APW7153B 47	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT	3D3V_S5	1D8V_S0
SYSTEM DC/DC G9731 93		Switches	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
1D5V_S3	1V_VGA_S0	1D5V_S3	1D5V_S0
3D3V_S0	1D8V_VGA_S0	5V_S5	5V_S0
PCB LAYER		PCB LAYER	
L1:Top L4:Signal L2:GND L5:VCC L3:Signal L6:Bottom		L1:Top L4:Signal L2:GND L5:VCC L3:Signal L6:Bottom	



<Core Design>

A		B		C		D		E			
PCH Strapping		Huron River Schematic Checklist Rev.0		www.laptopblue.vn		Huron River Schematic Checklist Rev.0		7			
Name		Schematics Notes		Pin Name		Strap Description		Configuration (Default value for each bit is 1 unless specified otherwise)		Default Value	
SPKR		Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-k - 10-k weak pull-up resistor.		CFG[2]		PCI-Express Static Lane Reversal		1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...		1	
INIT3_3V#		Weak internal pull-up. Leave as "No Connect".		CFG[4]				1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connectd to the EMBEDDED display Port		0	
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51		GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.		CFG[6:5]		PCI-Express Port Bifurcation Straps		11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled		11	
SPI_MOSI		Enable Danbury: Connect to Vcc3_3 with 8.2-k? weak pull-up resistor.  Disable Danbury: Left floating, no pull-down required.		CFG[7]		PEG DEFER TRAINING		1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training			
NV_ALE		Enable Danbury: Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor]  Disable Danbury: Leave floating (internal pull-down)									
NC_CLE		DMI termination voltage. Weak internal pull-up. Do not pull low.									
HAD_DOCK_EN# /GPIO[33]		Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.									
HDA_SDO		Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.									
HDA_SYNC		Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.									
GPIO15		Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.									
GPIO8		GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.									
GPIO27		Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.									

POWER PLANE		VOLTAGE		Voltage Rails		DESCRIPTION	
				ACTIVE IN			
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0		5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V		S0		CPU Core Rail Graphics Core Rail	
5V_USBX_S3 1D5V_S3 DDR_VREF_S3		5V 1.5V 0.75V		S3			
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5		6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V		All S states		AC Brick Mode only	
3D3V_LAN_S5		3.3V		WOL_EN		Legacy WOL	
3D3V_AUX_KBC		3.3V		DSW, Sx		ON for supporting Deep Sleep states	
3D3V_AUX_S5		3.3V		G3, Sx		Powered by Li Coin Cell in G3 and +V3ALW in Sx	

SATA Table	
SATA	
Pair	Device
0	HDD1
1	N/A
2	N/A
3	N/A
4	ODD
5	N/A

USB Table	
Pair	Device
0	X
1	USB Ext. port 2 (MB)
2	X
3	X
4	X
5	CARD READER
6	X
7	X
8	USB Ext. port 3
9	USB Ext. port 1
10	X
11	Mini Card1 (WLAN+BT)
12	CAMERA
13	X

SMBus ADDRESSES	
I <sup>2</sup> C / SMBus Addresses	HURON RIVER ORB
Device	Ref Des Address Hex Bus
EC SMBus 1 Battery CHARGER	BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP	SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI	PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

PCIE Routing	
LANE1	X
LANE2	LAN
LANE3	X
LANE4	Wireless
LANE5	X
LANE6	X
LANE7	X
LANE8	X

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Dell Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
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SSID = CPU

Signal Routing Guideline:  
PEG\_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.  
PEG\_ICOMPI & PEG\_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Note:  
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:  
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

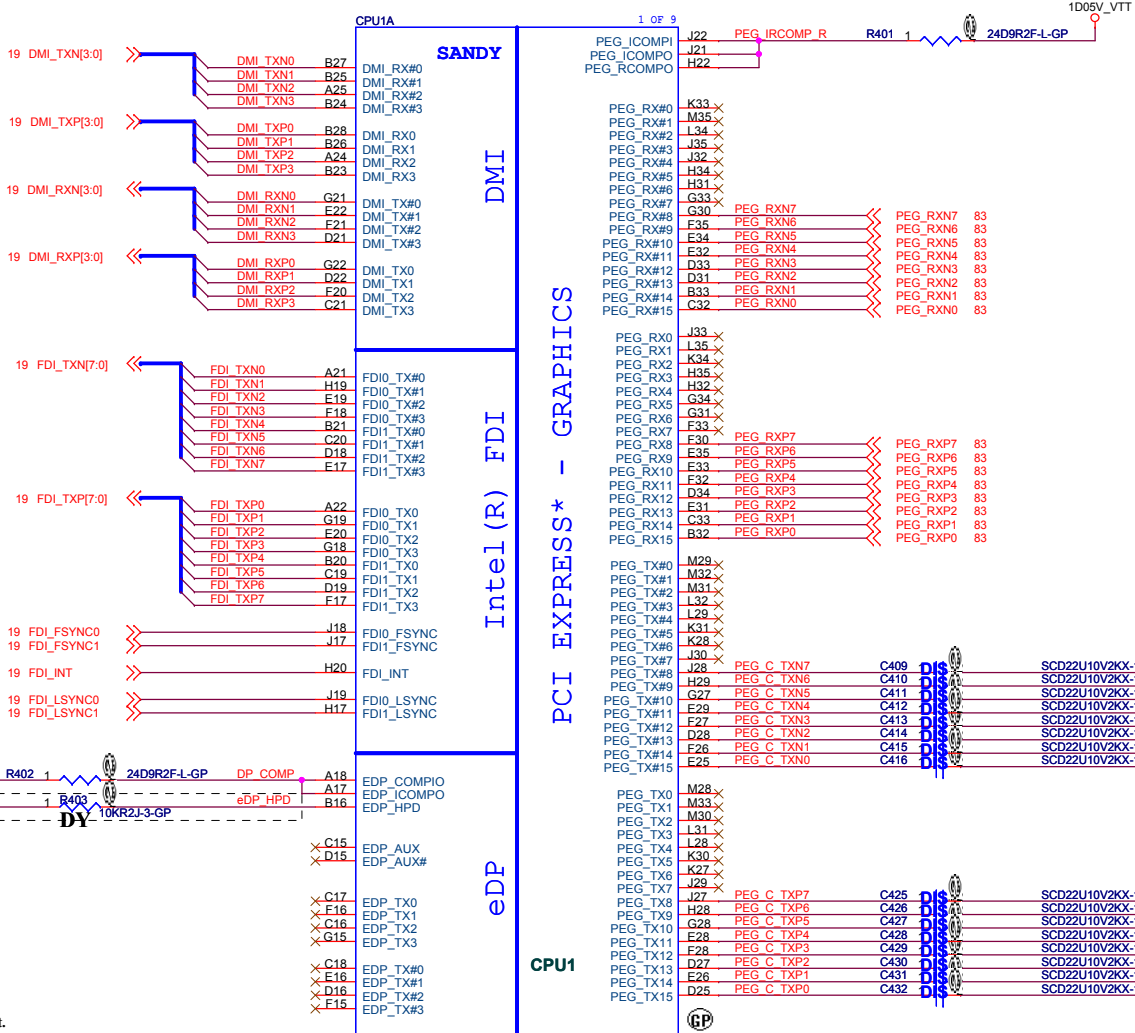
Note:  
Lane reversal does not apply to FDI sideband signals.

Signal Routing Guideline:  
EDP\_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.  
EDP\_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.  
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

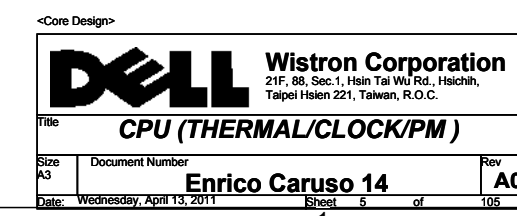
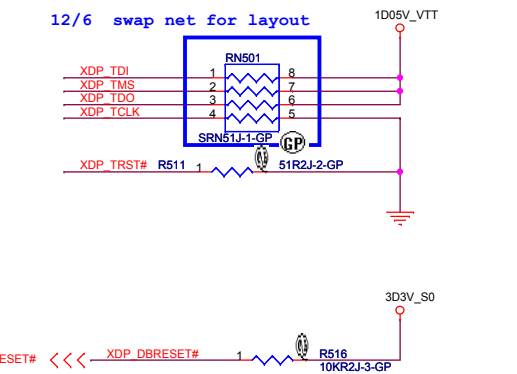
Stuff to disable internal graphics function for power saving.

NOTE:  
Select a Fast FET similar to 2N7002E whose rise/fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-k pull-Up resistor on the motherboard.



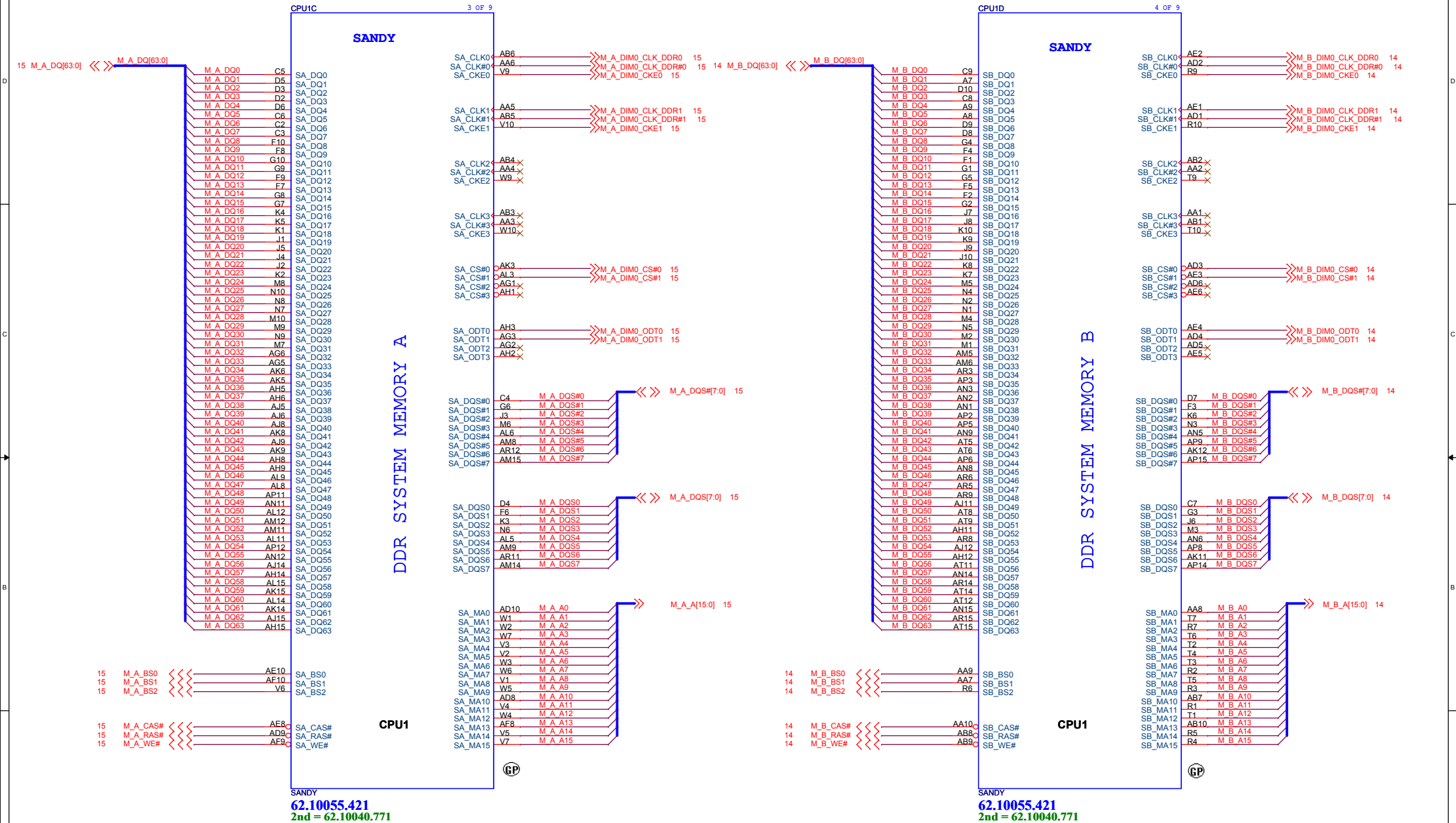
NOTE.  
If PEG is not implemented, the RX&TX pairs can be left as No Connect  
PEG Static Lane Reversal

SANDY SKT-BGA989C470395-1H180  
62.10055.421  
2nd = 62.10040.771



SSID = CPU

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**CPU (DDR)**

Size

Document Number
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## Enrico Caruso 14

ev

Date \_\_\_\_\_

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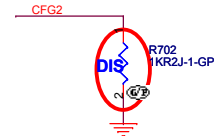
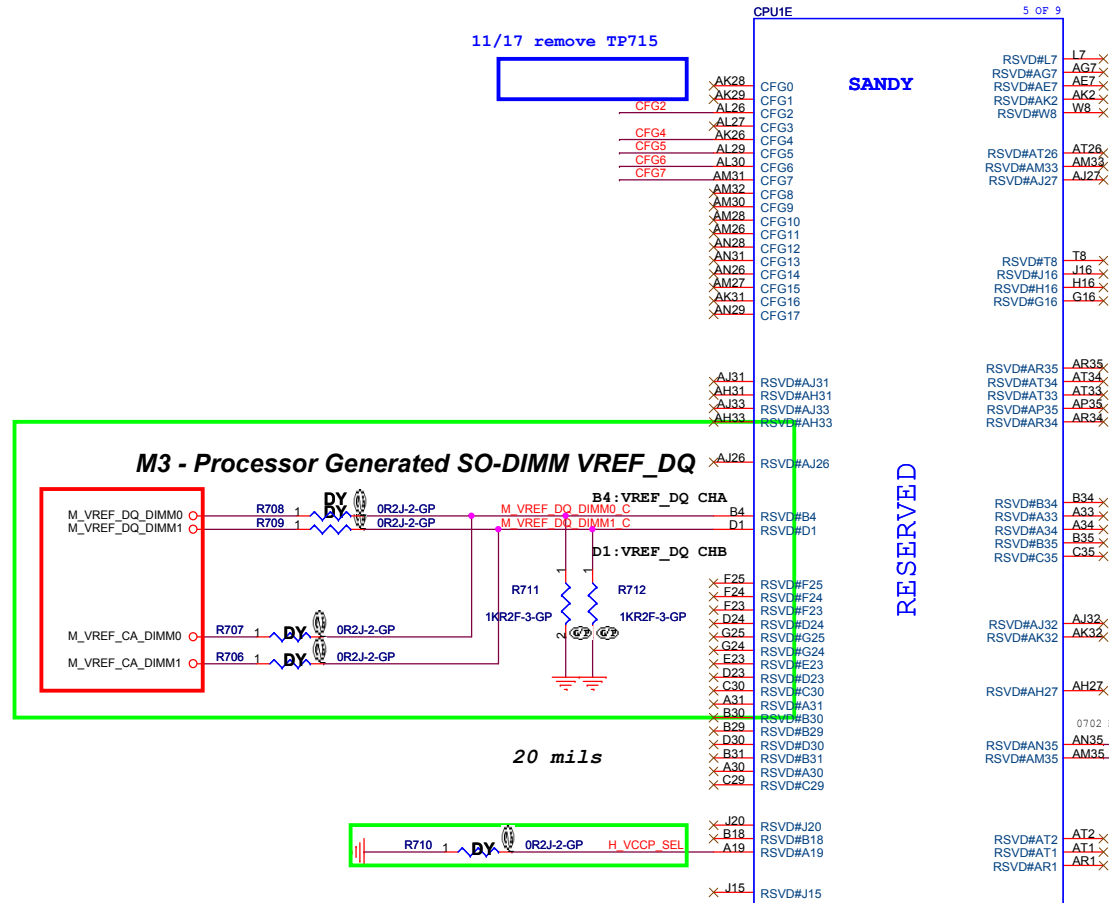
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05

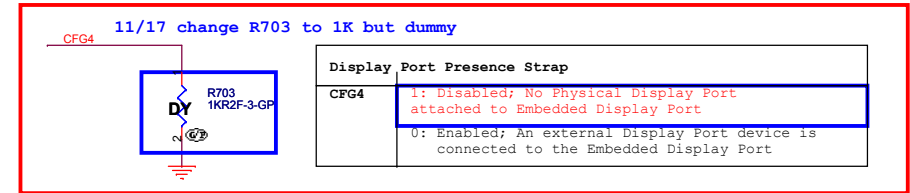
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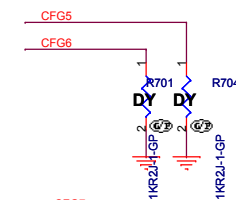
11/17 remove TP715



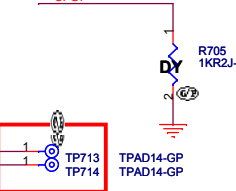
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled 01: Reserved - (Device 1 function 1 disabled; function 2 enabled) 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

SANDY SKT-BGA989C470395-1H180  
62.10055.421  
2nd = 62.10040.771

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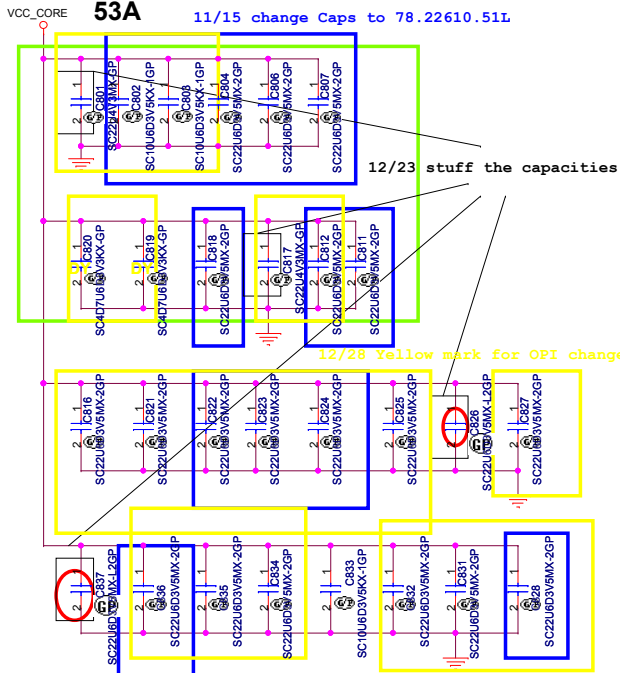
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Voltage Rail	Voltage	Iccmax
VCC_CORE(QC)	0.8~1.35	94A
VCC_CORE(DC)	0.8~1.35	53A
VCCIO	1.05	8.5A
VDDQ	1.5	10A
VCCSA	0.75~0.9	6A
VCCPLL	1.8	1.2A
VAXG	0~1.52	33A

## PROCESSOR CORE POWER

53A

11/15 change Caps to 78.22610.51L



VCC Output Decoupling Recommendation:  
 4 x 470 uF at Bottom Socket Edge  
 8 x 22 uF at Top Socket Cavity  
 8 x 22 uF at Top Socket Edge  
 8 x 22 uF at Bottom Socket Cavity

11/4 add Caps to 28 location as vendor recommend.  
 X01-0127 Stuff C812, C822, C831, C834  
 for VCC core noise issue.

X01-0217 Stuff C801=22uF  
 change C817 to 22uF

VCC\_CORE

SANDY

AG35 VCC  
 AG34 VCC  
 AG33 VCC  
 AG32 VCC  
 AG31 VCC  
 AG30 VCC  
 AG29 VCC  
 AG28 VCC  
 AG27 VCC  
 AG26 VCC  
 AF35 VCC  
 AF34 VCC  
 AF33 VCC  
 AF32 VCC  
 AF31 VCC  
 AF30 VCC  
 AF29 VCC  
 AF28 VCC  
 AF27 VCC  
 AF26 VCC  
 AD35 VCC  
 AD34 VCC  
 AD33 VCC  
 AD32 VCC  
 AD31 VCC  
 AD30 VCC  
 AD29 VCC  
 AD28 VCC  
 AD27 VCC  
 AC35 VCC  
 AC34 VCC  
 AC33 VCC  
 AC32 VCC  
 AC31 VCC  
 AC30 VCC  
 AC29 VCC  
 AC28 VCC  
 AC27 VCC  
 AC26 VCC  
 AA35 VCC  
 AA34 VCC  
 AA33 VCC  
 AA32 VCC  
 AA31 VCC  
 AA30 VCC  
 AA29 VCC  
 AA28 VCC  
 AA27 VCC  
 AA26 VCC  
 V35 VCC  
 Y34 VCC  
 Y33 VCC  
 Y32 VCC  
 Y31 VCC  
 Y30 VCC  
 Y29 VCC  
 Y28 VCC  
 Y27 VCC  
 Y26 VCC  
 V35 VCC  
 V34 VCC  
 V33 VCC  
 V32 VCC  
 V31 VCC  
 V30 VCC  
 V29 VCC  
 V28 VCC  
 V27 VCC  
 V26 VCC  
 U35 VCC  
 U34 VCC  
 U33 VCC  
 U32 VCC  
 U31 VCC  
 U30 VCC  
 U29 VCC  
 U28 VCC  
 U27 VCC  
 U26 VCC  
 R35 VCC  
 R34 VCC  
 R33 VCC  
 R32 VCC  
 R31 VCC  
 R30 VCC  
 R29 VCC  
 R28 VCC  
 R27 VCC  
 R26 VCC  
 P35 VCC  
 P34 VCC  
 P33 VCC  
 P32 VCC  
 P31 VCC  
 P30 VCC  
 P29 VCC  
 P28 VCC  
 P27 VCC  
 P26 VCC

CORE SUPPLY

SVID

SENSE LINES

CPU1

SANDY  
 62.10055.421  
 2nd = 62.10040.771

VCCIO Output Decoupling Recommendation:  
 2 x 330 uF (3 x 330 uF for 2012 capable designs)  
 5 x 22 uF & 5 x 0805 no-stuff at Bottom  
 7 x 22 uF & 2 x 0805 no-stuff at Top

12/28 Yellow mark for OPI change

PROCESSOR VCCIO: 8.5A

12/23 stuff the capacities

No-stuff sites outside the socket may be removed.  
 No-stuff sites inside the socket cavity need to remain.

11/16 follow DN13 to meet schematic check list

These resistors need to close to power IC  
 11/17 change part reference R807 to R805



VIDALERT#  
 VIDSLCK  
 VIDSOUT



VCC\_SENSE

VSSIO\_SENSE

VCC\_CORE

R801

100R2F-L1-GP-U

VCC\_SENSE 42

VSSIO\_SENSE 42

R802

100R2F-L1-GP-U

VCCIO\_SENSE 45

VSSIO\_SENSE 45

&lt;Core Design&gt;



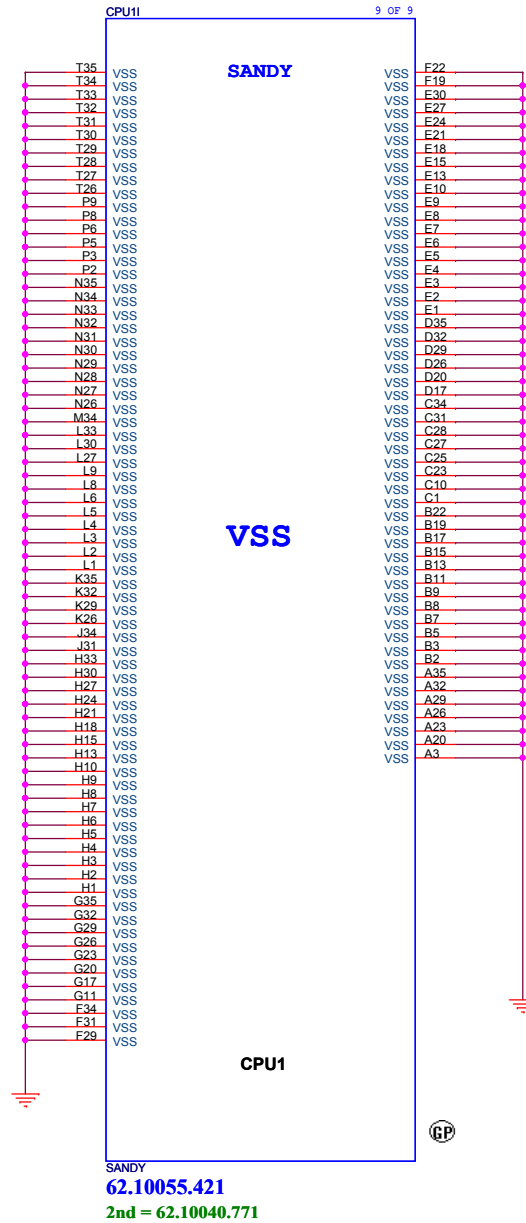
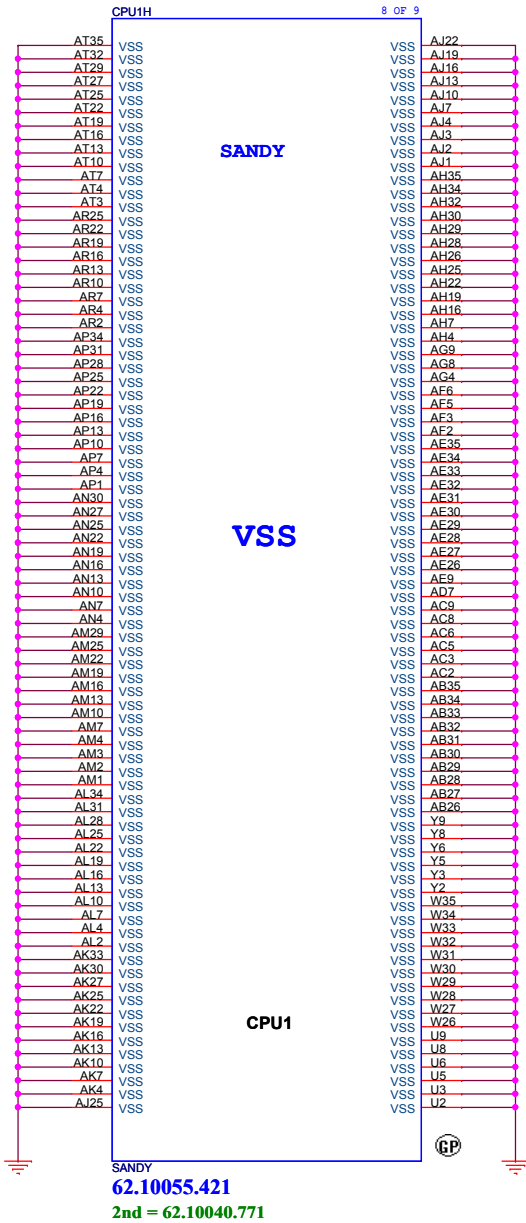
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SSID = CPU



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***XDP***

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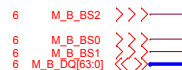
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0D75V\_S0

Place these caps close to VTT1 and VTT2.

C1418  
2 1  
SC1U6D3V2KX-CP

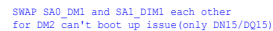
C1420  
2 1  
SC1U6D3V2KX-CP

C1421  
2 1  
SC1U6D3V2KX-CP

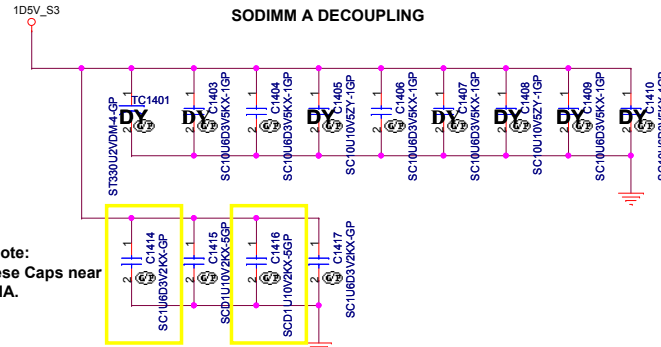
C1422  
2 1  
SC1U6D3V2KX-CP

C1419  
2 1  
SC1U6D3V5KX-1CP

Ground



If SA0\_DIM0 = 0, SA1\_DIM0 = 1  
SO-DIMMA SPD Address is 0xA4  
SQ-DIMMA TS Address is 0x34



**Layout Note:**  
Place these Caps near  
SO-DIMMA.

12/22 Change DM2 to 62.10024.E21

DDR3-204P-135-GP  
62.10024.E21

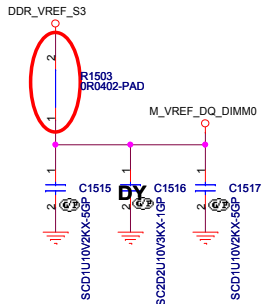
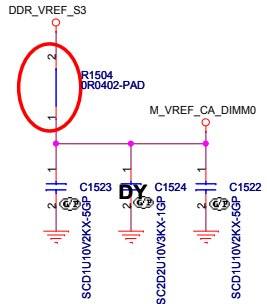
## SSID = MEMORY

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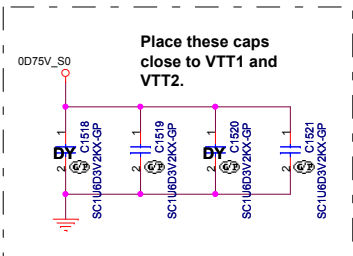
11/ 17 Change SMbus adress note

**Note:**  
SO-DIMMB SPD Address is 0xA0  
SO-DIMMB TS Address is 0x30

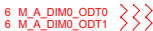
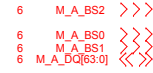
- SO-DIMMB is placed farther from the Processor than SO-DIMMA



X02-0303 change 0R to short pad



**Place these caps close to VTT1 and VTT2.**

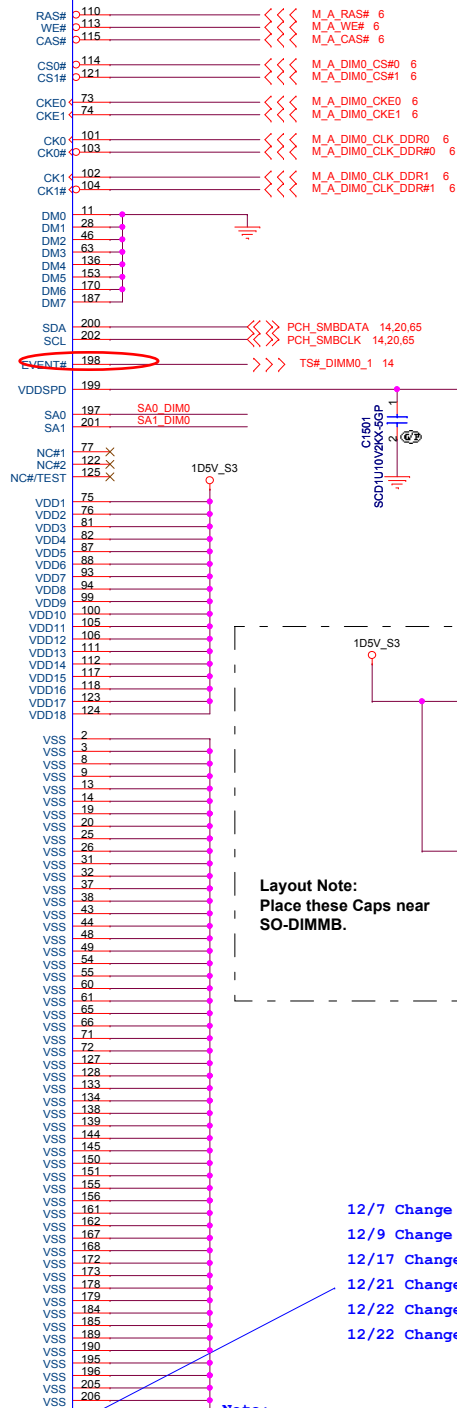


14,37 DDR3\_DRAMRST# >>>

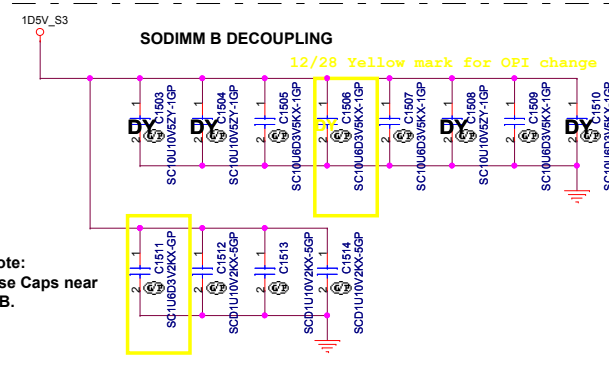


**H =9.2mm**

DDR3-204P-128-GP  
**62.10024.D51**



Note:  
The symbol DM1 is change value and PN only.



**Note:**  
Use Caps near  
B.

12/7 Change DM1 to 62.10024.D51

12/9 Change DM1 to 62.10017.K11

12/17 Change DM1 to 62.10017.N11

12/21 Change DM1 to 62.10017.Q41

12/22 Change DM1 to 62.10024.D91

12/22 Change DM1 to 62.10024.D51

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<b>DDR3-SODIMM1</b>			
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Title

**Reserved**

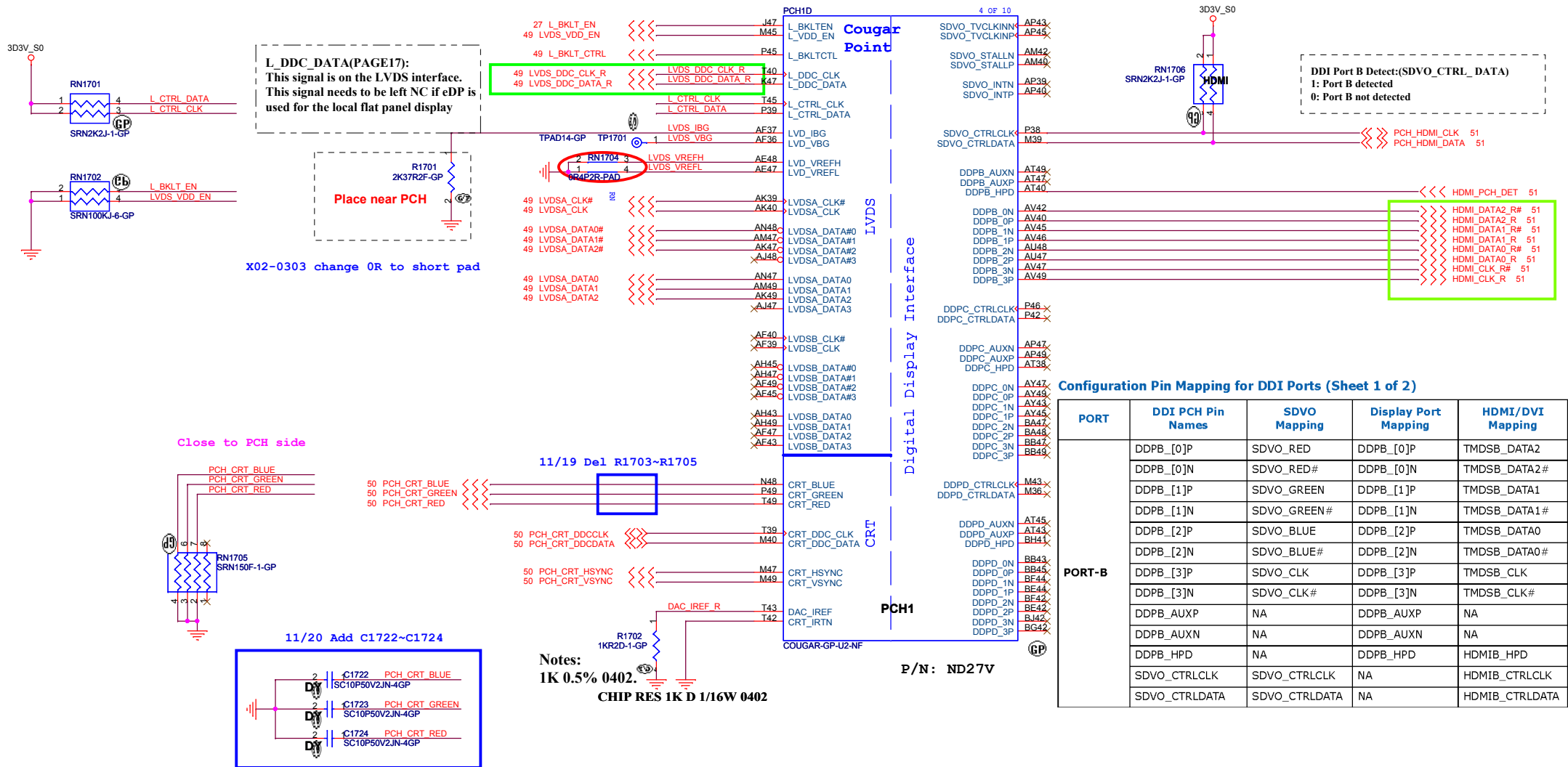
Size  
A3

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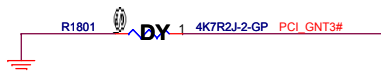
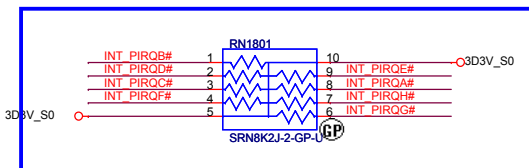


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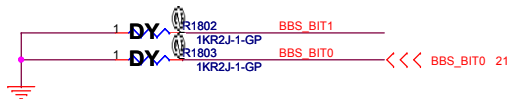
**DELL** Wistron Corporation  
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (LVDS/CRT/DDI)**  
Size: A3 Document Number: **Enrico Caruso 14** Rev: **A00**  
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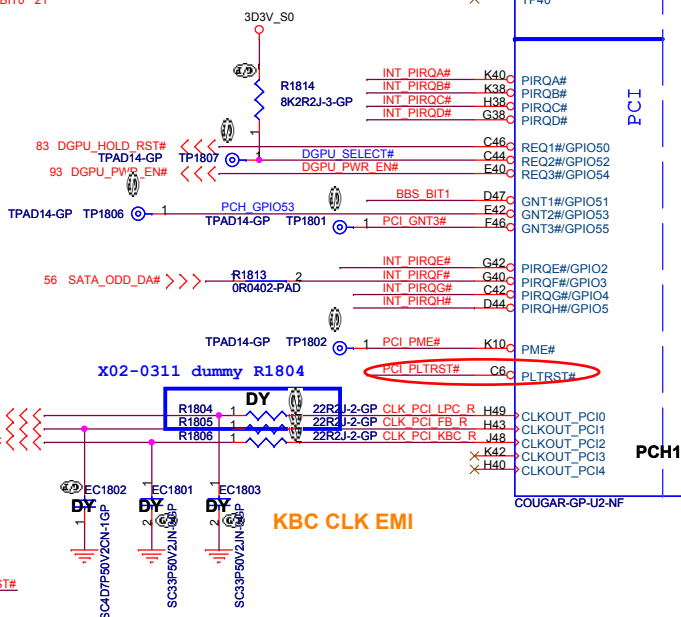
12/2 Net swap for layout



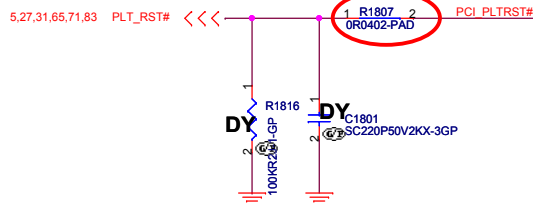
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI (Default)



X02-0303 change 0R to short pad



Cougar  
Point

## INVRAM

RSVD

USB

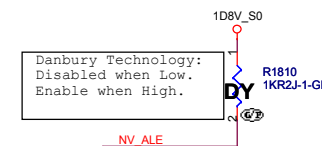
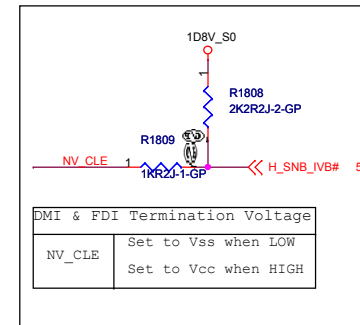
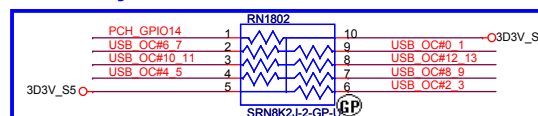
**PCH1**

COUGAR-GP-U2-NF

P/N: ND27V

12/1 Swap net for layout

11/11 change to RN1802 to meet schematic check result.



✗ USB Ext. port 1 (HS)  
External debug port use on Huron river platform

## USB Table

Pair	Device
0	X
1	USB Ext. port 2 (MB)
2	X
3	X
4	X
5	CARD READER
6	X
7	X
8	USB Ext. port 3
9	USB Ext. port 1
10	X
11	Mini Card1 (WLAN+BT)
12	CAMERA
13	X

### USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

**<Core Design>**



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### PCH (PCI/USB/NVRAM)

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Deep S4/S5 **Not** Supported

[illegible]

RSMRST#

#### 4.SUSWRN# used as SUSPWRDNACK/GPIO30

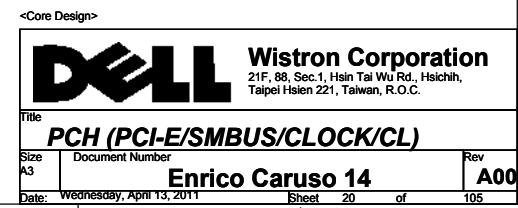
PCH SUSCLK KBC  
EC1901  
BY  
SC4D7P50V2CN-1GP

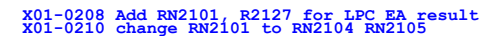


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A00

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3D3V\_S0

R2202

100KR2J-1-GP

SATA\_ODD\_PSRST#

3D3V\_S0

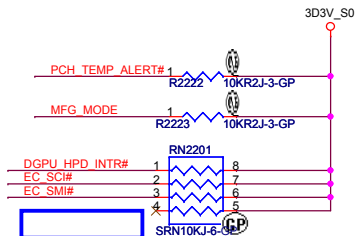
RN2203

SRN10KJ-5-GP

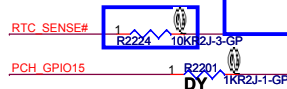
H\_A20GATE

H\_RCIN#

11/11 Remove R2220 for GPIO48 set to GPO

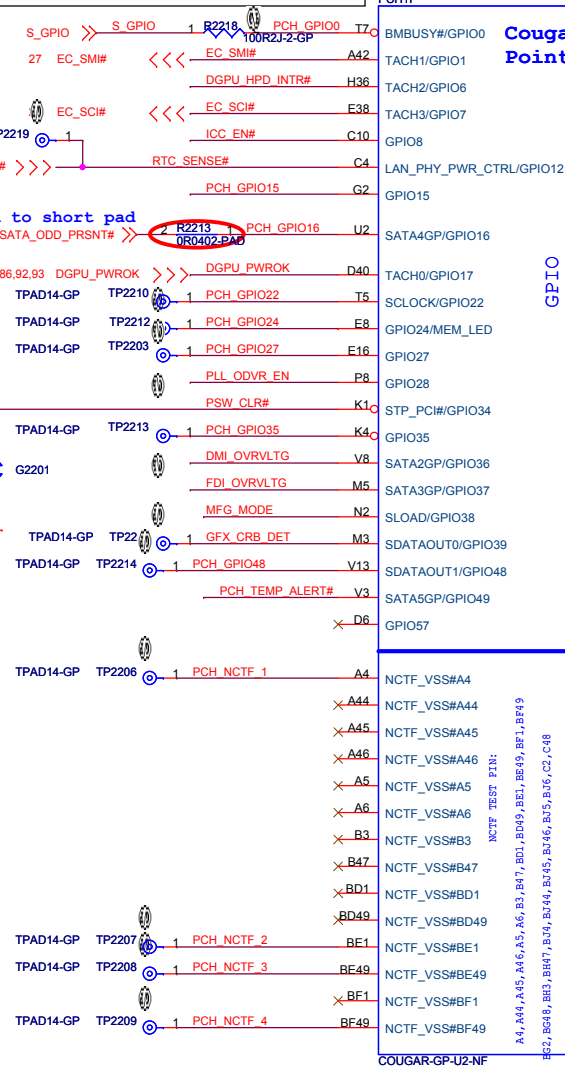


12/1 Add R2224 pull high



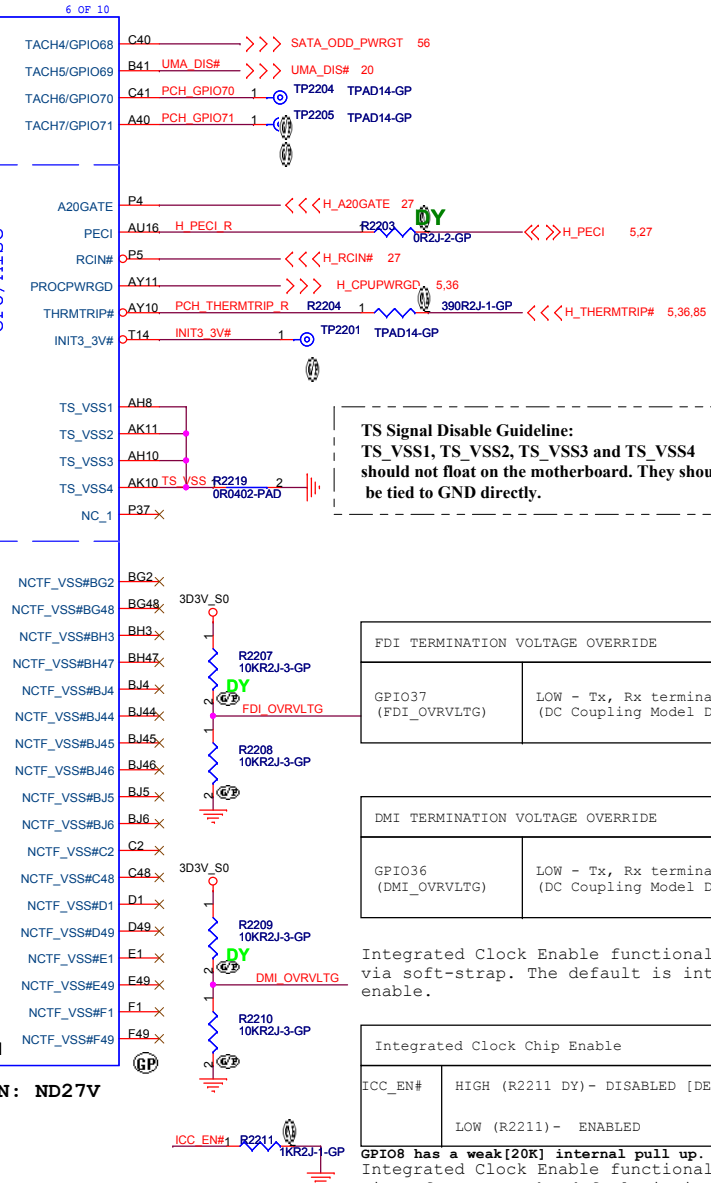
11/15 Remove Rn2204

11/ 17 Dummy R2201 because GPIO15 internal PH



NCIF TEST PIN:  
A4, A44, A45, A46, A5, A6, B3, B47, BDI, BD49, BE1, BE49, BF1, BF49  
C, C648, BH3, BH47, B34, B44, B45, B346, B35, B36, C2, C48  
D, D1, D49, E1, E49, F1, F49

P/N: ND27V



FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT]  LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.  
Integrated Clock Enable functionality is achieved  
via soft-strap. The default is integrated clock  
enable.

PLL ON DIE VR ENABLE

NOTE: This signal has a weak internal pull-up 20K  
 ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT  
 DISABLED -- LOW (R2212 STUFFED)

PLL\_ODVR\_EN **DY** 1 R2212 1K02 L1-CP

### <Core Design>



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**PCH (GPIO/CPU)**

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A3

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## Enrico Caruso 14

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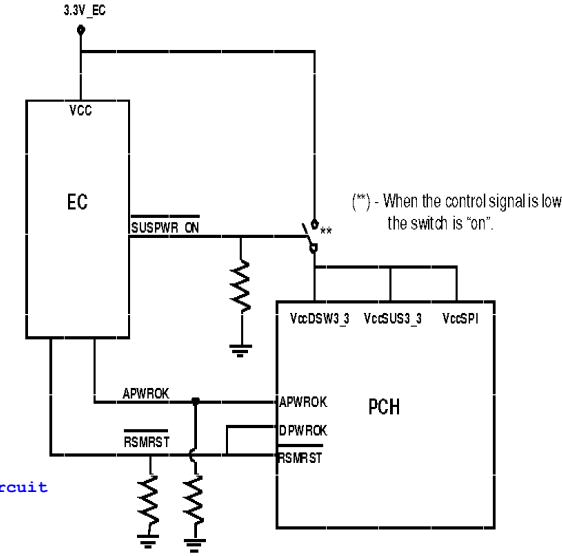


SSID = PCH 6A

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and change L2301 source to 3D3V\_DAC\_S0

Voltage Rail	Voltage	Iccmax
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLb	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.1	0.042
VccIO3	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW3_3	3.3	0.002
VccDFTerm	1.8	0.19
VccRTC	3.3	6u
VccSus3_3	3.3	0.097
VccSusHDA	3.3	0.01
VccVRM	1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS3	1.8	0.06

Refer to NPCE795 shared SPI flash architecture



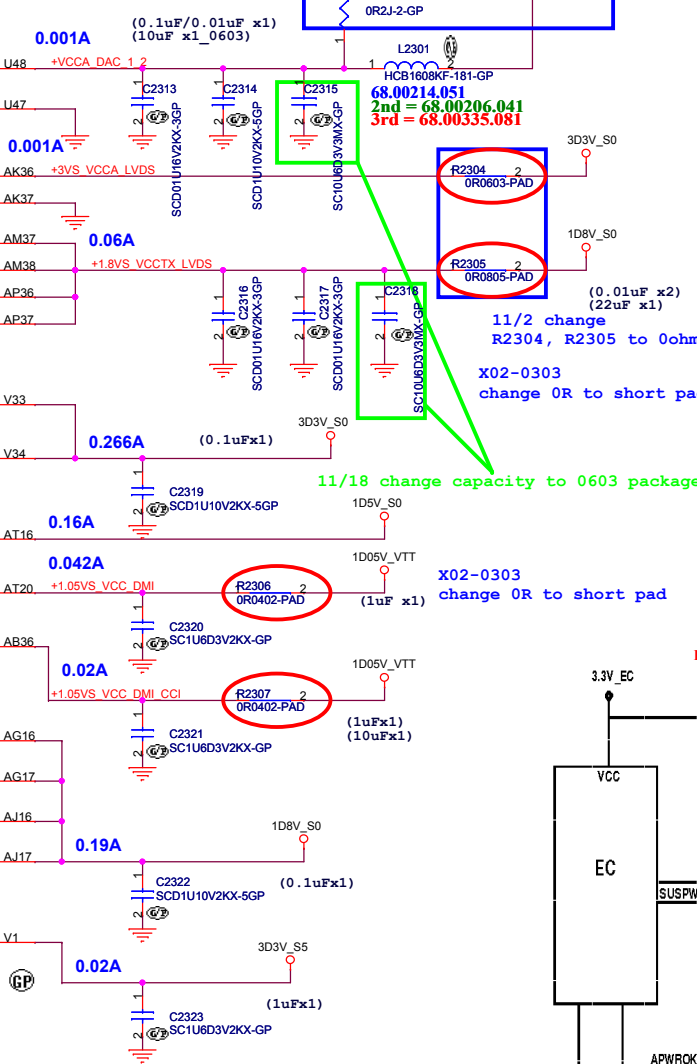
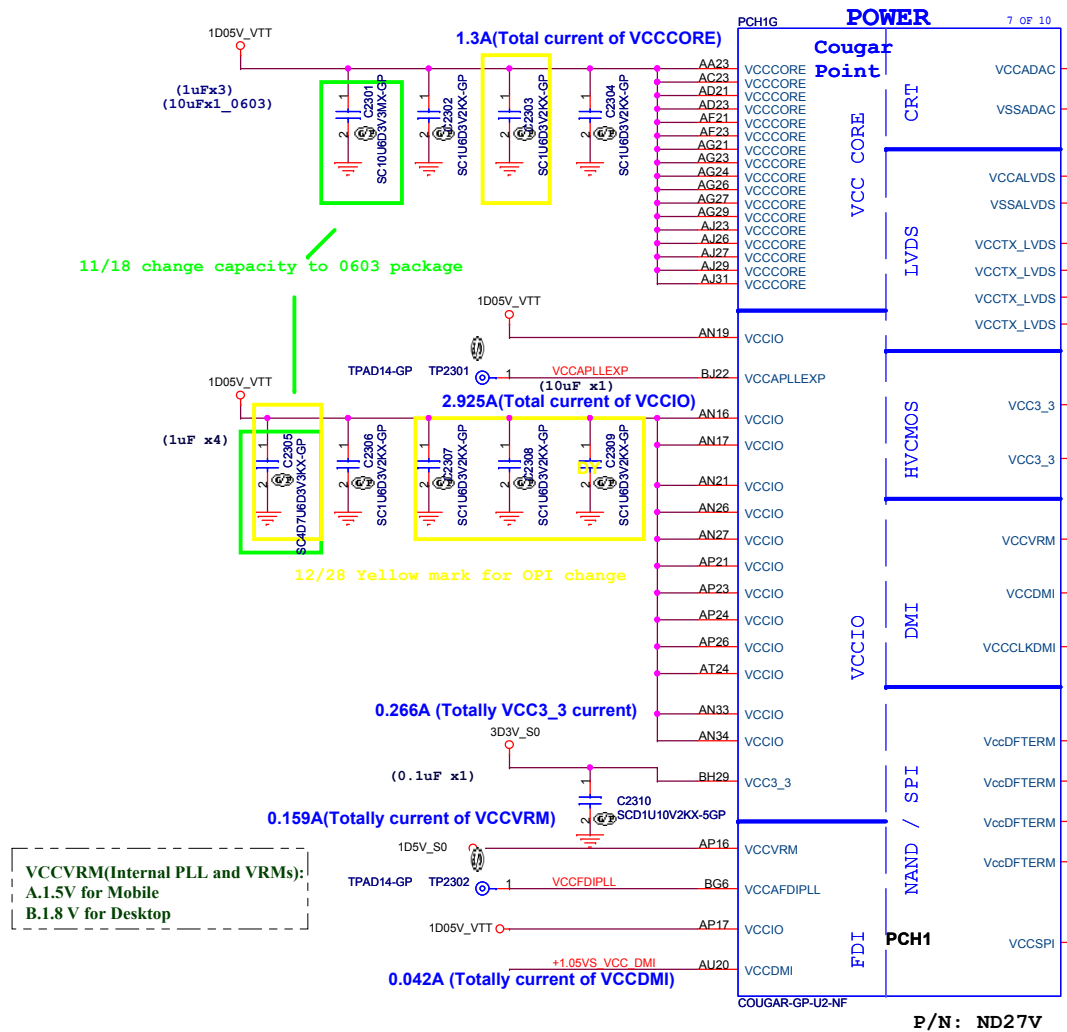
<Core Design>

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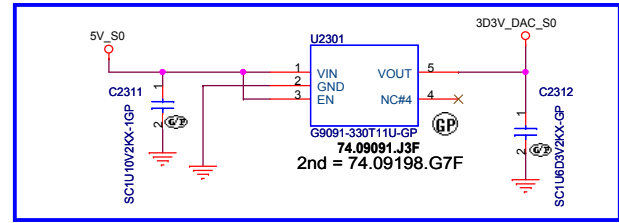
Title: **PCH (POWER1)**

Size: A3 Document Number: **Enrico Caruso 14** Rev: **A00**

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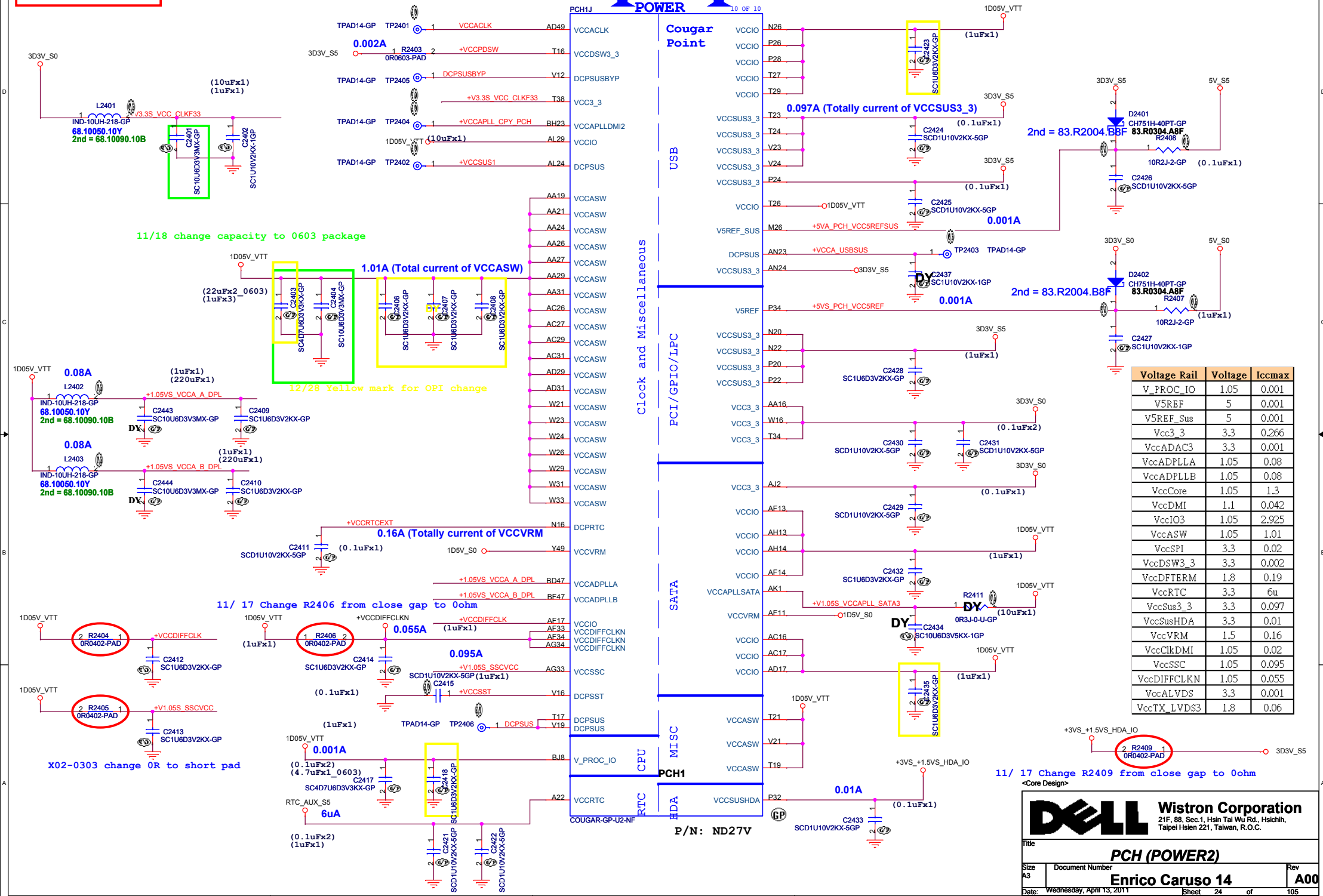
11/3 Add LDO for CRT DAC power  
11/ 17change U2301 Vout power rail and stuff the circuit



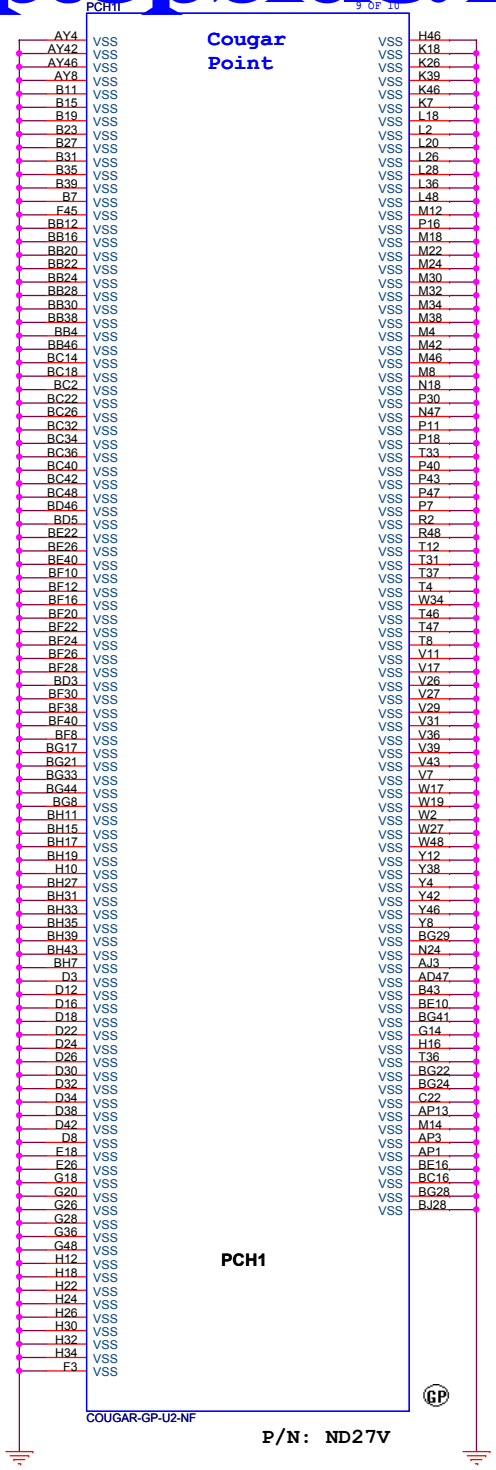
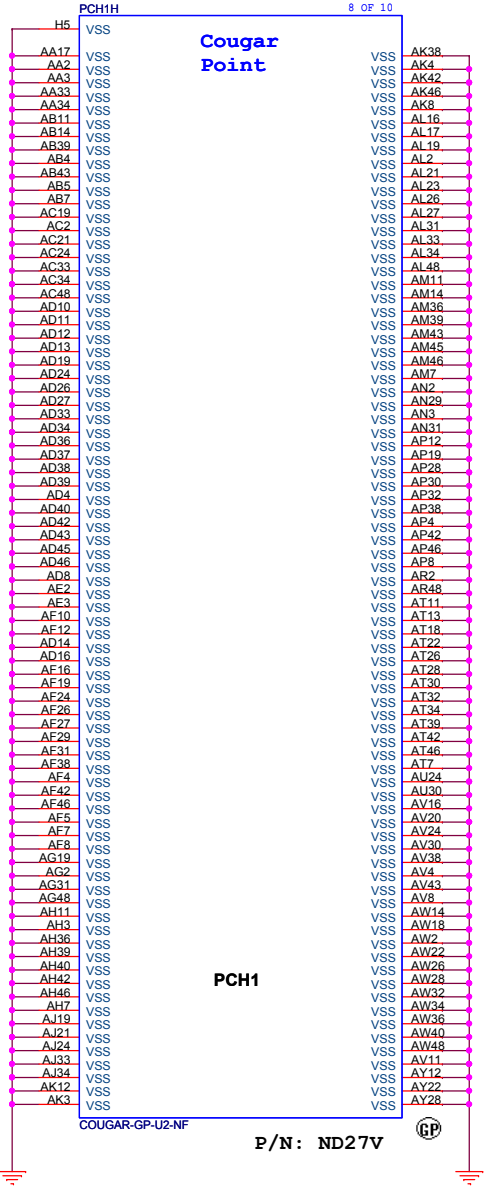
VCCVRM(Internal PLL and VRMs):  
A.1.5V for Mobile  
B.1.8 V for Desktop

(\*\*) - When the control signal is low, the switch is "on".

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SSID = PCH



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Title: **PCH (VSS)**

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[illegible]

SSID = Thermal

Thermal sensor P2800

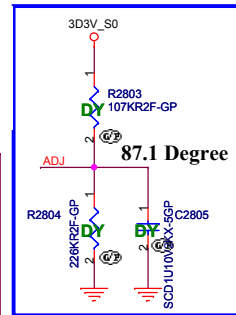
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Fan controller P2793

Option 1: OTZ=95°C → ADJ=3.3V

Option 2: OTZ=85°C → ADJ=Floating

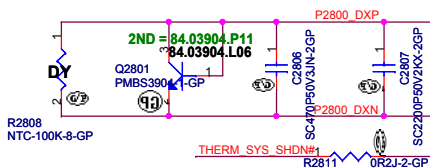
Option 3: OTZ=90°C → ADJ=GND



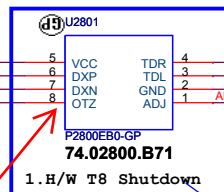
87.1 Degree

12/14 dummy R2803, R2804 and C2805

Layout notice :  
Both DXN and DXP routing 10 mil  
trace width and 10 mil spacing.



2.System Sensor, Put on palm rest

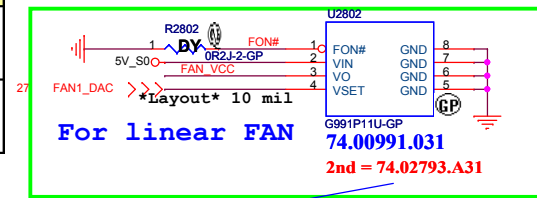


Very Close to CPU1

SYS\_THRM 27  
CPU\_THRM 27

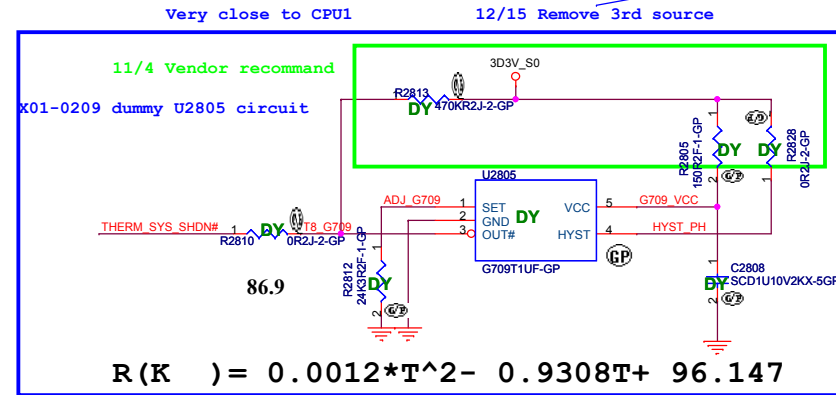
$$R(K) = 0.0012 * T^2 - 0.9308T + 96.147$$

	Pin-1	Definition
P2793A	/FON	Low(<0.4V): VOUT =Vin and the fan is fully-on High(>1.6V): VOUT=1.6*VSET This pin is internal Pull-High with ~500K ohm
P2793B	EN	Low(<0.4): IC is shutdown. High(>1.6V): VOUT=1.6*VSET This pin is internal Pull-High with ~500K ohm



For linear FAN

74.00991.031  
2nd = 74.02793.A31



Very close to CPU1

12/15 Remove 3rd source

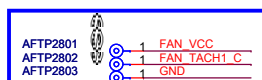
11/4 Vendor recommend

X01-0209 dummy U2805 circuit

THERM\_SYS\_SHDN# 1  
T8 G709

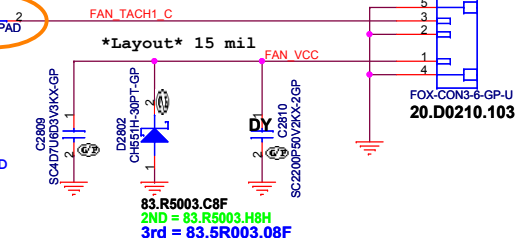
86.9

27 FAN\_TACH1 <<<



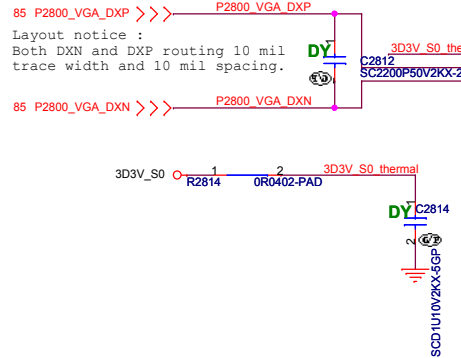
X02-0309 change AFTP to followDV14 AMD

12/13 change P2800 to ver B



83.R5003.C8F  
2ND = 83.R5003.H8H  
3rd = 83.5R003.08F

VGA Thermal sensor P2800



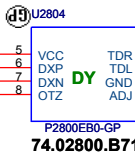
85 P2800\_VGA\_DXP >>>

P2800 VGA\_DXP

Layout notice :  
Both DXN and DXP routing 10 mil  
trace width and 10 mil spacing.

85 P2800\_VGA\_DNX >>>

P2800 VGA\_DNX

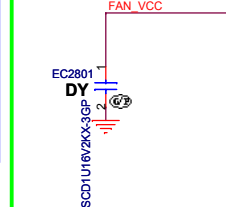


X02-0311 Add R2816& R2817 to  
option VGA\_THRM  
and DY the circuit

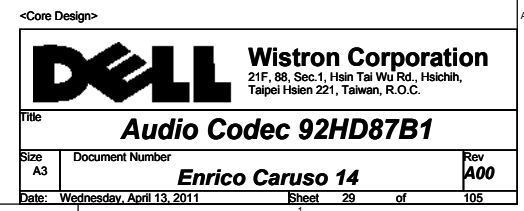
11/18 remove R2817, R2818, C2816  
and NC U2804 OTZ pin

VGA\_THRM 27

EMI/ESD



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Title

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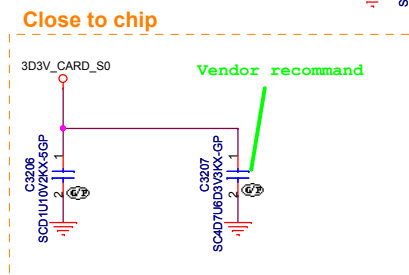
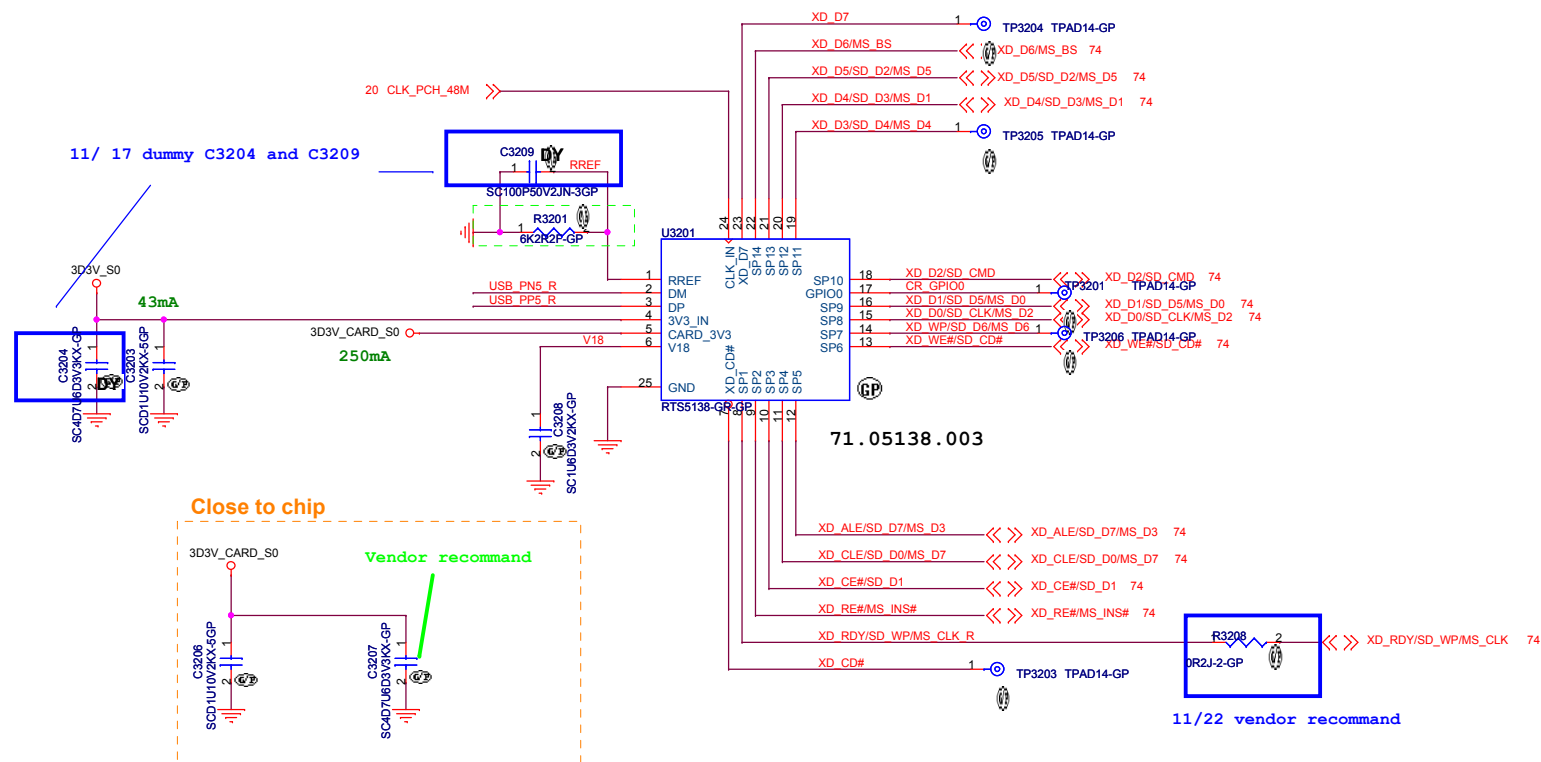
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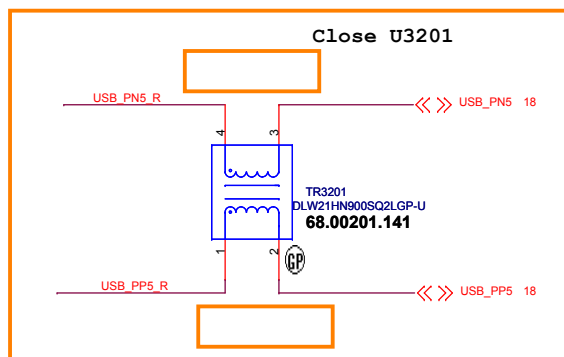
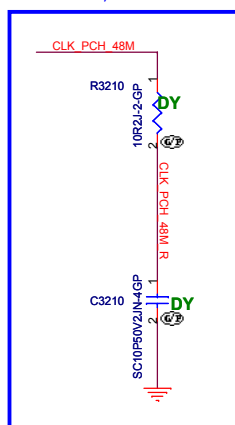


SSID = SDIO

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11/1 Add R3210, C3210 for EMI



X02-0311 stuff TR3201 and change symbol to 68.00201.141


A00-0324 change TR6102 to TR3201

A00-0406 remove R3206, R3207 PAD

<Core Design>

(Blanking)

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**Reserved**

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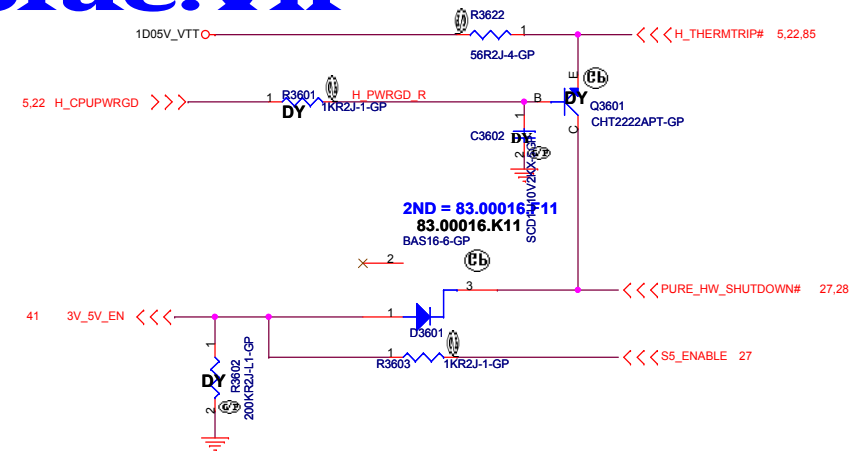
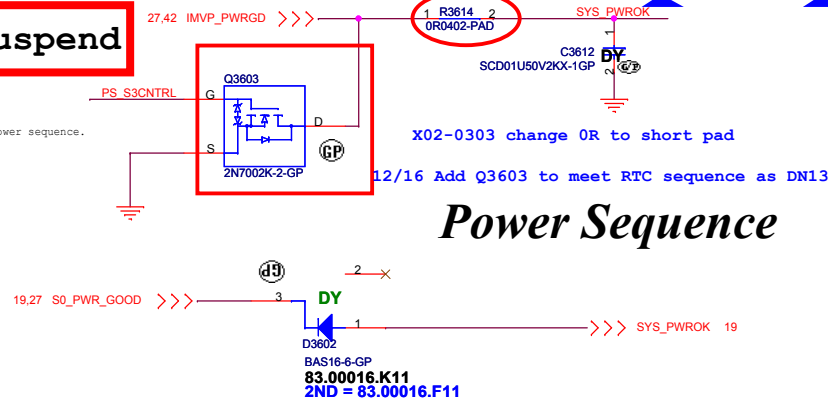
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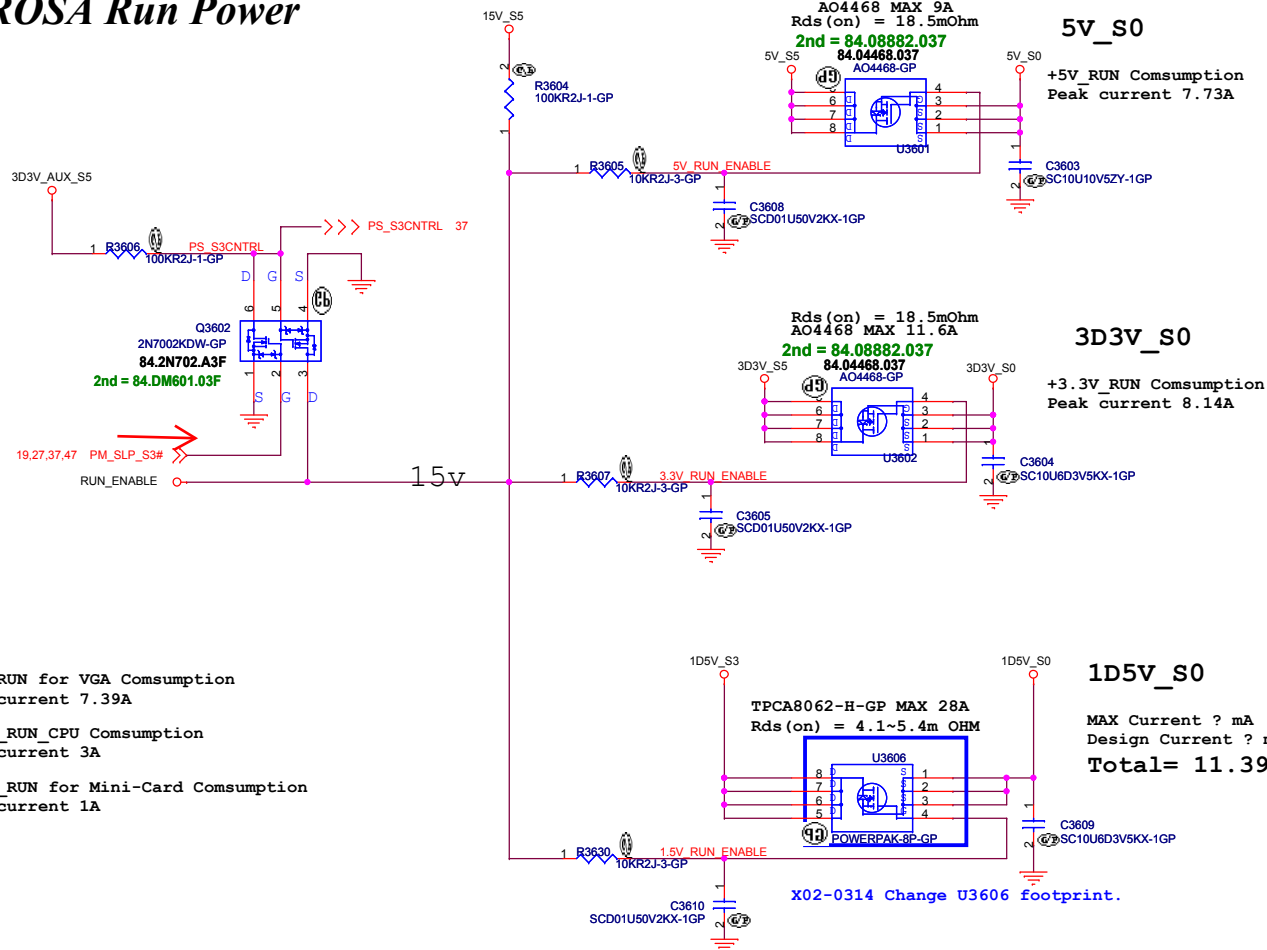
(Blanking)

SSID = Reset.Suspend

20101206 X02:  
Add Q3603 for RTC power sequence.



## ROSA Run Power



1.5V\_RUN for VGA Consumption  
Peak current 7.39A

+1.5V\_RUN\_CPU Consumption  
Peak current 3A

+1.5V\_RUN for Mini-Card Consumption  
Peak current 1A

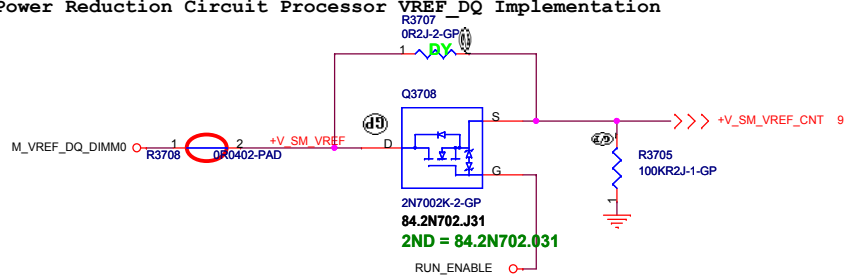
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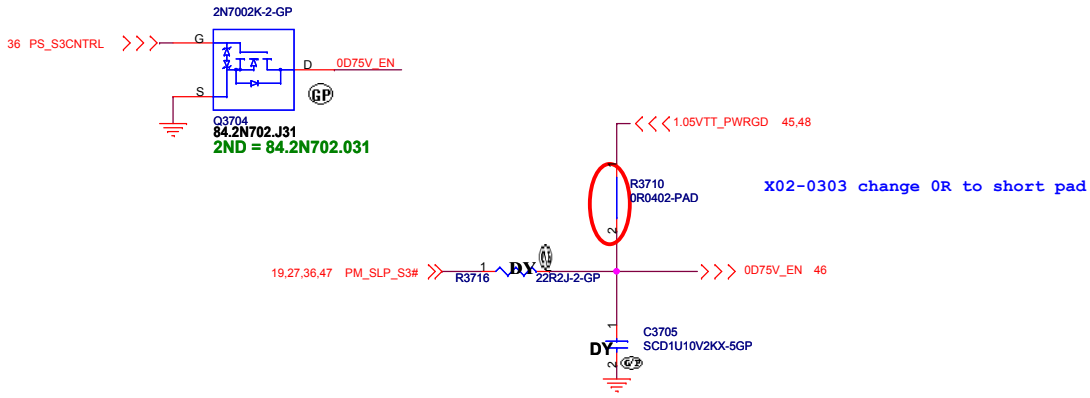
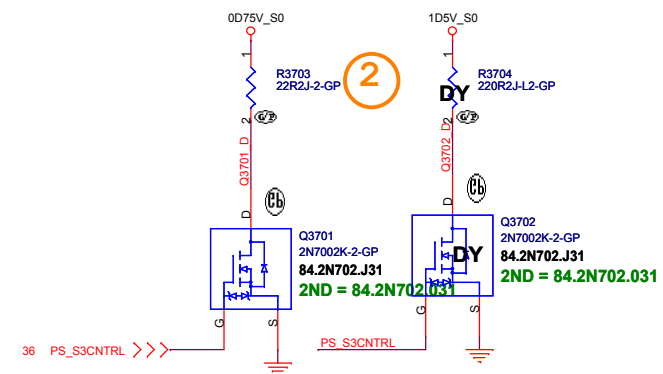
Title			<b>Power Plane Enable</b>	
Size	Document Number	Rev		A00
A3	<b>Enrico Caruso 14</b>		Sheet	36 of 105
Date:	Wednesday, April 13, 2011			



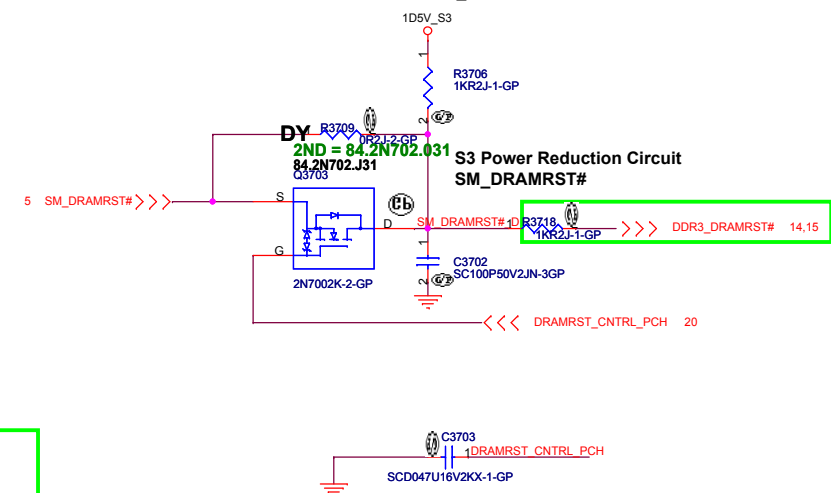
Close to CPU  
S3 Power Reduction Circuit Processor VREF\_DQ Implementation



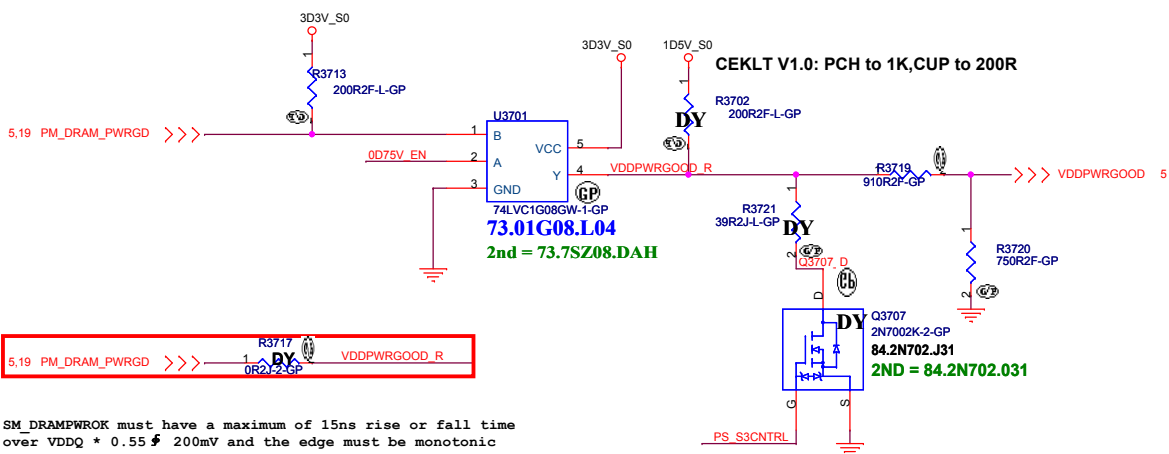
Close to DIMM  
S3 Power Reduction Circuit SM\_DRAMPWROK



Close to CPU  
S3 Power Reduction Circuit SM\_DRAMPWROK



Close to CPU  
S3 Power Reduction Circuit SM\_DRAMPWROK



SM\_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ \* 0.55 ± 200mV and the edge must be monotonic

SSID = PWR.Support

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DCin CONN

Modify 0923

X02-0314 Del short pad PAD1 to prevent system burn.

19,5V

11/25

12/2 change PD3801 to 83.P6SBM.DAG(CHENMKO)

X02-0309 Change AFTP to follow DV14 AMD

When PQ3801 is stuffed, the PR3806 need change to 2.2K 1% resistor

This cap should be used only as last resort for EMI suppression.

X01-0217 change PU3801 to 84.04407.G37

$I_d = -10A$   
 $Q_g = -22nC$   
 $R_{dson} = 14 \sim 30m\Omega$

<Core Design>



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Title

**DCIN Jack**

Size  
A3

Document Number

**Enrico Caruso 14**

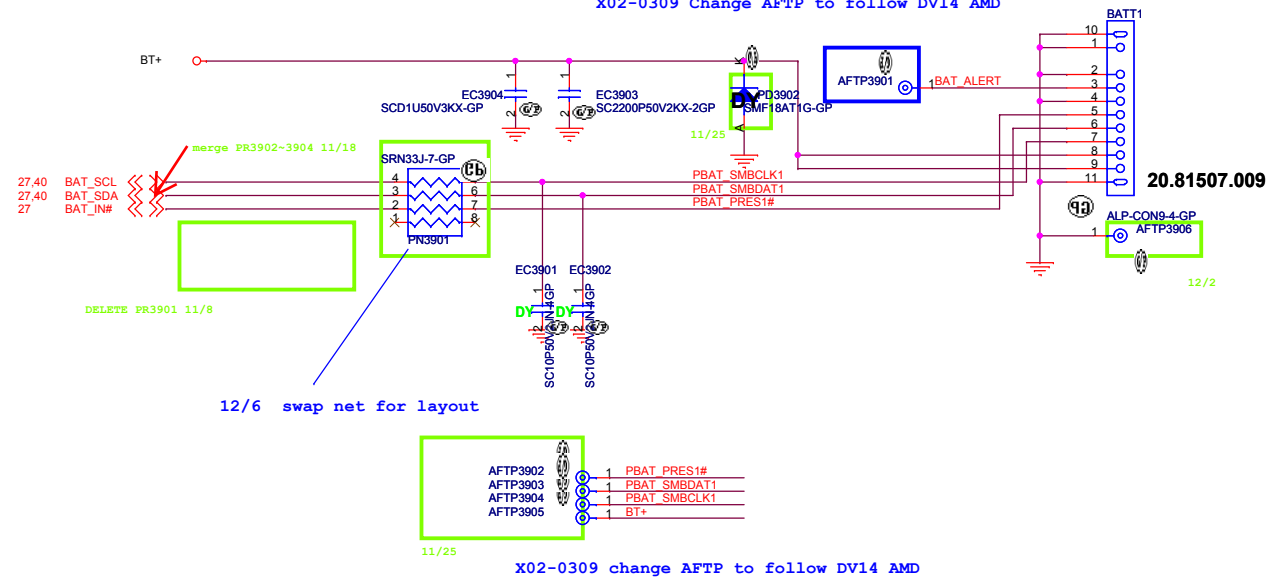
Rev

**A00**

Date: Wednesday, April 13, 2011

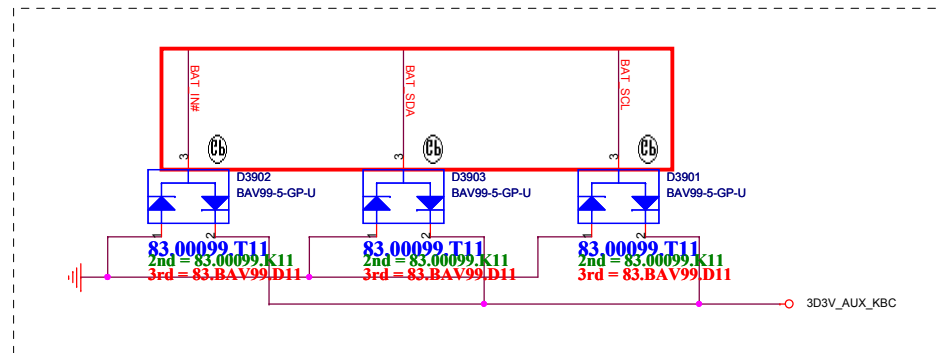
Sheet 38 of 105

X02-0309 Change AFTP to follow DV14 AMD



For actual location, need to be swap all pin

**Placement: Close to Batt Connector**



### <Core Design>



Title

**BATT CONN**

Size  
A3

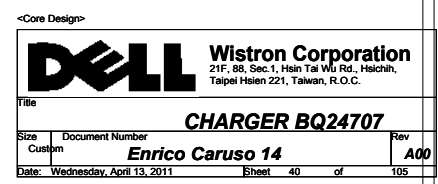
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**Enrico Caruso 14**

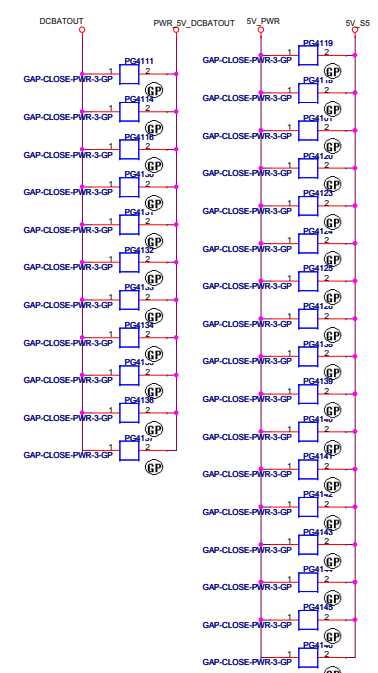
Rev  
**A00**

Date: Wednesday, April 13, 2011

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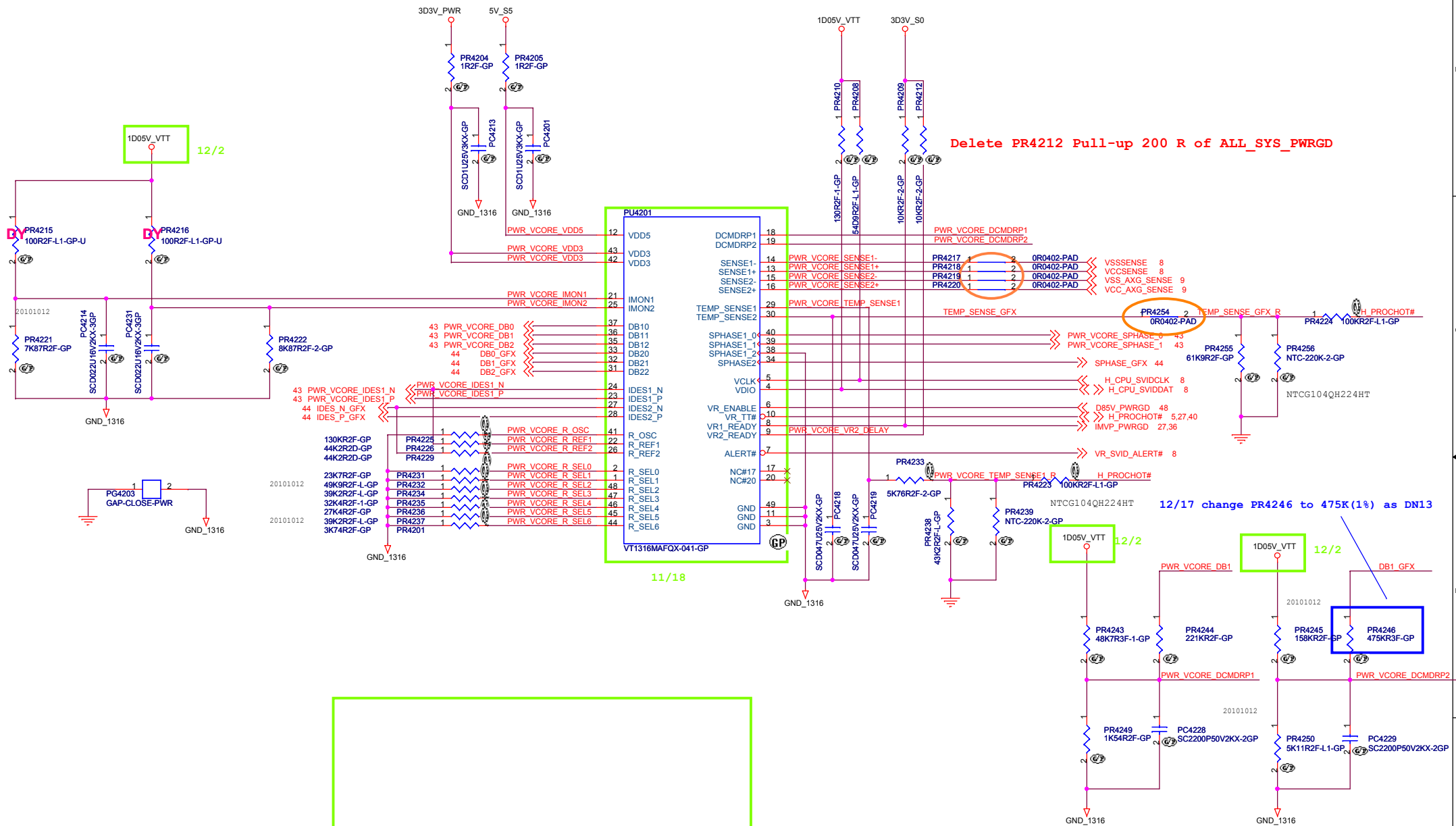


**www.laptopblue.vn**



SSID = CPU.Regulator

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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title			VT1316+1314 CPU CORE(1/3)	
Size	Document Number	Rev		A00
A3	Enrico Caruso 14			
Date:	Wednesday, April 13, 2011	Sheet	42	of 105

**VT1316+1314 CPU CORE(2/3)**

ev

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Sheet	44	of	105
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# TPS51218 for 1D05V

X01-0217 Change PR4501 to 78.7K(F)

84.00172.037  
BSZ115N03MSC  
Id=20A, Qg=9.8nC,  
Rdson=8.9 mohm

X02-0310 stuff EC4501

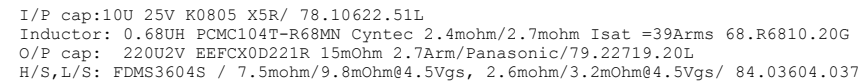
Design Current = 14.375A  
22.6A<OCP< 26.7A

79.33719.L01

$$V_{out} = 0.704V * (R1 + R2) / R2$$

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: 1.50UH PCMC104T Cyntec 3.8mohm/4.2mohm Isat =33Arms 68.1R510.10J  
O/P cap: 330U2V EEFSX0D331ER 9mOhm 3Arms Panasonic/79.33719.L01  
H/S: SiR172DP / 10.3mohm/12.4mOhm@4.5Vgs/ 84.00172.037  
L/S: SiR460DP / 0.49mohm/0.61mOhm@4.5Vgs/ 84.00460.037

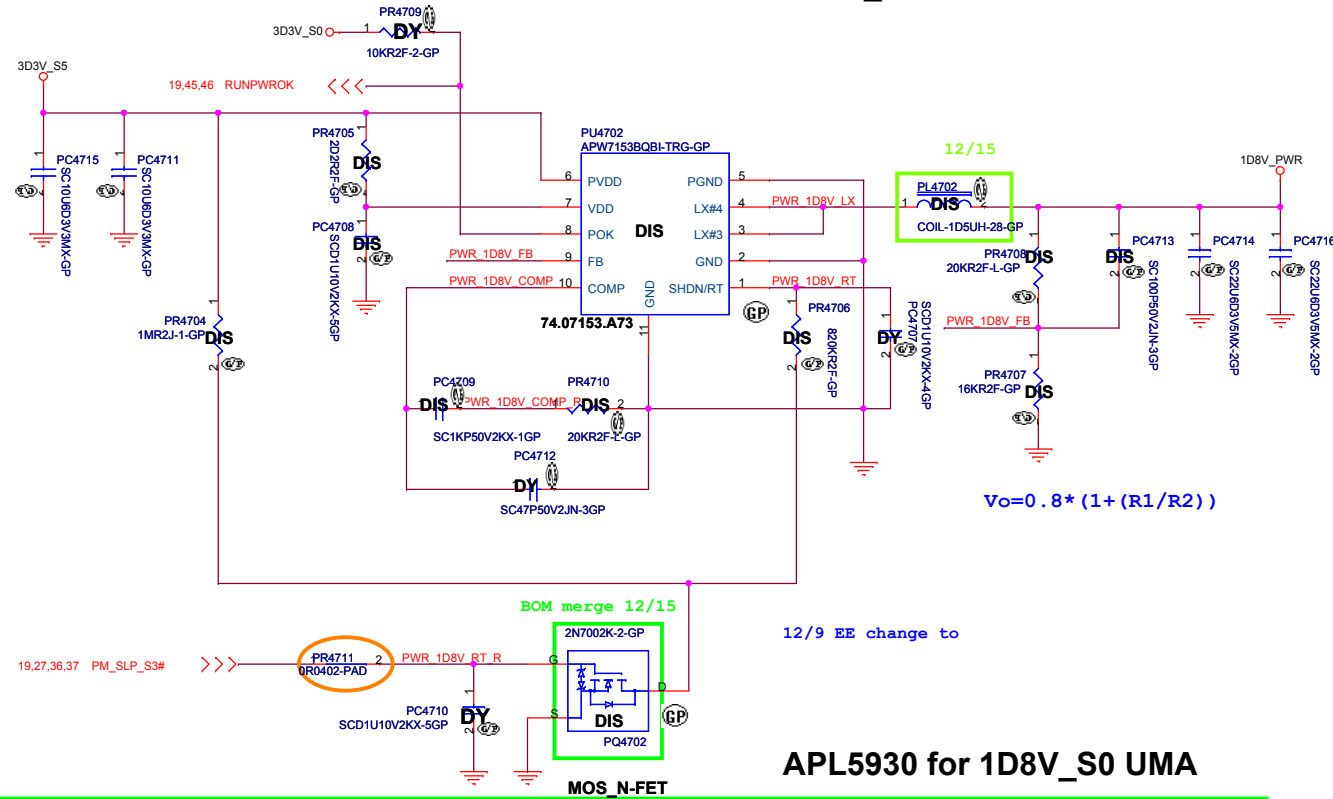
<Core Design>



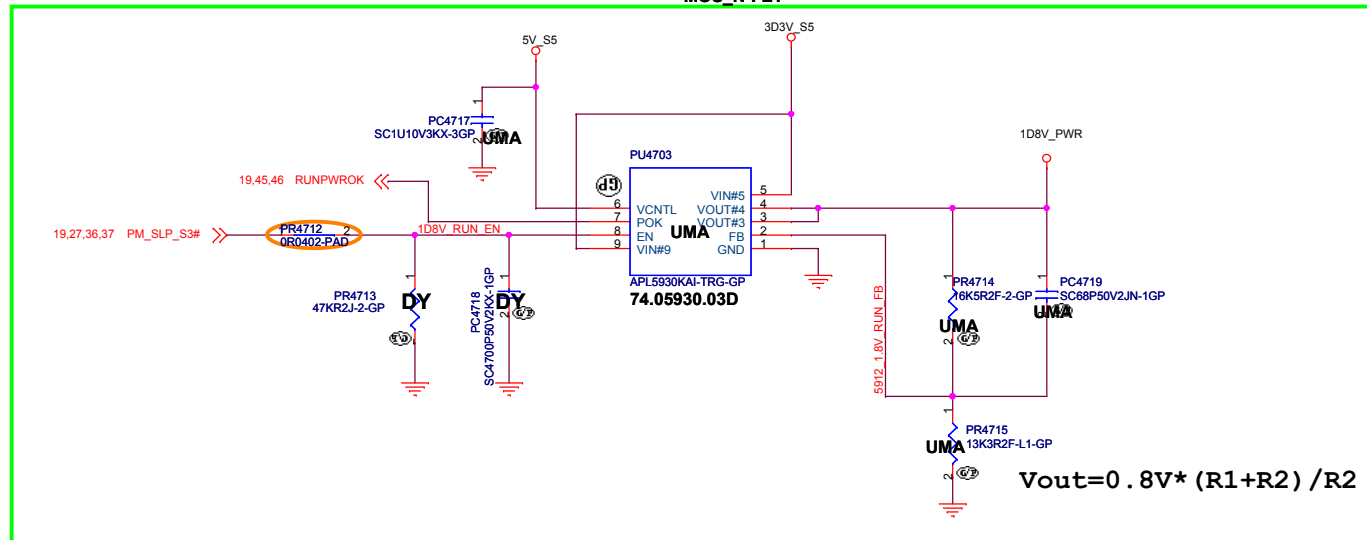
SSID = PWR.Plane.Regulator\_1p8v

APW7153B for 1D8V\_S0 DIS

+1.8V\_RUN  
Design current = 1.015A



APL5930 for 1D8V\_S0 UMA



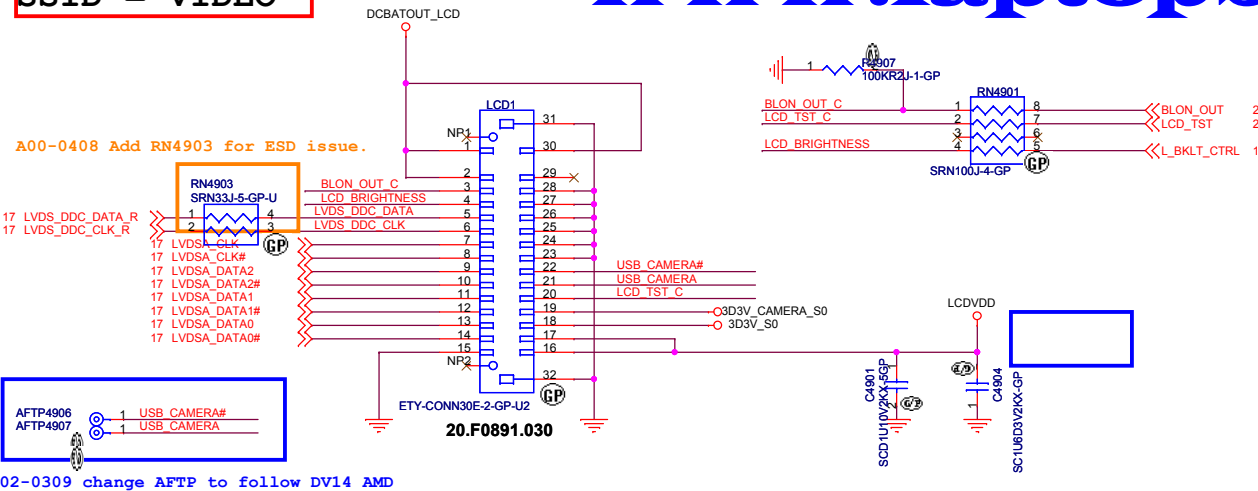
I/P cap: 4.7u 25V K0805 X5R/ 78.47522.51L  
O/P cap: 22u 25V M0805 X5R/ 78.22610.51L  
Inductor: 1.5u PCMC063T Cynotec 14mohm/15mohm Isat =18Arms 68.1R510.10K

<Core Design>

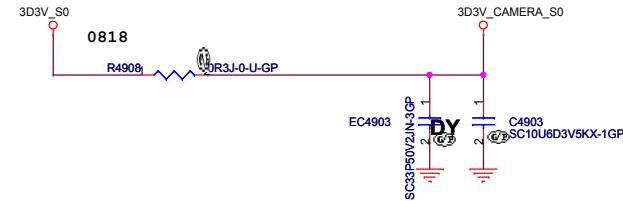
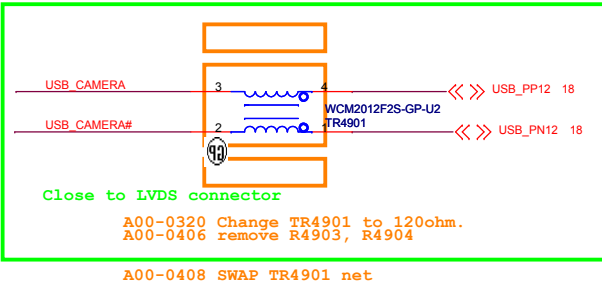
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b><i>APW7153B +1.8V_RUN</i></b>			
Size A3	Document Number	Rev	
<b><i>Enrico Caruso 14</i></b>		<b><i>A00</i></b>	
Date:	Wednesday, April 13, 2011	Sheet	47 of 105



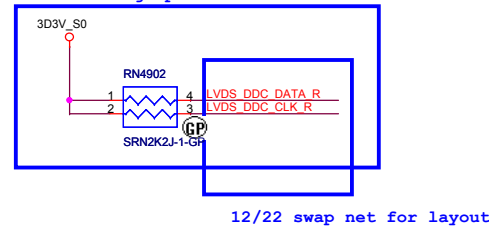
SSID = VIDEO



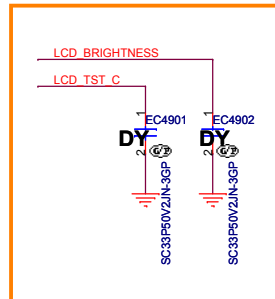
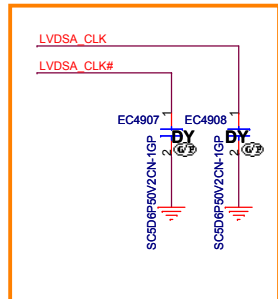
X02-0309 change AFTP to follow DV14 AMD



11/17 move RN1703 from P17 to P49  
and change part reference



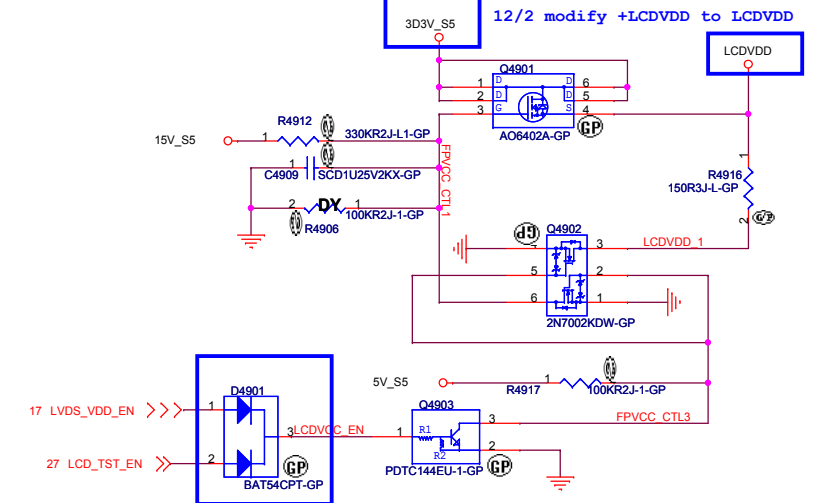
Close to LVDS connector



SSID = VIDEO

LCD POWER

11/15 change LCDVDD source from S0 to S5



<Core Design>

SSID = VIDEO

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11/3 Add RN5010 for CRT SMBus  
X02-0303 change 0R to short pad

11/ 17 Add RN5012 for SMBus pull high

X01: change RN5012 from 0R to 2.2K

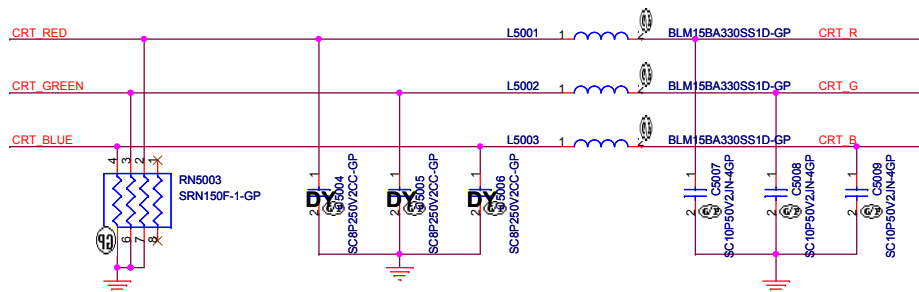
17 PCH\_CRT\_DDCDATA  
17 PCH\_CRT\_DDCCLK

5V Tolerance

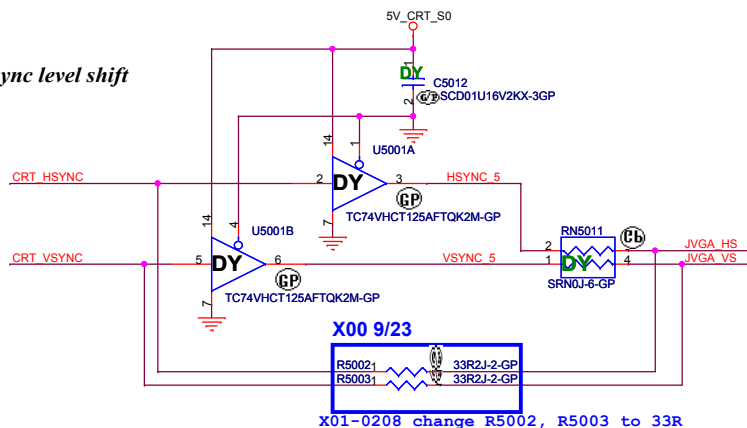
85 CRT\_GFX\_DDCDAT  
85 CRT\_GFX\_DDCCLK

Layout Note:

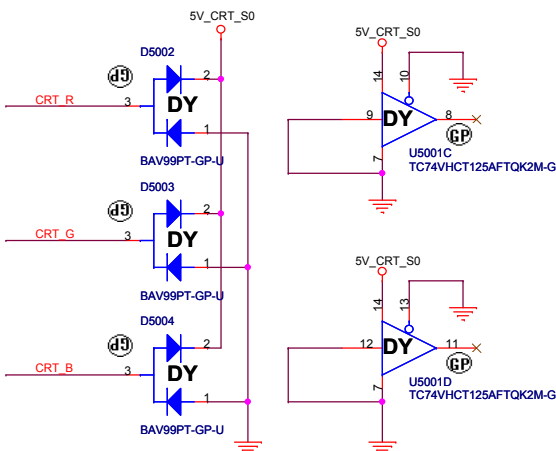
- \*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
- \* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.



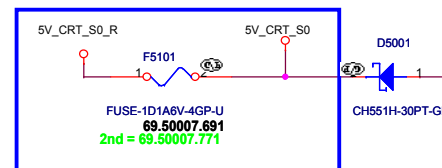
Hsync & Vsync level shift



X01-0208 change R5002, R5003 to 33R



11/18 change Fuse for CRT and HDMI share

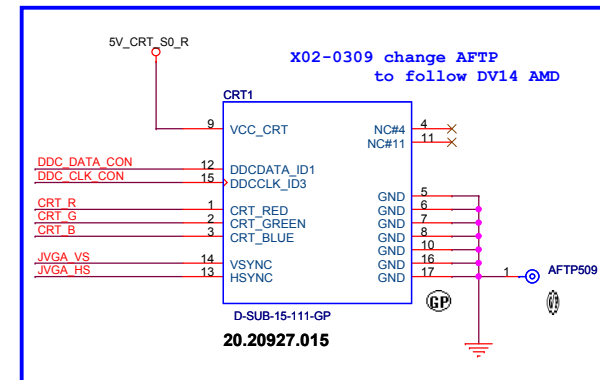


11/15 remove F5501 base on brazos result.  
11/ 17 Remove R5001



AFTP501  
AFTP502  
AFTP503  
AFTP504  
AFTP505  
AFTP506  
AFTP507  
AFTP508

11/29 change CRT1 to 20.20927.015





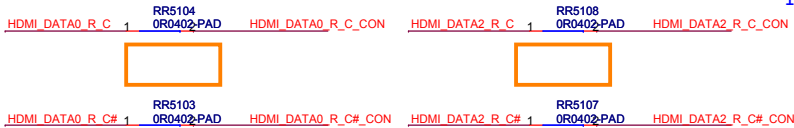
SSID = VIDEO

# HDMI Level Shifter & CONNECTOR

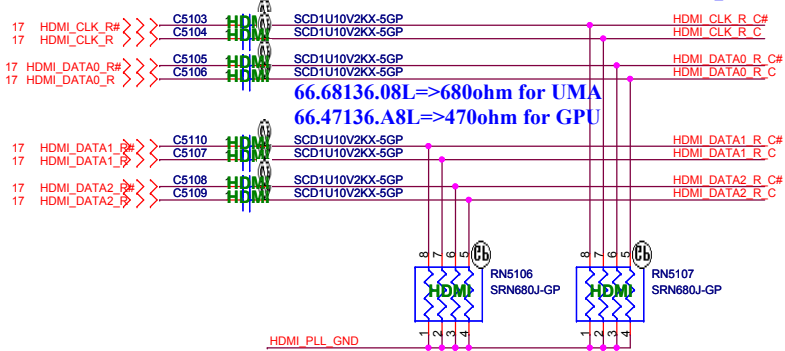
HDMI CONN



A00-0407 remove TR5101, TR5102, TR5103, TR5104 PAD and remove 0R PAD.

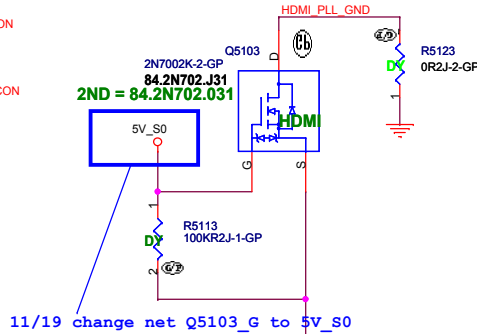


## HDMI DISCRETE/ UMA Co-lay

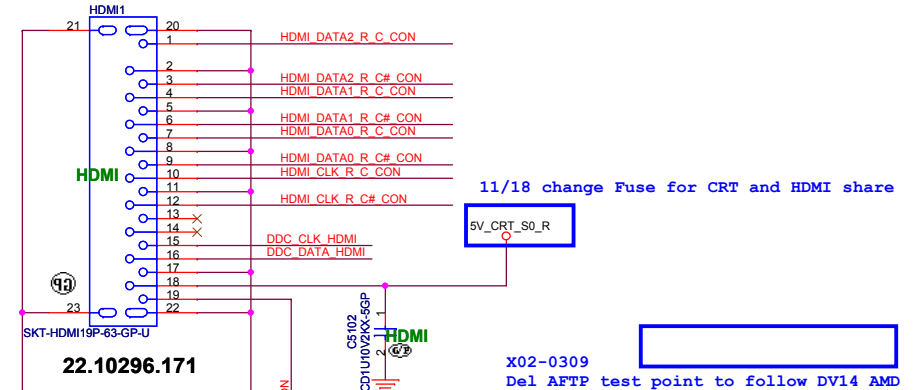


66.68136.08L=>680ohm for UMA  
66.47136.A8L=>470ohm for GPU

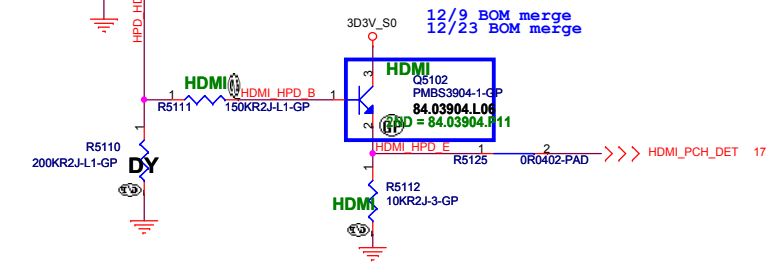
11/16 Del RN5112~5115 for no need to reserve for VGA



11/19 change net Q5103\_G to 5V\_S0



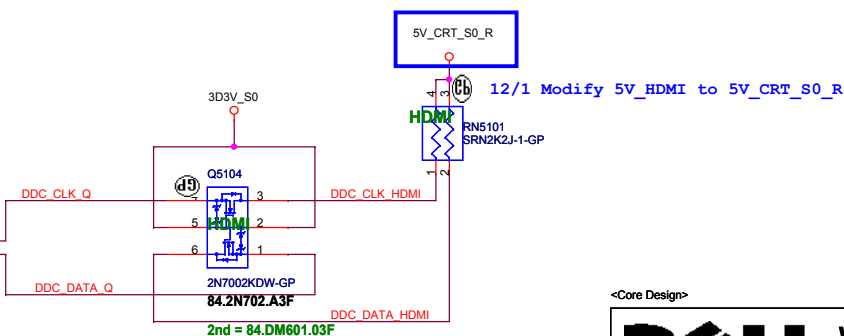
X02-0309 Del AFTP test point to follow DV14 AMD



11/18 change RN5117 BOM control property to HDMI

17\_PCH\_HDMI\_CLK  
17\_PCH\_HDMI\_DATA

X02-0303 change 0R to short pad



## Routing Guidelines:

CTRLDATA must be routed longer than CTRLCLK within 1000 mils (25.4 mm).  
The total delay on CTRLDATA should be longer than CTRLCLK.

<Core Design>

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Title: **HDMI Level Shifter/Connector**

Size A3 Document Number: **Enrico Caruso 14** Rev **A00**

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Title

**Reserved**

Size  
A3

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Rev  
**A00**


Date: Wednesday, April 13, 2011

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1

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**A00**

**LVDS\_Switch**

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Title

**Reserved**

Size  
A3

Document Number  
**Enrico Caruso 14**

Rev  
**A00**

Date: Wednesday, April 13, 2011

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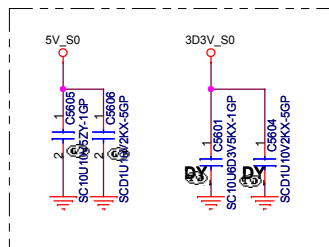
SSID = User.Interface

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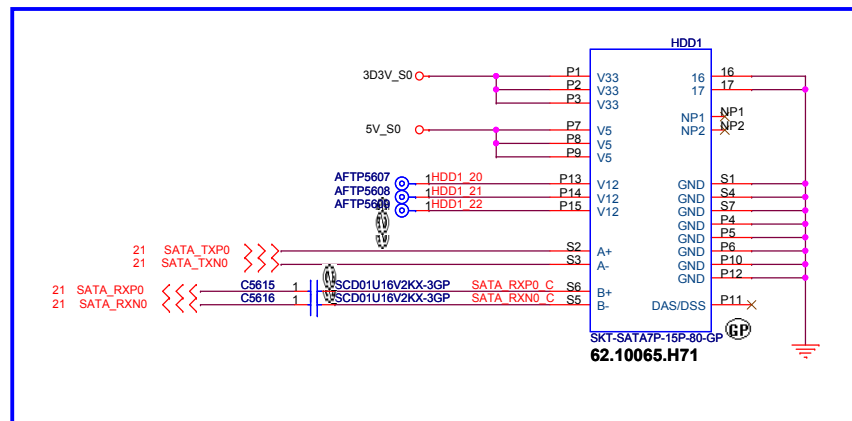
SSID = SATA

## SATA HDD Connector

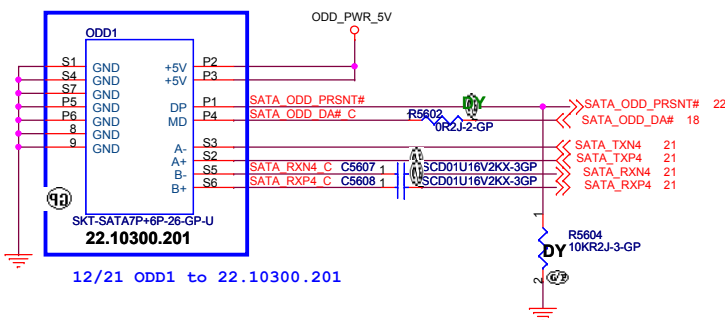
www.laptopblue.vn  
12/22 Change HDD1 CONN to 62.10065.H71



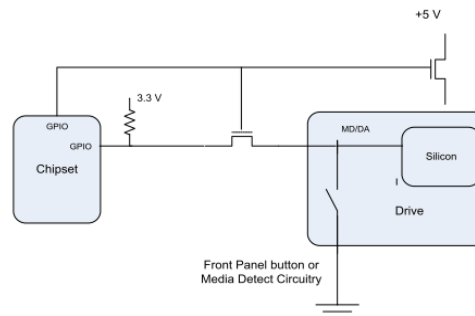
Close to HDD1



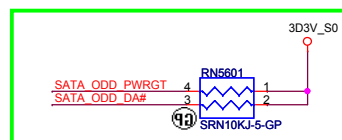
## ODD Connector



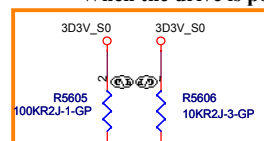
12/21 ODD1 to 22.10300.201



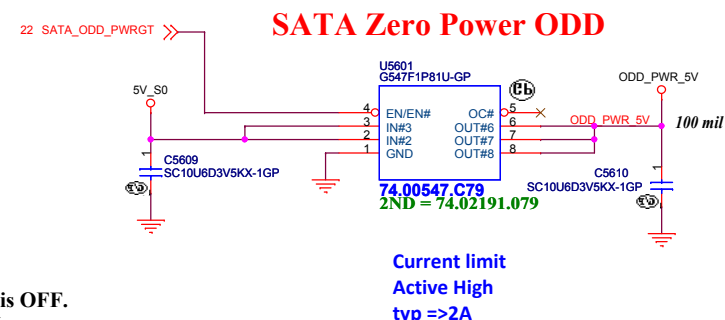
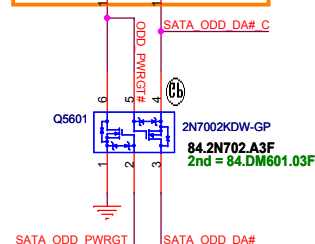
When the drive is powered on, the FET to the MD/DA pin drive is OFF.  
When the drive is powered off, the FET to the MD/DA pin is ON



SUPPORT ZERO SATA ODD



A00-0408 Add R5606 to pull high 3.3V\_S0  
Change pull high to 3.3V\_S0



<Core Design>

SSID = ESATA

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<Core Design>



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Title

ESATA

Size

A3

Document Number

Enrico Caruso 14

Date: Wednesday, April 13, 2011

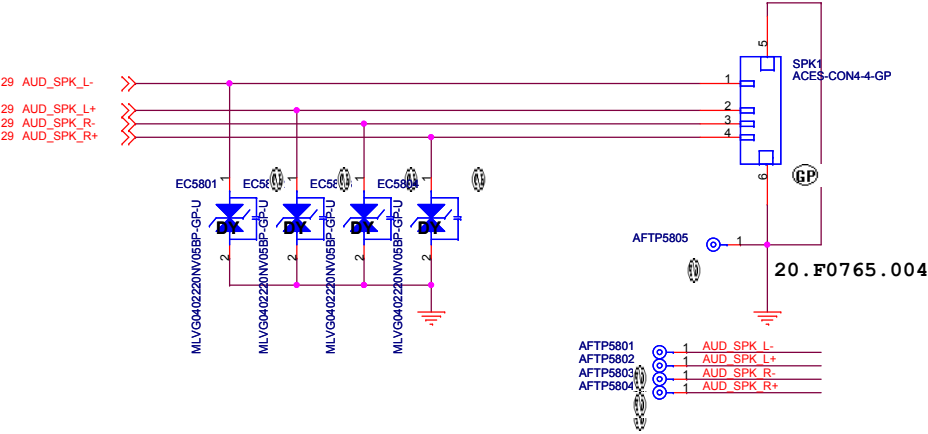
Rev

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Speaker Connector

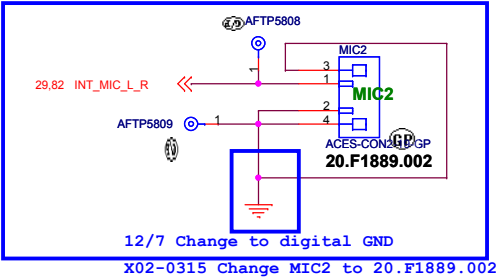


11/10 remove MIC1



11/26 reserve MIC2

12/7 change MIC2 to 20.F1050.002



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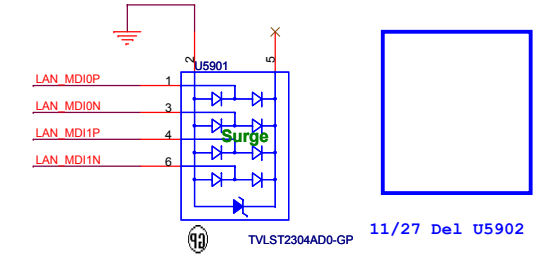
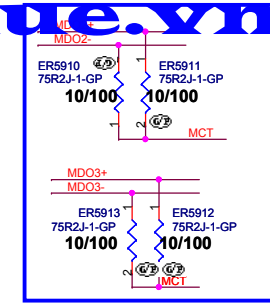
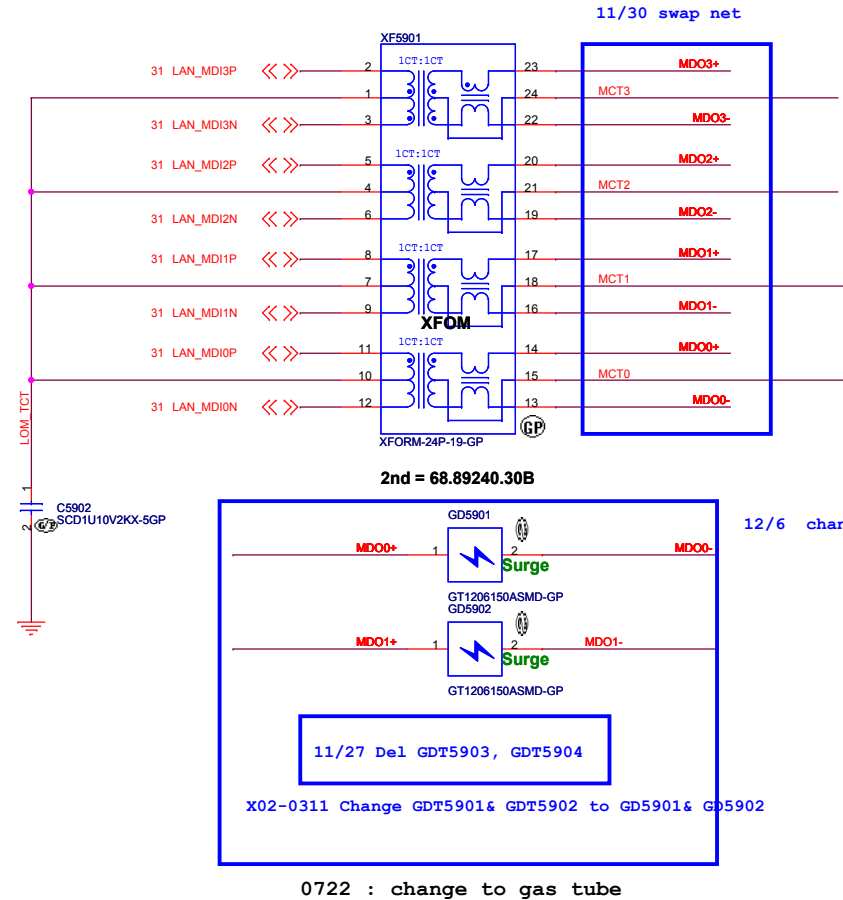
**Wistron Corporation**  
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Title			<b>SPEAKER CONN</b>	
Size	Document Number	Rev		
A3	<b>Enrico Caruso 14</b>	<b>A00</b>		
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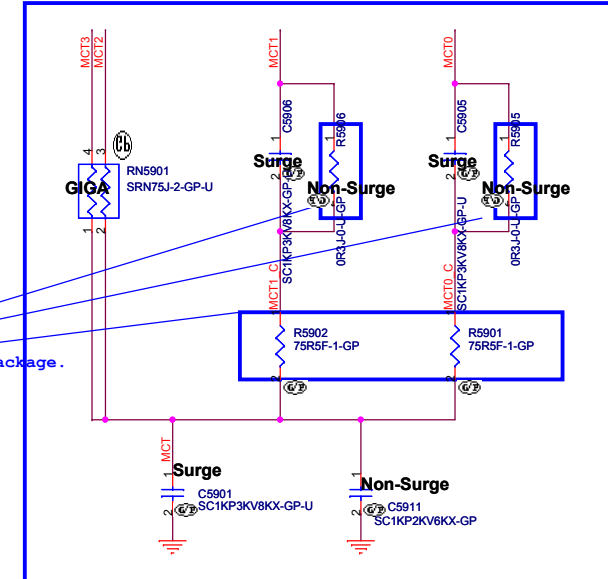
SSID = LOM

# LAN TransFormer

Giga Main: 68.IH601.301  
Giga 2nd: 68.05009.30A  
  
10/100 Main: 68.HH035.301  
10/100 Main: 68.01284.30A

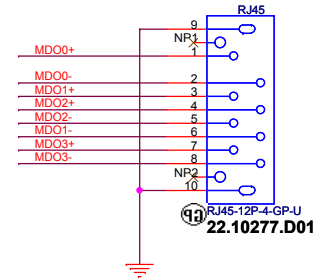


12/6 change resistor package.

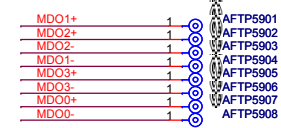


11/25 modify to CRC circuit and divided resistor as EMI suggest  
11/29 Change C5911 to 78.1022S.22L

## RJ45



11/29 change RJ45 to 22.10277.D01



SSID = Flash.ROM

## SPI FLASH ROM (4M byte) for PCH

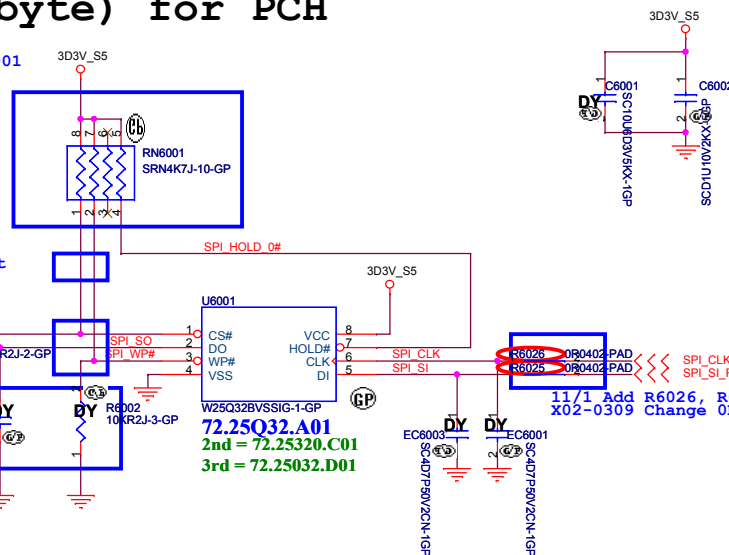
11/18 Merge R6003, R6004, R6005 to RN6001

12/6 swap net for layout  
X01-0211 swap CS#, WP# for layout

X01: modify CS#, WP#

21.27 SPI\_CS0#\_R  
21.27 SPI\_SO\_R

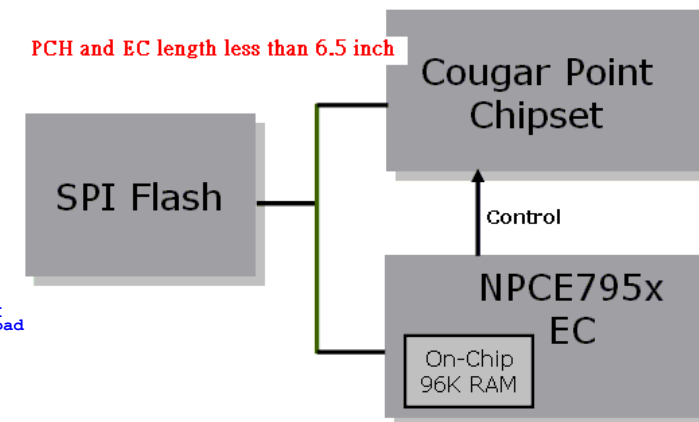
11/18 reserve R6002 for WP# and change  
change DO pin pull down to capacity



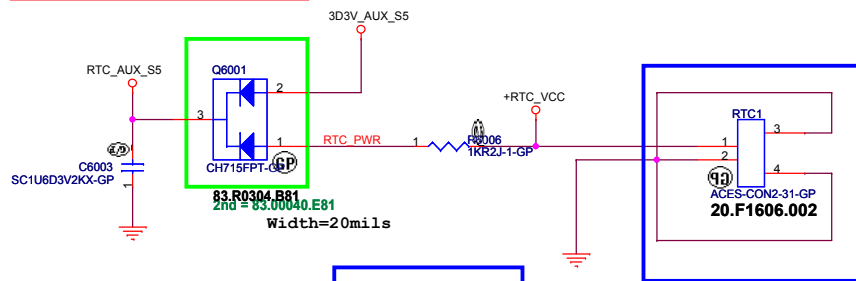
Priority	Wistron P/N	Manufacturer	Vendor P/N
1	72.25Q32.A01	WINBOND	W25Q32BVSSIG
2	72.25320.C01	MXIC	MX25L3206EM2I-12G
3	72.25032.D01	SST	SST25VF032B-80-4I-S2AF
4	72.25P32.C01	Numonyx	M25PX32-VMW6F

The total SPI interface signal between EC and PCH  
can't not exceed 6500mil. The mismatch between  
SPI signal must be within 500mil

PCH and EC length less than 6.5 inch

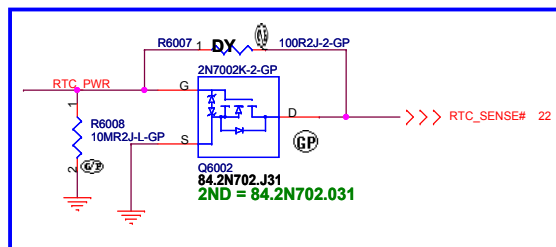


SSID = RBATT

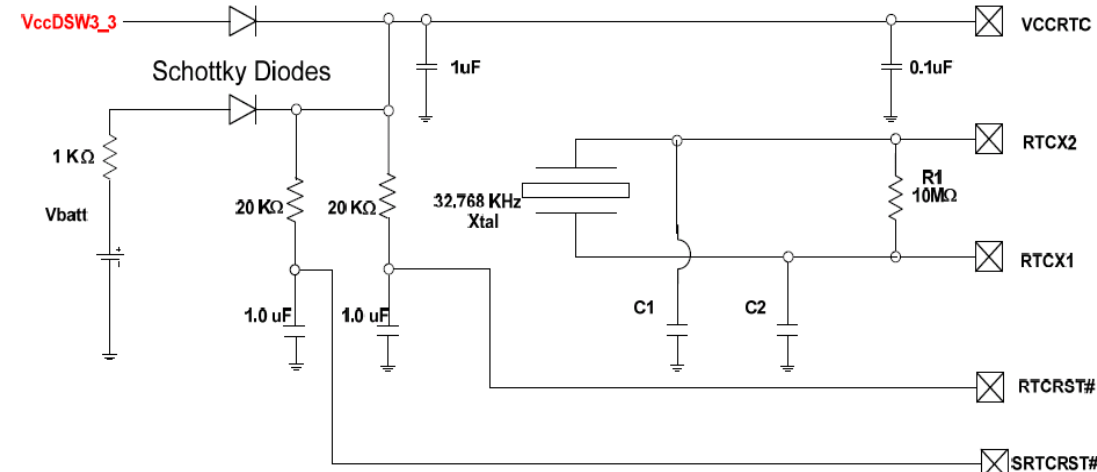


X02-0310 Del RTC AFTP to follow DV14 AMD

11/29 change RTC1 to 20.F1606.002



11/23 add RTC DET circuit



VccRTC is now connected to VccDSW3\_3  
through the Schottky diode instead of the 3.3V Sus well.

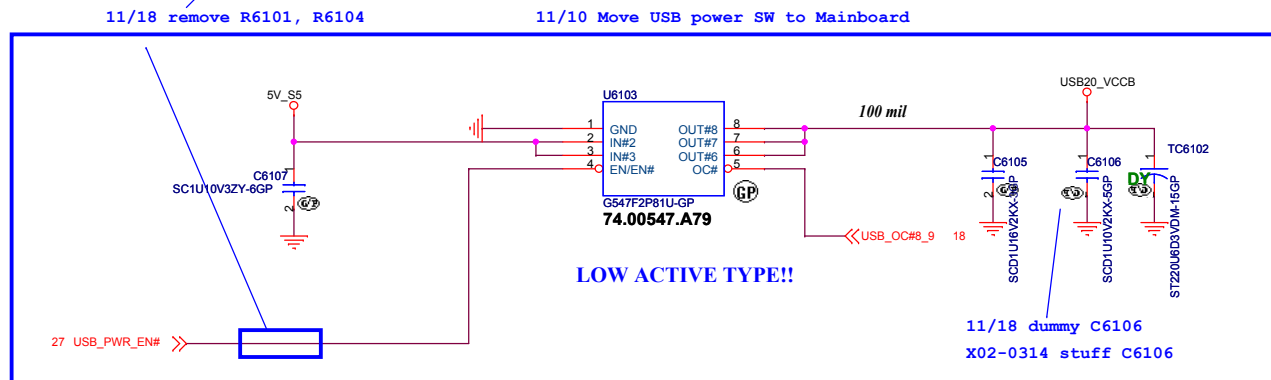
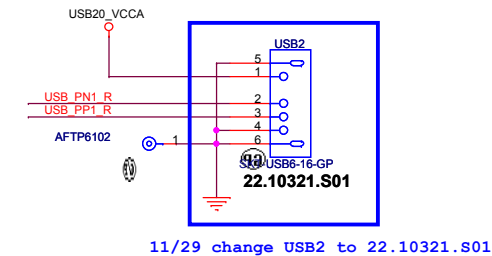
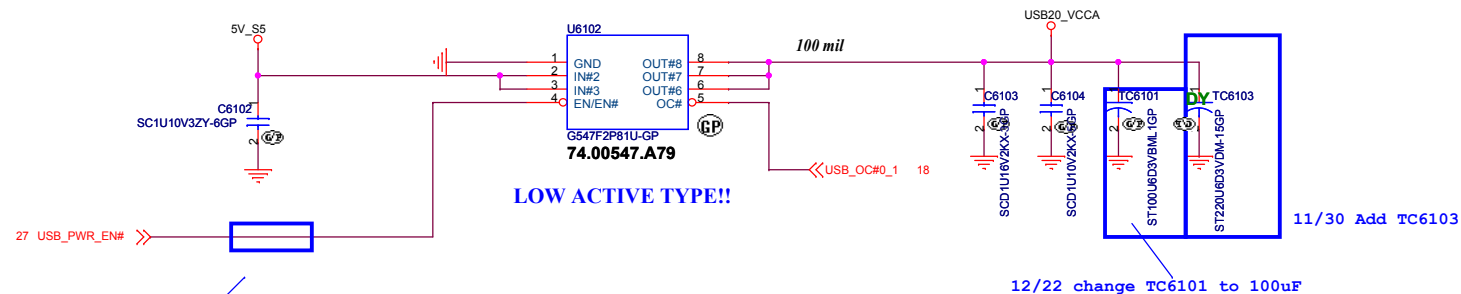
<Core Design>

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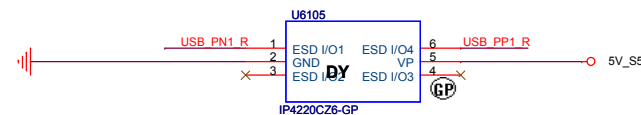
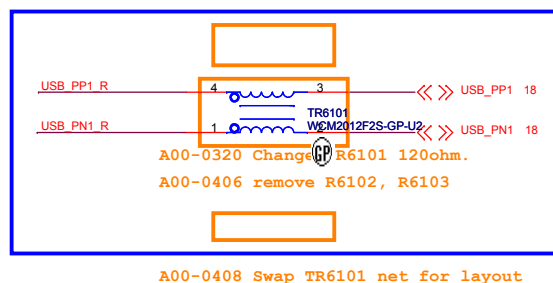
Title	Flash/RTC		
Size	Document Number	Rev	
A3	Enrico Caruso 14	A00	
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SSID = USB

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11/1 Stuff TR6101 for EMI



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: <b>USB Power SW</b>			
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SSID = User.Interface

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Title			
<b>Bluetooth</b>			
Size	Document Number		Rev
A3	<b>Enrico Caruso 14</b>		<b>A00</b>
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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

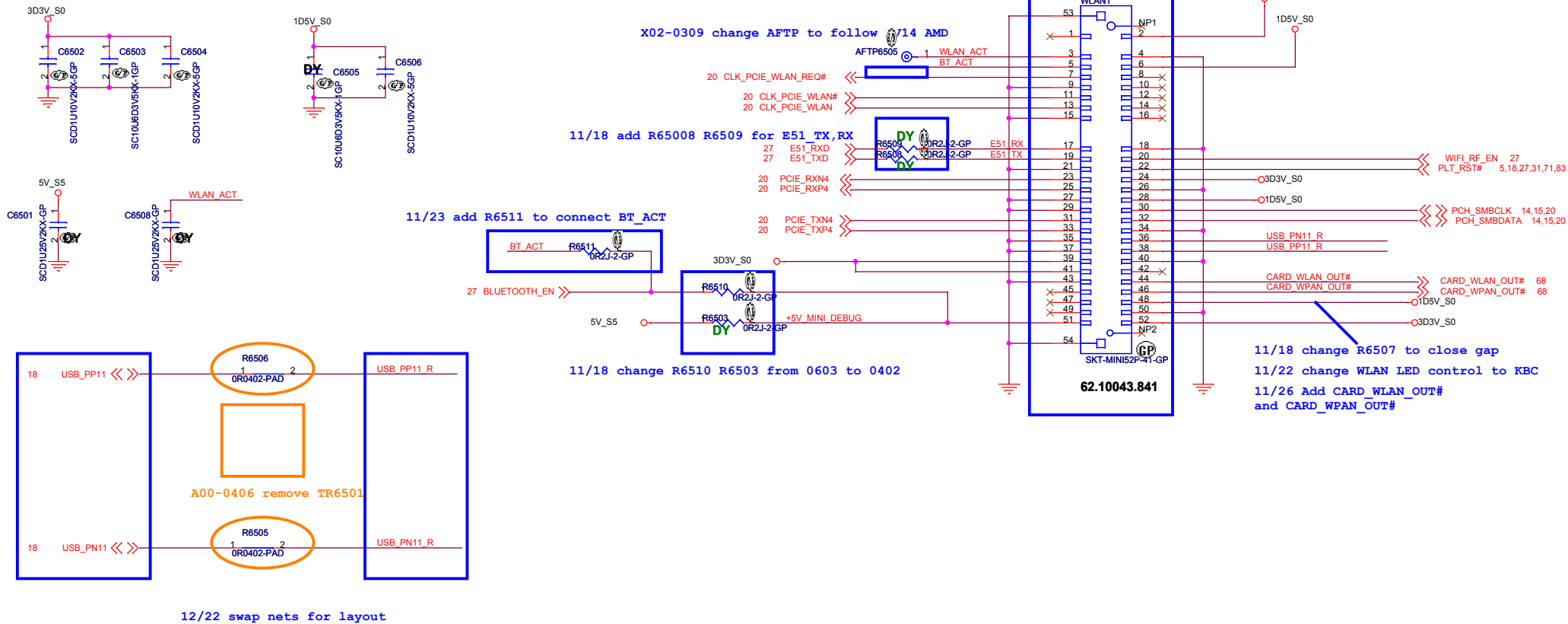
**RESERVED**

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SSID = Wireless

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Mini Card Connector(802.11a/b/g)



DN15ATI Whistler

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Title  
**MINICARD(WLAN)/ITP CONN**  
Size A3 Document Number  
**Enrico Caruso 14** Rev  
**A00**  
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DN15ATI Whistler



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Title

Size  
A3

Document Number  
**Enrico Caruso 14**

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**Reserved**

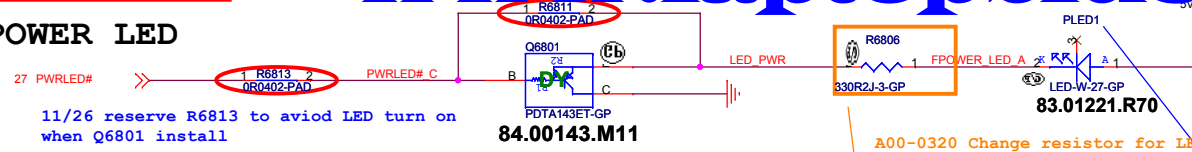
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DN15ATI Whistler

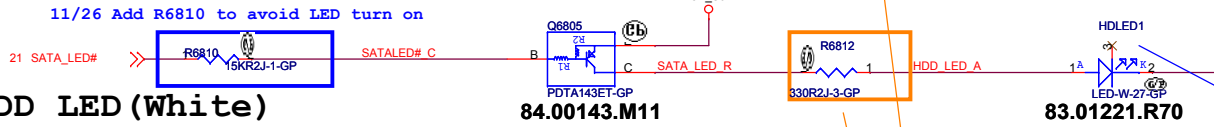
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Reserved</b>			
Size	Document Number		Rev
A3	<b>Enrico Caruso 14</b>		<b>A00</b>
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SSID = User.Interface

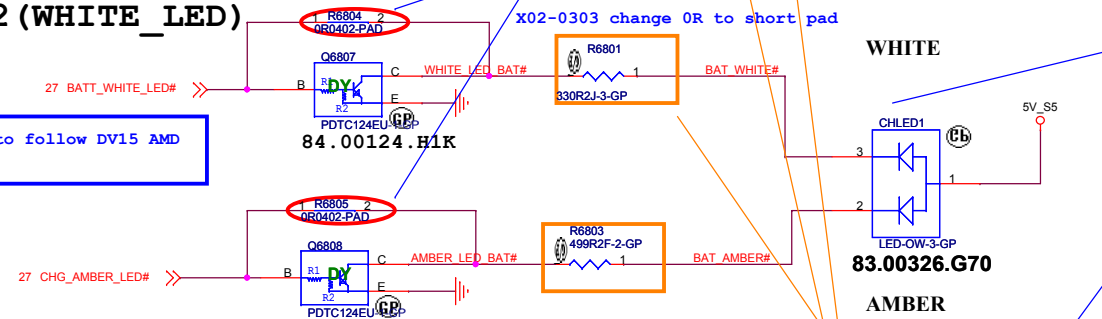
FRONT POWER LED



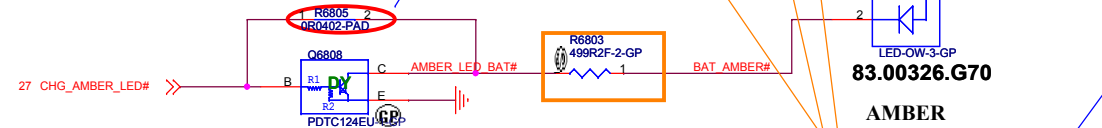
SATA HDD LED (White)



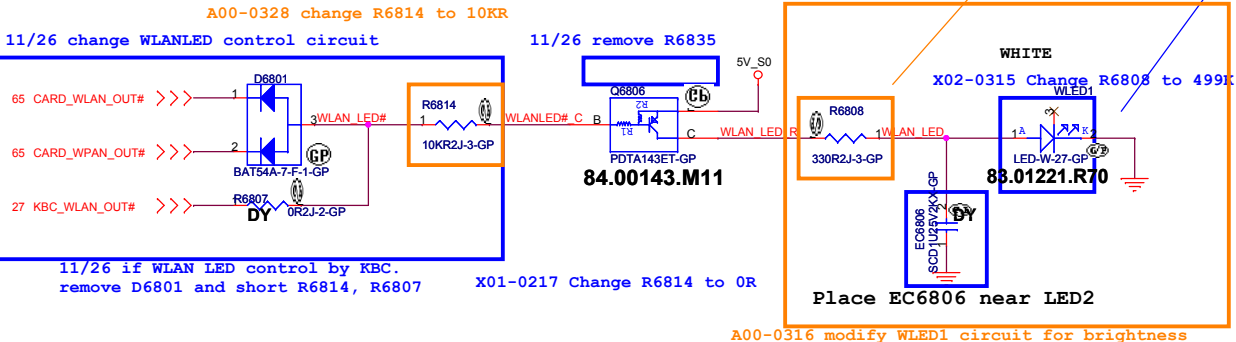
Battery LED2 (WHITE\_LED)



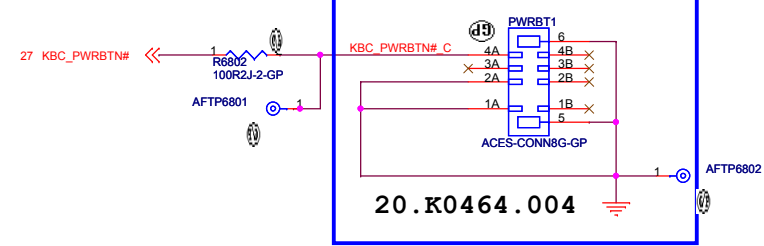
Battery LED1 (AMBER\_LED)



Wireless LED



Power button



SSID = KBC

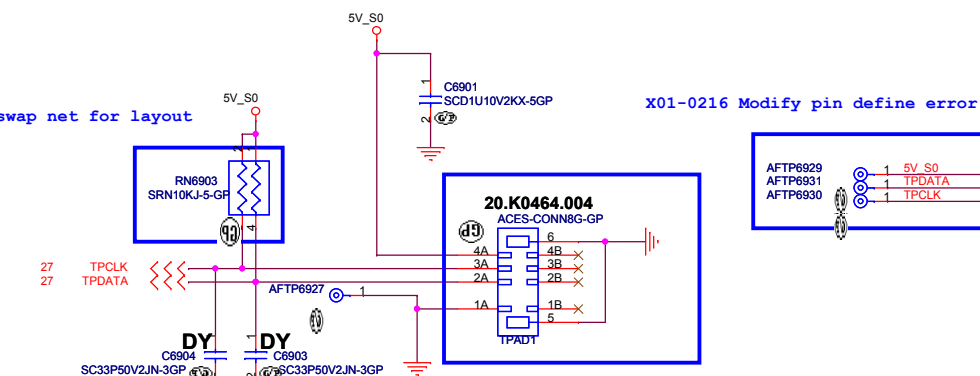
SSID = Touch.Pad

X01-0216 Modify pin define error

## TouchPad Connector

12/6 swap net for layout

X01-0216 Modify pin define error



X01-0216 exchange C6903&amp; C6904

11/23 change TPAD1 to 20.K0320.004

X01-0208 change TPAD1 to 20.K0464.004

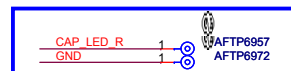
X01-0216 Modify pin define error

20.K0565.030

11/26 change KB1 to 20.K0597.030

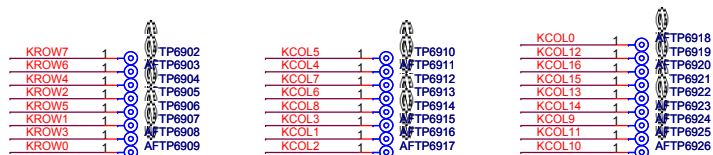
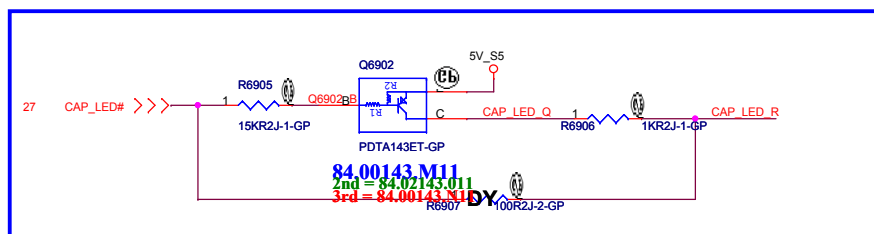
12/8 Change KB1 to 20.K0565.030

X02-0309 change AFTP to follow DV14 AMD



12/8 Add Cap LED control circuit

## CAP LED CONTROL



&lt;Core Design&gt;



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Title

Key Board/Touch Pad

Size  
A3

Document Number

Enrico Caruso 14

Rev


A00

Date: Wednesday, April 13, 2011

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DN15ATI Whistler



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Taipei Hsien 221, Taiwan, R.O.C.

Title

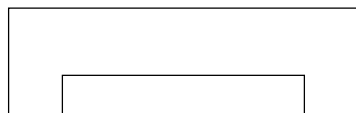
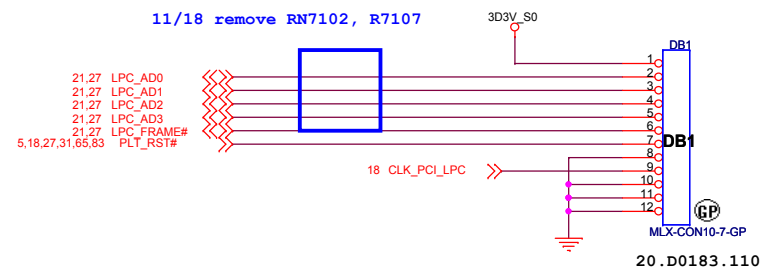
*Hall Sensor*

Size  
A3

Document Number  
**Enrico Caruso 14**

Rev  
**A00**

Date: Wednesday, April 13, 2011Sheet 70 of 105



DN15ATI Whistler



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Taipei Hsien 221, Taiwan, R.O.C.

Title			<b>Debug connector</b>	
Size	Document Number	Rev		
A3		<b>Enrico Caruso 14</b>		<b>A00</b>
Date: Wednesday, April 13, 2011		Sheet	71	of 105

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DN15ATI Whistler



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Title

**Reserved**

Size  
A3

Document Number  
**Enrico Caruso 14**

Rev  
**A00**

Date: Wednesday, April 13, 2011

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DN15ATI Whistler



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size  
A3

Document Number  
**Enrico Caruso 14**

Rev  
**A00**

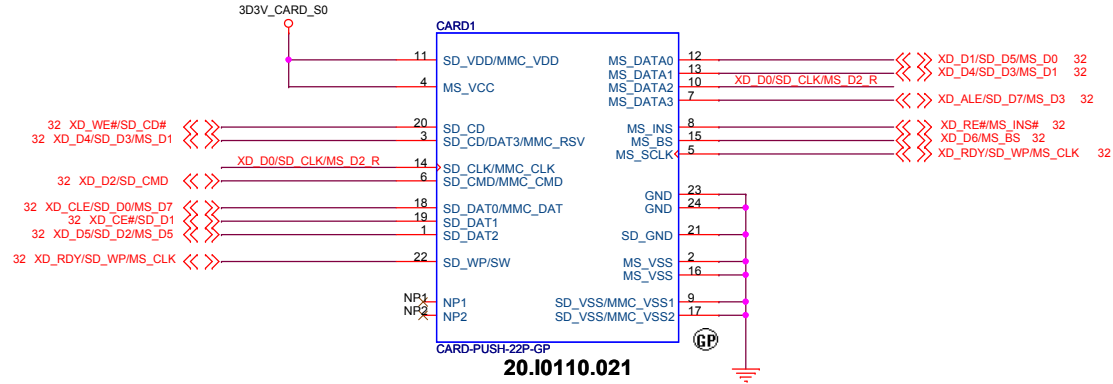
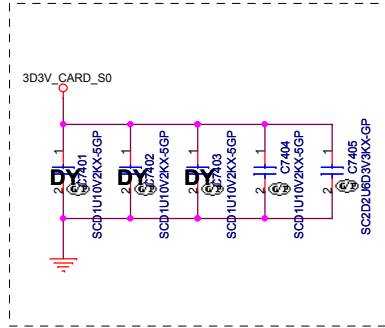
Date: Wednesday, April 13, 2011

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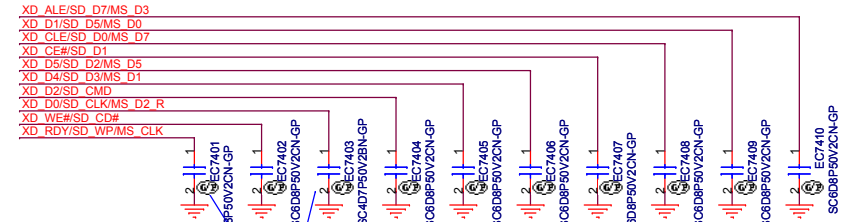
**Reserved**



SSID = SDIO

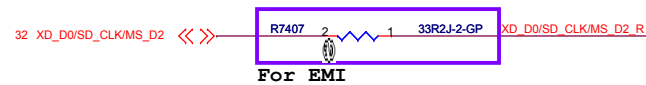


#### 0810 Vendor Recommend



For EMI

11/18 Dummy EC7401, EC7403  
11/20 vendor recommend to reserve 5P  
X01-0216 stuff EC7401~EC7410 for EMI



For EMI

<Core Design>

SSID = ExpressCard

www.laptopblue.vn

<Core Design>



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Title

Size  
A3

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**A00**

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DN15ATI Whistler



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Title

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SSID = User.Interface

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Title

**Free Fall Sensor**

Size  
A3

Document Number  
**Enrico Caruso 14**

Rev  
**A00**

Date: Wednesday, April 13, 2011Sheet 79 of 105

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DN15ATI Whistler



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Title

**Reserved**

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DN15ATI Whistler



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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

Size  
A3

Document Number  
**Enrico Caruso 14**

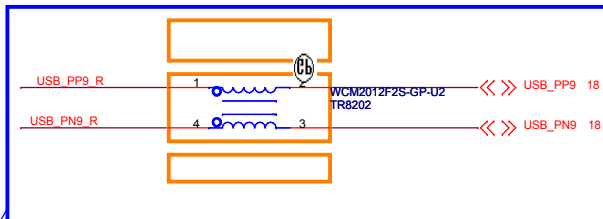
Rev  
**A00**

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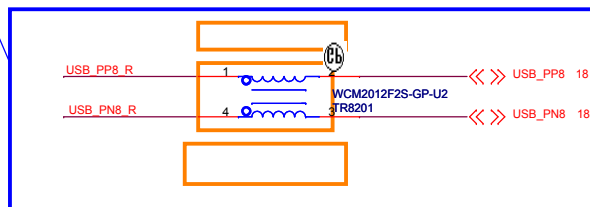


11/1 Stuff TR8201, TR8202 for EMI

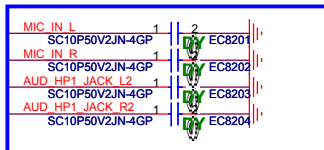


A00-0406 remove R8201, R8202, R8203, R8204 pad  
A00-0320 Change TR8201, TR8202 to 120ohm.  
A00-0408 Swap net for layout

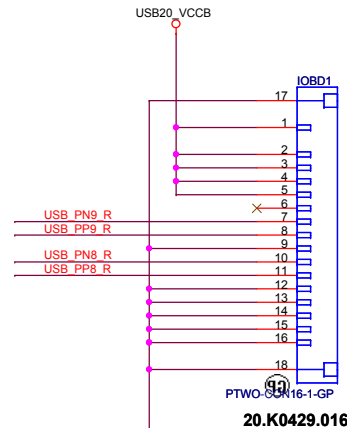
12/6 swap net for layout



11/1 Add EC2901~EC2904 for EMI request



IOBD1 is for USB board

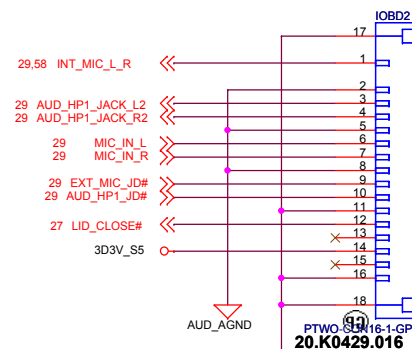


11/10 modify B2B CONN and pin define

X01-0214 add AFTP8201~8210

X02-0309 Del AFTP8201~8210

IOBD2 is for Audio board



X02-0309 Del AFTP8201~8210

12/10 Change pin defien for audio board routing smooth.

12/14 Change IOBD2 to 20.K0429.016 and change pin define.

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title  
**IO Board Connector**  
Size A3 Document Number  
**Enrico Caruso 14** Rev  
**A00**  
Date: Wednesday, April 13, 2011 Sheet 82 of 105

SSID = VIDEO

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CONFIRM IN STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS  
0= DO NOT INSTALL RESISTOR  
1= INSTALL 3K RESISTOR  
X = DESIGN DEPENDANT  
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0: Advertises the PCIe device as 2.5GT/s capable at power on. 1: Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
GPIO8_ROMSO	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0: VGA Controller capacity enabled 1: The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (2.56MB)
GPIO21_BB_EN	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0: Disable external BIOS ROM device 1: Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]: 11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSXNC		X	1

PCI EXPRESS INTERFACE

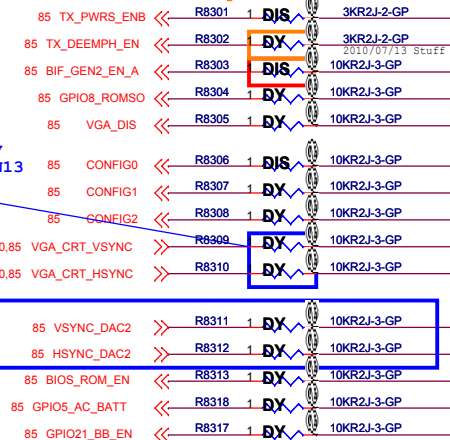
VGA1

11/18 Add R8311, R8312 and dummy R8319, R8310 to follow DN13

A00-0322  
Dummy R8302 for disable de-emphasis

2010/06/11  
Need to check

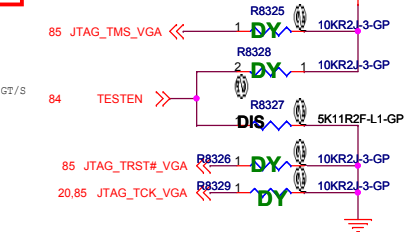
PIN STRAPS



2010/06/11

3D3V\_VGA\_S0

3D3V\_VGA\_S0



JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1" (PU)	"1" (PU)	"0" (PD)
JTAG_TRST#	"0" (PD)	"1" (PU)	NC
JTAG_TCK	CLK	"1" (PU)	NC
JTAG_TMS	"1" (PU)	"1" (PU)	NC

<Core Design>

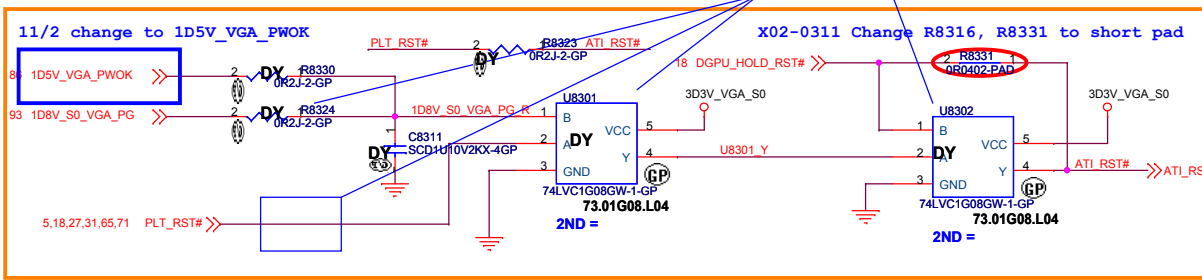
**DELL** Wistron Corporation  
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Title: **GPU PCIE/STRAPPING(1/5)**

Size A3 Document Number **Enrico Caruso 14** Rev **A00**

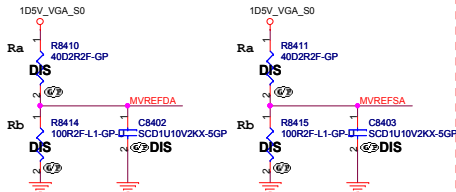
Date: Wednesday, April 13, 2011 Sheet 83 of 105

	PE_GPIO0
dGPU mode	H
IGPU	L
IGPU with BACQ	H



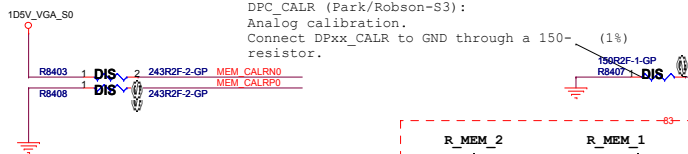
SSID = VIDEO

PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC



DDR3/GDDR3 Memory Stuff Option (ROBSON-S3/SEYMOUR-XT-S3)

	DDR5	DDR3
MVDDQ	1.5V	1.5V/1.8V
Ra	40.2R	40.2R
Rb	100R	100R

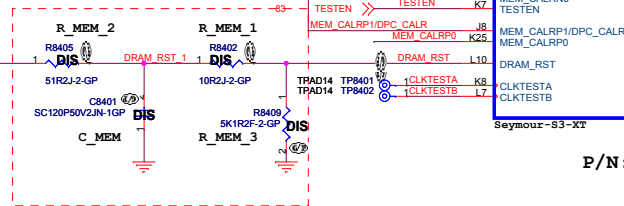


DPC\_CALR (Park/Robson-S3):  
Analog calibration.  
Connect DPxx\_CALR to GND through a 150-ohm resistor.

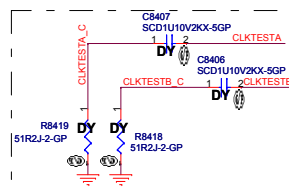
\*\*\*This basic topology should be used for DRAM\_RST for DDR3/GDDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory, DRAM Load and board to pass Reset Signal Spec.

Designator	For SEYMOUR	For Robson
R_MEM_1	10R	10R
R_MEM_2	50R	50R
R_MEM_3	5K	5K
C_MEM	120pF	120pF

Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except R\_MEM\_2



P/N: FUPJP



For normal GPU operation, these signals can be left floating (do not populate the capacitors and resistors).

VGA1

MEMORY INTERFACE

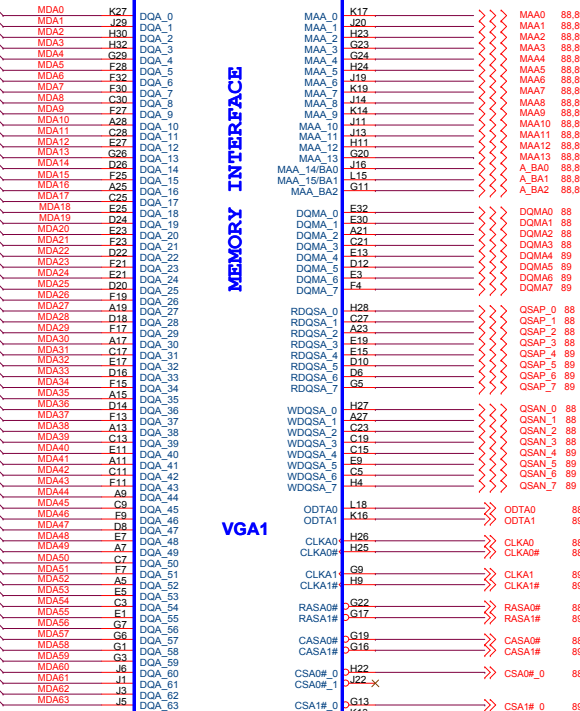
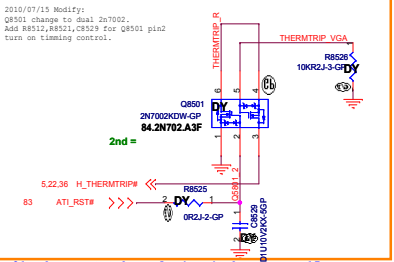


Table with 2 columns: DVDPDATA [3:0] and Description. Rows include DDR3 Samsung and Hynix configurations for 900MHz and 128M\*16.

For Seymour,  
DPC\_PVDD is DPC\_VDD18 2010/06/11  
DPC\_PVSS and all DPC\_VSSR are DP\_VSSR



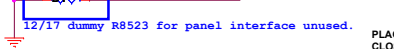
X01: dummy VGA thermal circuit based on DN15 11/18 Del C8529 to follow DN13



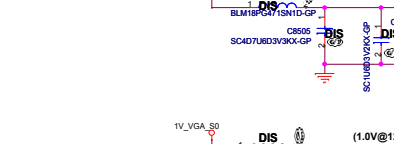
GPIO\_6, GPIO\_15 PWRCNTL\_0, GPIO\_16 SSIN, GPIO\_20 PWRCNTL\_1: Voltage control signals for the core (VDDC and VDDCI).



2010/07/07 Change to RSVD based on DS v3.05



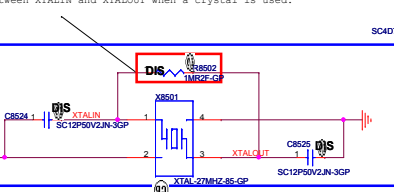
12/17 dummy R8523 for panel interface unused.



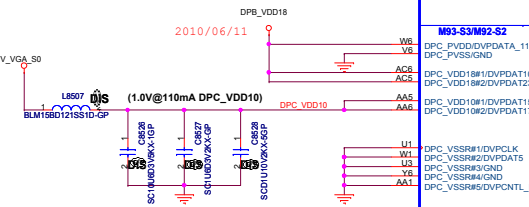
11/18 Del 27M CLK circuit from PCH



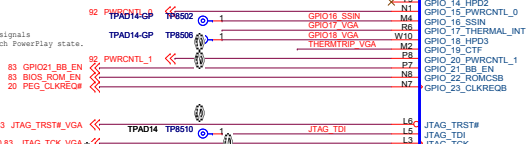
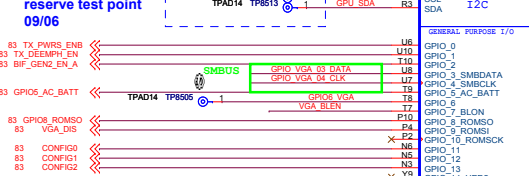
2010/07/06 Schematics check list: A 1-m ohm resistor must be connected between XTALIN and XTALOUT when a crystal is used.



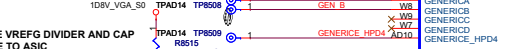
MEM\_ID Control



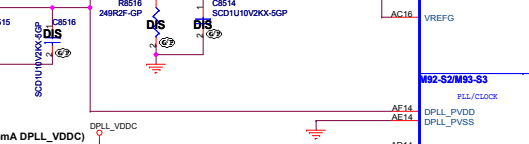
2010/07/07 Remove TP8517, TP8518, TP8506, TP8519, TP8512 Vendor suggest to reserve test point 09/06



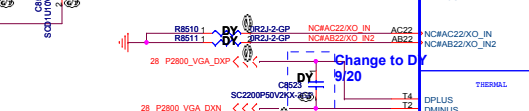
2010/07/07 Change to RSVD based on DS v3.05



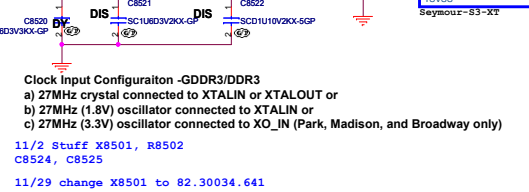
PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC



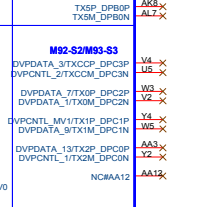
11/18 Del 27M CLK circuit from PCH



2010/07/06 Schematics check list: A 1-m ohm resistor must be connected between XTALIN and XTALOUT when a crystal is used.



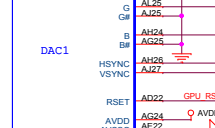
DVO



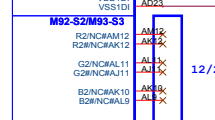
I2C



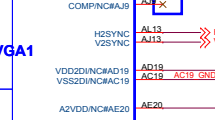
DAC1



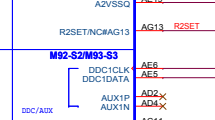
DAC2



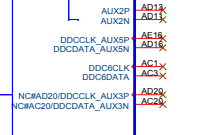
VGA1



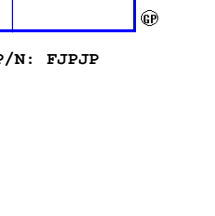
DAC1



DAC2



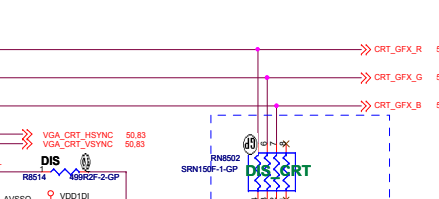
VGA1



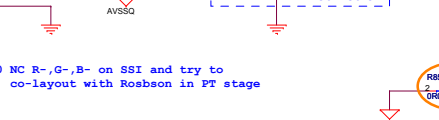
DPC



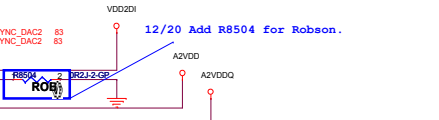
DAC1



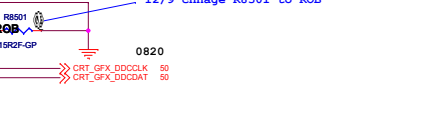
DAC2



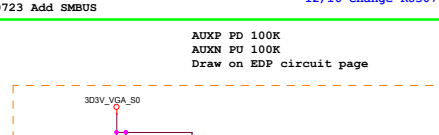
VGA1



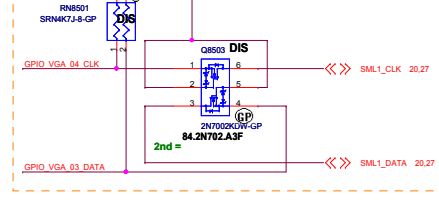
DAC1



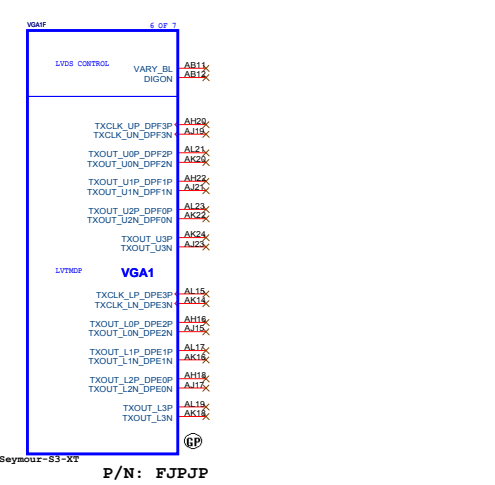
DAC2



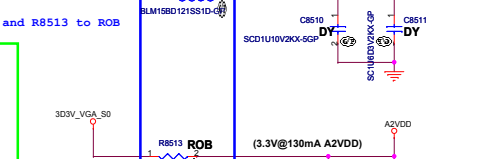
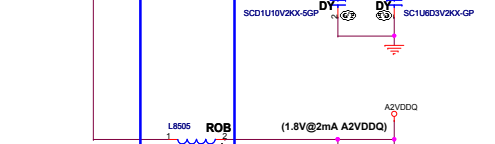
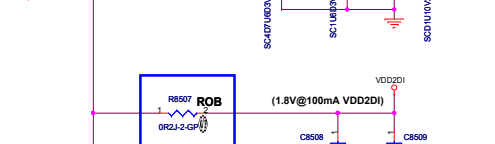
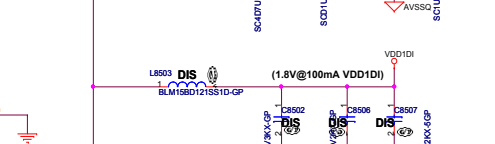
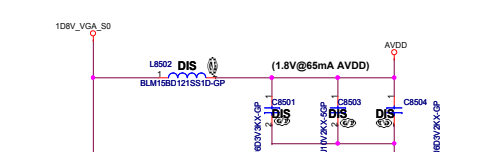
VGA1



LVDS Interface



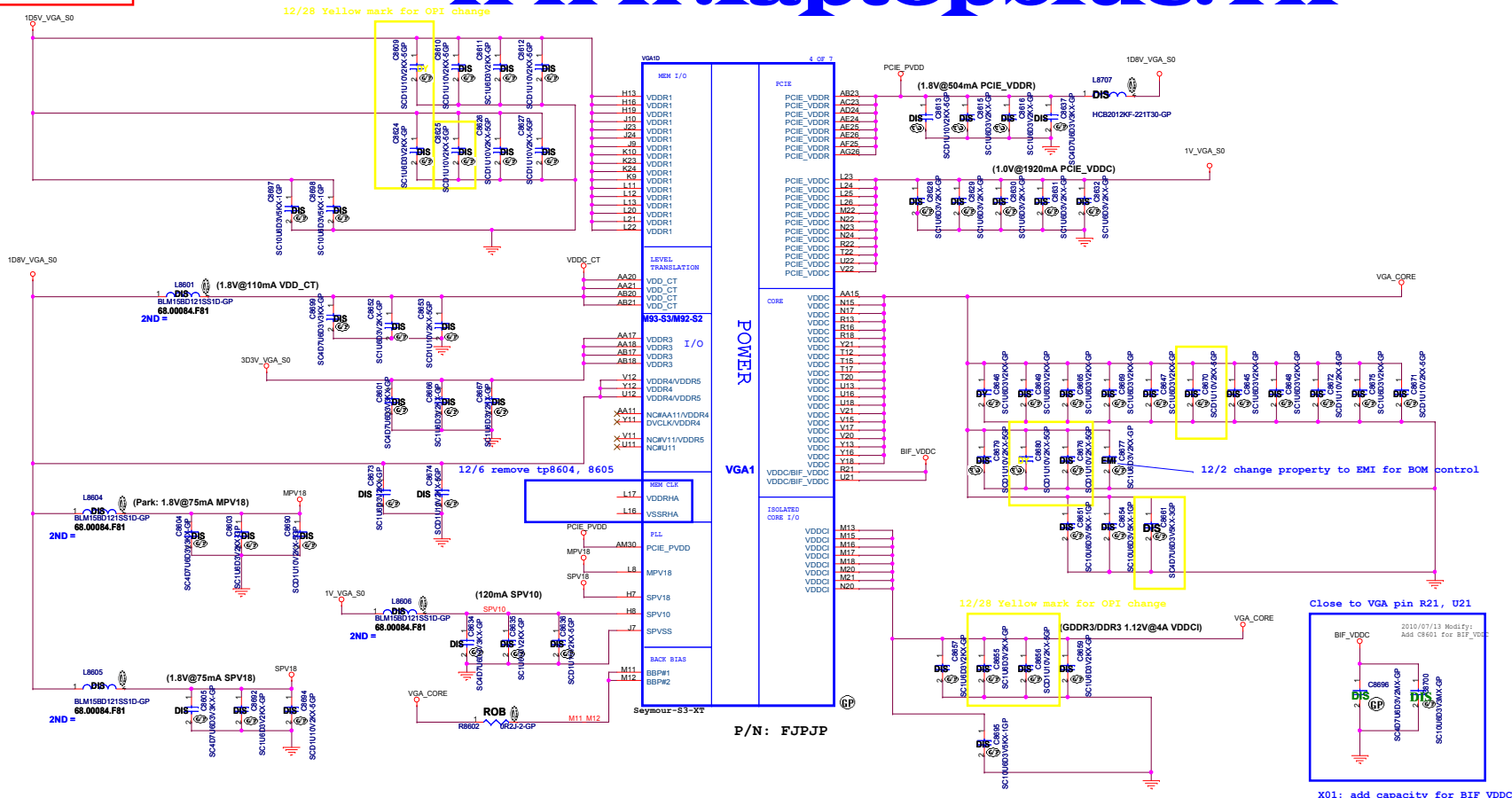
Seymour-S3-XT P/N: FJFJJP



Wistron Corporation logo and address information.

SSID = VIDEO

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2010/06/17\_1

Rds(on) = low  
VGS=0.7-1.5V

AO4468 MAX 3.1A  
Rds(on) = 101-155mOhm  
VGS=+/-12V

2010/07/08

1D5V\_VGA\_PWOK

11/18 dummy 1D5V\_VGA\_PWOK circuit

X02-0302 Add R8605, R8609 PU 5V for lower Rds(on)

X01: modify to DGPU\_PWOK

Change polarity, switch pin D and pin S 9/6

Non-BACO= HIGH  
BACO = LOW

	PX_EN#	8209A_EN/DEM_VGA/1D5V_VGA_PWOK_R	PX_EN#	PX_EN#
Non-BACO	0	1	1	0
BACO	1	0	0	1

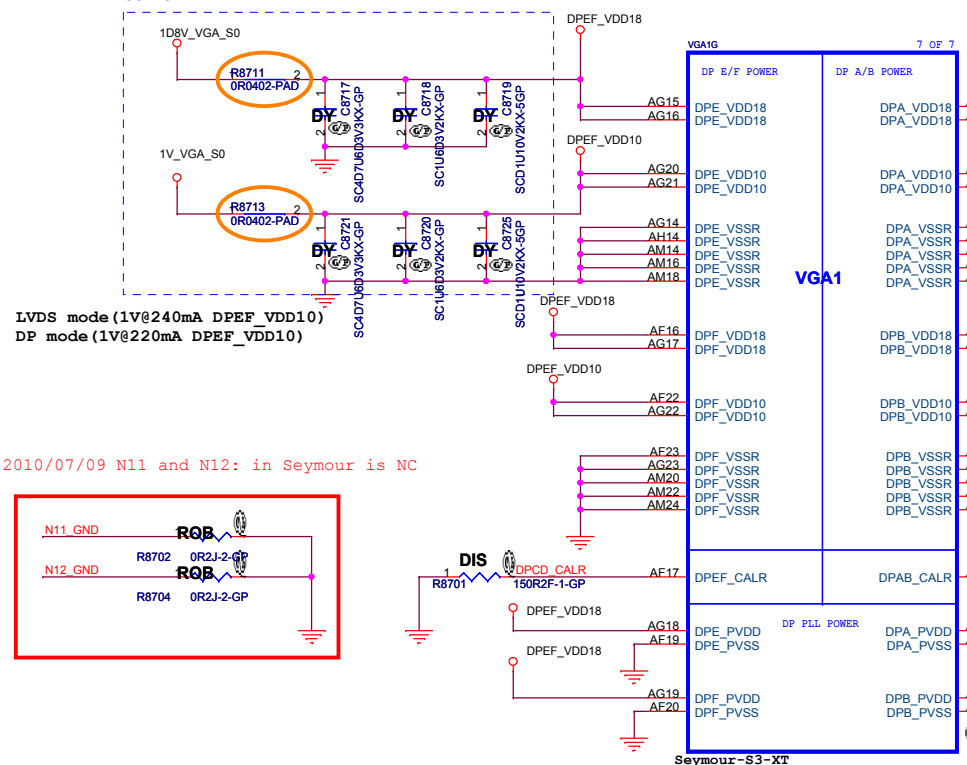
PX\_EN# = High, BIF\_VDDC = 1V\_VGA\_S0  
PX\_EN## = High, BIF\_VDDC = VGA\_CORE

12/16 dummy U8605 and stuff R8601 to follow standard schematic.

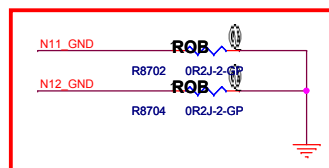
<Core Design>



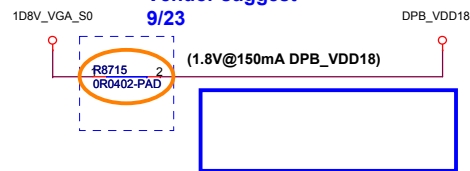
LVDS mode (1.8V@440mA DPEF\_VDD18)  
DP mode (1.8V@300mA DPEF\_VDD18)



2010/07/09 N11 and N12: in Seymour is NC

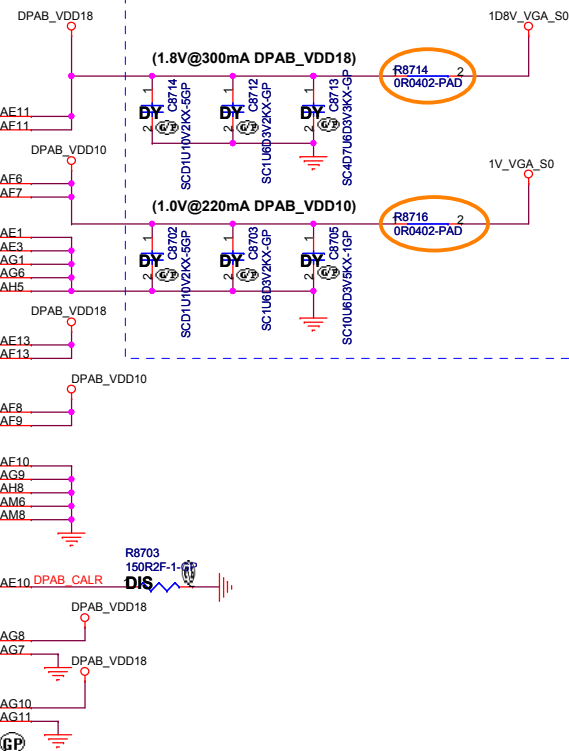


Vendor suggest  
9/23



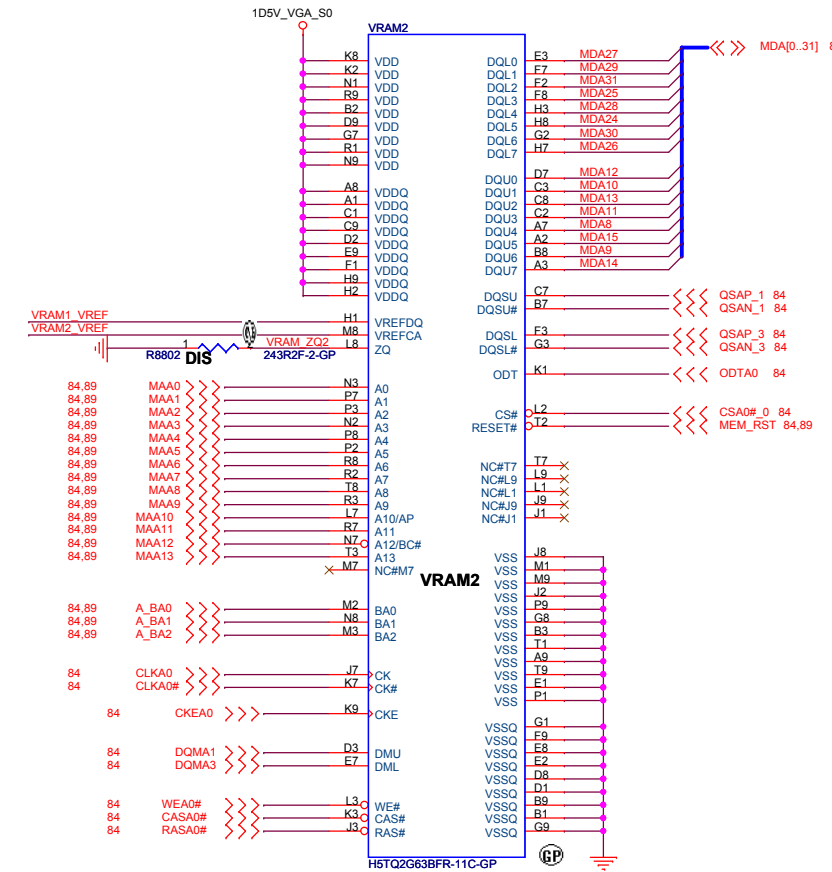
11/18 Del R8709, C8710, C8711

Vendor suggest  
09/23



P/N: FJPJP





105V\_VGA\_S0

R8806  
2K1R2F-GP

DIS

VRAM2\_VREF

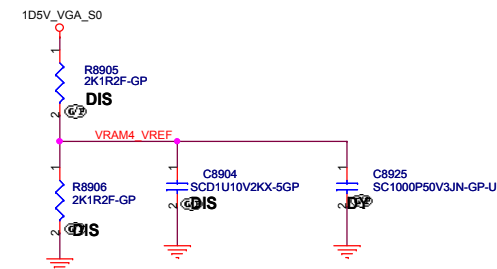
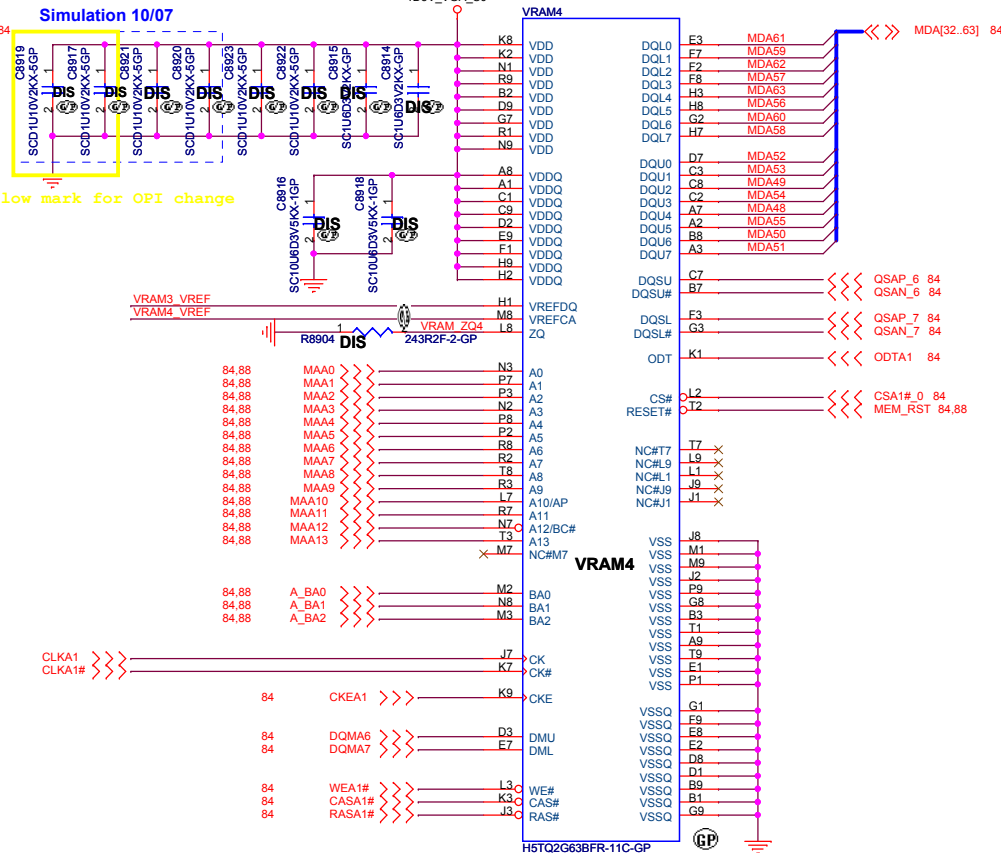
R8807  
2K1R2F-GP

DIS

C8805  
SCD1U10V2KX-5GP

DY


C8807  
SC1000P50V3JN-GP-U





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**GPU-VRAM5,6 (3/4)**

Size  
A3

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**GPU-VRAM7,8 (4/4)**

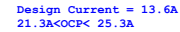
Size  
A3

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X01-0217 change PT9202 -->79.33719.20L  
PT9203 -->79.33719.L01

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: 0.68UH PCMB0637-R68MS Cyntec 4.8mohm/5.3mohm Isat =17Arms 68.R6810.20J  
O/P cap: 330U2V EEFC0X0D331R 15mohm 2.7Arms Panasonic/79.33719.20D  
H/S: S1R172DP / 10.3mohm/12.4mohm@4.5Vgs/ 84.00172.037  
L/S: S1R460DP / 0.49mohm/0.61mohm@4.5Vgs/ 84.00460.037

PWRCNTL_1	PWRCNTL_0	VGA_CORE_PWR
L	L	1.05V
L	H	1.0V
H	H	0.9V

PWRCNTL_1	PWRCNTL_0	VGA_CORE_PWR
L	L	1.12V
H	L	0.95V
H	H	0.9V


For Robson:  
PR9218=10K  
PR9213=49.9K  
PR9211=150K  
PR9210=44.2K

$$V_{out} = 0.75V * (R1 + R2) / R2$$

Date	Wednesday, April 13, 2011	Price	\$0	or	100

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***LVDS Switch***

Size

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CRT Switch

Size

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SSID = SDIO

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**TOUCH PANEL**

Size  
A3

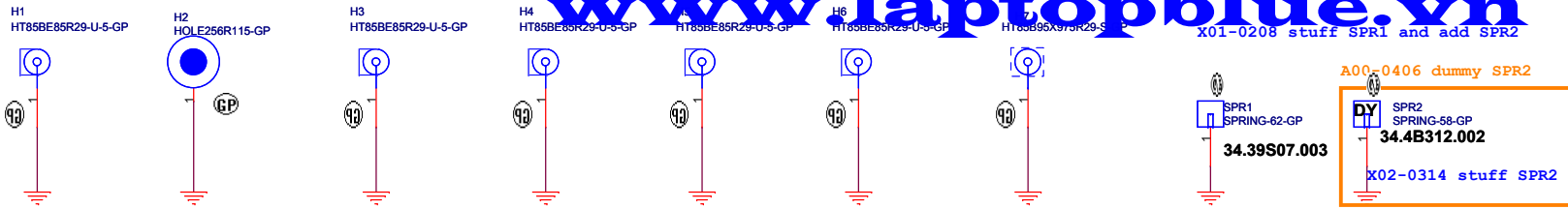
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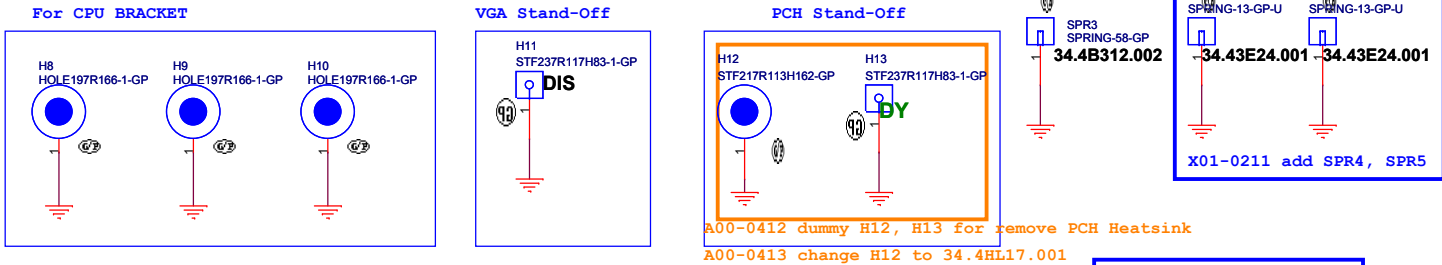
SSID = Mechanical



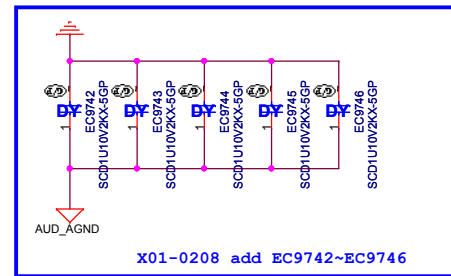
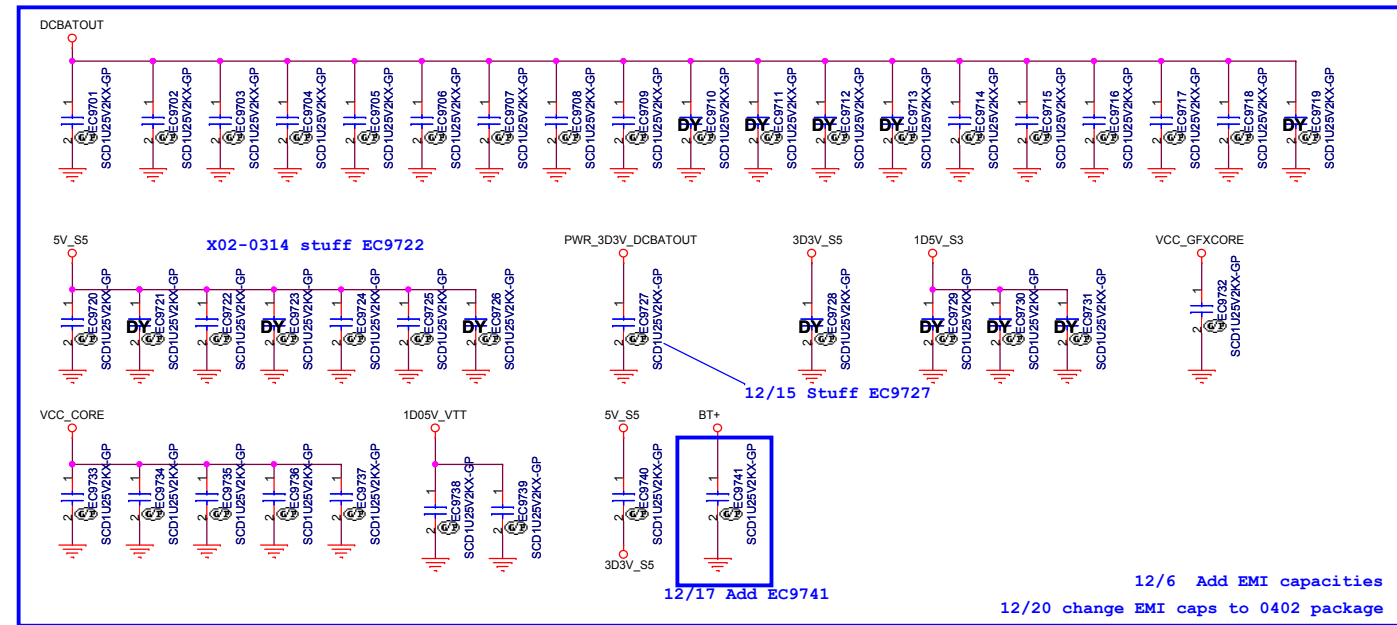
12/17 add SPR1 for EMI  
12/21 change SPR1 to 34.4B312.002  
12/22 change SPR1 to 34.39S07.003

X01-0211 change SPR2, SPR3 to 34.4B312.002

X01-0210 add SPR3



12/2 Delete SPR1, SPR2



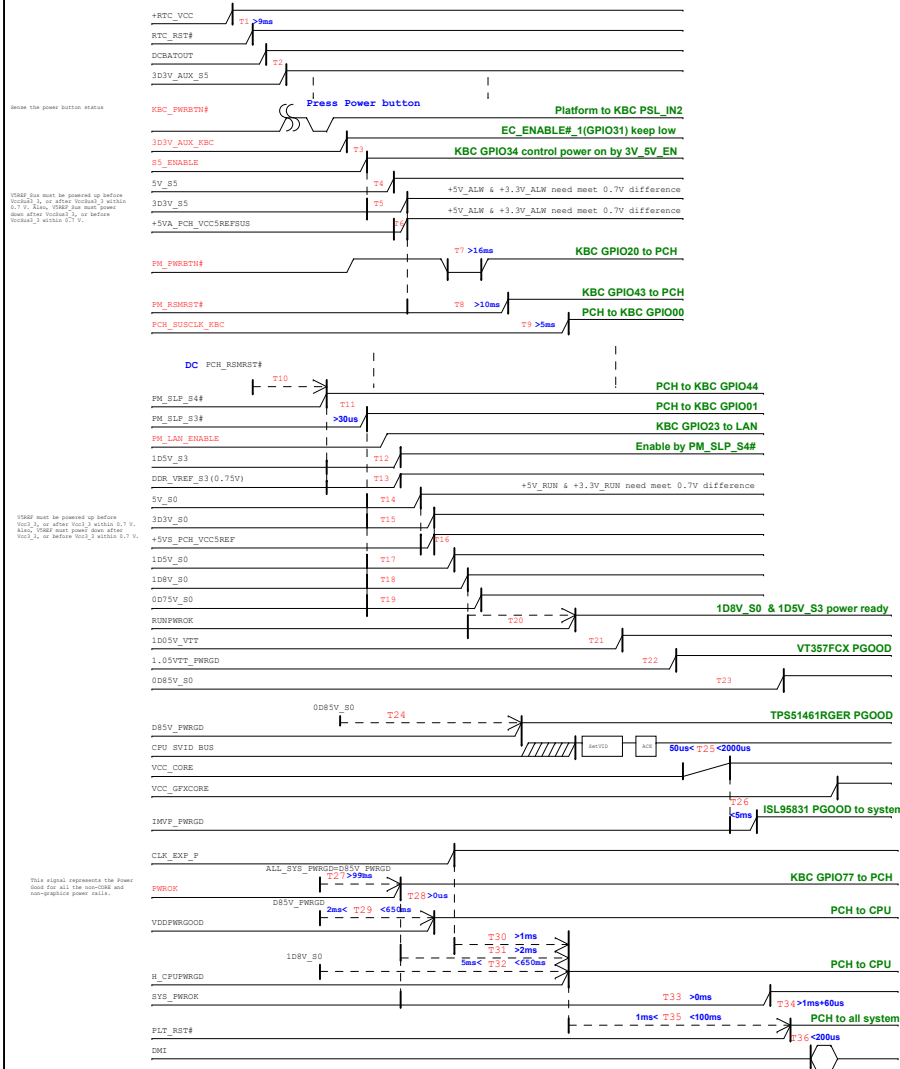
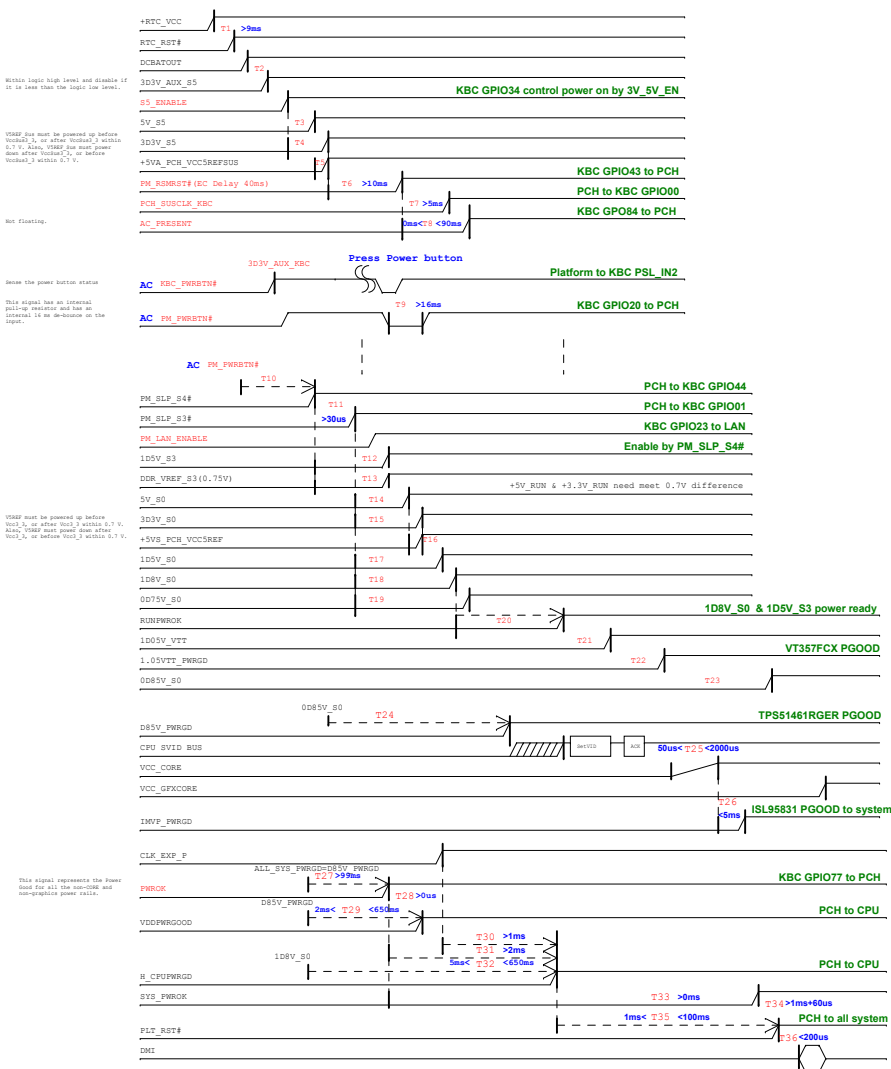


(AC mode)

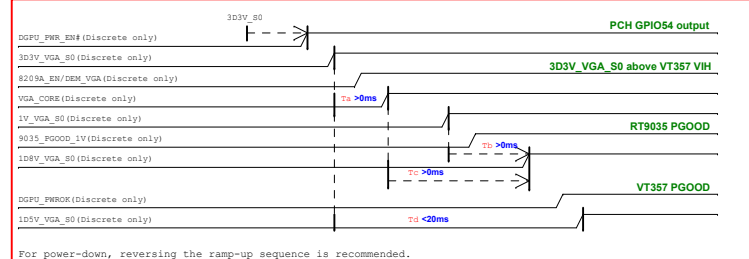
red word: KBC GPIO

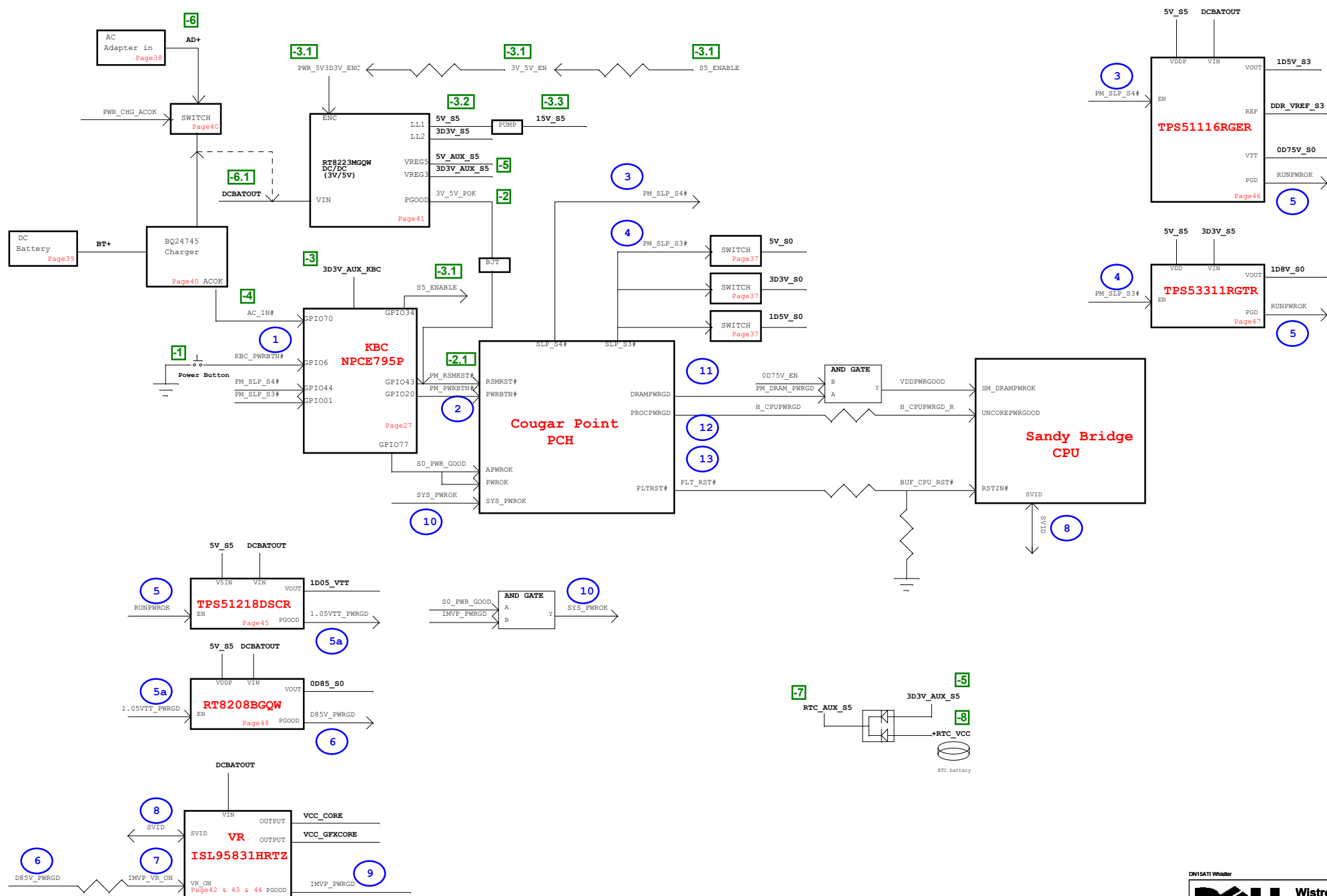
(DC mode)

red word: KBC GPIO

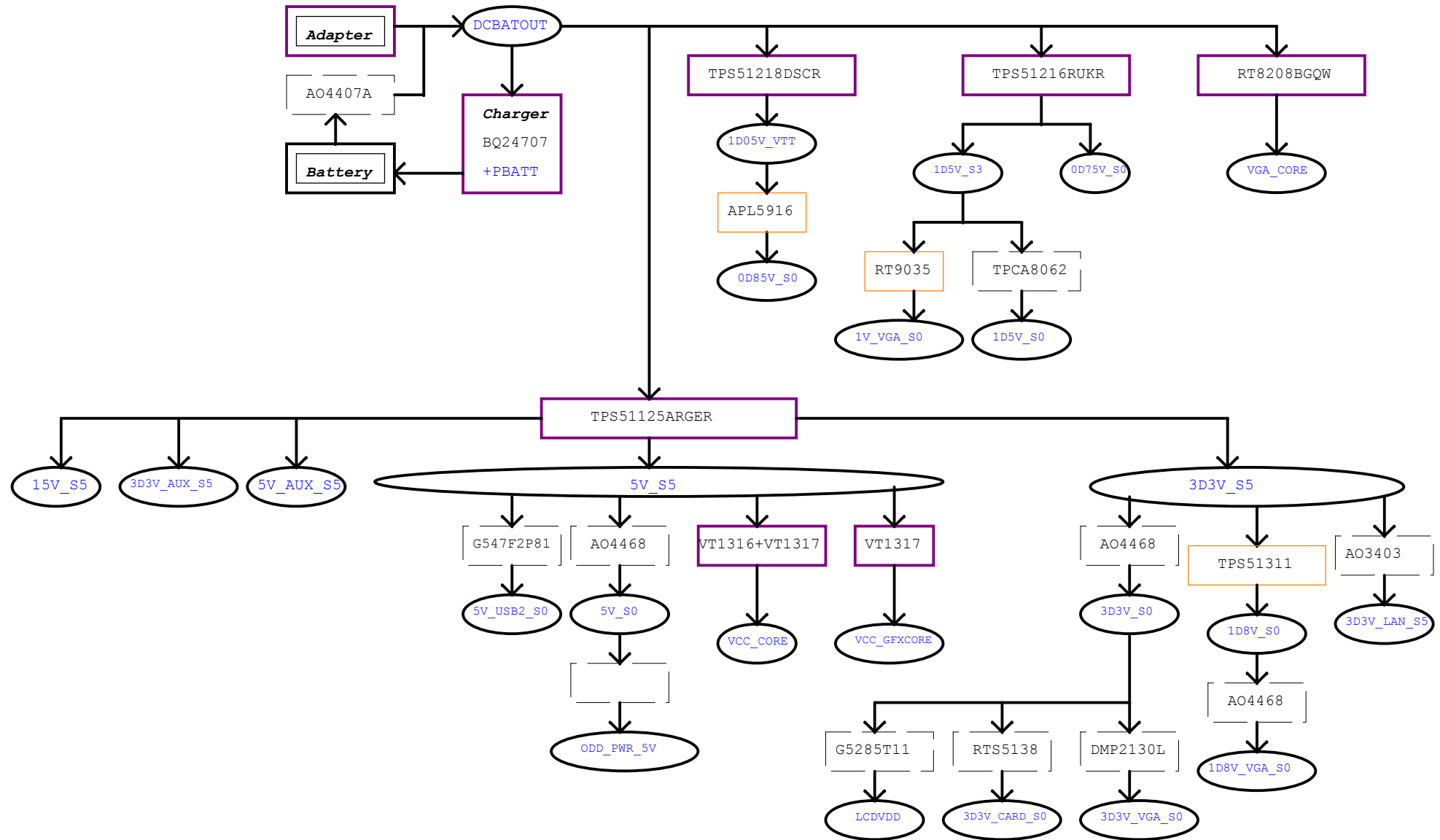


## Robson XT Power-Up/Down Sequence





Power Up Sequence: -8 ~ 13



Power Shape

Regulator

LDO

Switch

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**Power Block Diagram**

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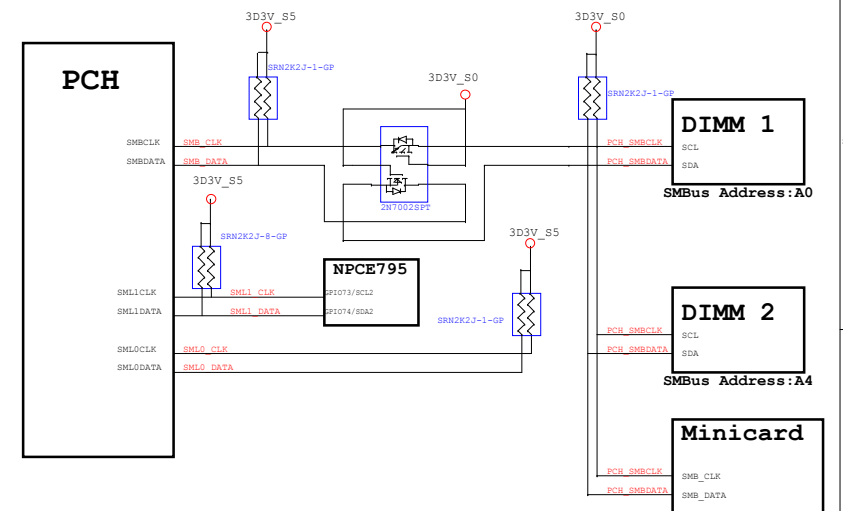
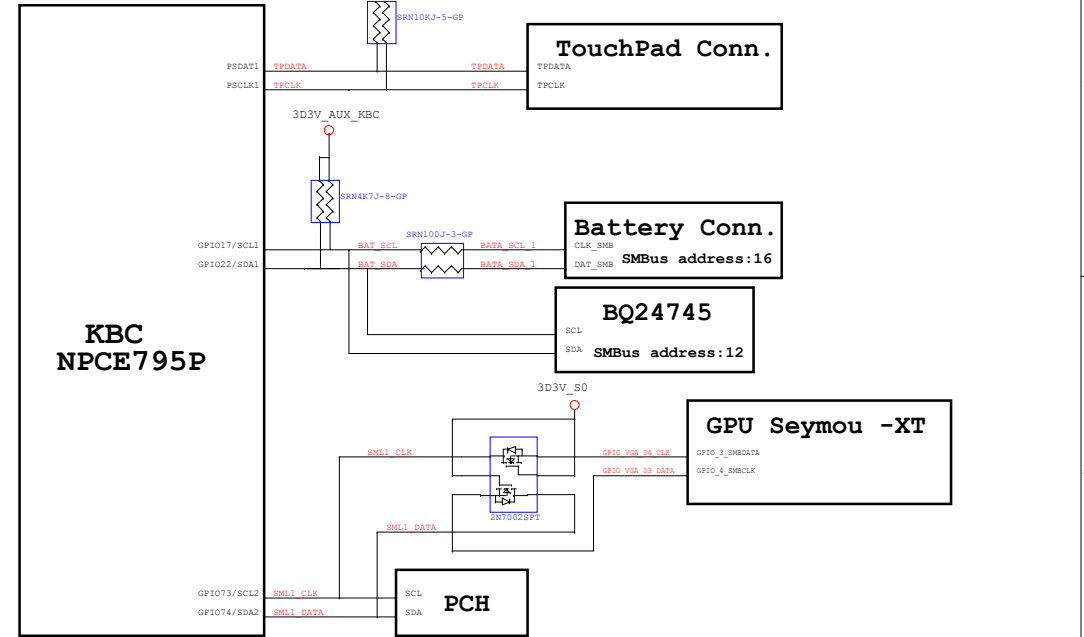
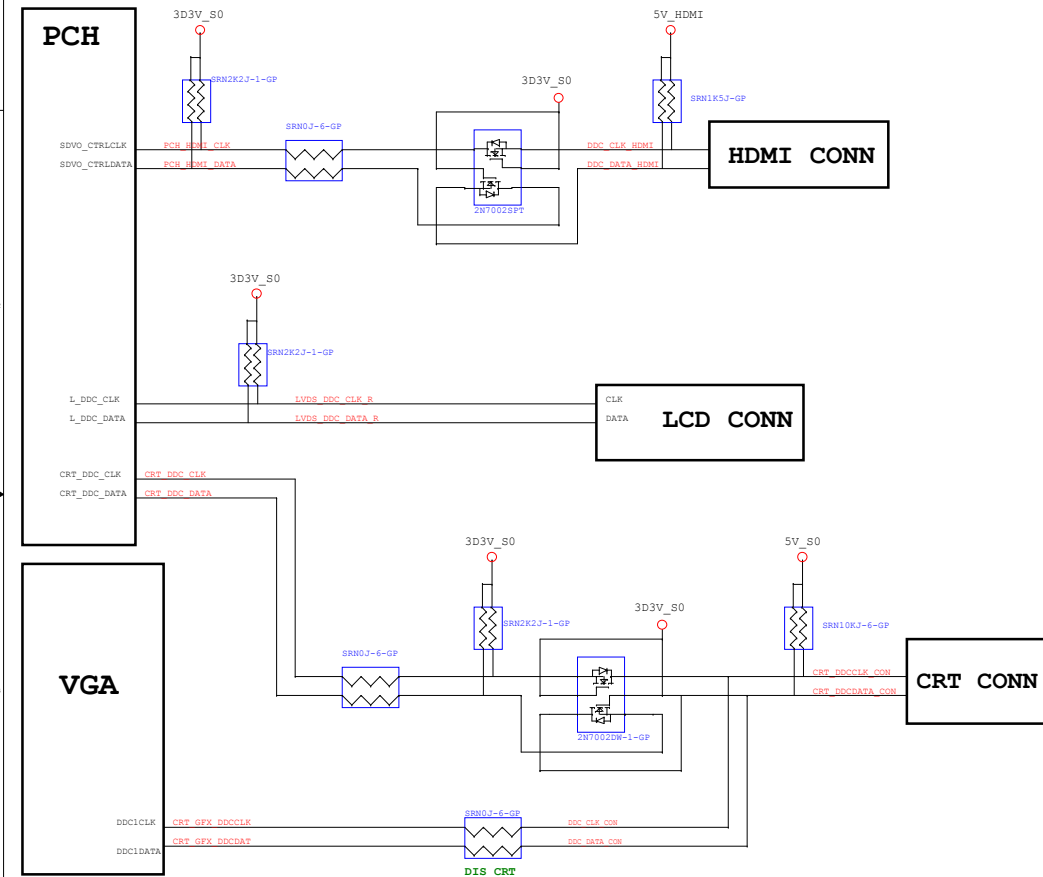
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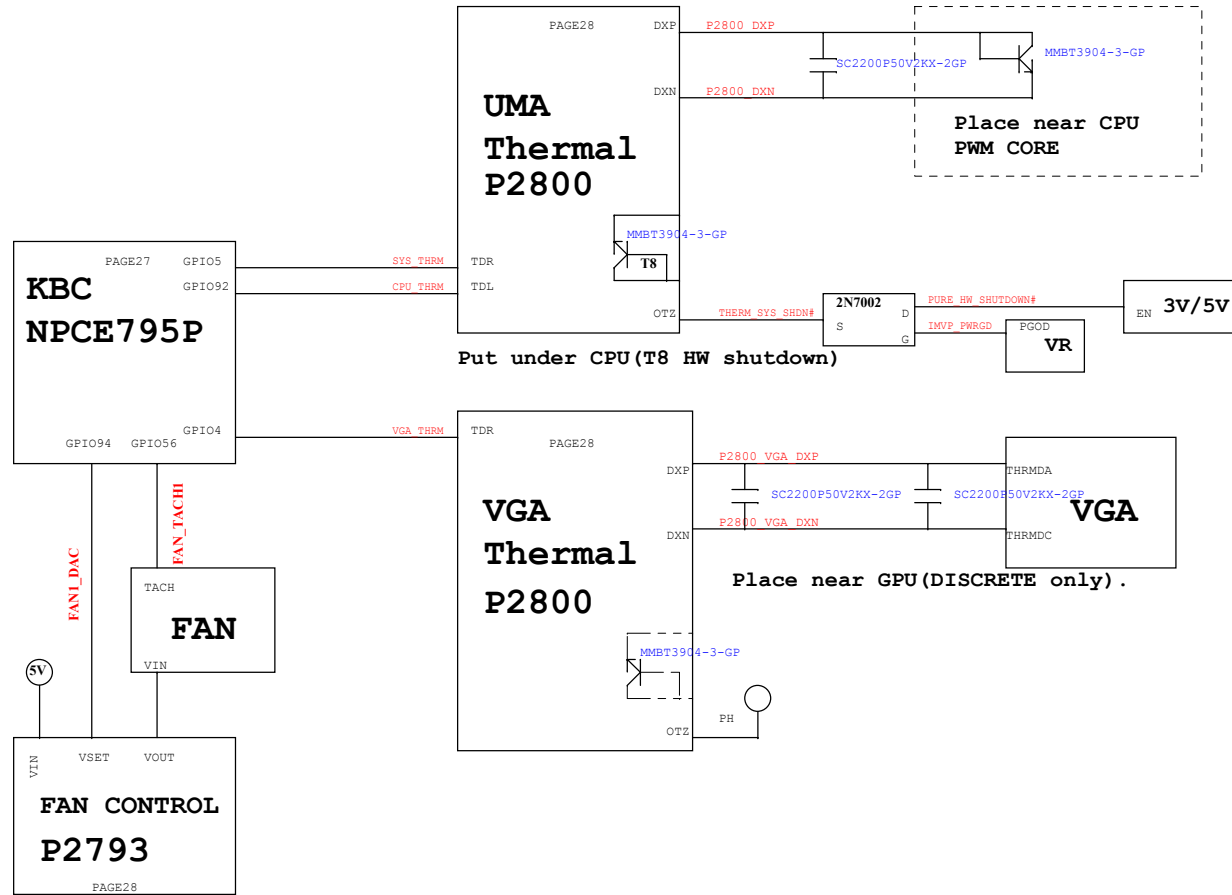
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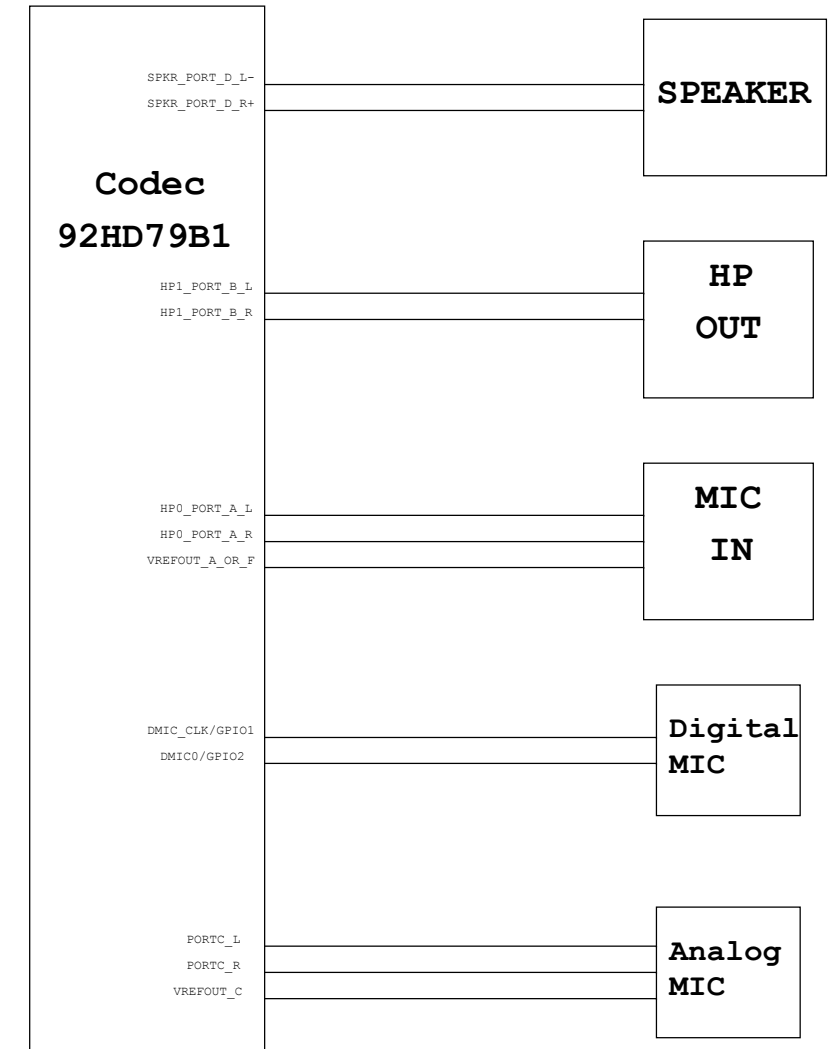
# PCH SMBus Block Diagram



# Thermal Block Diagram



# Audio Block Diagram



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DATA	PAGE	Change Description	Version
12/28	85	dummy VGA thermal circuit	X01
12/28	86	modify to DGPU_PWROK	X01
12/28	86	add capacity for BIF_VDDC	X01
12/28	93	dummy PR9326	X01
1/14	93	modify CS#, WP#	X01
1/27	5	Add C504 for noise couple.	X01
1/27	8	Stuff C812, C822, C831, C834 for VCC core noise issue.	X01
1/27	27	Del R2757 to follow standard 10mW circuit	X01
1/27	31	change Q3101 base power rail for leakage issue.	X01
1/27	40	X01-0127 DY PQ4007, PR4038, PR4039 for new version BQ24707	X01
2/8	21	Add RN2101, R2127 for LPC EA result	X01
2/8	27	Dummy R2769	X01
2/8	50	change R5002, R5003 to 33R	X01
2/8	69	TPAD1 to 20.K0464.004	X01
2/8	27	change R5002, R5003 to 33R	X01
2/8	97	add EC9742~EC9746	X01
2/8	97	stuff SPR1 and add SPR2	X01
2/9	28	dummy U2805 circuit	X01
2/9	46	PT4603 UMA-->220uF DIS-->470uF	X01
2/9	48	dummy PC4809 for BBU result.	X01
2/10	5	Merge R512 R514	X01
2/10	21	change RN2101 to RN2104 RN2105	X01
2/10	27	change R2724 to meet X01 PCB ver	X01
2/10	46	del PT4602	X01
2/10	46	change PC4610 from 0.22uF to 10uF	X01
2/10	97	add SPR3	X01
2/10	21	Merge R5115 R2116	X01
2/11	31	add C3122 for soft-sart	X01
2/11	59	Add EMI solution for Surge	X01
2/11	19,27	Change R1925, R1924, R1906, R1913, R2720, R2758, R2759, R2760 to short-pad	X01
2/14	82	add AFTP8201~8210	X01

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DATA	PAGE		
0212	40	Change charger IC to new version	X01
0302	31	Dummy PCIE_CLK_LAN_REQ# circuit	X02
0302	86	Add R8605, R8609 PU 5V for lower Rdson	X02
0303	14,15,17,18 19,22,23,24 27,29,31,36 37,50,51,68	Change R1404, R1405,R1504, R1503,RN1704, R1807, R1903, R1910, R1912, R2214, R2304, R2305, R2306, R2307, R2404, R2405, R2406, R2409, R2702, R2735,R2762, R2756, R2911,R2914, R2917, R3104, R3115, R3117, R3614, R3710, RN5010, RN5117, R6811, R6813, R6804, R6805 OR to short pad	X02
0309	86	Change AFTP test point to follow DV14 AMD	X02
0310	41,45,92,97	Stuff PC4120, EC4501, PC9205, EC9708, EC9709, EC9714, EC9715, EC9716, EC9717, EC9718, EC9720, EC9724, EC9725, EC9740	X02
0311	28	Add R2816& R2817 to option VGA_THRM and DY the circuit	X02
0311	83	Change R8316, R8331 to short pad	X02
0311	59	Change GDT5901& GDT5902 to GD5901& GD5902	X02
0311	18	dummy R1804	X02
0311	31	add rest circuit to provent leakage.	X02
0311	32	Stuff TR3201 and change symbol to 68.00201.141	X02
0314	38	Del short pad PAD1 to prevent system burn.	X02
0314	97	Stuff SPR2	X02
0314	61,97	Stuff EC9722,C6106	X02
0314	36	Change U3606 footprint.	X02
0315	58	Change MIC2 to 20.F1889.002	X02
0315	88,89	Modify VRAM property PN and footprint	X02
0315	32,59	Modify part reference problem of ER5912& TR3201.	X02
0316	68	Modify WLED1 cirucit for brightness.	A00
0320	31	Change R3118 for LOM power sequence	A00
0320	49	Change TR4901 to 120ohm.	A00
0320	61	Change TR601 120ohm.	A00
0320	68	Change resistor for LED brightness	A00
0320	82	Change TR8201, TR8202 to 120ohm.	A00
0320	83	Dummy R8302 for disable de-emphasis	A00
0329	27	change R2735 to 10R and C2711 to 220p	A00
0329	68	Change R6814 to 10KR	A00
0406	97	Dummy SPR2	A00
0406	32, 49, 61, 65,82	Remove R3206, R3207, R4903, R4904, R6102, R6103, TR6501, R8201, R8202, R8203, R8204 PAD	A00

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