

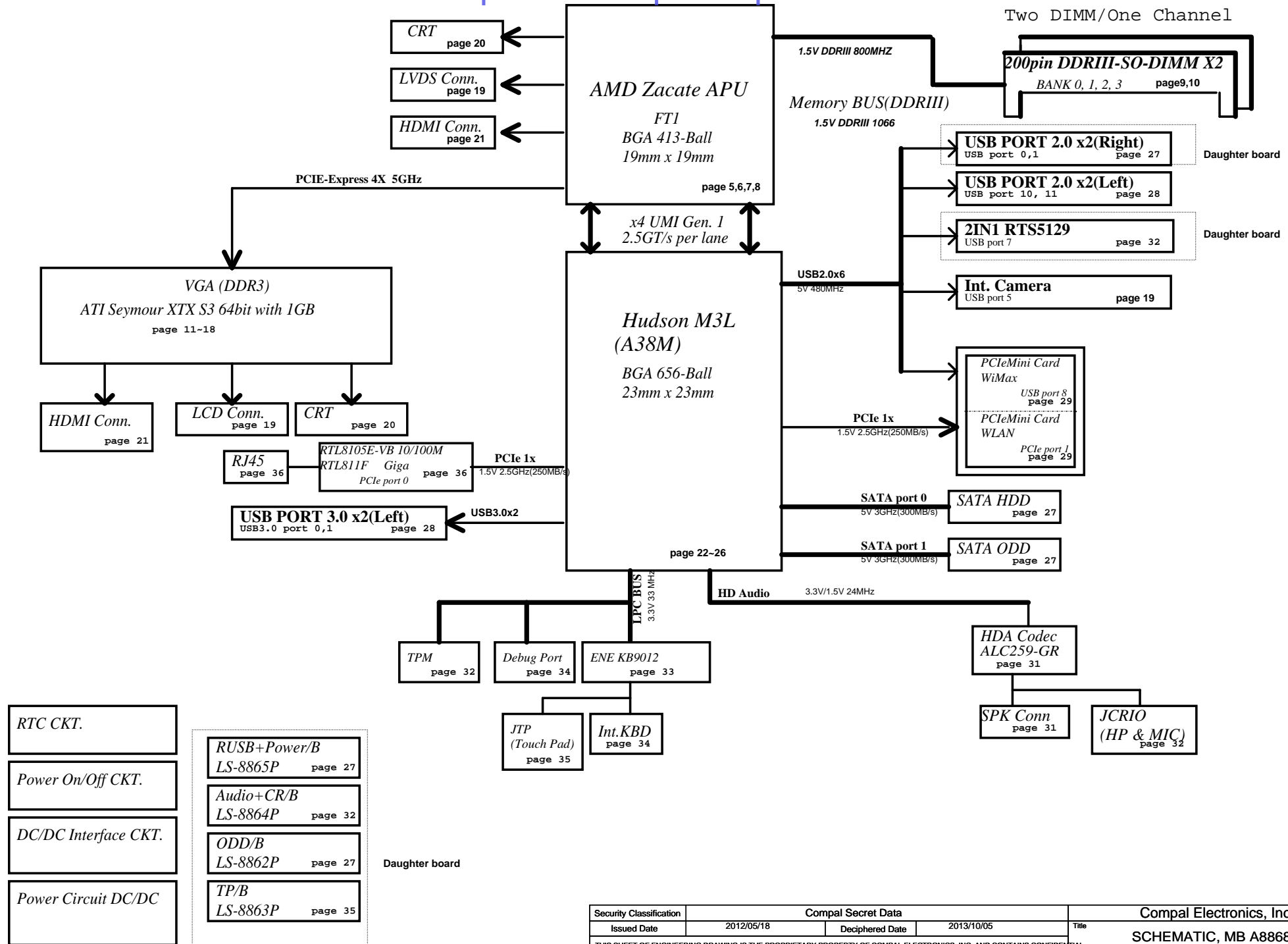
VBLE4 / VBLE5

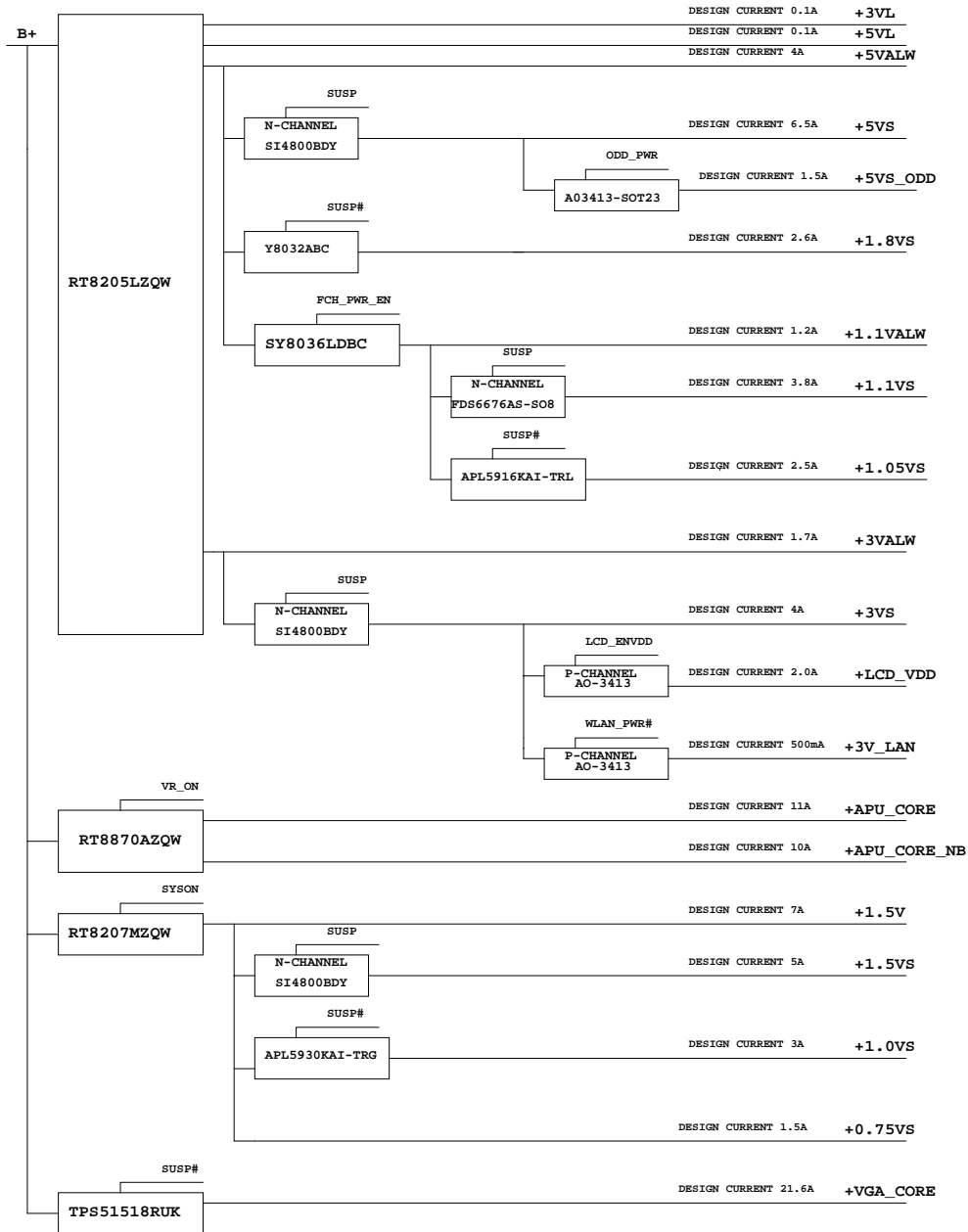
Eureka

LA-8868P REV 1.0 Schematic

AMD Brazos 2.0 / Zacate APU / Hudson-M3L FCH
2012-07-12 Rev 1.0

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Voltage Rails

O MEANS ON X MEANS OFF

power plane State	B+ +3VL +5VL +RTCVCC	+5VALW +3VALW +1.1VALW	+1.5V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +0.9VS +0.75VS +NB_CORE +VDDNB +CPU_CORE_0
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note



: means Digital Ground



: means Analog Ground

@ : means just reserve , no build
 K625R3@ : means just for 1.5G CPU
 K125R3@ : means just for 1.7G CPU
 K325R3@ : means just for 1.3G CPU
 K625R1@ : means just for 1.5G CPU
 K125R1@ : means just for 1.7G CPU
 K325R1@ : means just for 1.3G CPU
 M@ : means just reserve for
 S@ : means just reserve for 11.6 control
 GSENSOR@ : means just reserve for G sensor
 part 1ST@ : means just reserve 1st G sensor
 1STGSENSOR@ : means just reserve 1st G sensor
 IC 2ND@ : means just reserve 2nd G sensor IC
~~2NDGSENSOR@ : means just reserve 2nd G sensor~~
 IC NOSIDE@ : means just reserve NOSIDE
 SIDE@ : means just reserve SIDE
 RS880MR1@ : means just for
 RS880MR3@ : means just for
 SB820MR1@ : means just for SB820MR1
 SB820MR3@ : means just for SB820MR3

SB SM Bus1 Address

SB SM Bus2 Address

Power	Device	HEX	Address	Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b	+3VALW	WLAN/WIMAX		
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b				
+3VS	Clock Generator	D2 H	1101 0010 b				

SMBUS Control Table

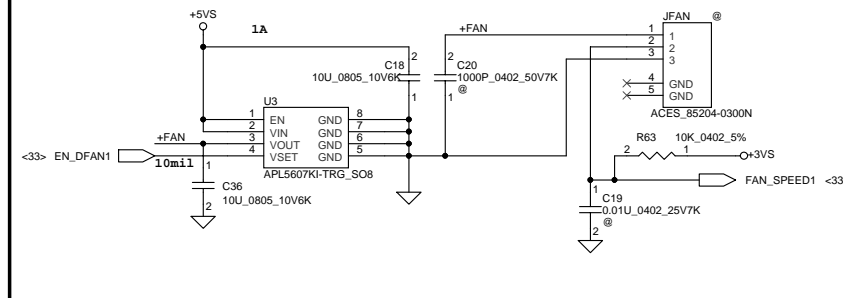
	SOURCE	BATT	CPU THERMAL SENSOR	SODIMM 0	CLK GEN	WLAN WWAN	LCD DDC ROM	HDMI DDC ROM	APU
EC_SMB_CK1 EC_SMB_DA1	KB926	V							
EC_SMB_CK2 EC_SMB_DA2	KB926								V
LCD_EDID_CLK LCD_EDID_DATA	APU FT1						V		
HDMICLK HDMIDAT	APU FT1							V	
SMB_CK_CLK0 SMB_CK_DAT0	FCH M1			V					
SMB_CK_CLK1 SMB_CK_DAT1	FCH M1					V			

EC SM Bus1 Address

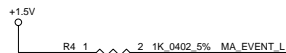
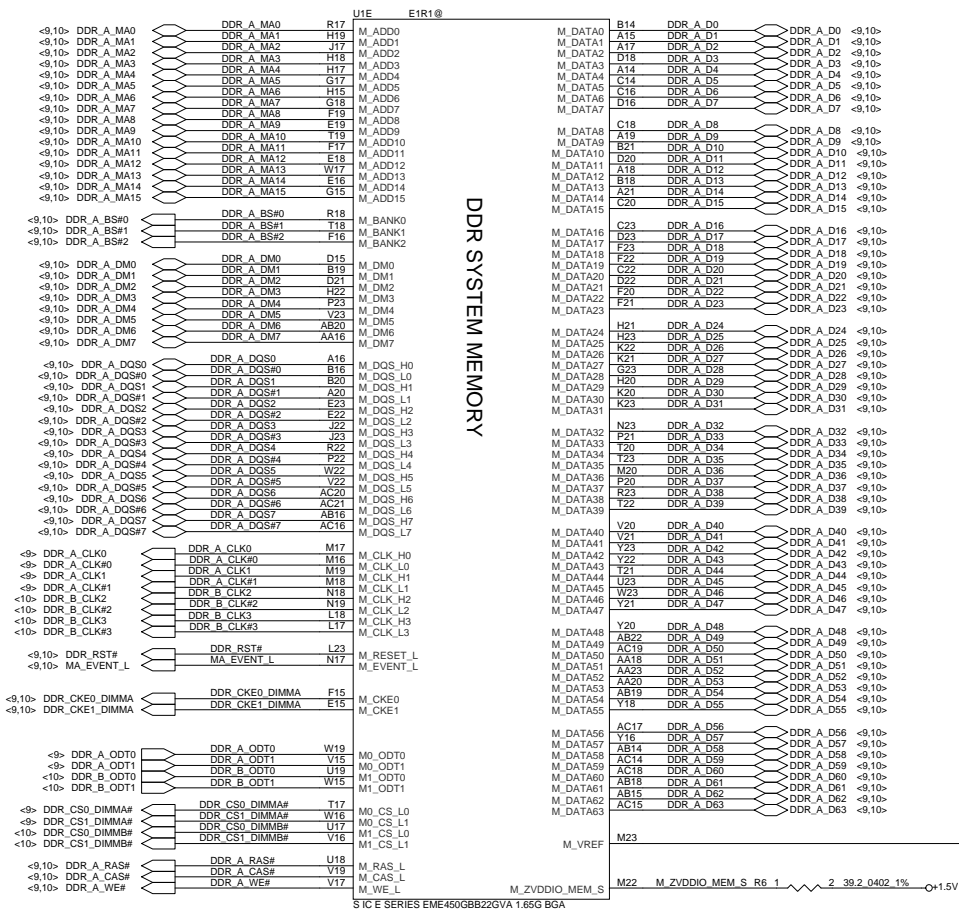
EC SM Bus2 Address

Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 011X b	+3VS	CPU_ADM1032-1	98 H	1001 100X b
				+3VS	G-Sensor		

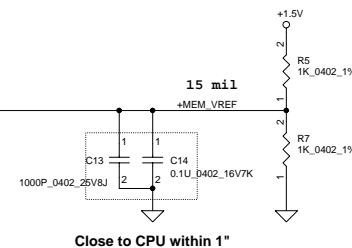
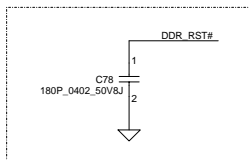
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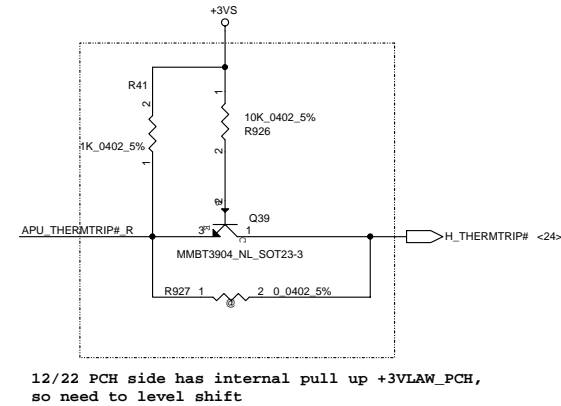
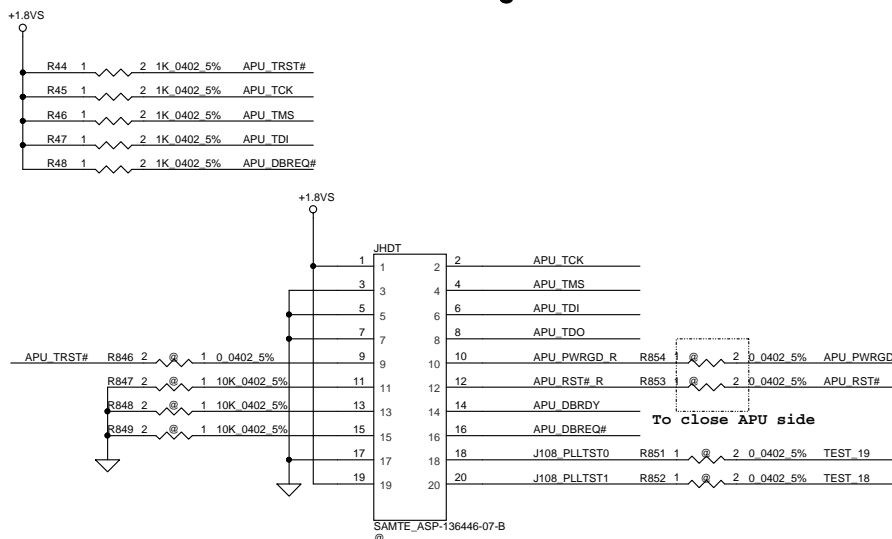
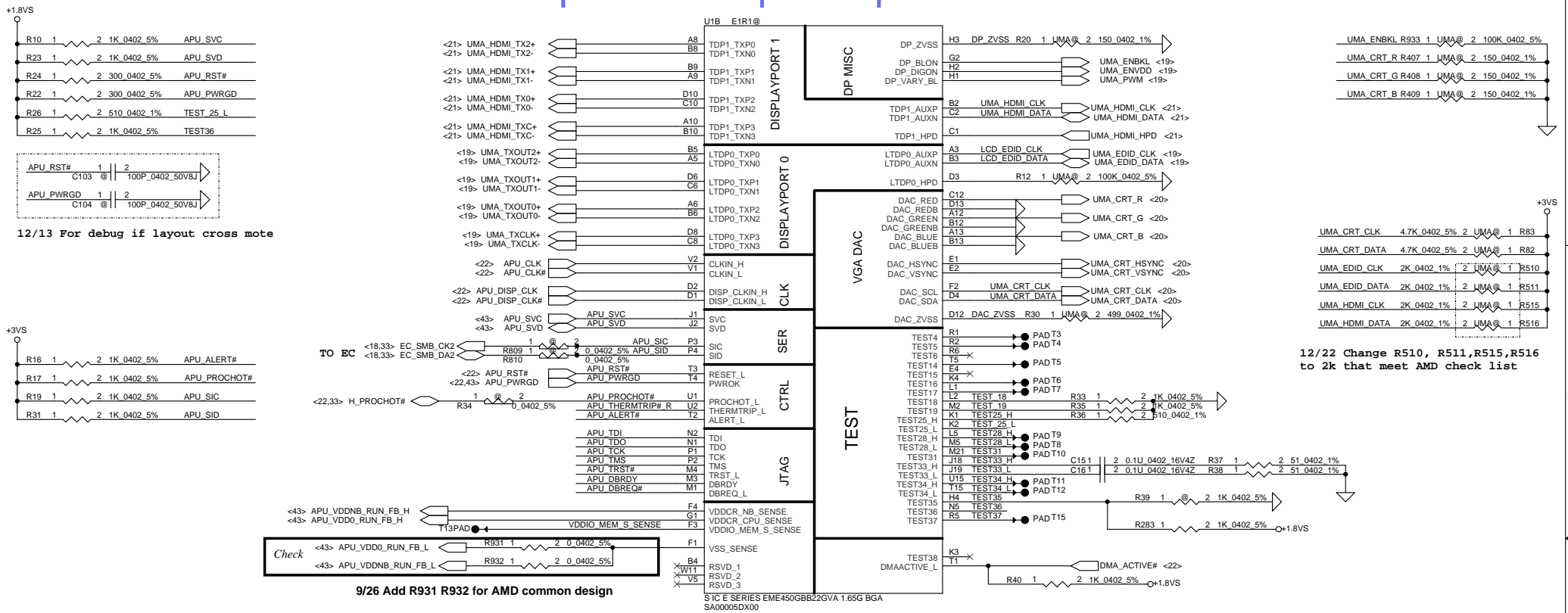


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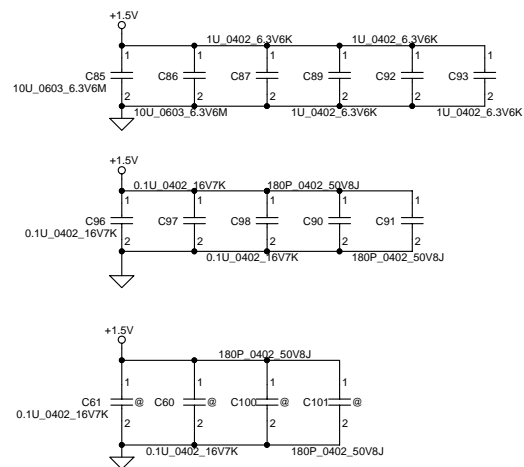
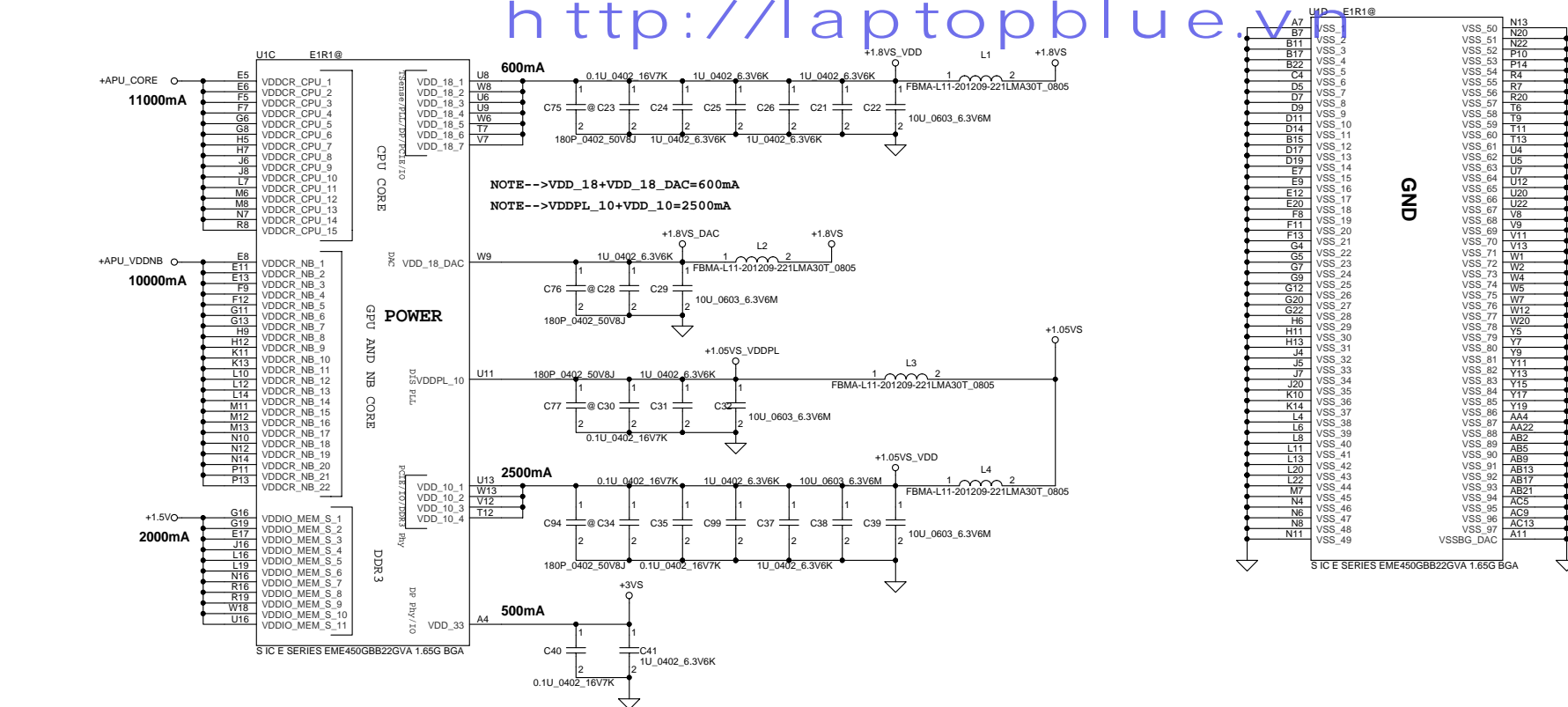
8/6 Add C78 for ESD request



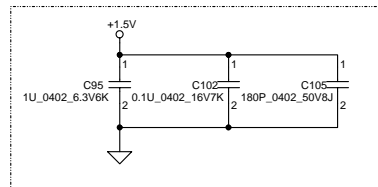


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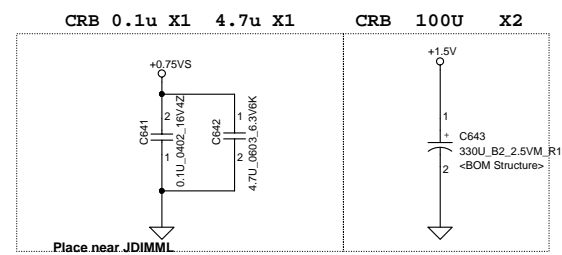
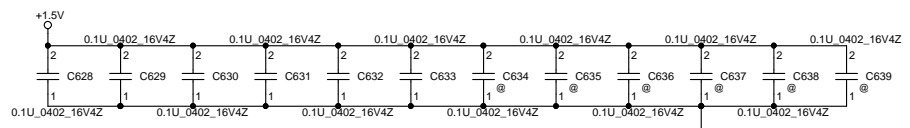
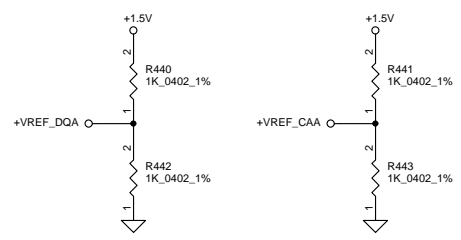
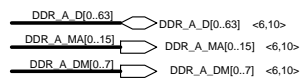
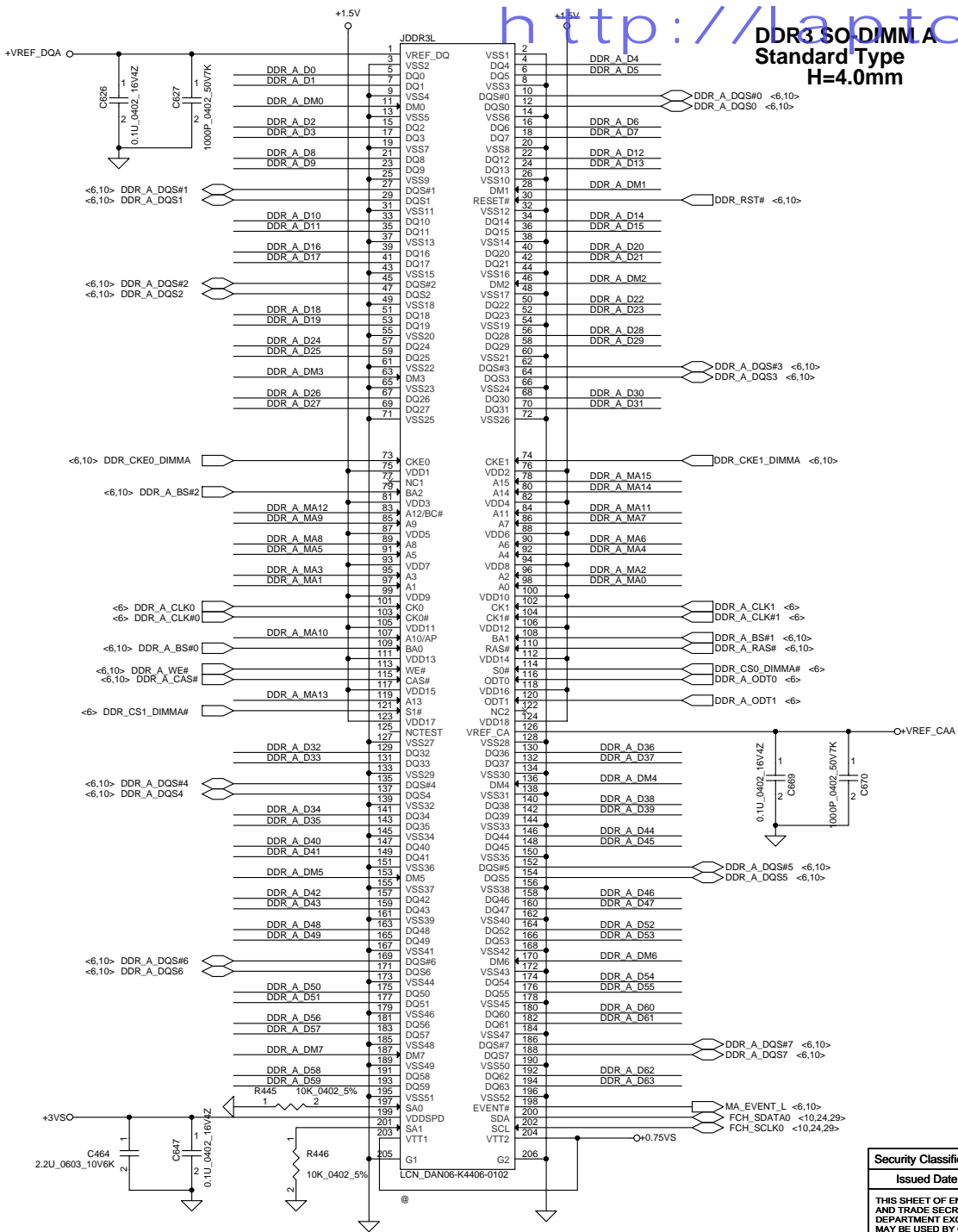


Add for EMI request on DVT



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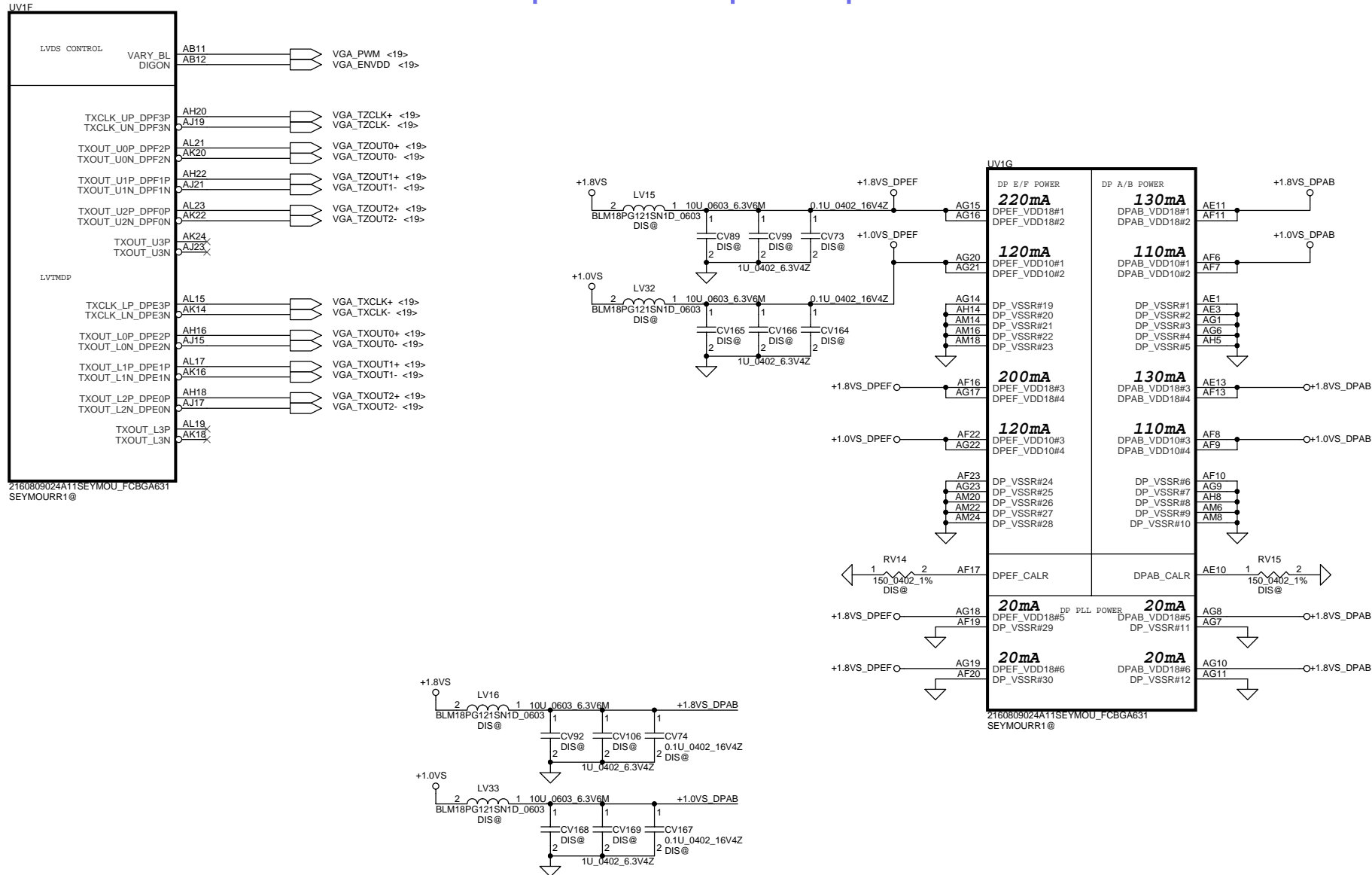
DDR3 SO DIMM A
Standard Type
H=4.0mm



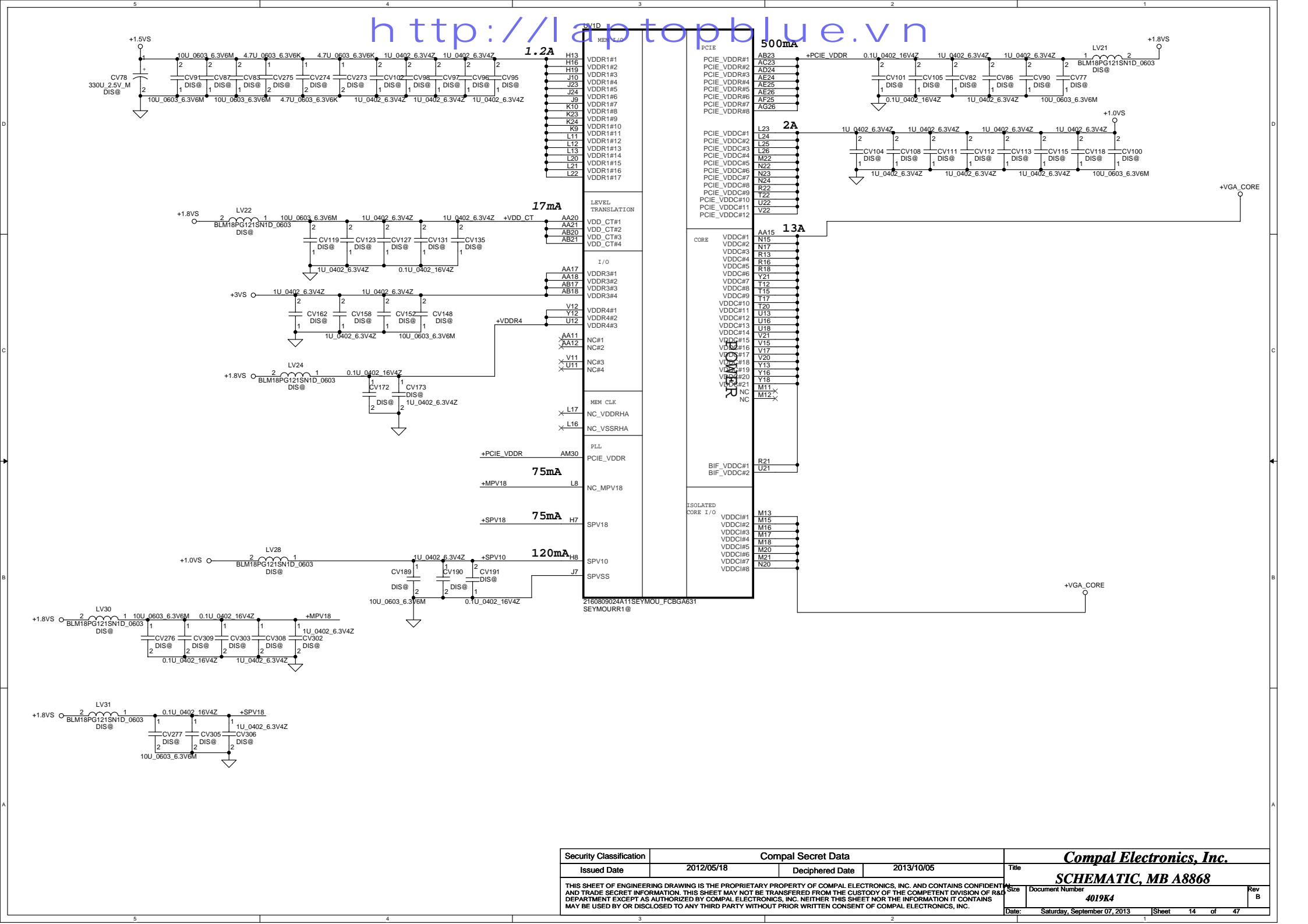
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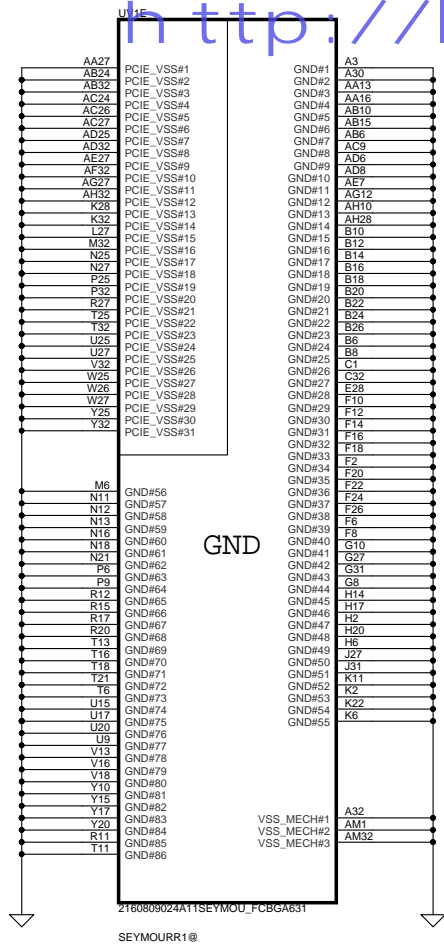
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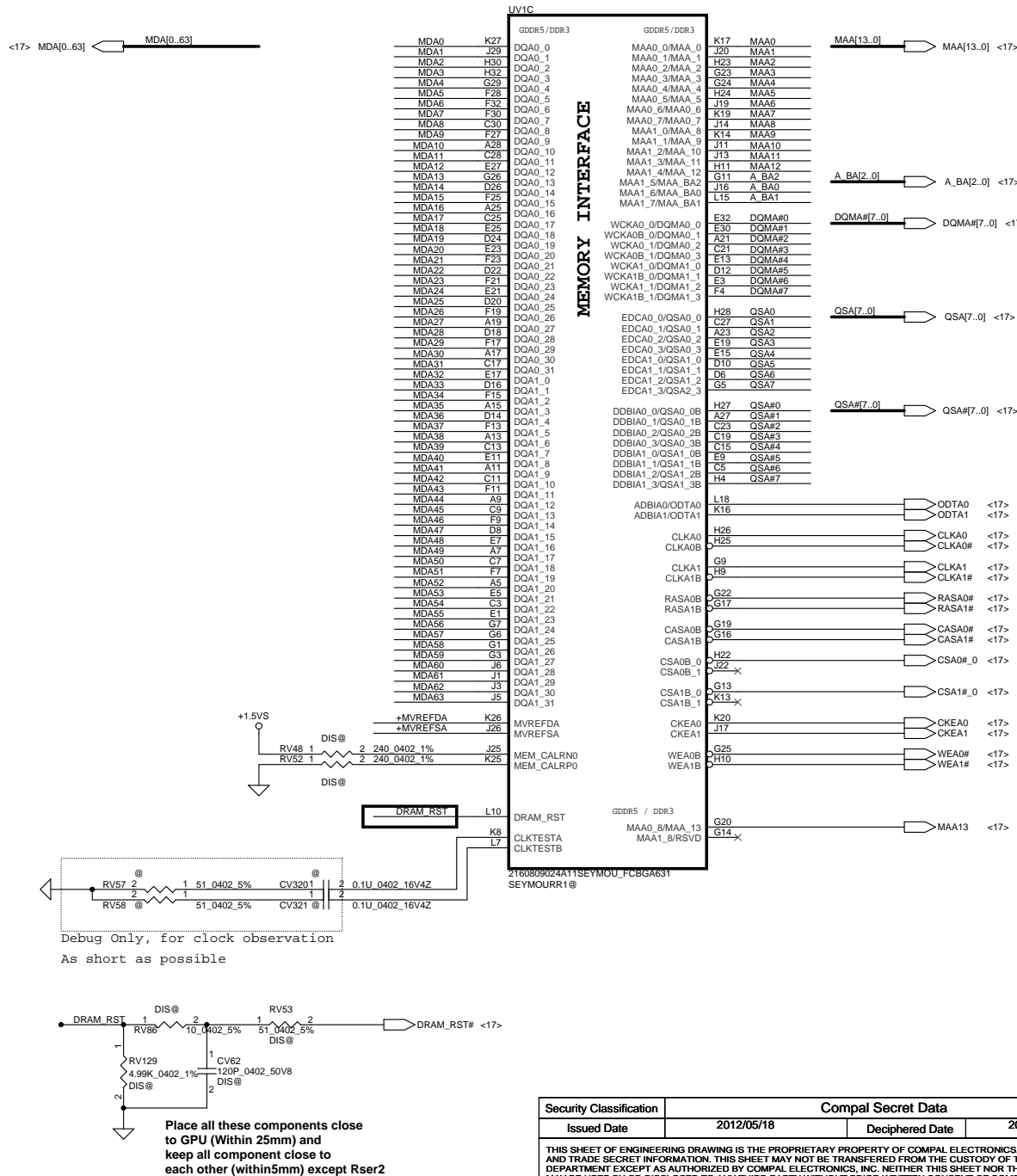


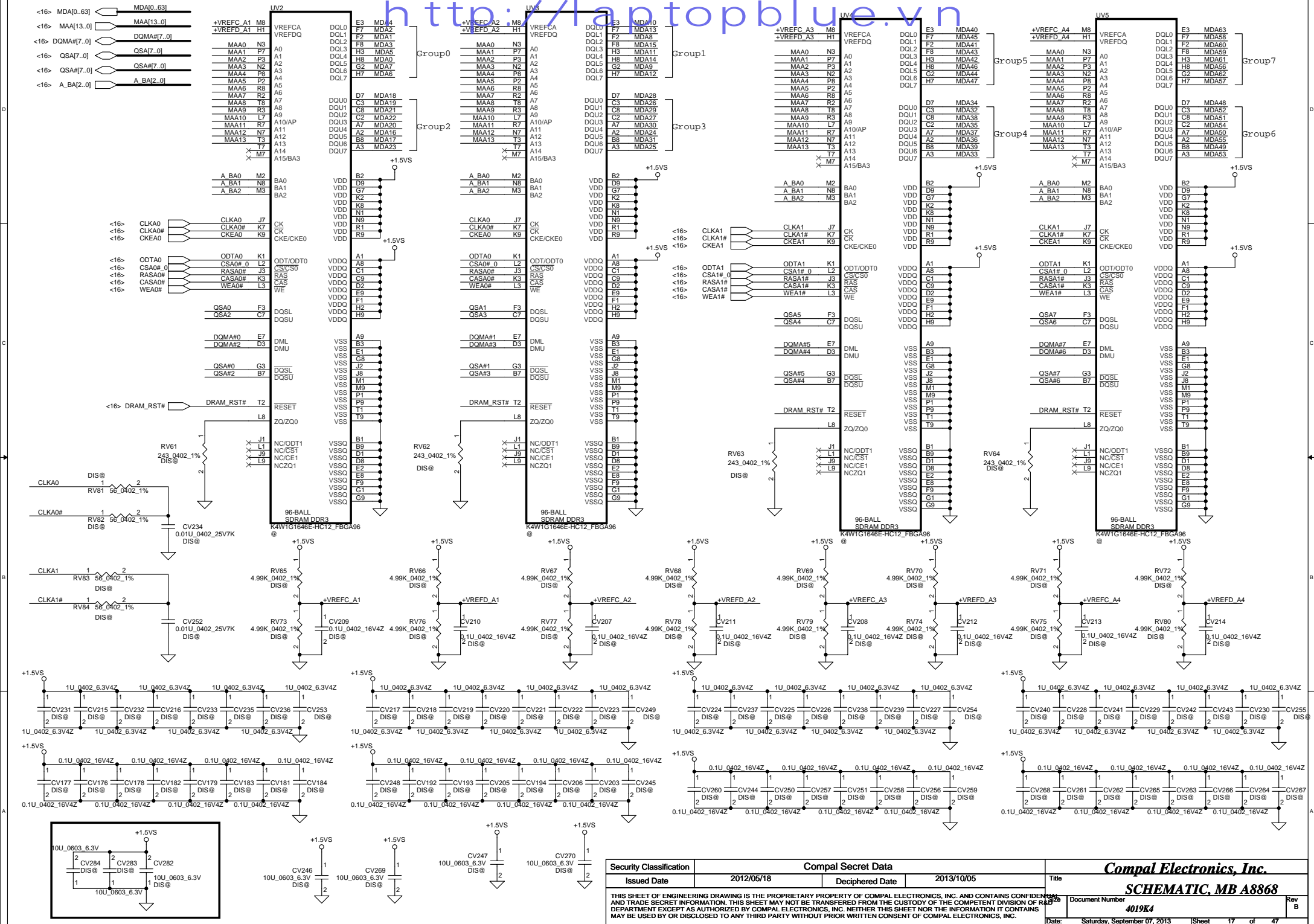
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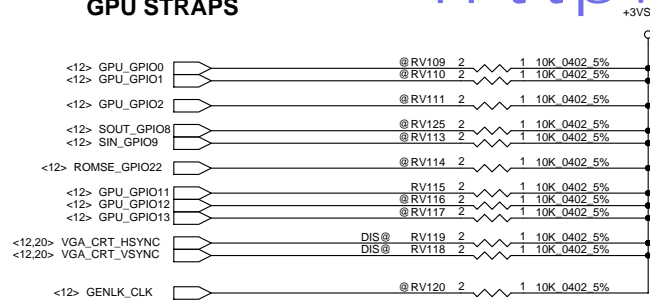






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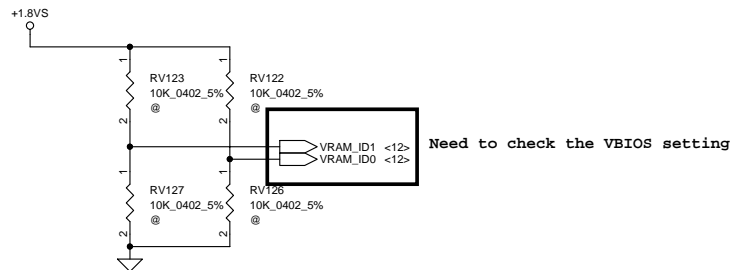
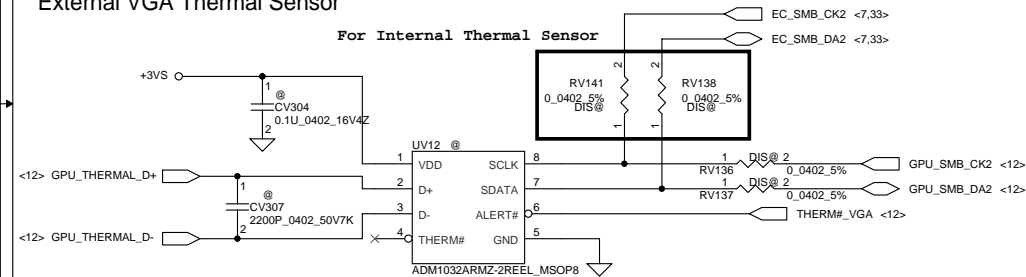
GPU STRAPS



GPU by the system BIOS		GPU by VBIOS
GPIO22 = 0 (BIOS_ROM_EN = 0)		GPIO22 = 1 (BIOS_ROM_EN = 1)
GPIO[13:11]	MEMORY SIZE	GPIO[13:11]
0 0 0	128MB	1 0 0
0 0 1	256MB	(M25P05A)
0 1 0	64MB	

External VGA Thermal Sensor

For Internal Thermal Sensor



Need to check the VBIOS setting

CONFIGURATION STRAPS

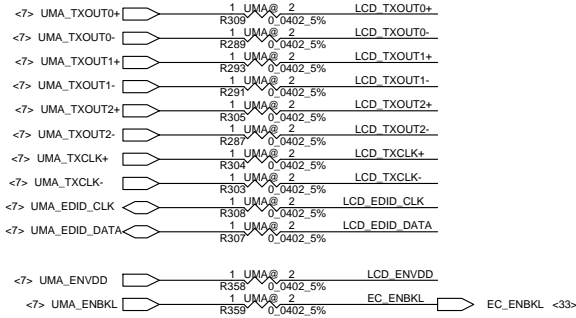
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

Straps Name	Pin Name	Net Name	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	GPU_GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	0
TX_DEEMPH_EN	GPIO1	GPU_GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	0
BIF_GEN2_EN_A	GPIO2	GPU_GPIO2	PCIE GNE2 ENABLED 0 = Advertises the PCIe device as 2.5 GT/s capable at power-on 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	0 5.0 GT/s capability will be controlled by software
RESERVED	GPIO_8_ROMSO	SOUT_GPIO8	RESERVED	0
RESERVED	GPIO_21_BB_EN	N.C	RESERVED	0 (Internal pulldown)
VGA_DIS	GPIO_9_ROMSI	SIN_GPIO9	VGA Controller 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0 (Enable)
BIOS_ROM_EN	GPIO_22_ROMCSB	ROMSE_GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0
CONFIG(2:0)	GPIO[13:11]	GPU_GPIO11 GPU_GPIO12 GPU_GPIO13	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size.	0 0 1 (256M)
RESERVED	GENLK_CLK	GENLK_CLK		0
AUD[1] AUD[0]	HSYNC VSYNC	VGA_CRT_HSYNC VGA_CRT_VSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	0 0

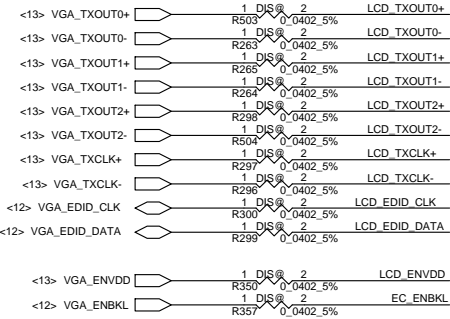
STRAPS	PIN	GPU	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 1,0
VRAM_ID[1:0]	DVDATA (1,0)	Seymour-S3	512M 64Mx16 (x4)	SAM K4W1G1646G-BC11	SA00004GS00	1 0
			1G 128Mx16 (x4)	SAM K4W2G1646C-HC11	SA000047Q00	1 1

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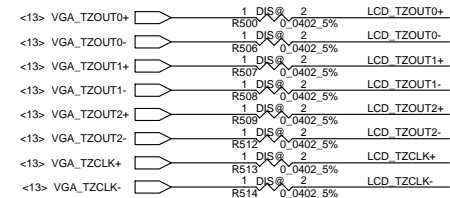
UMA



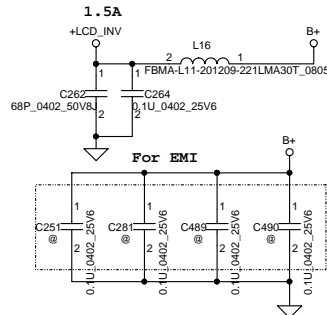
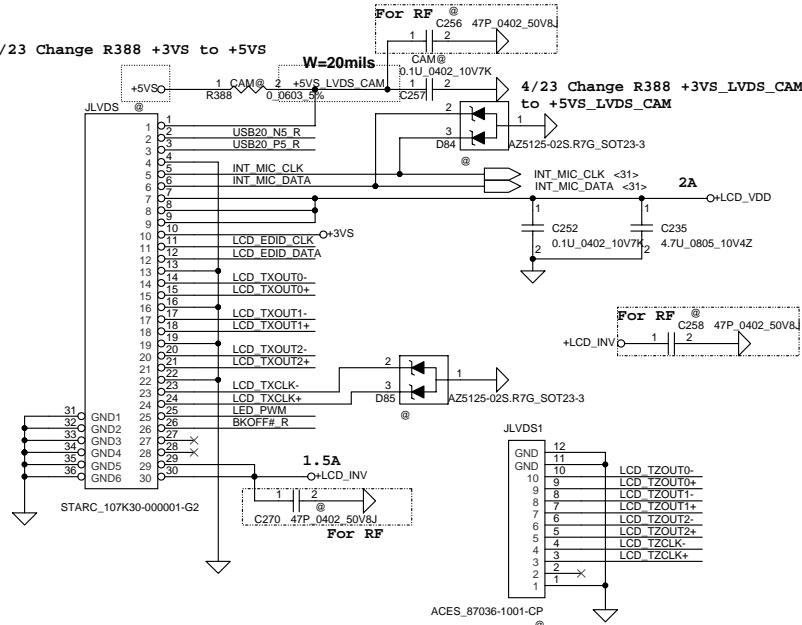
DISCRETE



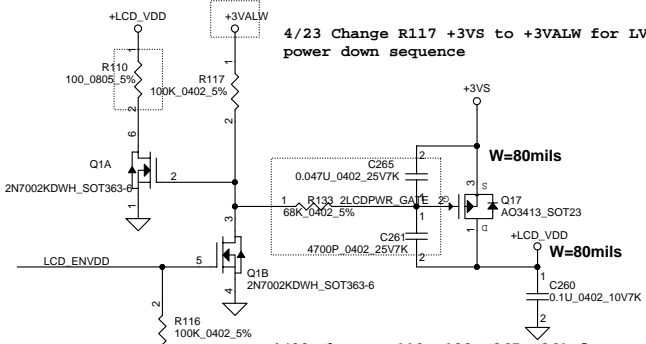
Close to LVDS Connector



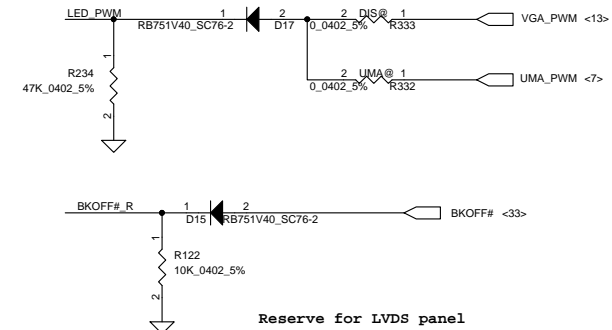
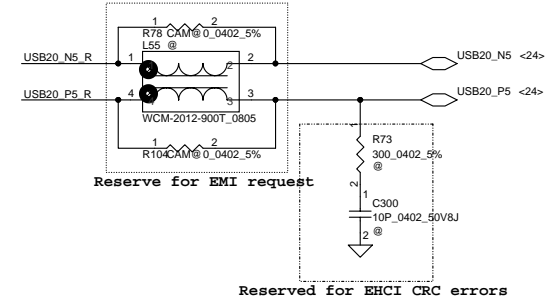
4/23 Change R388 +3VS to +5VS



4/23 Change R117 +3VS to +3VALW for LVDS power down sequence



4/23 Change R110,R133,C265,C261 for LVDS power down sequence

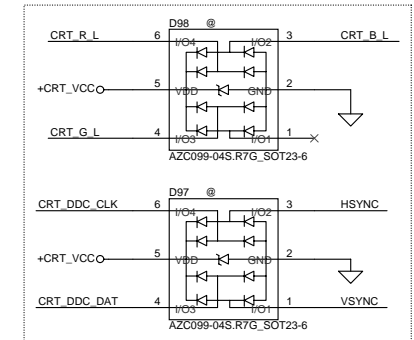
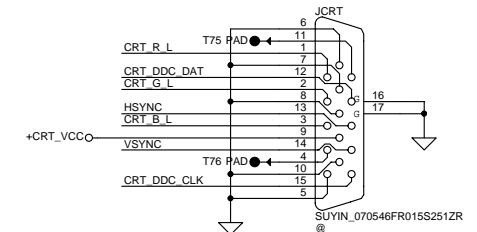
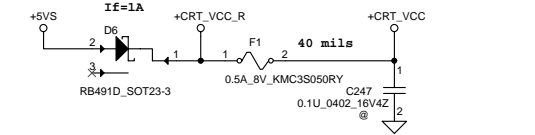


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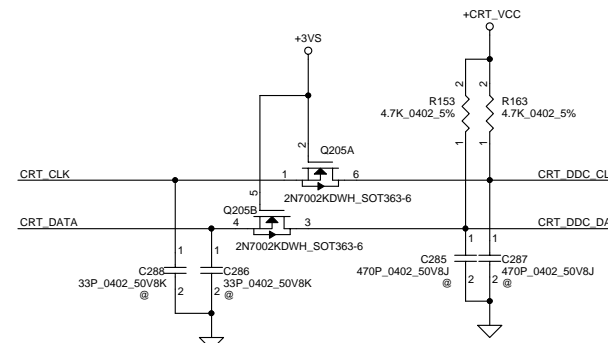
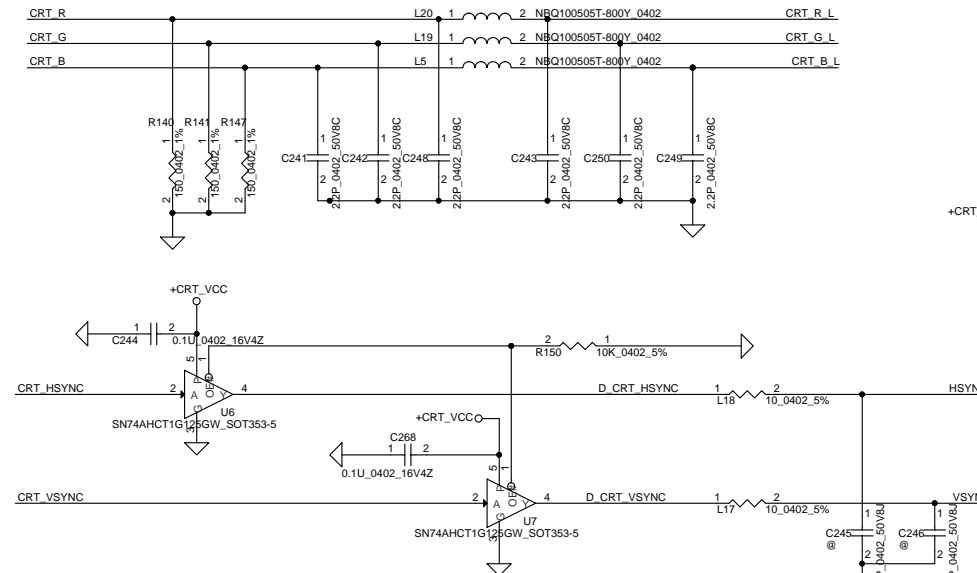
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CRT CONNECTOR

Remove D3~D5 on DVT



Reserve ESD for CRT connector on DVT



UMA

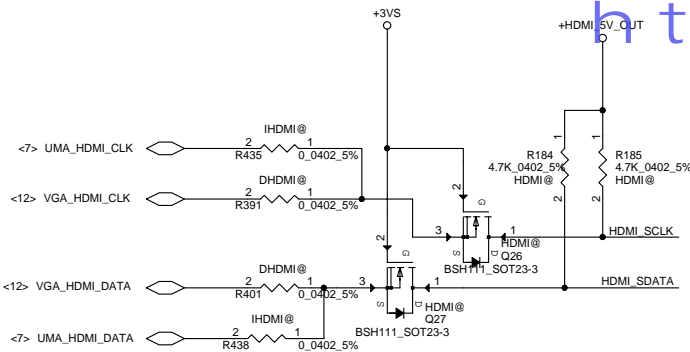
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<7> UMA_CRT_G	1 UMA@ 2	CRT_G
<7> UMA_CRT_B	1 UMA@ 2	CRT_B
<7> UMA_CRT_HSYNC	1 UMA@ 2	CRT_HSYNC
<7> UMA_CRT_VSYNC	1 UMA@ 2	CRT_VSYNC
<7> UMA_CRT_CLK	1 UMA@ 2	CRT_CLK
<7> UMA_CRT_DATA	1 UMA@ 2	CRT_DATA

Close to CRT Connector

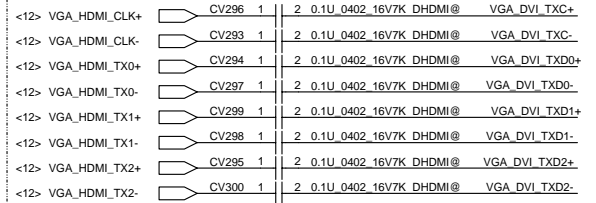
DISCRETE

<12> VGA_CRT_R	1 DIS@ 2	CRT_R
<12> VGA_CRT_G	1 DIS@ 2	CRT_G
<12> VGA_CRT_B	1 DIS@ 2	CRT_B
<12,18> VGA_CRT_HSYNC	1 DIS@ 2	CRT_HSYNC
<12,18> VGA_CRT_VSYNC	1 DIS@ 2	CRT_VSYNC
<12> VGA_CRT_CLK	1 DIS@ 2	CRT_CLK
<12> VGA_CRT_DATA	1 DIS@ 2	CRT_DATA

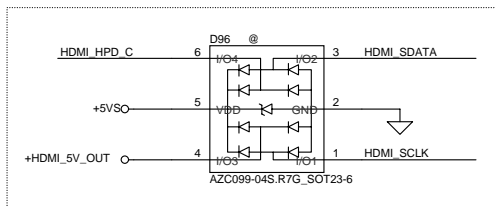
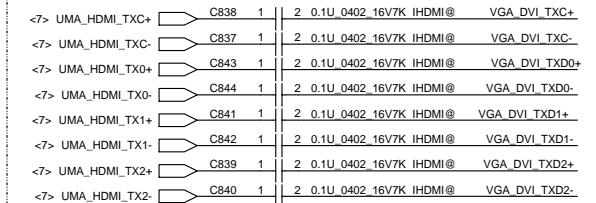
Close to CRT Connector



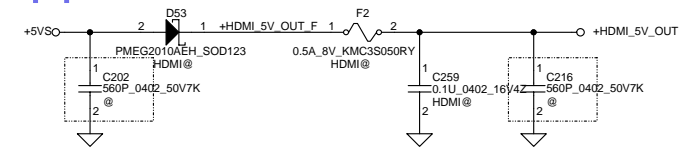
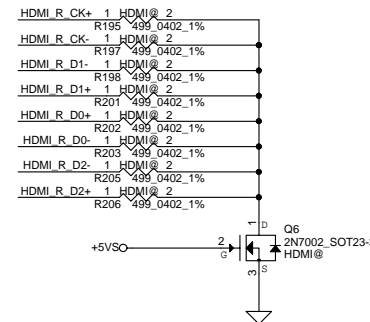
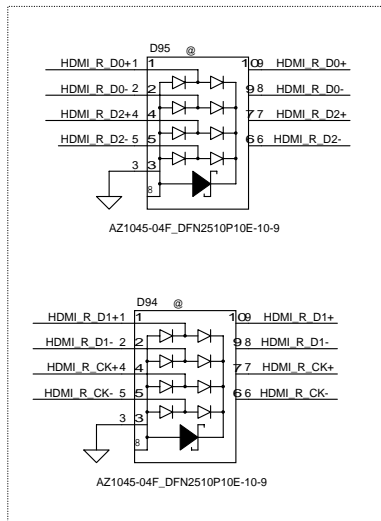
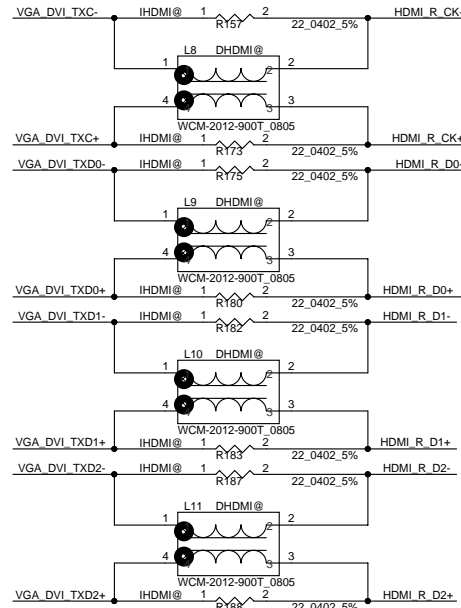
DISCRETE



UMA

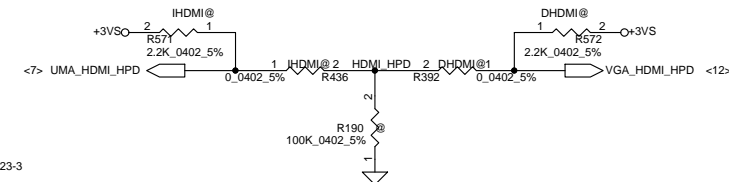
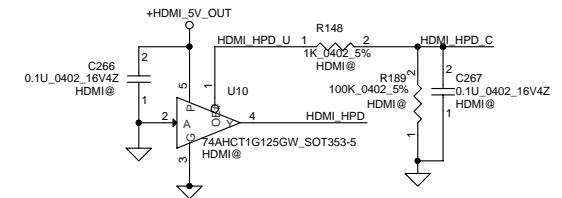
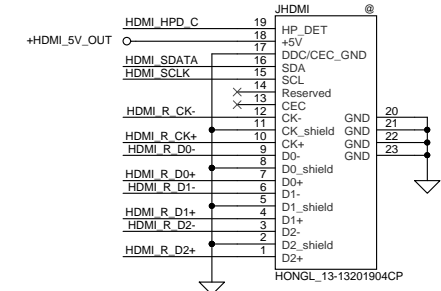


Reserve ESD for HDMI conn. on DVT



4/23 Add C202 and C216 for EMI request

HDMI Connector



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Compal Electronics, Inc.

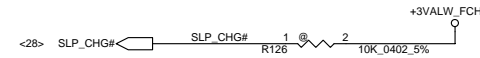
SCHEMATIC, MB A8868



Check

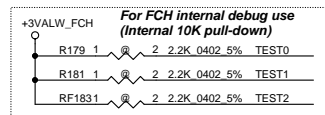
FCH_SPI_CS1# 1 2 +3VALW_FCH

R115 10K 0402 5% from QMLE4

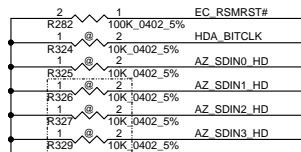


Compal Electronics, Inc.			
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DESIGN NO.	Document Number	Rev B	
OF RATINGS	Custom	4019K4	
Date:	Saturday, September 07, 2013	Sheet	23 of 47

PCIE_RST2: Reset PCIE device on Hudson 3

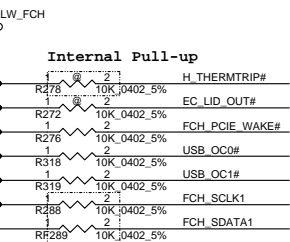


SM Bus 0-->S0 PWR domain--> SO-DIMM, WLAN
SM Bus 1-->S5 PWR domain--> no use

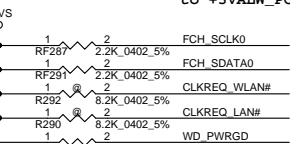


12/22 Reserve R326,R327,R329 but
AMD have internal pull down

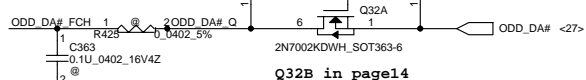
USB_OC1# is for left USB3.0 ports
USB_OC0# is for right USB2.0 ports



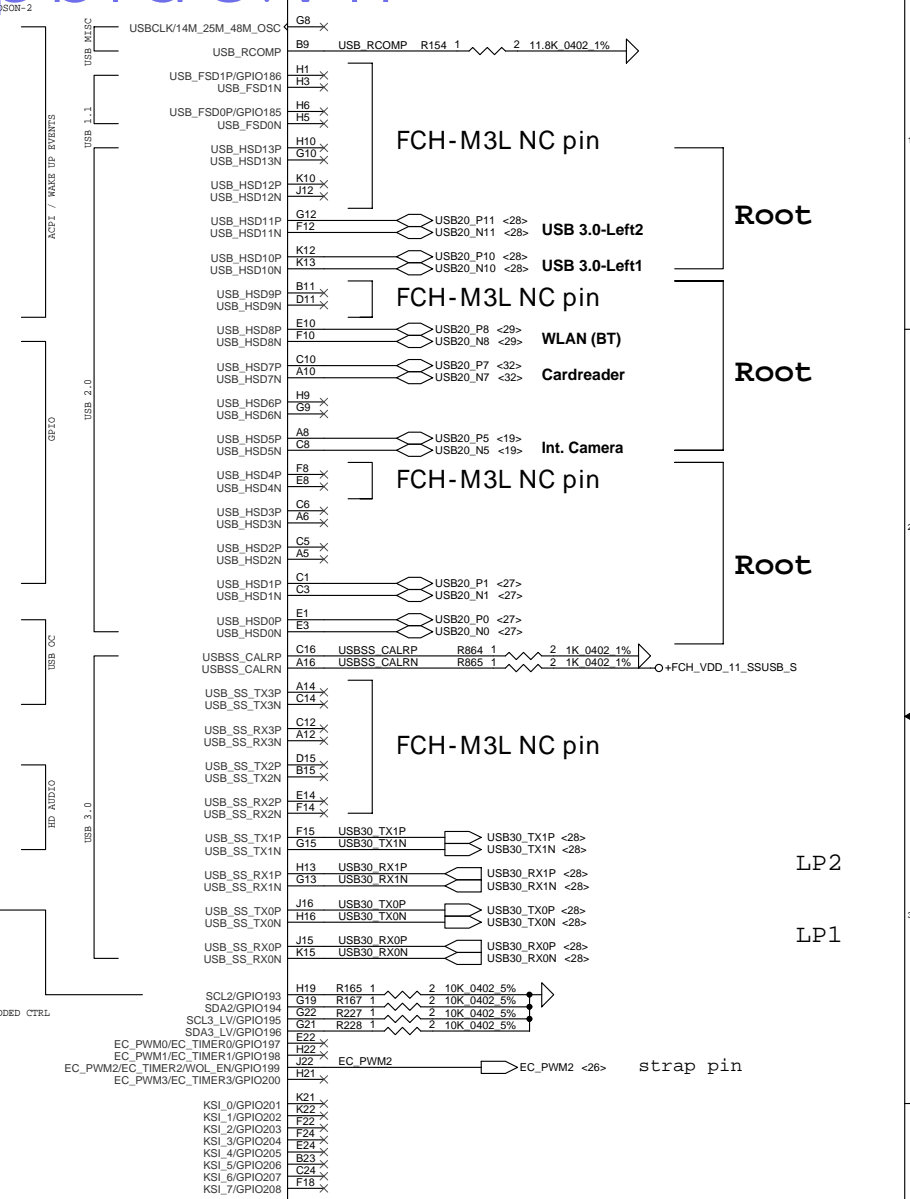
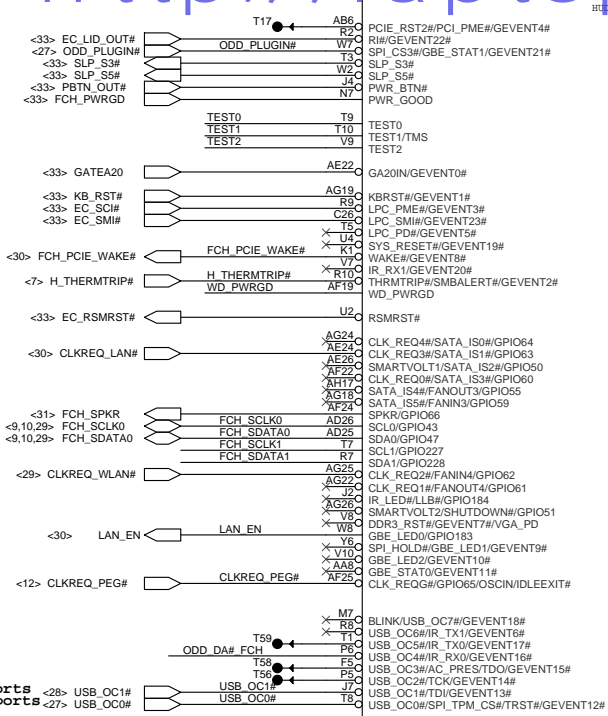
12/22 SMBus Not Implemented use 10k pull up
to +3VALW_PCH



Place R425 and C363
close to FCH for ESD



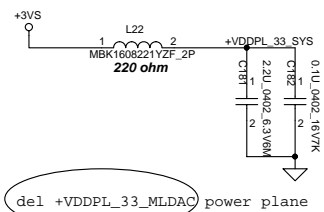
Q32B in page14



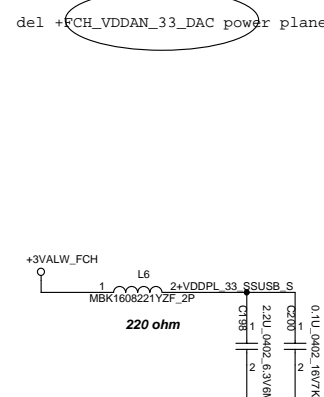
218-0755091 A13 HUDSON-M3L FCBGA 656P C38

M3LR1@

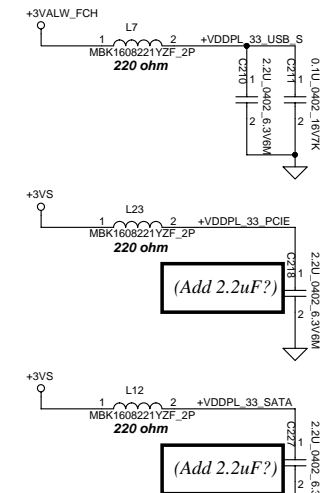
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(del +VDDPL_33_MLDAC) power plane

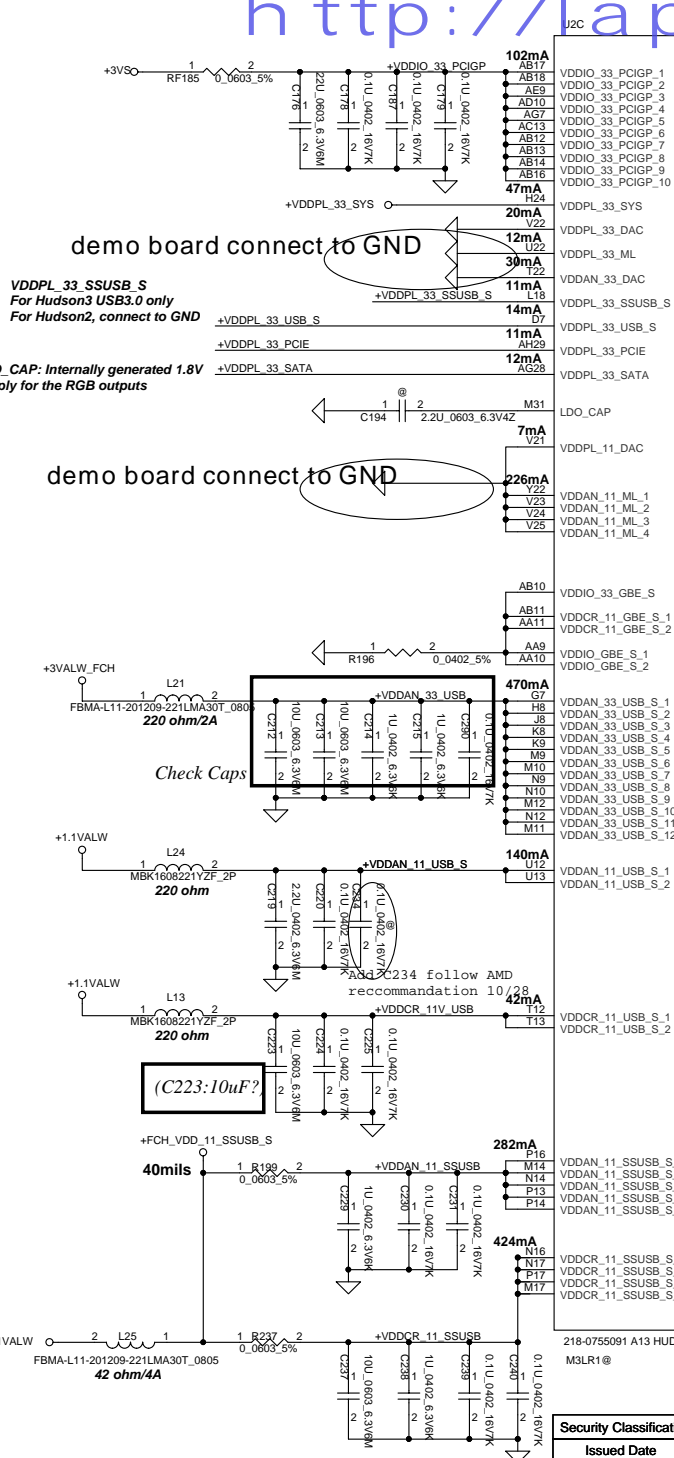


```
del +FCH_VDDAN_33_DAC power plane
```



(Add $2.2\mu F$?)

(Add $2.2\mu F$?)



demo board connect to GND

VDDPL_33_SSUSB_S
For Hudson3 USB3.0 only
For Hudson2, connect to GND

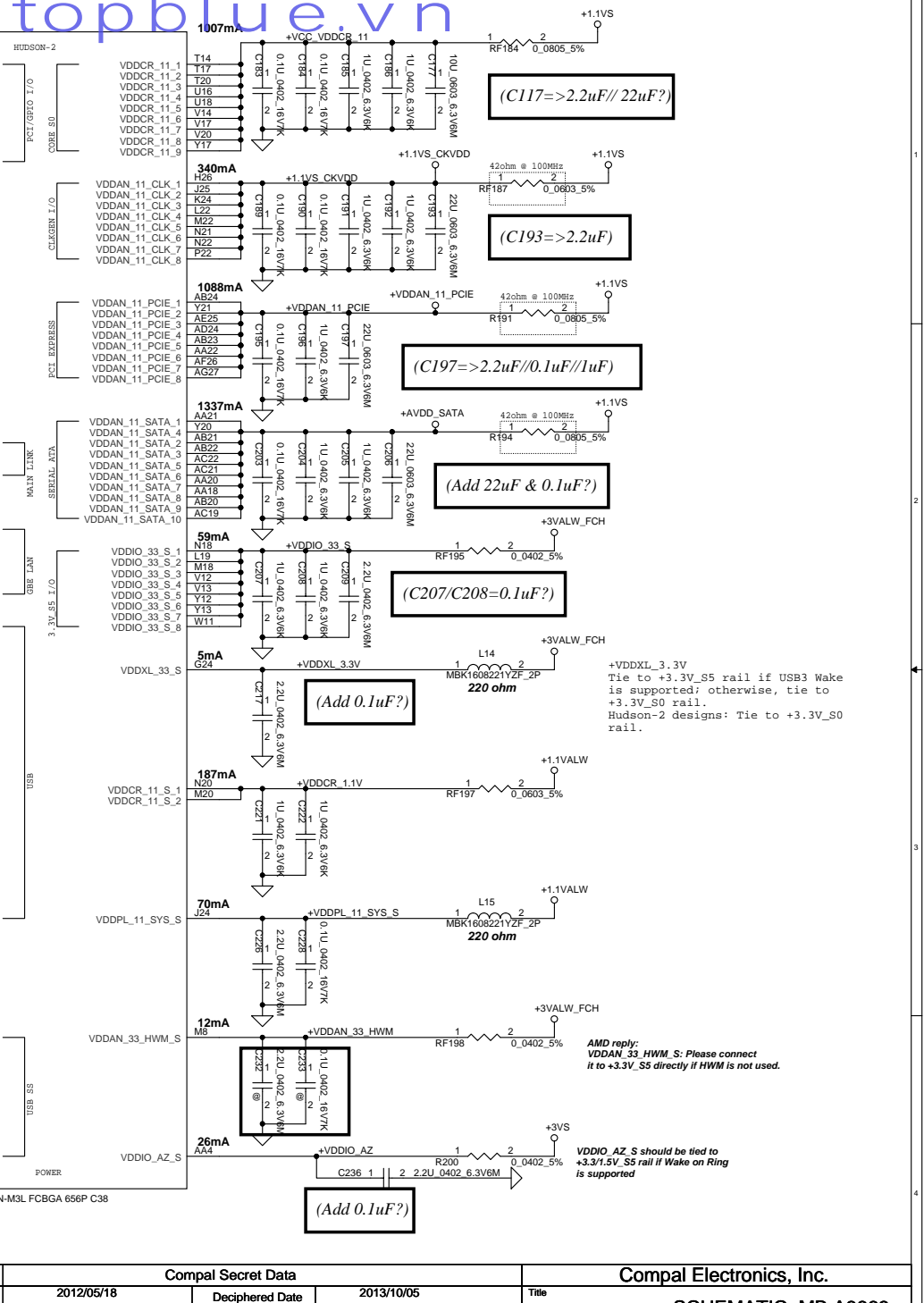
LDO_CAP: Internally generated 1.8V supply for the RGB outputs

demo board connect to GND

Check Caps

Add C234 follow AM
recommandation 10

(C223:10uF:



(C117=>2.2uF// 22uF?)

(C193=>2.2uF)

(C197=>2.2uF//0.1uF//1uF)

(Add 22uF & 0.1uF?)

(C207/C208=0.1uF?)

(Add 0.1uF?)

Tie to +3.3V_S5 rail if USB3 Wake is supported; otherwise, tie to +3.3V_S0 rail.
Hudson-2 designs: Tie to +3.3V_S0 rail.

AMD reply:
VDDAN_33_HWM_S: Please connect it to +3.3V S5 directly if HWM is not used.

VDDIO_AZ_S should be tied to +3.3/1.5V_S5 rail if Wake on Ring is supported

(Add $0.1\mu F$?)

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				Document Number		4019K4	
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http://laptopblue.vn

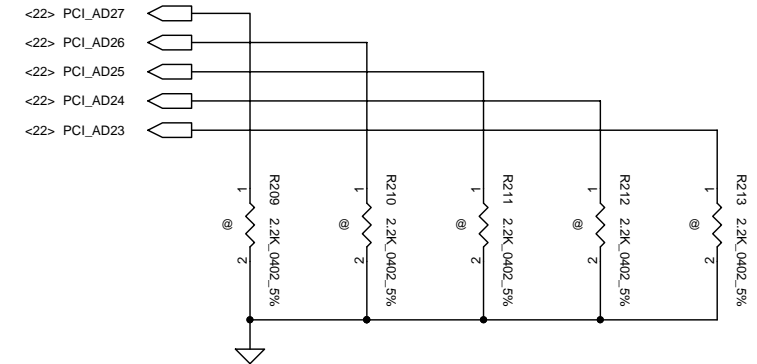
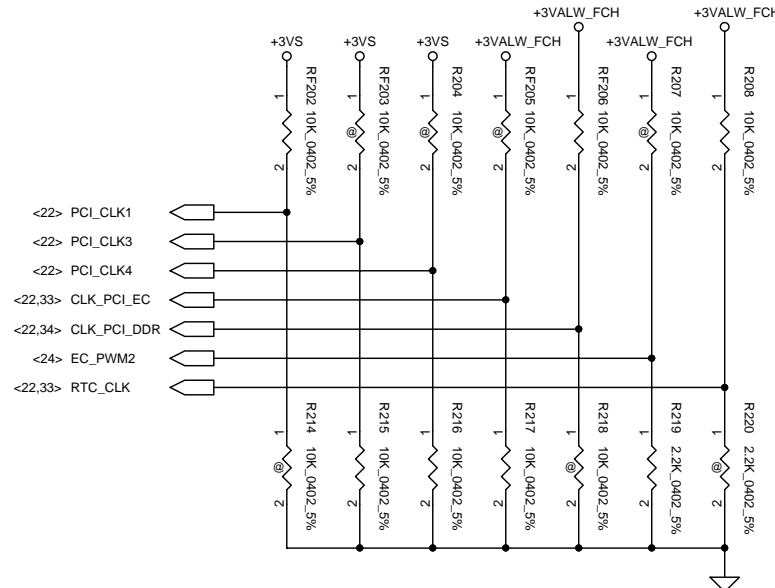
DEBUG STRAPS

STRAP PINS

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

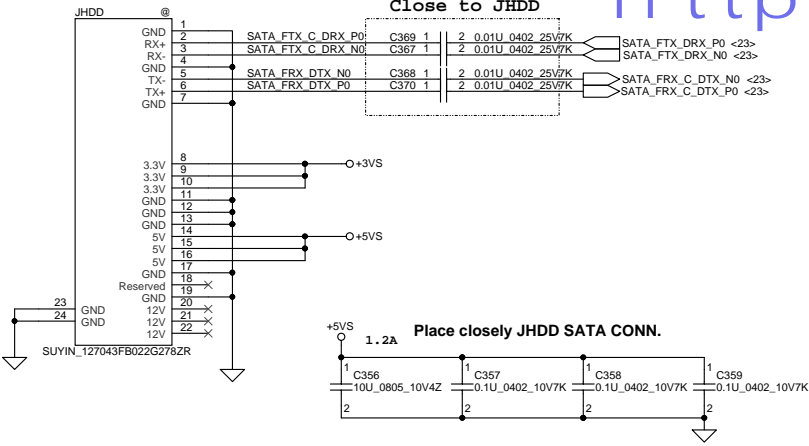


218-0755091 A13 HUDSON-M3L FCBGA 656P C36

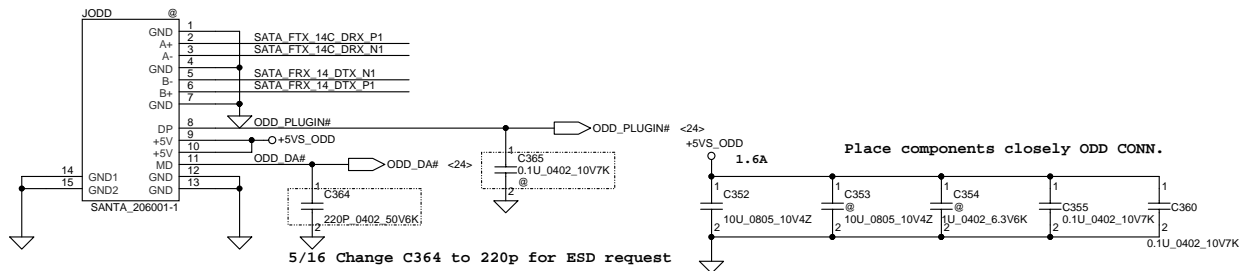
M3LR1@

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				Date:	Saturday, September 07, 2013
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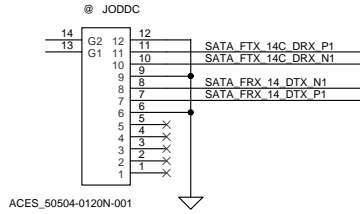
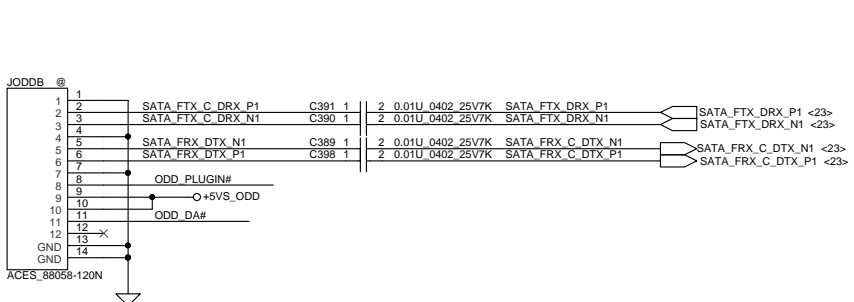
SATA HDD Conn.



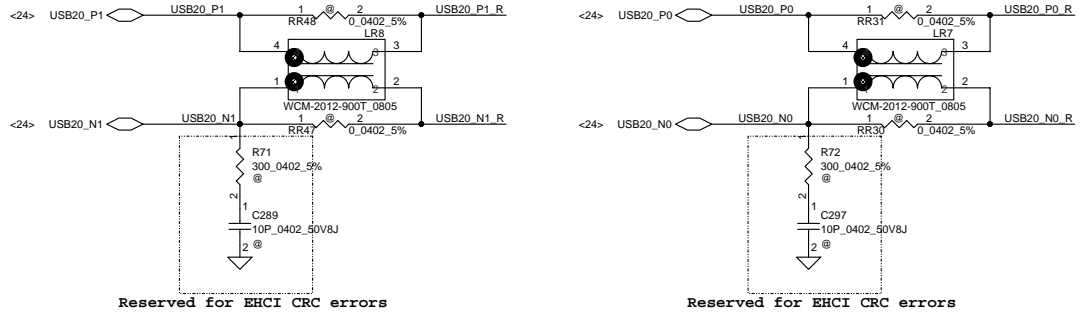
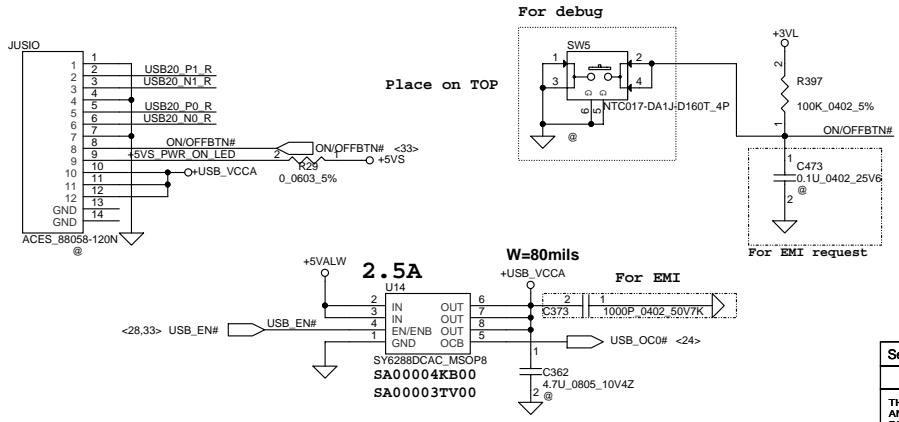
SATA ODD Conn (for 14")



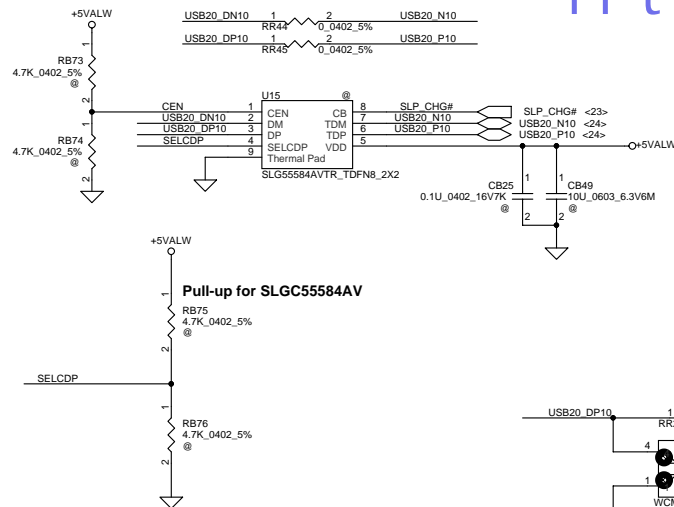
SATA ODD Conn (for 15")



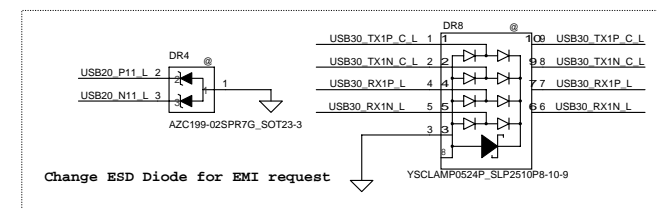
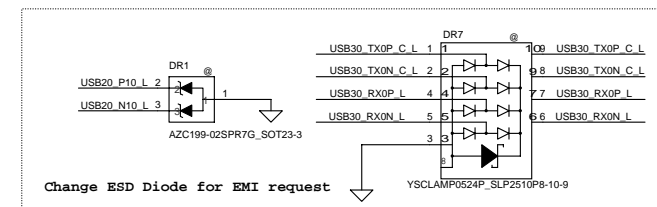
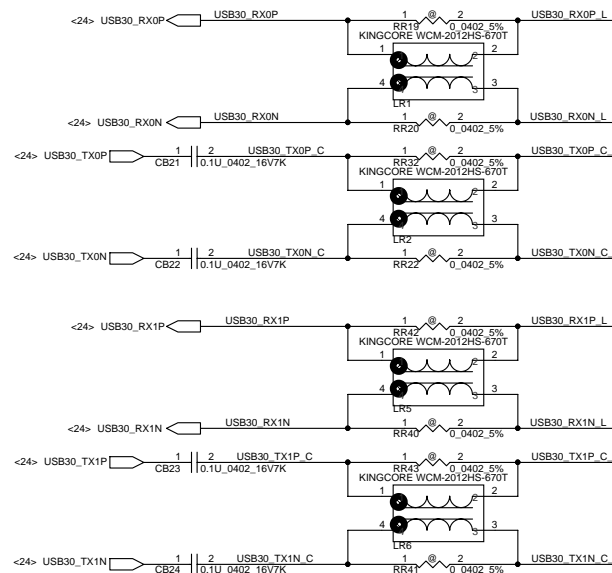
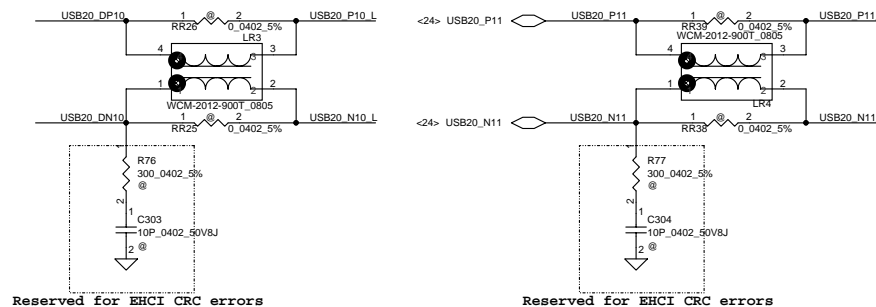
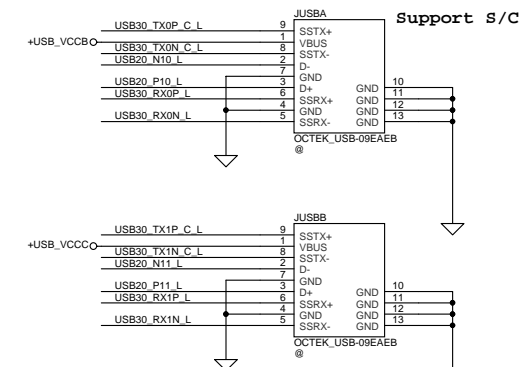
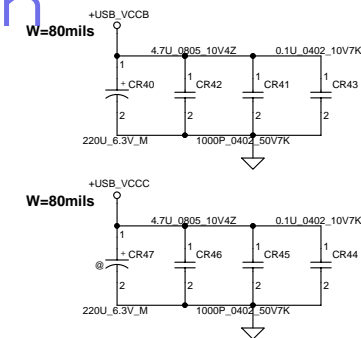
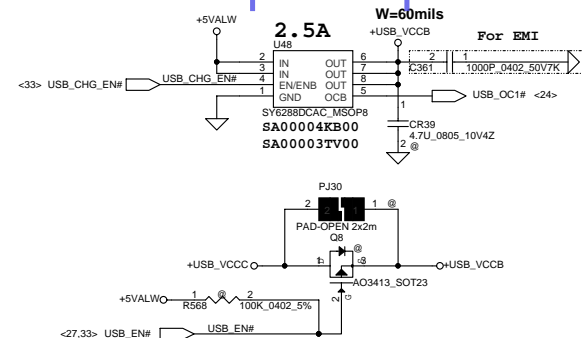
Power Button & RUSB connector



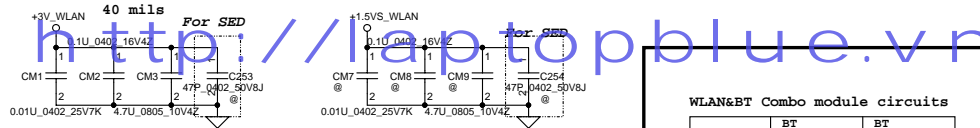
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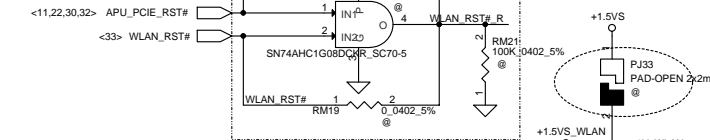
SLP_CHG#	SELCDP	Function
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only



Slot 1 Half PCIe Mini Card-WLAN

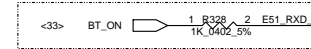


Add WLAN_RST# on DVT



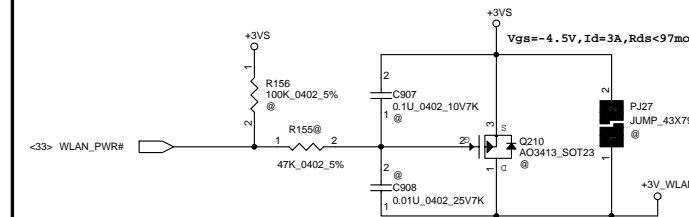
WLAN&BT Combo module circuits

	BT on module	BT on module
	Enable	Disable
BT_ON	H	L



For isolate BT_CTRL and Compal Debug Card.

+3VALW TO +3V_WLAN

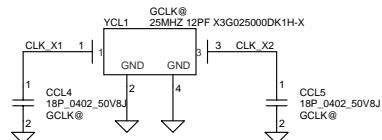
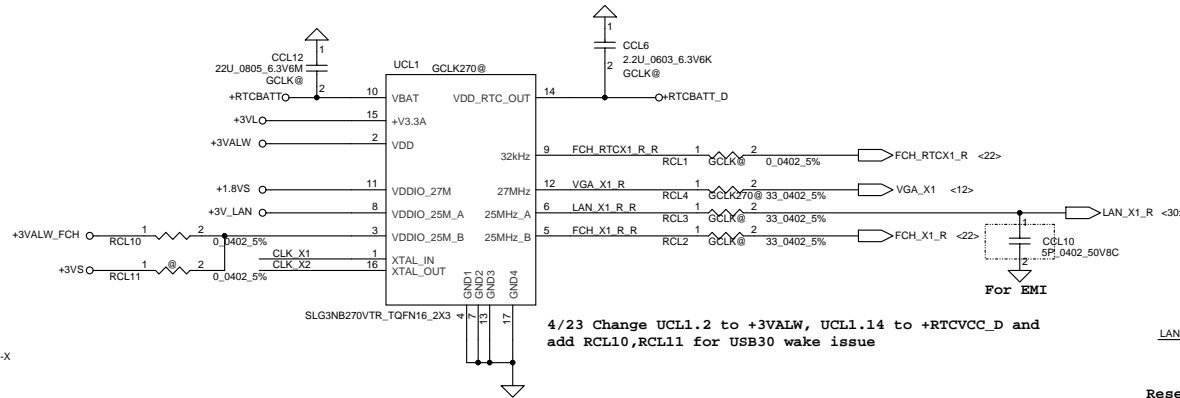
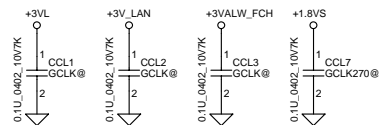


Add WLAN power circuit on DVT

Change JWLAN symbol to SP07000TB00 on DVT

Reserved for EHCI CRC errors

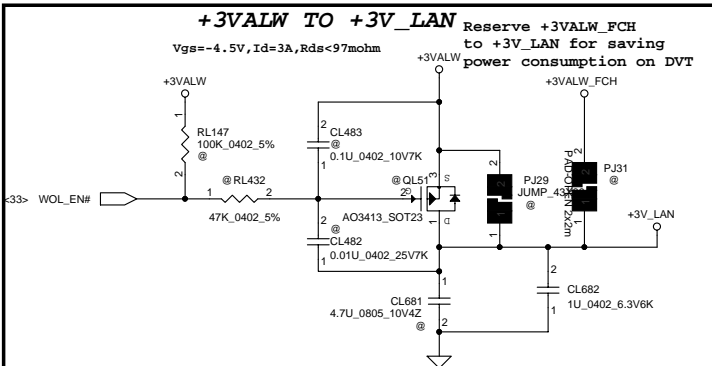
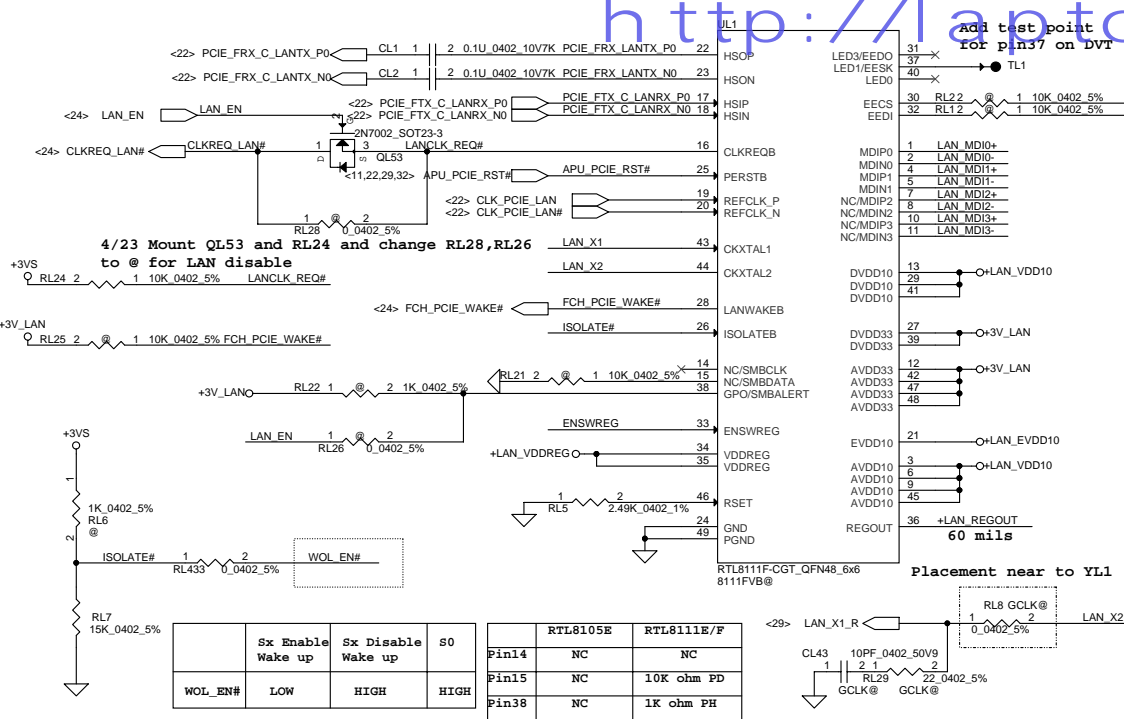
Green Clock Generator



For UMA



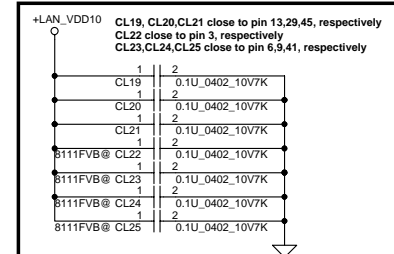
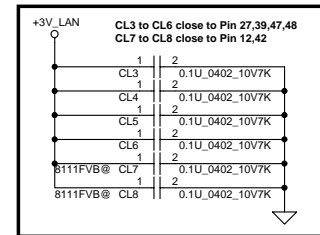
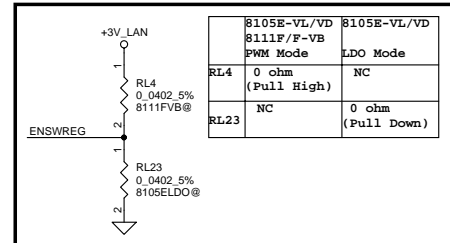
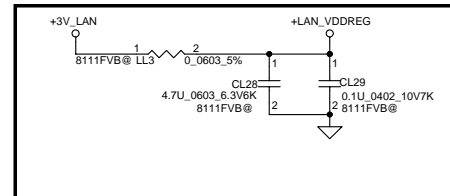
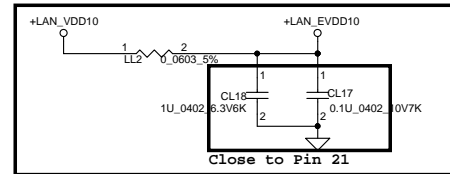
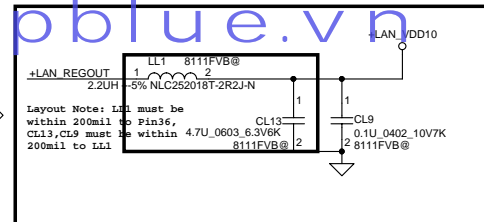
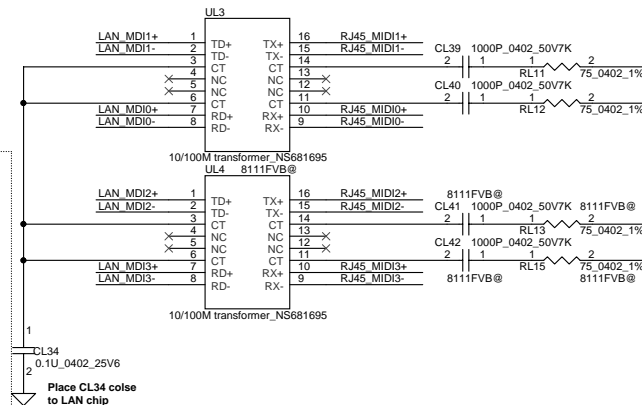
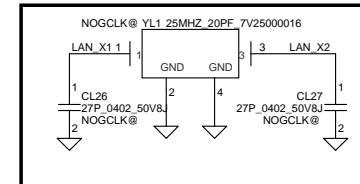
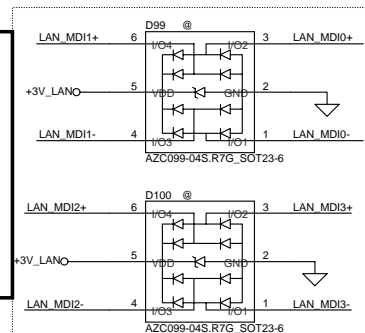
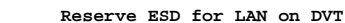
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				Date:	Saturday, September 07, 2013	Sheet 29 of 47



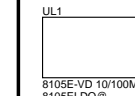
+3V_LAN rising time (10%~90%) need > 1ms and <100ms.

LAN	WOL	LAN_EN		ISOLATEB	
		S0	Sx	S0	Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

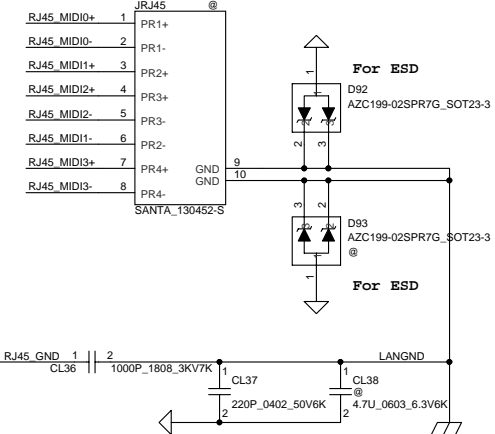
```
*
S3:  after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms
```



For P/N and footprint
Please place them to ISPD page



LAN Conn.

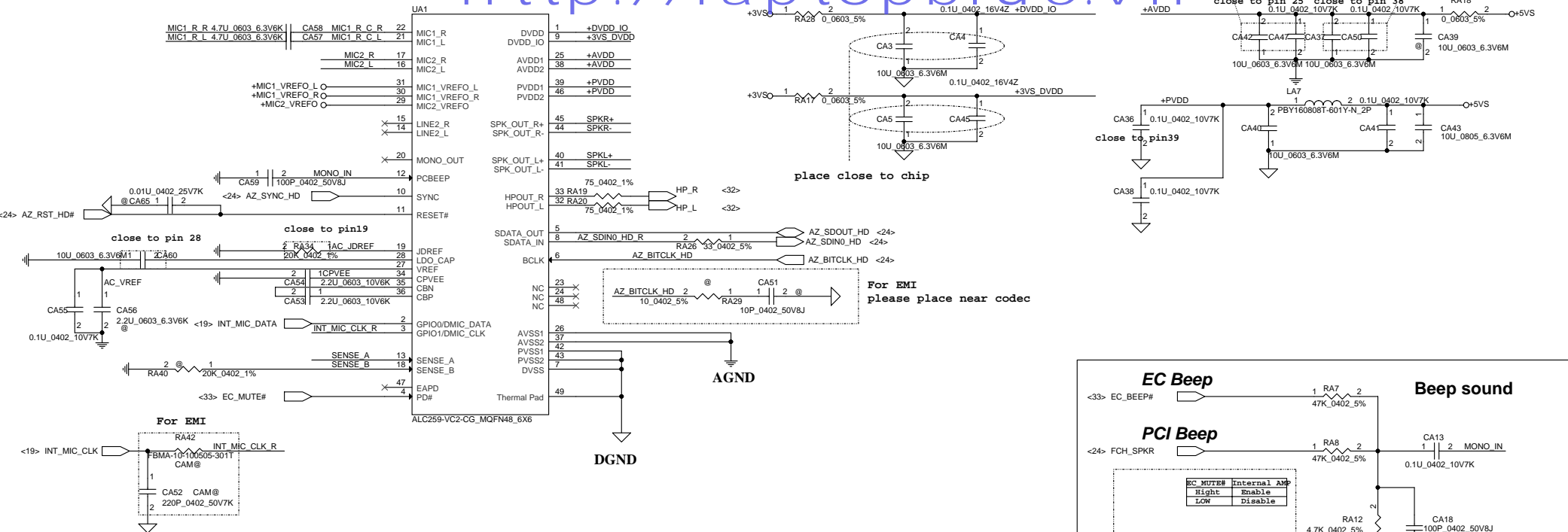


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Issued Date	2012/05/18	Deciphered Date	2013/10/05

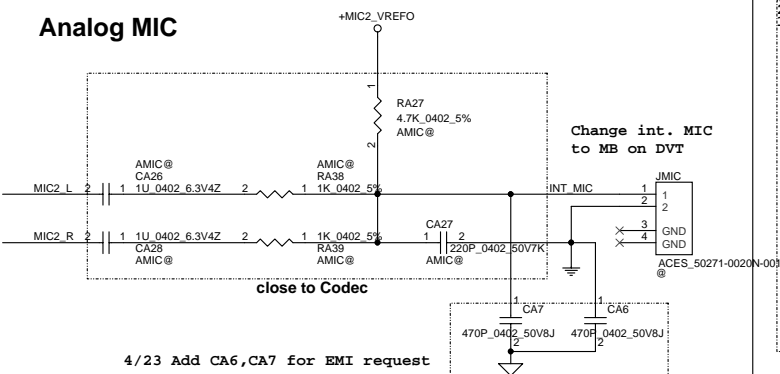
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Title			
SCHEMATIC, MB A8868			
NEED 228 Rack Custom	Document Number		Rev B
	4019K4		
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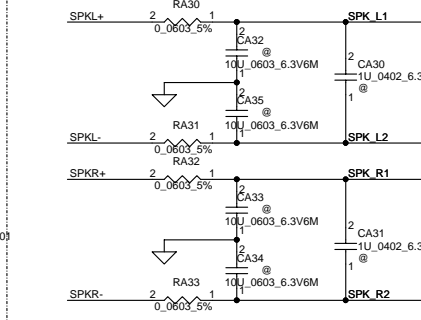
35mA for 3.3V level



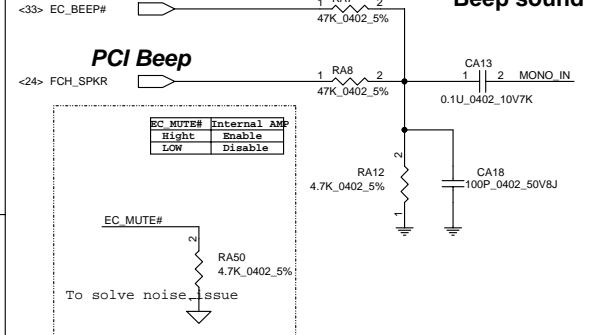
Analog MIC



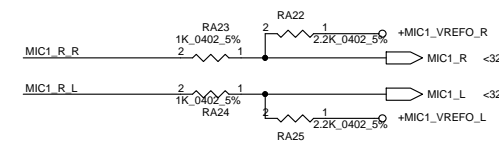
placement near Audio Codec



EC BEEP

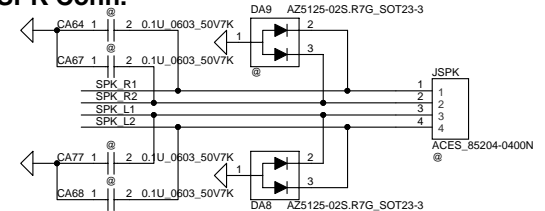


Ext.MIC/LINE IN JACK



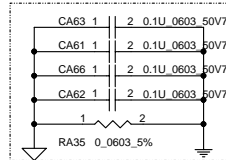
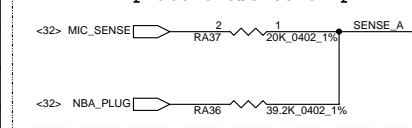
SPK Conn.

4/23 Add CA64,CA67,CA68,CA77 for EMI request



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Analog MIC
	10K	PORT-H (PIN 20)	

place close to chip



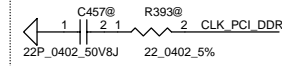
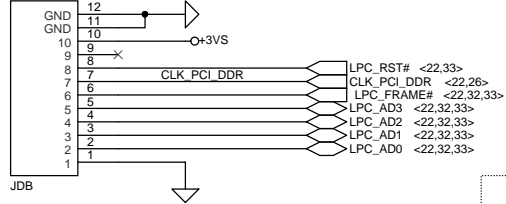
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SCHEMATIC, MB A8868				
4019K4				
Date: Saturday, September 07, 2013				
Sheet 31 of 47				

LPC Debug Port

Place the PAD under DDR DIMM.

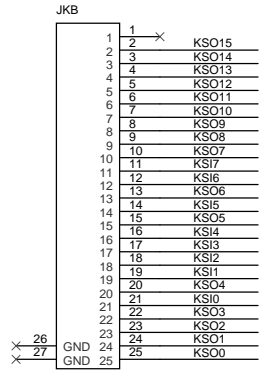
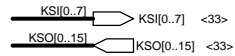
<http://laptopblue.vn>

@
E-T_3801K-F10N-01L



For EMI

KEYBOARD CONN.



ACES_50524-02501-001
@

For EMI

Close to JKB

KSO2	1	2
C404	1	100P_0402_50V8J
KSO1	2	1
C405	2	100P_0402_50V8J
KSO0	1	2
C406	1	100P_0402_50V8J
KSO4	2	1
C407	2	100P_0402_50V8J
KSO3	1	2
C408	1	100P_0402_50V8J
KSO5	2	1
C409	2	100P_0402_50V8J
KSO14	1	2
C410	1	100P_0402_50V8J
KSO6	2	1
C411	2	100P_0402_50V8J
KSO7	1	2
C412	1	100P_0402_50V8J
KSO13	2	1
C413	2	100P_0402_50V8J
KSO8	1	2
C415	1	100P_0402_50V8J
KSO9	2	1
C416	2	100P_0402_50V8J
KSO10	1	2
C417	1	100P_0402_50V8J
KSO11	2	1
C418	2	100P_0402_50V8J
KSO12	1	2
C419	1	100P_0402_50V8J
KSO15	2	1
C420	2	100P_0402_50V8J
KSI7	1	2
C421	1	100P_0402_50V8J
KSI2	2	1
C422	2	100P_0402_50V8J
KSI3	1	2
C423	1	100P_0402_50V8J
KSI4	2	1
C424	2	100P_0402_50V8J
KSI0	1	2
C425	1	100P_0402_50V8J
KSI5	2	1
C427	2	100P_0402_50V8J
KSI6	1	2
C429	1	100P_0402_50V8J
KSI1	2	1
C431	2	100P_0402_50V8J

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Rev

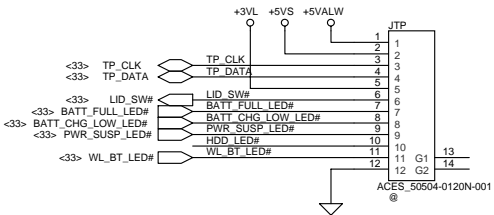
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Date: Saturday, September 07, 2013

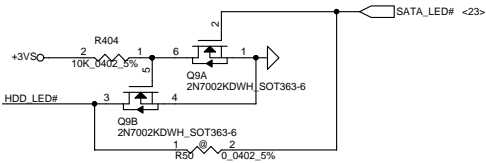
Sheet 34 of 47

Touchpad Connector
(Reserve 7 pins for LED & Win8 TP)

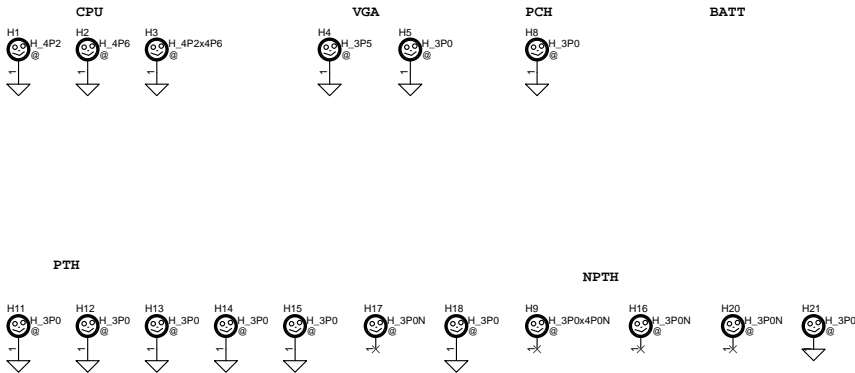
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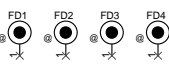
HDD LED



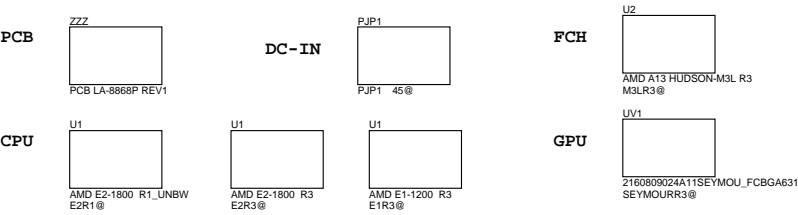
Screw Hole



PCB Fedical Mark PAD

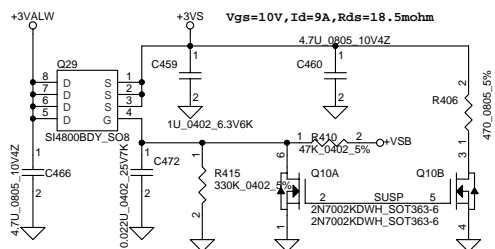


ISPD

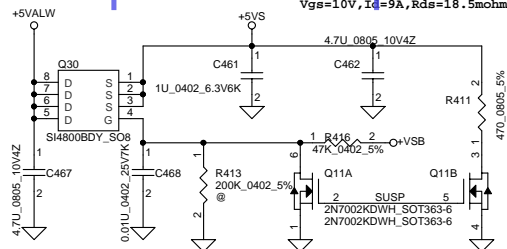


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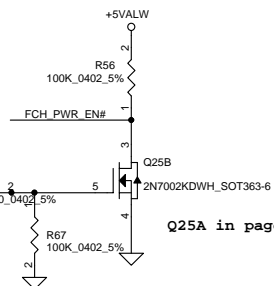
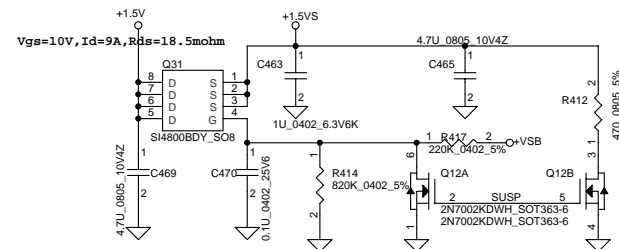
+3VALW TO +3VS



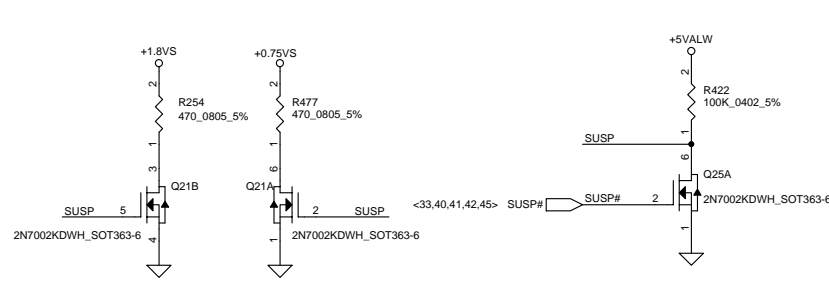
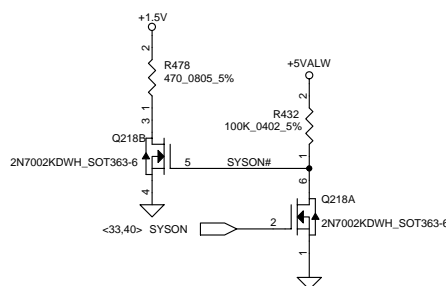
+5VALW TO +5VS



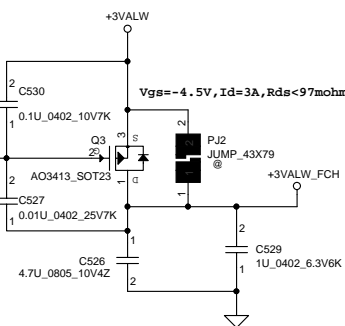
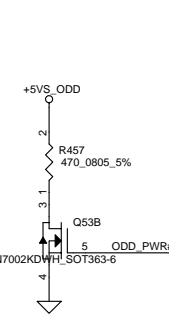
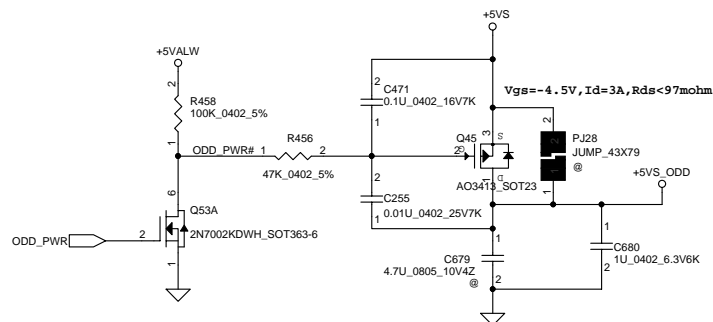
+1.5V to +1.5VS



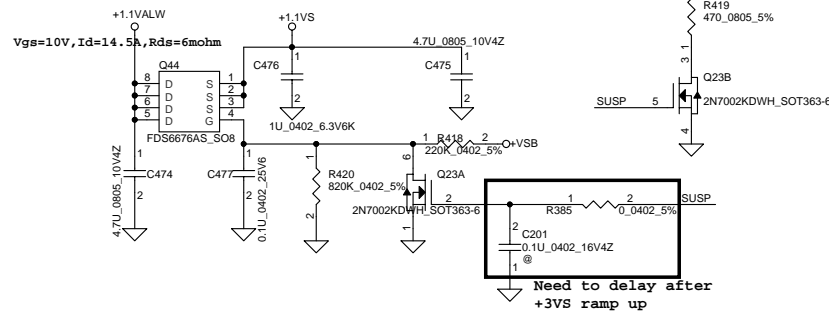
Q25A in page22



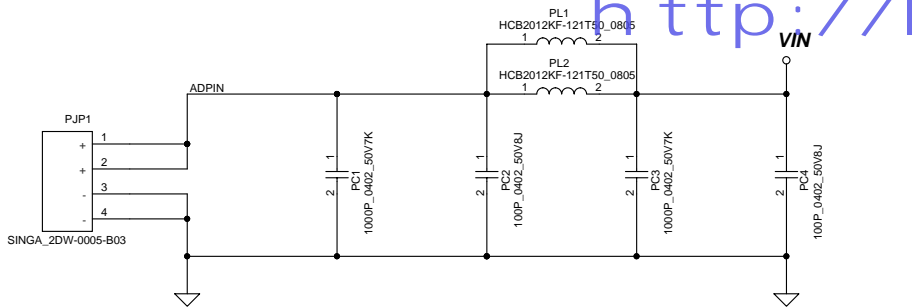
+5VS TO +5VS_ODD



+1.1VALW to +1.1VS

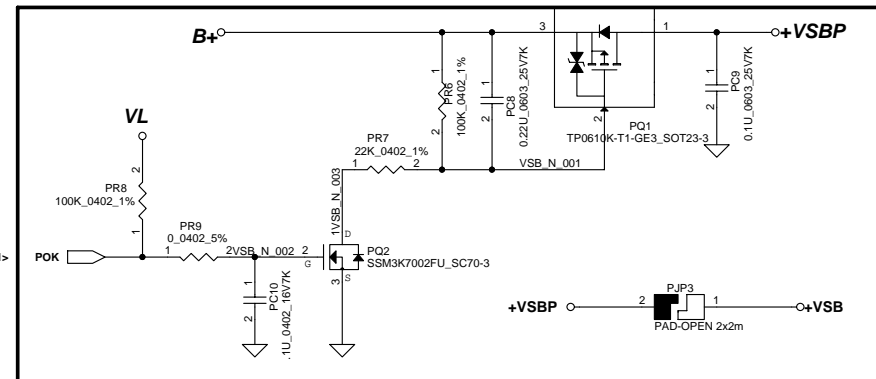
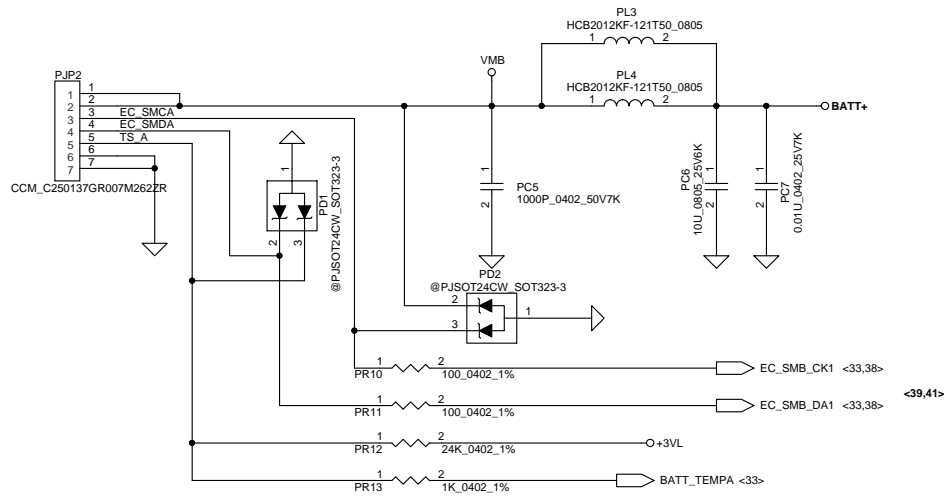
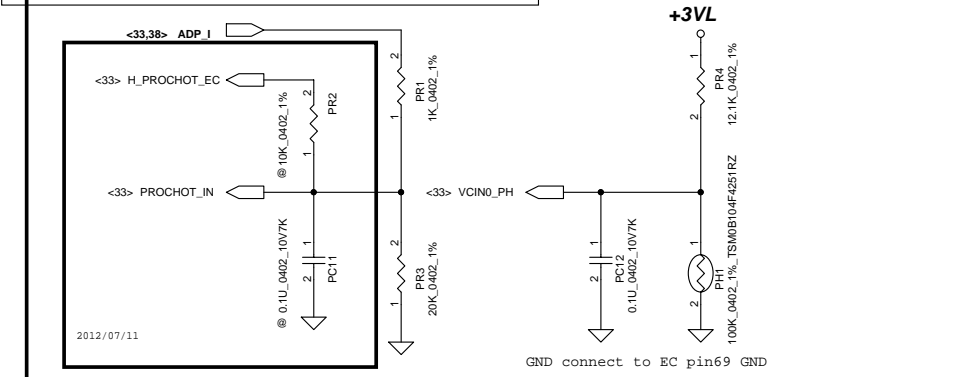


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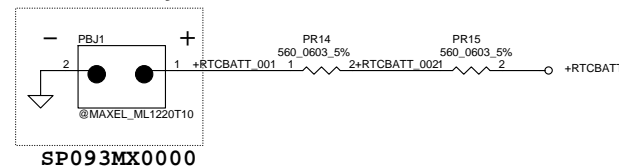


PL1 under CPU bottom side:
CPU thermal protection at 93 +3 degree C
Recovery at 56 +3 degree C

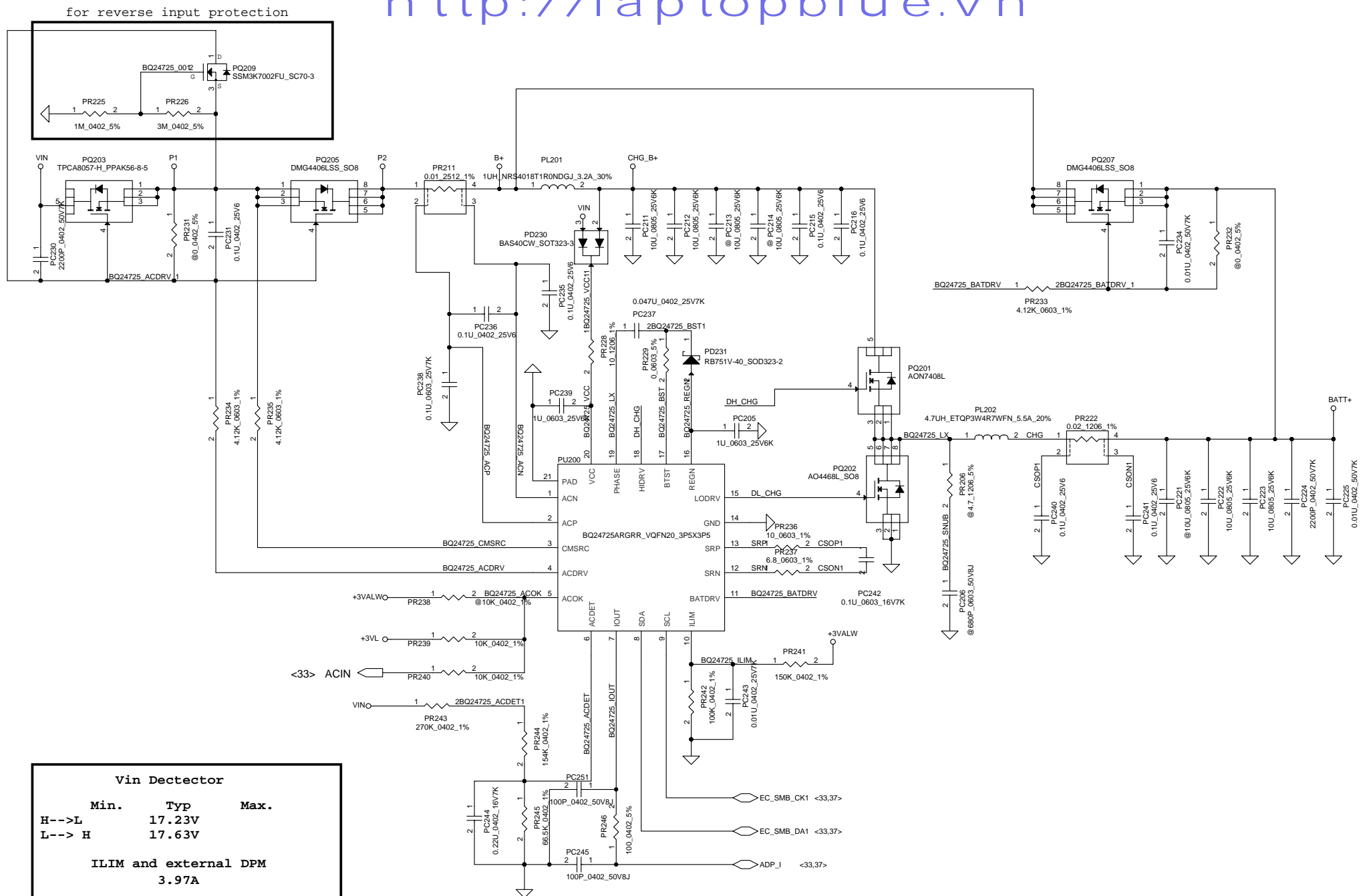
Please locate these parts
Near EC chip



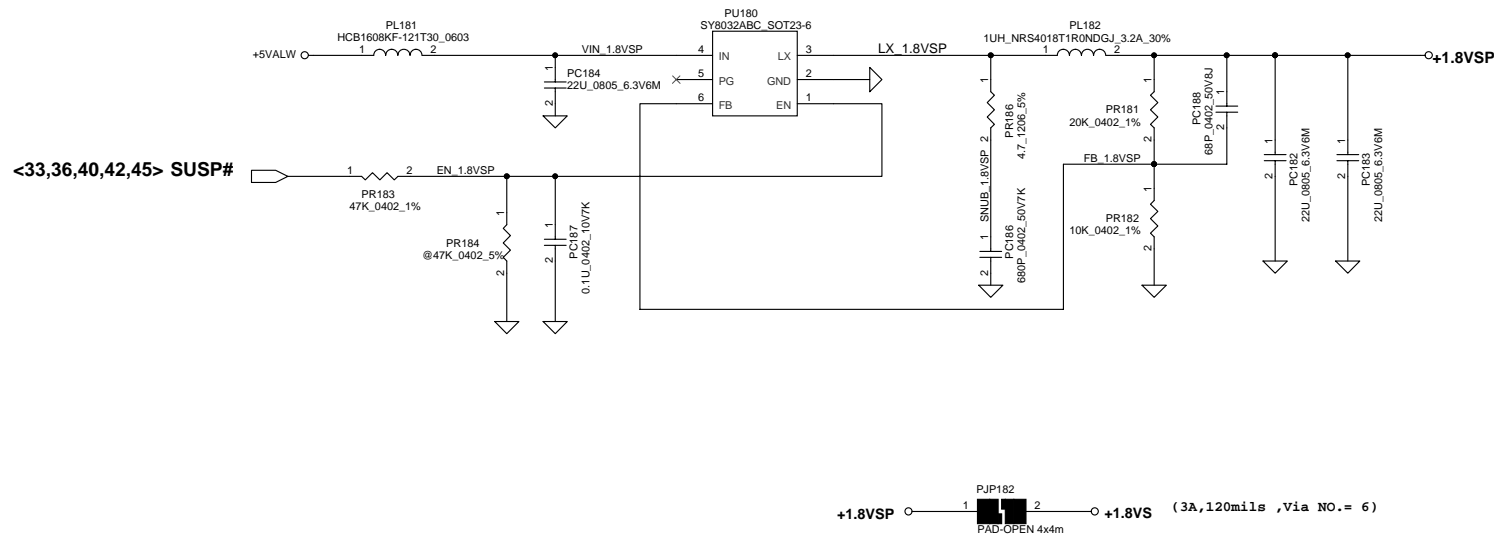
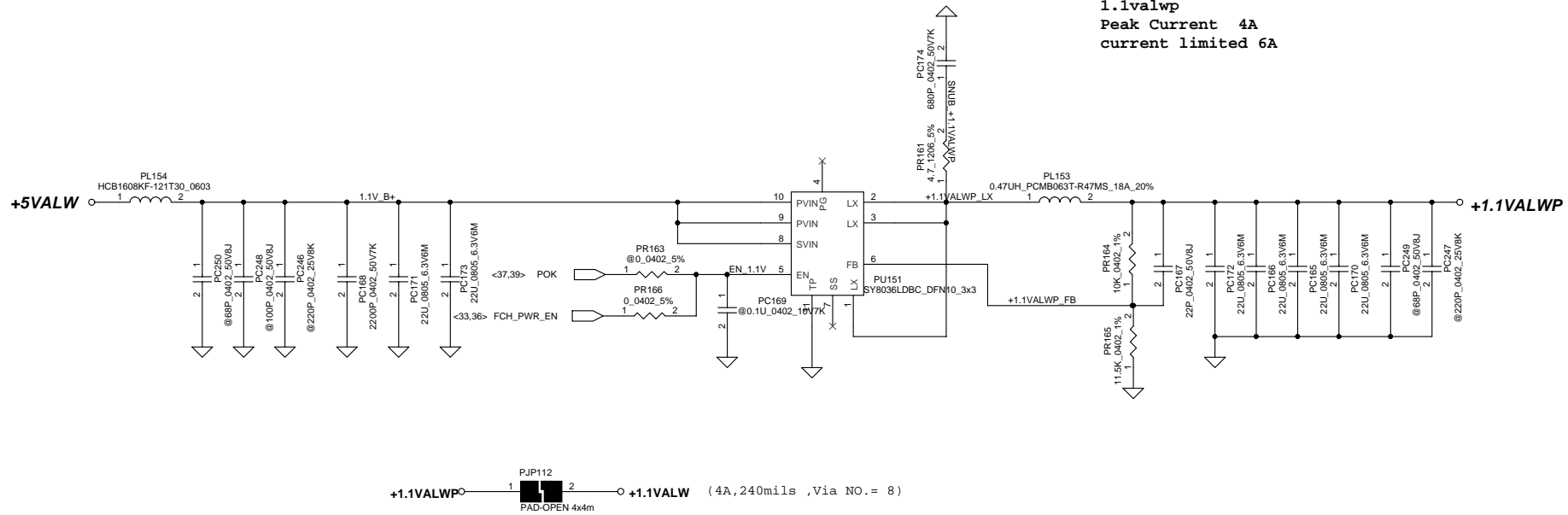
RTC Battery



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1.1valwp
Peak Current 4A
current limited 6A



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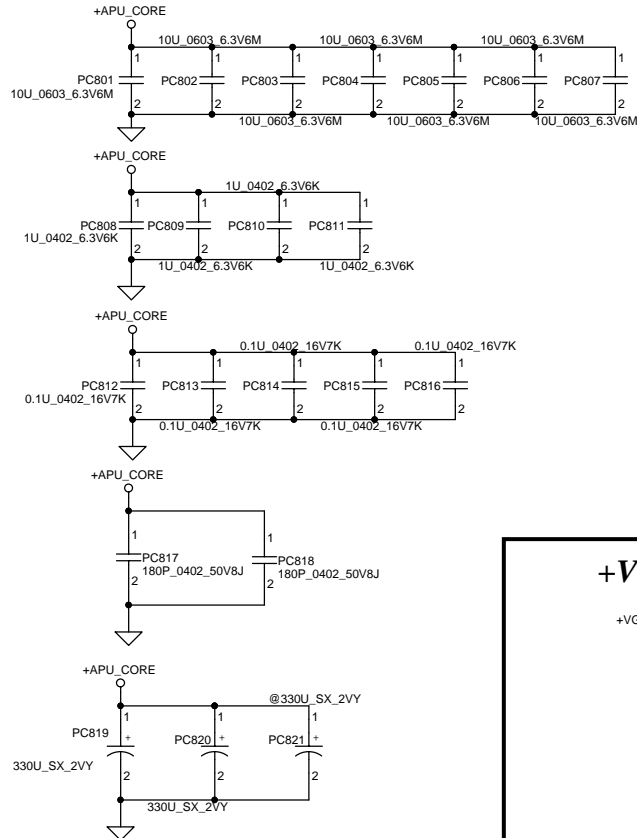
SCHEMATIC, MB A8868

LA-8712P

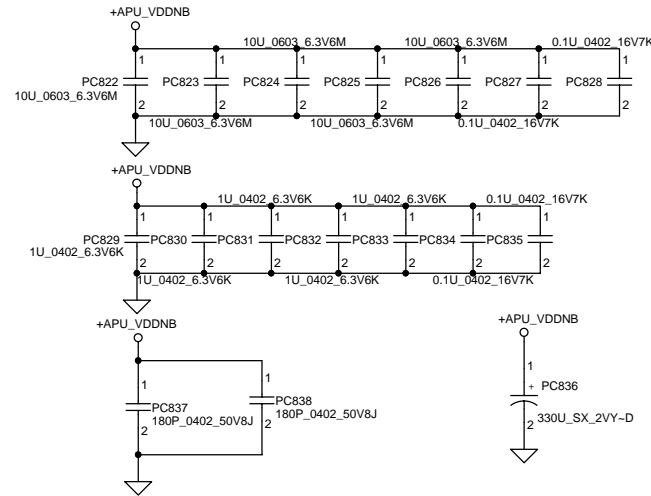
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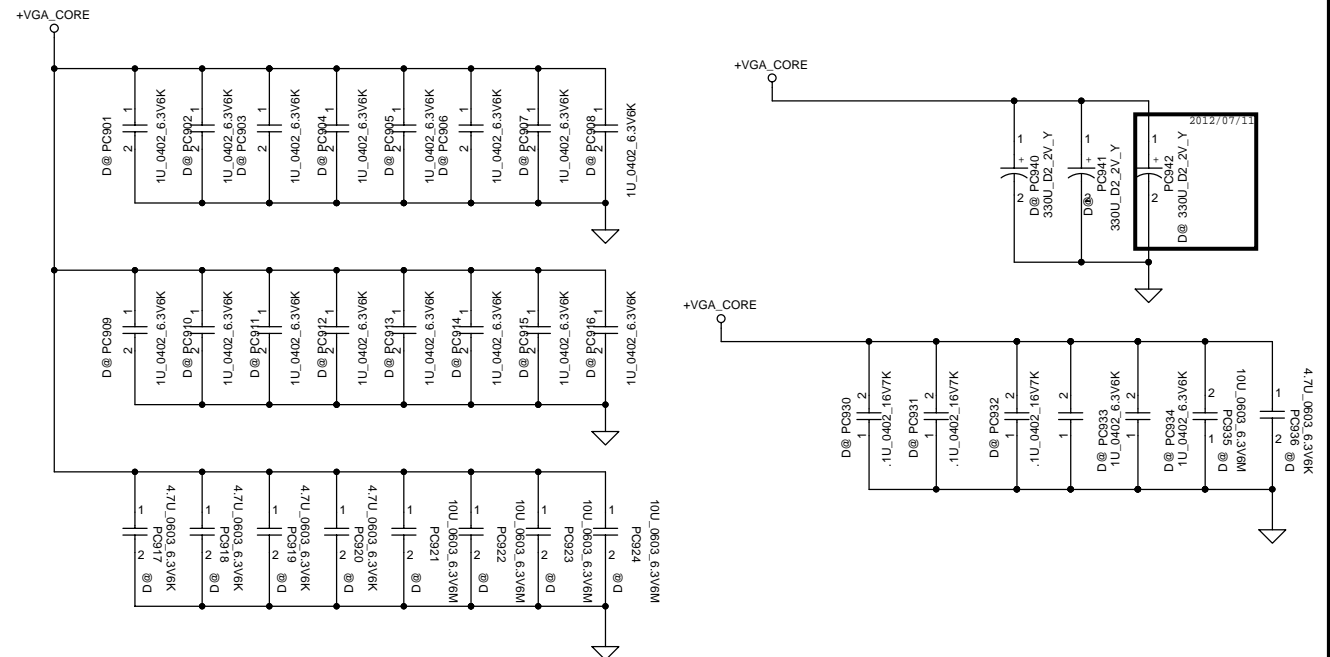
+APU_CORE



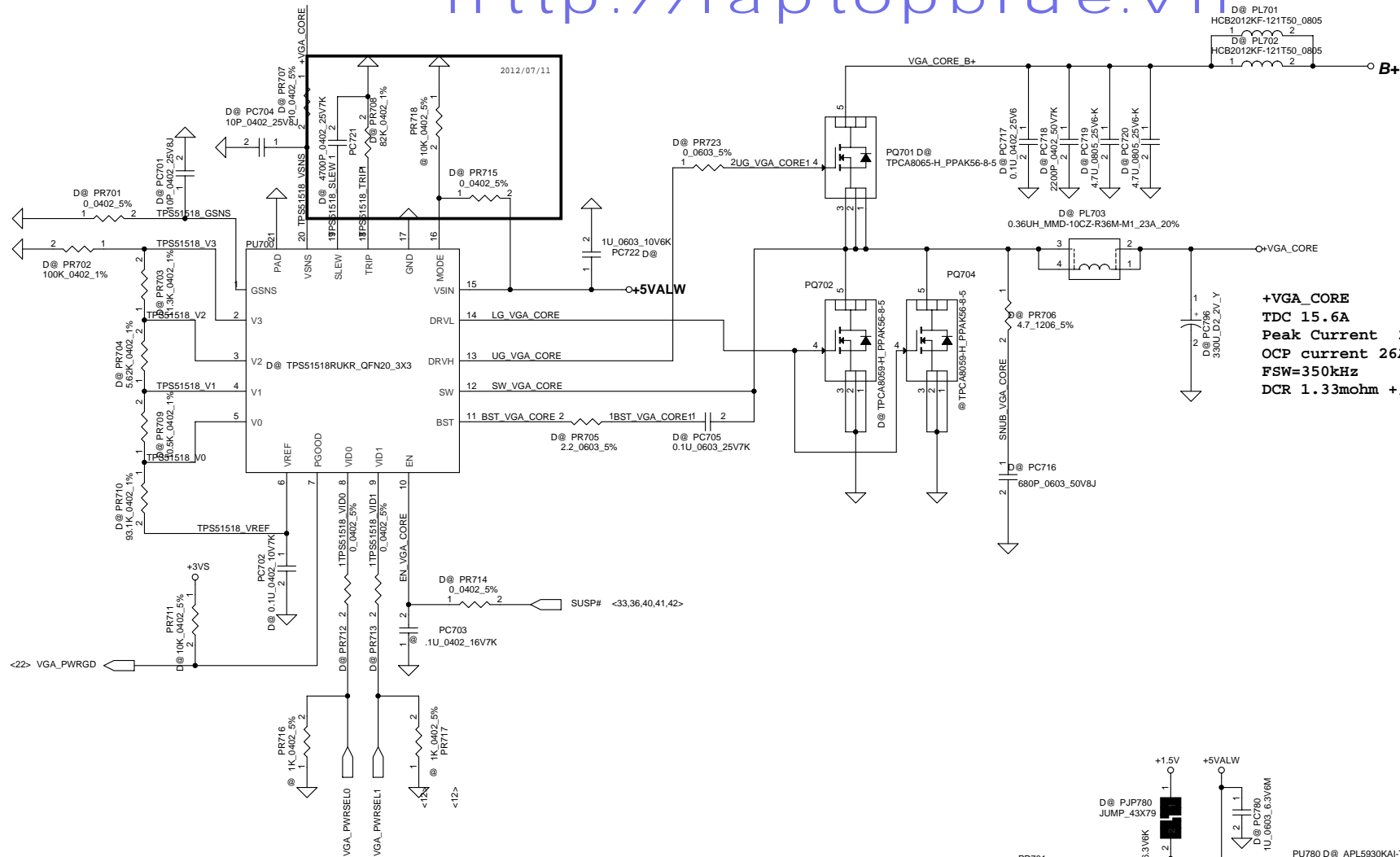
+APU_CORE_NB



+VGA_CORE



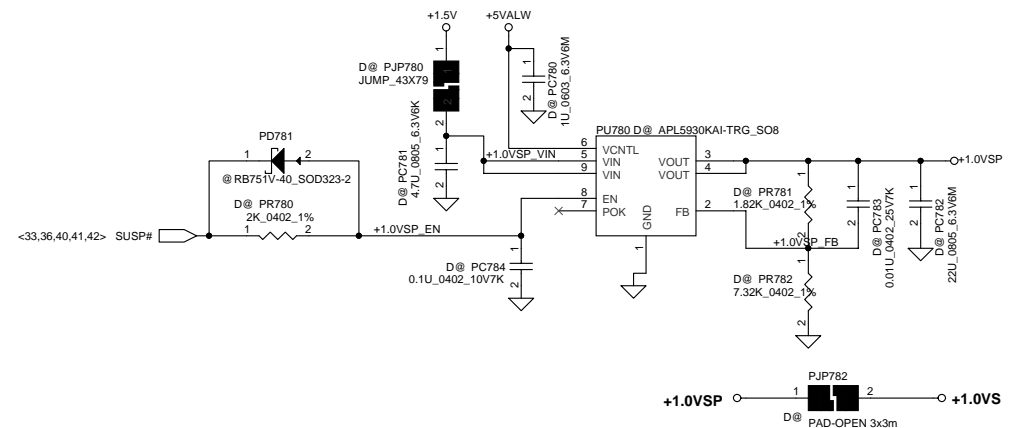
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+VGA_CORE
TDC 15.6A
Peak Current 21.6A
OCF current 26A
FSW=350kHz
DCR 1.33mohm +/-5%

Seymour XT

VGA_PWRSEL1	VGA_PWRSEL0	Core Voltage Level
1	1	0.90V
1	0	1.00V
0	1	1.05V
0	0	1.15V



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HW PIR (Product Improve Record)

http://laptopblue.vn

VBLE4/5 LA-8866P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 TO 0.2

GERBER-OUT DATE: 2012/02/14

Item	Date	Page	Solution	Request
1.	2/1	P28	Change JUSBB.1 from +USB_VCCB to +USB_VCC	For USB power
2.	2/1	P18	Change RV141,RV138,RV138,RV137 to DIS@	For VGA int. sensor
3.	2/1	P12	Remove RV29, change RV28 to 0 ohm	For VGA 2MHz
4.	2/1	P22	Change R339 to UMA@ , Change R340 to DIS@	For board ID
5.	2/1	P29	Change +1.8VGS to +1.8V	For Green CLK
6.	2/2	P30	Change CL36 from SE120102K80 to SE120102K90	For shortage
7.	2/6	P32	Update JCRI0 pin definition	Change int. MIC to MB
8.	2/6	P31	Add RA36,RA37 and delete CA64	Move sense resistors to MB
9.	2/6	P35	Change JTP from SP010015H00 to SP01001BF10	For ME request
10.	2/6	P31	Add JM1C connector SP02000RO00	For customer request
11.	2/6	P29	Change JWLAN from SP07000JP00 to SP07000TB00	For ME request
12.	2/8	P30	Add PJ31	For saving power consumption
13.	2/8	P29	Add PJ33, WLAN power circuit and reset pin	For customer request
14.	2/8	P29	Change CM7,CM8,CM9 to @	For cost down
15.	2/8	P29	Add WLAN_PWR# and WLAN_RST#	For customer request
16.	2/8	P30	Add test point TLI for pin37	For vendor request
17.	2/8	P27	Delete SW4	For layout request
18.	2/8	P11	Change UV1 from SA000047G70 to SA000047G60	For PJE request
19.	2/8	P18	Change RV118, RV119 to DIS@	For HDMI issue
20.	2/8	P35	Add screw H17, H20 and H21	For ME request
21.	2/9	P21	Reserve ESD D94-D96 for HDMI	For ESD request
22.	2/9	P9	Change C218 from 390U to 330U (SF0000002080)	For cost down
23.	2/9	P20	Remove D3-D5 and add D97 and D98	For ESD request
24.	2/9	P30	Reserve ESD D99 and D100 for LAN	For ESD request
25.	2/9	P27	Add resistors R87,R89,R164,R158	Improve SATA signal quality
26.	2/10	P27	Add JODDC	For HW experiment on DVT
27.	2/10	P8	Add C95,C102,C105	For EMI request
28.	2/10	P34	Change C457,R393 to mount	For EMI request
29.	2/10	P29	Change CCL10 to mount	For EMI request
30.	2/10	P24	Change ODD_DA#_FCH connect to U2.P6	For Module Design
31.	2/10	P24	Change ODD_PLUGIN# connect to P2.W7	For Module Design
32.	2/10	P21	Change Q6 from SB00000M700 to SB570020020	For BOM reduce
33.	4/23	P19	Change R117 +3VS to +3VALW	For LVDS power down sequence
34.	4/23	P19	Change R110,R133,C265,C261	For LVDS power down sequence
35.	4/23	P19	Change R388 +3VS to +5VS,R388 +3VS_LVDS_CAM to +5VS_LVDS_CAM	
36.	4/23	P21	Add C202 and C216	For EMI request
37.	4/23	P22	Change R241 from GCLK@ to @	For USB30 wake issue
38.	4/23	P22	Change C294,C293,Y1,R242 to mount	For USB30 wake issue
39.	4/23	P22	Change R271 and add R277,R268,C305,+RTCBATT_D	
40.	4/23	P29	Change R156,R155,C907,C908,Q210 to @	
41.	4/23	P29	Add RM20 and change UM5,RM21 to @	
42.	4/23	P29	Change UCL1.2 to +3VALW, UCL1.14 to +RTCVCC_D and add RCL10 ,RCL11	For USB30 wake issue
43.	4/23	P30	Mount QL53 and RL24 and change RL28,RL26 to @	For LAN disable
44.	4/23	P31	Add CA6,CA7	For EMI request
45.	4/23	P31	Add CA64,CA67,CA68,CA77	For EMI request
46.	5/16	P27	Delete R90-R93,R166,R168-R170,C379-C382,R87,R89,R96,R97,R158 R164,R171,R172	For ODD 14" and 15" common PCBA issue
47.	5/16	P27	Add U4	For ODD 14" and 15" common PCBA issue
48.	5/16	P23	Reserve R174	For ODD 14" and 15" common PCBA issue
49.	5/16	P27	Change C364 to 220p	For ESD request

REVISION CHANGE: 0.2 TO 0.3

GERBER-OUT DATE: 2012/06/18

Item	Date	Page	Solution	Request
1.	6/11	P27	Add JODDC circuit and remove U4 circuit	SATA ODD
2.	6/11	P33	Reserve RB8,RB9	Due to TP module for win8 feature
3.	6/15	P7	Change R846,R847,R848,R849,R851,R852 to Reserve	For Debug only

REVISION CHANGE: 0.3 TO 1.0

GERBER-OUT DATE: 2012/07/18

Item	Date	Page	Solution	Request
1.	7/12	P19	Add D85	For avoid LVDS_CLK damage issue
2.	7/17	P6	Add C78	For EMI request
3.	7/18	P27	Un-stuff SW5	For debug only
4.	7/25	P30	Stuff D92	For ESD request
5.	8/27	P32	Stuff CT7 and RT4 on TPM SKU	For EMI request

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Issued Date	2012/05/18	Deciphered Date	2013/10/05	Title	SCHEMATIC, MB A8868
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