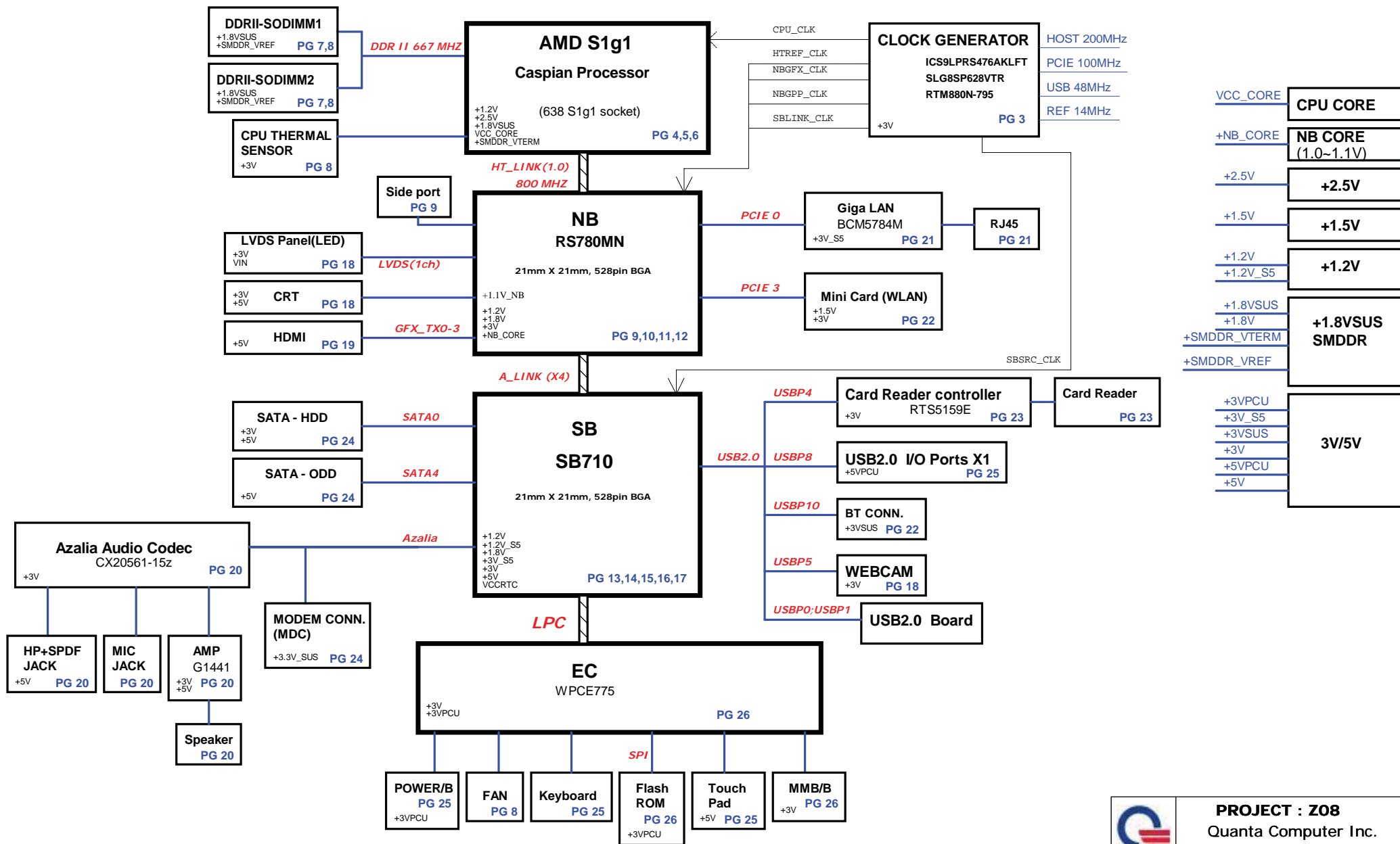


Z08 SYSTEM BLOCK DIAGRAM



01

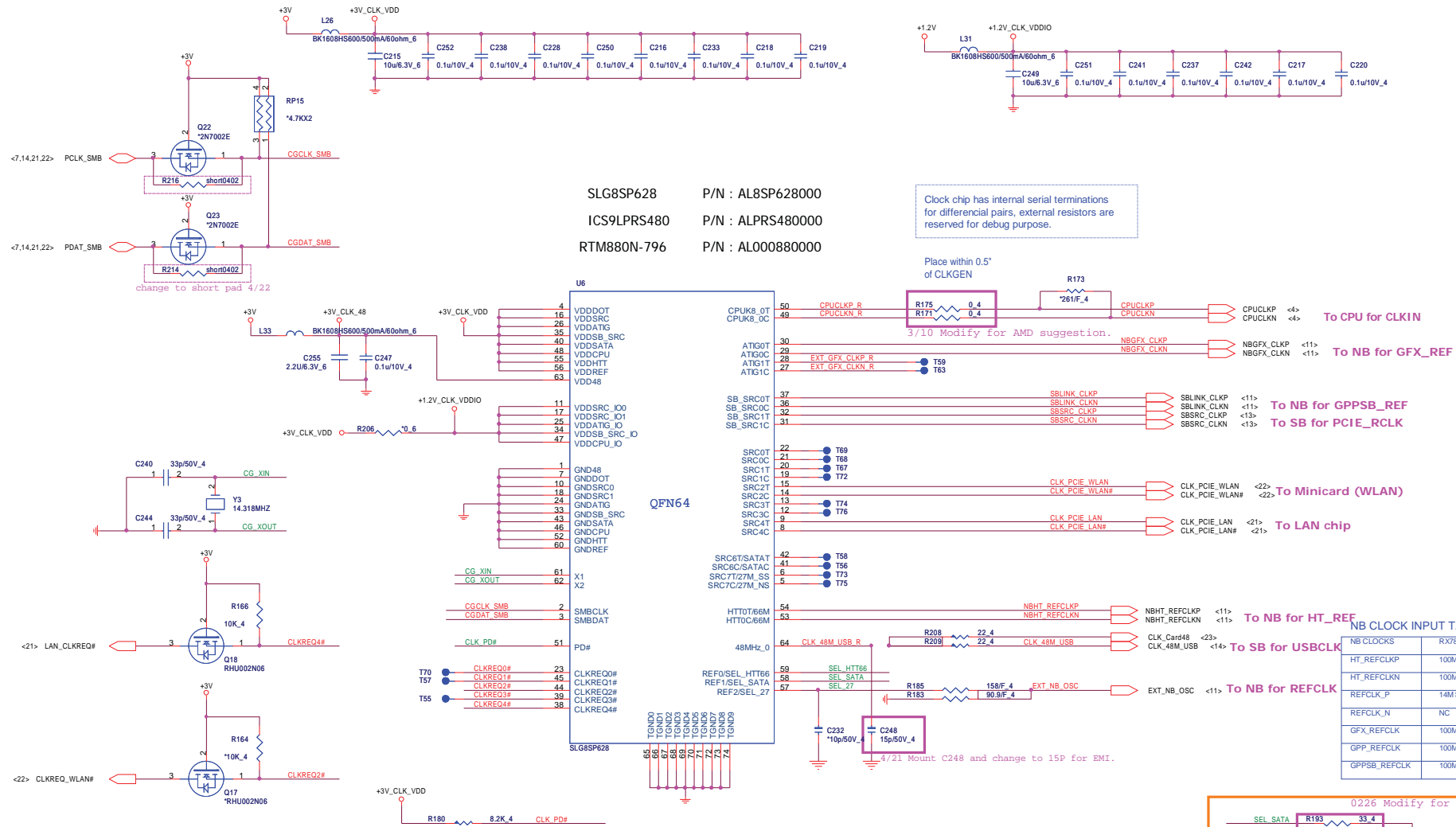


Model	REV	DATE	CHANGE LIST	NOTE
HW	C1A	2009/04/09	1.Page 11: Exchange Pin define for LVDS ON & PWM. 2.Page 21: U20 Footprint change to trf-10-1-24p-nb4. 3.Page 16: L39 Footprint from RC0603 change to RC0805. 4.Page 21: R389,R425 P/N change to CS12204JA44. 5.Page 22: CN23 Footprint change to mipcie-as0b223-s40n-7f-52p-nb4. 6.Page 23: R460 change to 33 ohm;C586 change to 10P for EMI. 7.Page 26: Add Q37,Q38,R484,R485 for MMB leakage. And 3RD_MBCLK & 3RD_MBDATA pull high from +3V to +3VPCU.	
		2009/04/16	8.Page 26: Add CP8,CP9 for EMI. 9.Page 24: Remove R284;mount C347 for EMI. 10.Page 20: Remove R312;mount C365 for EMI. 11.Page 3: Mount C248 and change to 15P for EMI. 12.Page 23: Remove R295;Mount C358 and change to 15P for EMI. 13.Page 12: Add C597,C598 30P (+NB_CORE) for EMI. Add C599,C600 30P (+1.2V_VDDHTTX) for EMI. Add C601,C602 30P (+1.2V) for EMI.	
		2009/04/22	14.R120,R112,R388,R116,R387 change to short pad_0402. 15.Page 19: Del Q20,Q21,R196,R204;add R486,R487 for AMD suggestion. 16.Page 18: CN2 footprint from msc-rb30-5-fg-30p-1 to msc-rb30-5-fg-30p-1-nb4. 17.R8,R10,R214,R216,R437,R200,R28,R4,R419,R266,R265,R275,R287,R293, R314,R319,R325,R332,R334,R258,R283,R146,R148,R198 change to short pad_0402. 18.R106,R79,R117,R118,R480,R267,R482,L1 change to short pad_0603. 19.R105,R438,R223,R249,R29,R181,L21 change to short pad_0805.	
		2009/04/23	20.Page 19:Modify HDMI detect circuit_Del R174,R447,R441,Q35,Q36,R442;add R312,R488,D31. 21.Page 18:U2 pin7 modify voltage from +5V to +3V. 22.Page 26:Swap NET CP8,CP9.	
		2009/04/27	23.Page 20:Mount U14,C435,C418;unmount L47 for Audio noise issue.	
		2009/04/28	24.Page 26:Modify Y1 Footprint.	
		2009/04/10	1.Page27 : Mount PR141(10K ohm) for Charger Issue. 2.Page32 : Change Z08A PU5 part number from AL009338014 to AL009334000. 3.Page32 : Change PC77 from 10u/4V_8 to 10u/10V_8. 4.PL5,PL8,PL10,PL11 Footprint change to choke-etqp41r36wfc-nb4.	
		2009/04/17	5.page27: 1.add PC163 2.PR110,PR139,PR149 change to short pad 3.PR141 un-mount 6.page28: 1.PR87,PR90,PR106,PR190,PR91 change to short pad. 2.JP2,JP3 remove 3.PR92 un-mount 4.PR101 mount 7.page29: 1.JP4,JP5 remove 2.PR44,PR43,PR18,PR19,PR128,PR131, PR117,PR5 change to short pad. 3.add PC164,PC165 4.add PR197,PR196 8.page30: 1.Remove JP8,JP9 9.page31: 1.Remove JP1,JP6,JP7 2.PR35,PR41,PR155,PR148 change to short pad. 3.+1.8VSUS_SRC net name change to +1.8VSUS 4.VIN_1.8 net name change to VIN. 5.+1.8V_out net name change to +1.8VSUS	
		2009/04/22	10.PL3,PL7 Footprint change to choke-spm10040t-r45m200-4p.	
		2009/04/23	11.page28: Del NET RT8206_VIN. 12.page29: Add PC166 27uF/25V to VIN.	
		2009/04/27	13.page28: Modify component from AO4496 to AO6402A..	
Power				



PROJECT : Z08
Quanta Computer Inc.

Size	Document Number	Rev
	Change List	1A
Date:	Tuesday, April 28, 2009	Sheet 2 of 38



NB CLOCK INPUT TABLE

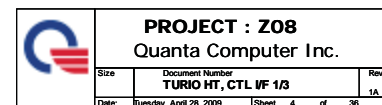
NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DFF	100M DFF
HT_REFCLKN	100M DFF	100M DFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLKP	100M DFF	100M DFF (IN/OUT)
GPP_REFCLK	100M DFF	NC or 100M DFF OUTPUT
GPPSB_REFCLK	100M DFF	100M DFF

CLOCKS name	RX780	RS780	Clock pin function
NBGFCLKP NBGFCLKN	RP1001 STUFF	RP1001 STUFF	to NB for VGA reference clock
MXM_REFCLKP MXM_REFCLKN	RP66 STUFF	RP66 NC	to M82-S external reference clock -RX780 only
NBGPCLKP NBGPCLKN	RP1005 STUFF	RP1005 NC	to NB for RX780 for PCIeX2 interface reference clock only RS780 is internal share with AC-LINK clock, RS780 not need
SBLINK_CLKP SBLINK_CLKN	RP1003 STUFF	RP1003 STUFF	to NB for AC-LINK reference clock

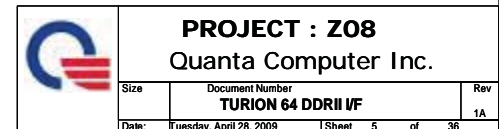
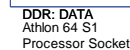
SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27	1	27MHz and 27M SS outputs
	0*	100 MHz SRC clock

* default

Size	Document Number	Rev
	CLOCK GENERATOR_SLG8SP628	1A
Date:	Tuesday, April 28, 2009	Sheet 3 of 36

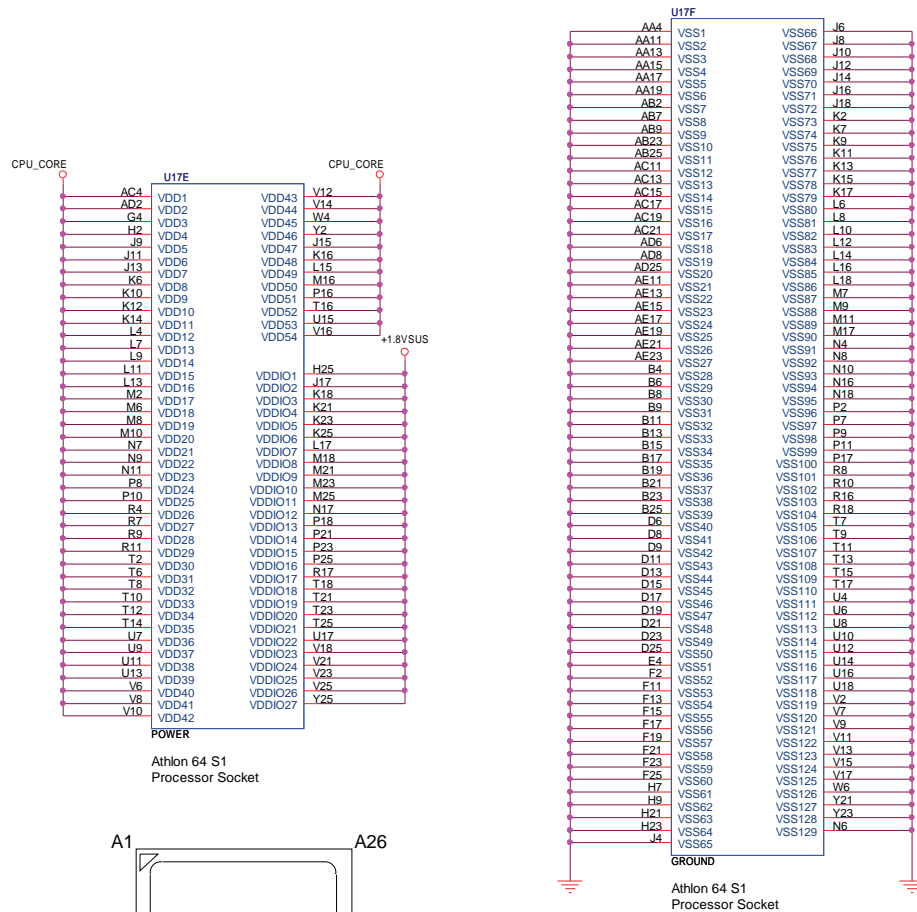


05

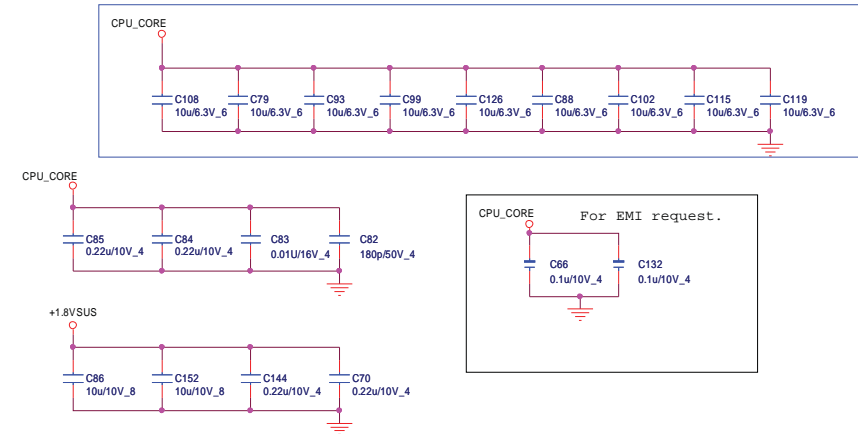


PROCESSOR POWER AND GROUND

06

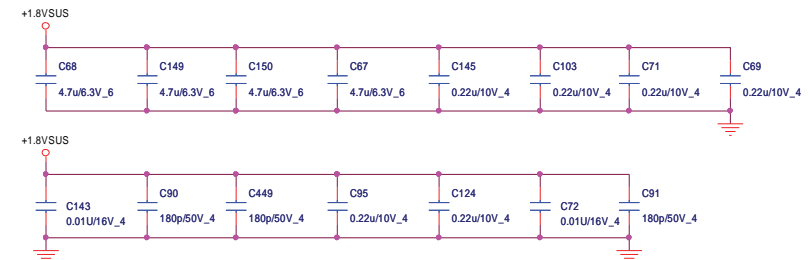


BOTTOMSIDE DECOUPLING

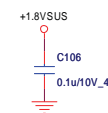


DECOUPLING BETWEEN PROCESSOR AND DIMMS

PLACE CLOSE TO PROCESSOR AS POSSIBLE

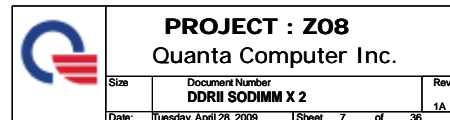


For EMI request.

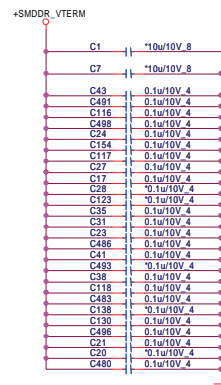


0319 Modify for EMI.

		PROJECT : Z08	
		Quanta Computer Inc.	
Size	Document Number	Rev	
	TURION 64 PWR & GND	1A	
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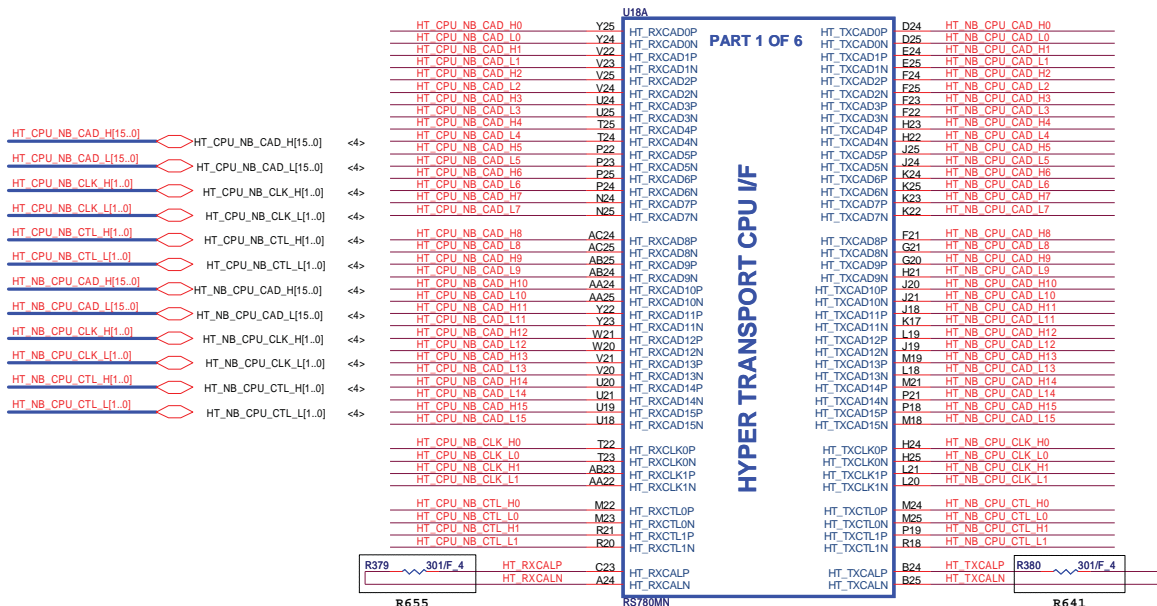
08



<SMOR-000>

MEM_MA, MEM_MB, MEM_MA_ADD, MEM_MB_ADD

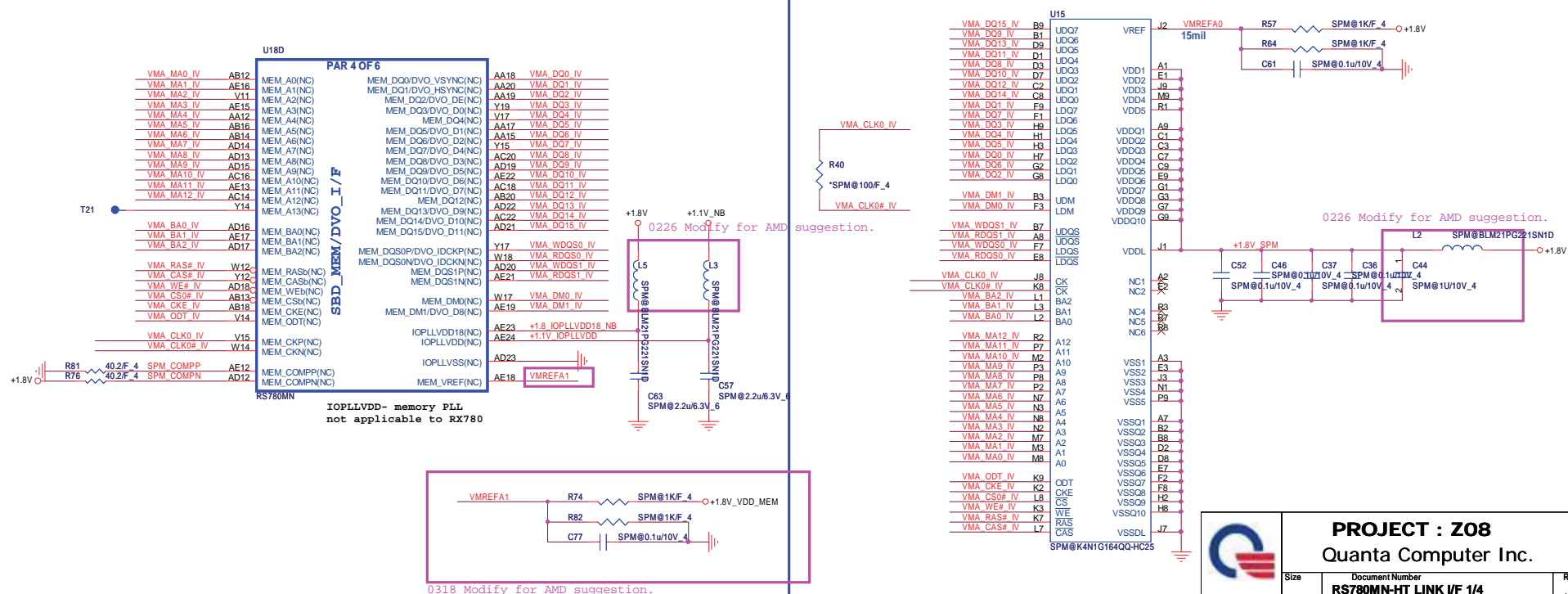
Signal	Value	Signal	Value	Signal	Value	Signal	Value
<5.7> MEM_MA_CKE0	MEM_MA_CKE0	R99	47.4				
<5.7> MEM_MA_CKE1	MEM_MA_CKE1	R94	47.4				
<5.7> MEM_MB_CKE0	MEM_MB_CKE0	R88	47.4				
<5.7> MEM_MB_CKE1	MEM_MB_CKE1	R93	47.4				
<5.7> MEM_MA_ODT0	MEM_MA_ODT0	R60	47.4				
<5.7> MEM_MA_ODT1	MEM_MA_ODT1	R48	47.4				
<5.7> MEM_MA_ODT1	MEM_MA_ODT1	R55	47.4				
<5.7> MEM_MA_ODT0	MEM_MA_ODT0	R53	47.4				
<5.7> MEM_MB_ODT0	MEM_MB_ODT0	R55	47.4				
<5.7> MEM_MB_ODT1	MEM_MB_ODT1	R53	47.4				
<5.7> MEM_MA_BANK0	MEM_MA_BANK0	R84	47.4				
<5.7> MEM_MA_BANK1	MEM_MA_BANK1	R78	47.4				
<5.7> MEM_MA_BANK2	MEM_MA_BANK2	R90	47.4				
<5.7> MEM_MA_WE#	MEM_MA_WE#	R83	47.4				
<5.7> MEM_MA_CAS#	MEM_MA_CAS#	R70	47.4				
<5.7> MEM_MA_RAS#	MEM_MA_RAS#	R75	47.4				
<5.7> MEM_MB_BANK0	MEM_MB_BANK0	R69	47.4				
<5.7> MEM_MB_BANK1	MEM_MB_BANK1	R77	47.4				
<5.7> MEM_MB_BANK2	MEM_MB_BANK2	R86	47.4				
<5.7> MEM_MB_WE#	MEM_MB_WE#	R63	47.4				
<5.7> MEM_MB_CAS#	MEM_MB_CAS#	R58	47.4				
<5.7> MEM_MB_RAS#	MEM_MB_RAS#	R71	47.4				
<5.7> MEM_MA_CS#0	MEM_MA_CS#0	R66	47.4				
<5.7> MEM_MA_CS#1	MEM_MA_CS#1	R46	47.4				
<5.7> MEM_MA_CS#2	MEM_MA_CS#2	R91	47.4				
<5.7> MEM_MA_CS#3	MEM_MA_CS#3	R52	47.4				
<5.7> MEM_MB_CS#0	MEM_MB_CS#0	R61	47.4				
<5.7> MEM_MB_CS#1	MEM_MB_CS#1	R49	47.4				
<5.7> MEM_MB_CS#2	MEM_MB_CS#2	R92	47.4				
<5.7> MEM_MB_CS#3	MEM_MB_CS#3	R51	47.4				
<5.7> MEM_MA_ADD[0..15]	MEM_MA_ADD13	R56	47.4				
	MEM_MA_ADD10	R85	47.4				
	MEM_MA_ADD0	47.4P2R.4	2				
	MEM_MA_ADD2	47.4P2R.4	3				
	MEM_MA_ADD4	47.4P2R.4	3				
	MEM_MA_ADD6	47.4P2R.4	3				
	MEM_MA_ADD15	47.4P2R.4	3				
	MEM_MA_ADD14	47.4P2R.4	3				
	MEM_MA_ADD9	47.4P2R.4	3				
	MEM_MA_ADD12	47.4P2R.4	3				
	MEM_MA_ADD3	47.4P2R.4	3				
	MEM_MA_ADD5	47.4P2R.4	3				
	MEM_MA_ADD1	47.4P2R.4	3				
	MEM_MA_ADD8	47.4P2R.4	3				
	MEM_MA_ADD7	47.4P2R.4	3				
	MEM_MA_ADD11	47.4P2R.4	3				
<5.7> MEM_MB_ADD[0..15]	MEM_MB_ADD0	RP2	1				
	MEM_MB_ADD2	RP4	3				
	MEM_MB_ADD4	RP4	3				
	MEM_MB_ADD6	RP4	3				
	MEM_MB_ADD7	RP8	3				
	MEM_MB_ADD11	RP8	3				
	MEM_MB_ADD10	RP1	3				
	MEM_MB_ADD5	RP3	3				
	MEM_MB_ADD12	RP5	3				
	MEM_MB_ADD9	RP3	3				



9-2 ^a	HT_RXCALP, HT_RXCALN ^b	<p>RS740: HT_RXCALP connected to GND through a 49.9-Ω 1% resistor. HT_RXCALN connected to VDDHTTX through a 49.9-Ω 1% resistor.^c</p> <p>RS780: Connected together through a 301-Ω 1% resistor.^c</p> <p>RX780: Connected together through a 1.21-kΩ 1% resistor.^c</p>
9-3 ^a	HT_TXCALP, HT_TXCALN ^b	<p>RS740: Connected together through a 100-Ω 1% resistor.^c</p> <p>RS780: Connected together through a 301-Ω 1% resistor.^c</p> <p>RX780: Connected together through a 1.21-kΩ 1% resistor.^c</p>

signals	RS780	RX780	RES CHIP 1.21K 1/16W +-1%(0402) P/N : CS21212FB18 RES CHIP 300 1/16W +-1%(0402) P/N : CS13002FB00
HT_TXCALP	R641 300 ohm 1%	R641 1.21K ohm 1%	
HT_TXCALN			
HT_RXCALP	R655 300 ohm 1%	R655 1.21k ohm 1%	
HT_RXCALN			

SPM(CLG)





RS780 Display Port Support (muxed on GFX)

	RS740	RX780/RS780
NB_PCIECALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1

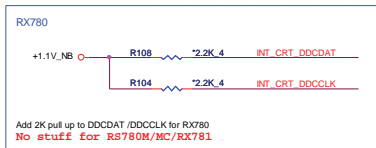


PROJECT : Z08
Quanta Computer Inc.

Size	Document Number RS780MN-PCIE V/F 2/4	Rev 1A
Date:	Tuesday, April 28, 2009	Sheet 10 of 36

`<18> INT_CRT_BLU`
`<18> INT_HSVN`
`<18> INT_VSVN`
`<18> INT_CRT_DDO`
`<18> INT_CRT_DDO`

`<4>13> CPU_LDT_RST#` `R113` `T0_4`
`<4>13> NB_PLTRST#` `R112` `short402` `NB_PLTRST# N`
 change to short pad 4/21
Red Bridge RESET

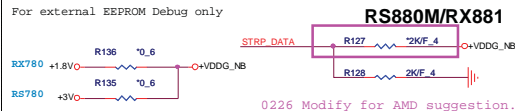


STRP_DATA Level	Northbridge Core Voltage
0	1.0 V
1	1.1 V

```
selects Loading of straps from
EPROM
1 : use default vaule , default
0 : I2C Master can load strap
values from EEPROM
if connected, or use default
values if not connected
RX780 --RS780_AUX_CAL
RS780 -- SUS_ATAT
```



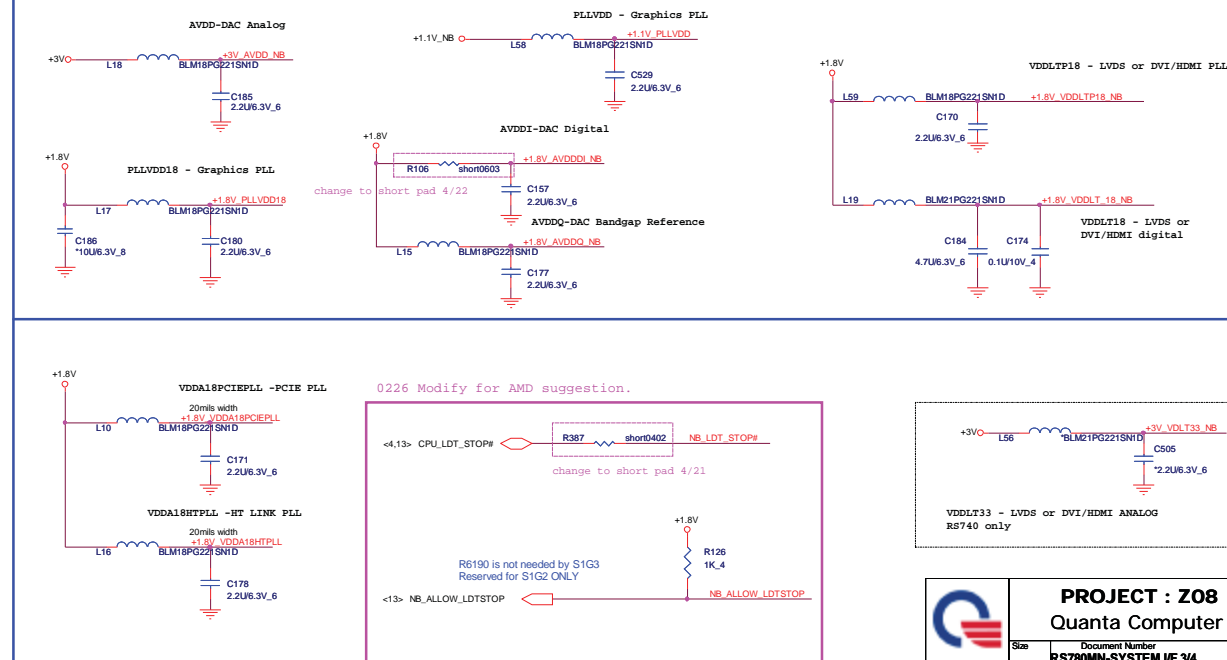
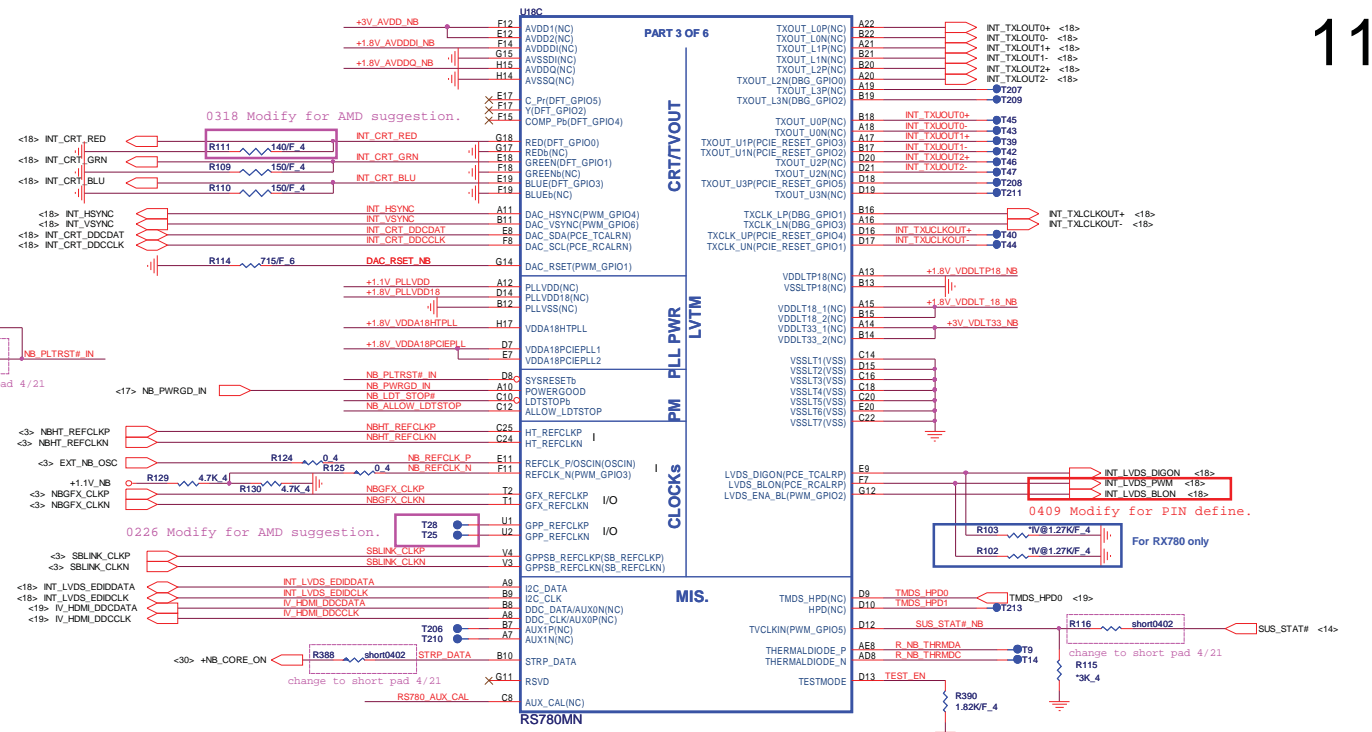
For external EEPROM Debug only



Enables Debug Bus access
through memory T/O pads and GPIO.
1 : Enable RS780 , Default
0 : Disable RS780
(RS780 use VSYNC#)



Indicates if memory Side port
is available or not
0: available RS780 , Default
1: Not available RS780
(RS780 use HSYNC#)



RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLT18	NC	+1.8V
VDDG33	NC	+3.3V	VDDLT18	NC	+1.8V
IOPLLVD18	NC	+1.8V	VDDLT33	NC	NC

GROUND

+1.1V 2A for RS780M 0226 Modify for AMD suggestion.

VDDHT - HT
LINK digital
I/O for
RX780/RS780VDDHTRX - HT
LINK RX I/O for
RX780/RS780

+1.2V 2A for RS780M+SB700

VDDHTTX - HT
LINK TX I/O for
RX780/RS780

+1.8V 1A for RS780M+SB700

VDDA18PCIE -
PCIE TX stage
I/O for
RX780/RS780VDD18 - RS780 I/O
transformVDD18_MEM For UMA RS780 only
Not applicable to RX780
memory I/O transform+1.2V
C601
30p_4
C602
30p_4

4/21 Add C601,C602 for EMI.

PART 5/6

POWER

RS780MN

VDDPCIE - PCIE-E Main power

VDDC - Core Logic power

4/21 Add C597,C598 for EMI.

0226 Modify for AMD suggestion.

VDD_MEM For UMA RS880M(SPM) only
Not applicable to RX881
memory I/O transform

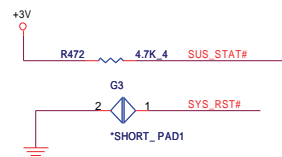
PROJECT : Z08
Quanta Computer Inc.

Size Document Number
RS780MN-POWER4/4

Date: Tuesday, April 28, 2009 Sheet 12 of 36

Rev
1A





<20> BIT_CLK_AUDIO R470 33 4 ACZ_BITCLK

<24> BIT_CLK_MDC R471 33 4

<20> ACZ_SDOUT_AUDIO R469 33 4 ACZ_SDOUT

<24> ACZ_SDOUT_MDC R468 33 4

<20> ACZ_SYNC_AUDIO R243 33 4 ACZ_SYNC

<24> ACZ_SYNC_MDC R247 33 4

<20> ACZ_RST#_AUDIO R237 33 4 ACZ_RST#

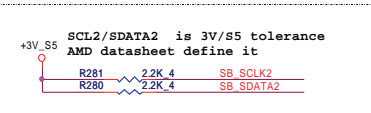
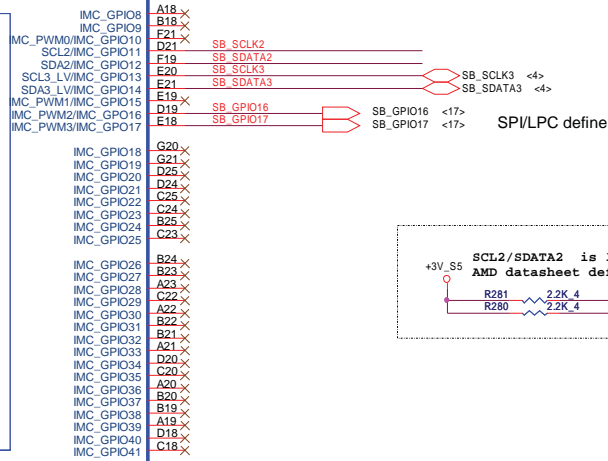
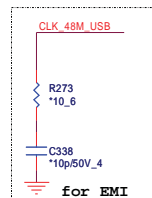
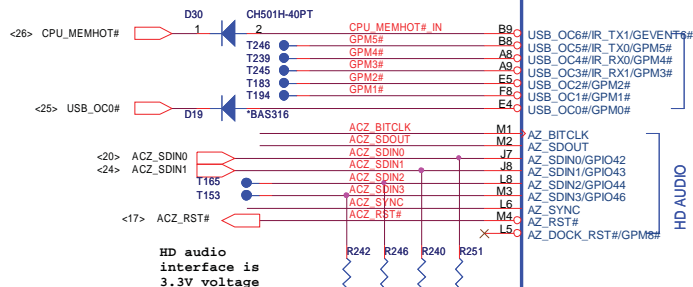
<24> ACZ_RST#_MDC R234 33 4

R2 10

+3V

R226 10K_4

SATA2_HOTPLUG



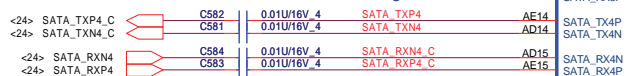
PLACE SATA AC COUPLING
CAPS CLOSE TO SB710

HDD



PLACE SATA AC COUPLING
CAPS CLOSE TO SB710

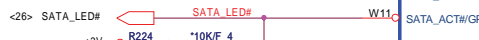
ODD



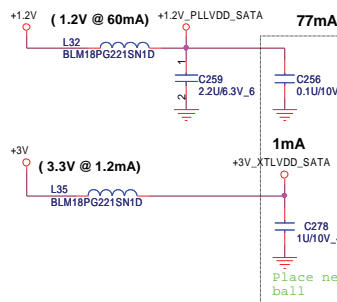
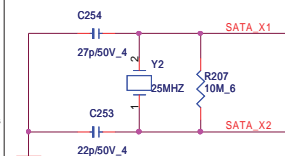
PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF SB700

NOTE:

R6171 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK



PLVDD_SATA--
SATA PLL
POWER
XTLVDD_SATA-- SATA
crystal power



U22B

SB700 Part 2 of 5

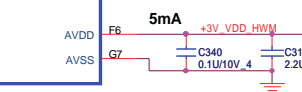
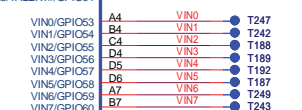
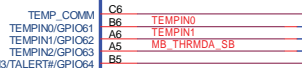
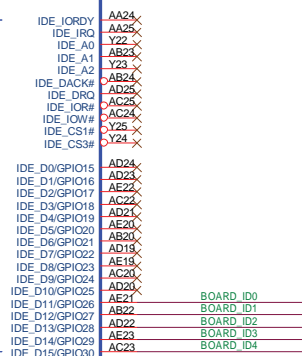
SERIAL ATA

ATA 66/100/133

SPI ROM

HW MONITOR

SB710



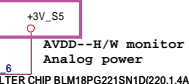
MB ID Selection Table

Board ID	ID4	ID3	ID2	ID1	ID0
For ZK8/Z08 ZK8=0, Z08=1				H	L
TBD				H	L
UMA/MXM UMA=0, MXM=1			H	L	
For side port W/O=0, W/=1		H	L		
TBD	H	L			

MB ID



0226 Modify for AMD suggestion.



PROJECT : Z08
Quanta Computer Inc.

Size	Document Number	Rev
	SB710-SATA/IDE/HWM/SPI 3/4	1A
Date:	Tuesday, April 28, 2009	Sheet 15 of 36



Size	Document Number SB710-PWR/DECOUPLING 4/4	Rev 1A
Date:	Tuesday, April 28, 2009	Sheet 16 of 36

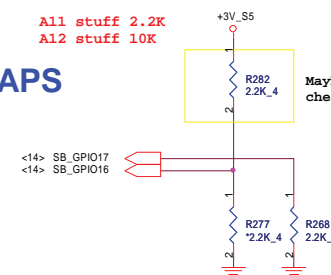


OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

It must ready
before RSMRST#

REQUIRED STRAPS

All stuff 2.2K
All stuff 10K



Maybe can be remove -- internal pull up
check AMD

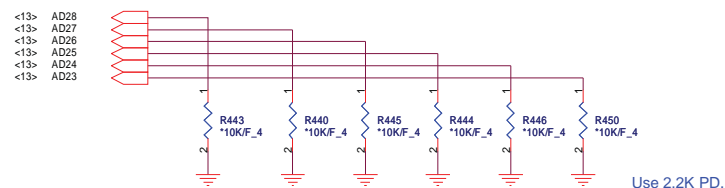
TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

NB_PWRGD IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Ck Gen
(Need SB PLL initialize firstly)

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED
PULL LOW	BOOTFAIL DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT

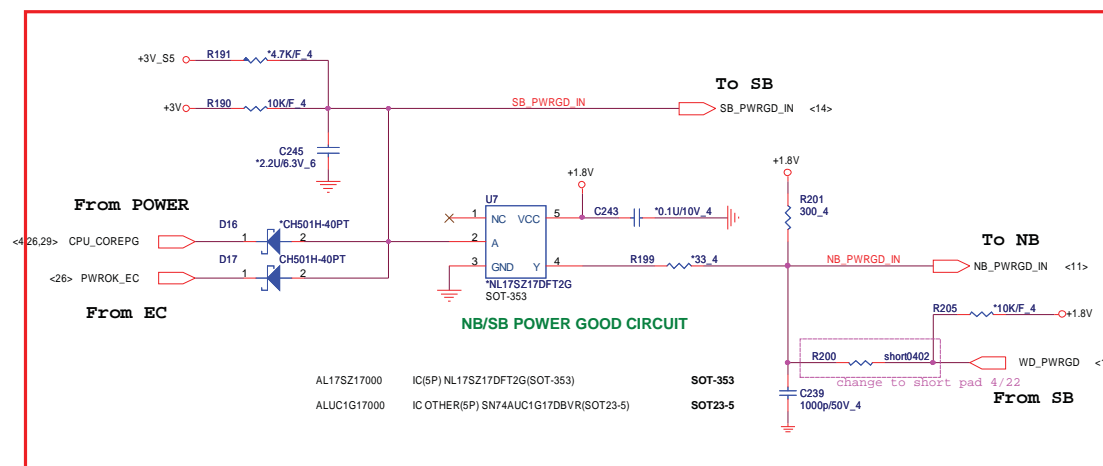
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



Use 2.2K PD.

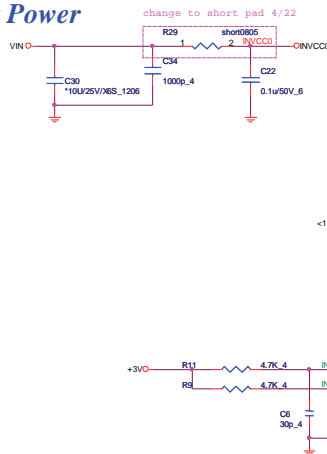
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



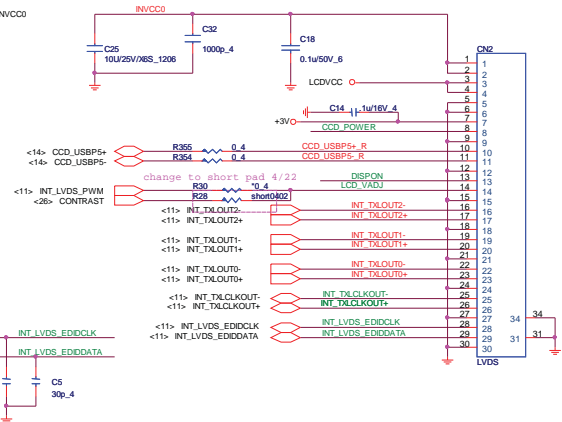
PROJECT : Z08
Quanta Computer Inc.

Size	Document Number	Rev
	SB710-STRAPS	1A
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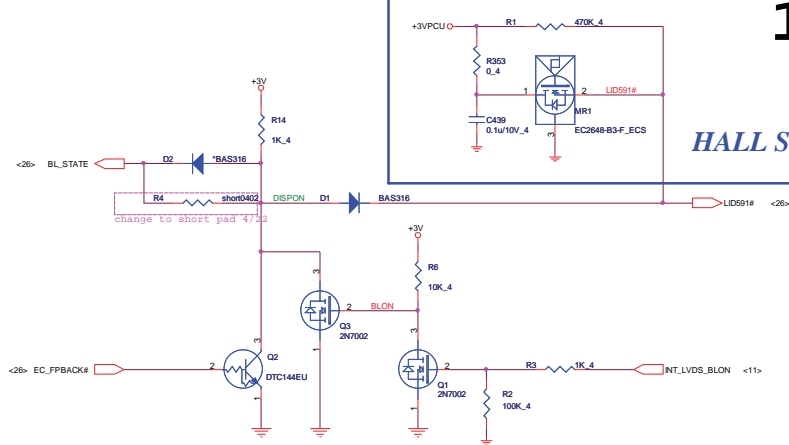
Backlight Power (LDS)



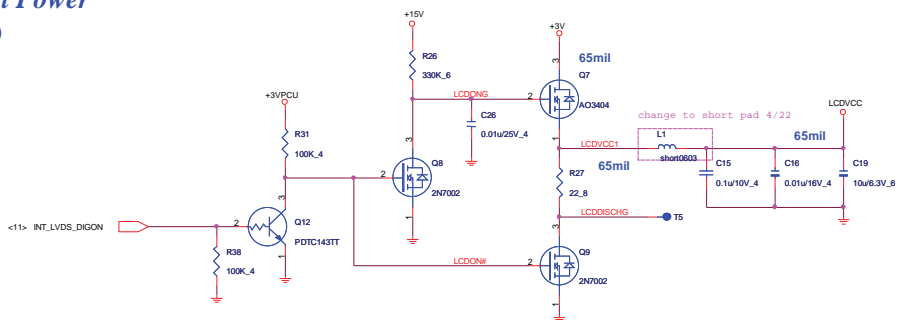
LVDS Coaxial Connector



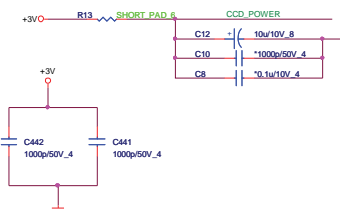
HALL Sensor (HSR)



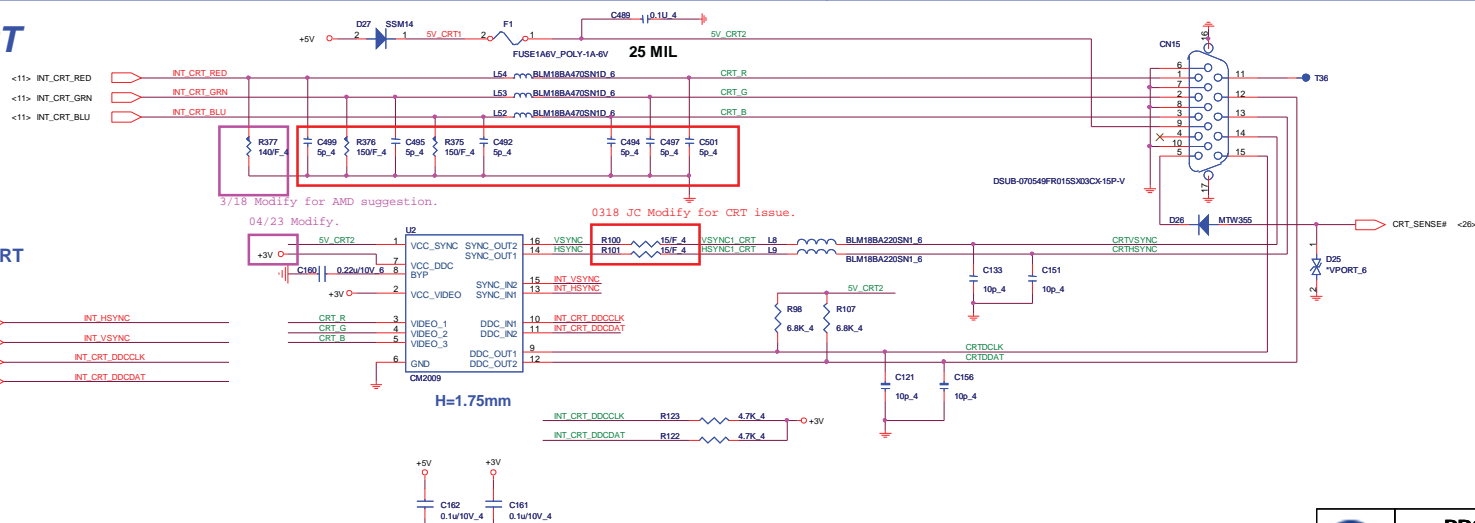
Panel Power
(LDS)



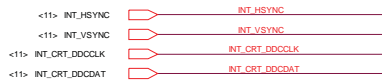
CAMERA Module (CCD)



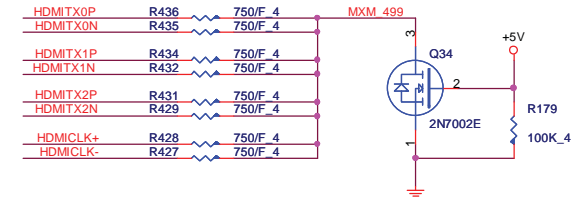
CRT PORT
(CRT)



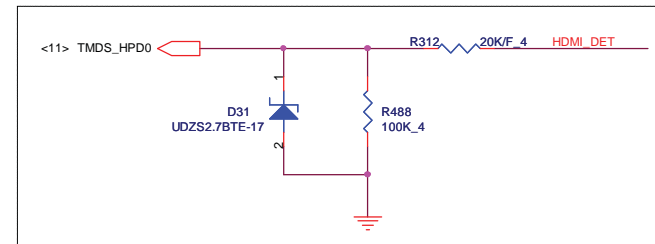
UMA to CRT



(HDM)

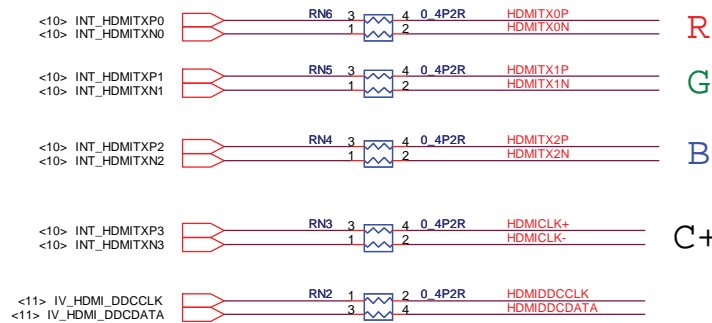


HDMI HPD SENSE



4/23 Modify HDMI detect circuit.

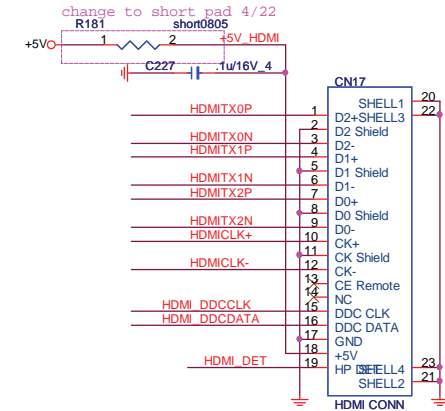
(HDM)




Close to HDMI Connector

DDC4 is 5V tolerance, the MOSFET level shifter no need.

HDMI connector



	PROJECT : Z08		
	Quanta Computer Inc.		
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			1A
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(CX20561-15Z for QFN)

(ADO)

For EMI Request

4/25 Remove R312/mount C365 for EMI.
BIT_CLK_AUDIO
C365
10P/50VCG_4

PC BEEP GAIN CONTROL

GAIN	GPIO1	GPIO2
0dB	10K	10K
-6dB	omit	omit
-12dB	10K	omit
-18dB	omit	10K

CX20561-12Z Not support digital MIC
CX20561-13Z support digital MIC

Port A -- System headphone Jack (JD : HP_PLG)
Port C -- System Stereo Microphone Jack (JD : MIC1_PLG)
Port D -- System Speaker (JD : N/A)

Int. Stereo Speakers

20

AUD_SPK_R1 L14 BK1608HM241-T
AUD_SPK_R2 L13 BK1608HM241-T
AUD_SPK_L1 L12 BK1608HM241-T
AUD_SPK_L2 L11 BK1608HM241-T
AUD_SPK_R1_S
AUD_SPK_R2_S
AUD_SPK_L1_S
AUD_SPK_L2_S
3800-ED4N-00R
C419
1U10V/50V_6
1U10V/50V_6
ADO_GND

EXT. Mic in

Normal Open Type

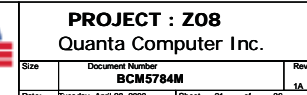
(AMP)

AUDIO AMPLIFIER G1441

Speaker Amplifier

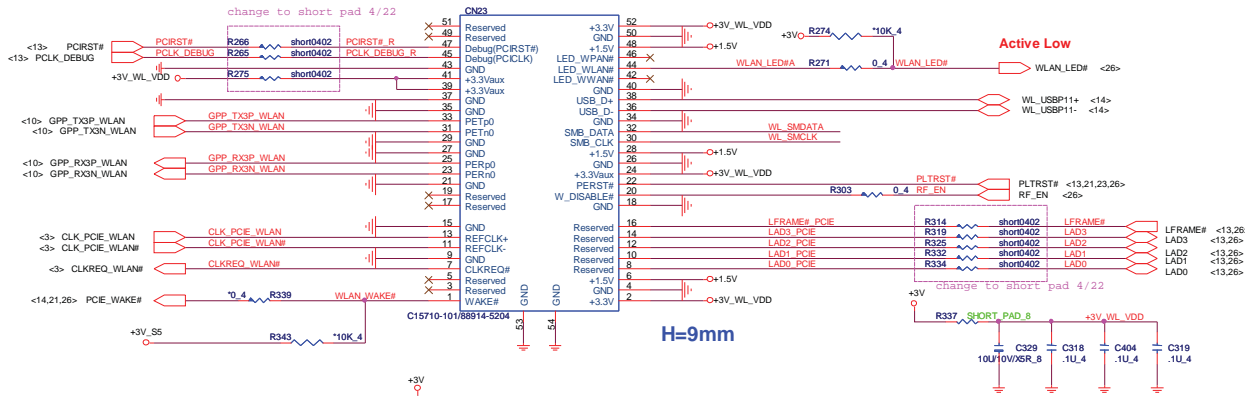
Headphone out + Spdif Out (normal open)

(Normal open)

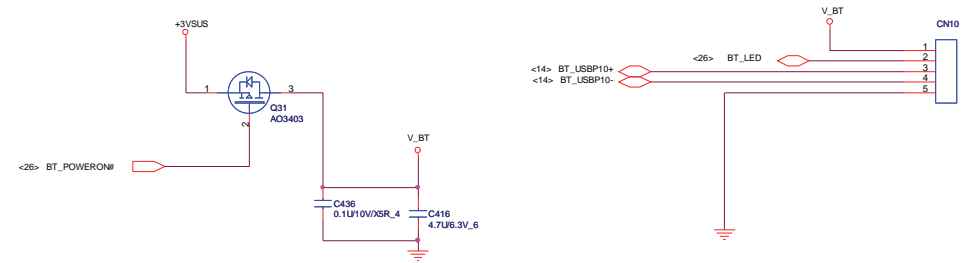



MINI-Card I (WLAN)

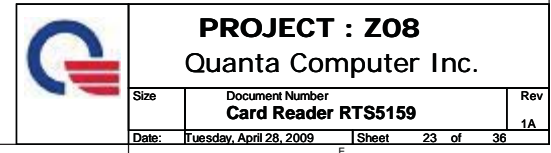
22



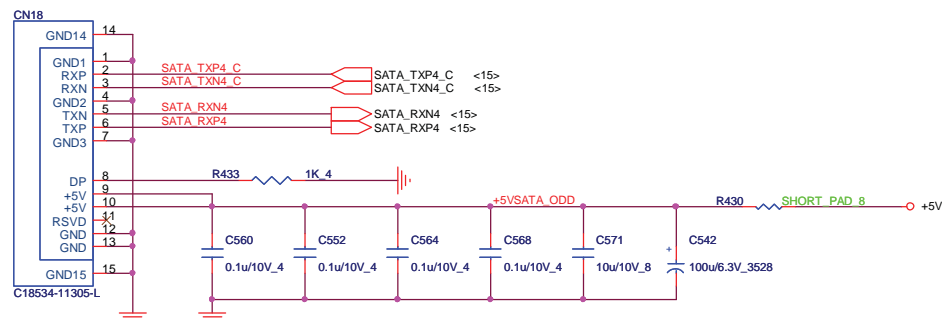
BLUETOOTH CONNECTOR



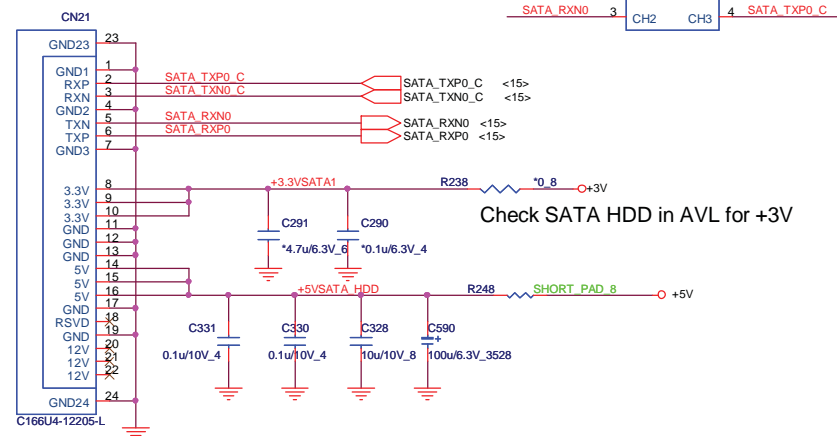
 PROJECT : Z08 Quanta Computer Inc.		
Size	Document Number	Rev
	Mini-Card/WL	1A
Date:	Tuesday, April 28, 2009	Sheet 22 of 36



SATA ODD

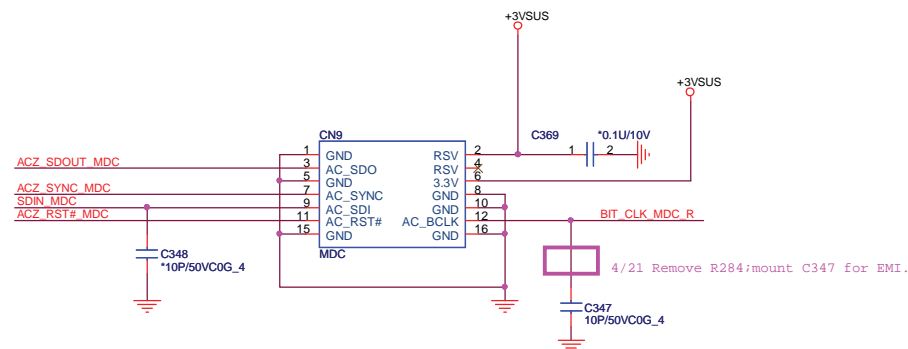
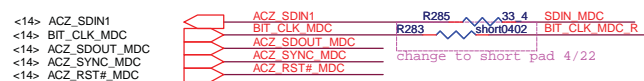


SATA HDD



Check SATA HDD in AVL for +3V

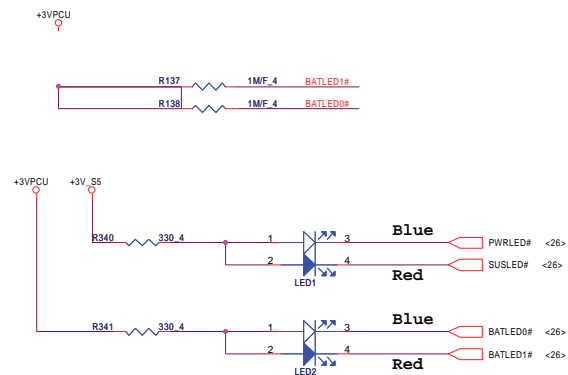
For MDC Module



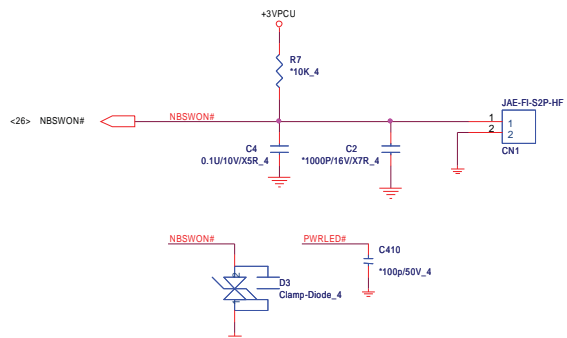
PROJECT : Z08
Quanta Computer Inc.

Size	Document Number	Re
	SATA/HDD&ODD/MDC	1A
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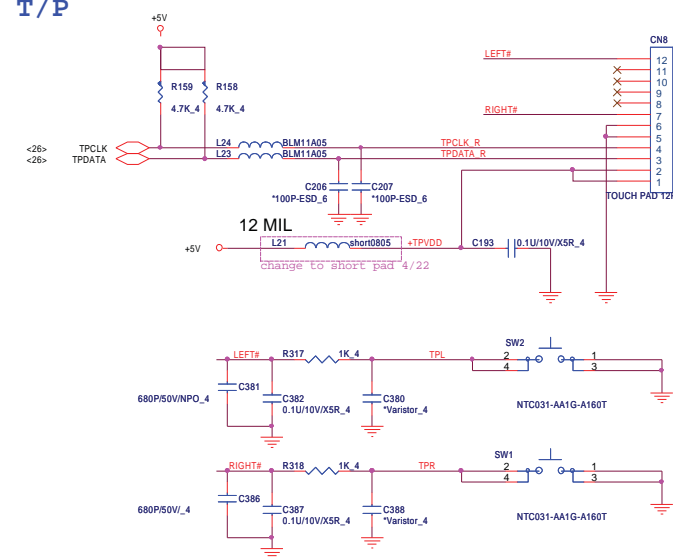
LED



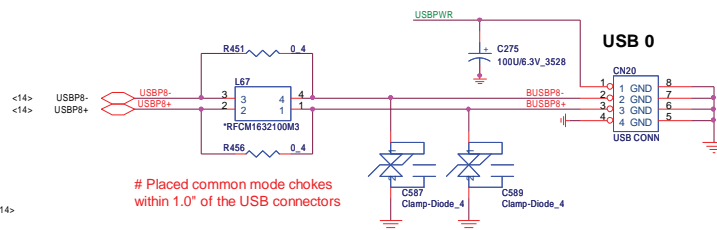
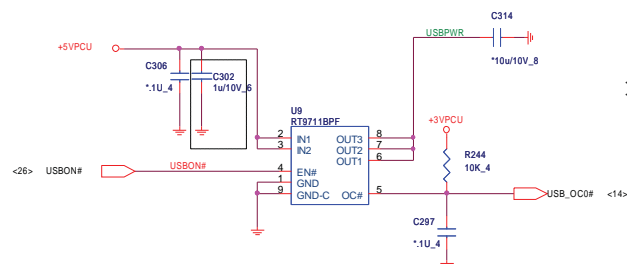
To Power Board



T/P

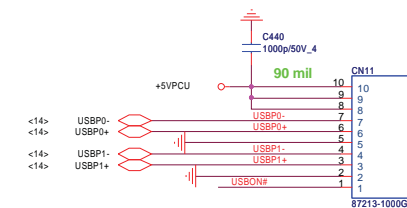


USB PORT (X1)




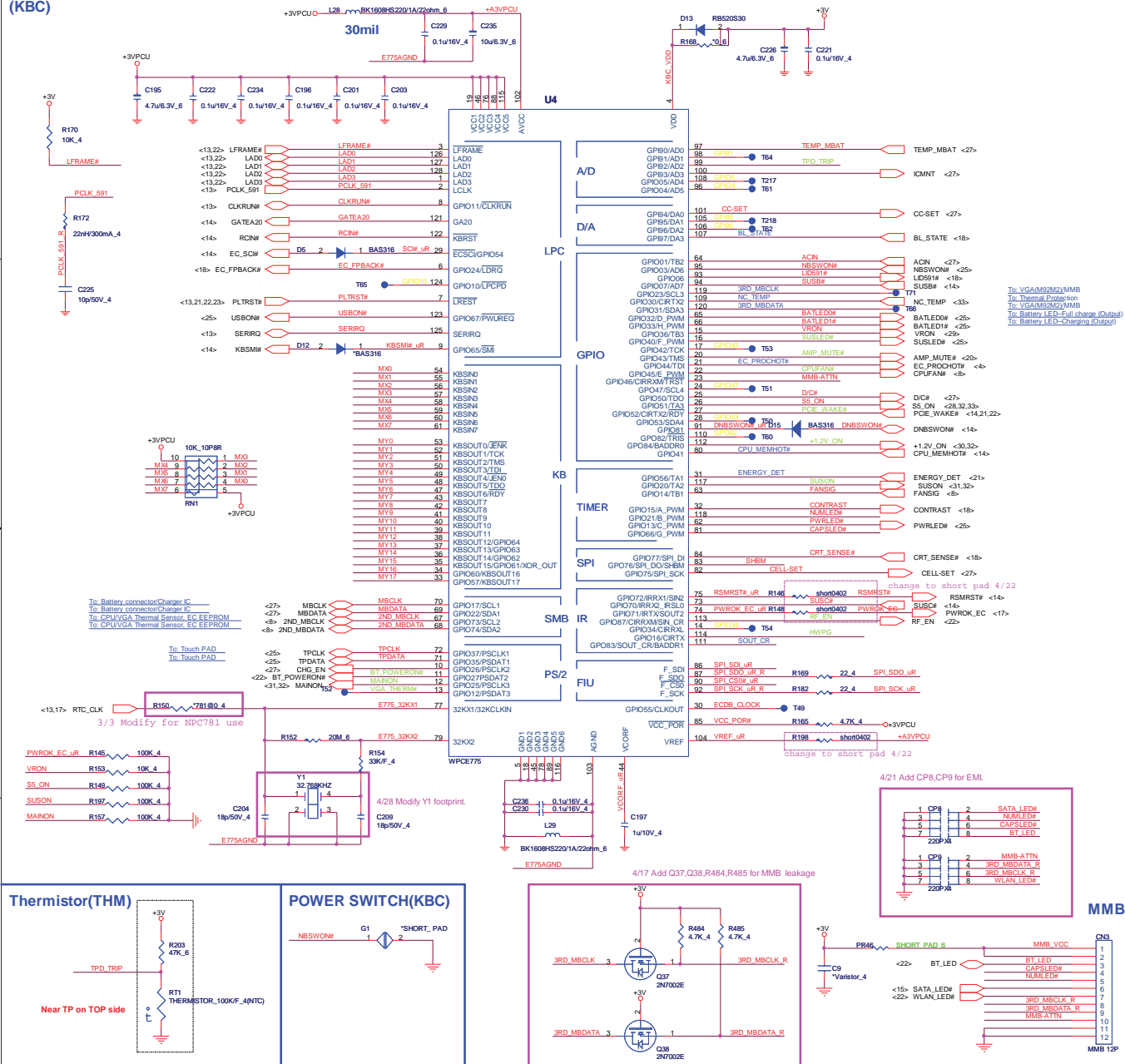
Placed common mode chokes within 1.0" of the USB connectors

To USB Board



Please reserve Cin = 1uF(stuff), Cout = 10uF(don't stuff) for Richtek RT9711BPF
Please reserve Cin = 4.7uF(stuff), Cout = 10uF(don't stuff) for GMT solution

		
Size	Document Number	Rev
FP/ TP/ USB /BT/FELICA/FM	FP/ TP/ USB /BT/FELICA/FM	1A
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I/O Address		
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

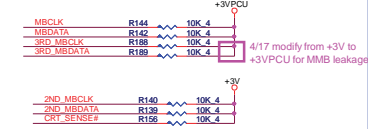
BADDR0: +1.2V_ON R187 10K_4

BADDR1: SOUT_CR R186 10K_4

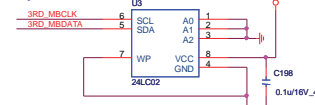
SHBM: SHBM R180 10K_4

1/13 Confirm by vendor mail:
Disabled (*) if using FW device on LPC.
Enabled (*) if using SPI flash for both system BIOS and EC firmware

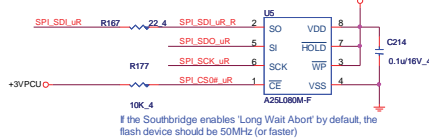
SM BUS PU(KBC)



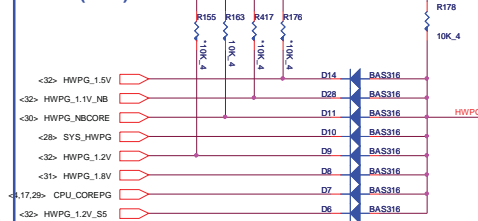
ACER ID(KBC)



SPI FLASH(KBC)



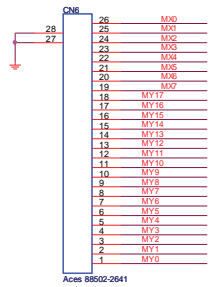
HWPG(KBC)



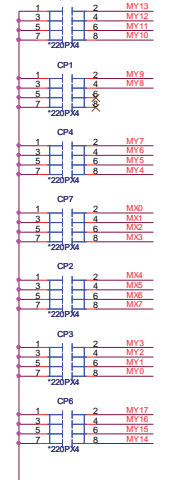
INTERNAL KEYBOARD STRIP SET (KBC)



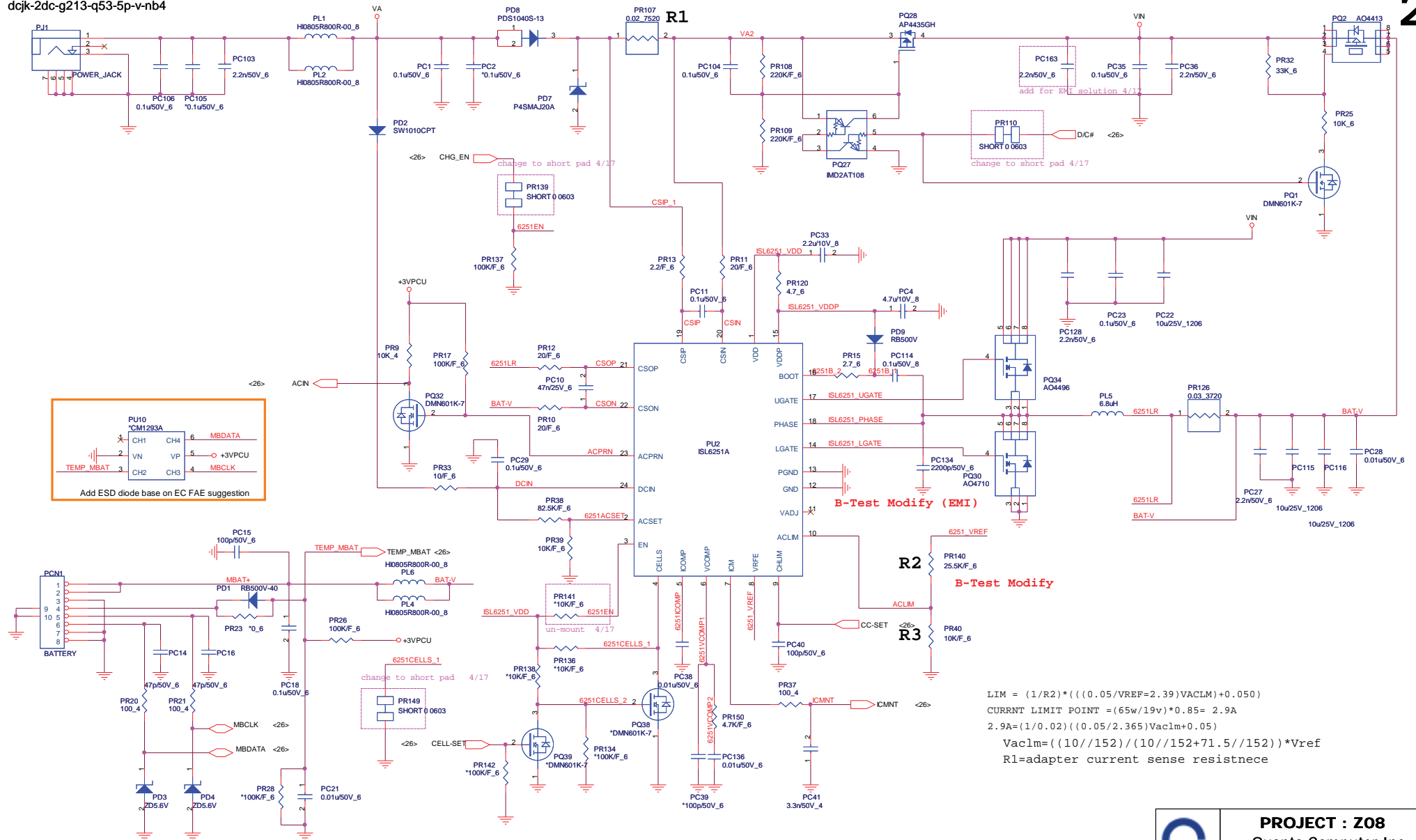
KEYBOARD



Acer RS602-2641

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Quanta Computer Inc.

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	WPCE775C_0DG & FLASH	1A
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$$LIM = (1/R2) * (((0.05/VREF=2.39)VACLIM) + 0.050)$$

$$CURRNT LIMIT POINT = (65w/19v) * 0.85 = 2.9A$$

$$2.9A = (1/0.02) * ((0.05/2.365)VACLIM + 0.05)$$

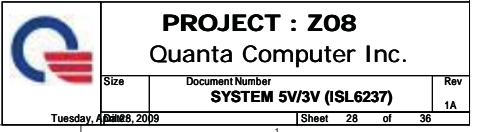
$$VACLIM = ((10//152)/(10//152+71.5//152)) * VREF$$

R1=adapter current sense resistance



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Quanta Computer Inc.

Size	Document Number	Rev
	CHARGER (ISL6251A)	
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Close to Phase 1 Inductor

Parallel

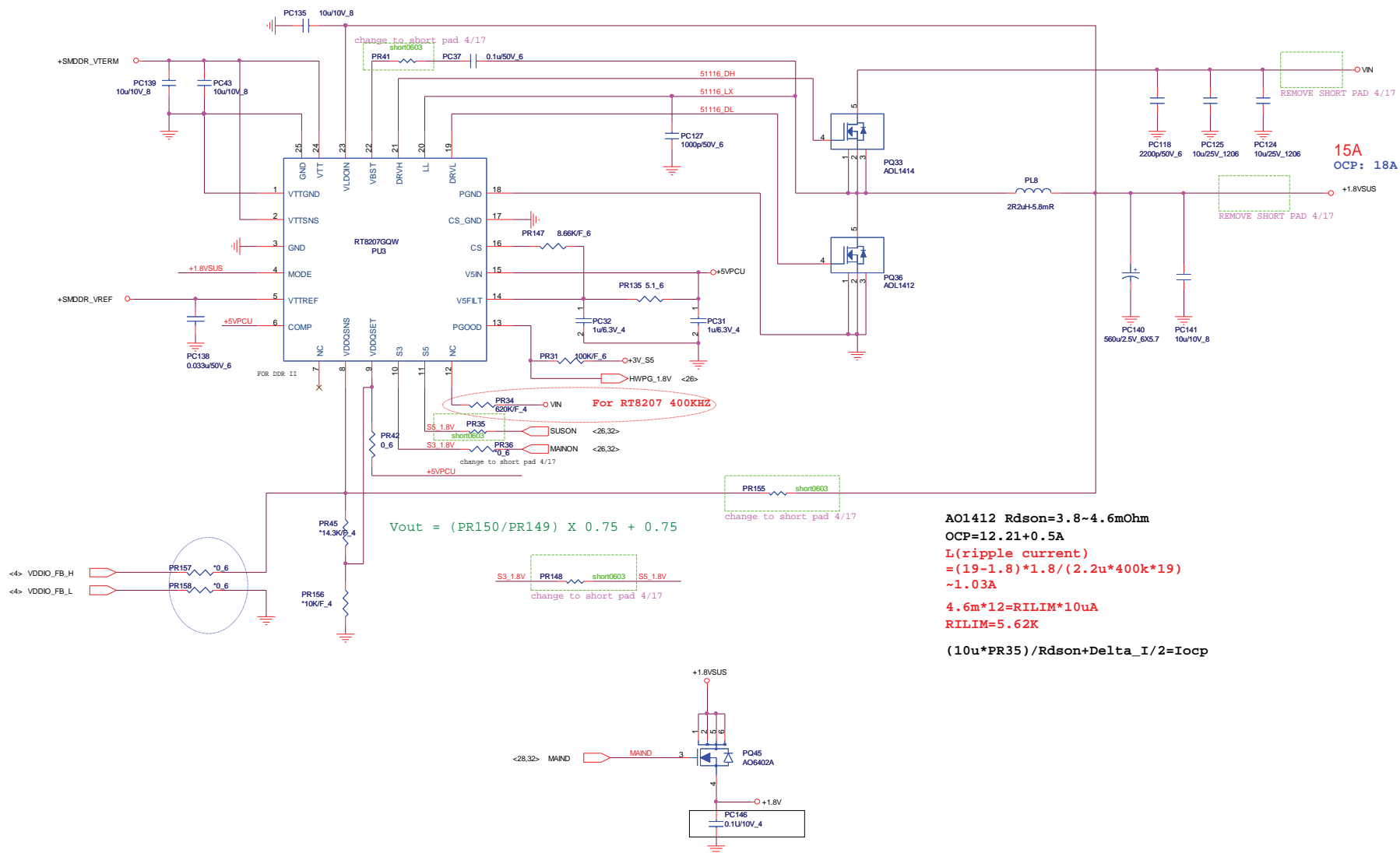
00:00

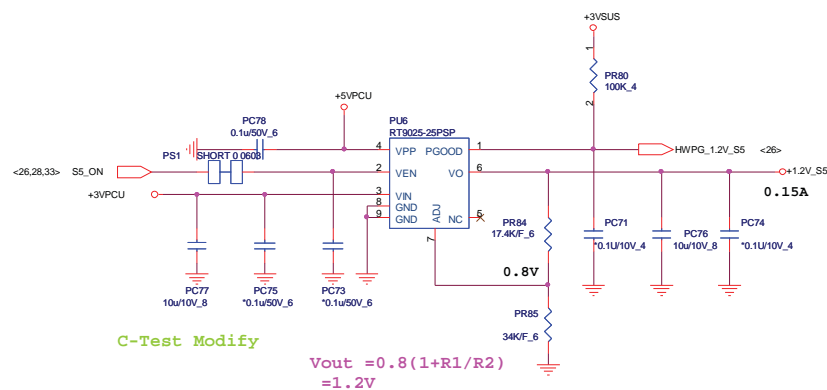
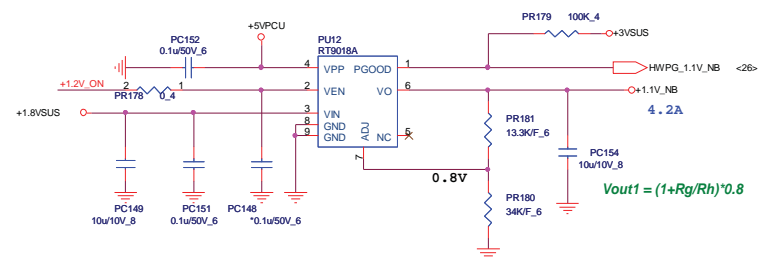
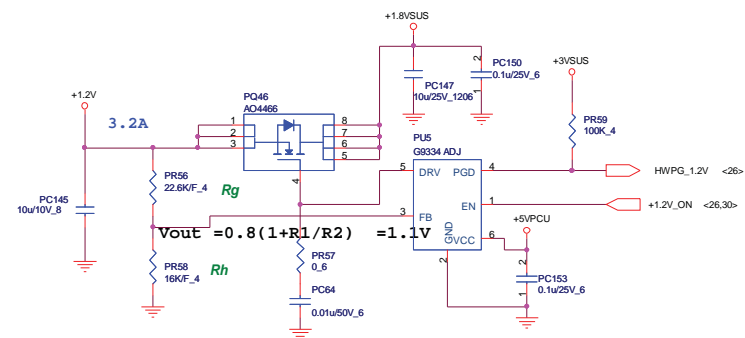
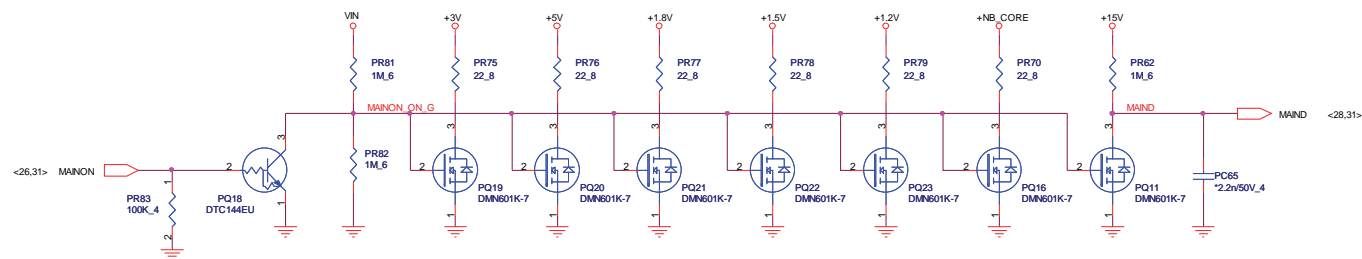
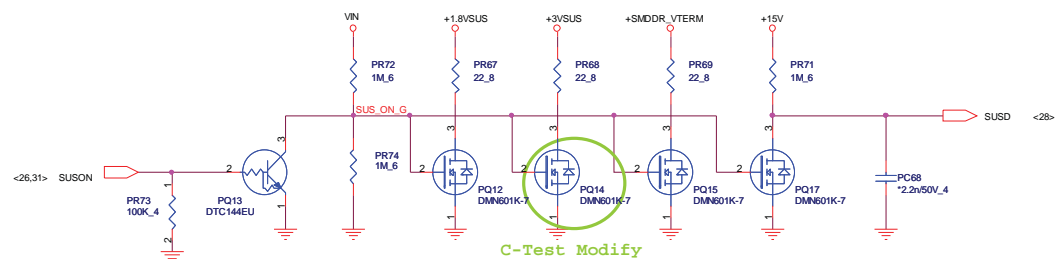
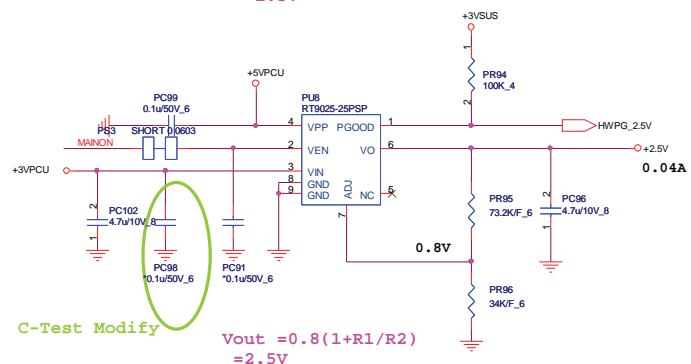
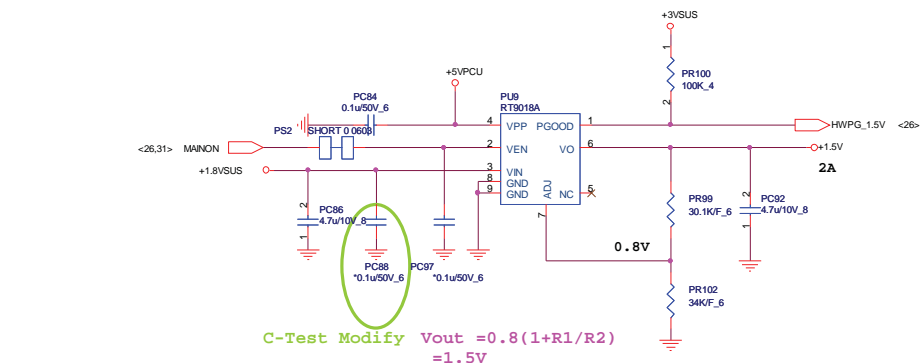
*10/F_6

PR133

A circuit diagram showing a resistor connected to a voltage source. The voltage source is represented by a battery symbol with a positive terminal on the left and a negative terminal on the right. The resistor is represented by a zigzag line. The circuit is a single loop.

Size	Document Number CPU CORE(ISL6264)	Rev 1A
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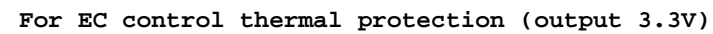




PROJECT : Z08
Quanta Computer Inc.

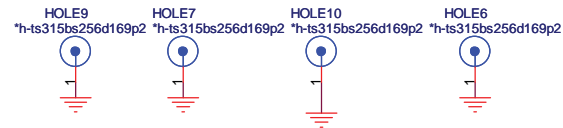
Size	Document Number	Rev
	Discharge (1.25V/1.5V)	
Date:	Tuesday, April 28, 2009	Sheet 32 of 36

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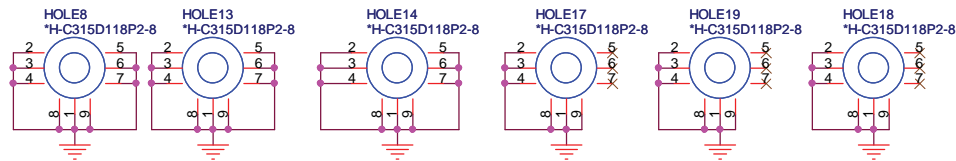


Size	Document Number Discharge (1.25V/1.5V)			Rev 1A
Date:	Tuesday, April 28, 2009	Sheet	33 of 36	

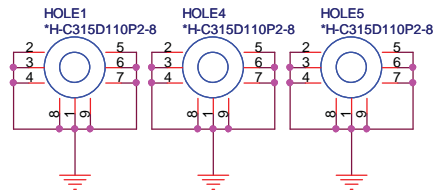
CPU HOLE



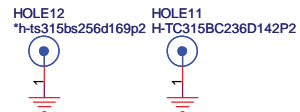
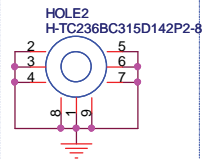
8 X 3.0



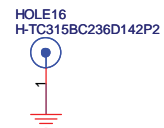
8 X 2.8



TOP 8 X 3.6 BOT 6 X 3.6



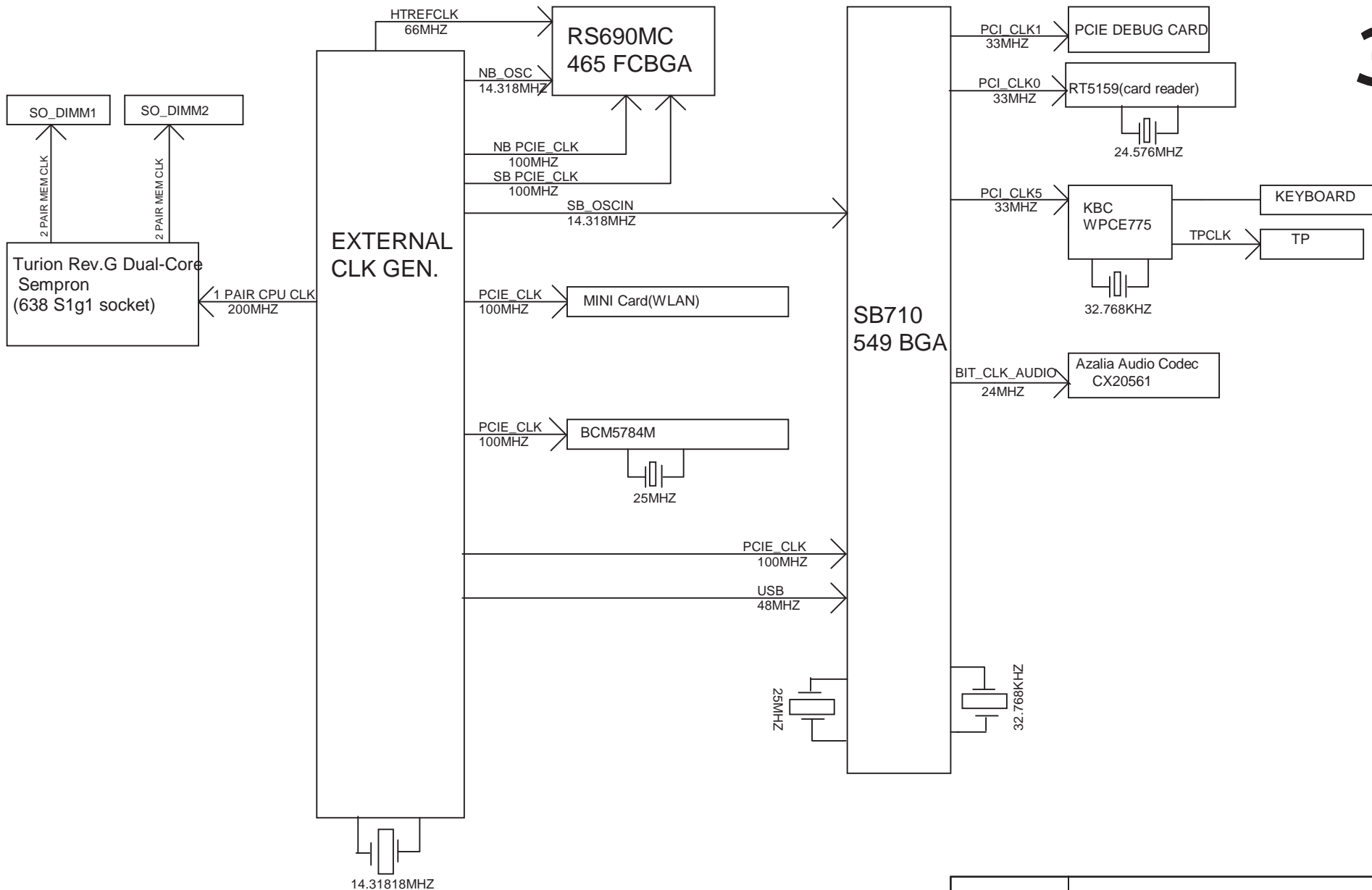
MDC

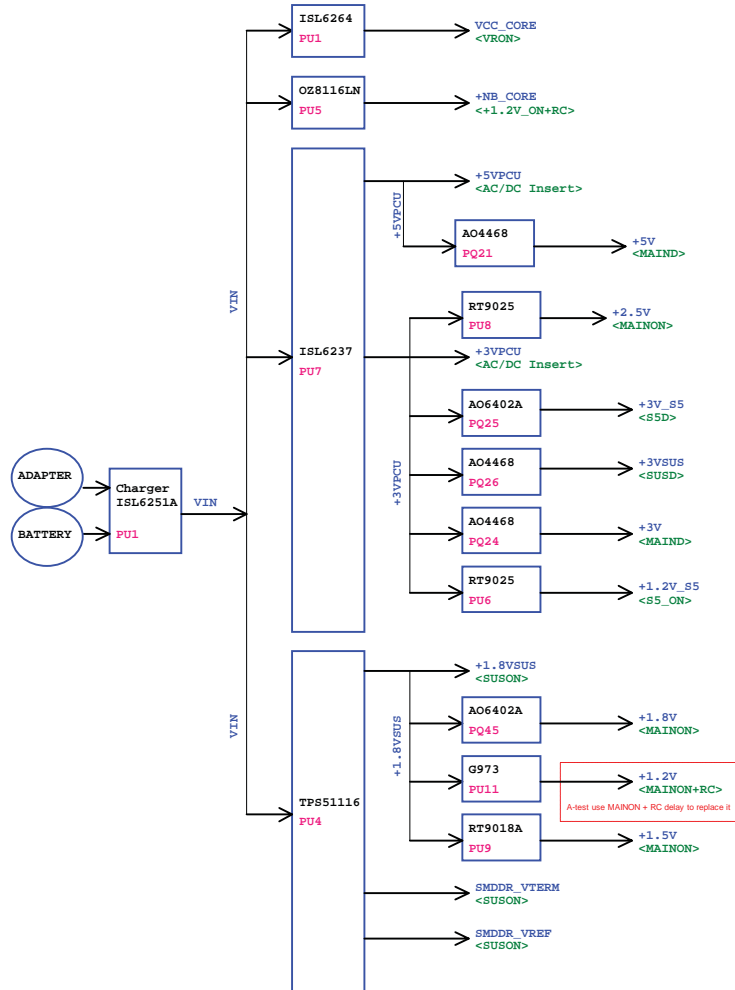


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	Blank	1A
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POWER	Distribution
VCC_CORE	CPU
+5VPCU	Battery LED , Power LED , USB , CIR , RTC
+3VPCU	HALL SENSOR , Battery LED , RF LED , kill SW , Jumper LED , KB , Power Board , EC , ID , SPI Flash , CIR
+NB_CORE	RS690M
+5V	CAMERA , Card Reader LED , ODD/HDD LED , Felica , T/P , T/sensor , CRT , HDMI , SB600 , CPU FAN , MXM , Headphone , EC , INT SPK AMP
+3V	HALL SENSOR , LCD PANEL , LVDS , WLAN , HD Decoder , NEW CARD , KB , KB LED , XD LED , Blue tooth , Touch sensor , Card Reader (OZ129) , ODD/HDD , HDMI , CRT , TVOUT , REQUIRED STRAPS , DEBUG STRAPS , SB600 , RS690M , DDR , CPU Thermal monitor , CPU FAN , CLK , MXM , VR , FM Tuner MDC , Headphone , EC , LAN , Codec(CX 20561)
+3V_S5	WLAN , NEW CARD , SB600 , MXM , LAN
+3VSUS	Finger print , SB600
+2.5V	CPU
+1.2V_S5	SB600
+1.8VSUS	SB600 , DDR , CPU , HDT
+1.8V	SB600 , LCD , LVDS , RS690M
+1.2V	SB600 , RS690M , CPU , WLAN , HD Decoder , NEW CARD
+SMDDR_VTERM	DDR , CPU
+SMDDR_VREF	DDR
+5V_S5	