

Compal Confidential

Schematics Document

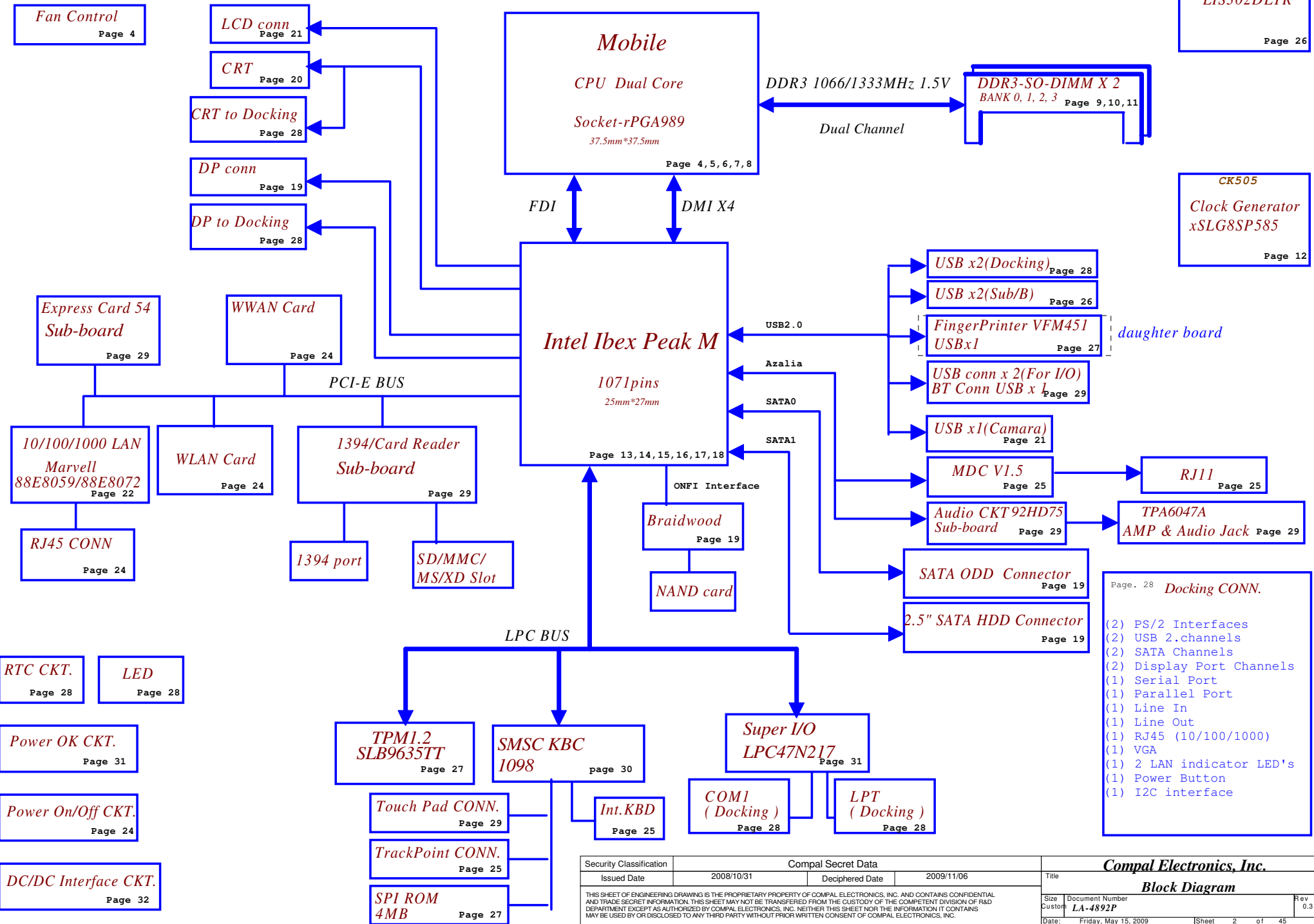
AUBURNDALE with Intel
IBEX PEAK-M core logic

Dior UMA

2009-05-16

REV: 0.3

Security Classification		Compal Secret Data		Title	
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				Custom	0.3
				Cover Sheet	
				Date:	Friday, May 15, 2009
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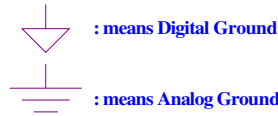


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Voltage Rails (O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	+B +3VL	+5VALW +3VALW	+1.5V +0.75V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +1.05VS +1.8VS
S0	O	O	O	O	O
S1	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC	O	O	O	X	X
S5 S4/ Battery only	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X

Symbol Note :



Install below 43 level BOM structure for ver. 0.2

8072@ : Install for 8072 NIC controller

Install below 45 level BOM structure for ver. 0.2

45@ : means just put it in the BOM of 45 level.

Reserve below BOM structure for ver. 0.2

@ : means just reserve , no build

CONN@ : means ME part.

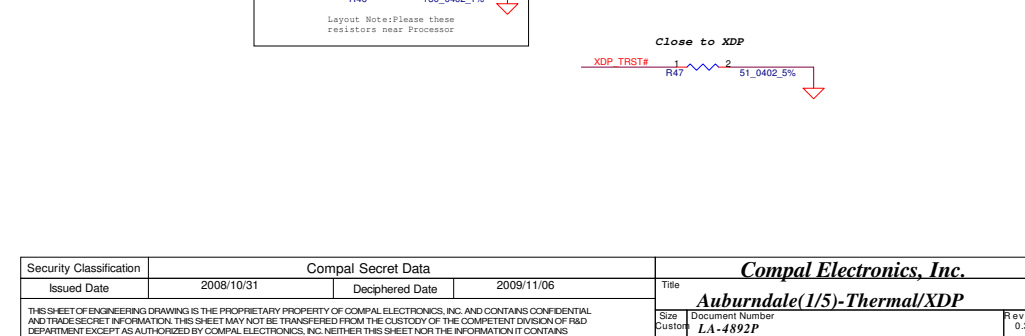
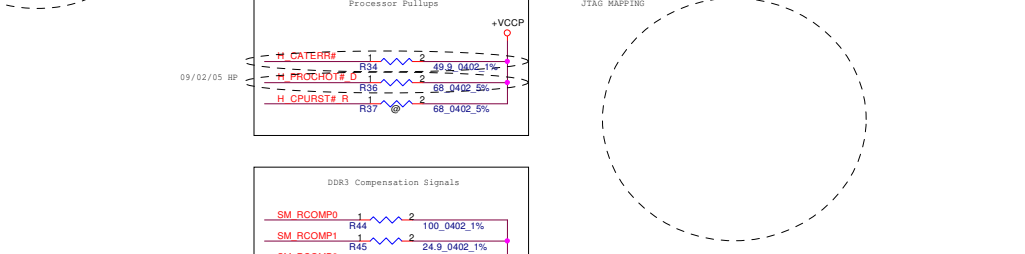
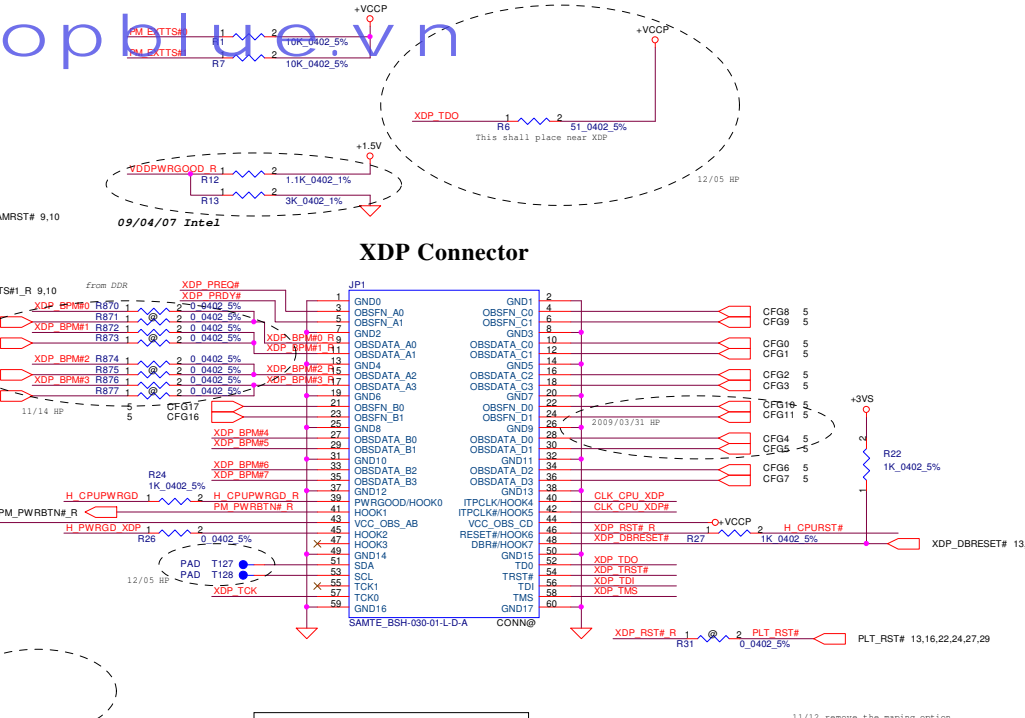
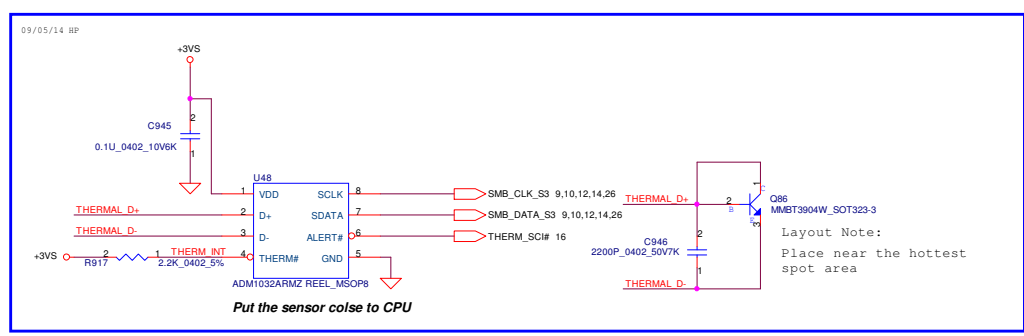
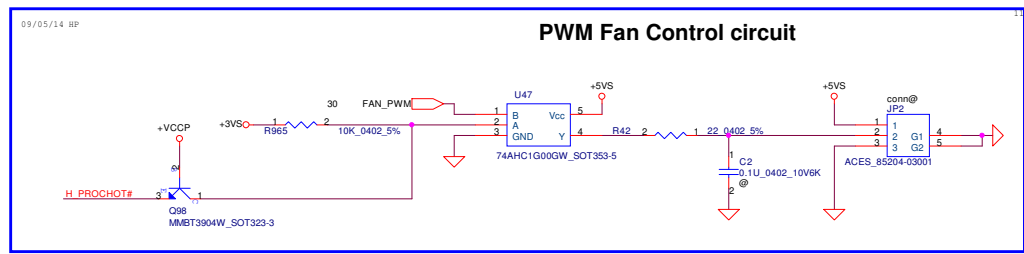
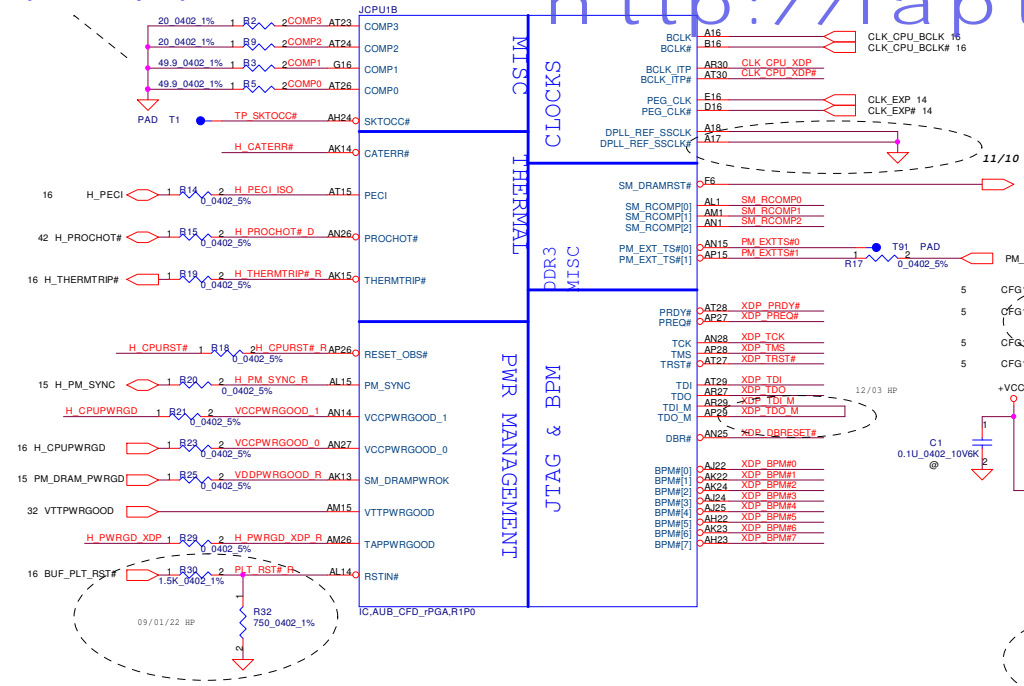
8059@ : Install for 8059 NIC controller

SMBUS Control Table

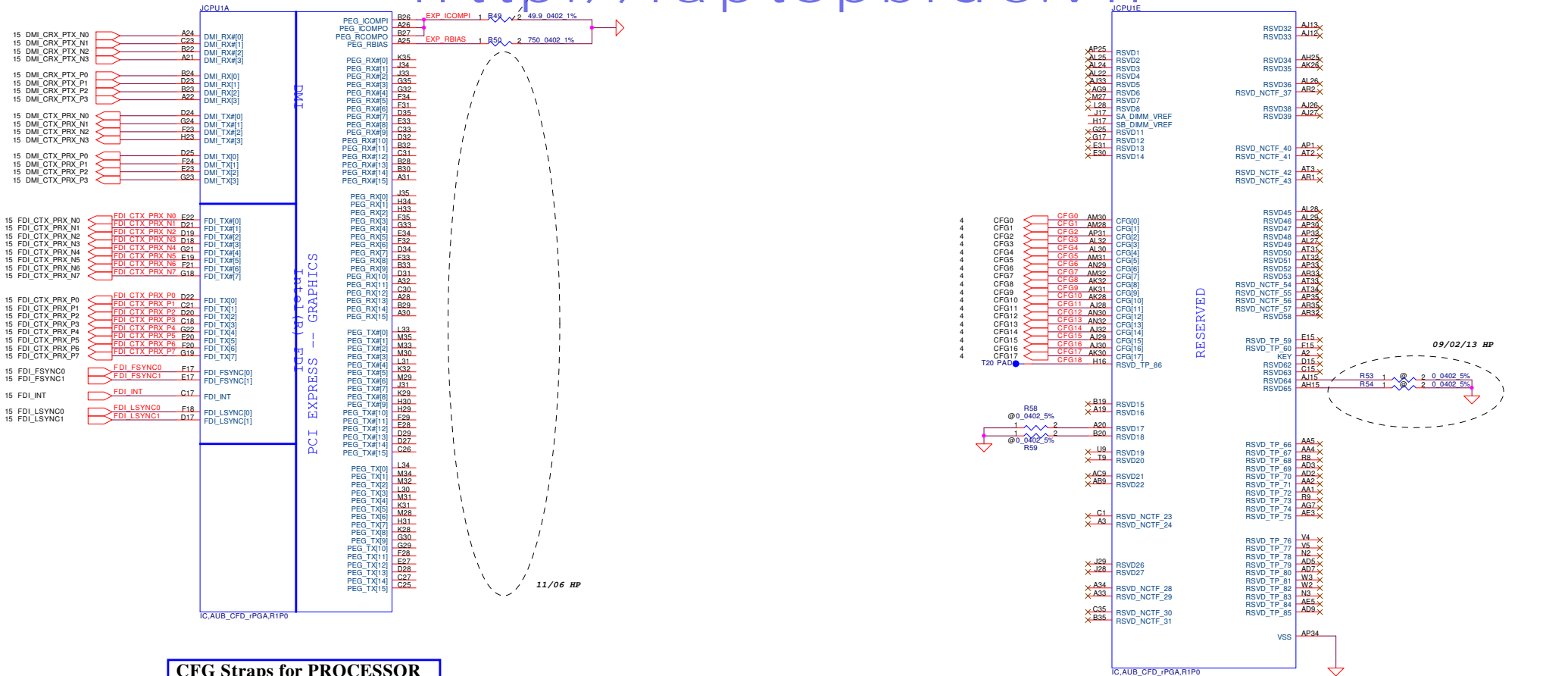
	SOURCE	BATT	XDP	SODIMM	CLK CHIP	MINI CARD	DOCK	NIC	THERMAL SENSOR	G-SENSOR
SMB_EC_CK1 SMB_EC_DA1	SMSC1098	V	X	X	X	X	X	X	X	X
SMBCLK SMBDATA	Calpella	X	V	V	V	V	V	V	X	V
SML0CLK SML0DATA	Calpella	X	X	X	X	X	X	X	X	X
SML1CLK SML1DATA	Calpella	X	X	X	X	X	X	X	V	X

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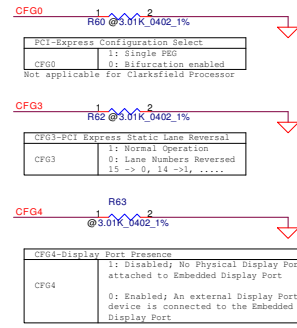
Layout rule: 10mil width trace
length < 0.5", spacing 20mil



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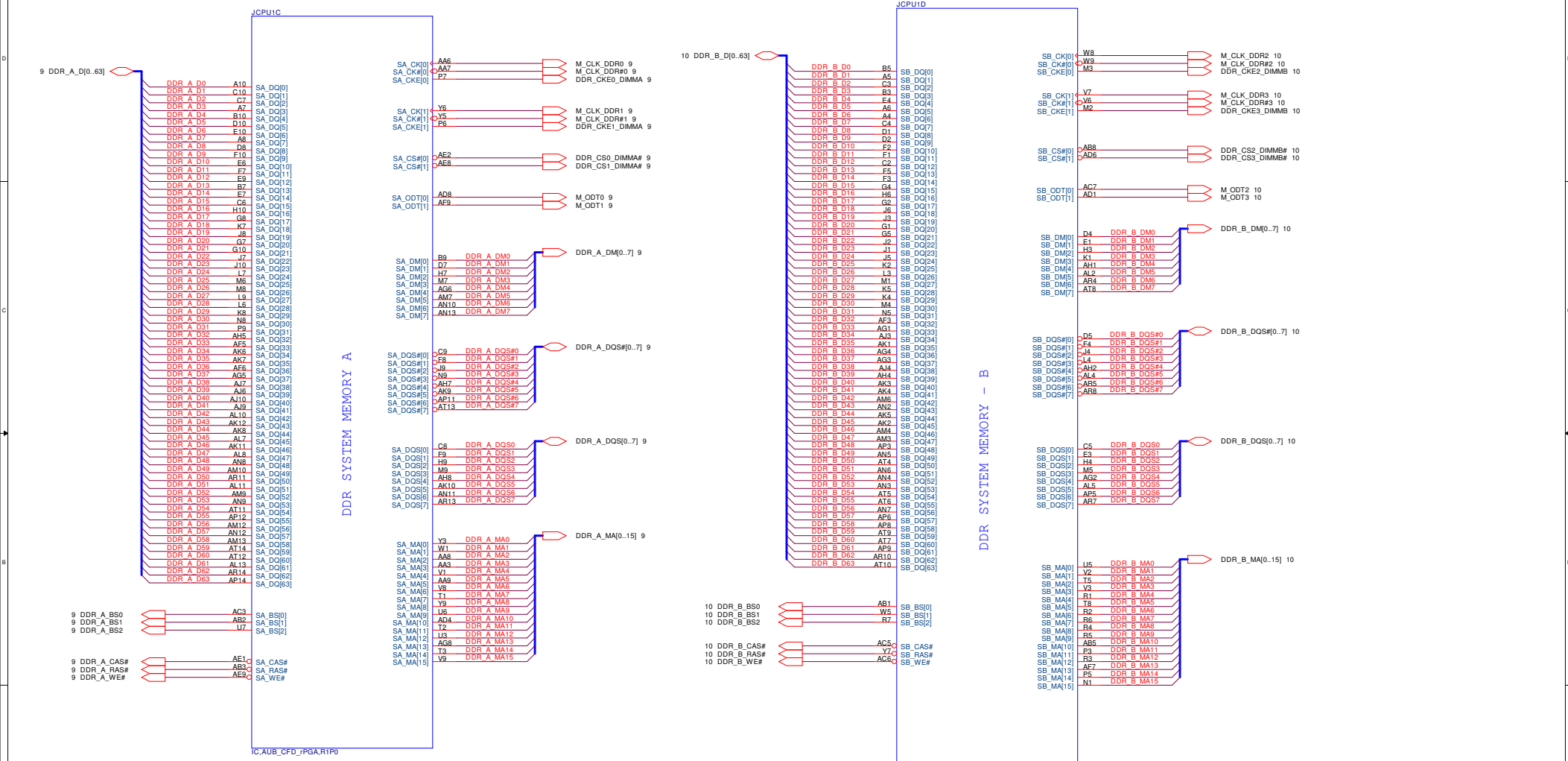


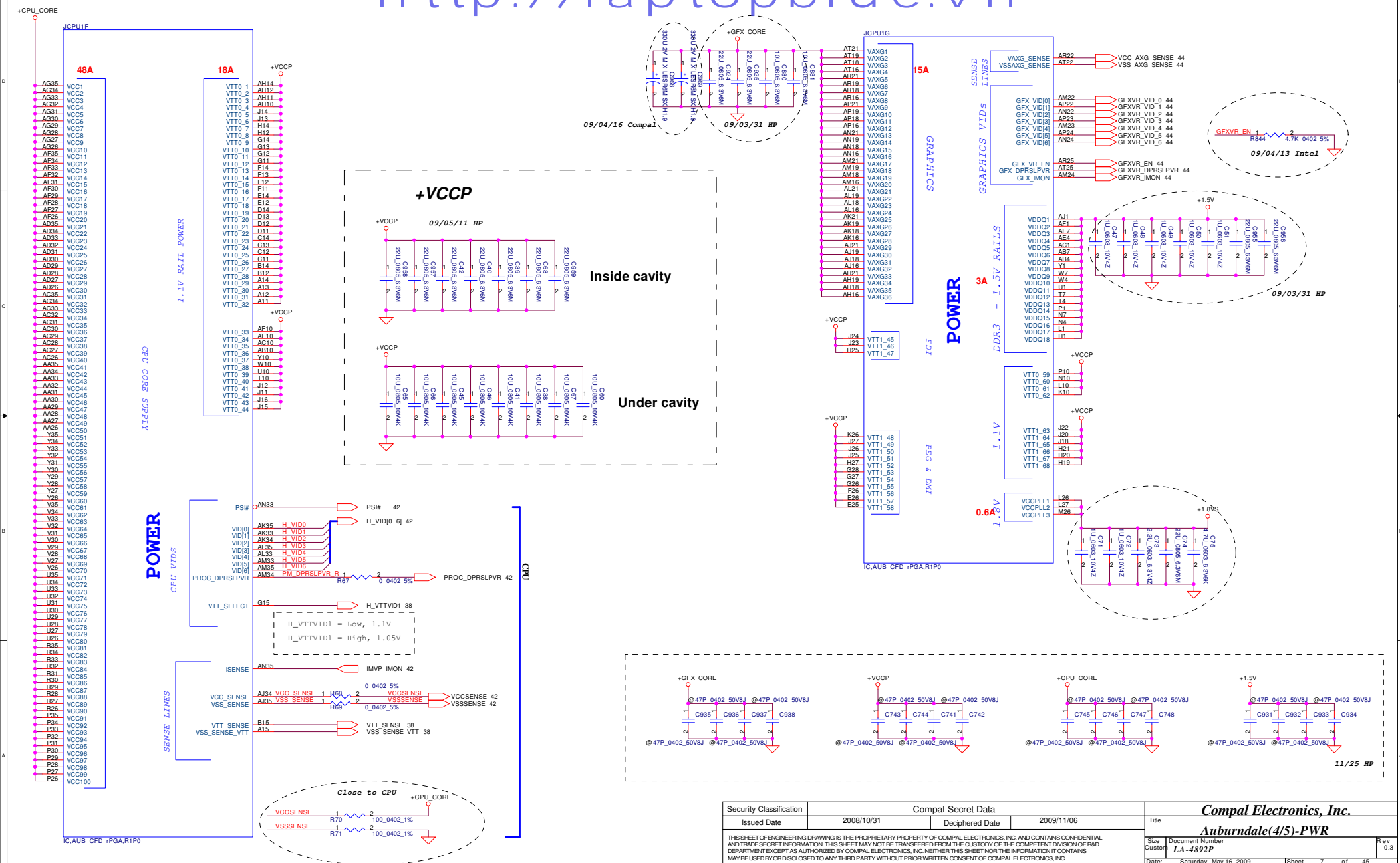
CFG Straps for PROCESSOR



CFG7
R61 @ 5.01K_0402_1%
Only temporary for early CTD samples (rPGA/BGA)
No needed by MoW41.

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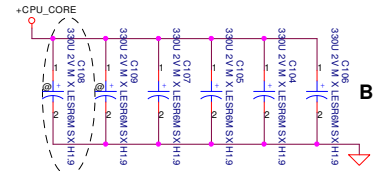
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Title		Compal Electronics, Inc.	
Size		Auburndale(4/5)-PWR	
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Under cavity

Bulk caps

Inside cavity



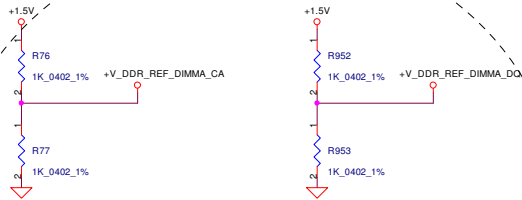
09/01/15 HF

09/01/15 HP

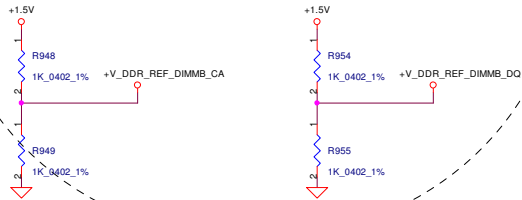
BGA Ball Cracking Prevention and Detection

Security Classification	Compal Secret Data			<i>Compal Electronics, Inc.</i> <i>Auburndale(5/5)-GND/Bypass</i>		
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09/04/03 Auburndale/Arrandale only supports M1 change Vref to +V_DDR_CPU_REF



09/04/23 HP



11/20 HP

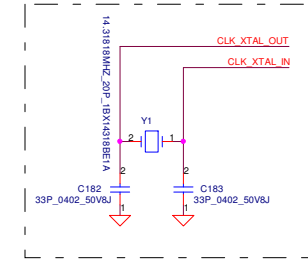
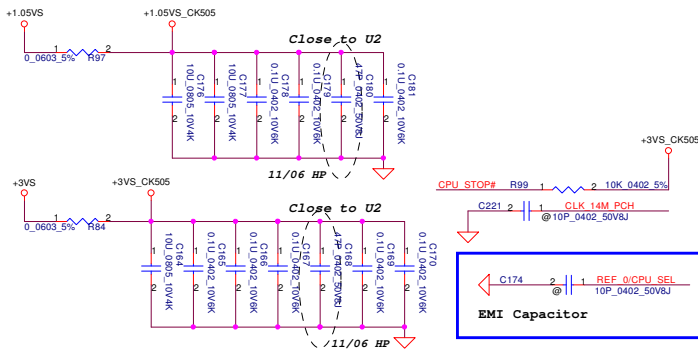
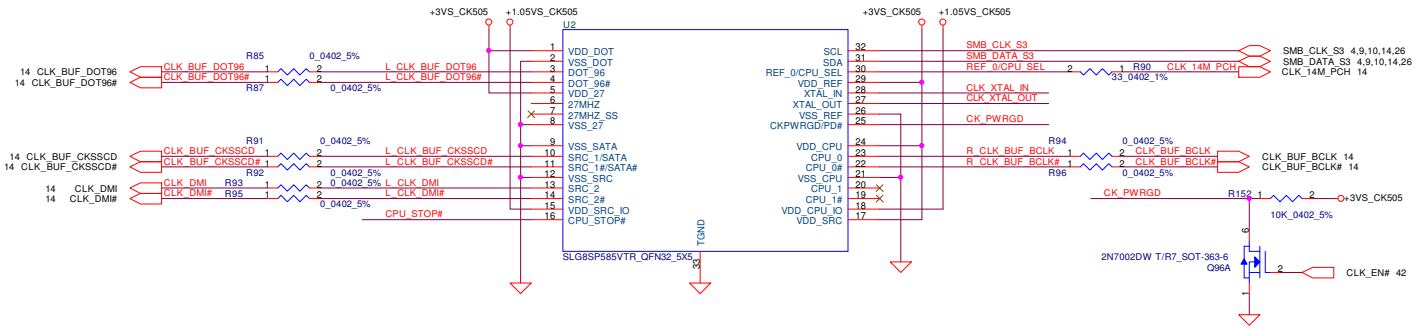
09/03/31 Auburndale/Arrandale only supports M1, HP

11/20 HP

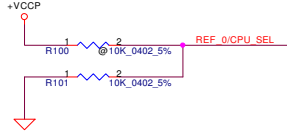
09/03/31 Auburndale/Arrandale only supports M1, HP

11/20 Auburndale does not require to support M2 for VrefDQ, HP

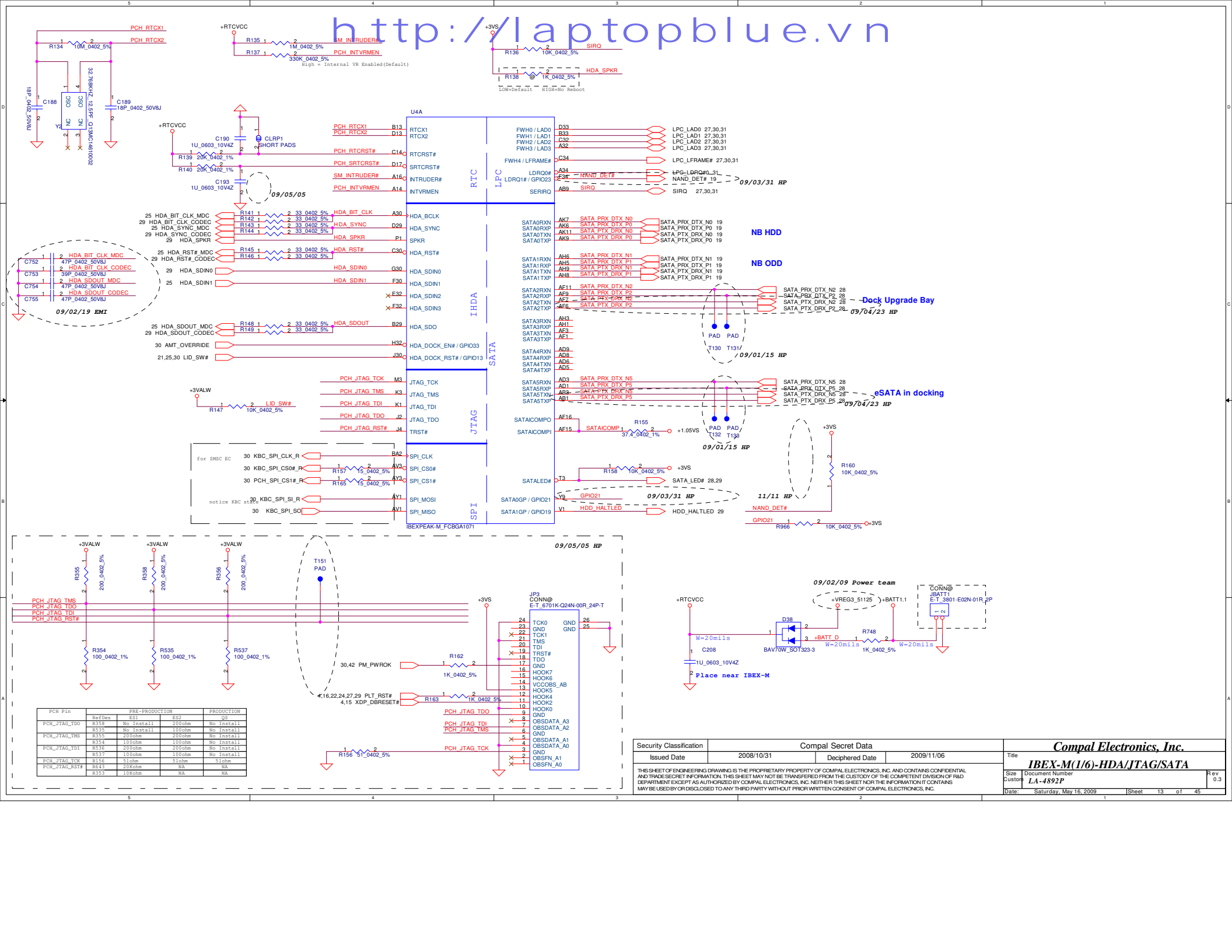
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PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

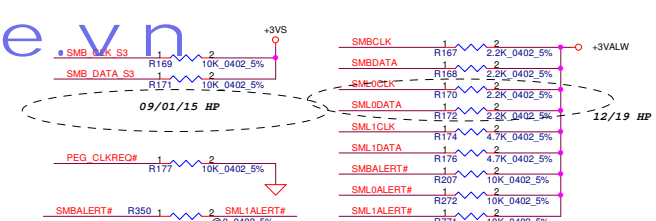


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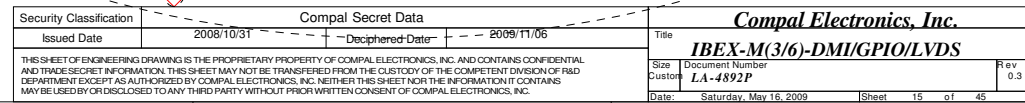
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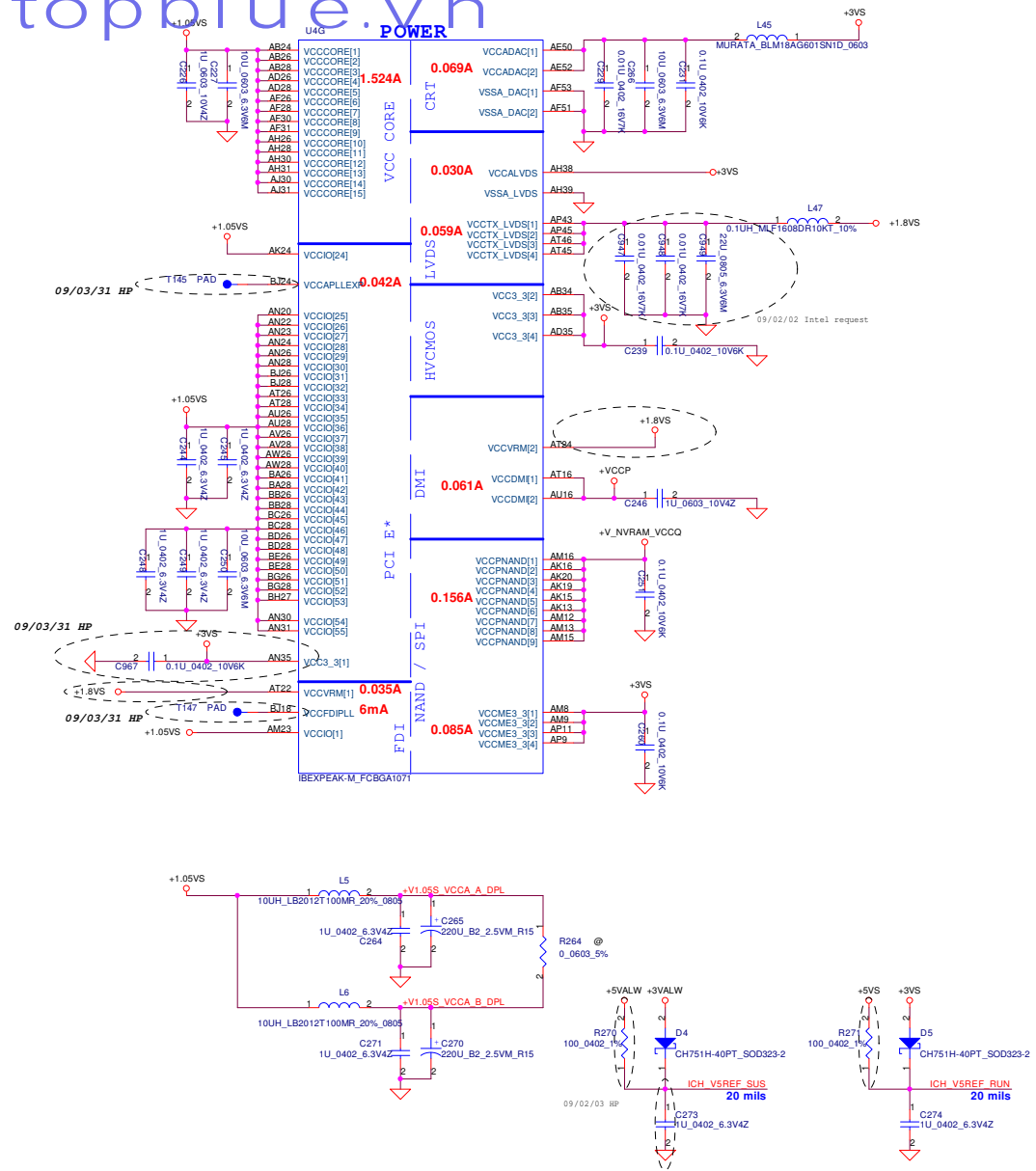
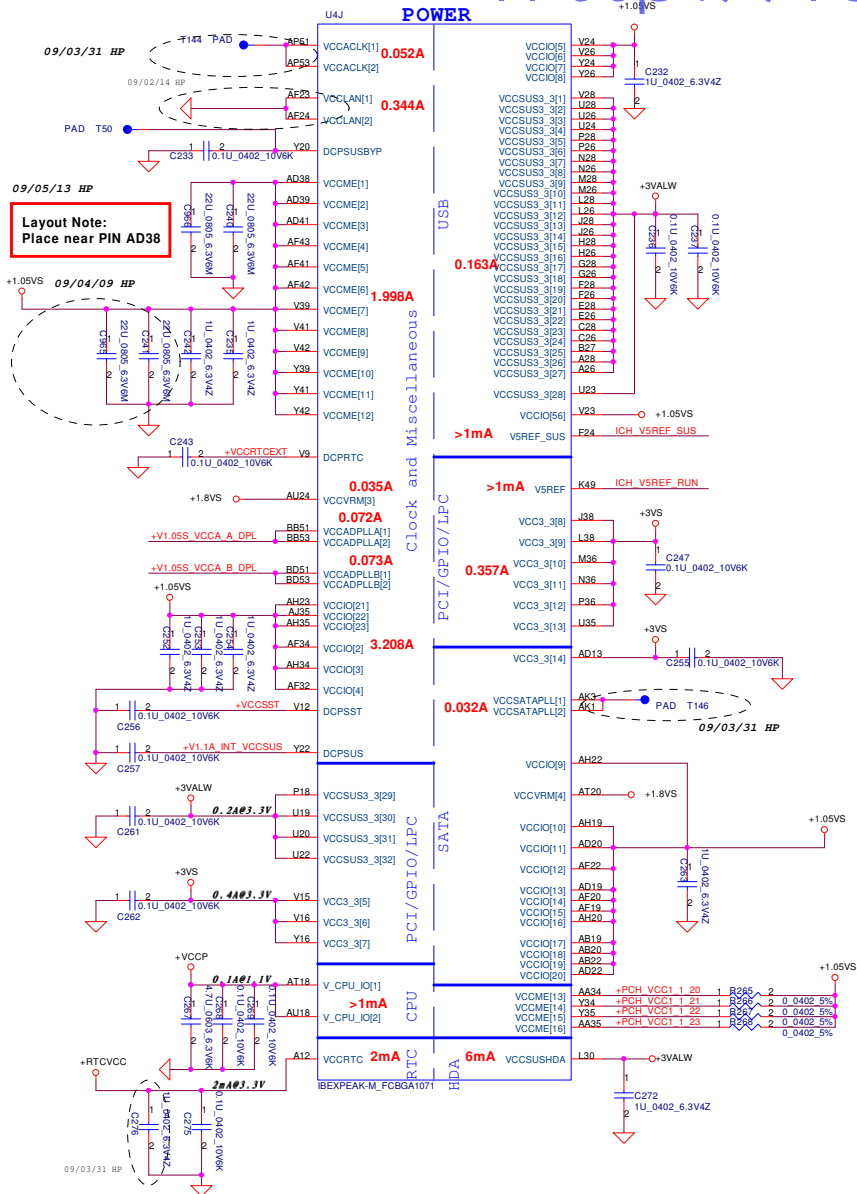
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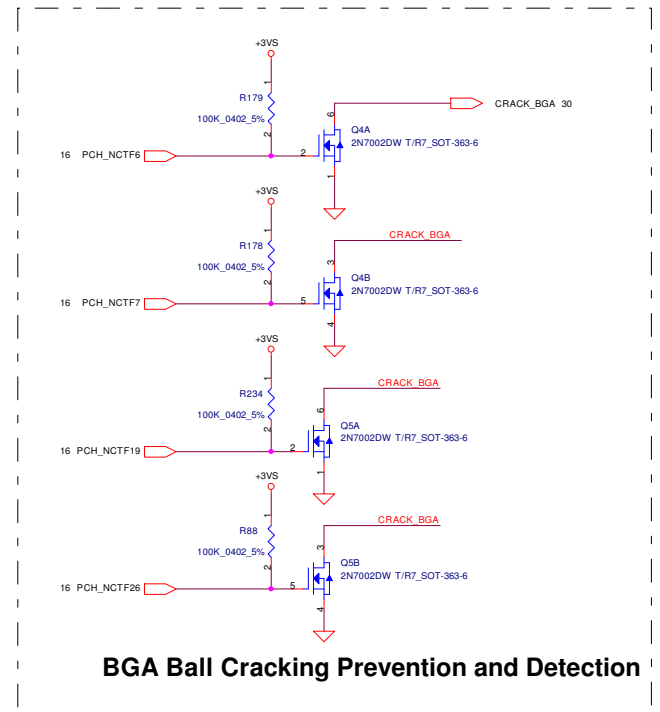
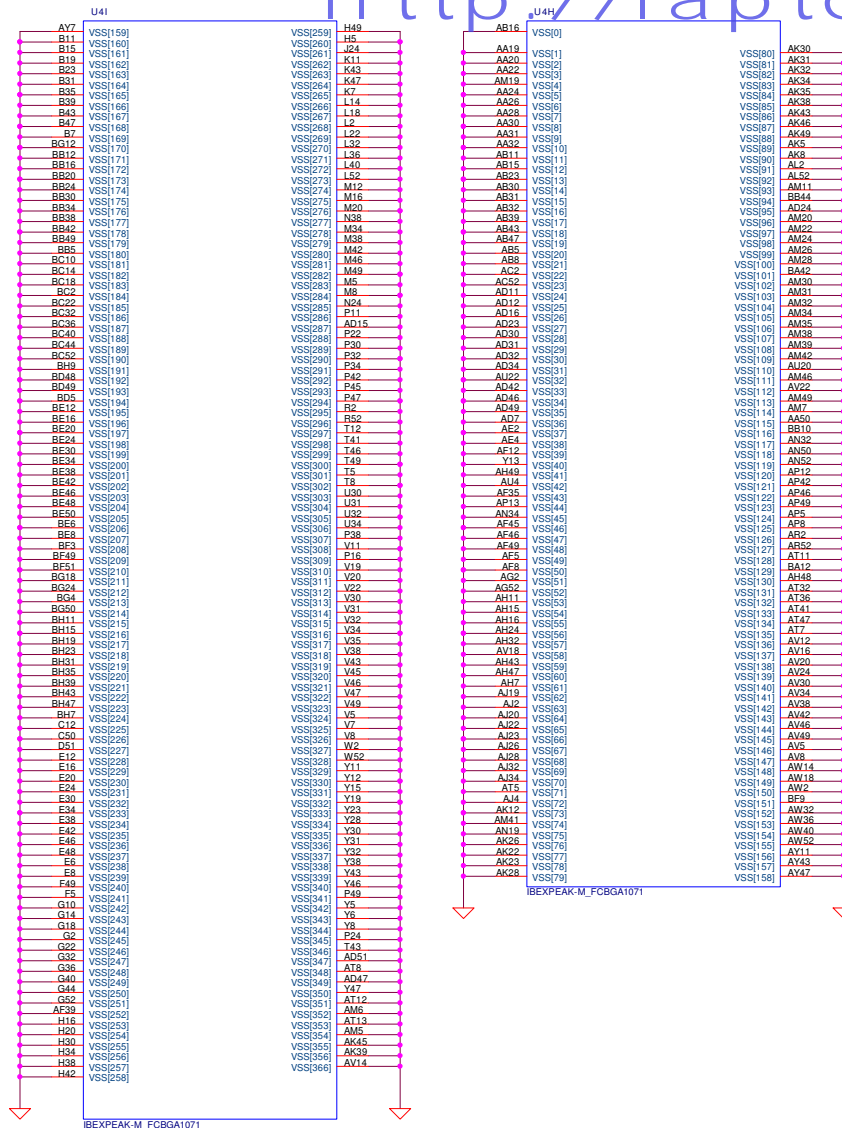
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IBFA-M (20)-PCI-E/SMBUS/CLK			
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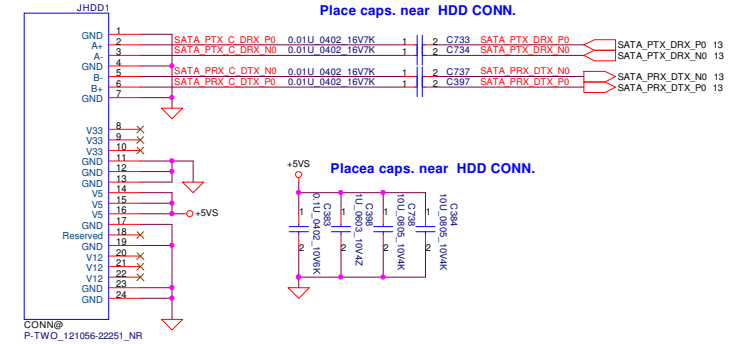
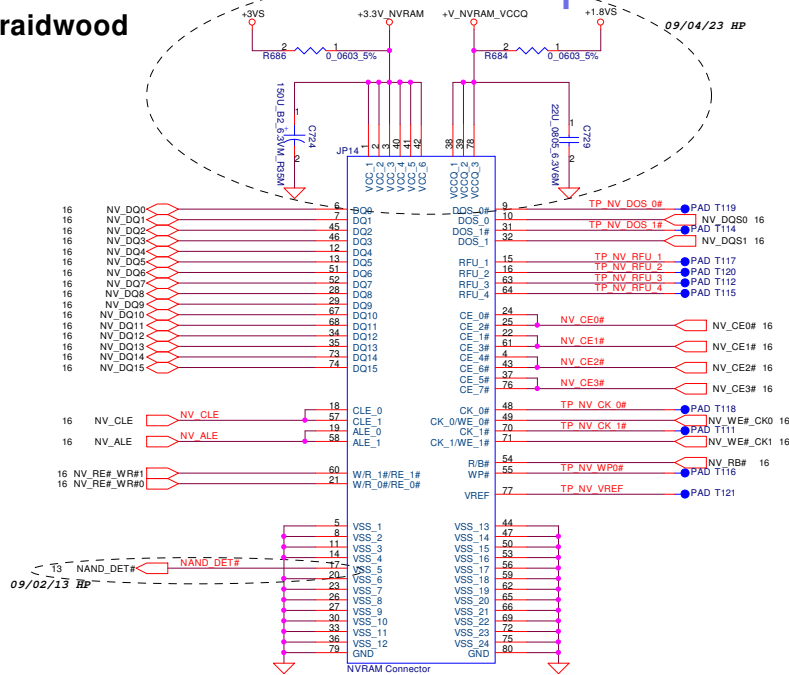
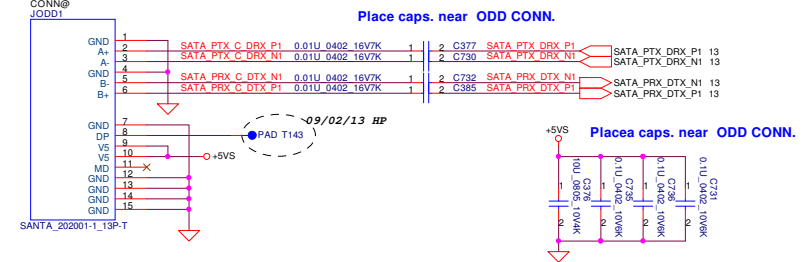


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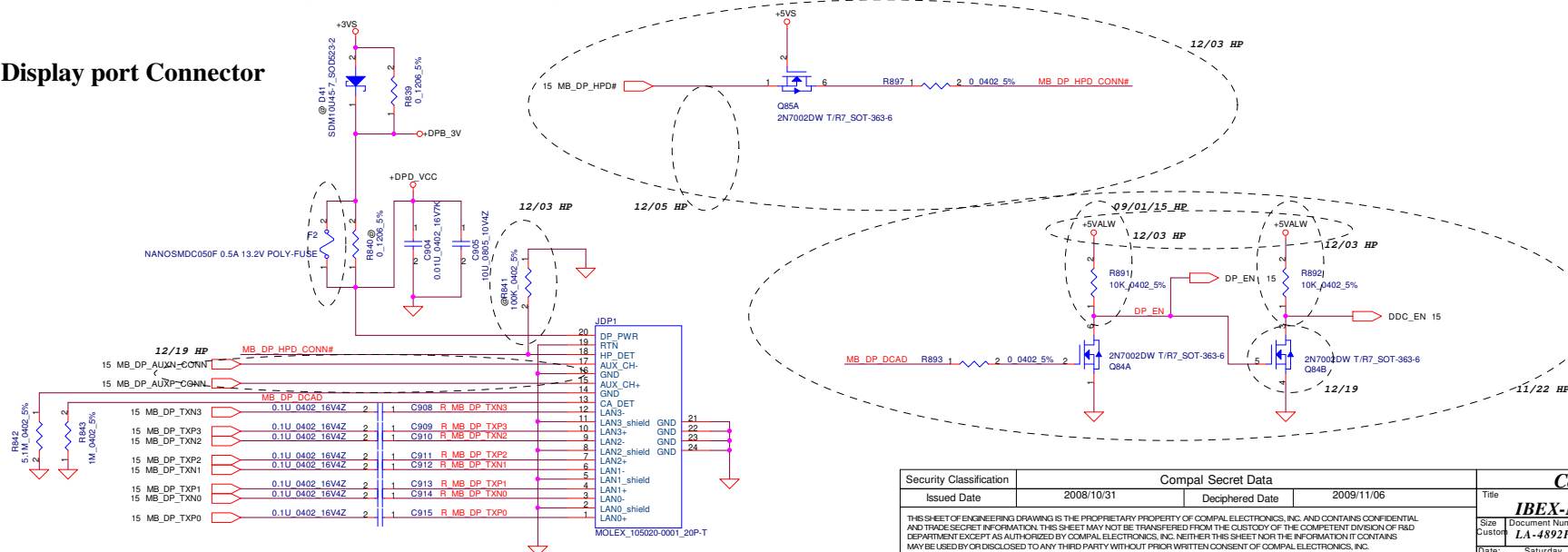


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Braidwood

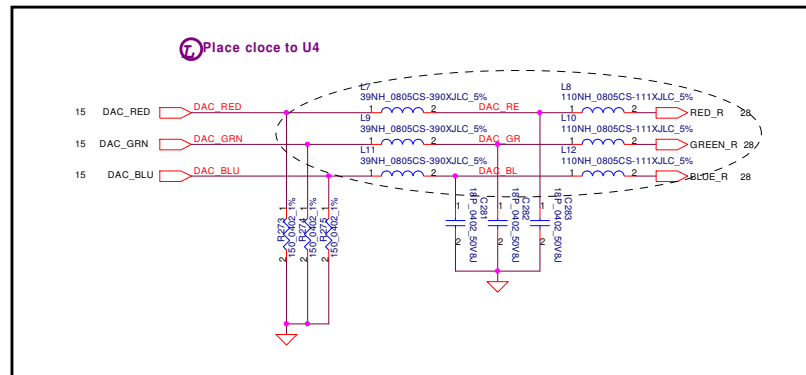
**SATA ODD CONN.**

Display port Connector

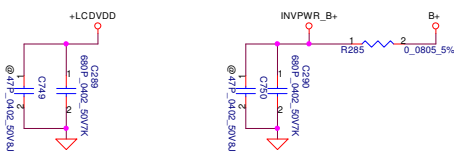
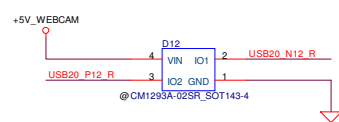
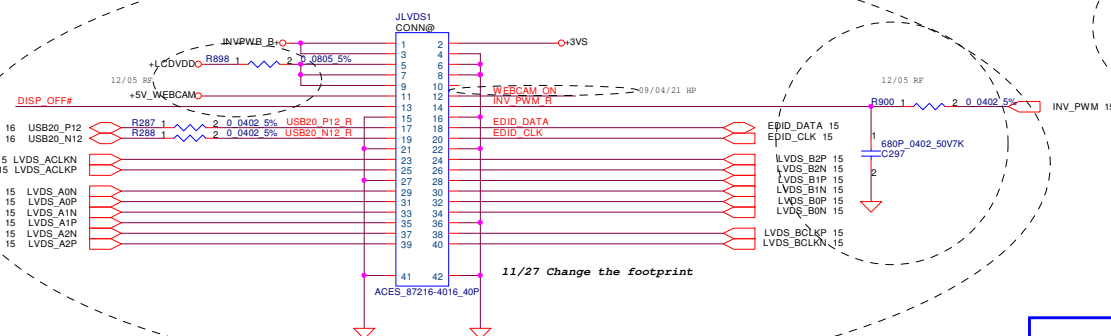


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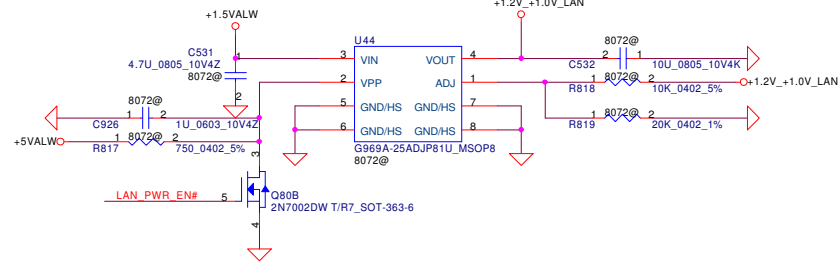
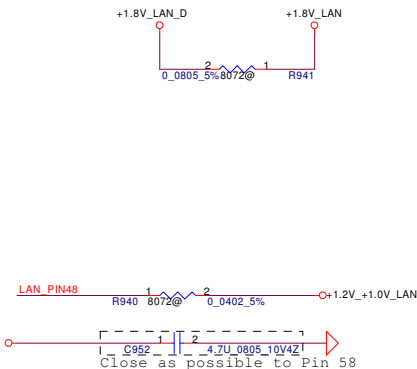


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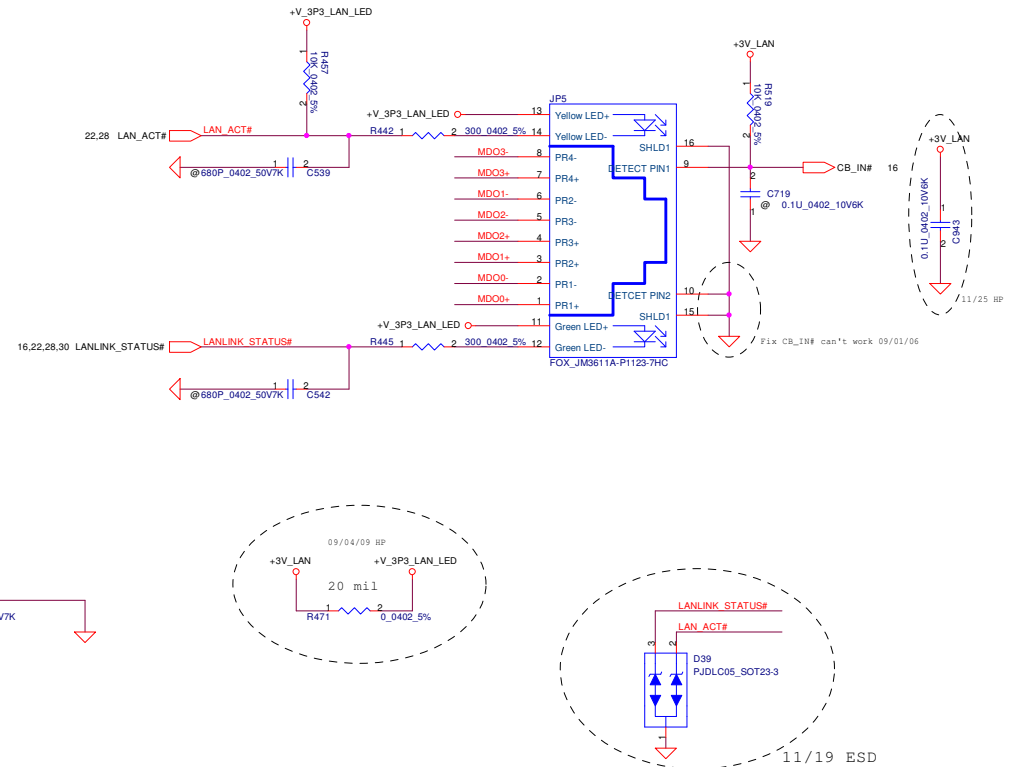
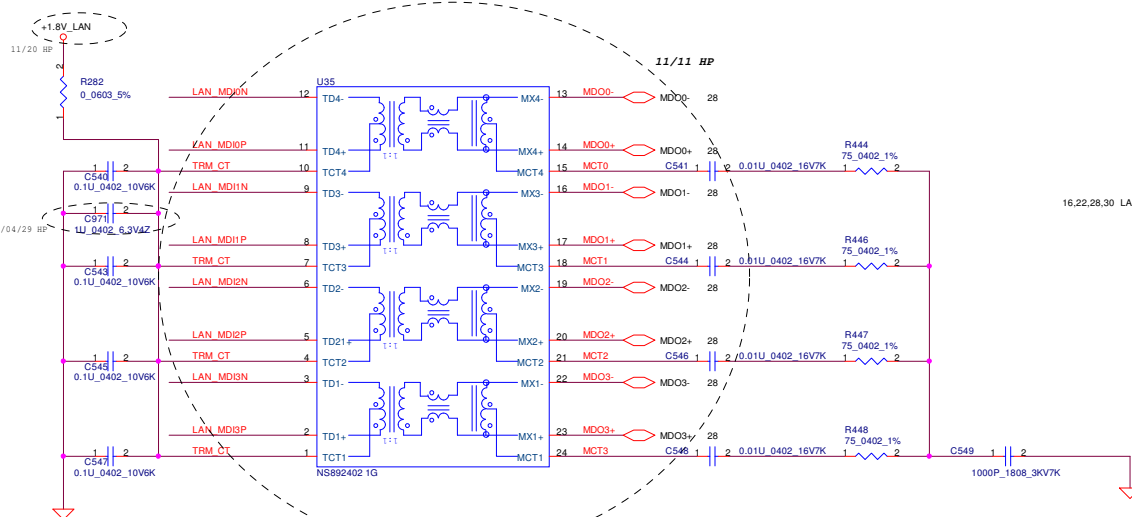
09/04/13 HP

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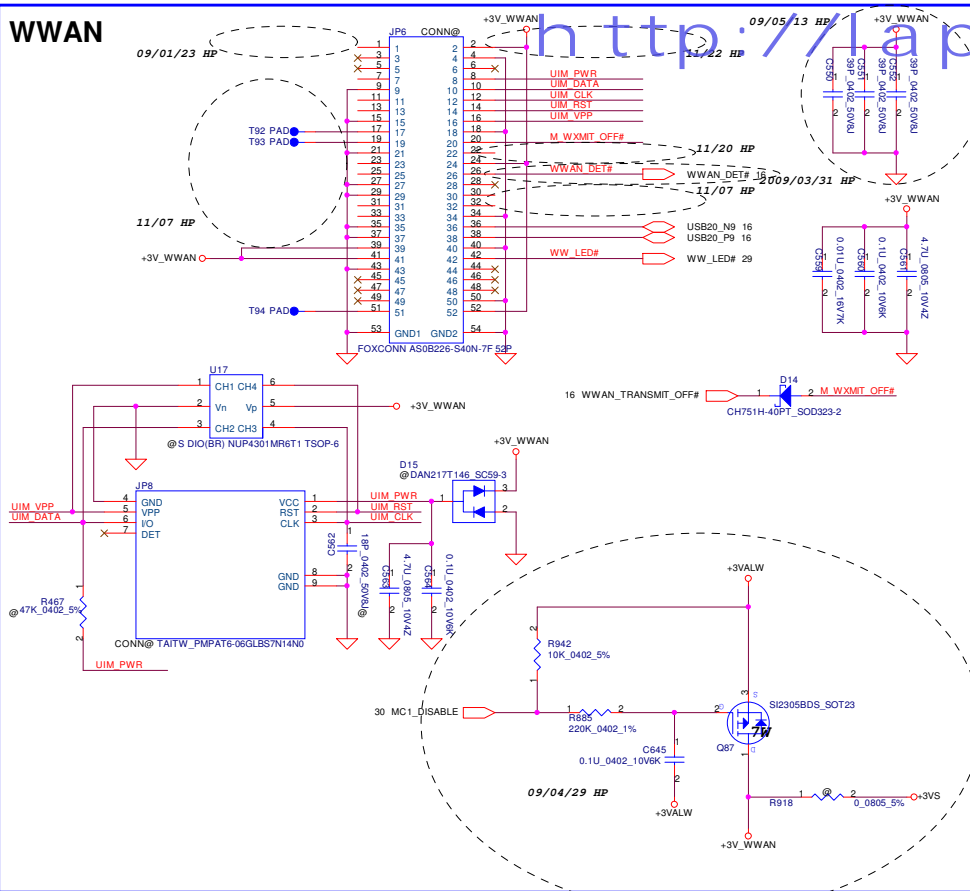
<i>Compal Electronics, Inc.</i>			
Title Giga LAN 88E8059/88E8072			
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22 LAN_MD10P LAN_MD10N
22 LAN_MD10N LAN_MD10N
22 LAN_MD11P LAN_MD11P
22 LAN_MD11N LAN_MD11N
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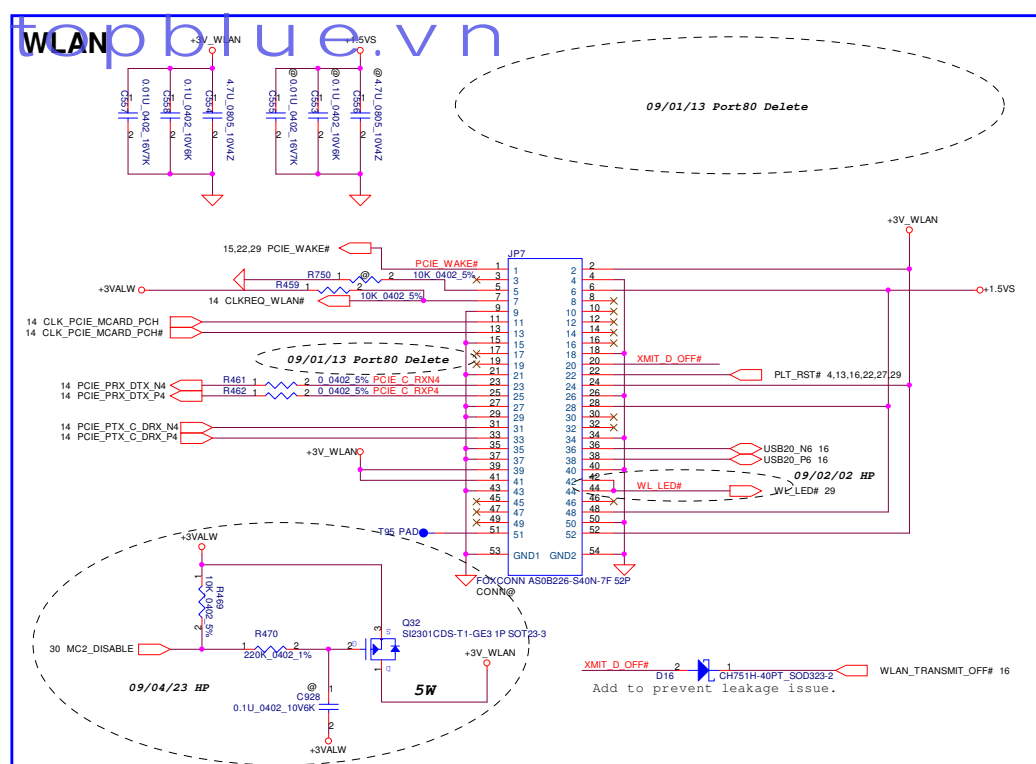


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WWAN



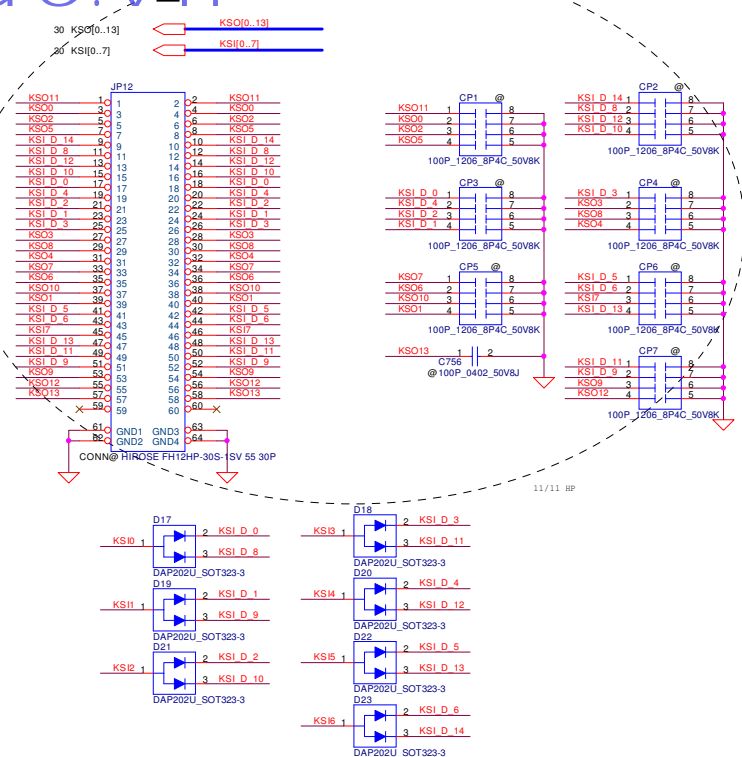
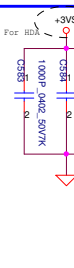
WLAN



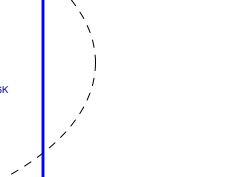
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http://laptopblue.wpi.edu INT_KBD_CONN.

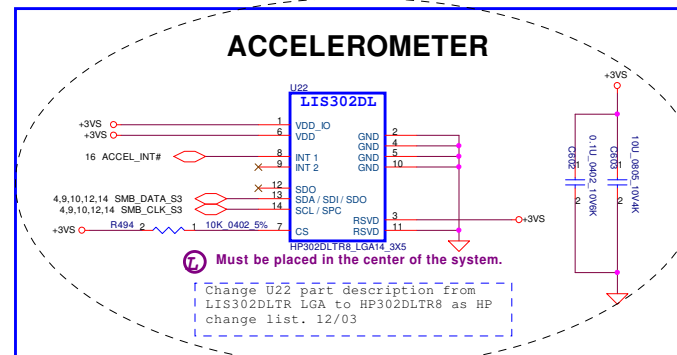
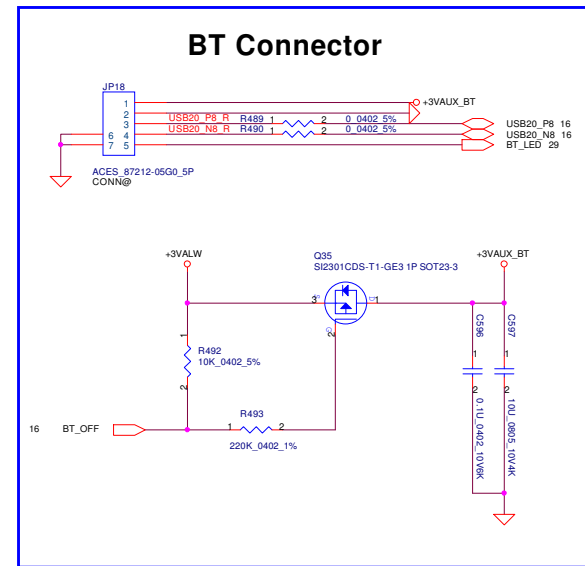
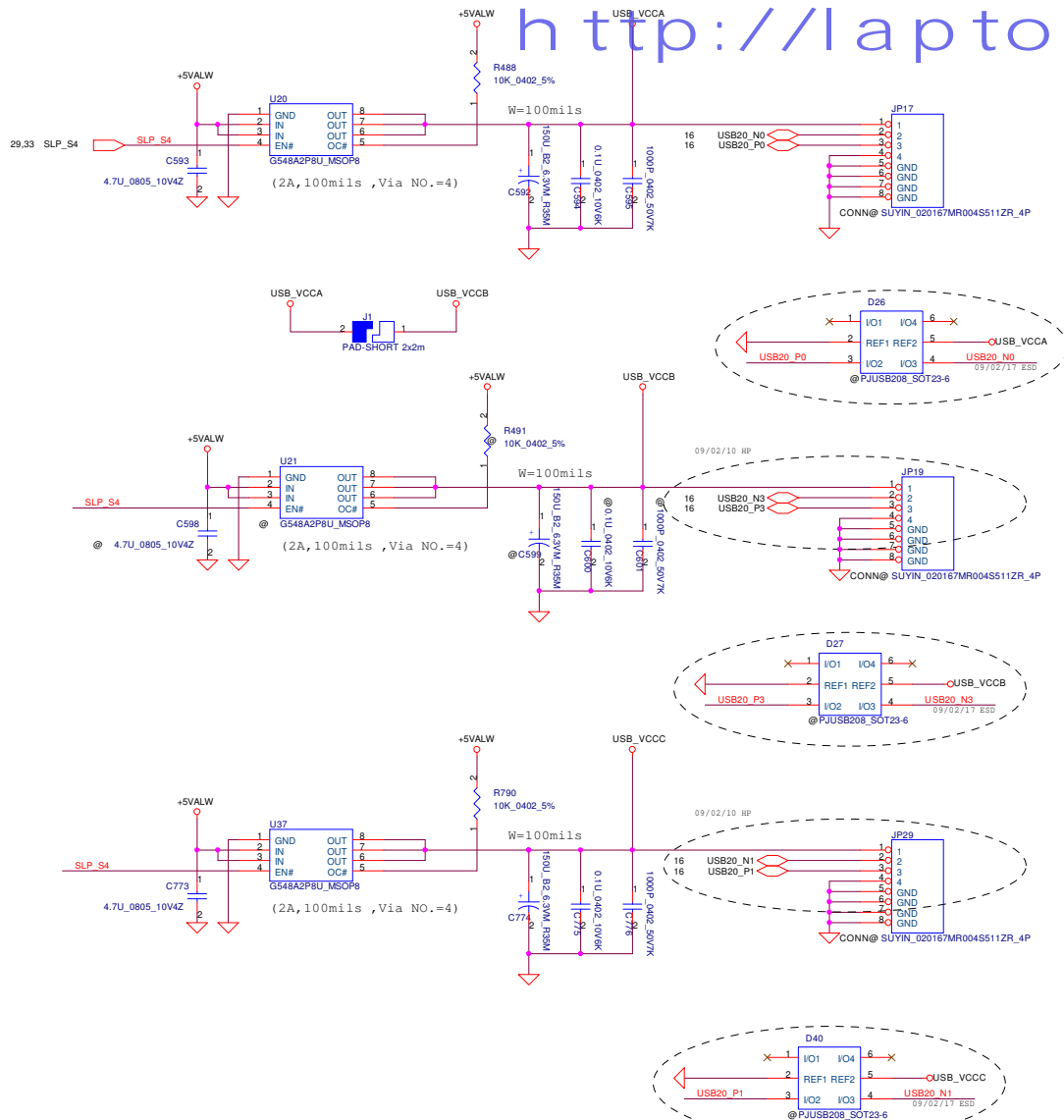
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Issued Date		Deciphered Date		USB & BT Connector & Accelerometer	
2008/10/31		2009/11/06		Size	
				Document Number	
				LA-4892P	
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				Saturday, May 16, 2009	
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				26 of 45	
				Rev	
				0.3	

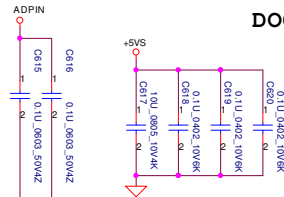
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TPM1.2 on board



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Issued Date	2008/10/31	Deciphered Date	2009/11/06	Title	TCG/BIOS ROM/PS2/SW LPC DEBUG	
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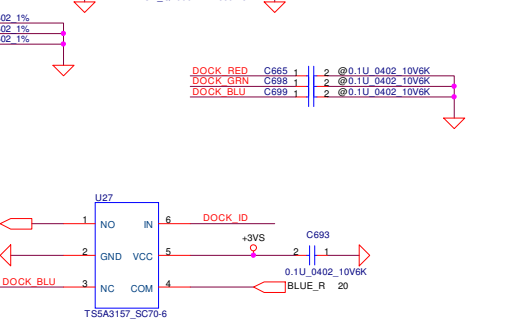
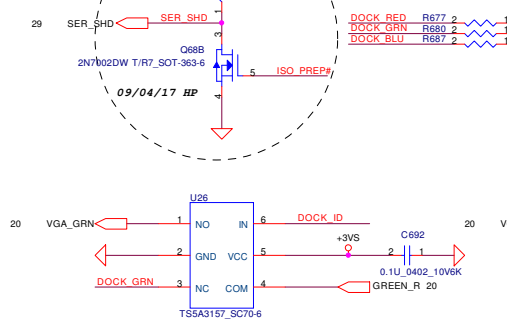
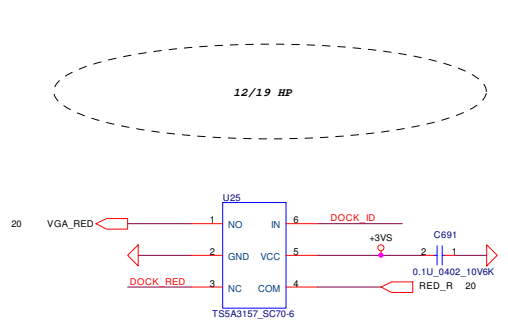
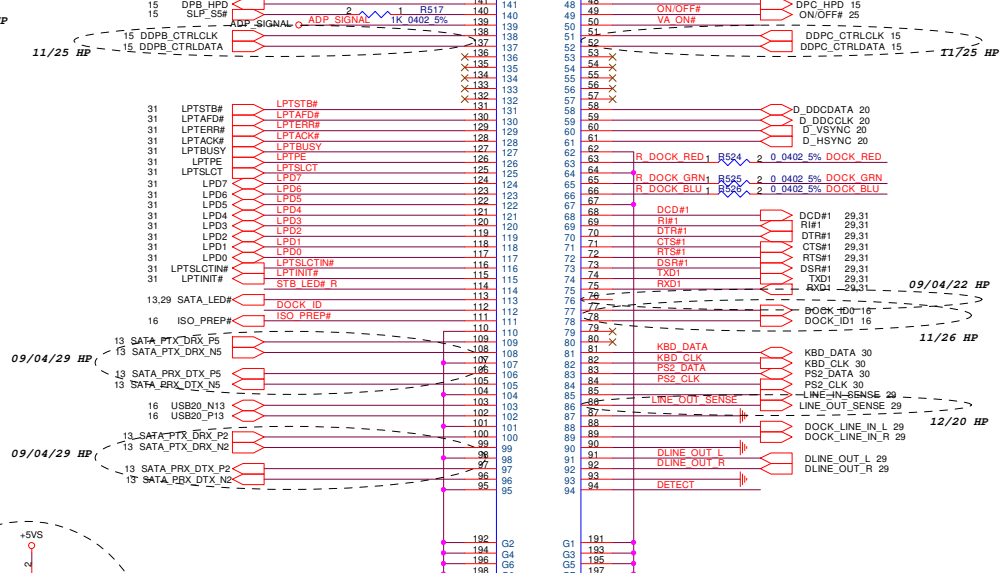
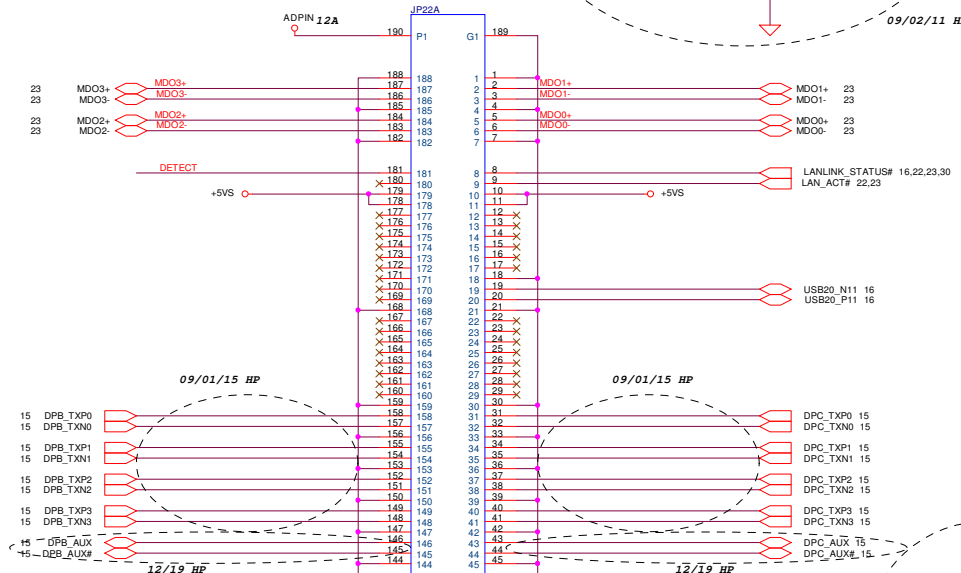
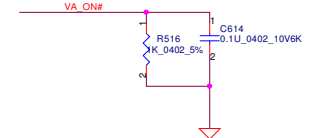
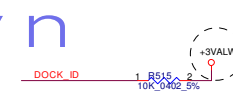
- (2) PS/2 Interfaces
- (2) USB 2.channels
- (2) SATA Channels
- (2) Display Port Channels
- (1) Serial Port
- (1) Parallel Port
- (1) Line In
- (1) Line Out
- (1) RJ45 (10/100/1000)
- (1) VGA
- (1) 2 LAN indicator LED's
- (1) Power Button
- (1) I2C interface



DOCK CONN. 190PIN

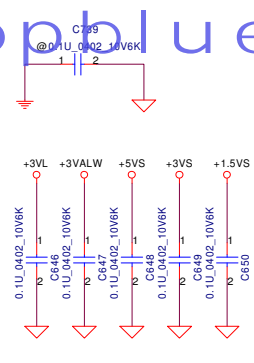
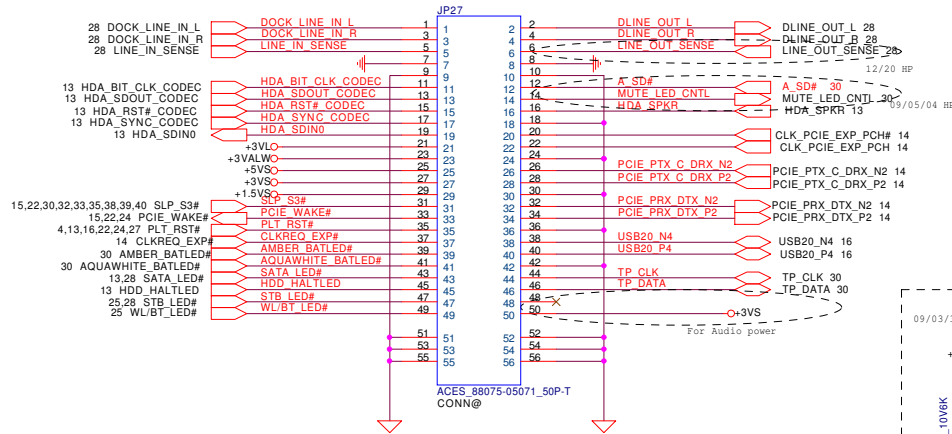
DOCKING CONNECTOR

blue.vn

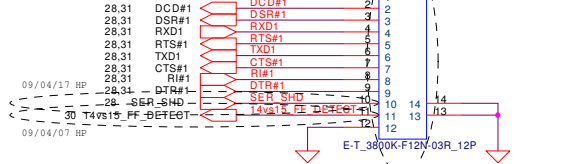


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H	OFF	ON

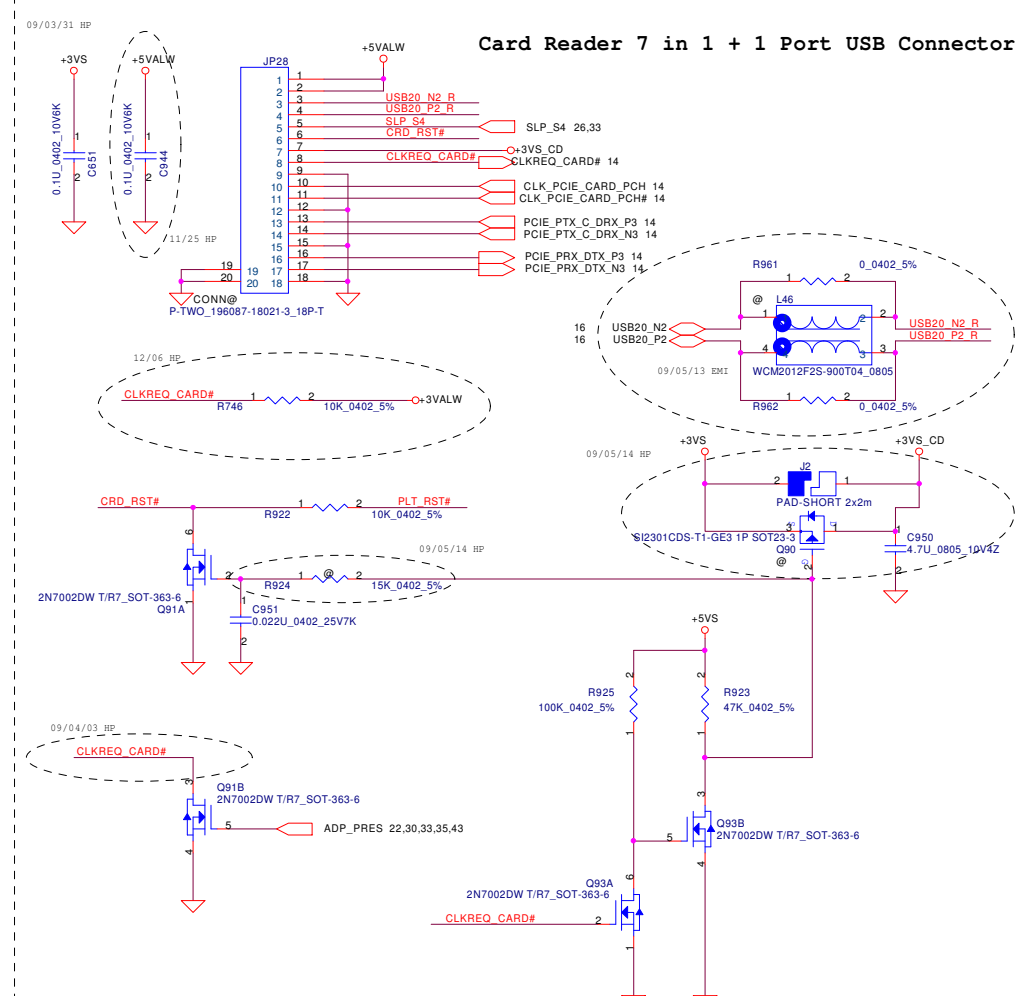
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Issued Date	2008/10/31	Deciphered Date	2009/11/06	Title		
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Serial Port CONN



Card Reader 7 in 1 + 1 Port USB Connector



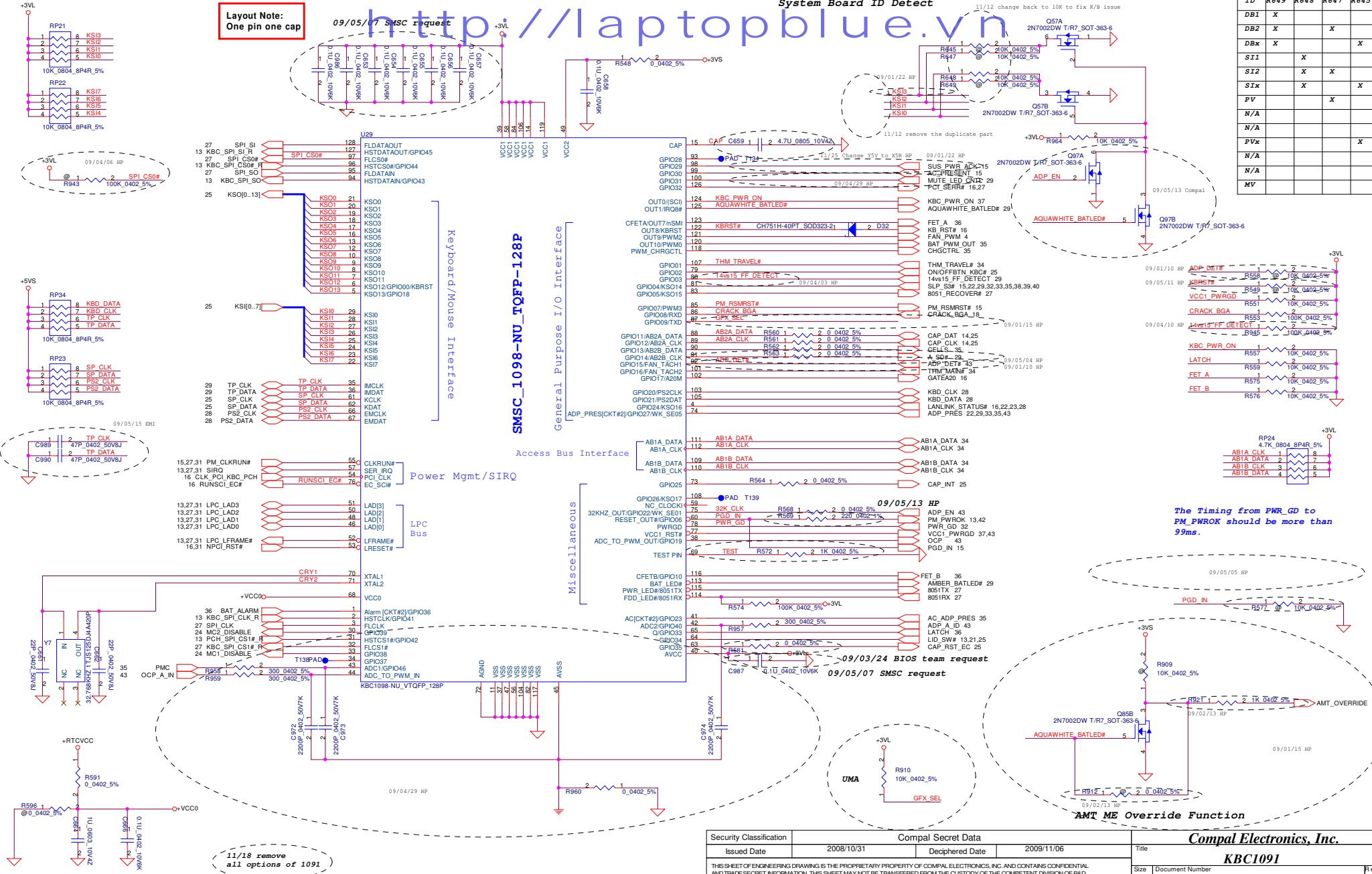
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Issued Date	2008/10/31	Deciphered Date	2009/11/06	Title	CR&LEDS&PW&Audio&Exp Conn
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Layout Note:
One pin one cap

09/05/07 SMC request

11/12 change back to 10K to fix K/B issue

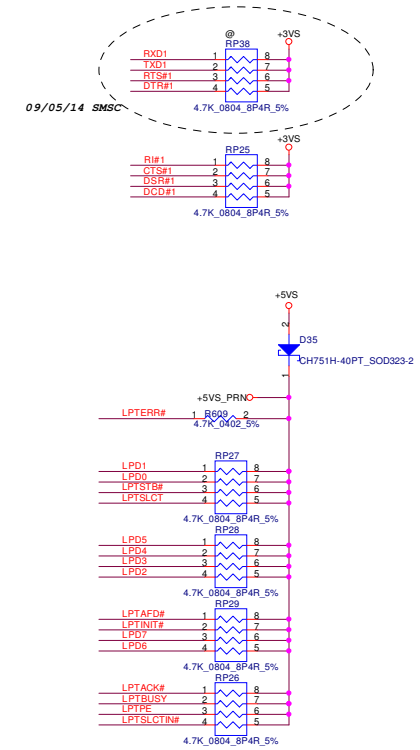
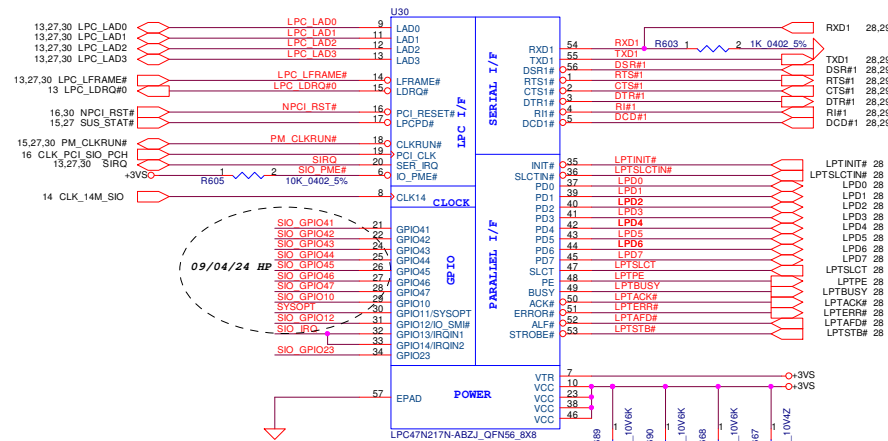
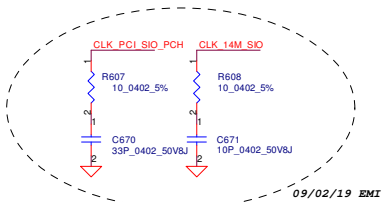
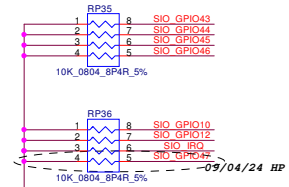
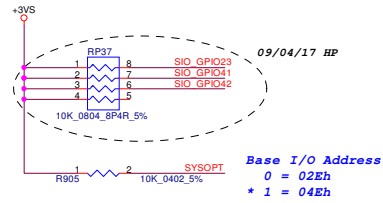
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DB1	X			
DB2			X	
DBx	X			X
SI1		X		
SI2			X	X
SIx		X		X
PV			X	
N/A				
N/A				
PVx				X
N/A				
N/A				
MV				



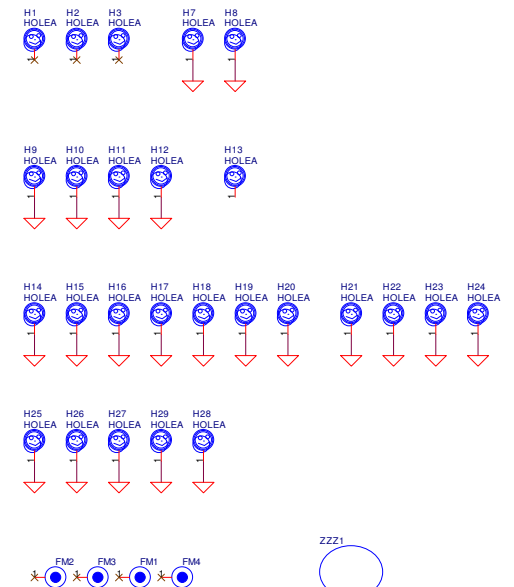
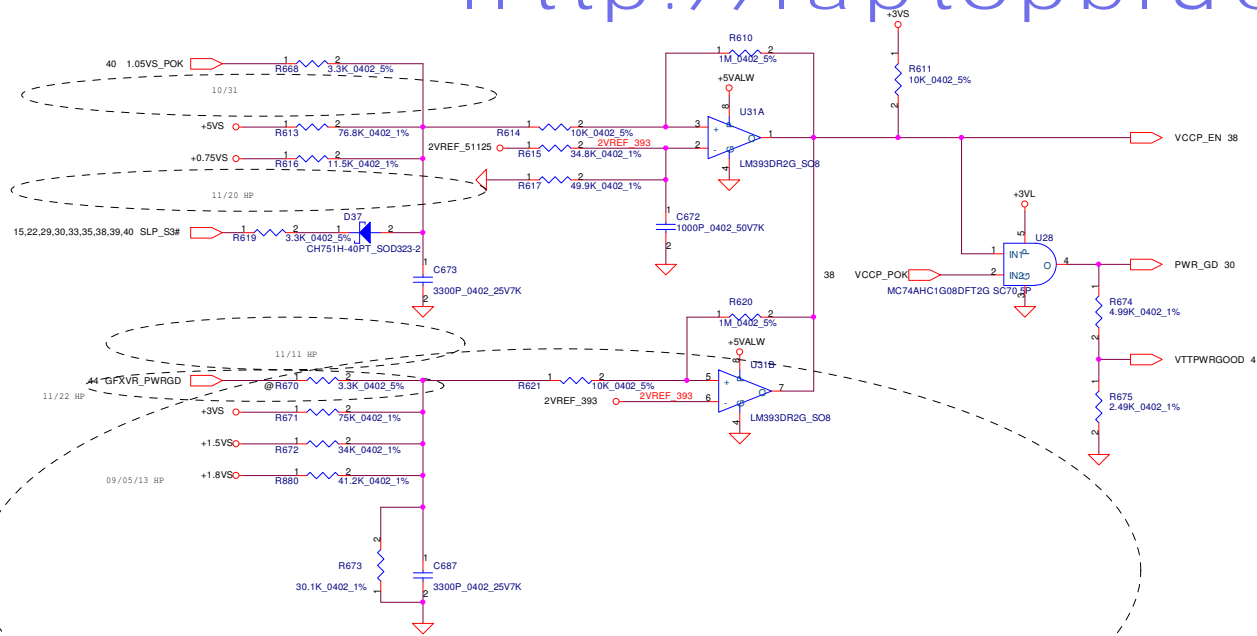
The Timing from PWR_GD to PM PWROK should be more than 99ms.

AMT ME Override Function

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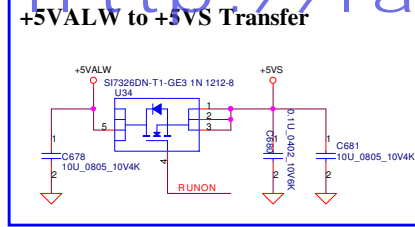


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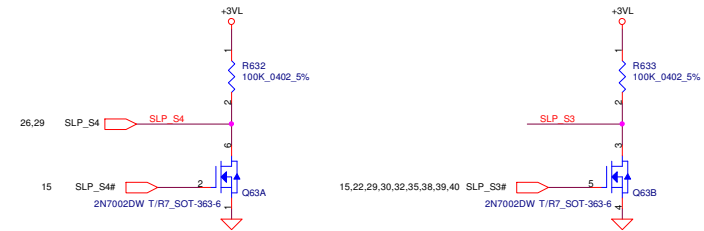
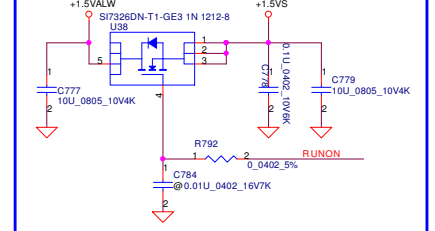


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+5VALW to +5VS Transfer



+1.5VALW to +1.5VS Transfer

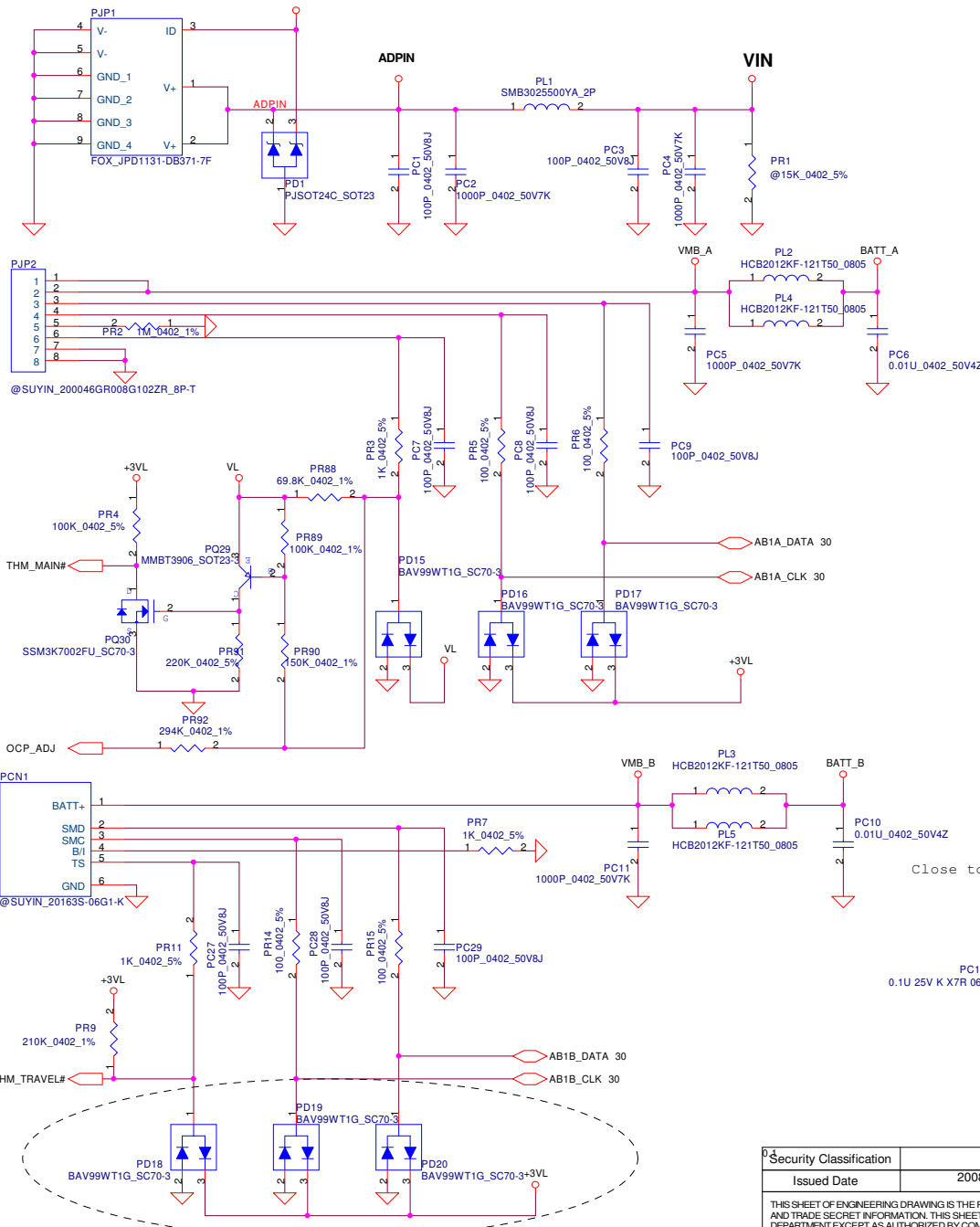


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ADP_SIGNAL

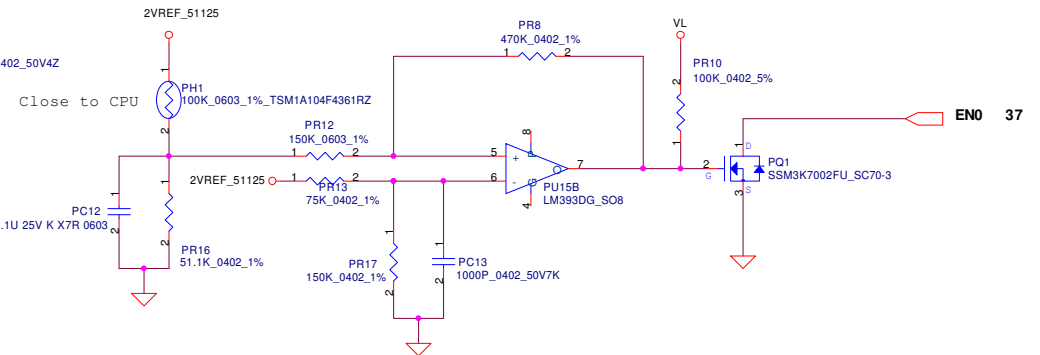
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VIN

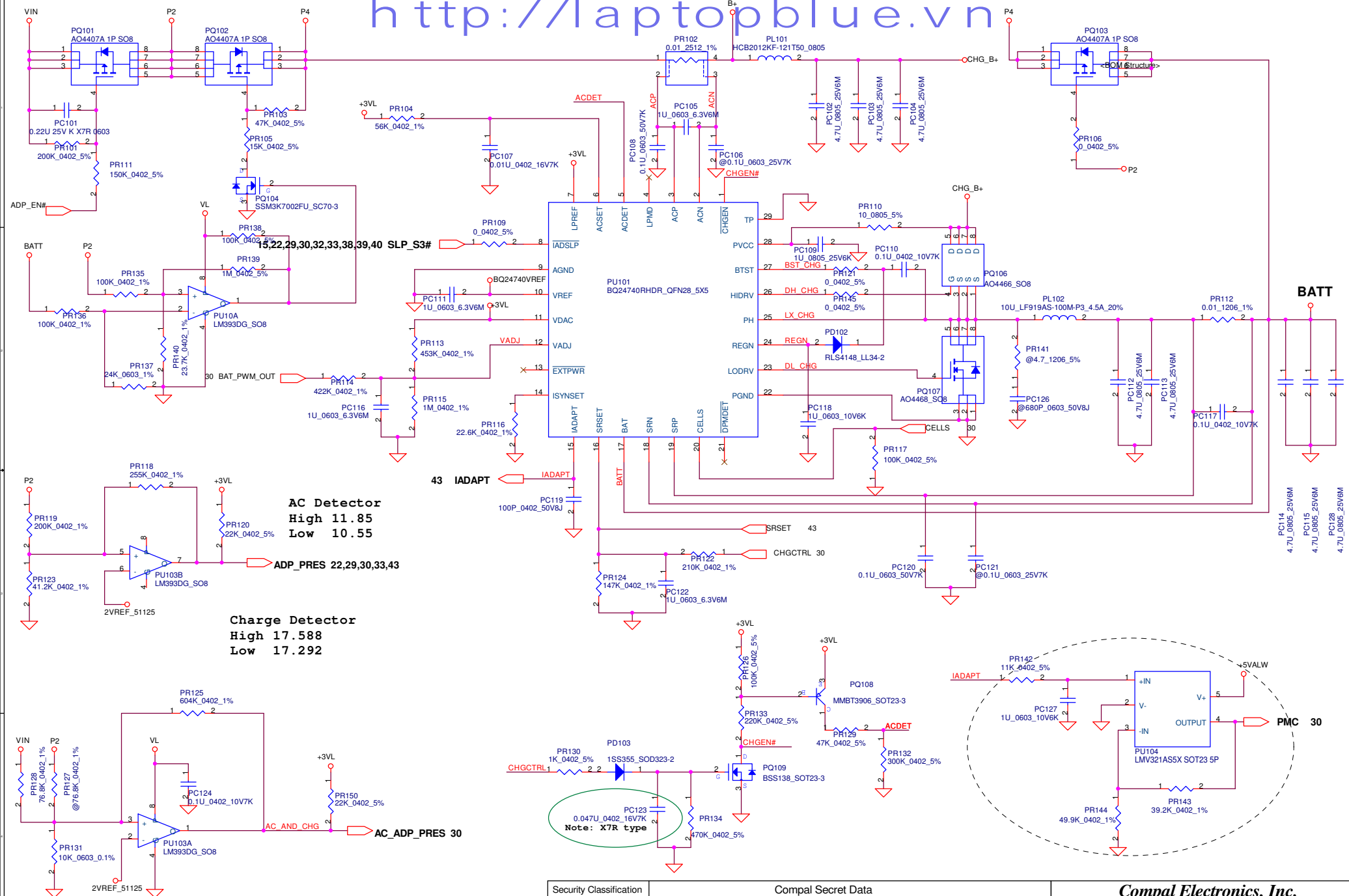


PH1 under CPU bottom side :

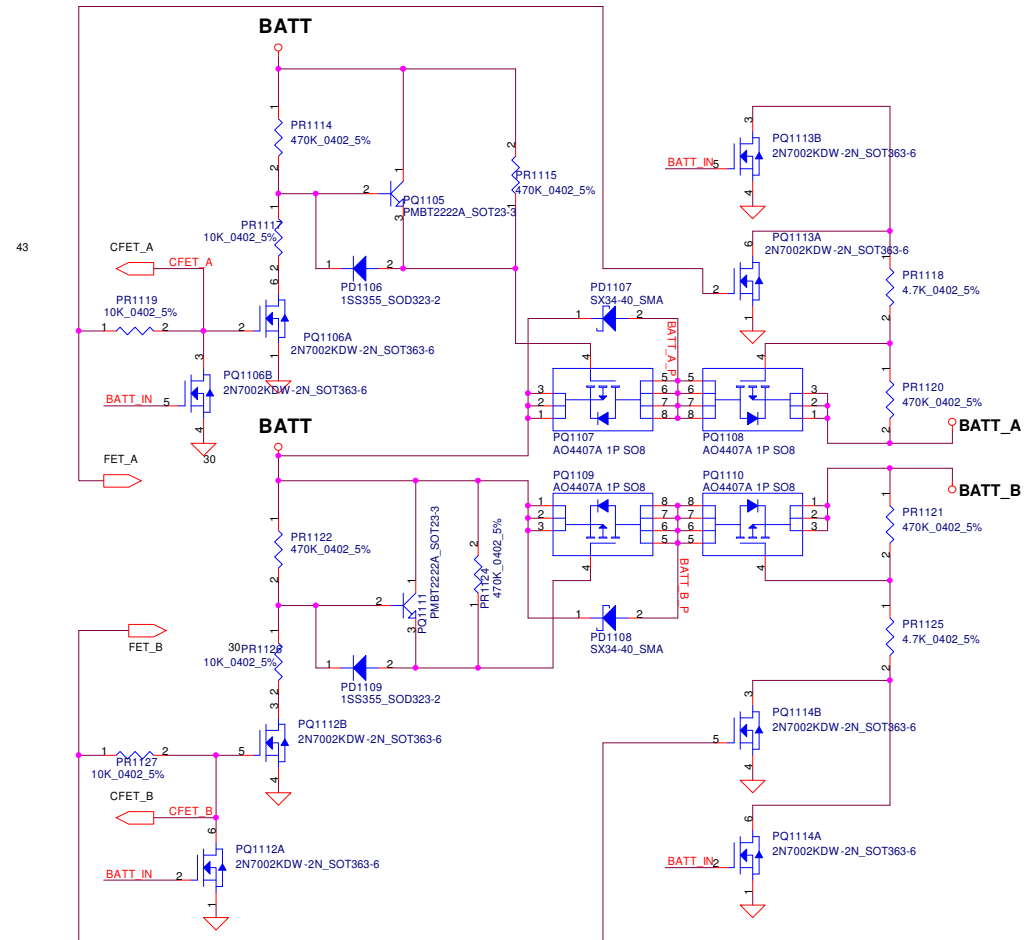
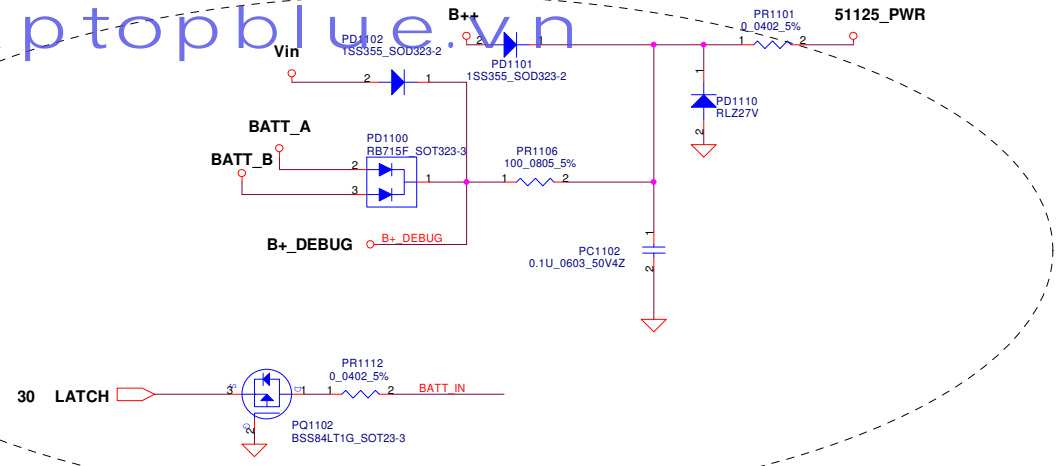
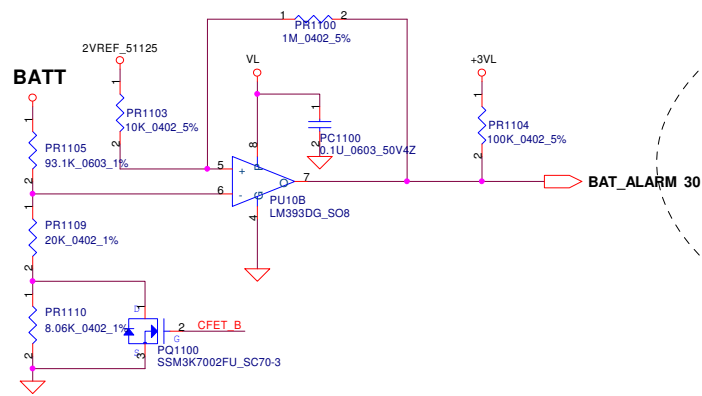
CPU thermal protection at 90 +-3 degree C
(Need to be checked)



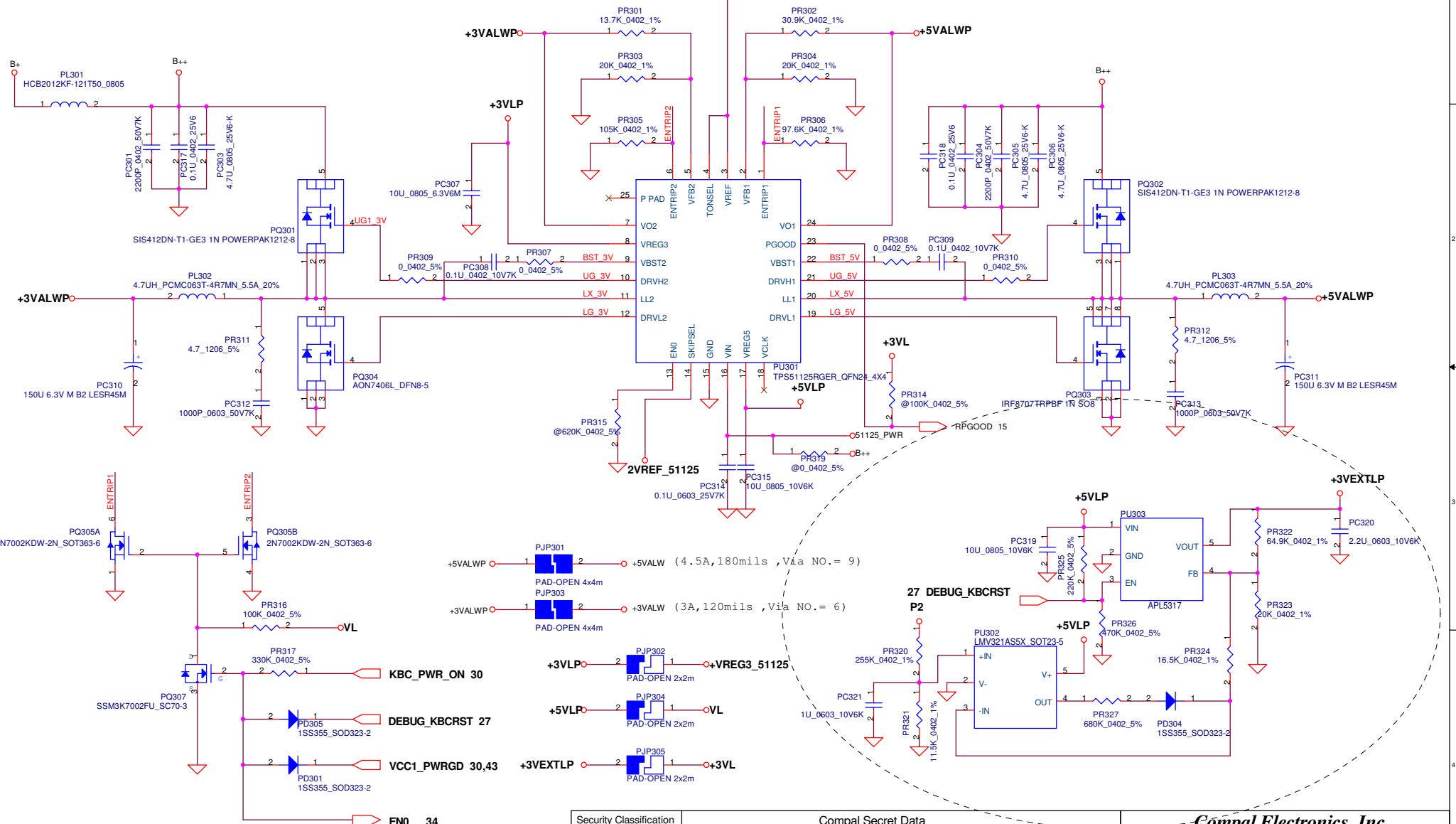
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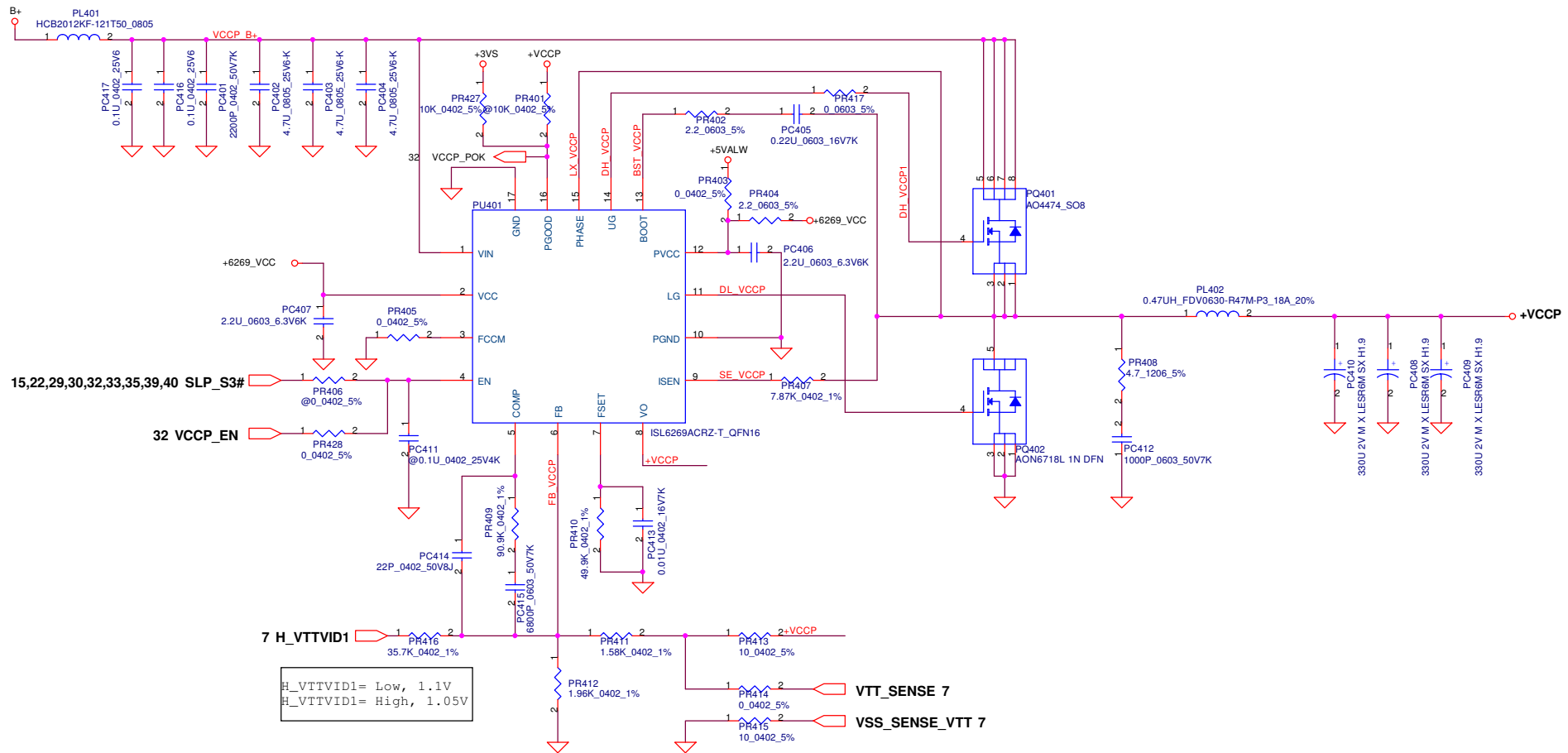
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				Sheet 36 of 45
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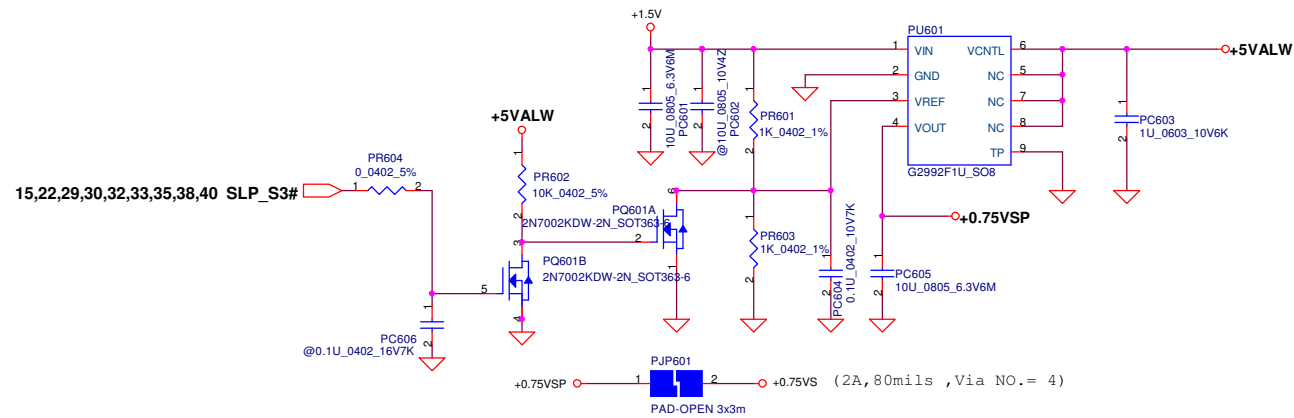


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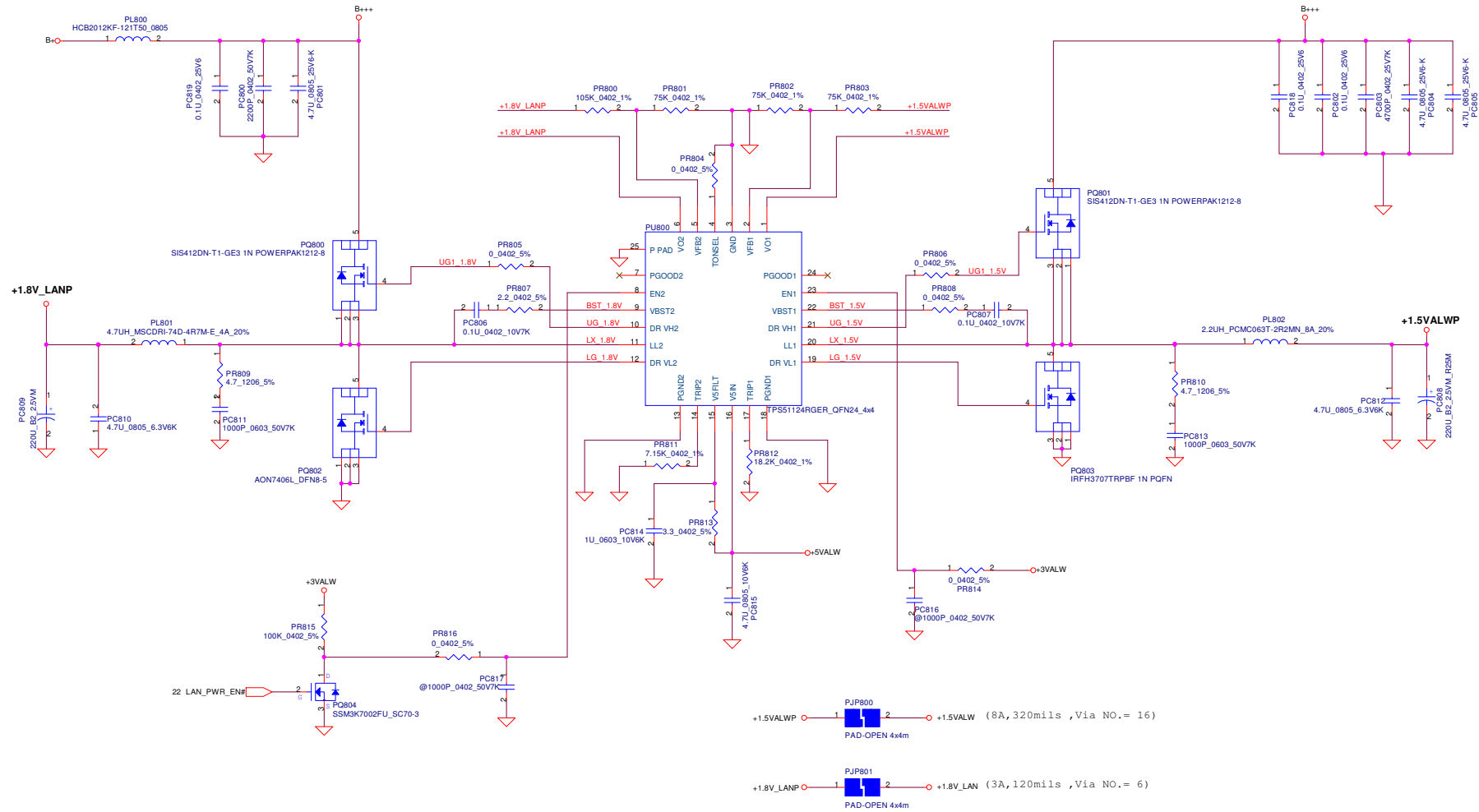
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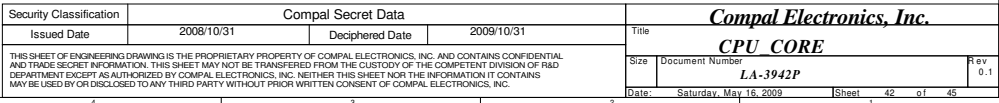


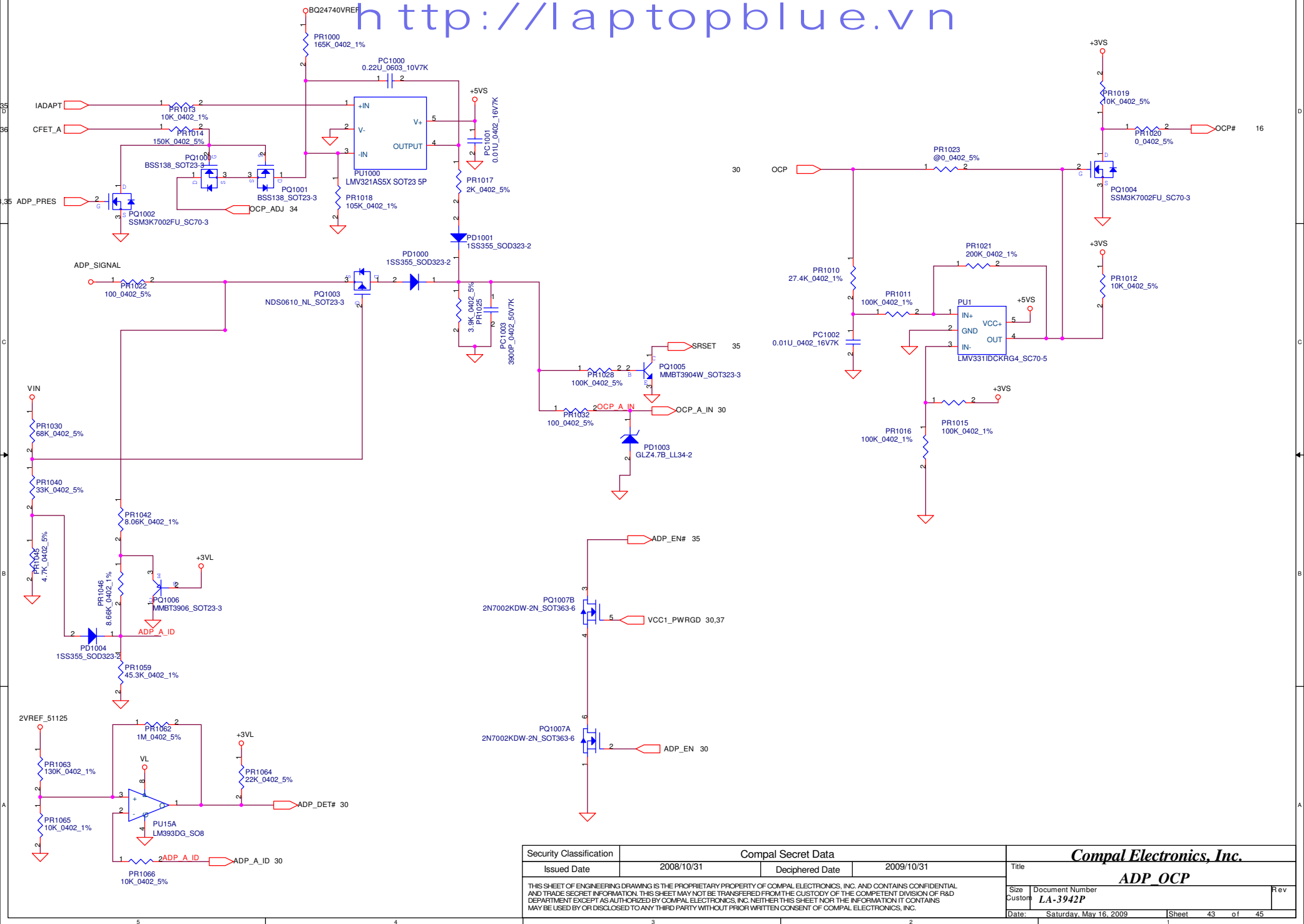
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