

Compal confidential

Schematics Document

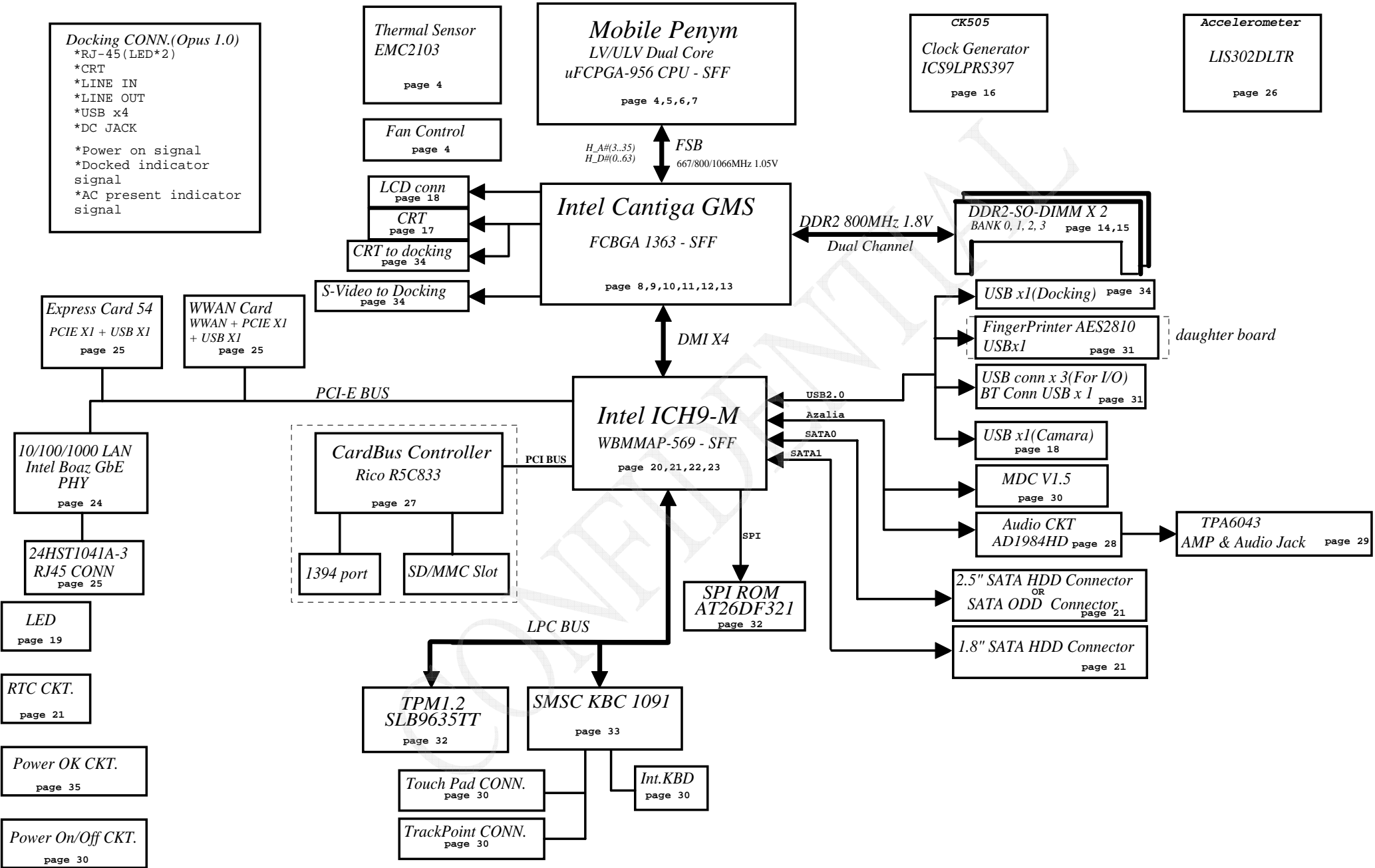
Mobile Penryn uFCPGA with Intel
Cantiga_GM+ICH9-M SFF core logic

SKYY

2008-07-29

機 密	等級	硬體二部
	產出人員	
	產出日期	
	解密日期	

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2006/02/13	Deciphered Date	2006/03/10	Title	
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Voltage Rails (O MEANS ON X MEANS OFF)

power plane State	+B	+5VALW +3VALW +3VM +1.05VM	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +0.9V
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build

CONN@ : means ME part.

45@ : means install after SMT.

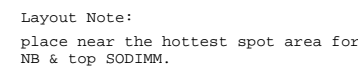
SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
CLOCK GENERATOR (EXT.)	D2	11010010

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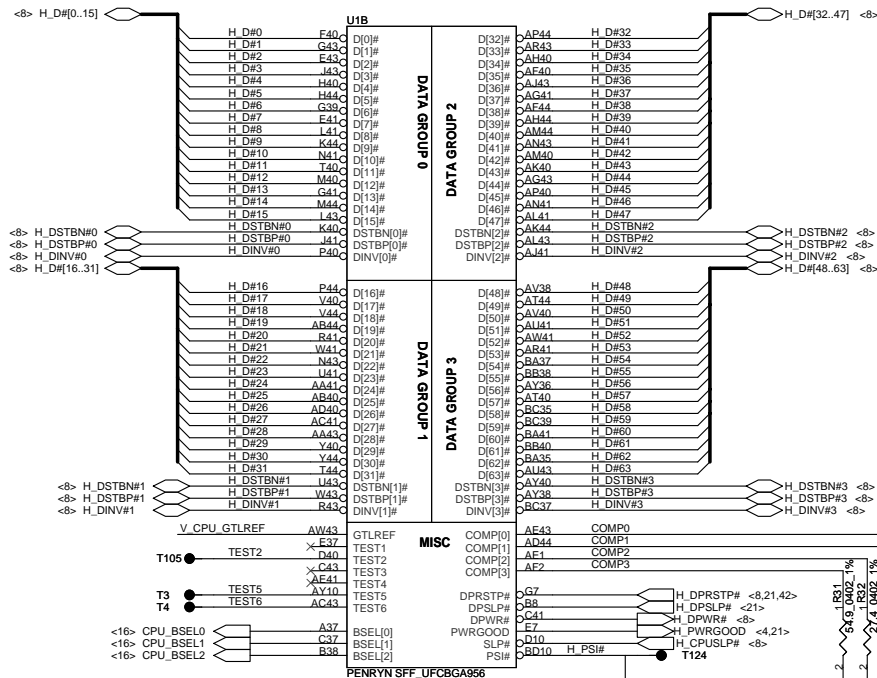


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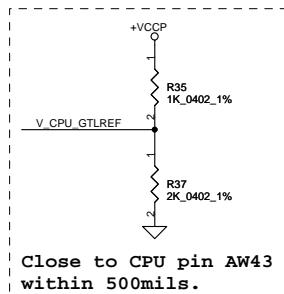
Date: Wednesday, June 03, 2009 | Sheet 4 of 36



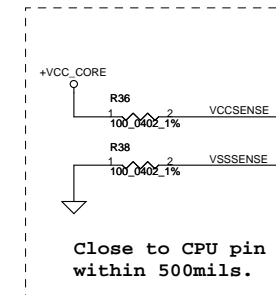
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

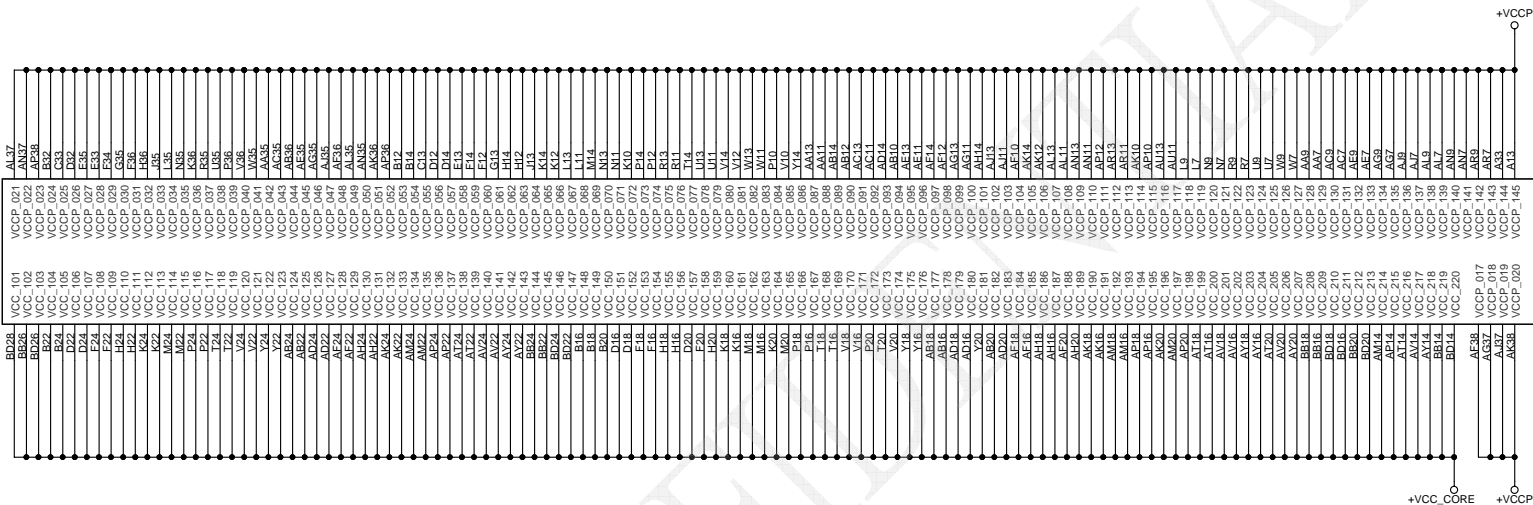
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



Length match within 25 mils. The trace width/space/other is 20/7/25.

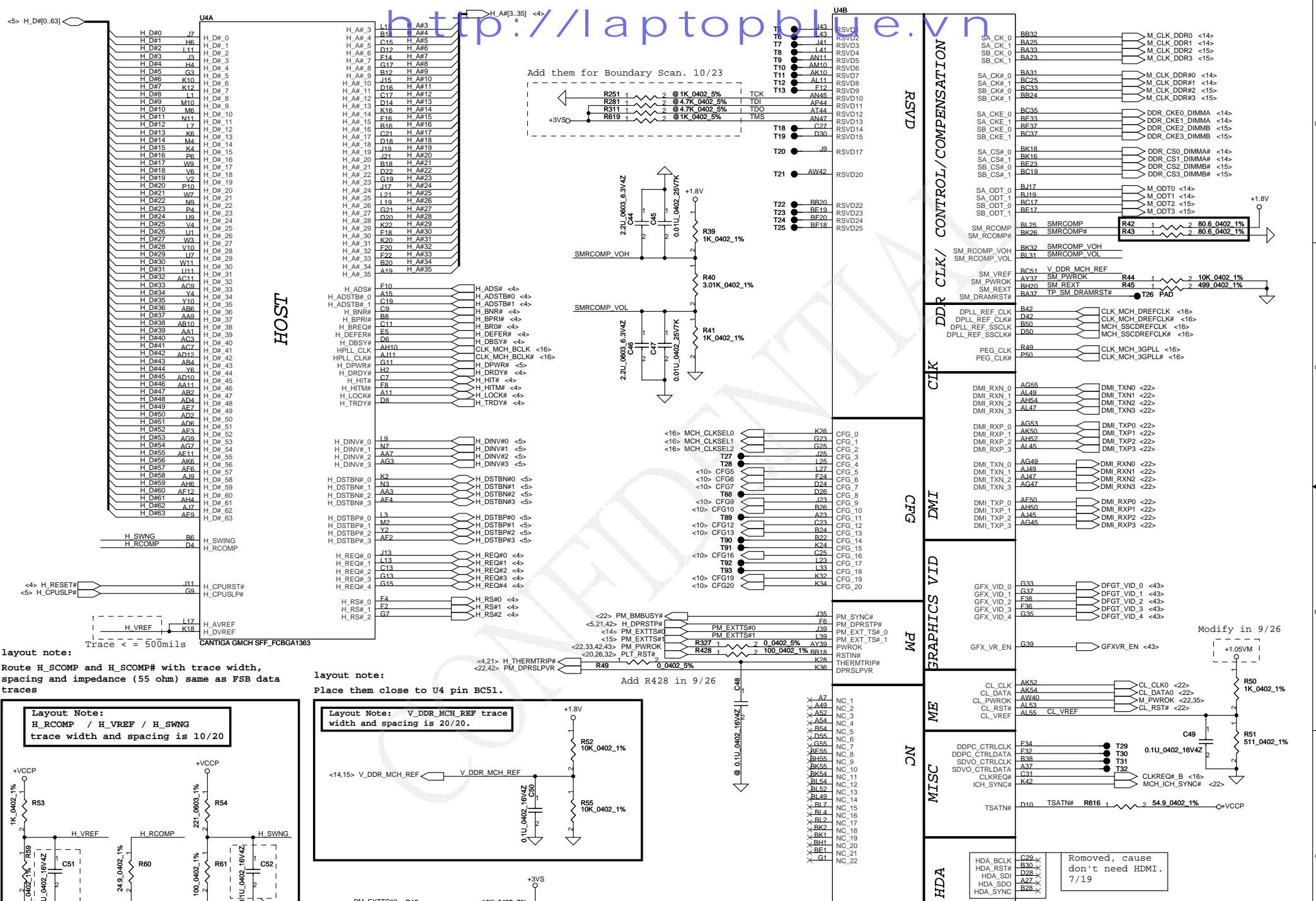




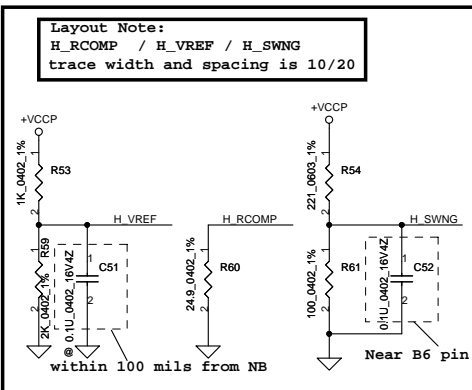
U1F
PENRYN SFF_UFCBGA956

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							Doc No	Document Number				Rev
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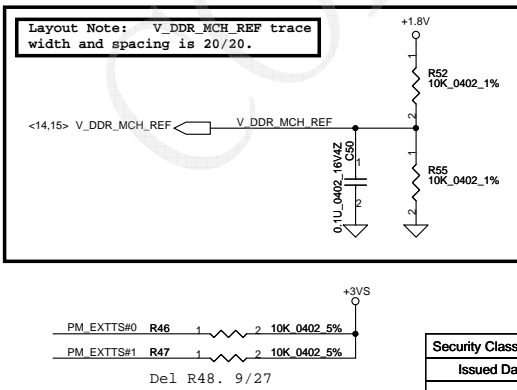
U1D			U1E		
B42	VSS[001]	VSS[082]	G25	VSS_164	VSS_280
F44	VSS[002]	VSS[083]	G21	VSS_165	VSS_281
D42	VSS[003]	VSS[084]	G23	VSS_166	VSS_282
F42	VSS[004]	VSS[085]	J25	VSS_167	VSS_283
H42	VSS[005]	VSS[086]	J23	VSS_168	VSS_284
K42	VSS[006]	VSS[087]	J21	VSS_169	VSS_285
M42	VSS[007]	VSS[088]	L26	VSS_170	VSS_286
P42	VSS[008]	VSS[089]	L23	VSS_171	VSS_287
T42	VSS[009]	VSS[090]	L21	VSS_172	VSS_288
V42	VSS[010]	VSS[091]	N25	VSS_173	VSS_289
Y42	VSS[011]	VSS[092]	N23	VSS_174	VSS_290
AB42	VSS[012]	VSS[093]	N21	VSS_175	VSS_291
AD42	VSS[013]	VSS[094]	R25	VSS_176	VSS_292
AF42	VSS[014]	VSS[095]	R23	VSS_177	VSS_293
AH42	VSS[015]	VSS[096]	R21	VSS_178	VSS_294
AK42	VSS[016]	VSS[097]	U25	VSS_179	VSS_295
AM42	VSS[017]	VSS[098]	U23	VSS_180	VSS_296
AP42	VSS[018]	VSS[099]	U21	VSS_181	VSS_297
AY44	VSS[019]	VSS[100]	W25	VSS_182	VSS_298
AV44	VSS[020]	VSS[101]	W23	VSS_183	VSS_299
AT42	VSS[021]	VSS[102]	W21	VSS_184	VSS_300
AA42	VSS[022]	VSS[103]	AA25	VSS_185	VSS_301
AA42	VSS[023]	VSS[104]	AA23	VSS_186	VSS_302
BA43	VSS[024]	VSS[105]	AA21	VSS_187	VSS_303
BB42	VSS[025]	VSS[106]	AC25	VSS_188	VSS_304
C48	VSS[026]	VSS[107]	AC23	VSS_189	VSS_305
E38	VSS[027]	VSS[108]	AC21	VSS_190	VSS_306
G37	VSS[028]	VSS[109]	AE25	VSS_191	VSS_307
H38	VSS[029]	VSS[110]	AE23	VSS_192	VSS_308
J39	VSS[030]	VSS[111]	AE21	VSS_193	VSS_309
L39	VSS[031]	VSS[112]	AG25	VSS_194	VSS_310
M38	VSS[032]	VSS[113]	AG23	VSS_195	VSS_311
N39	VSS[033]	VSS[114]	AG21	VSS_196	VSS_312
R39	VSS[034]	VSS[115]	IJ25	VSS_197	VSS_313
T38	VSS[035]	VSS[116]	IJ23	VSS_198	VSS_314
U39	VSS[036]	VSS[117]	IJ21	VSS_199	VSS_315
W39	VSS[037]	VSS[118]	AL25	VSS_200	VSS_316
Y38	VSS[038]	VSS[119]	AL23	VSS_201	VSS_317
AC39	VSS[039]	VSS[120]	AL21	VSS_202	VSS_318
AD38	VSS[040]	VSS[121]	AN25	VSS_203	VSS_319
AE39	VSS[041]	VSS[122]	AN23	VSS_204	VSS_320
AF39	VSS[042]	VSS[123]	AN21	VSS_205	VSS_321
AG39	VSS[043]	VSS[124]	AR25	VSS_206	VSS_322
AH38	VSS[044]	VSS[125]	AR23	VSS_207	VSS_323
AI39	VSS[045]	VSS[126]	AR21	VSS_208	VSS_324
AL39	VSS[046]	VSS[127]	AU25	VSS_209	VSS_325
AM38	VSS[047]	VSS[128]	AU23	VSS_210	VSS_326
AN39	VSS[048]	VSS[129]	AU21	VSS_211	VSS_327
AR39	VSS[049]	VSS[130]	AW25	VSS_212	VSS_328
AS37	VSS[050]	VSS[131]	AW23	VSS_213	VSS_329
AT38	VSS[051]	VSS[132]	AW21	VSS_214	VSS_330
AV39	VSS[052]	VSS[133]	BA25	VSS_215	VSS_331
AW39	VSS[053]	VSS[134]	BA23	VSS_216	VSS_332
AX39	VSS[054]	VSS[135]	BA21	VSS_217	VSS_333
AY37	VSS[055]	VSS[136]	BC25	VSS_218	VSS_334
BA39	VSS[056]	VSS[137]	BC23	VSS_219	VSS_335
BC41	VSS[057]	VSS[138]	BC21	VSS_220	VSS_336
BD40	VSS[058]	VSS[139]	C17	VSS_221	VSS_337
BD38	VSS[059]	VSS[140]	C19	VSS_222	VSS_338
B36	VSS[060]	VSS[141]	F17	VSS_223	VSS_339
D36	VSS[061]	VSS[142]	F19	VSS_224	VSS_340
H34	VSS[062]	VSS[143]	G17	VSS_225	VSS_341
K34	VSS[063]	VSS[144]	G19	VSS_226	VSS_342
M34	VSS[064]	VSS[145]	J19	VSS_227	VSS_343
M36	VSS[065]	VSS[146]	J17	VSS_228	VSS_344
P34	VSS[066]	VSS[147]	L19	VSS_229	VSS_345
T34	VSS[067]	VSS[148]	L17	VSS_230	VSS_346
V34	VSS[068]	VSS[149]	N19	VSS_231	VSS_347
Y34	VSS[069]	VSS[150]	N17	VSS_232	VSS_348
AB34	VSS[070]	VSS[151]	R19	VSS_233	VSS_349
AD34	VSS[071]	VSS[152]	R17	VSS_234	VSS_350
AE34	VSS[072]	VSS[153]	BA27	VSS_235	VSS_351
AF34	VSS[073]	VSS[154]	BA29	VSS_236	VSS_352
AG34	VSS[074]	VSS[155]	BA27	VSS_237	VSS_353
AH34	VSS[075]	VSS[156]	BC27	VSS_238	VSS_354
AI34	VSS[076]	VSS[157]	BC29	VSS_239	VSS_355
AK34	VSS[077]	VSS[158]	BA31	VSS_240	VSS_356
AM34	VSS[078]	VSS[159]	CA19	VSS_241	VSS_357
AN34	VSS[079]	VSS[160]	CA17	VSS_242	VSS_358
AP34	VSS[080]	VSS[161]	C25	VSS_243	VSS_359
AR34	VSS[081]	VSS[162]	AE19	VSS_244	VSS_360
AS34	VSS[082]	VSS[163]	AE17	VSS_245	VSS_361
AT34	VSS[083]	VSS[164]	AG19	VSS_246	VSS_362
AV34	VSS[084]	VSS[165]	AG17	VSS_247	VSS_363
AW34	VSS[085]	VSS[166]	AH19	VSS_248	VSS_364
AX34	VSS[086]	VSS[167]	AH17	VSS_249	VSS_365
AY34	VSS[087]	VSS[168]	AI19	VSS_250	VSS_366
BA34	VSS[088]	VSS[169]	AI17	VSS_251	VSS_367
BB34	VSS[089]	VSS[170]	AN19	VSS_252	VSS_368
BC34	VSS[090]	VSS[171]	AN17	VSS_253	VSS_369
BD34	VSS[091]	VSS[172]	AR19	VSS_254	VSS_370
BE34	VSS[092]	VSS[173]	AR17	VSS_255	VSS_371
BF34	VSS[093]	VSS[174]	AU19	VSS_256	VSS_372
BG34	VSS[094]	VSS[175]	AU17	VSS_257	VSS_373
BH34	VSS[095]	VSS[176]	AW19	VSS_258	VSS_374
BI34	VSS[096]	VSS[177]	AW17	VSS_259	VSS_375
BJ34	VSS[097]	VSS[178]	BA19	VSS_260	VSS_376
BK34	VSS[098]	VSS[179]	BA17	VSS_261	VSS_377
BL34	VSS[099]	VSS[180]	BC19	VSS_262	VSS_378
BM34	VSS[100]	VSS[181]	BC17	VSS_263	VSS_379
BN34	VSS[101]	VSS[182]	C11	VSS_264	VSS_380
BO34	VSS[102]	VSS[183]	C15	VSS_265	VSS_381
BP34	VSS[103]	VSS[184]	F15	VSS_266	VSS_382
BQ34	VSS[104]	VSS[185]	F17	VSS_267	VSS_383
BR34	VSS[105]	VSS[186]	G15	VSS_268	VSS_384
BS34	VSS[106]	VSS[187]	H15	VSS_269	VSS_385
BT34	VSS[107]	VSS[188]	H17	VSS_270	VSS_386
BU34	VSS[108]	VSS[189]	I15	VSS_271	VSS_387
BV34	VSS[109]	VSS[190]	I17	VSS_272	VSS_388
BW34	VSS[110]	VSS[191]	M15	VSS_273	VSS_389
BX34	VSS[111]	VSS[192]	M17	VSS_274	VSS_390
BY34	VSS[112]	VSS[193]	R15	VSS_275	VSS_391
BZ34	VSS[113]	VSS[194]	T15	VSS_276	VSS_392
CA34	VSS[114]	VSS[195]	T17	VSS_277	VSS_393
CB34	VSS[115]	VSS[196]	W15	VSS_278	VSS_394
CC34	VSS[116]	VSS[197]	W17	VSS_279	VSS_395
CD34	VSS[117]	VSS[198]	Y15	VSS_280	VSS_396
CE34	VSS[118]	VSS[199]	Y17	VSS_281	VSS_397
CF34	VSS[119]	VSS[200]	AD12	VSS_282	VSS_398
CG34	VSS[120]	VSS[201]			
CH34	VSS[121]	VSS[202]			
CI34	VSS[122]	VSS[203]			
CJ34	VSS[123]	VSS[204]			
CK34	VSS[124]	VSS[205]			
CL34	VSS[125]	VSS[206]			
CM34	VSS[126]	VSS[207]			
CN34	VSS[127]	VSS[208]			
CO34	VSS[128]	VSS[209]			
CP34	VSS[129]	VSS[210]			
CQ34	VSS[130]	VSS[211]			
CR34	VSS[131]	VSS[212]			
CS34	VSS[132]	VSS[213]			
CT34	VSS[133]	VSS[214]			
CU34	VSS[134]	VSS[215]			
CV34	VSS[135]	VSS[216]			
CW34	VSS[136]	VSS[217]			
CX34	VSS[137]	VSS[218]			
CY34	VSS[138]	VSS[219]			
CA34	VSS[139]	VSS[220]			
CB34	VSS[140]	VSS[221]			
CC34	VSS[141]	VSS[222]			
CD34	VSS[142]	VSS[223]			
CE34	VSS[143]	VSS[224]			
CF34	VSS[144]	VSS[225]			
CG34	VSS[145]	VSS[226]			
CH34	VSS[146]	VSS[227]			
CI34	VSS[147]	VSS[228]			
CJ34	VSS[148]	VSS[229]			
CK34	VSS[149]	VSS[230]			
CL34	VSS[150]	VSS[231]			
CM34	VSS[151]	VSS[232]			
CN34	VSS[152]	VSS[233]			
CO34	VSS[153]	VSS[234]			
CP34	VSS[154]	VSS[235]			
CQ34	VSS[155]	VSS[236]			
CR34	VSS[156]	VSS[237]			
CS34	VSS[157]	VSS[238]			
CT34	VSS[158]	VSS[239]			
CU34	VSS[159]	VSS[240]			
CV34	VSS[160]	VSS[241]			
CW34	VSS[161]	VSS[242]			
CX34	VSS[162]	VSS[243]			
CY34	VSS[163]	VSS[244]			
CA34	VSS[164]	VSS[245]			
CB34	VSS[165]	VSS[246]			
CC34	VSS[166]	VSS[247]			
CD34	VSS[167]	VSS[248]			
CE34	VSS[168]	VSS[249]			
CF34	VSS[169]	VSS[250]			
CG34	VSS[170]	VSS[251]			
CH34	VSS[171]	VSS[252]			
CI34	VSS[172]	VSS[253]			
CJ34	VSS[173]	VSS[254]			
CK34	VSS[174]	VSS[255]			
CL34	VSS[175]	VSS[256]			
CM34	VSS[176]	VSS[257]			
CN34	VSS[177]	VSS[258]			
CO34	VSS[178]	VSS[259]			
CP34	VSS[179]	VSS[260]			
CQ34	VSS[180]	VSS[261]			
CR34	VSS[181]	VSS[262]			
CS34	VSS[182]	VSS[263]			
CT34	VSS[183]	VSS[264]			
CU34	VSS[184]	VSS[265]			
CV34	VSS[185]	VSS[266]			
CW34	VSS[186]	VSS[267]			
CX34	VSS[187]	VSS[268]			
CY34	VSS[188]	VSS[269]			
CA34	VSS[189]	VSS[270]			
CB34	VSS[190]	VSS[271]			
CC34	VSS[191]	VSS[272]			
CD34	VSS[192]	VSS[273]			
CE34	VSS[193]	VSS[274]			
CF34	VSS[194]	VSS[275]			
CG34	VSS[195]	VSS[276]			
CH34	VSS[196]	VSS[277]			
CI34	VSS[197]	VSS[278]			
CJ34	VSS[198]	VSS[279]			
CK34	VSS[199]	VSS[280]			
CL34	VSS[200]	VSS[281]			
CM34	VSS[201]	VSS[282]			
CN34	VSS[202]	VSS[283]			
CO34	VSS[203]	VSS[284]			
CP34	VSS[204]	VSS[285]			
CQ34	VSS[205]	VSS[286]			
CR34	VSS[206]	VSS[287]			
CS34	VSS[207]	VSS[288]			
CT34	VSS[208]	VSS[289]			
CU34	VSS[209]	VSS[290]			
CV34	VSS[210]	VSS[291]			
CW34	VSS[211]	VSS[292]			
CX34	VSS[212]	VSS[293]			
CY34	VSS[213]	VSS[294]			
CA34	VSS[214]	VSS[295]			
CB34	VSS[215]	VSS[296]			
CC34	VSS[216]	VSS[297]			
CD34	VSS[217]	VSS[298]			
CE34	VSS[218]	VSS[299]			
CF34	VSS[219]	VSS[300]			
CG34	VSS[220]	VSS[301]			
CH34	VSS[221]	VSS[302]			
CI34	VSS[222]	VSS[303]			
CJ34	VSS[223]	VSS[304]			
CK34	VSS[224]	VSS[305]			
CL34	VSS[225]	VSS[306]			
CM34	VSS[226]	VSS[307]			
CN34	VSS[227]	VSS[308]			
CO34	VSS[228]	VSS[309]			
CP34	VSS[229]	VSS[310]			
CQ34	VSS[230]	VSS[311]			
CR34	VSS[231]	VSS[312]			
CS34	VSS[232]	VSS[313]			
CT34	VSS[233]	VSS[314]			
CU34	VSS[234]	VSS[315]			
CV34	VSS[235]	VSS[316]			
CW34	VSS[236]	VSS[317]			
CX34	VSS[237]	VSS[318]	</		

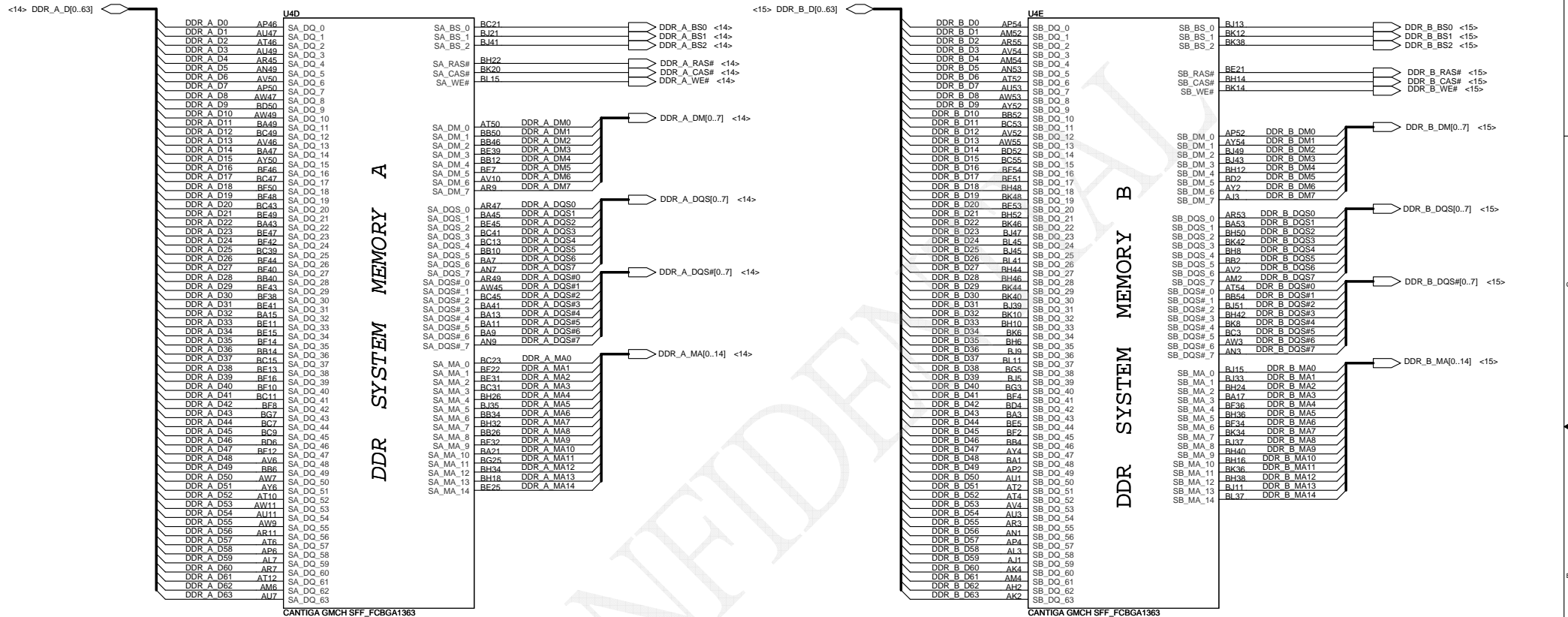


layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

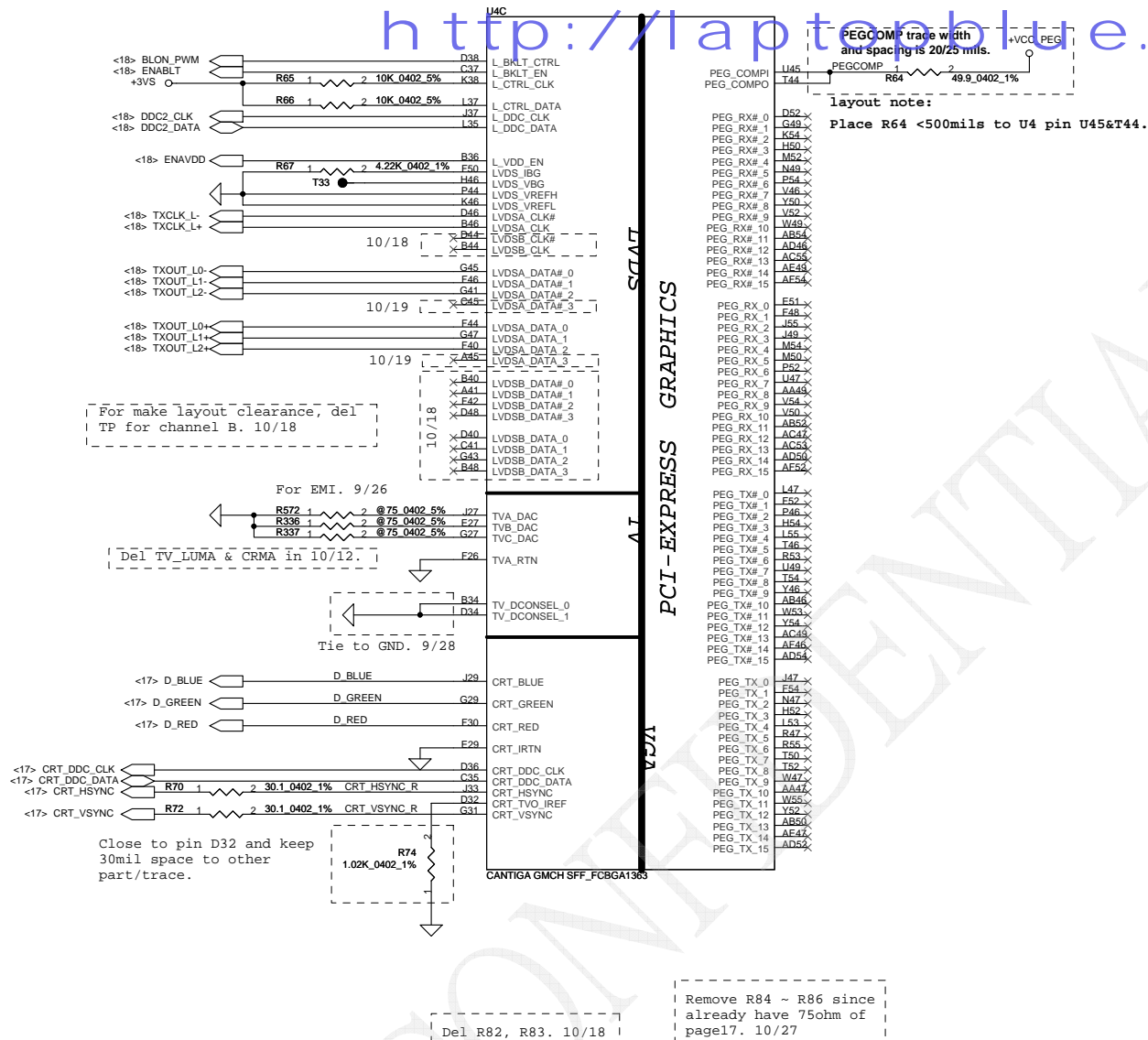


layout note:
Place them close to U4 pin BC51.

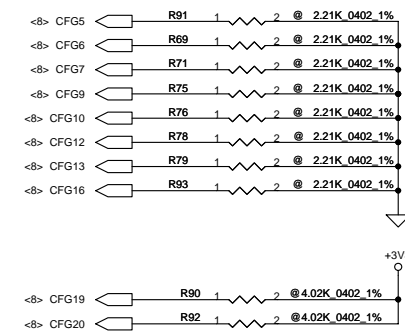


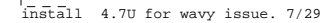


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Issued Date	2006/02/13	Deciphered Date	2006/03/10	Title	SCHEMATIC, M/B LA-4021P
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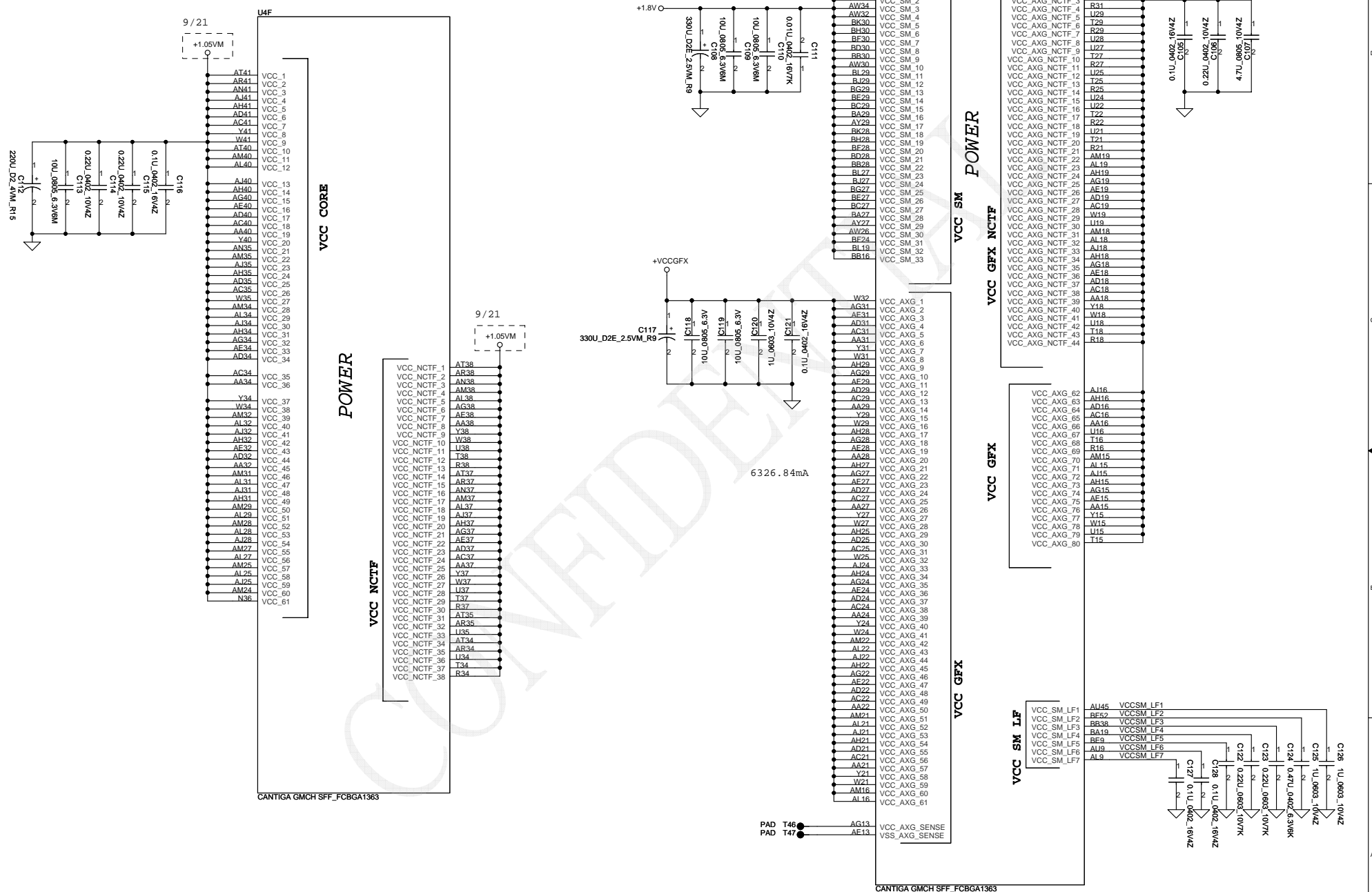
Setup File Table	
CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The ITPM Host Interface is enable 1 = The ITPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chipser suite with no confidentiality 1 =(TLS)chipser suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.





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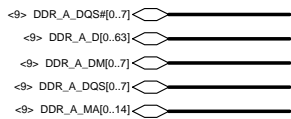
Extlnal Graphic: 1210.34mA
integrated Graphic: 1930.4mA



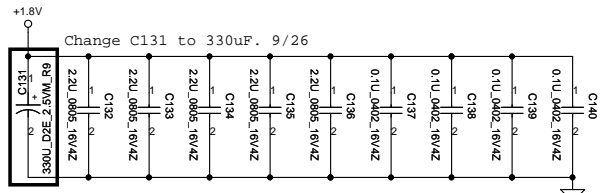
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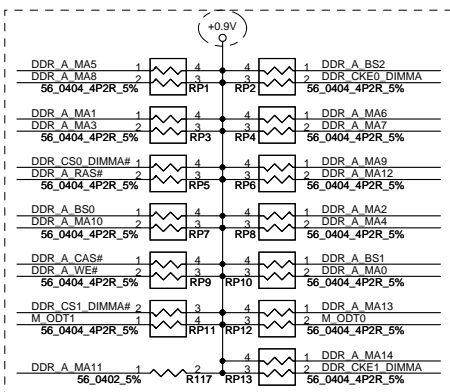
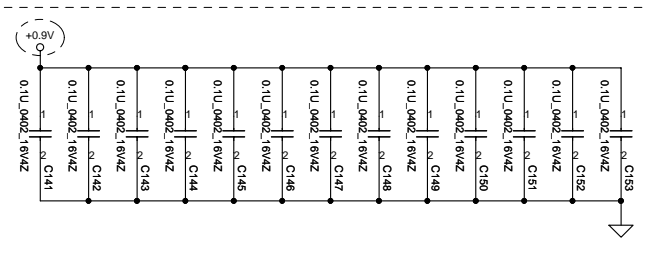
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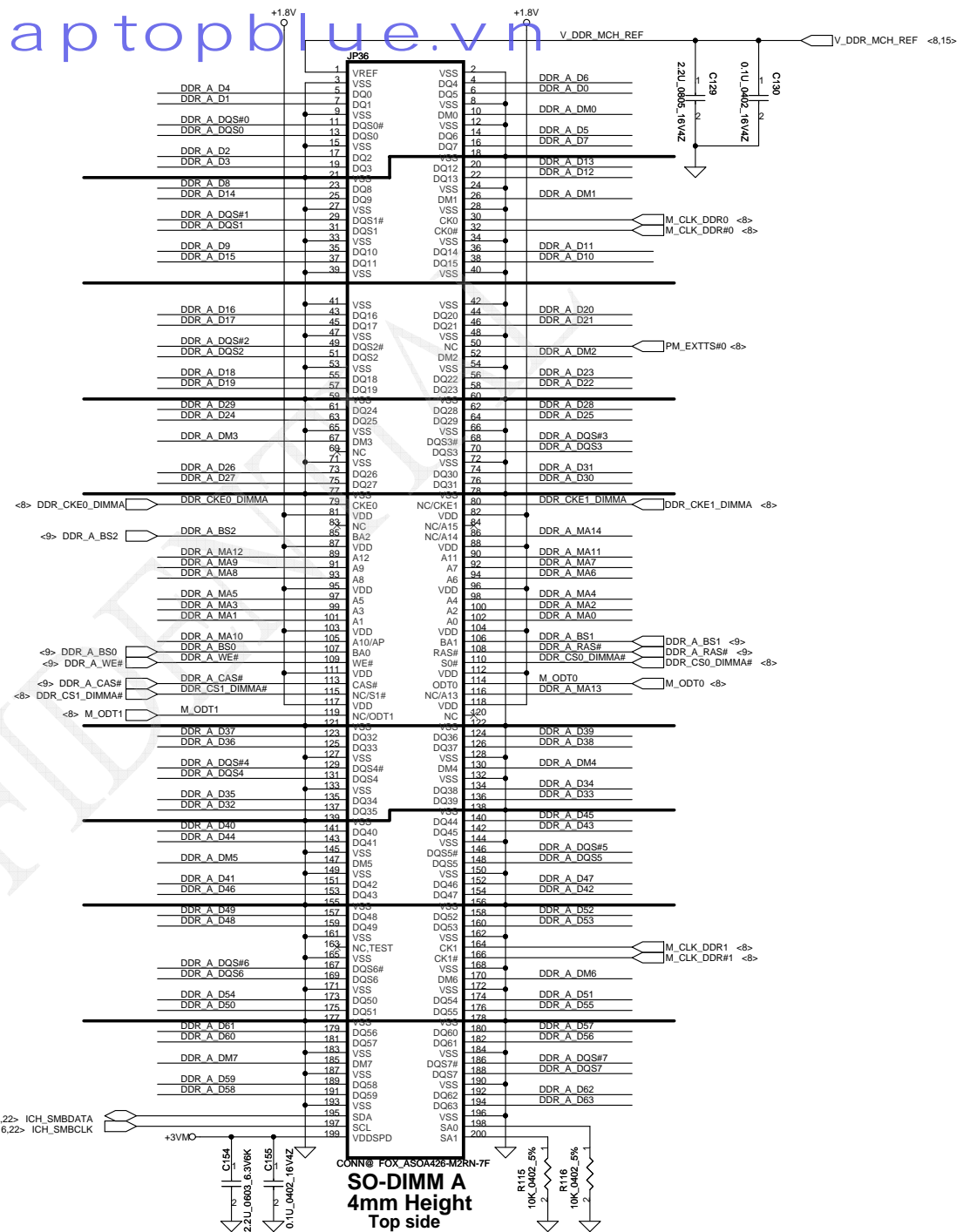
Layout Note:
Place near JP36



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V



Layout Note:
Place these resistor
closely JP9,all
trace length Max=1.5"

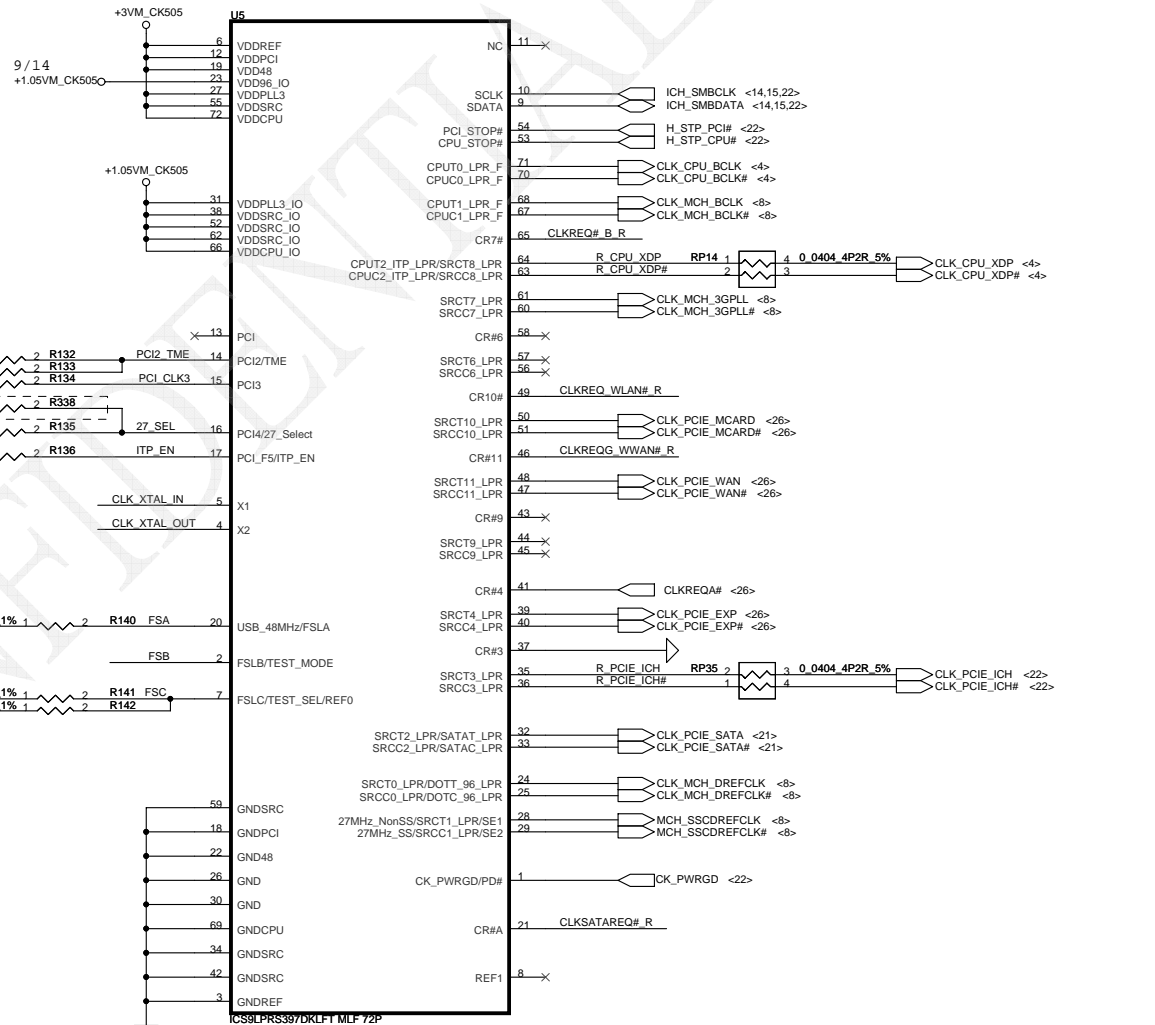
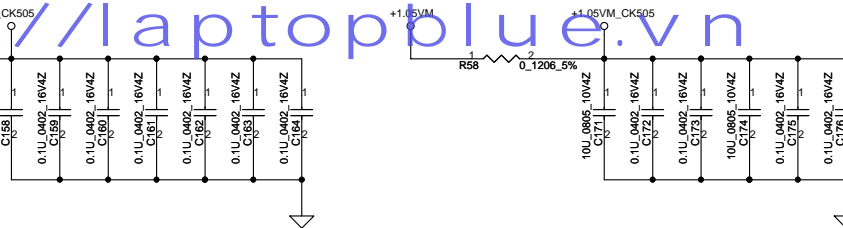
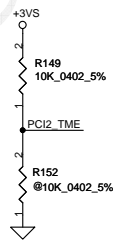
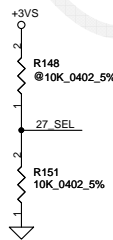
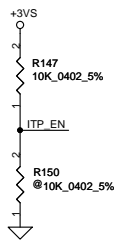
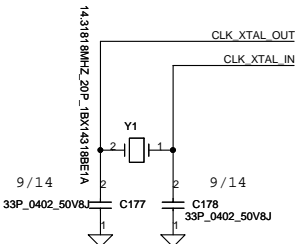
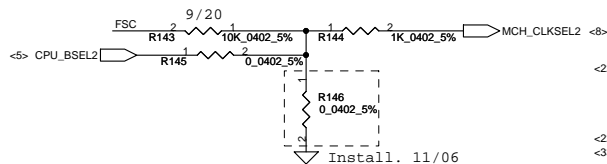
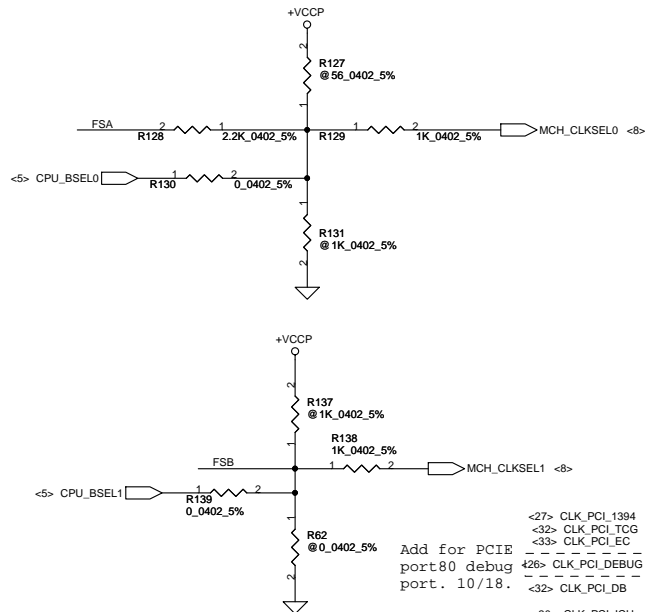


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FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	FSB MHz	SRC MHz	PCI MHz
0	0	0	266	1066	100	33.3
0	1	0	200	800	100	33.3
0	1	1	166	667	100	33.3

http://laptopblue.vn

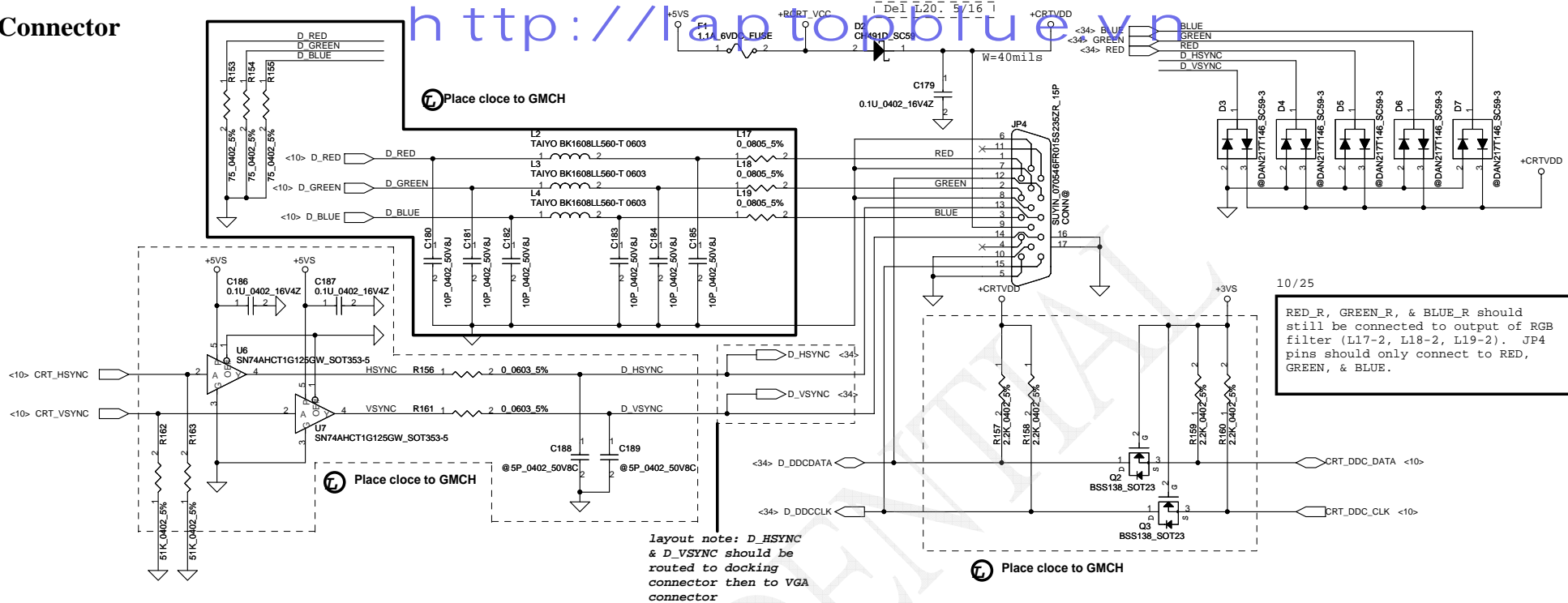


Component	Value	Part Number
C156	2	1 CLK 48M ICH @ 5P_0402_50V8C
C157	1	2 CLK 14M ICH 12P_0402_50V8J
C165	2	1 CLK PCI ICH @ 4.7P_0402_50V8C
C166	1	2 12P_0402_50V8J
C167	2	1 CLK PCI EC @ 4.7P_0402_50V8C
C168	2	1 CLK PCI TCG @ 4.7P_0402_50V8C
C169	2	1 CLK PCI 1394 @ 5P_0402_50V8C
C170	2	1 CLK PCI DB @ 5P_0402_50V8C

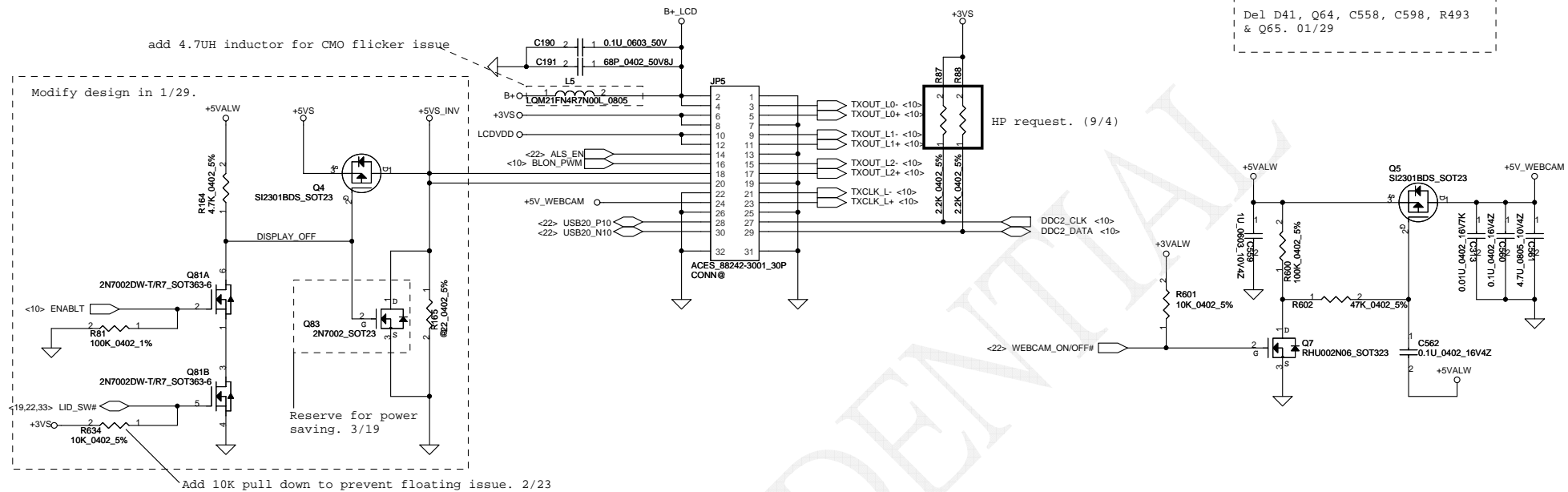
Place close to U5

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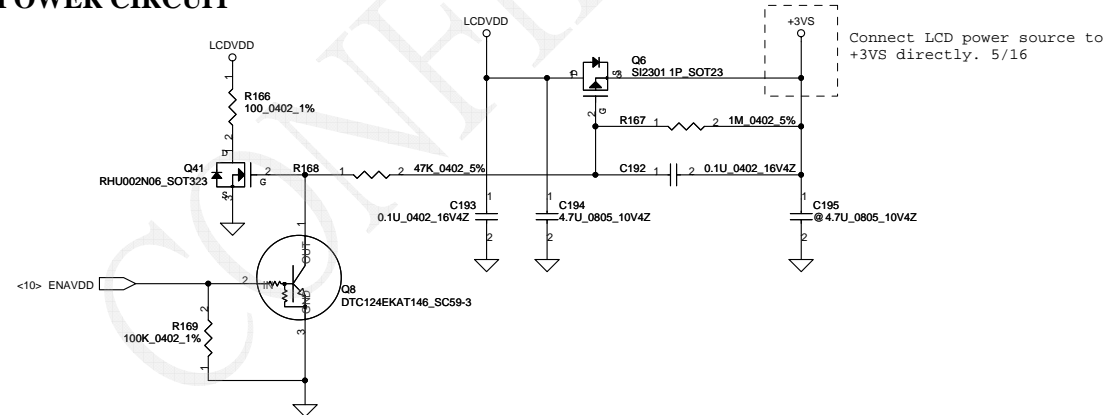
CRT Connector



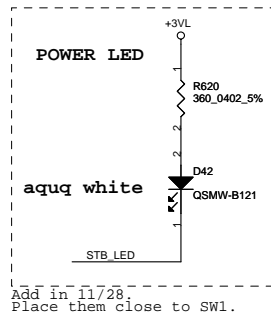
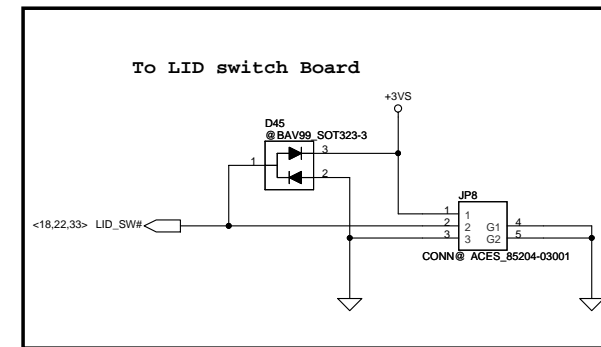
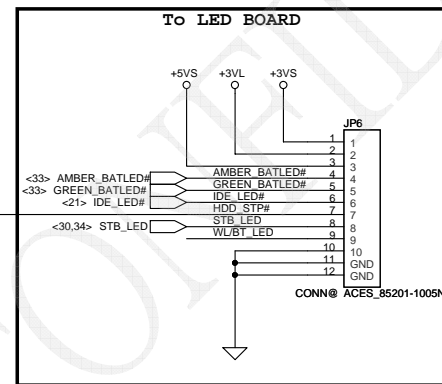
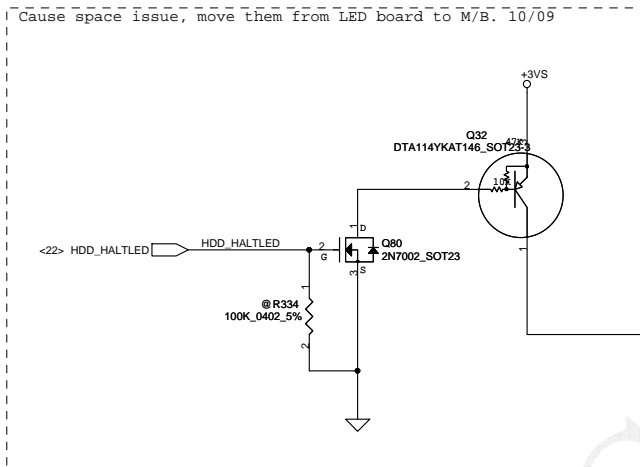
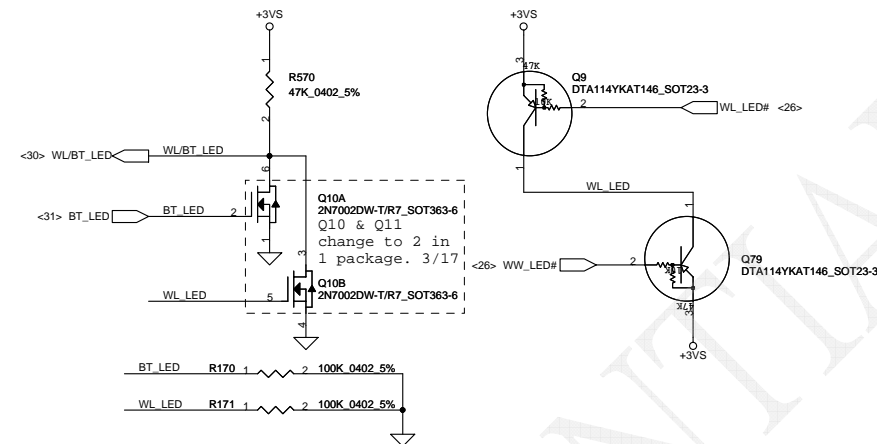
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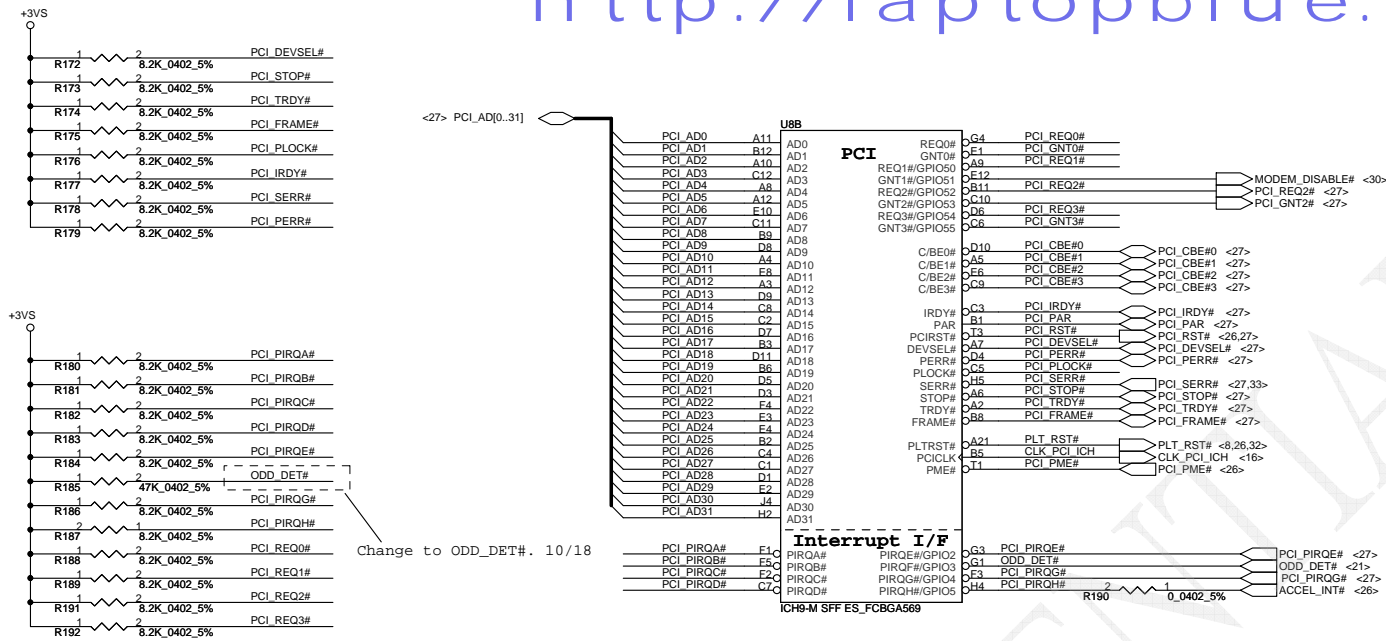
LCD/PANEL BD. CONN.

LCD POWER CIRCUIT

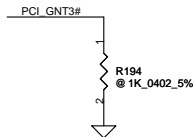


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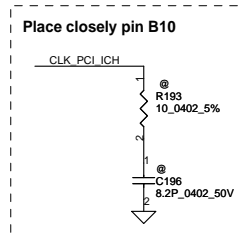
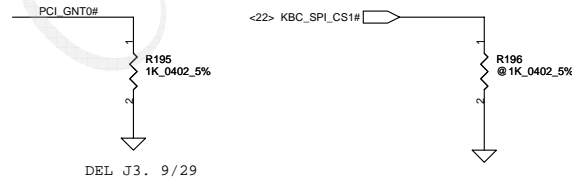


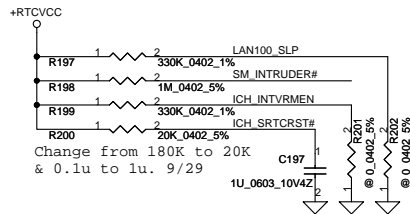


A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default *



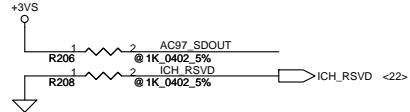
Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI *
1	0	PCI
1	1	LPC



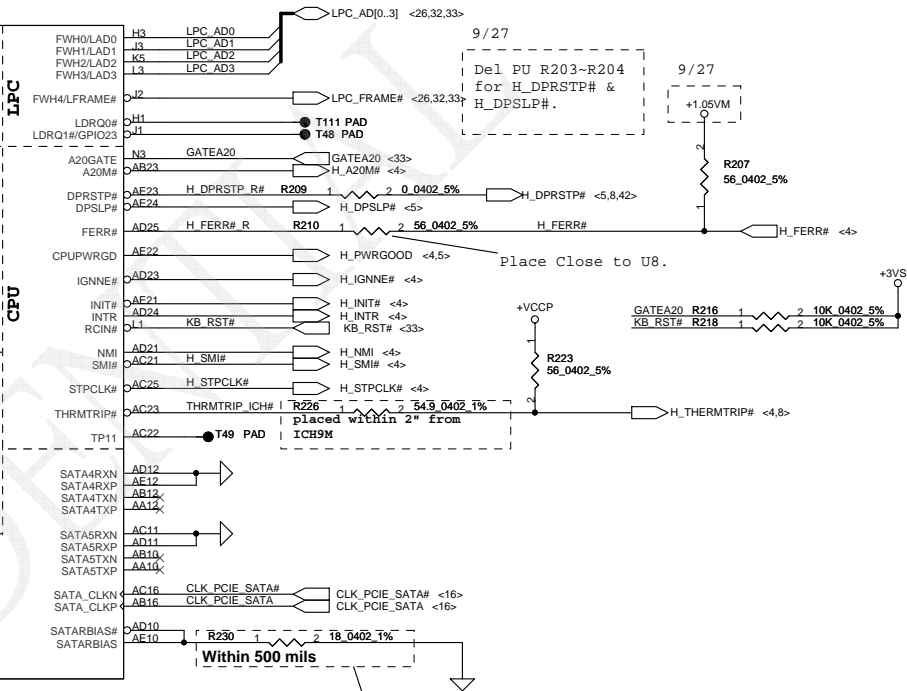
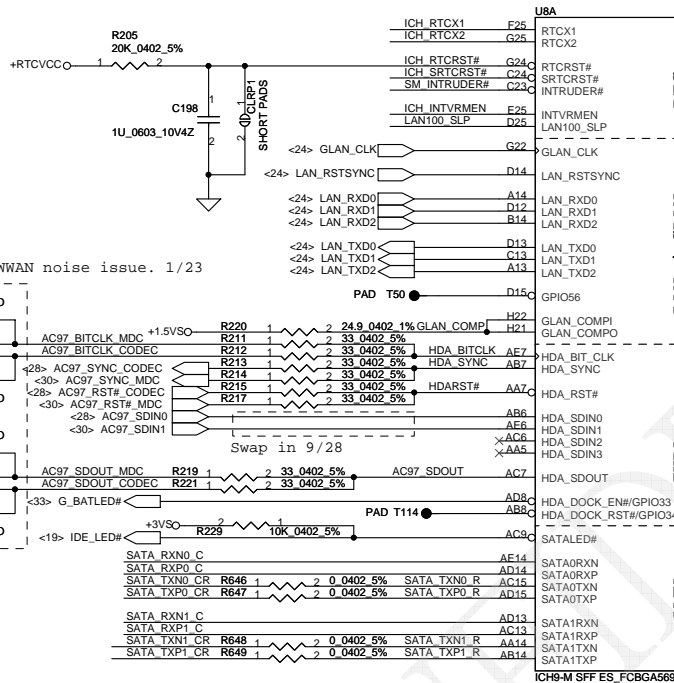
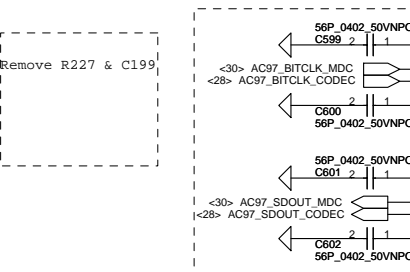


ICH_RSVD	HDA_SDOUT_CODECD	Description
0	0	RV
0	1	XOR
1	0	Normal (D
1	1	PCIE Bit.

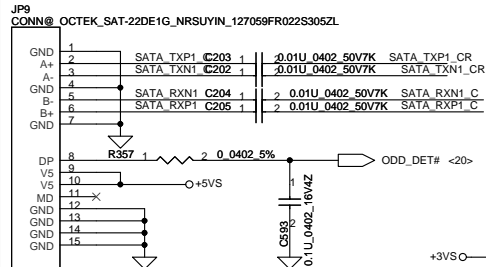
XOR CHAIN ENTRANCE STRAP:RSVD



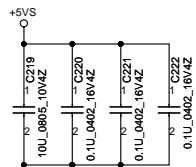
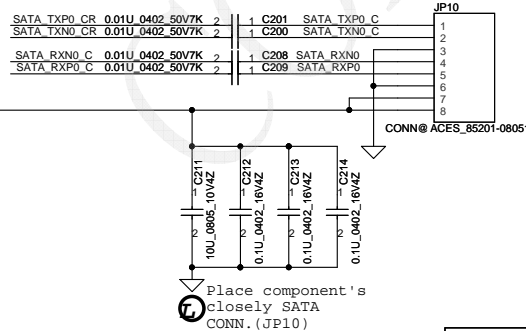
Add C599 ~ C602 to solve WWAN noise issue. 1/23



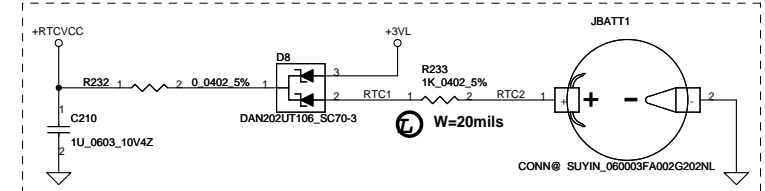
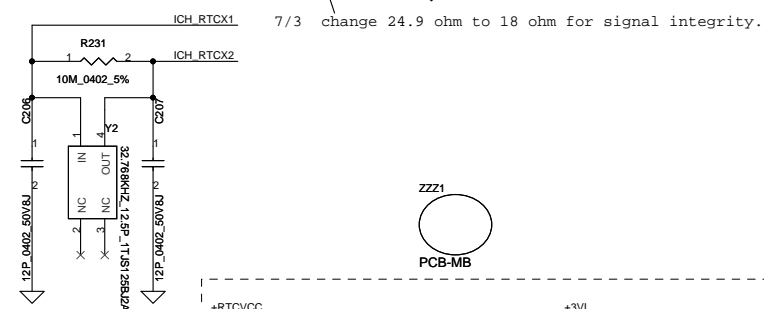
SATA CD-ROM Connector



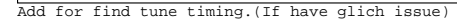
1.8" SATA HDD CONN



Place component's
closely SATA
CONN. (JP9)



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Reserve R254 at 9/19.

Add in 10/04.

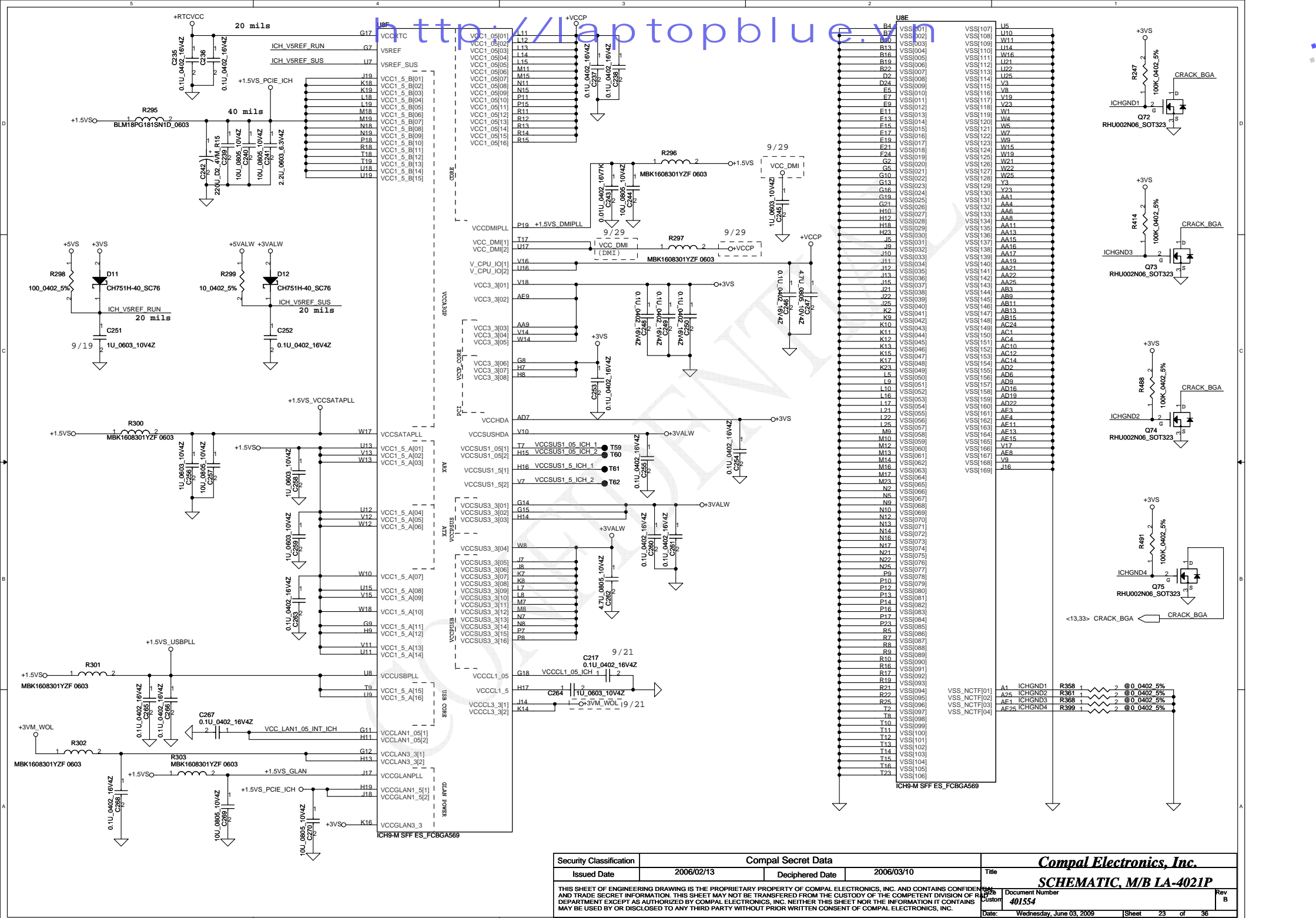
Within 500 mils

Place closely pin A

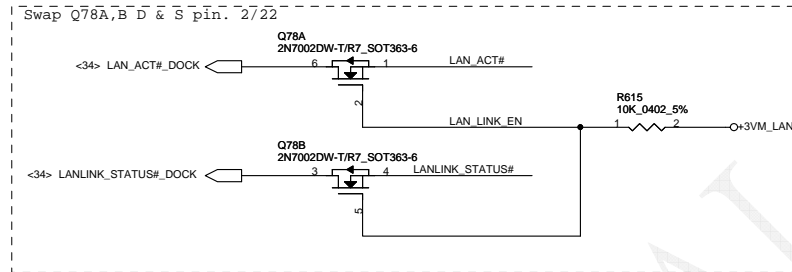
Place closely pin H1

Pin connection error, modify in 10/24.

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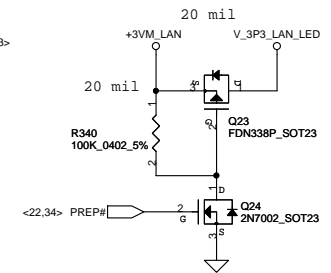
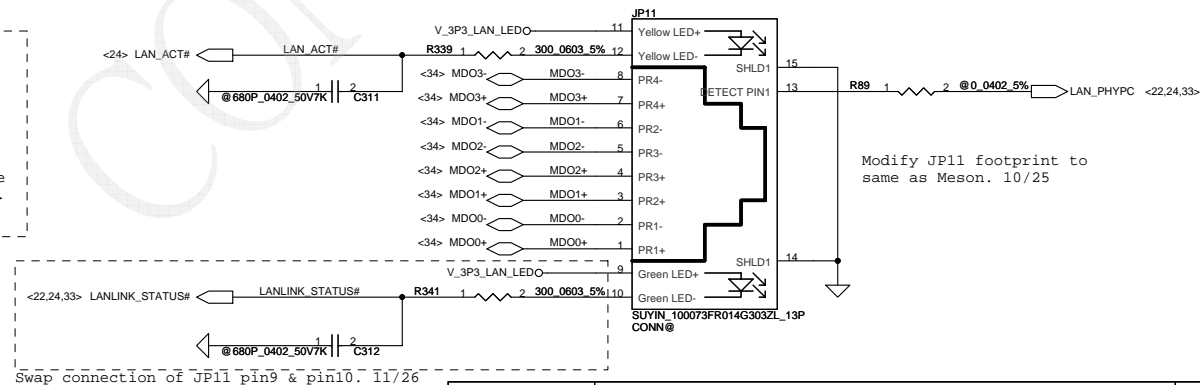
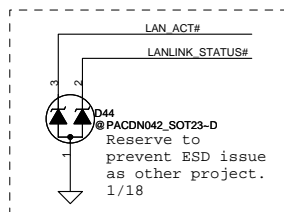
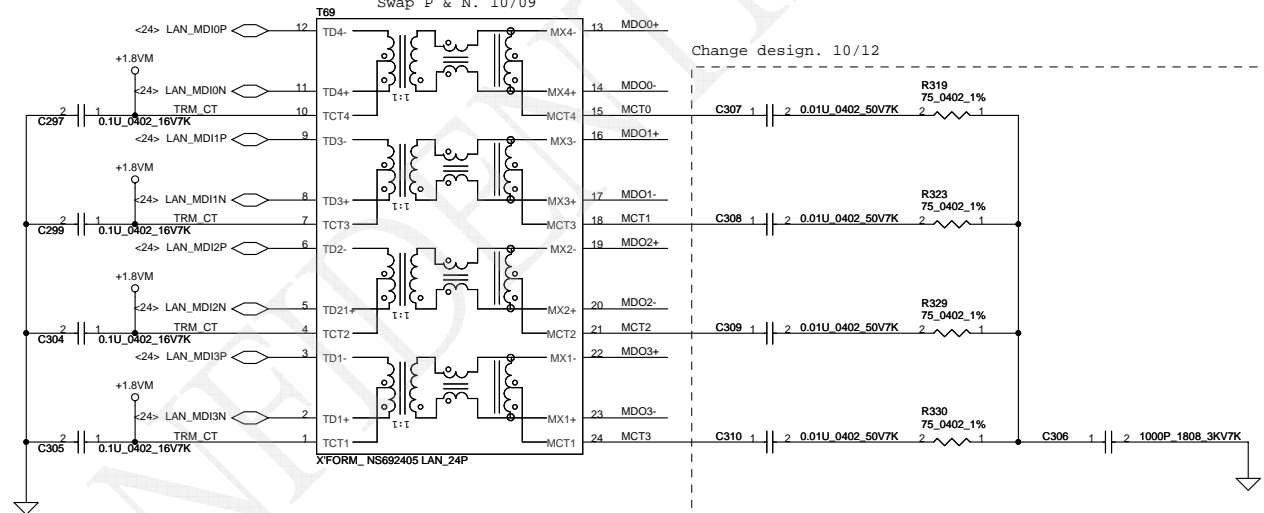


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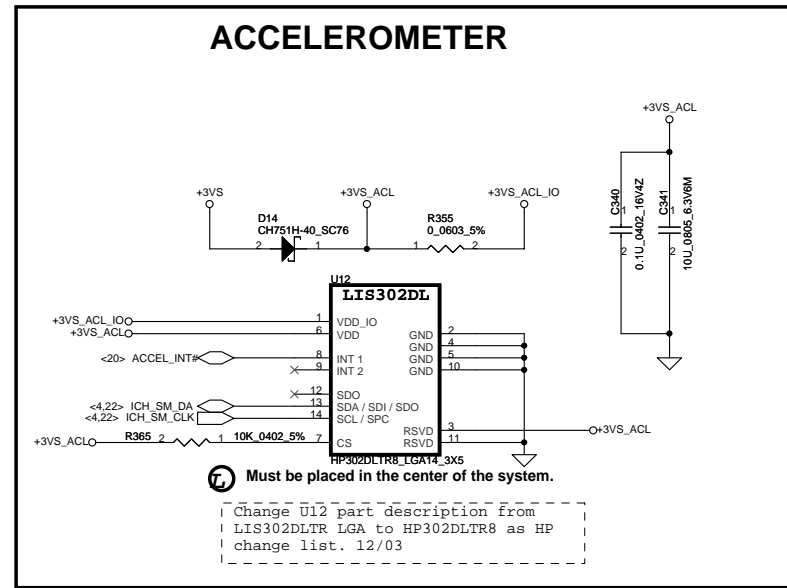
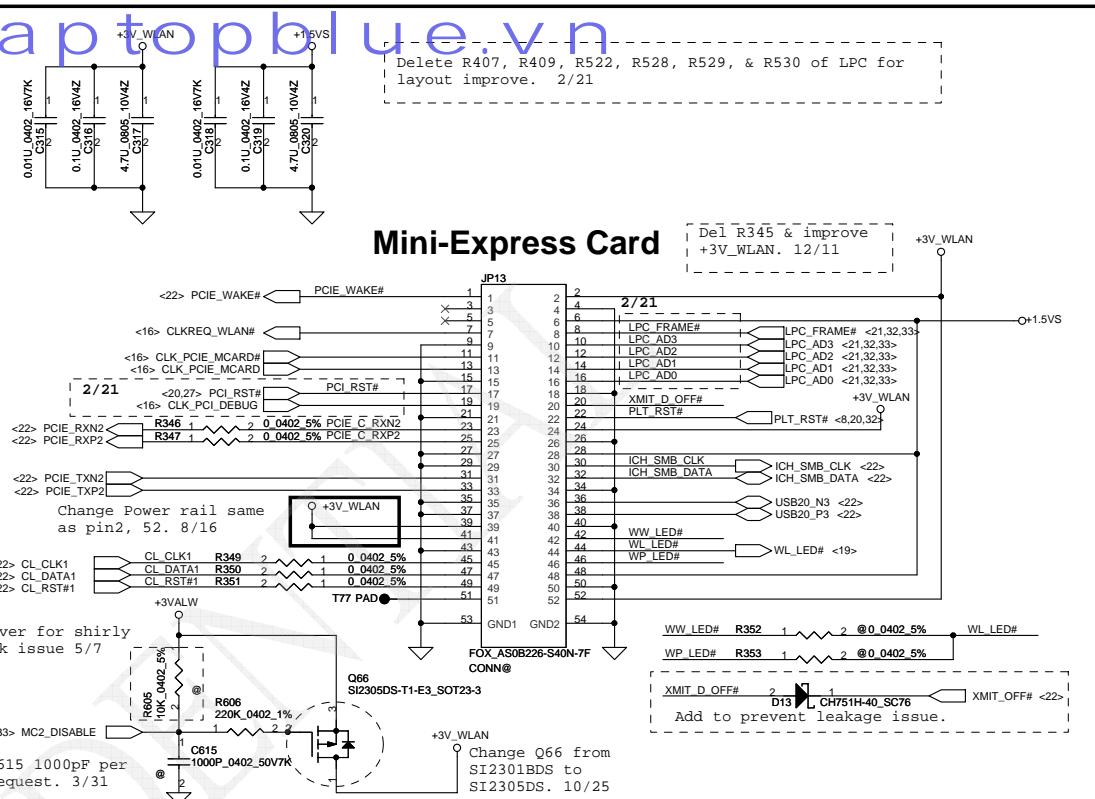


Delete all termination cause they are already inside BOAZMAN. 9/28

Pin Swap. 10/05
Swap P & N. 10/09



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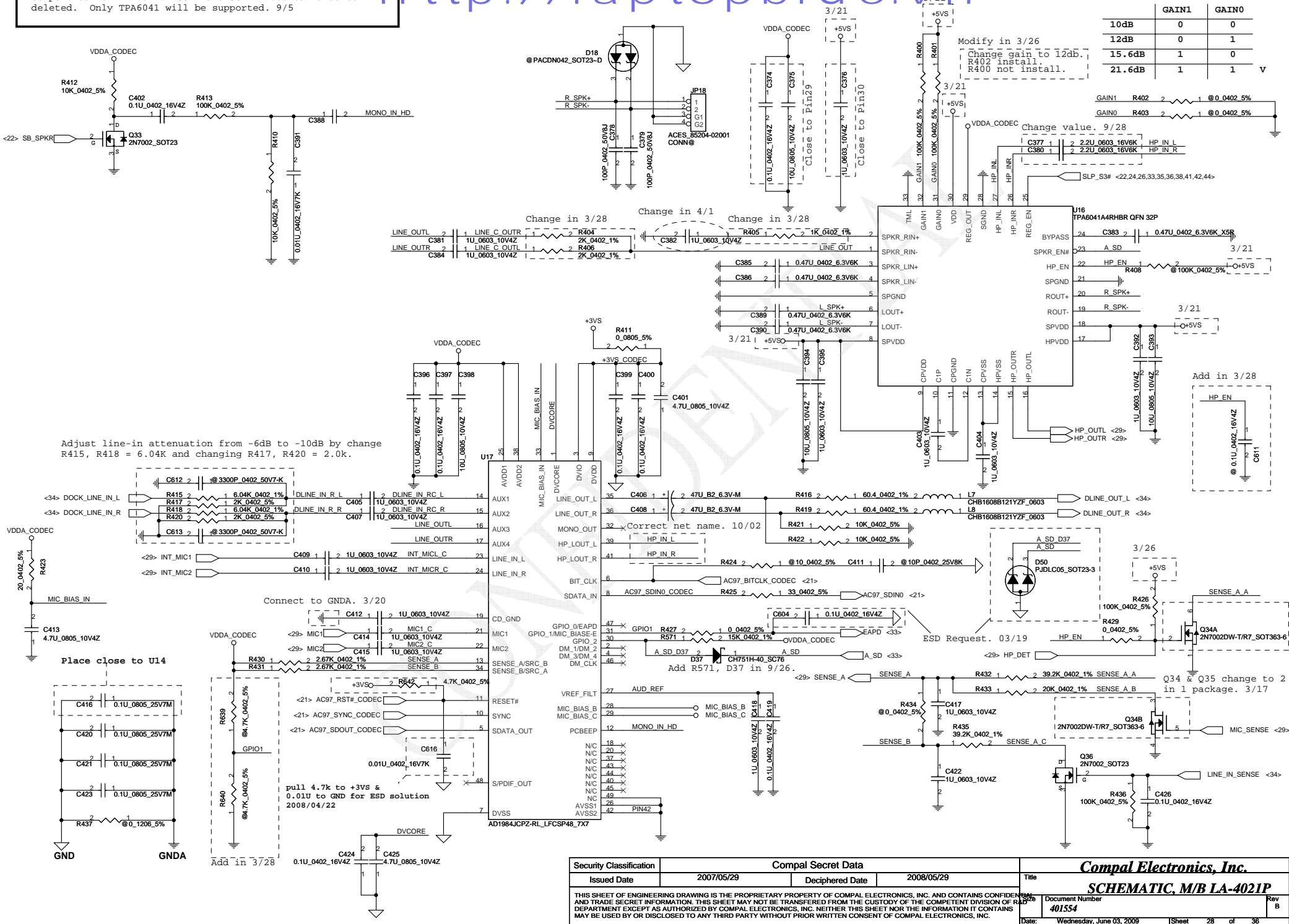
TPA6044 no longer needed. So delete BOM options & co-layout components for TPA6044. SGND and SGND1 nets can also be deleted. Only TPA6041 will be supported. 9/5

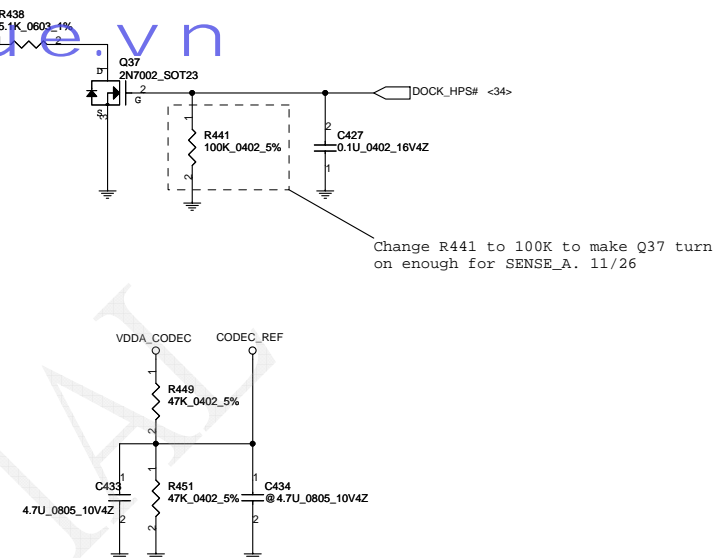
http://laptopblue.vi

AMP. FOR INTERNAL SPEAKER

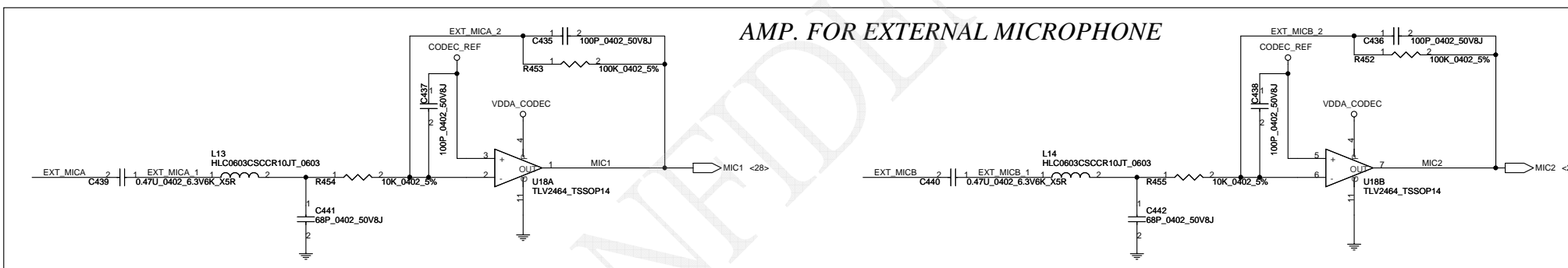
	GAIN1	GAIN0
10dB	0	0
12dB	0	1
15.6dB	1	0
21.6dB	1	1

v

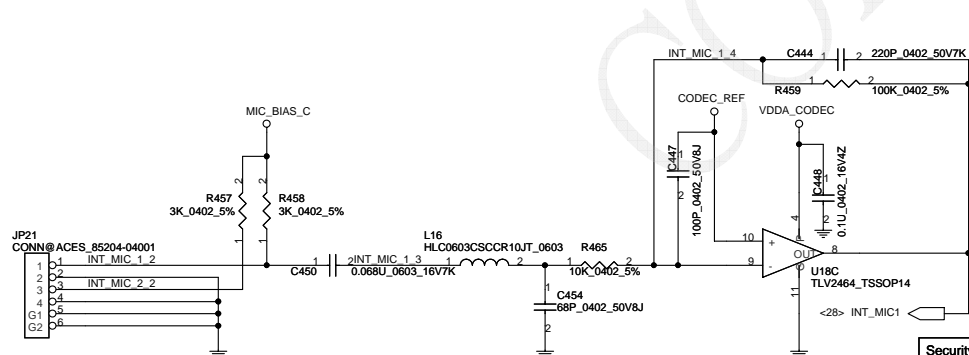




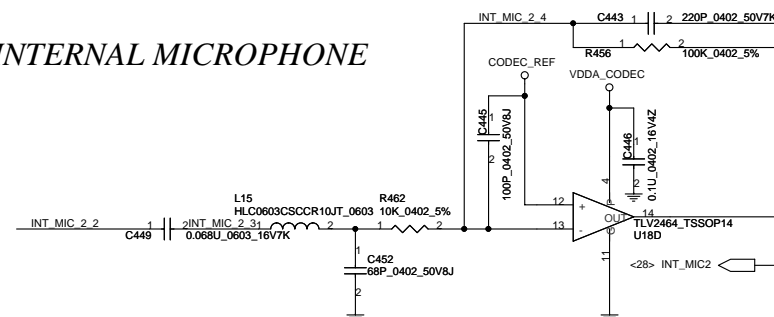
EXTERNAL MICROPHONE/LINE OUT JACK



AMP. FOR EXTERNAL MICROPHONE

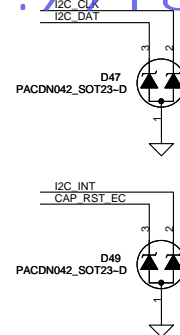
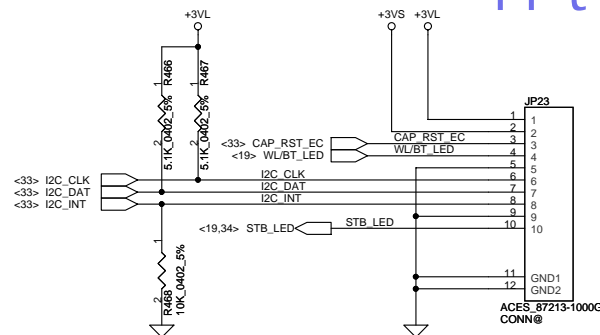


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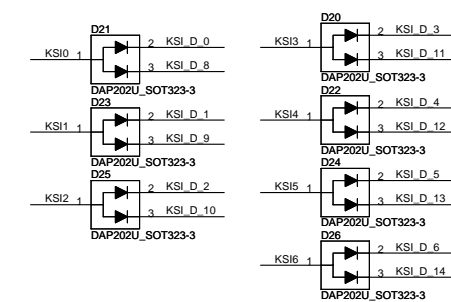
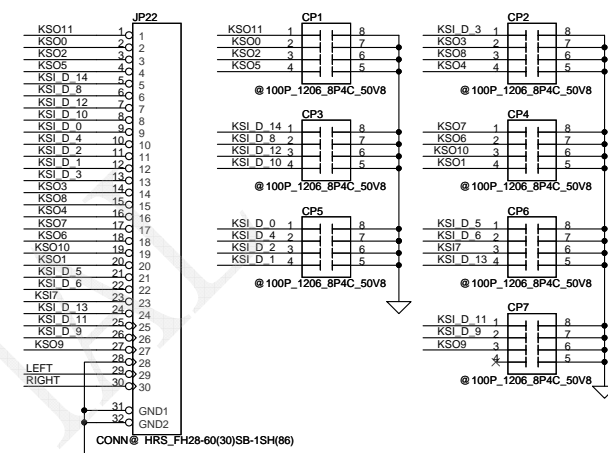


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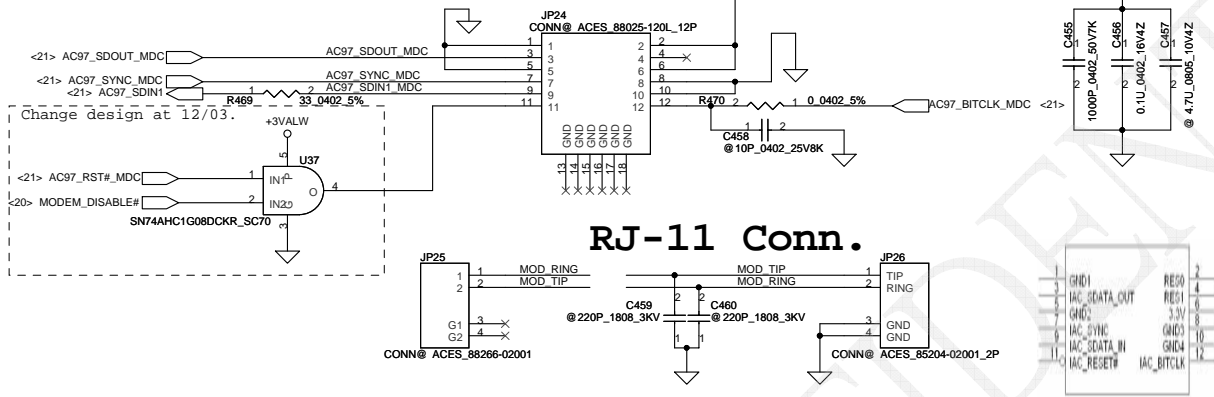
Diagram illustrating a network connection. A laptop is connected to a server via a network interface. The connection is labeled `http://laptopblue.vr`. The server is labeled `INT` and `KSOI(0,11)`. The connection is also labeled `I2C CLK` and `I2C DAT`.



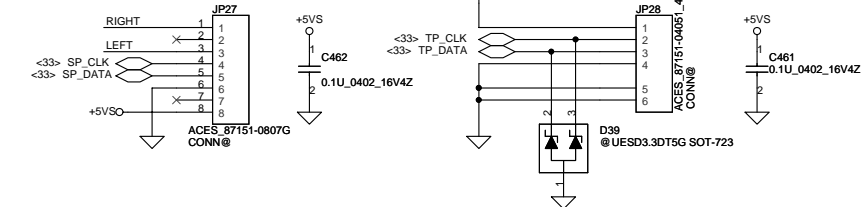
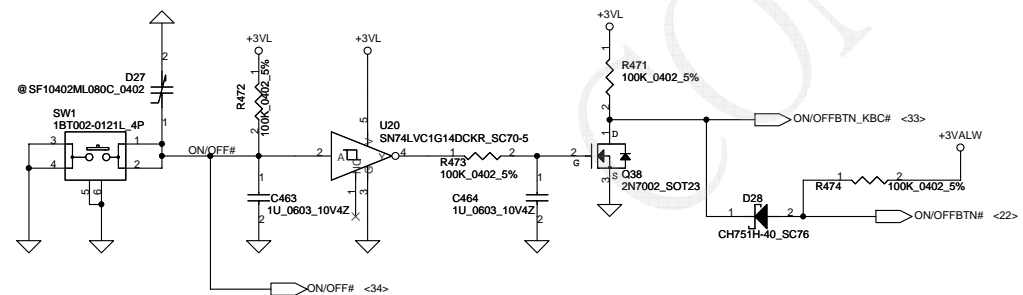
<33> KSO[0..11] KSO[0..11]
 <33> KSI[0..7] KSI[0..7]



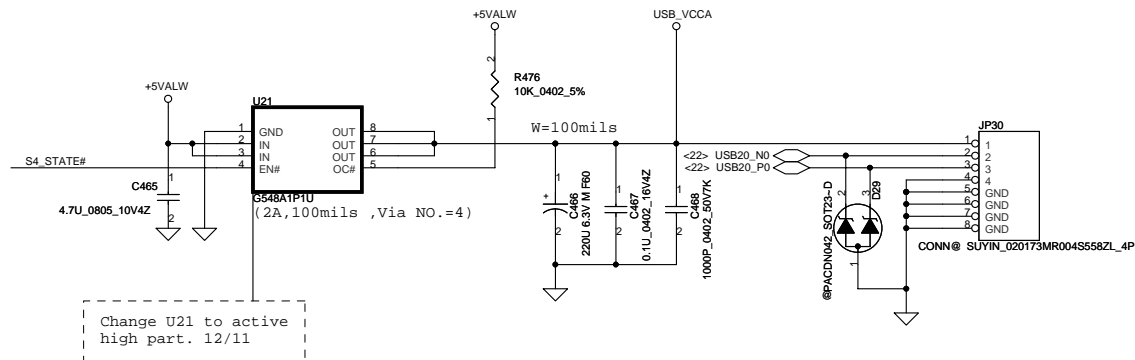
RJ-11 Conn.



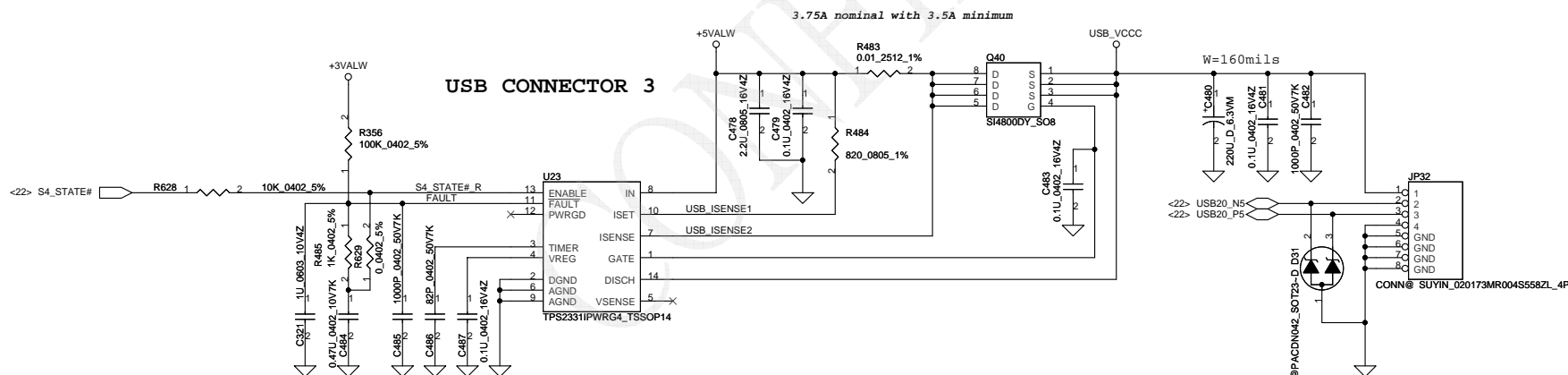
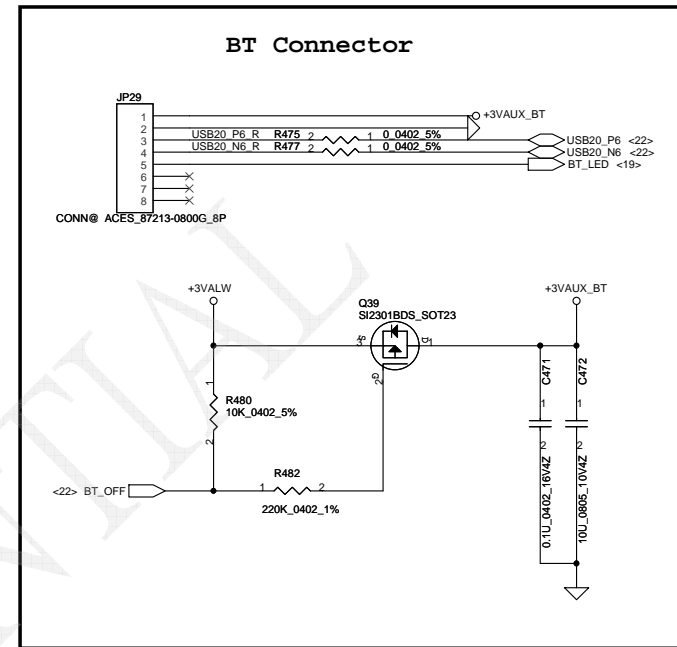
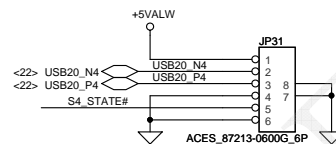
TrackPoint CONN. T/P BOARD.



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U22, D30, R481, C474 ~ C477 will move to USB board side to save M/B space.



Change C486 from 2200pF to 680pF.
Change C321 from 1000pF to 1uF.
Change R356 from 10K to 100K.
Change R484 from 1000pF to 0.47uF.
Change R484 from 1K to 820.

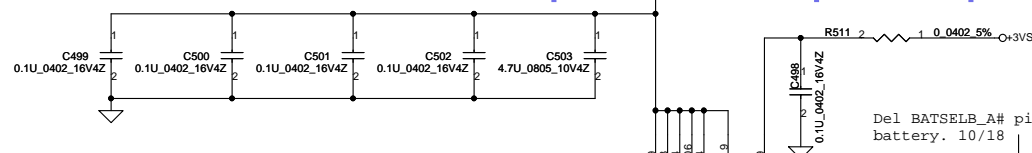
Currently power USB will not enable after OCP, so add R629 make it enable after OCP free.

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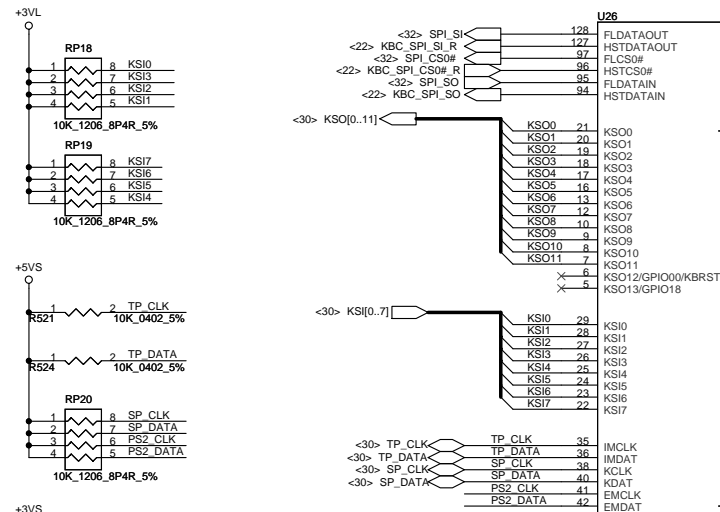
<http://laptopblue.vn>



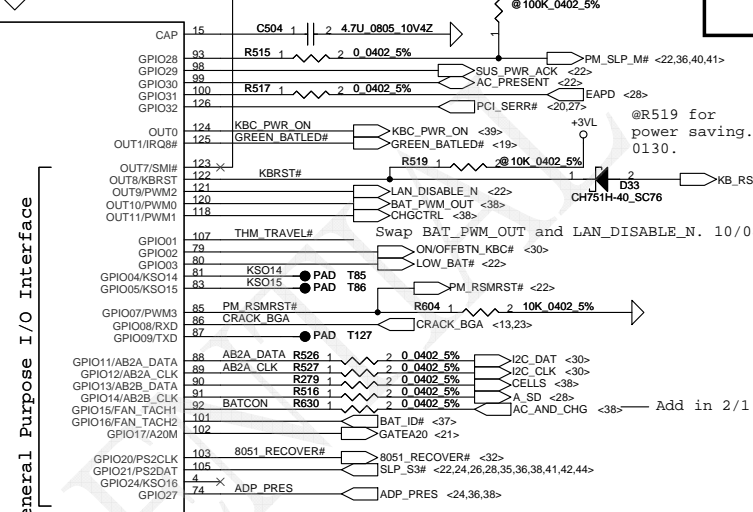
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Del D35 & @523 for
power saving. 0130



SMSC 1091-NU TQFP-128P

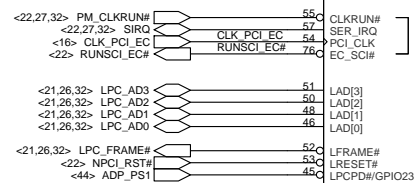
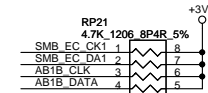
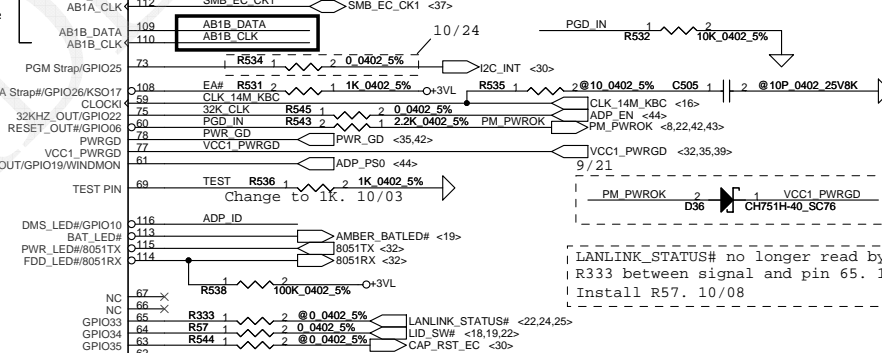
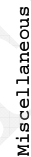
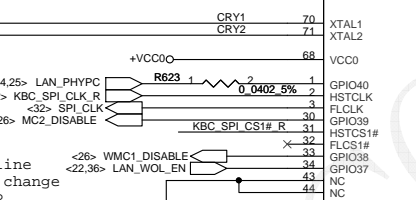


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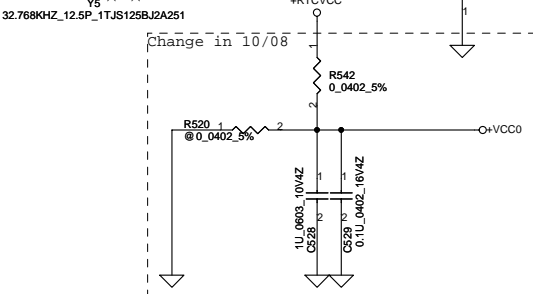
      |-----|
      | ADP PRES | 1 ----- 100K_0402_5%
      | CRACK BGA | R523 ----- 100K_0402_5%
      | BATCON    | R525 ----- 100K_0402_5%
      | THM TRAVEL | R322 ----- 100K_0402_5%
      |           | R320 ----- 100K_0402_5%
      | ADP ID    | R624 ----- 10K_0402_5%

```

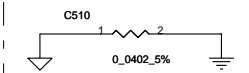
Keep location as PR154. IZ74

LPC
Bus

```
| LANLINK_STATUS# no longer read by KBC. Add
| R333 between signal and pin 65. 10/08
| Install R57. 10/08
```



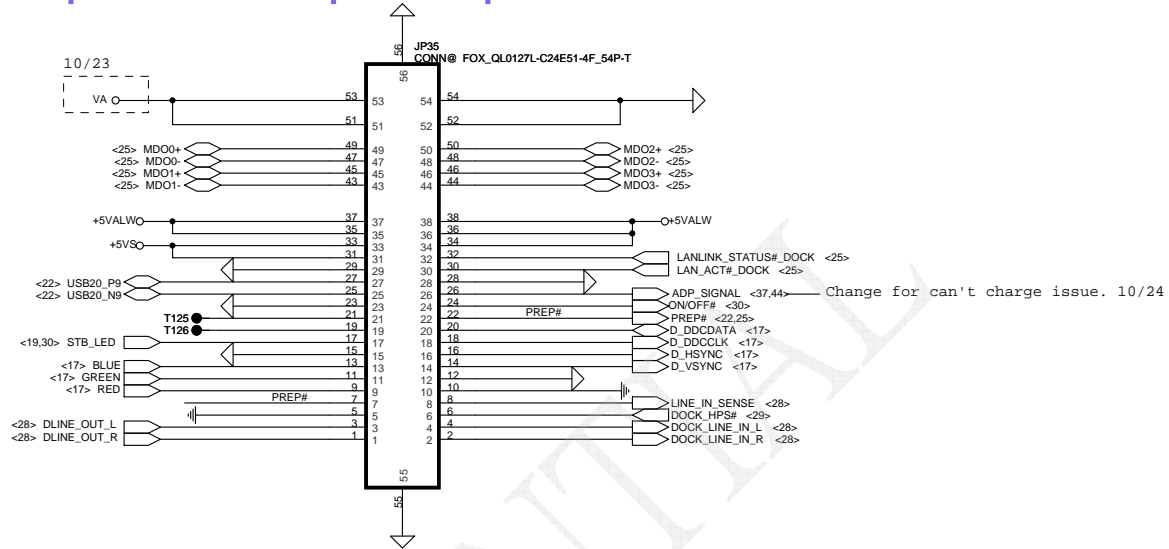
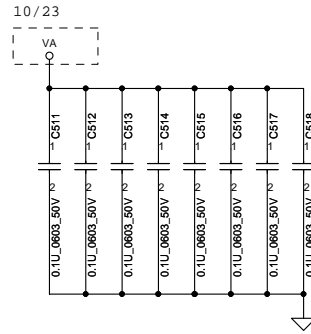
AGND FILTER



SMSC guideline suggest to change 0.1U to 0 ohm

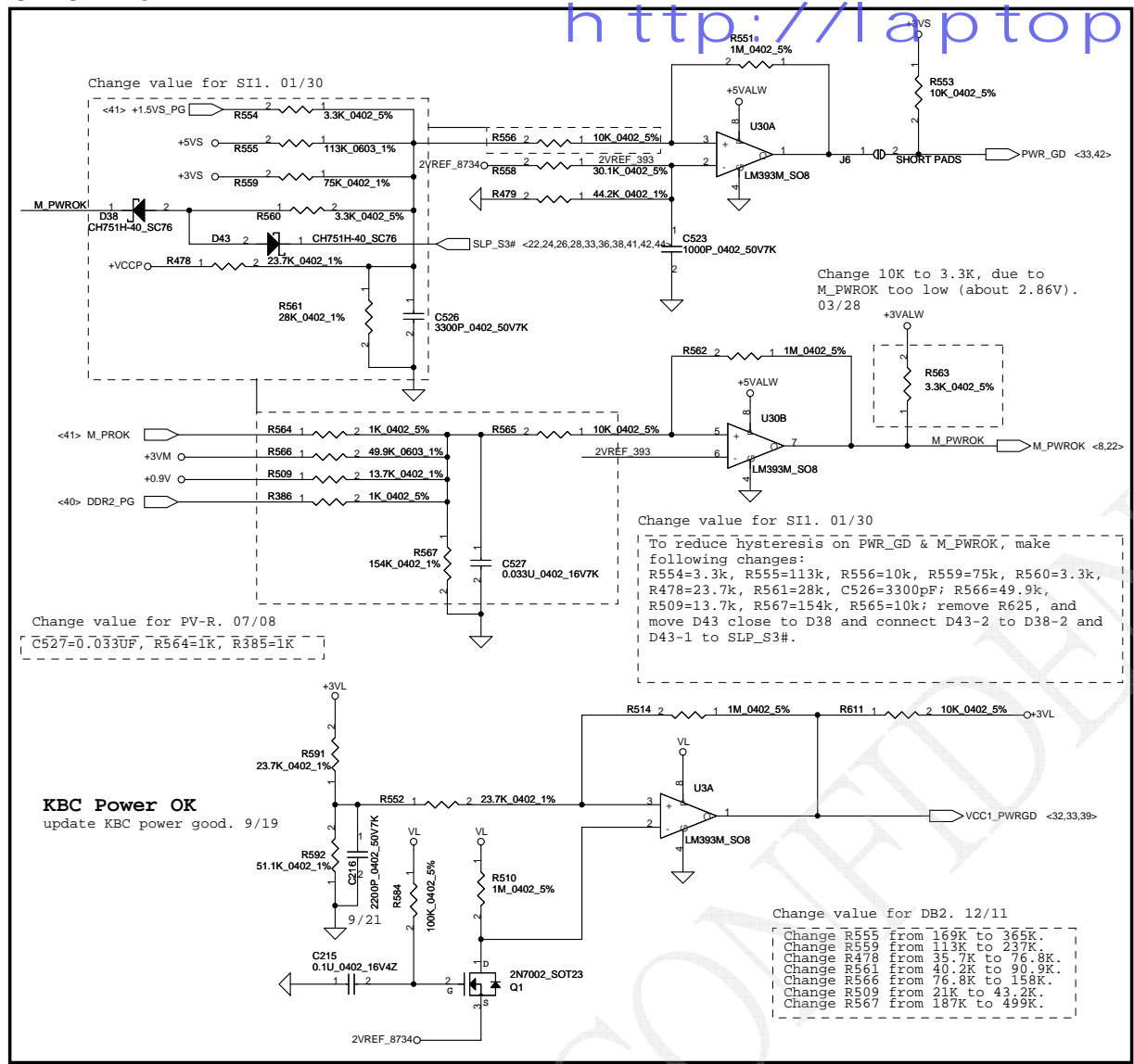
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DOCKING CONNECT

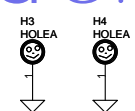


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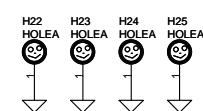
http://laptopblue.vn



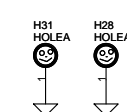
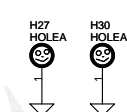
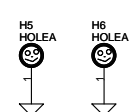
WWAN Card STANDOFF



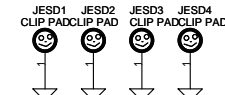
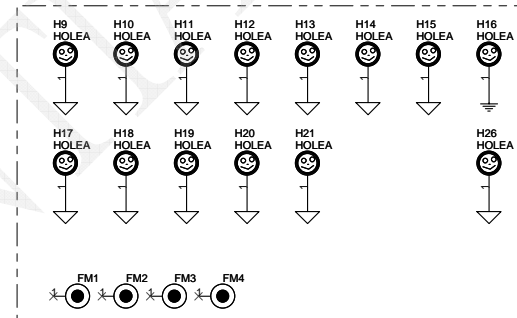
CPU support



MDC STANDOFF



Del H1, H7 & H8. 1/18



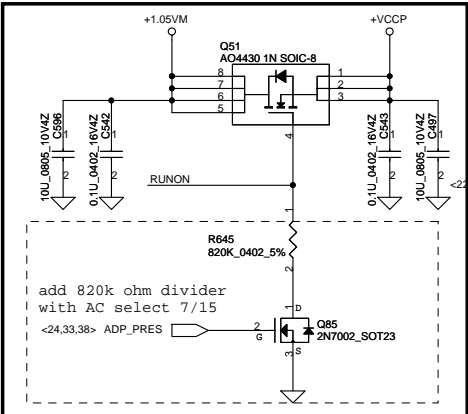
Change value for DB2. 12/11

Change R555 from 169K to 365K.
Change R559 from 113K to 23.7K.
Change R478 from 35.7K to 76.8K.
Change R561 from 40.2K to 90.9K.
Change R566 from 76.8K to 158K.
Change R509 from 21K to 43.2K.
Change R567 from 187K to 499K.

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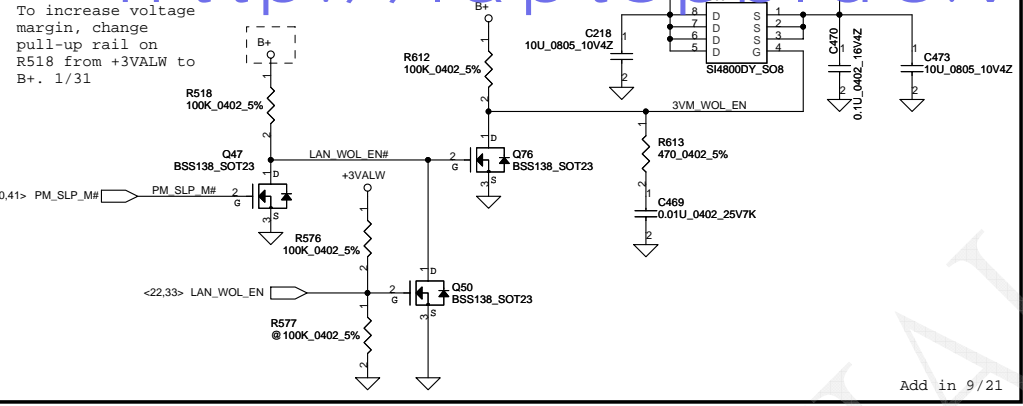
Modify at 7/31 after discuss with power team.

+1.05VM to +VCCP Transfer

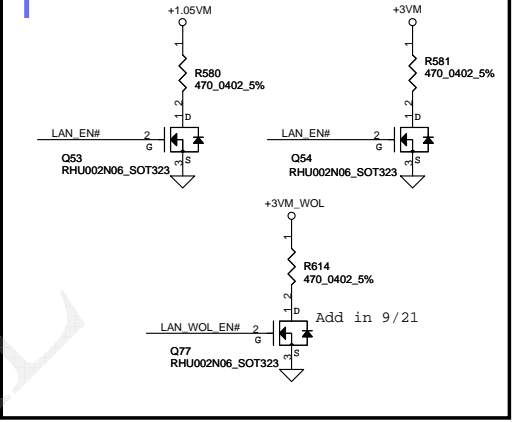


+3VALW to +3VM_WOL Transfer

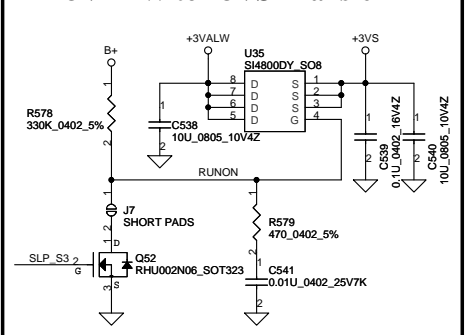
To increase voltage margin, change pull-up rail on R518 from +3VALW to B+. 1/31



Discharge circuit-2 for V-M

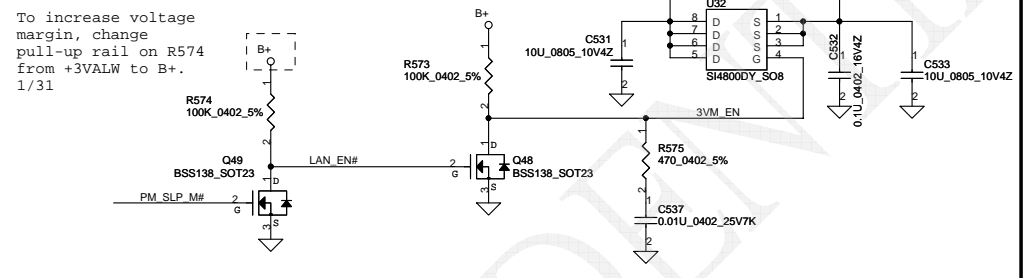


+3VALW to +3VS Transfer



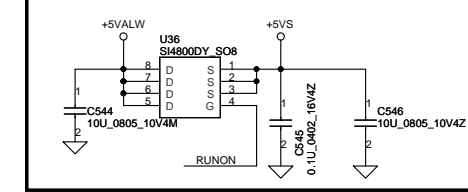
+3VALW to +3VM Transfer

To increase voltage margin, change pull-up rail on R574 from +3VALW to B+. 1/31

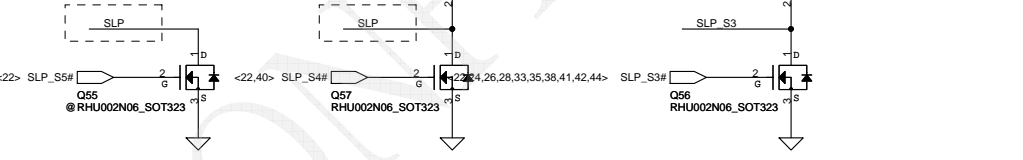


SYS. STATE	PM_SLP_M#	LAN_WOL_EN	+3VM_WOL	+3VM
M-off / No WOL	0	0	0V	0V
M-off / WOL	0	1	3.3V	0V
M1 (ME on)	1	0	3.3V	3.3V
M1 (ME on)	1	1	3.3V	3.3V

+5VALW to +5VS Transfer



Design Change at 9/14.



Discharge circuit-1

