

# PCB STACK UP

## 8L

LAYER 1 : TOP  
LAYER 2 : SGND  
LAYER 3 : IN1  
LAYER 4 : SVCC  
LAYER 5 : IN2  
LAYER 6 : IN3  
LAYER 7 : SGND1  
LAYER 8 : BOT

### Cable Docking

VGA  
RJ-45  
CIR/Pwr btn  
SPDIF Out  
Stereo MIC  
Headphone Jack  
USB Port  
VOL Cntr

PAGE 38

SYSTEM CHARGER ISL6251AHAZ-1  
PAGE 39

SYSTEM POWER ISL6237IRZ-T  
PAGE 40

DDR II SMDDR\_VTERM  
1.8V/1.8VSUS(TPS51116REGR)  
PAGE 44

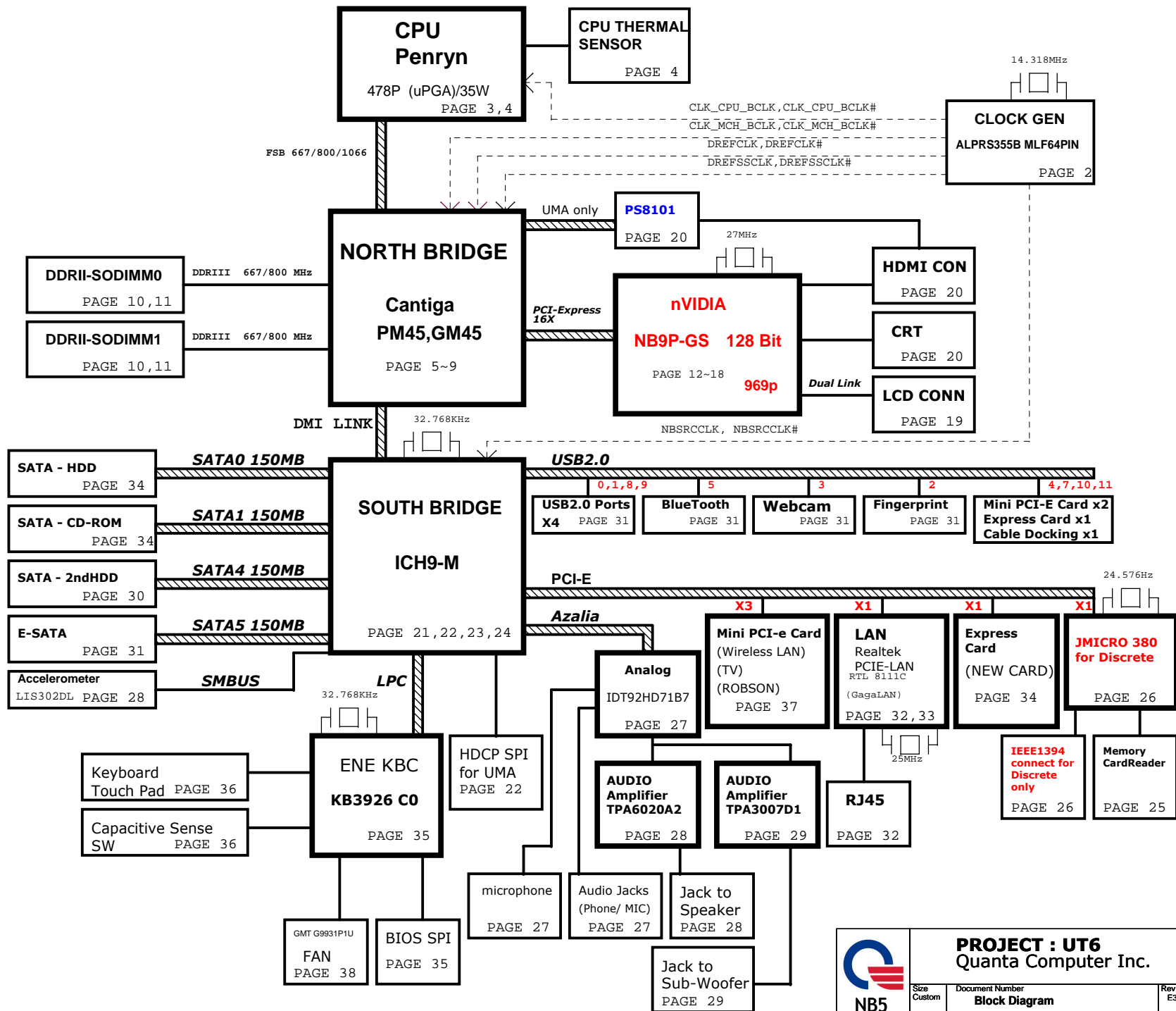
VCCP +1.5V AND GMCH  
1.05V(RT8204)  
PAGE 44

VGACORE(1.025V)Oz8118  
PAGE 43

CPU CORE ISL6266A  
PAGE 42

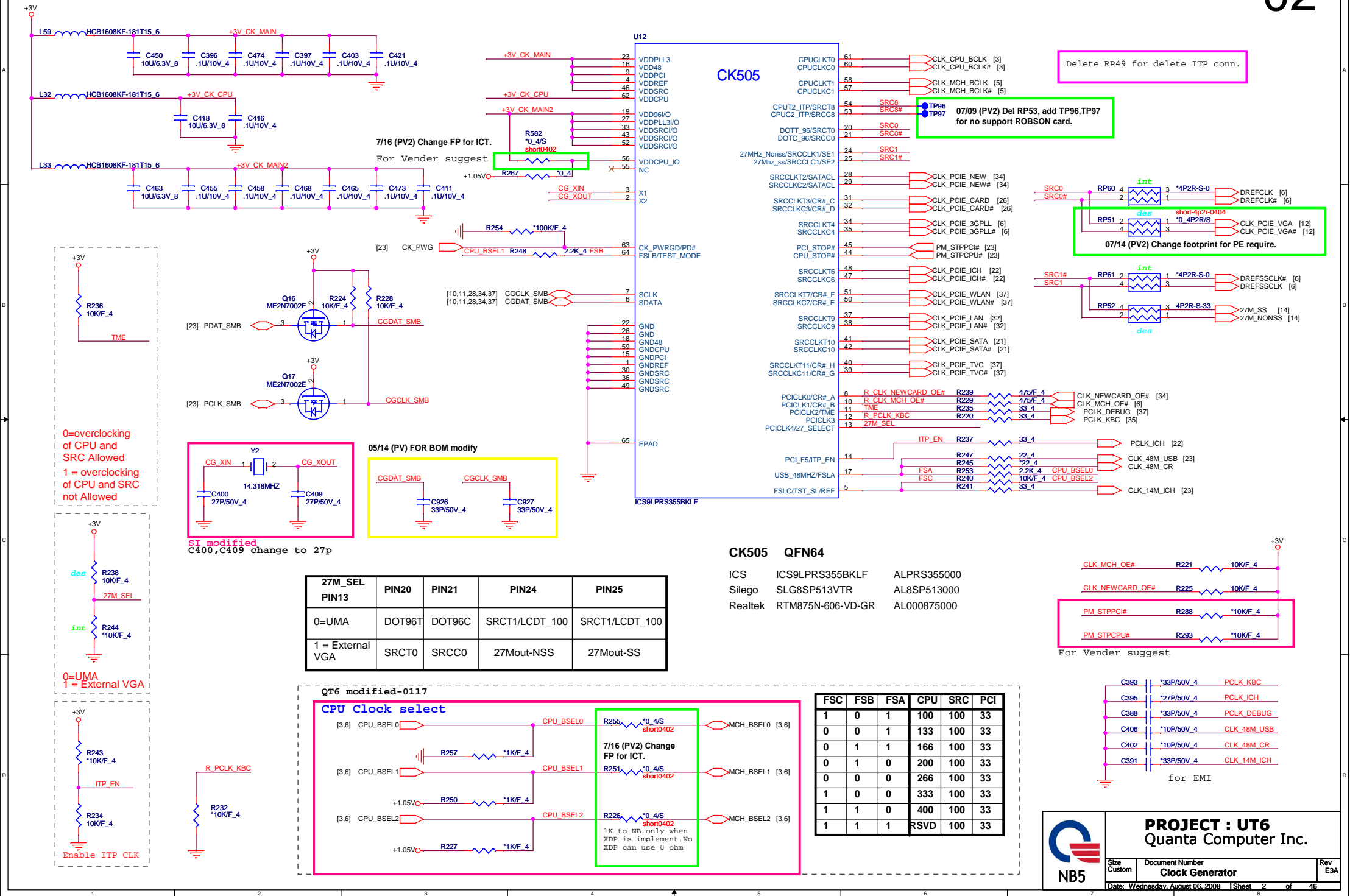
# UT6 BLOCK DIAGRAM

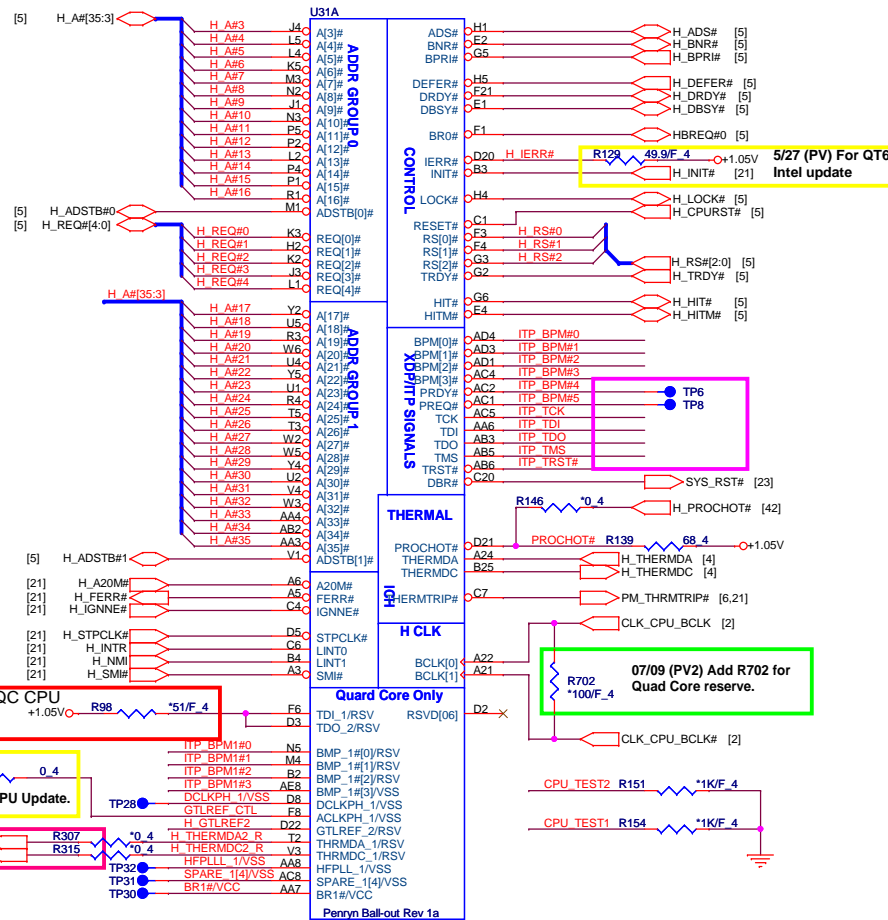
01



**PROJECT : UT6**  
Quanta Computer Inc.

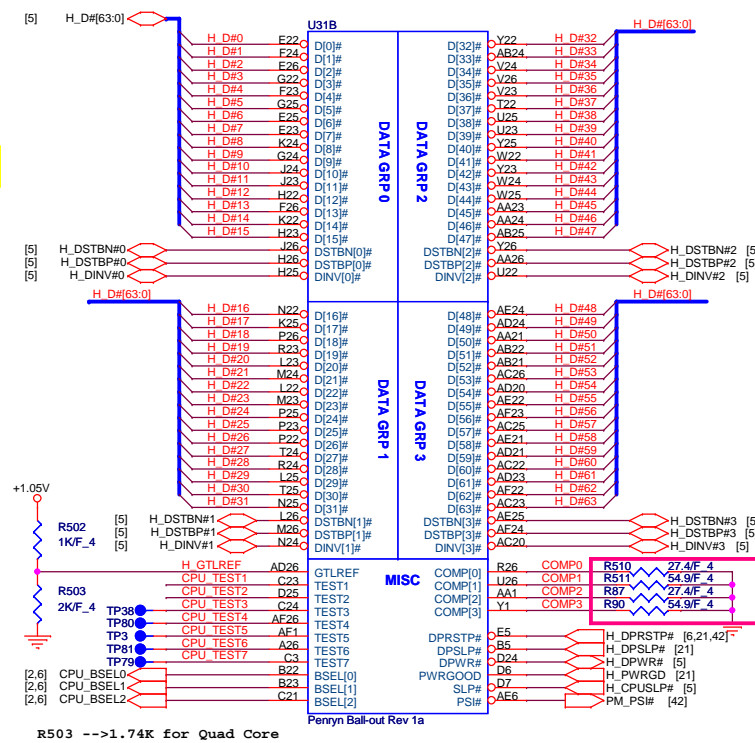
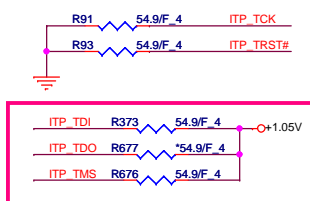
Size Custom	Document Number <b>Block Diagram</b>	Rev E3A
Date: Wednesday, August 06, 2008		Sheet 1 of 46



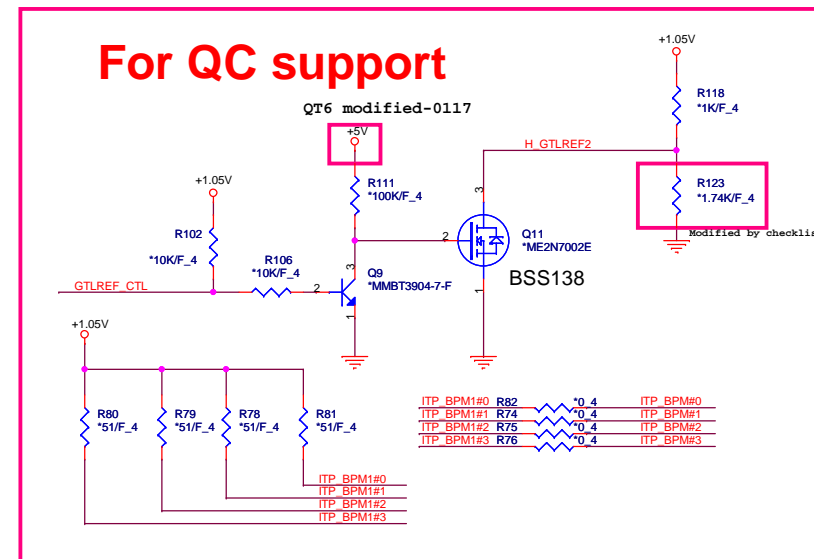


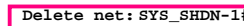
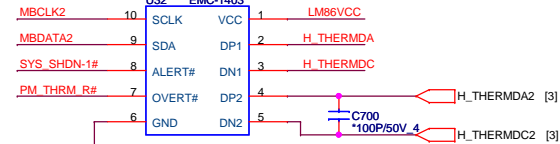
MODEL	UT7 Quad Core	UT6 Dual Core
R696	*0_4	0_4

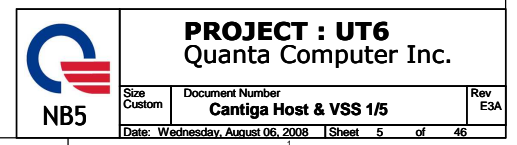
## Populate ITP700Flex for bringup



	COMP0/2	COMP1/3
Dual Core	27.4 Ohm (CS02742FB19)	54.9 Ohm (CS05492FB19)
Quard Core	24.9 Ohm (CS02492FB29)	49.9 Ohm (CS04992FB31)







**MCH\_CFG\_5** DMIx2 selection  
Low = DMI X2  
High = DMI X4 (Default)  
**MCH\_CFG\_16** FSB Dynamic ODT  
Low = Dynamic ODT disabled  
High = Dynamic ODT enabled (default)  
**MCH\_CFG\_9** PCI Express Graphic Lane  
Low: Reverse Lane  
High: Normal operation(Default)  
**MCH\_CFG\_19** DMI Lane Reversal  
Low = Normal operation (Default)  
High = Reverse Lanes

**MCH\_CFG\_6** ITPM Host Interface  
Low = The ITPM Host Interface is enabled2  
High = The ITPM Host Interface is disabled (default)

**MCH\_CFG\_7** Intel(R) Management Engine Crypto  
Low: Intel(R) Management Engine Crypto  
High: Intel(R) Management Engine Crypto  
TLS cipher suite with no confidentiality  
High: Intel(R) Management Engine Crypto  
TLS cipher suite with no confidentiality (Default)

**MCH\_CFG\_10** PCIe Lookback Enable  
Low = Enabled3  
High: Disabled (Default)

**MCH\_CFG\_12/13** XOR/ALL/CLOCK Un-gating

**MCH\_CFG\_13** **MCH\_CFG\_12** Configuration

0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)

**MCH\_CFG\_20**

Digital Display Port (SDVO/DP/HDMI) Concurrent with PCIE  
Low = Only digital display port (SDVO/DP/HDMI) or PCIE is operational (default)  
High = Digital display port (SDVO/DP/HDMI) and PCIE are operating simultaneously via the PEG port

**MCH\_CFG2:0**

000 = FSB1066  
010 = FSB800  
011 = FSB667

Others = Reserved

**MCH\_CFG\_2**

**MCH\_CFG\_3**

**MCH\_CFG\_4**

**MCH\_CFG\_5**

**MCH\_CFG\_6**

**MCH\_CFG\_7**

**MCH\_CFG\_8**

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**MCH\_CFG\_258**

**MCH\_CFG\_259**

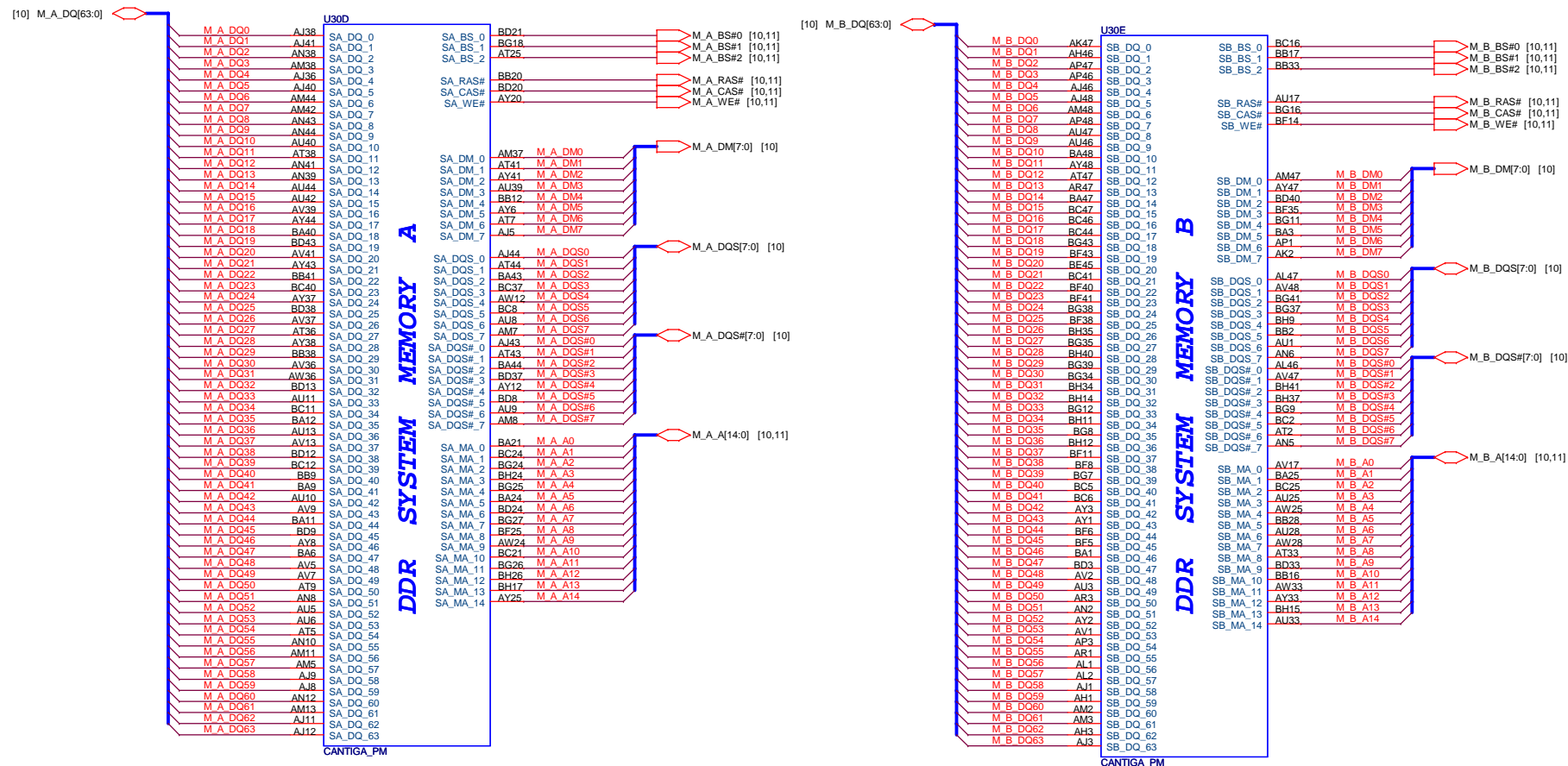
**MCH\_CFG\_260**

**MCH\_CFG\_261**

**MCH\_CFG\_262**

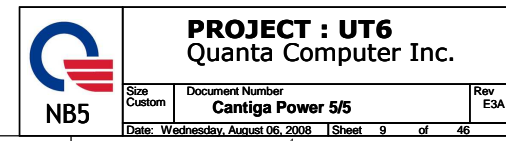
**MCH\_CFG\_263**

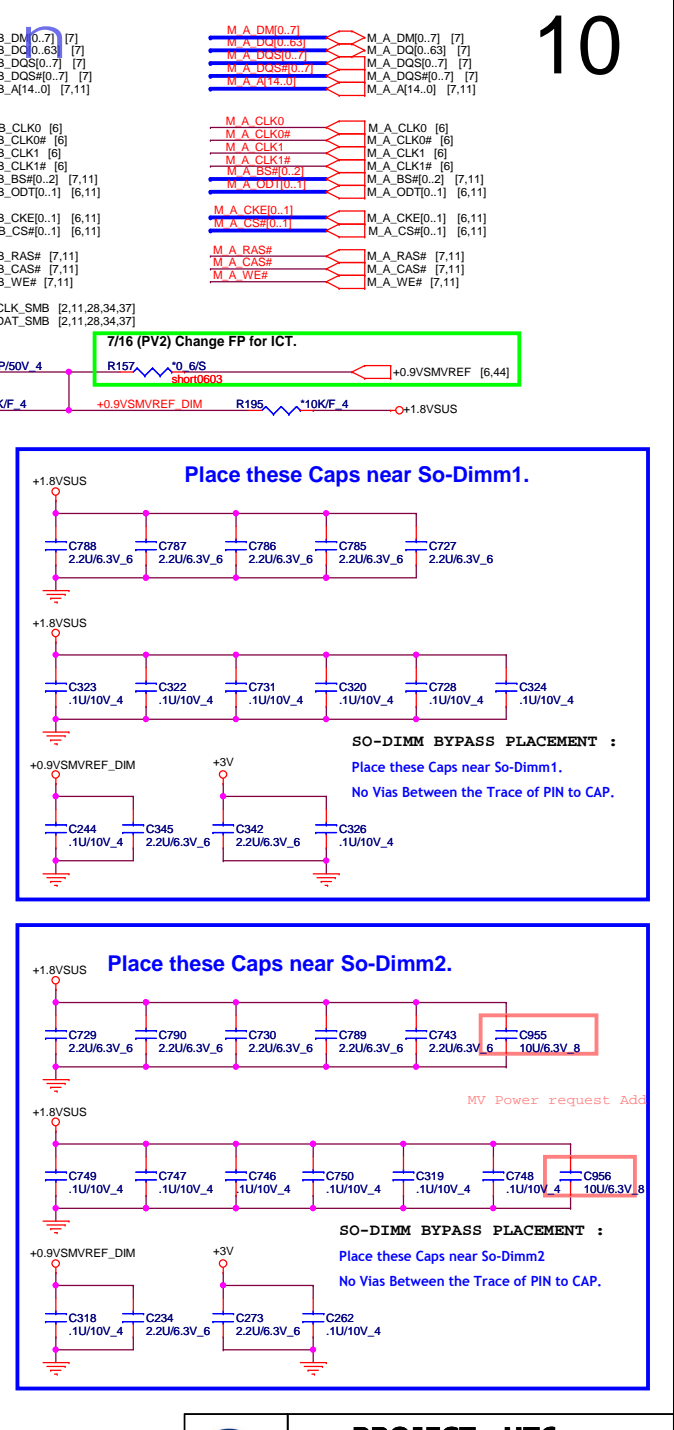
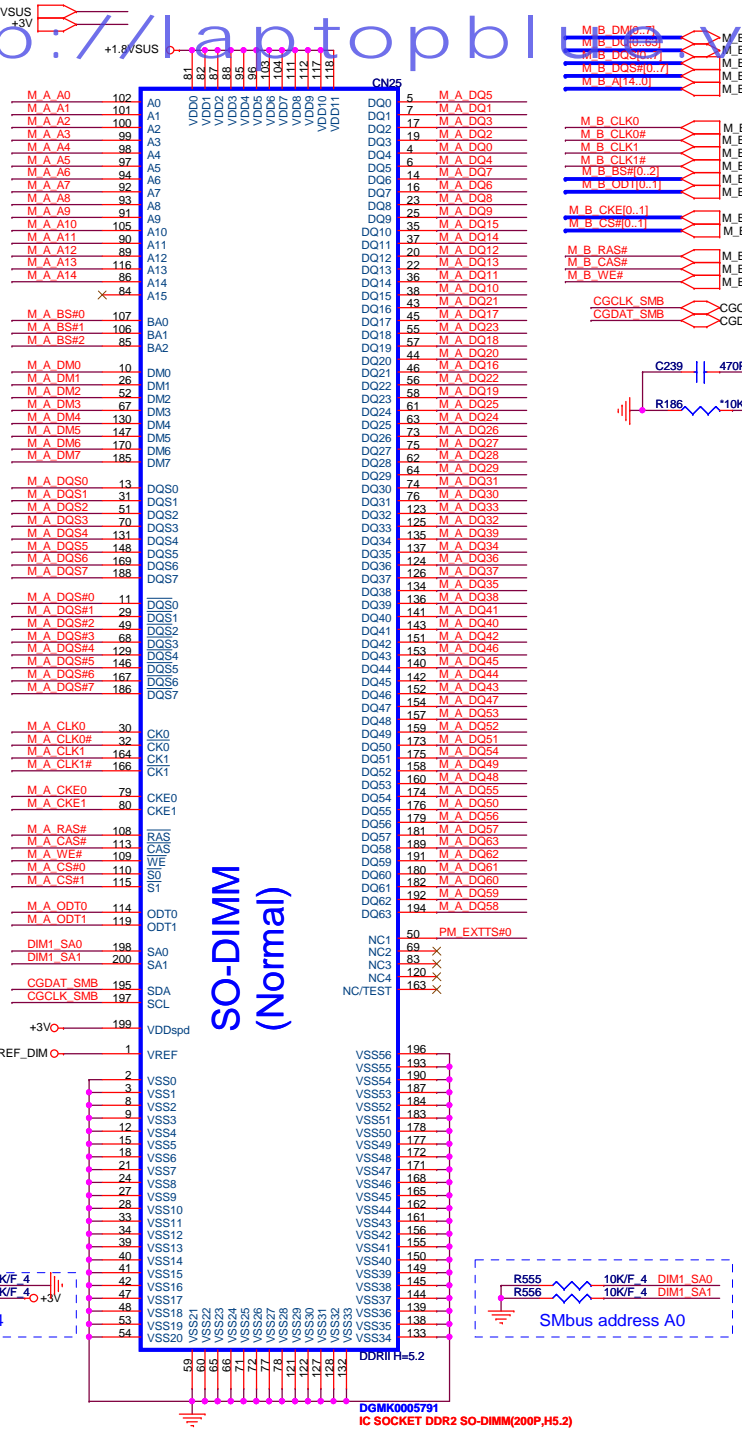
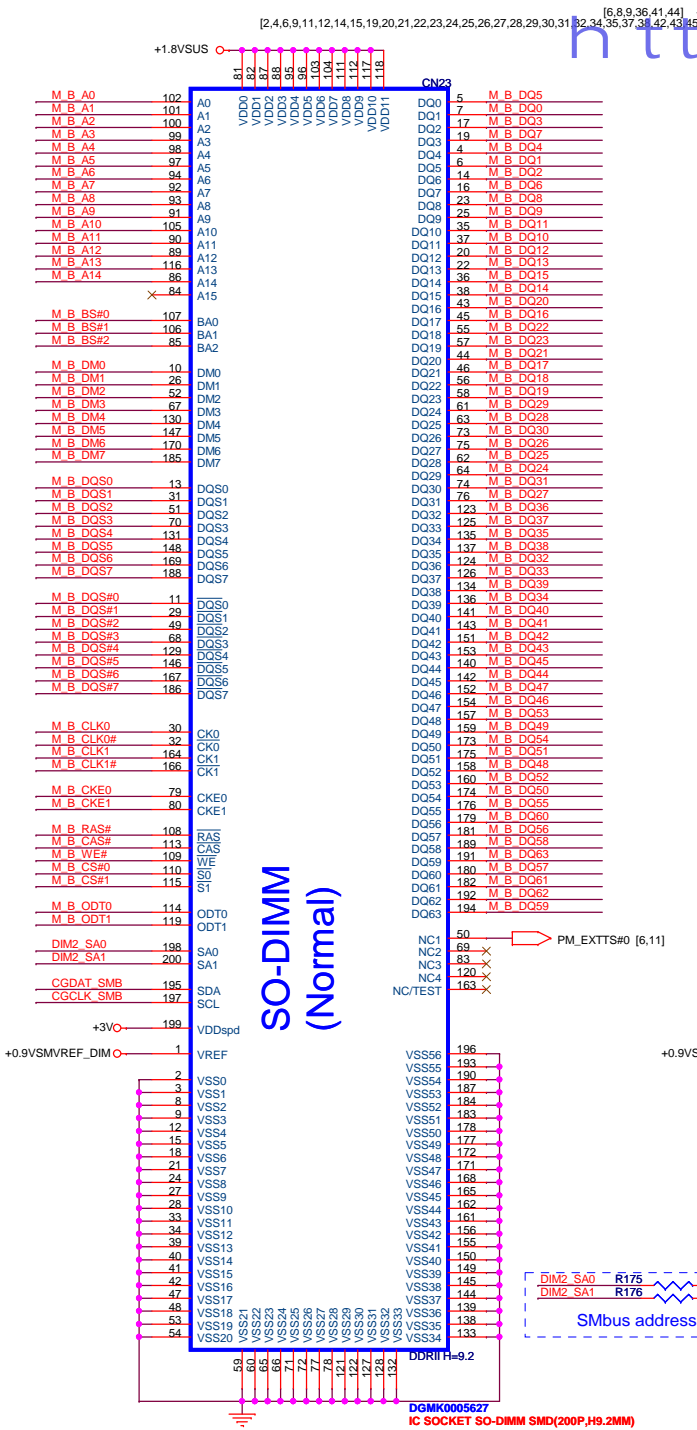
**MCH\_CFG\_264**





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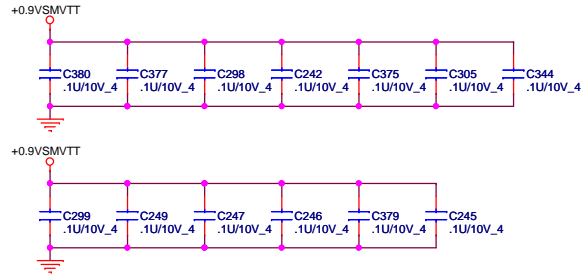




# DDRII DUAL CHANNEL A,B.

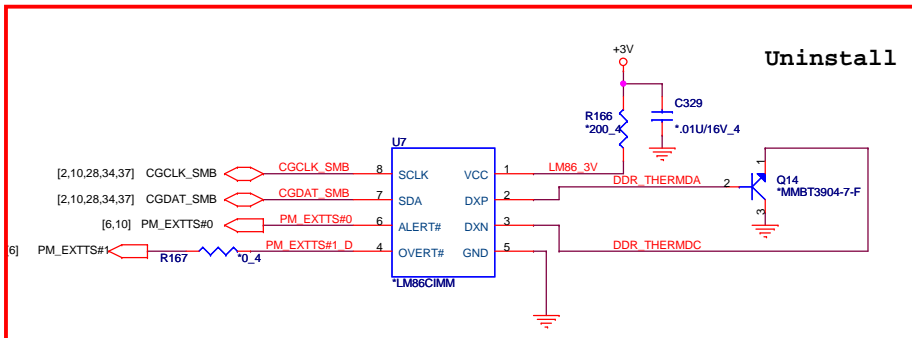
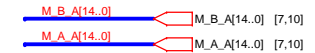
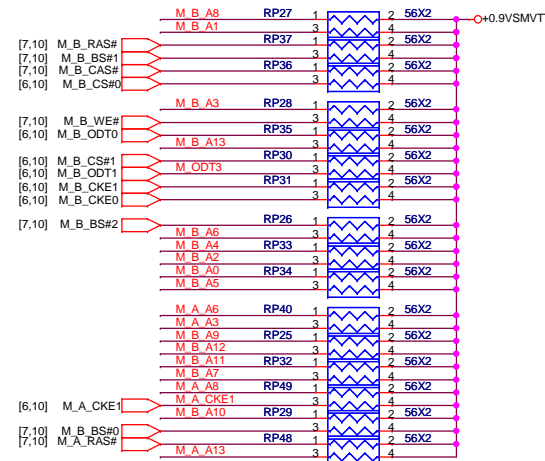
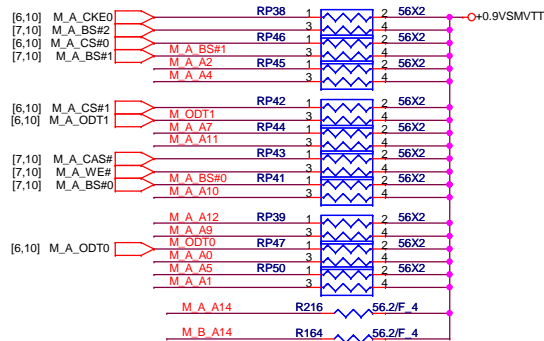
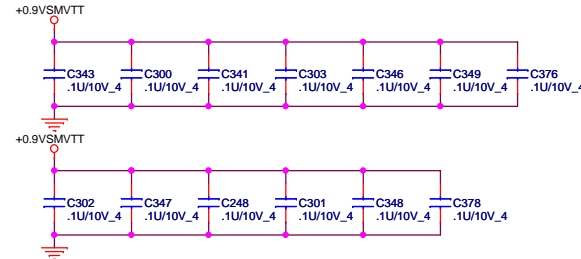
11

## DDRII A CHANNEL



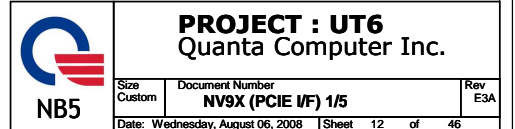
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDR\_VTERM

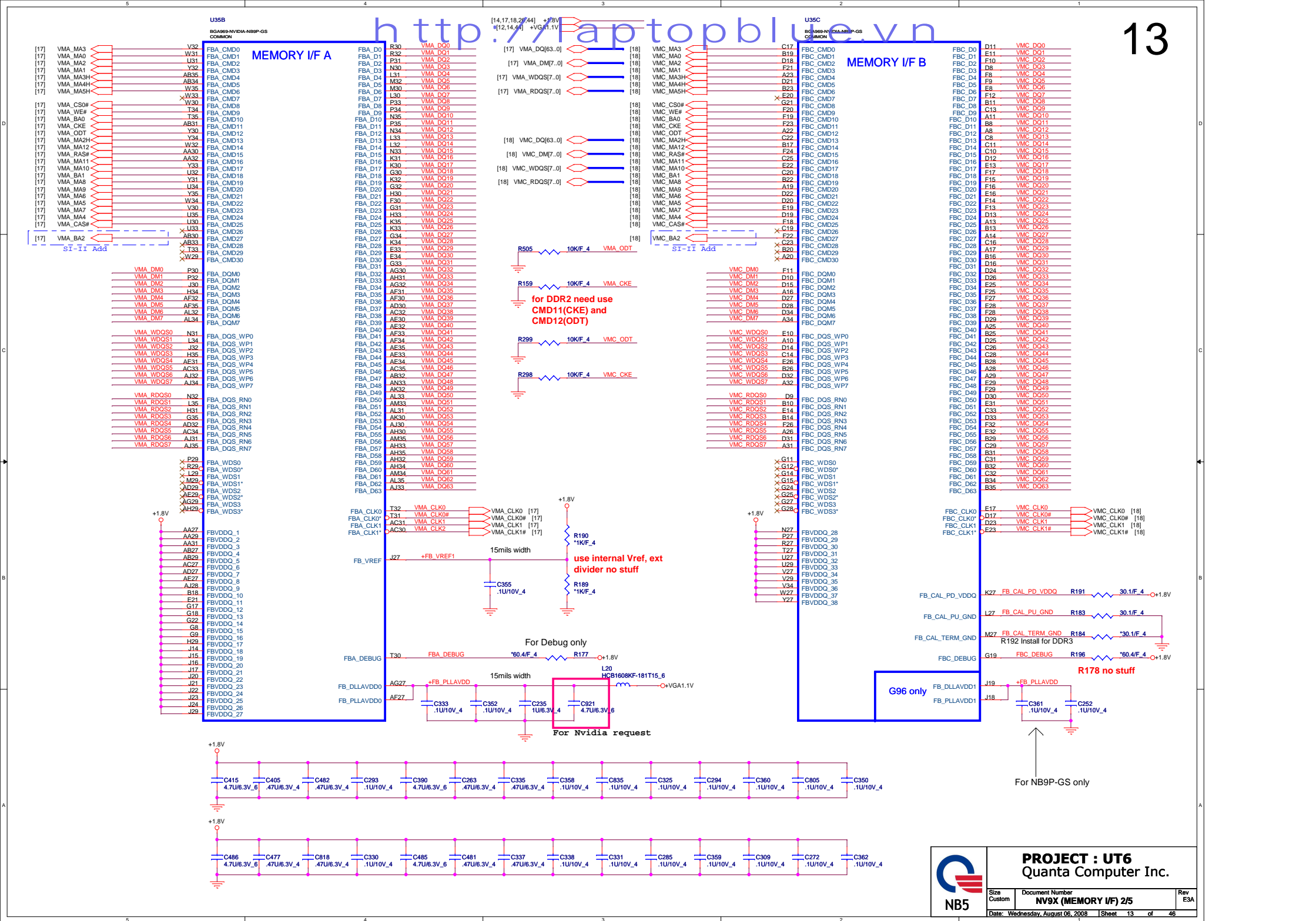
## DDRII B CHANNEL

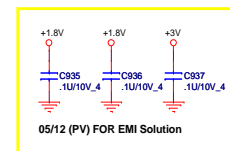
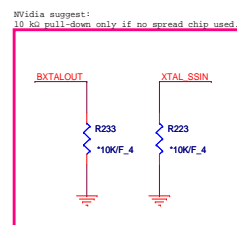
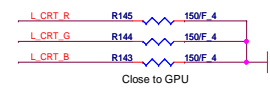


**PROJECT : QT6**  
Quanta Computer Inc.

Size Custom	Document Number <b>DDR2 termination</b>	Rev E3A
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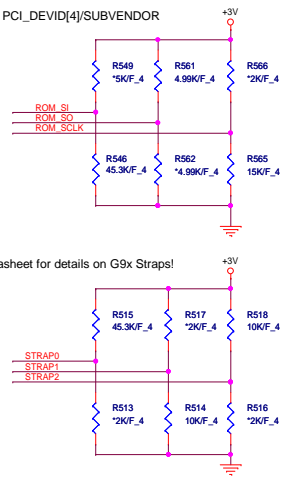






# NB9P-GS (G96) Straps NB9M-GE (G98) Straps GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	FBVDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL



Logical Strap Bit Mapping		
	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	XCLK_277	TVMODE[2]	TVMODE[1]	TVMODE[0]
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM100
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]

1000  
0010  
XXXX  
XXXX  
0001  
1111

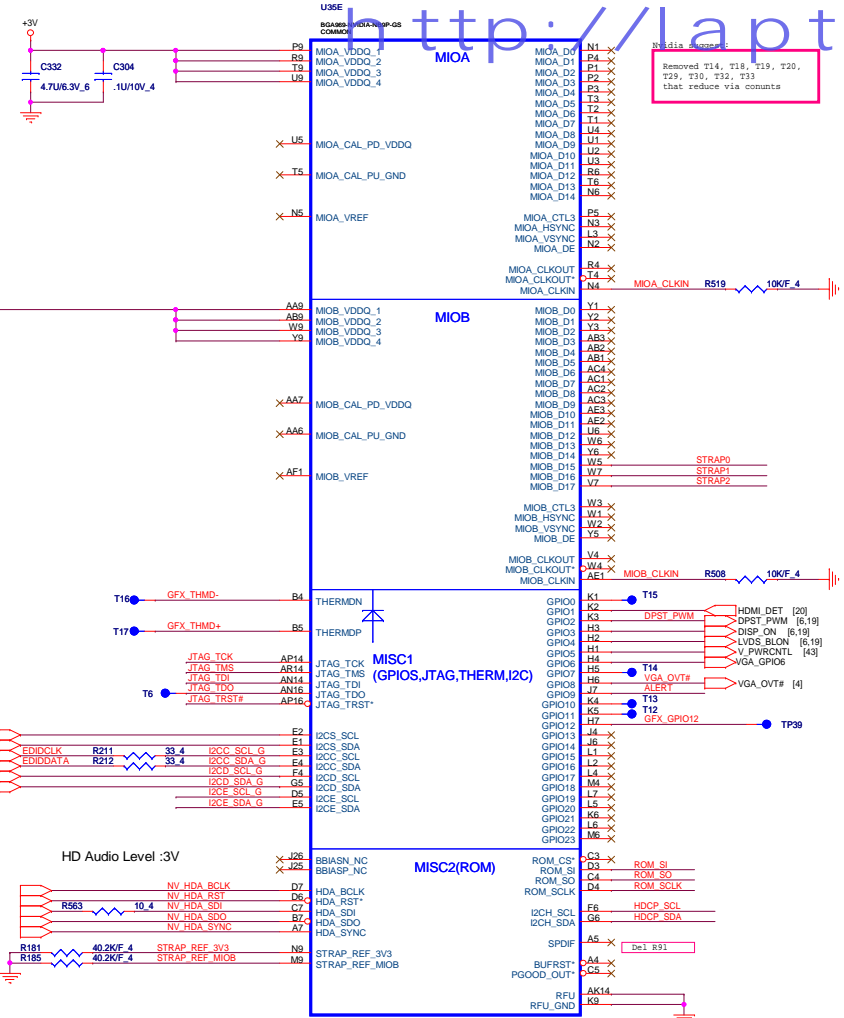
## PCI\_DEVID: STRAP2

NB9M-GE 0x06E 8 1000 default  
NB9M-GS 0x06E 9 1001  
NB9P-GE2 0x064 8 1000  
NB9P-GS 0x064 9 1001 default

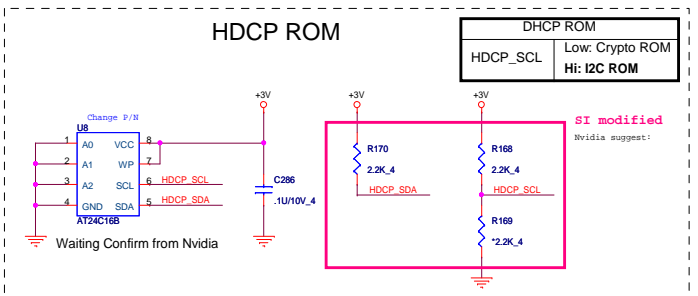
CS33572FB13 RES CHIP 35.7K 1/16W +-1%(0402)

NB9X VRAM Configuration Table

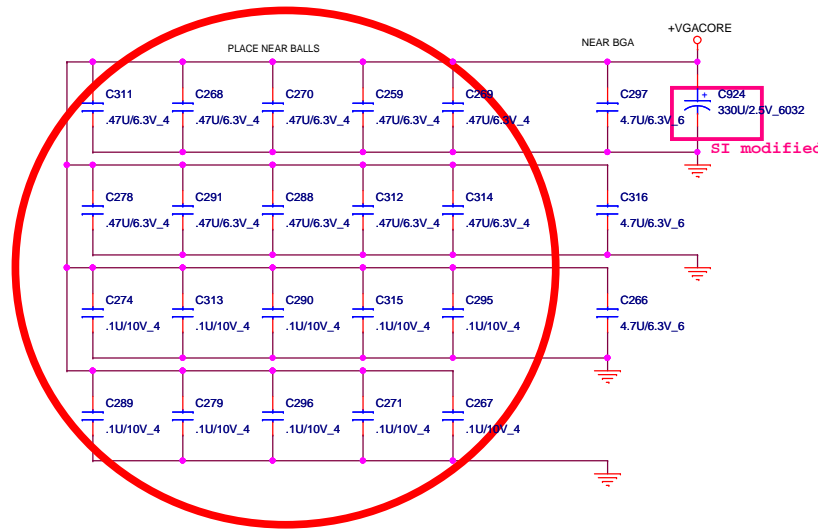
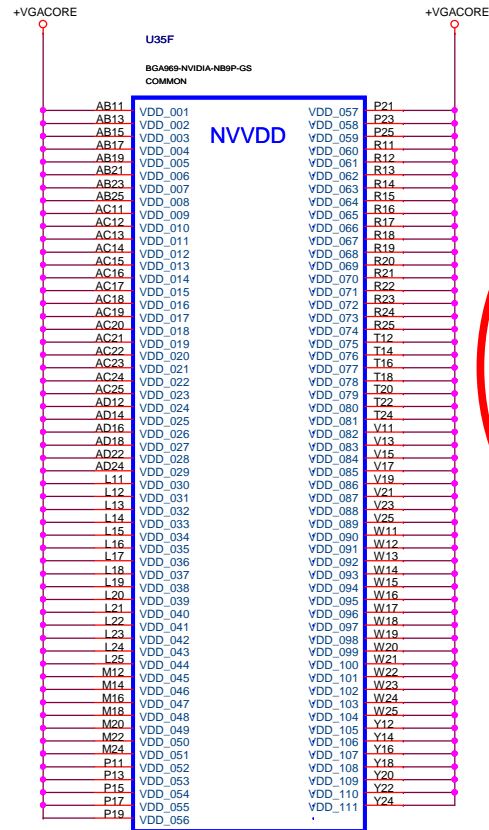
RAM_CFG[3:0]	DESCRIPTION	Vendor
0111	DDR2 32Mx16x8, 128bit, 512MB	Hynix HY5PS12162TQFP-25
0110	DDR2 32Mx16x8, 128bit, 512MB	Qimonda HYB18T512161B2P-25
0101	DDR2 32Mx16x8, 128bit, 512MB	Samsung K4N51163QE-ZC25
0100	DDR2 32Mx16x8, 128bit, 512MB	Nanya/Elipda
0000	DDR2 64Mx16x8, 128bit, 1GB	Hynix
0001	DDR2 64Mx16x8, 128bit, 1GB	Samsung
0010	DDR2 64Mx16x8, 128bit, 1GB	Qimonda



Delete VGA thermal circuit



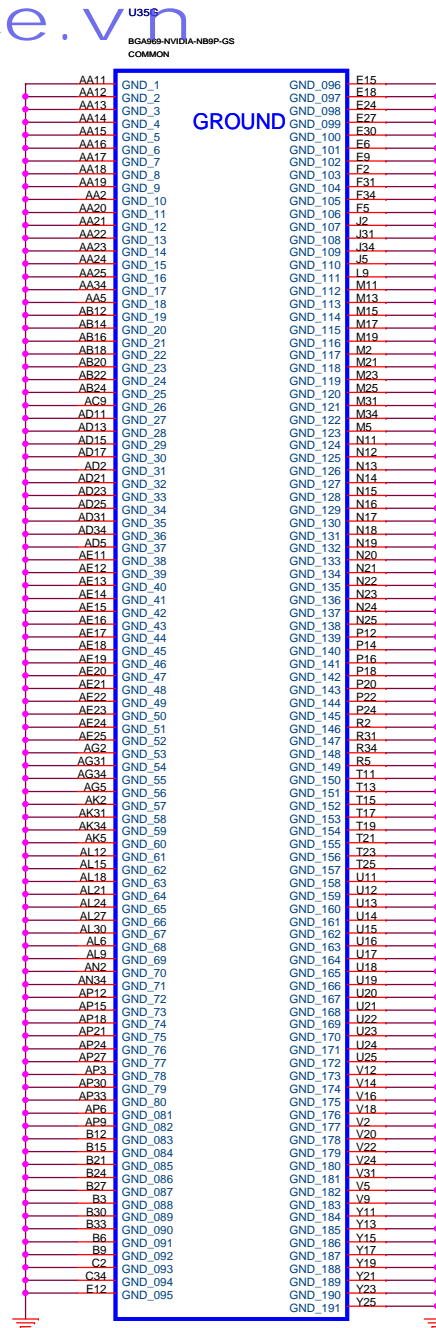
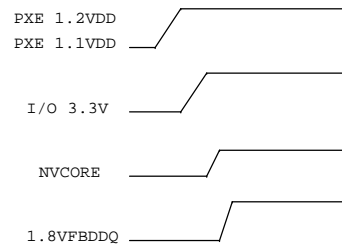
# NVVDD Decoupling

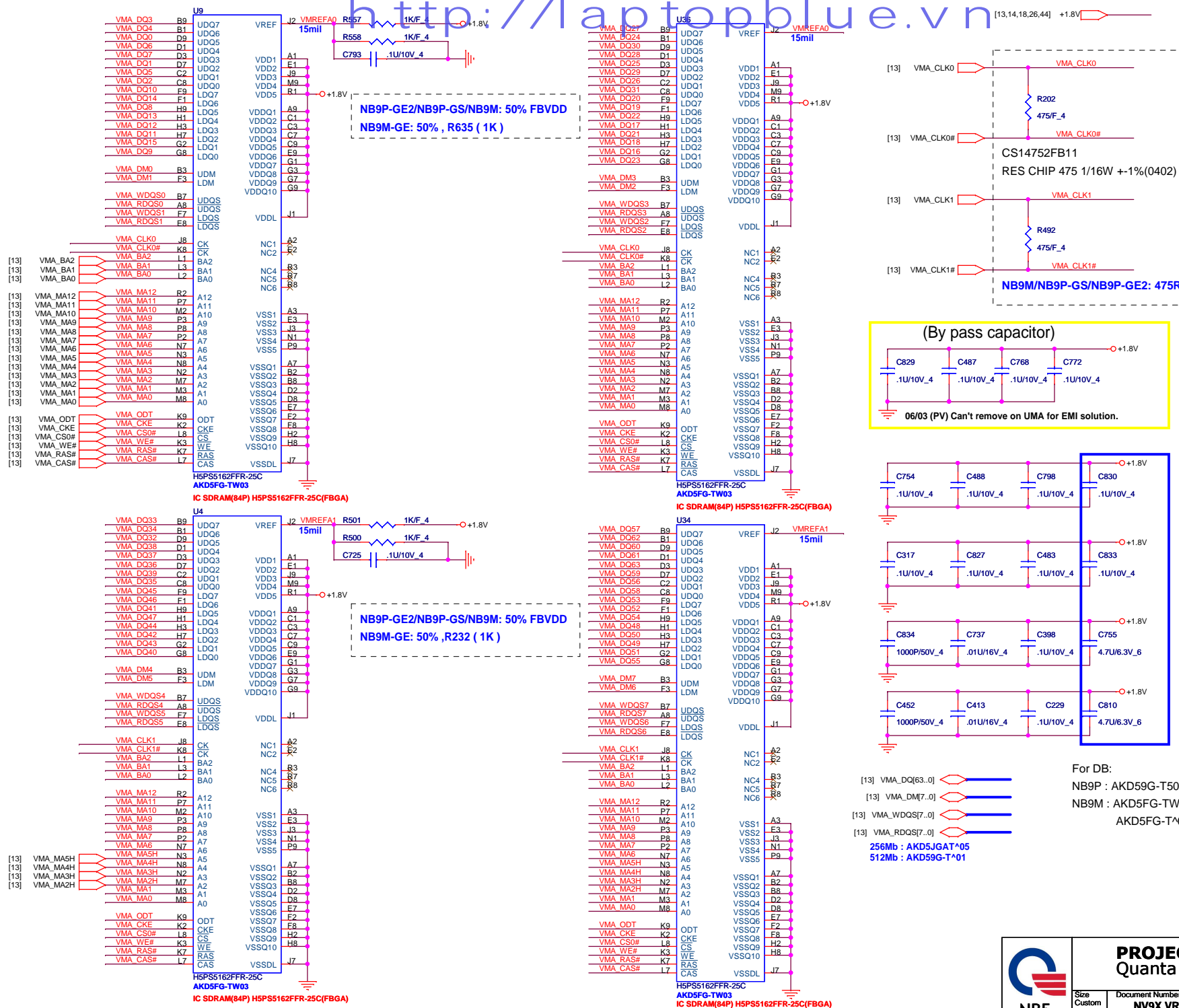


Follow Design Guide DG-03276-001 4.7uF x3  
and 0.47x10 uF instead of 0.1uF x10

NB9M: VGACORE +0.90V (Normal) , +1.09V

## power up sequence





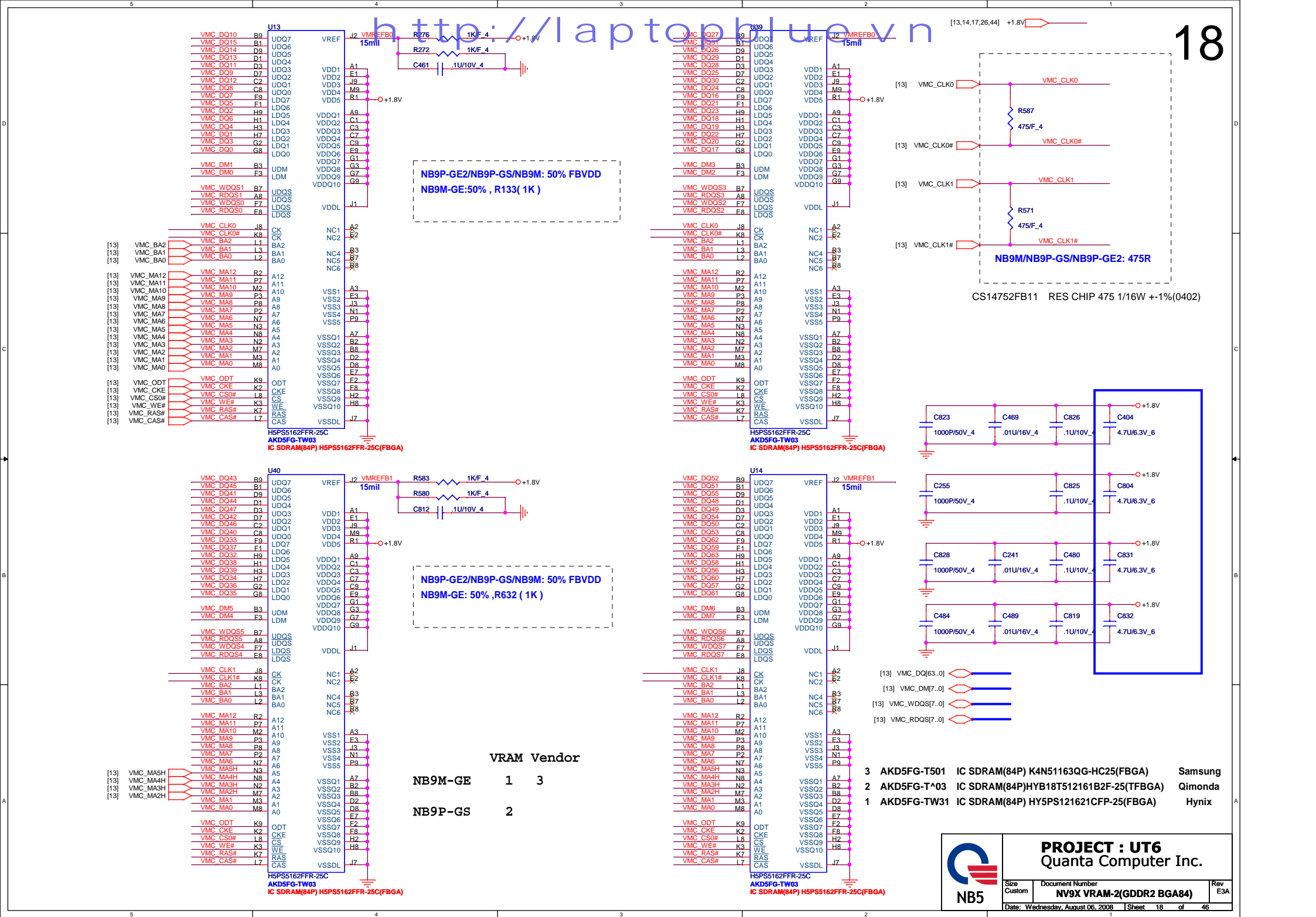
For DB:  
NB9P : AKD59G-T502(Samsung,32M\*16)  
NB9M : AKD5FG-TW31(Hynix,32M\*16)  
AKD5FG-T^03(Qimonda 32M\*16)

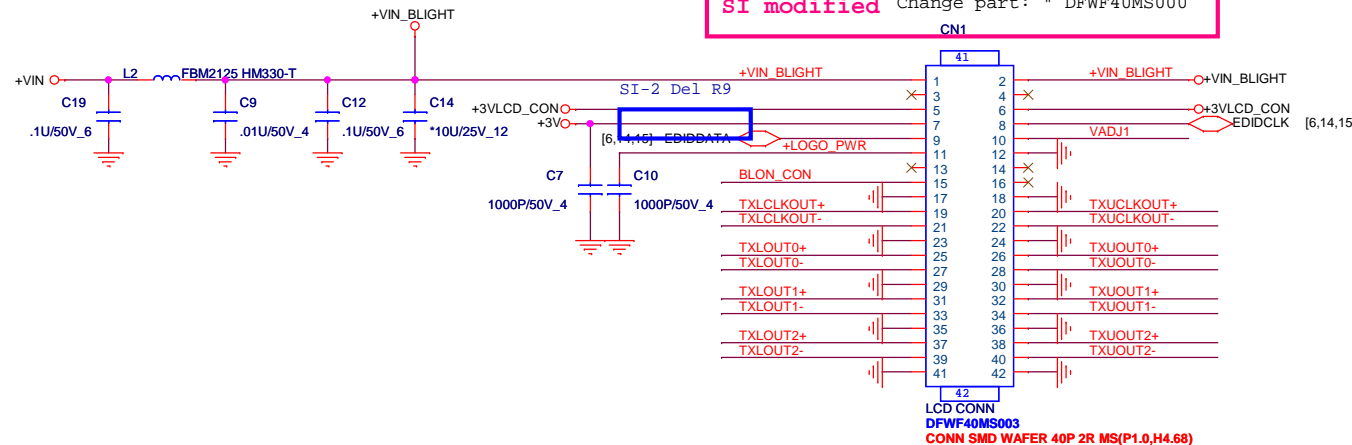
256Mb : AKD5JGAT^05  
512Mb : AKD59G-T^01



**PROJECT : UT6**  
Quanta Computer Inc.

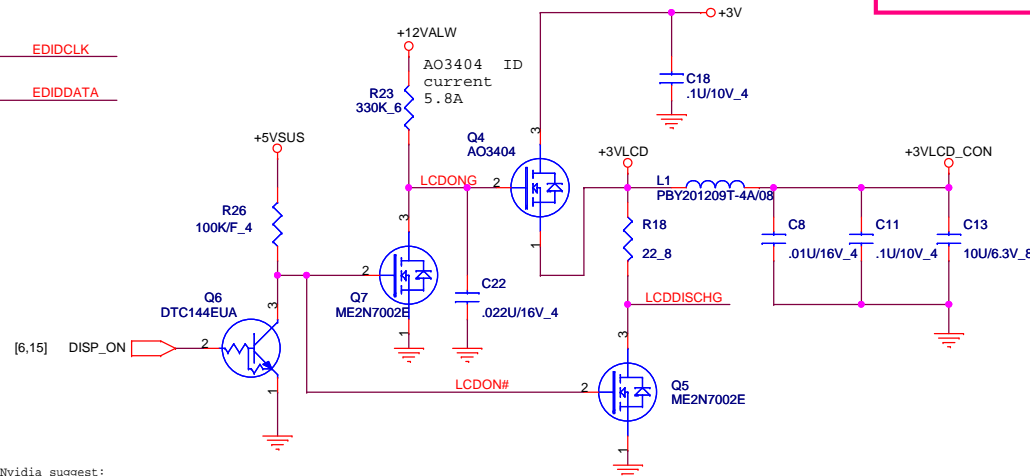
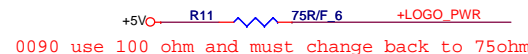
Size Custom	Document Number <b>NV9X VRAM-1(GDDR2 BGA84)</b>	Rev E3A
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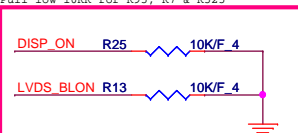


SI modified

```
Del CN7,R88,C115
Remove Logo light2
```

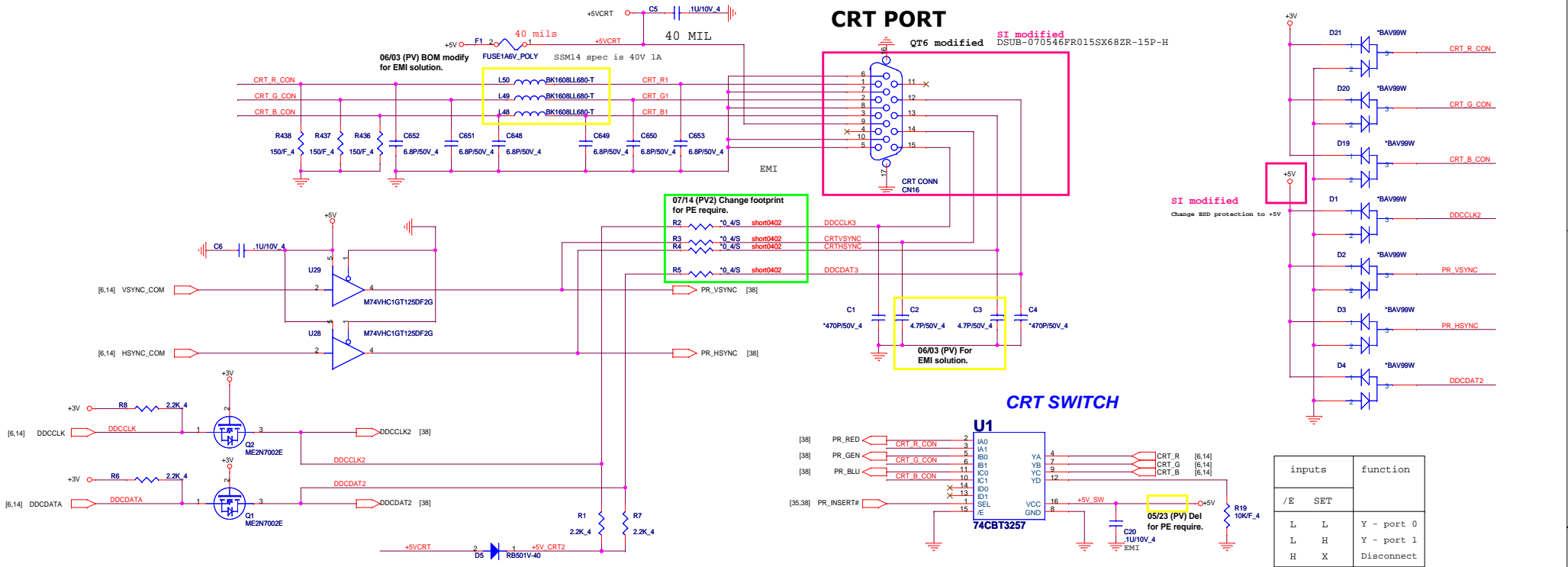


Nvidia suggest:  
Pull low 10KR for R95, R7 & R525

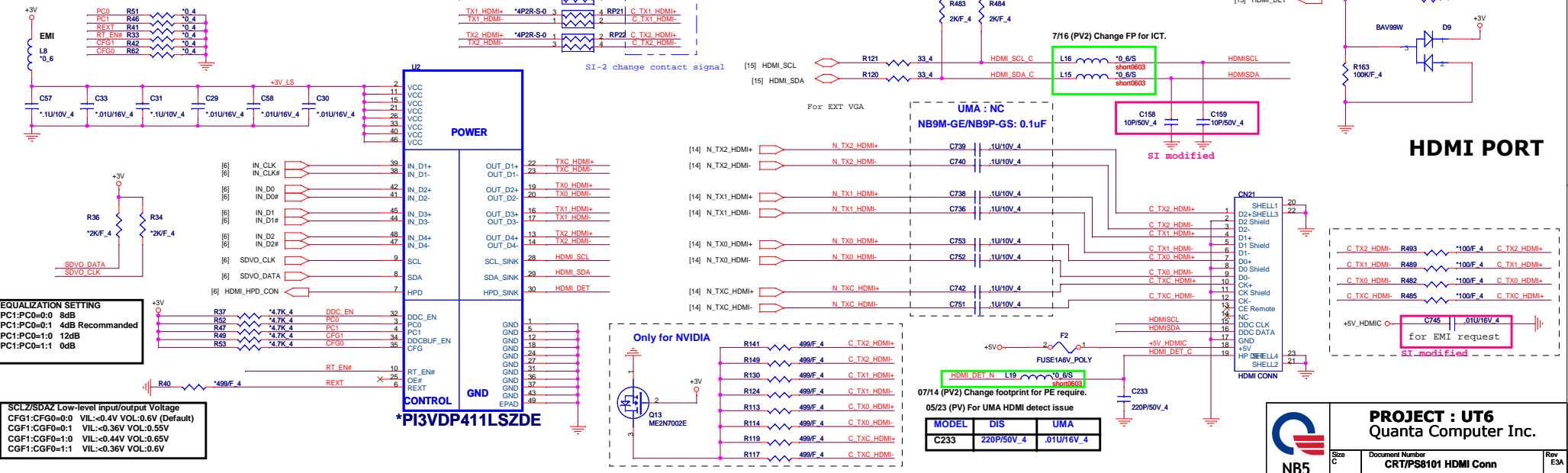


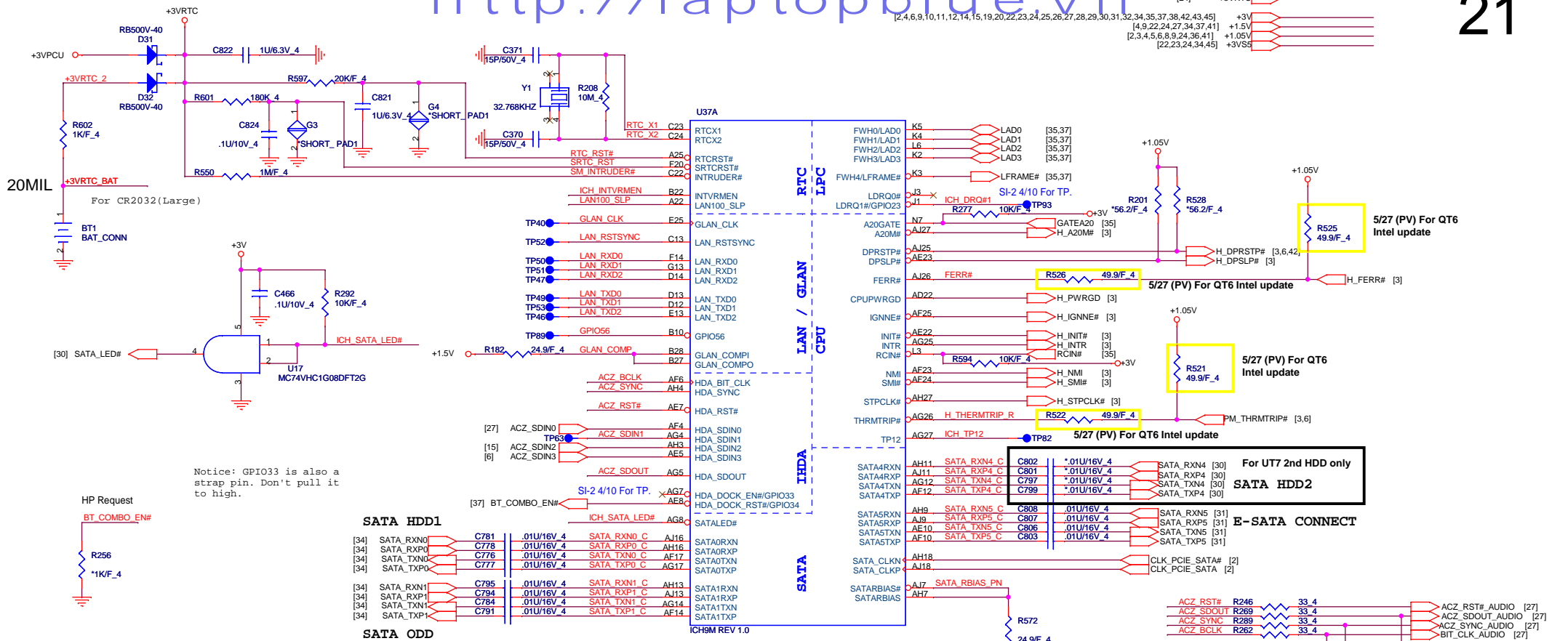
**PROJECT : UT6**  
Quanta Computer Inc.

Size B	Document Number <b>LCD CONN/Lid function</b>	Rev E3
Date: Wednesday, August 06, 2008		Sheet 19 of 46



## For UMA HDMI function





## SB Strap

**ICH9-M Internal VR Enable strap**  
(Internal VR for VccSus1\_05, VccSus1\_5 and VccCL1\_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)
LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

## XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIE port config bit 1

## ICH9 Boot BIOS select

STRAP	PCI_GNT0#	SPI_CS#1
SPI	0	1
PCI	1	0
LPC	1	1

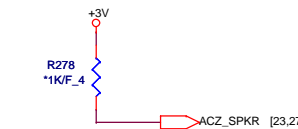
(default)



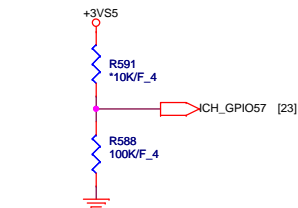
A16 swap override strap	
PCI_GNT#3	Low = A16 swap override enabled Hi = Default



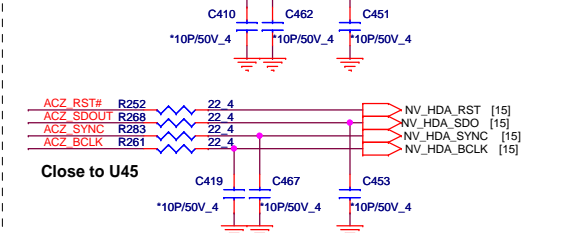
No Reboot Strap	
ACZ_SPKR	Low: Default Hi: No reboot



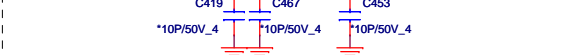
TPM physical presence	
ICH_GPIO57	Low: Default



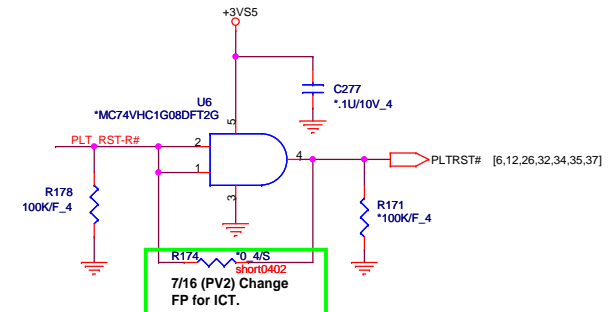
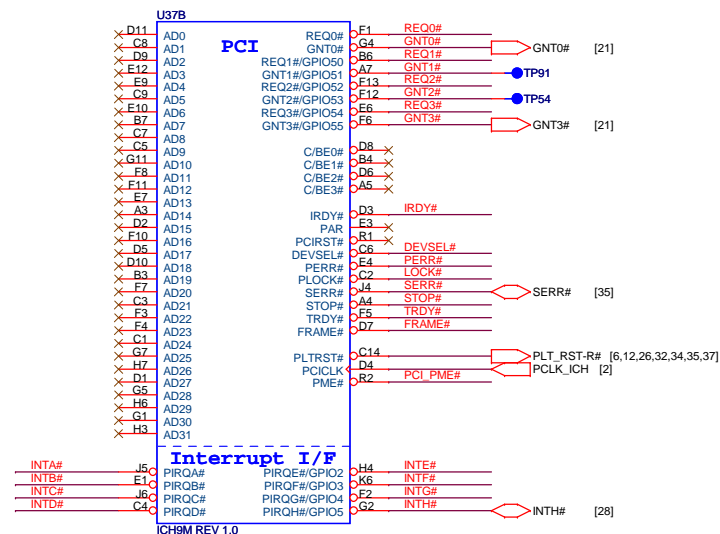
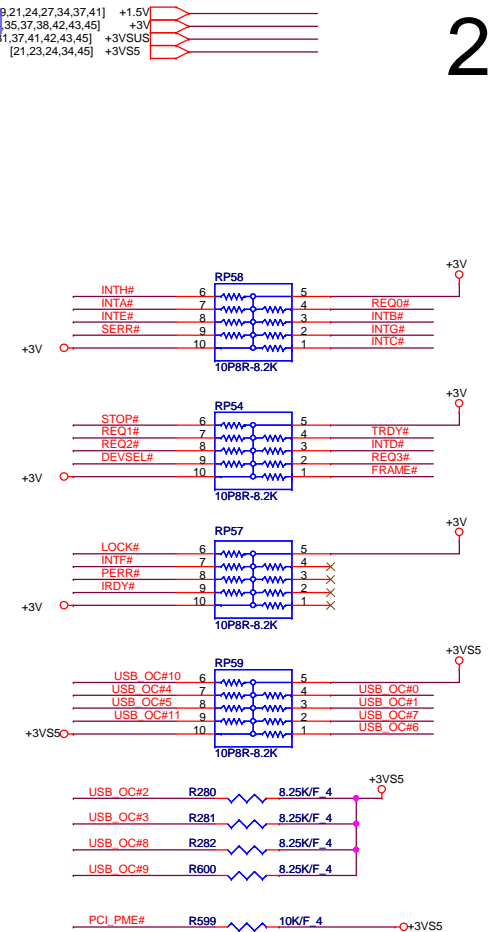
For GM UMA only				
ACZ_RST#	R242	*33_4	ACZ_RST#_MCH	[6]
ACZ_SDOUT	R266	*33_4	ACZ_SDOUT_MCH	[6]
ACZ_SYNC	R274	*33_4	ACZ_SYNC_MCH	[6]
ACZ_BCLK	R258	*33_4	ACZ_BITCLK_MCH	[6]



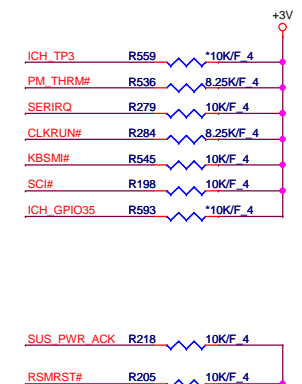
## Close to U45



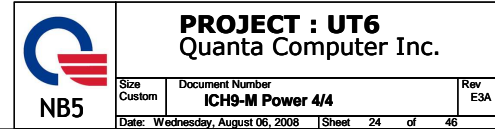
**PROJECT : UT6**  
Quanta Computer Inc.

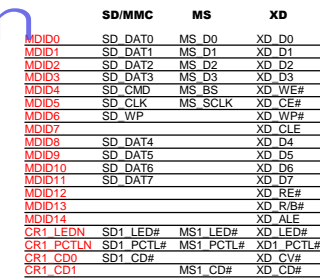


**PROJECT : UT6**  
Quanta Computer Inc.



Board ID 0: 1-->Discrete, 0-->UMA  
Board ID 1: 1-->18.4", 0-->16.0"  
Board ID 2: 1-->MXM, 0-->non-MXM  
Board ID 3: 1-->HDX, 0-->non-HDX  
Board ID 4  
Board ID 5





[26] MC\_PWR\_CTRL\_0#

Q34  
\*ME2307

+3V

+3VCARD

1

3

2

R629

\*10K/F\_4

+5V

20mils

R630

\*0.8S

short0805

+3VCARD

30mils

07/14 (PV2) Change footprint for PE require.



05/23 (PV) For IDT Dolby functionality.  
07/14 (PV2) R697 change footprint for PE require.

06/03 (PV) For EMI solution.  
[31] SUB-MUTE#  
[28,29] DIGITAL\_CLK  
[38] SPDIF  
[31] DIGITAL\_D1

QT6 Modified-0117  
C762,C763 10P

07/14 (PV2) Change footprint for PE require.

Close to Pin1

Close to Pin9

Close to Pin9

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07/14 (PV2) Add R713 for Audio power timing.

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07/14 (PV2) Add R713 for Audio power timing.

IDT  
92HP61B7X5NLGXA1X

IDT  
92HP61B7X5NLGXA1X

IDT  
92HP61B7X5NLGXA1X

IDT  
92HP61B7X5NLGXA1X

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92HP61B7X5NLGXA1X

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92HP61B7X5NLGXA1X

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92HP61B7X5NLGXA1X

IDT  
92HP61B7X5NLGXA1X

IDT  
92HP61B7X5NLGXA1X

Close to Pin38

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07/14 (PV2) Add R713 for Audio power timing.

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07/14 (PV2) Add R713 for Audio power timing.

05/12 (PV) FOR EMI Solution

PORT	PLACE TO
MONO_OUT	X
PORT A	HP OUT
PORT B	M/B MIC
PORT C	X
PORT D	Internal Speckers
PORT E	Docking MIC
PORT F	X
DM	DIGITAL MIC

07/14 (PV2) Change footprint for PE require.

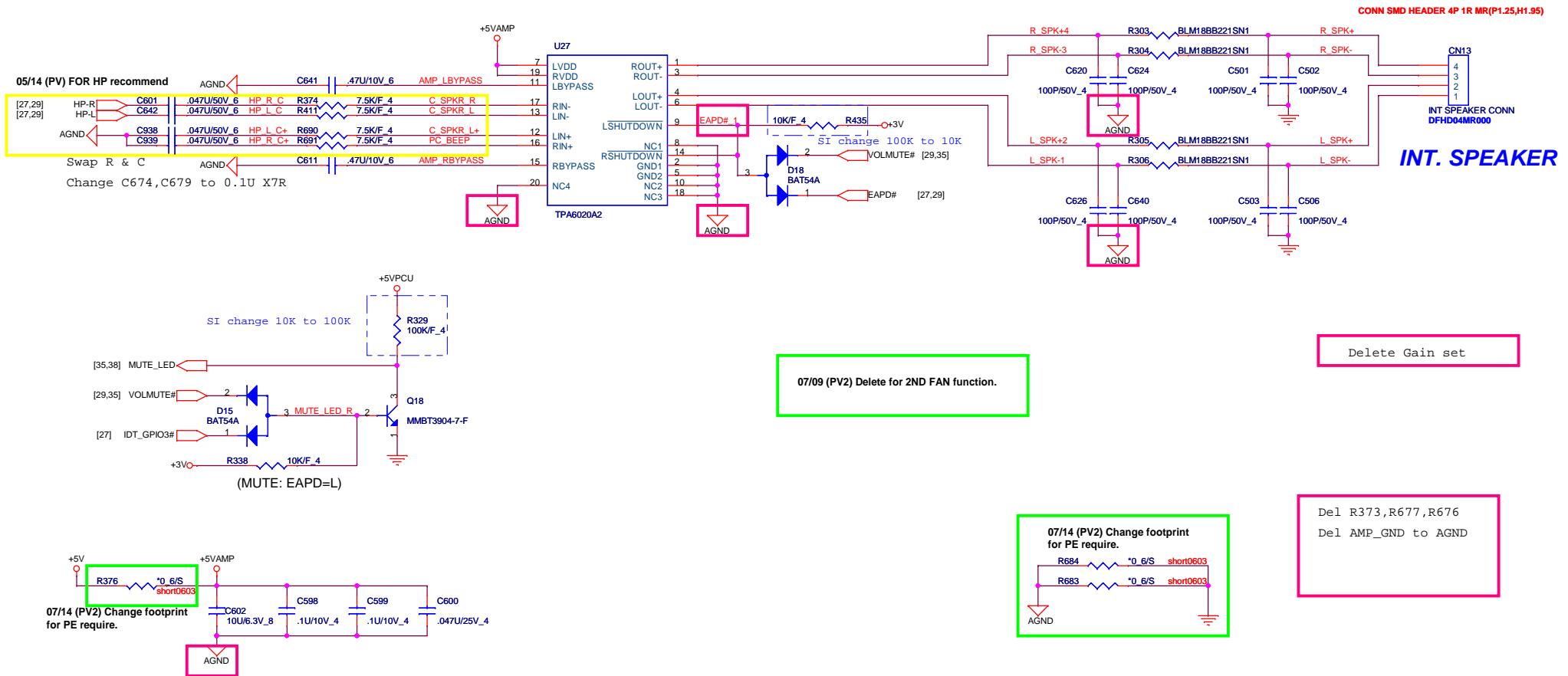
DOCK MIC DETECT

SA\_A# -->EXT HP  
SA\_B# -->EXT MIC  
SB\_E#--> DOCK MIC  
Audio JACK: Normal Open

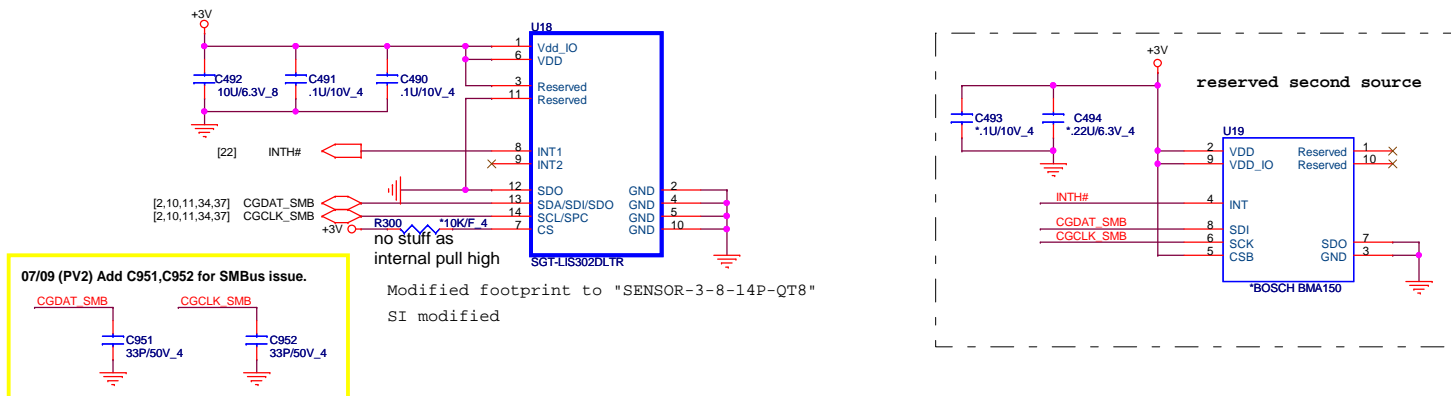
# AUDIO AMPLIFIER

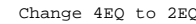
http://tao.pblue.vn

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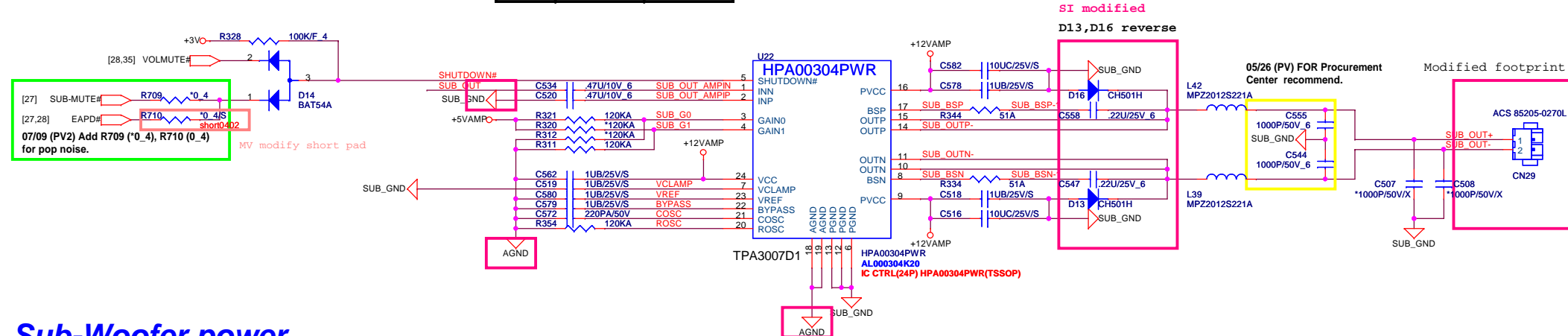


## Accelerometer Sensor

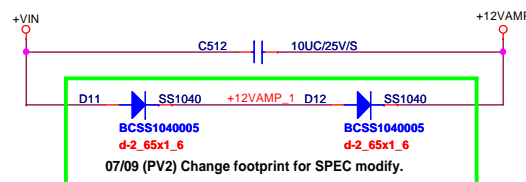




MODEL	UT6	UT7
R316	60.4K/F_6	40.2K/F_6
R319	60.4K/F_6	40.2K/F_6
R330	60.4K/F_6	80.6K/F_6
R314	60.4K/F_6	80.6K/F_6
C509	0.027U/25V_6	0.022U/50V_6
C510	0.027U/25V_6	0.022U/50V_6
C529	0.027U/25V_6	0.039U/16V_6
C543	0.027U/25V_6	0.039U/16V_6

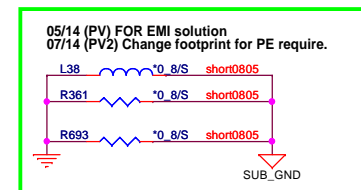


### ***Sub-Woofer power***

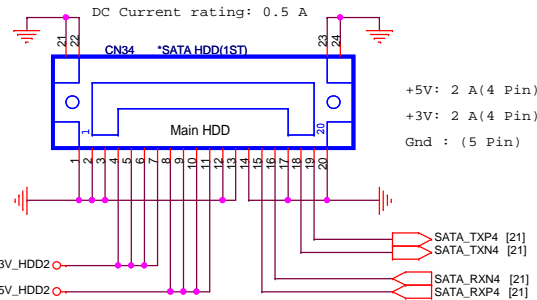


```
Del HP_GND to GND
Del R307,R315
```

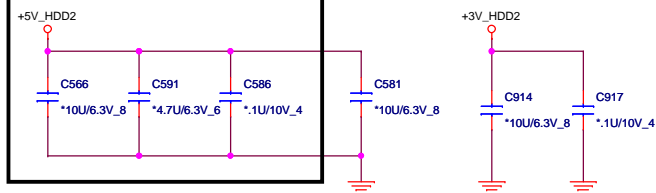
Delete L1003



## SATA\_2 CONNECTOR

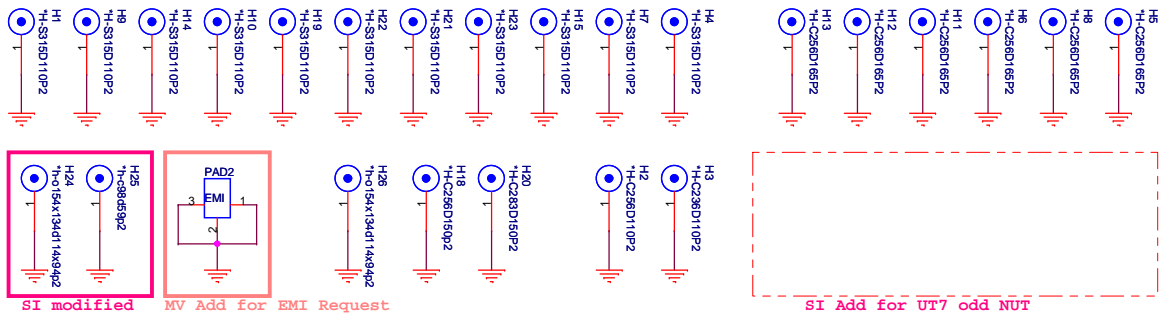


### FOR UT7 2ND HDD ONLY.



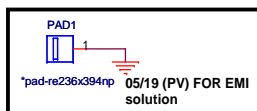
http://tao4topblue.vn

## M/B Screw Hole



delete all PAD & change screw footprint

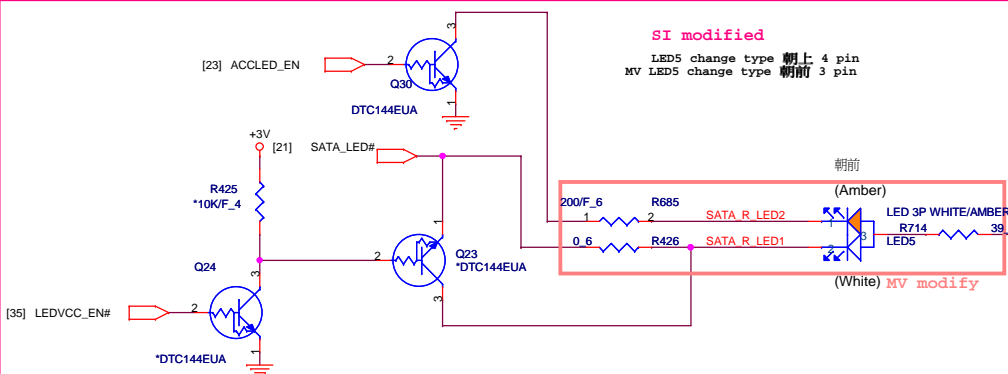
07/14 (PV2) Delete H16,H17 for no support ROBSON card.



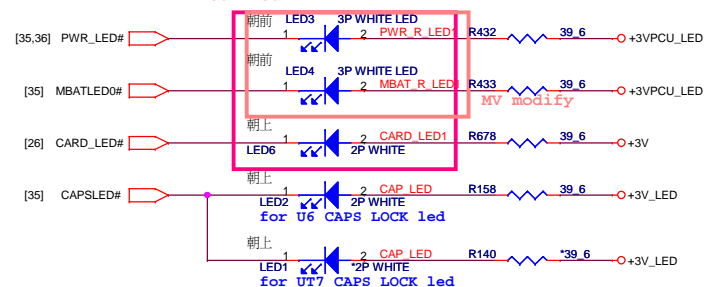
05/19 (PV) FOR M/E recommend for UT7 BAT NUT

SI modified

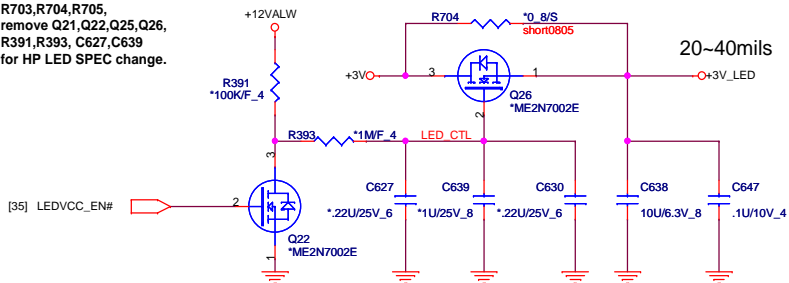
LED5 change type 朝上 4 pin  
MV LED5 change type 朝前 3 pin



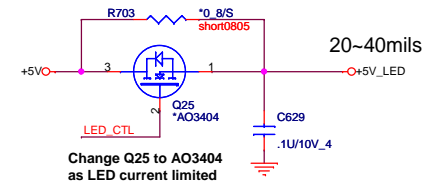
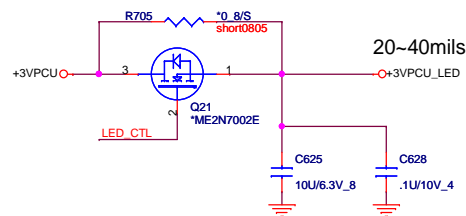
SI modified LED3,4,6 change type 朝上 2 pin



07/09 (PV2) Add  
R703,R704,R705,  
remove Q21,Q22,Q25,Q26,  
R391,R393, C627,C639  
for HP LED SPEC change.

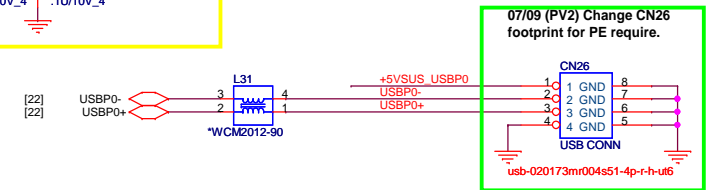
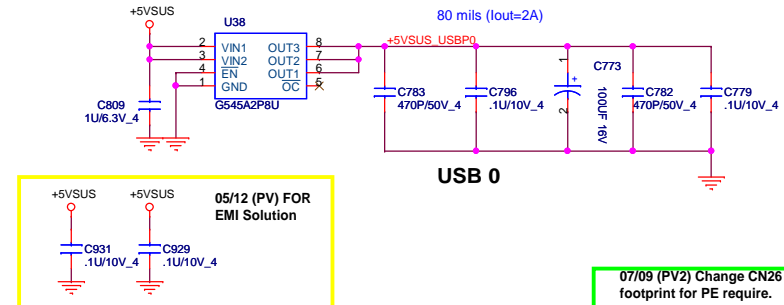
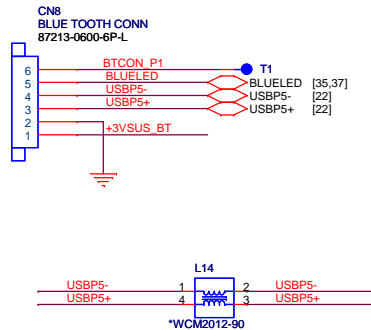
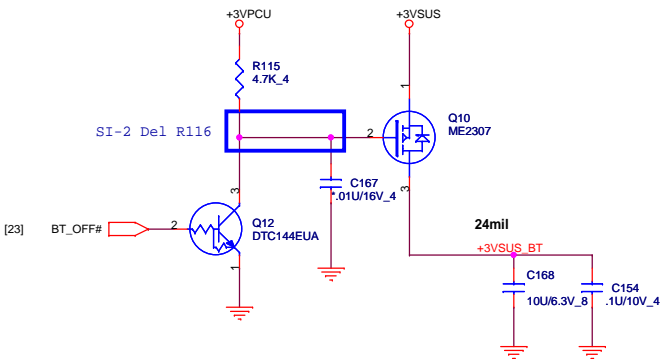


## LED PWR CONTROL

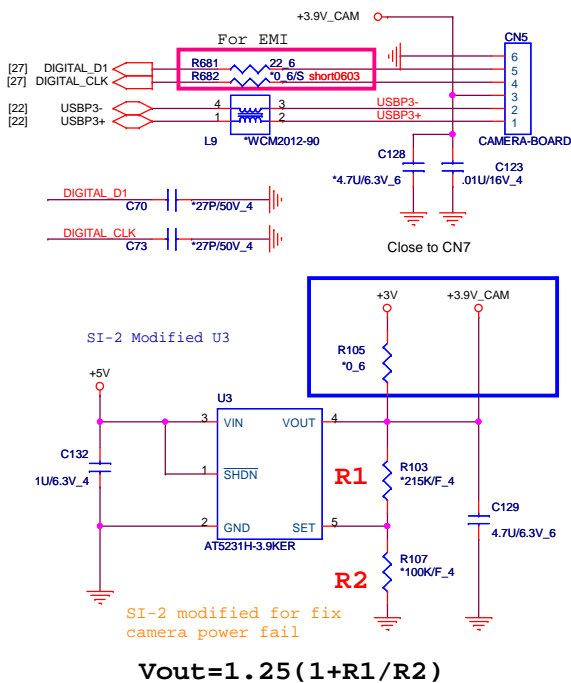


**PROJECT : UT6**  
Quanta Computer Inc.

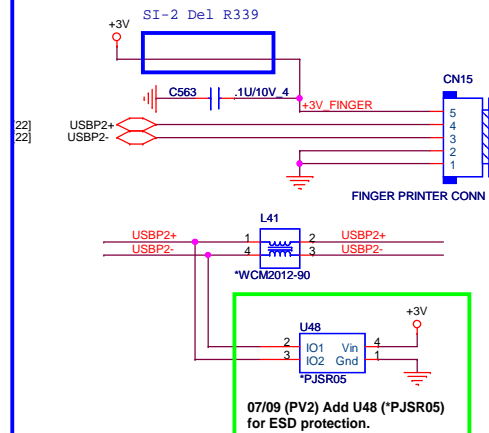
Size	Document Number	Rev
Custom	LED & 2nd HDD & Hole	E3A
Date: Wednesday, August 06, 2008	Sheet 30 of 46	



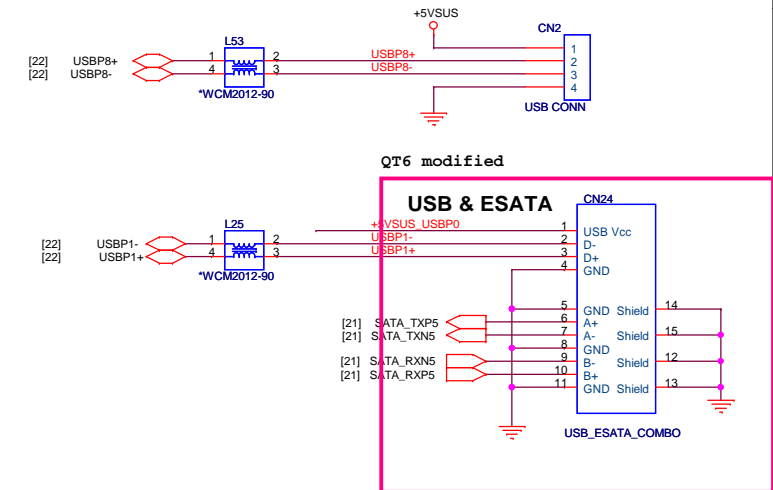
## USB CAMERA /DIGITAL MIC CONNECT



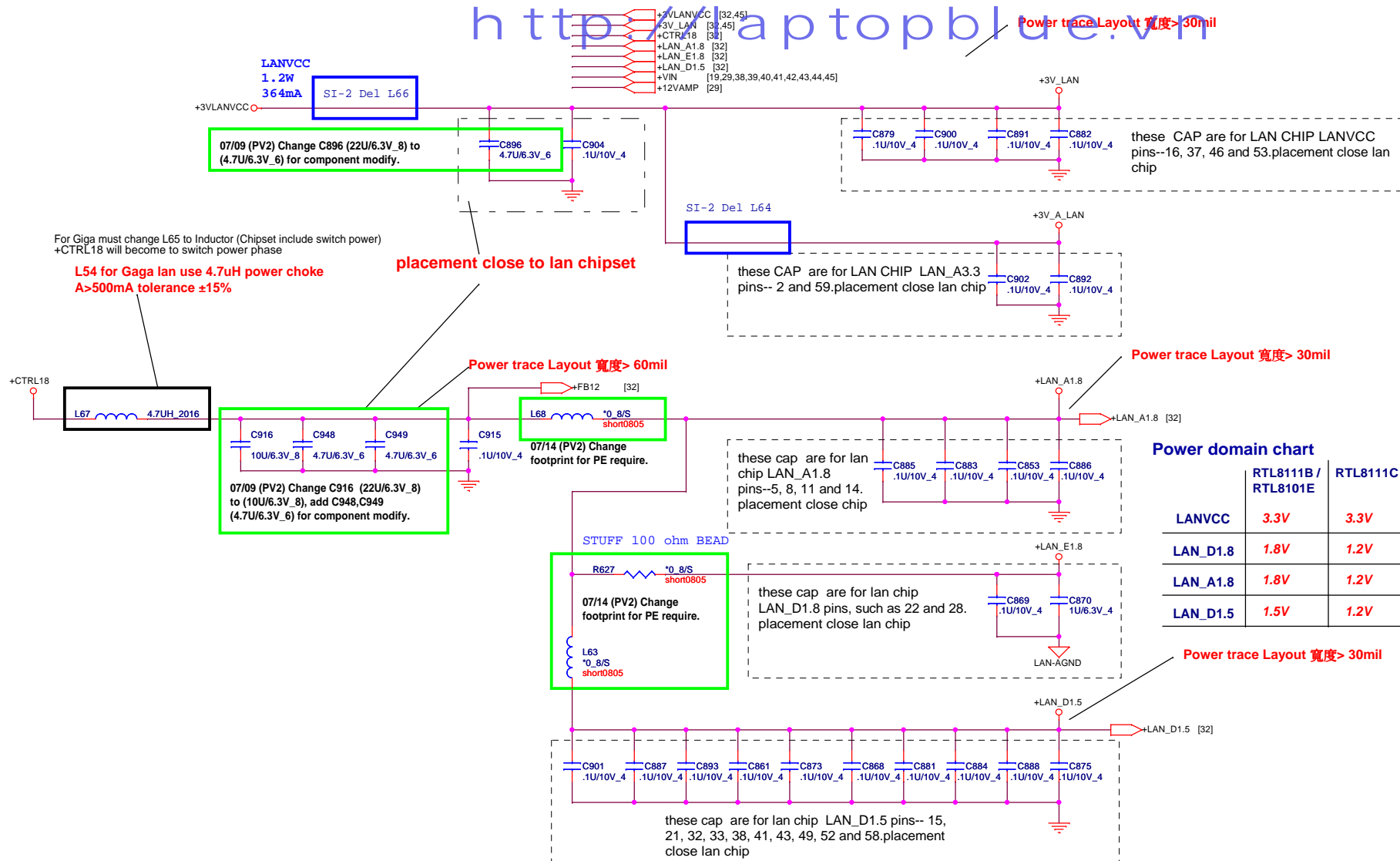
## USB fingerprint CON

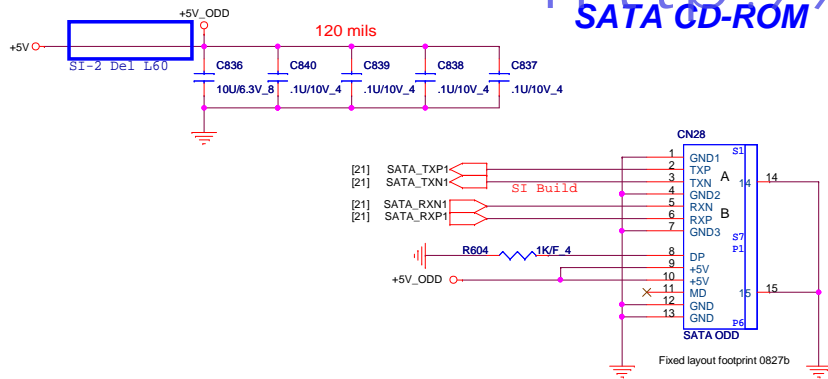


1. ESD GND
2. SYSTEM GND
3. USB-
4. USB+
5. USB PWR(+3V)

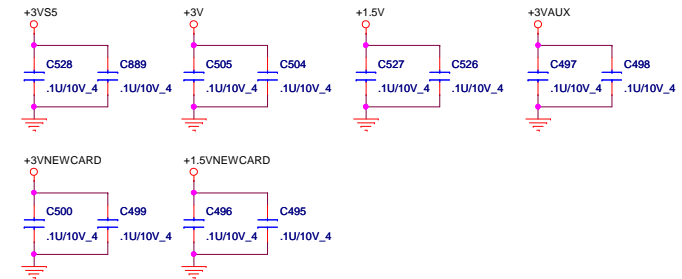
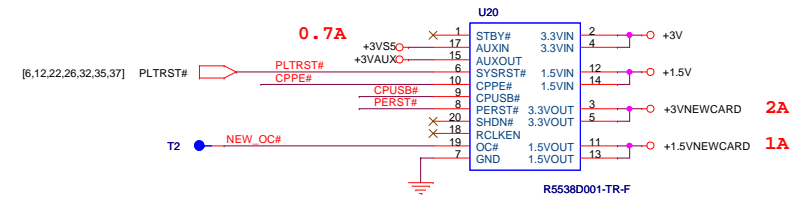
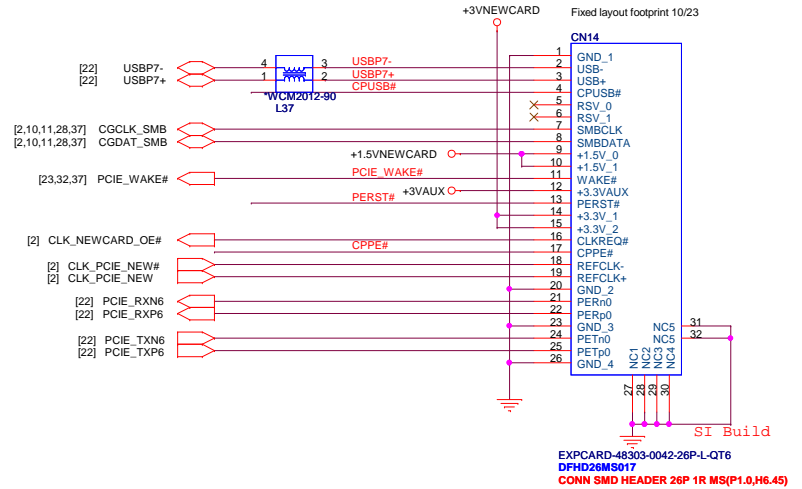
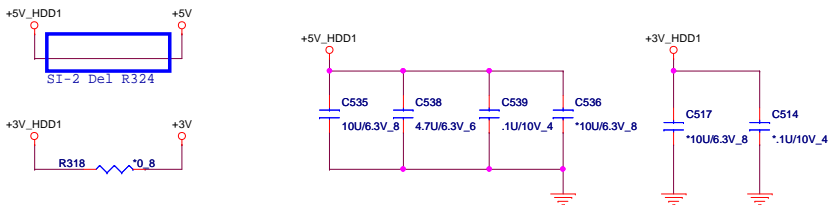
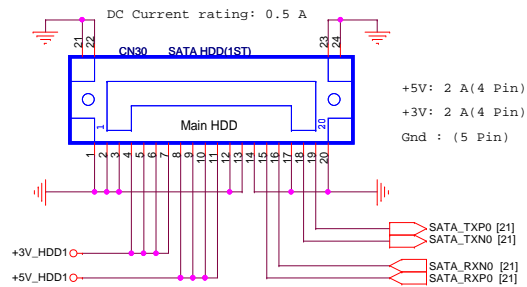




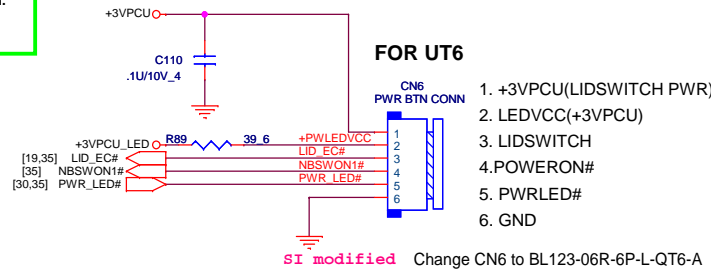
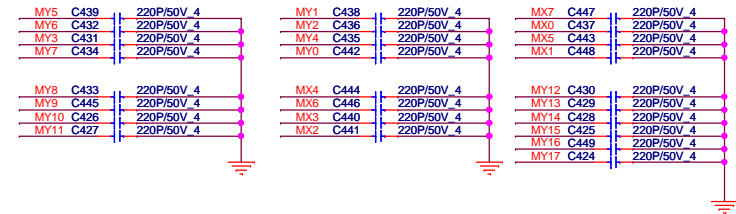
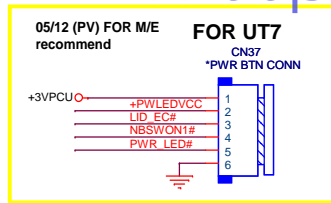
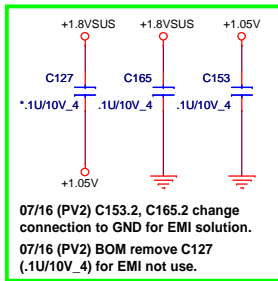




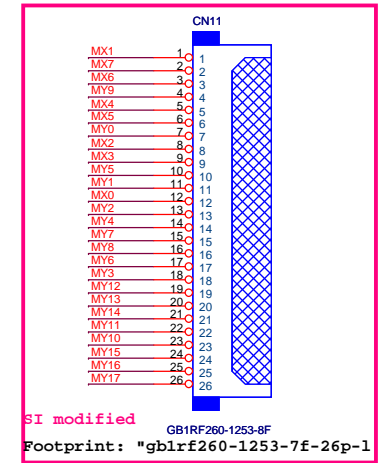
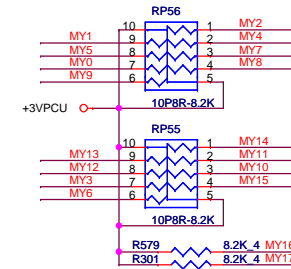
## SATA\_1 CONNECTOR



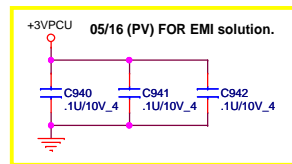
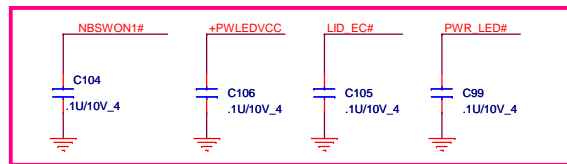




## KEYBOARD PULL-UP

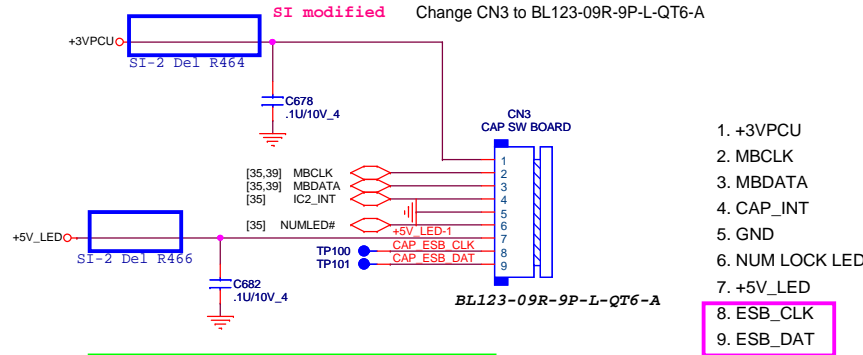


SI modified For EMI

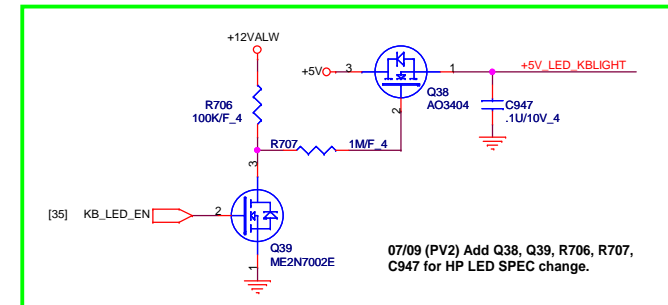
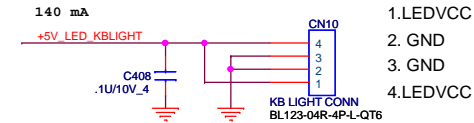
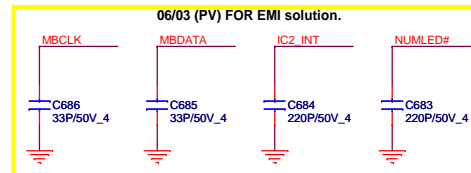


## CAP SW CONNECT

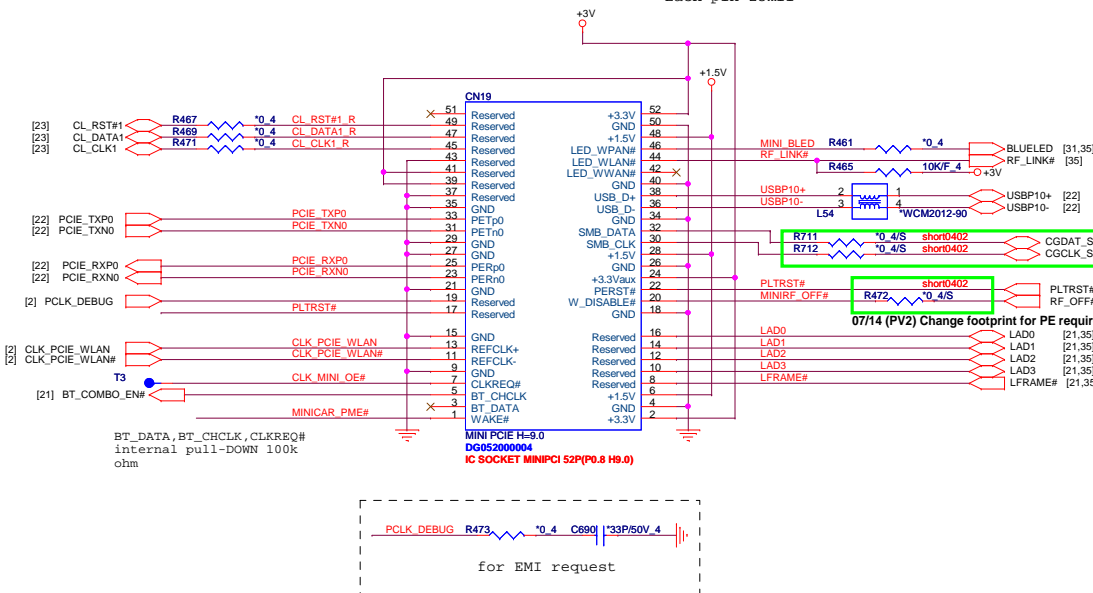
Change CN3 to BL123-09R-9P-L-QT6-A



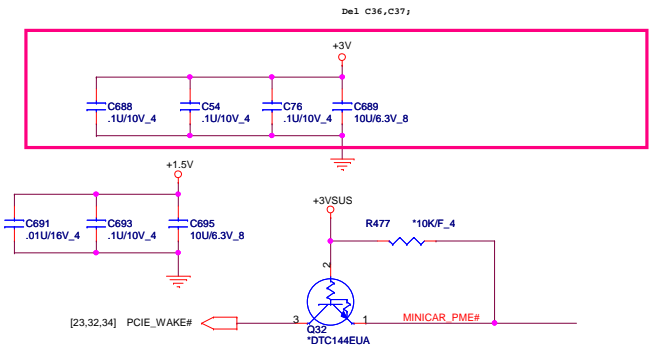
07/14 (PV2) Delete L69,L70,C922,C923 for EMI solution.



## Mini PCI-E Card 1 WLAN



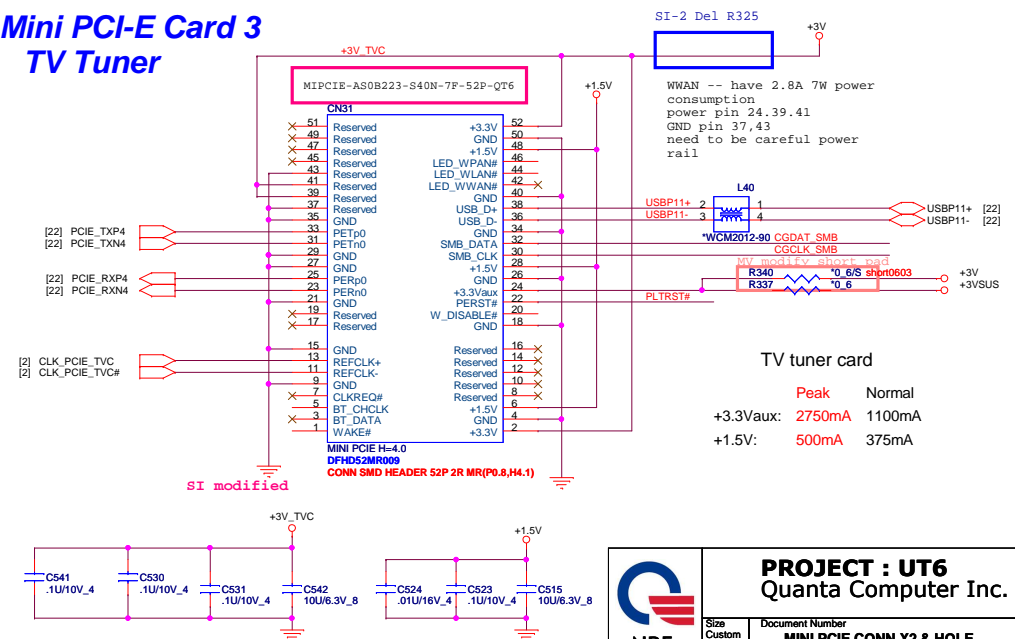
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## Mini PCI-E Card 2 ROBSON

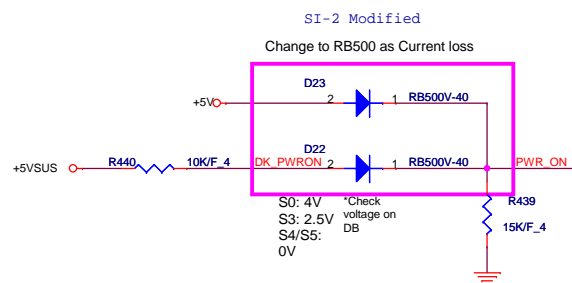
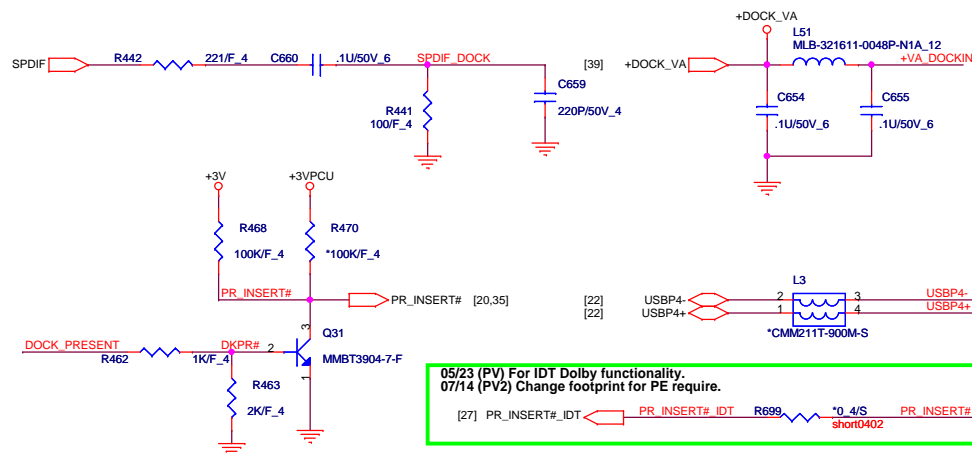
07/09 (PV2) Delete for no support ROBSON card.

## Mini PCI-E Card 3 TV Tuner



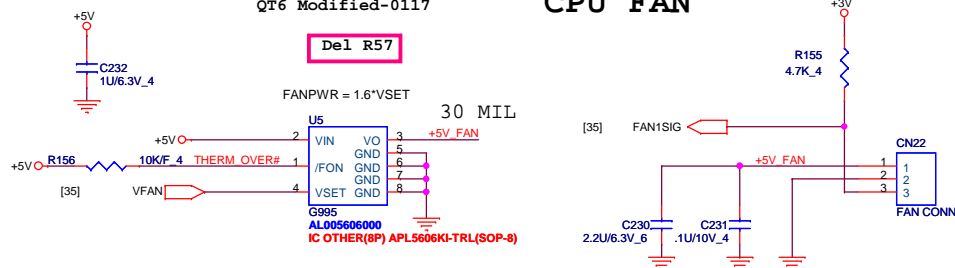
**PROJECT : UT6**  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI PCIE CONN X2 & HOLE	E3A
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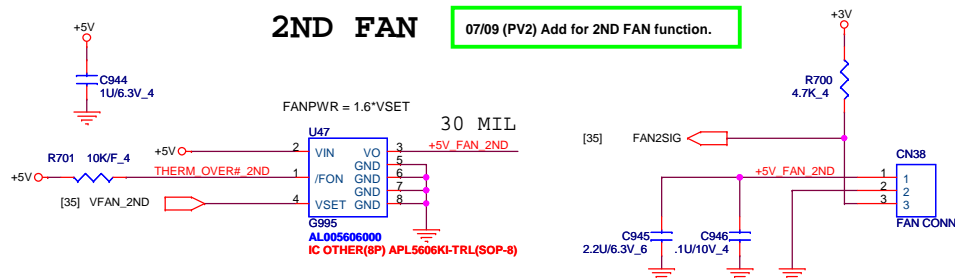
QT6 Modified-0117

CPU FAN

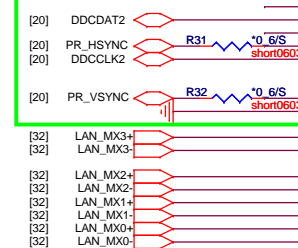


2ND FAN

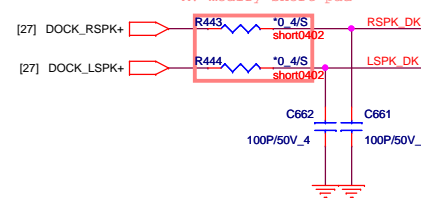
07/09 (PV2) Add for 2ND FAN function.



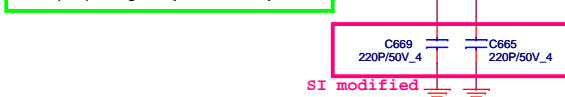
07/14 (PV2) Change footprint for PE require.



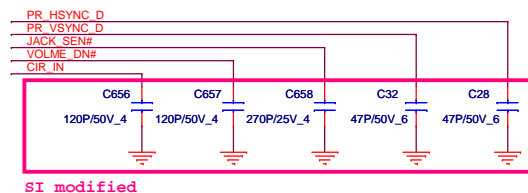
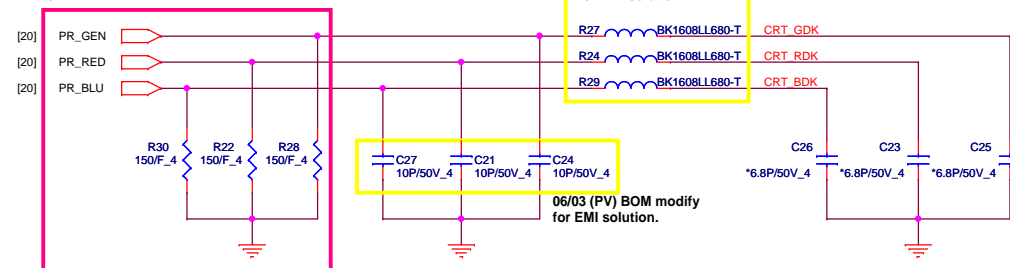
MV modify short pad



07/14 (PV2) Change footprint for PE require.



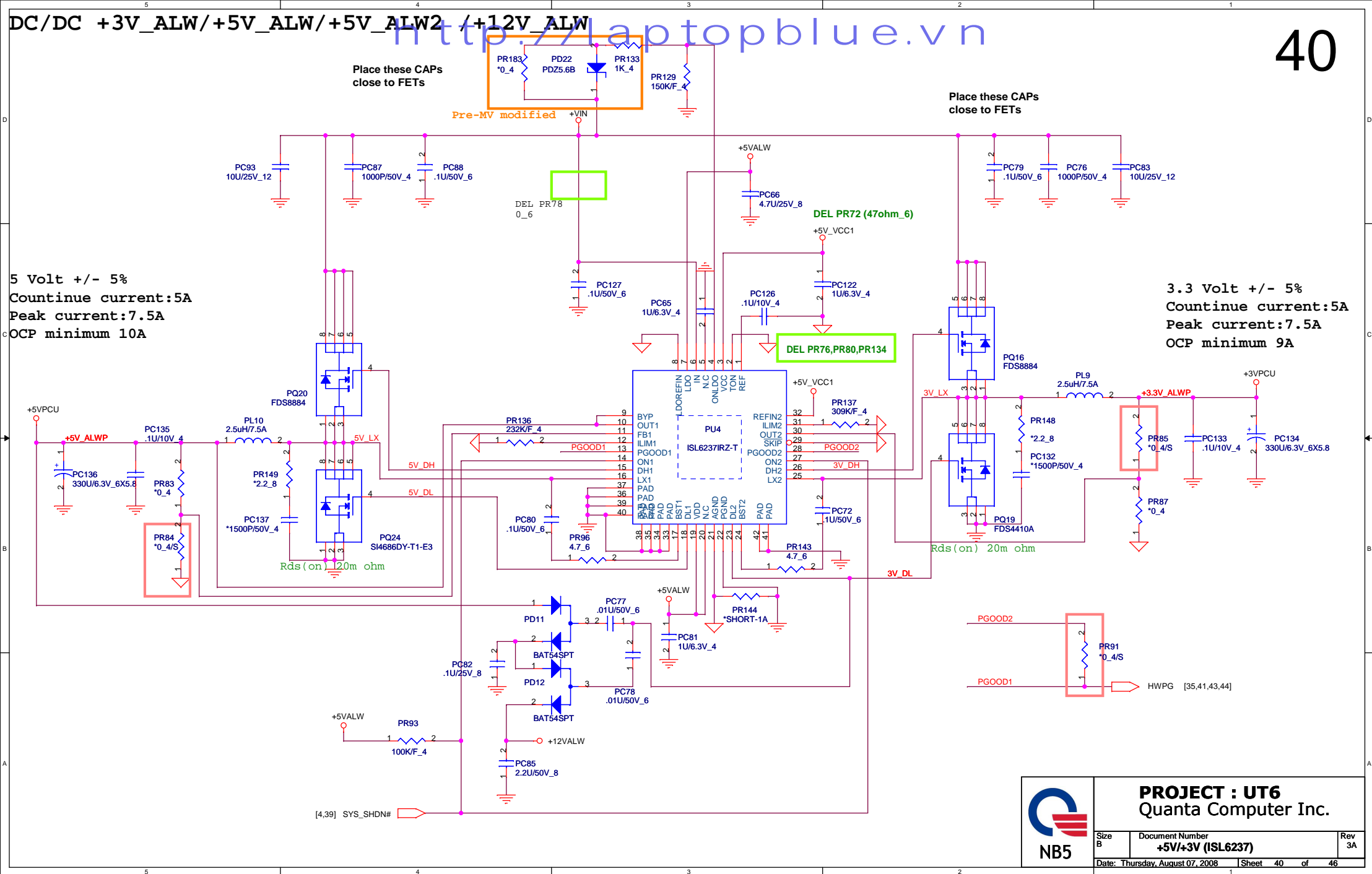
QT6 modified-0117

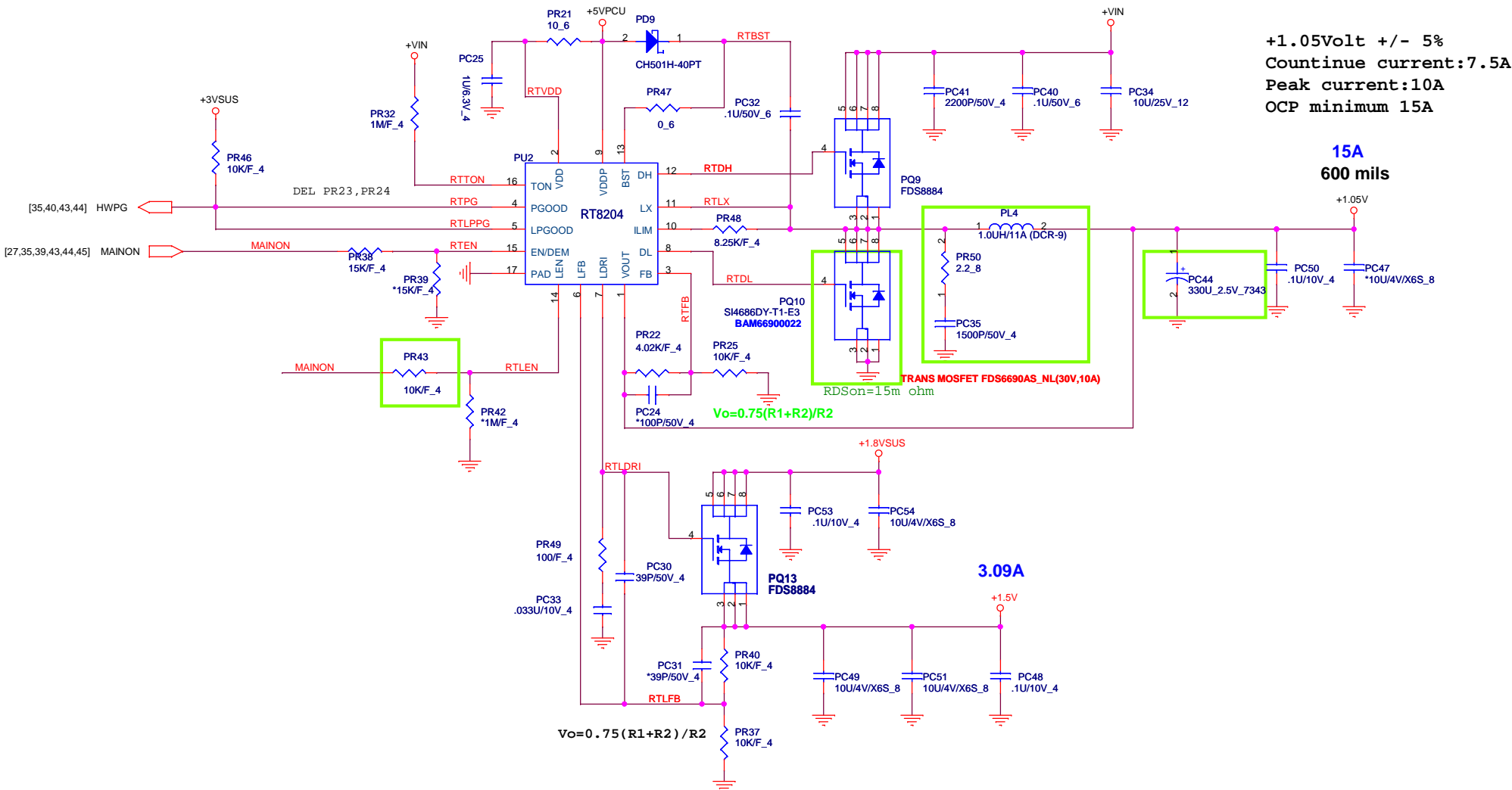


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Size	Document Number	Rev
Custom	CABLE DOCKING/FAN	E3A
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+1.05Volt +/- 5%  
Countinue current:7.5A  
Peak current:10A  
OCP minimum 15A

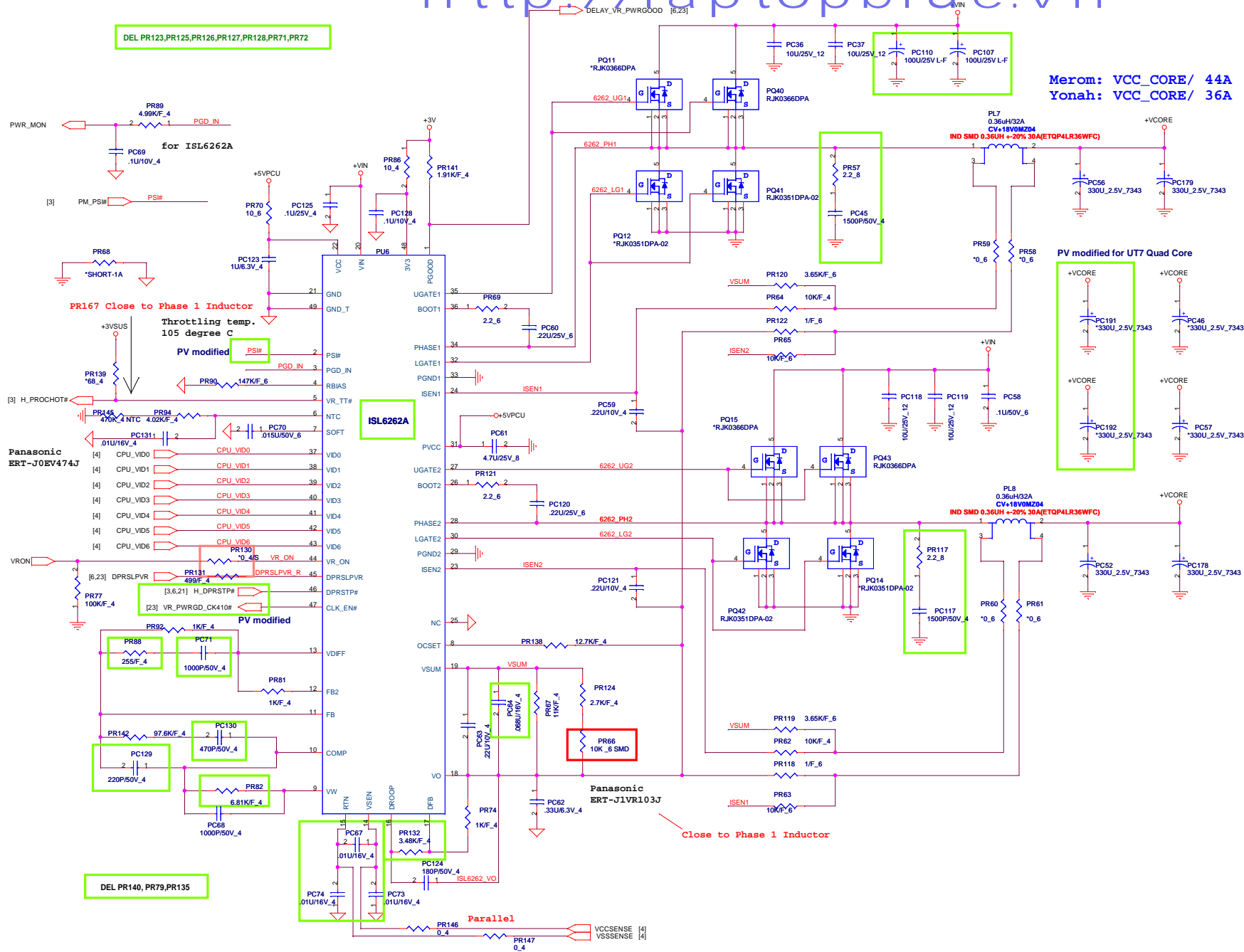
15A  
600 mils

### 3.09A

$$V_o = 0.75(R_1 + R_2) / R_2$$


**PROJECT : UT6**  
Quanta Computer Inc.

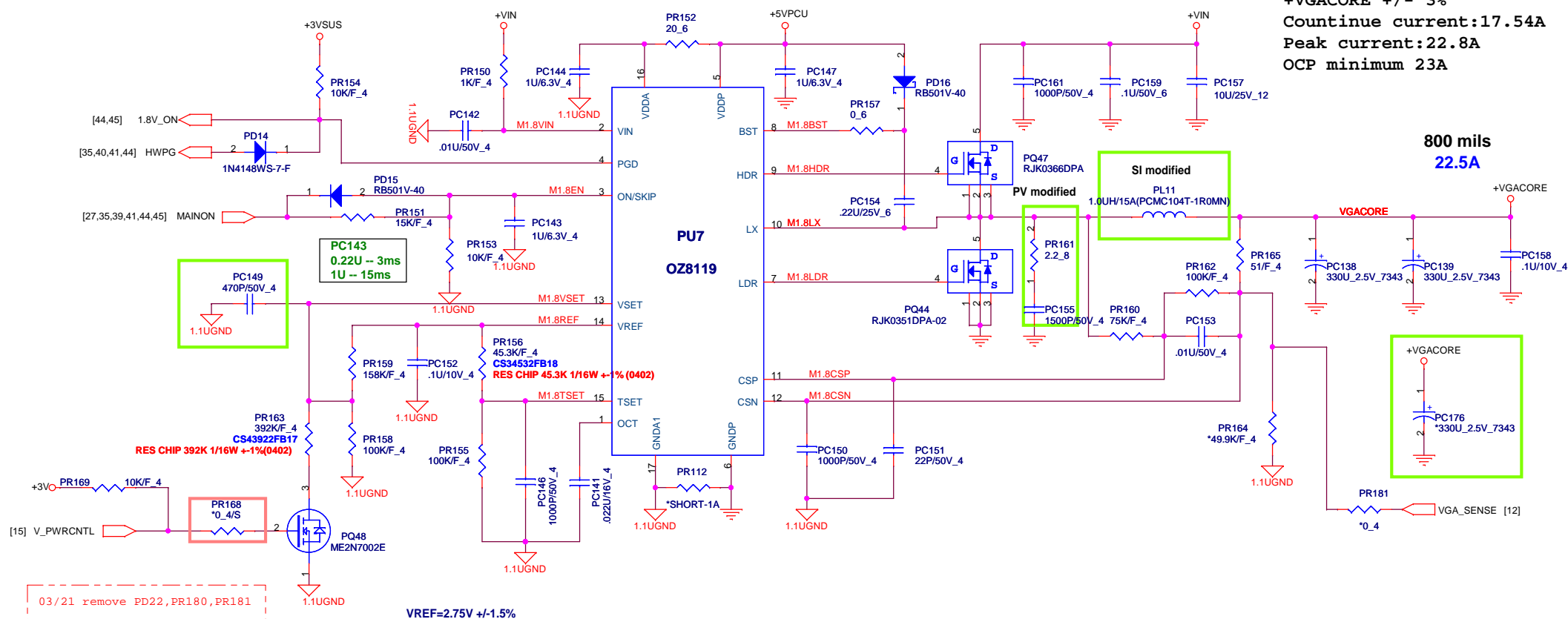
Size B	Document Number <b>+1.05V/+1.5V (RT8204)</b>	Rev 3A
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# VGA Core & VCC1.1

<http://laptopblue.vn>

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+VGACORE +/- 3%  
 Countinue current:17.54A  
 Peak current:22.8A  
 OCP minimum 23A

800 mils  
 22.5A

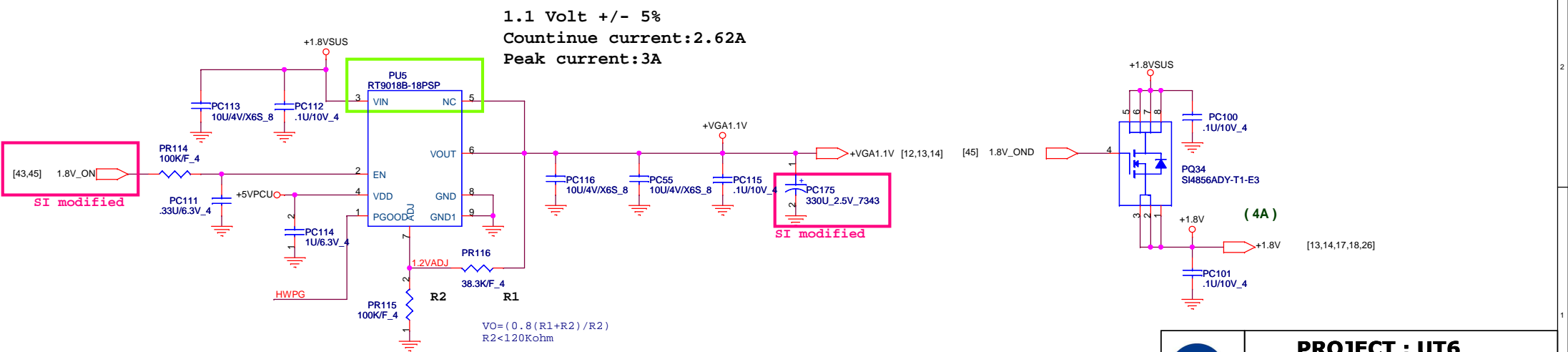
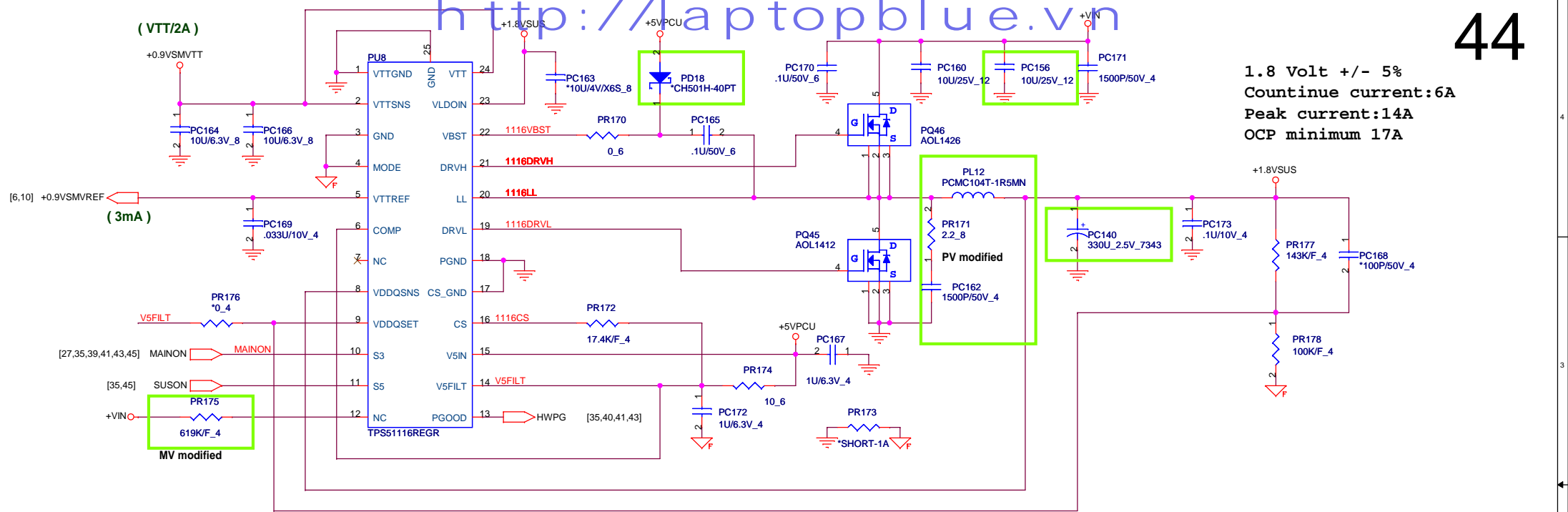
V_PWRCNTL	NB9P-GS
GPIO5	
Low	1.05V
High	0.9V

VGA_GPIO6	V_PWRCNTL		NB9P-GS	NB9M-GE
GPIO6	GPIO5			
Low	Low	MAX BAT	0.9V	0.9V
Low	High	SD DVD	0.9V	0.9V
High	Low	HD DVD	0.9V	0.9V
High	High	MAX PERF	1.05V	1.09V



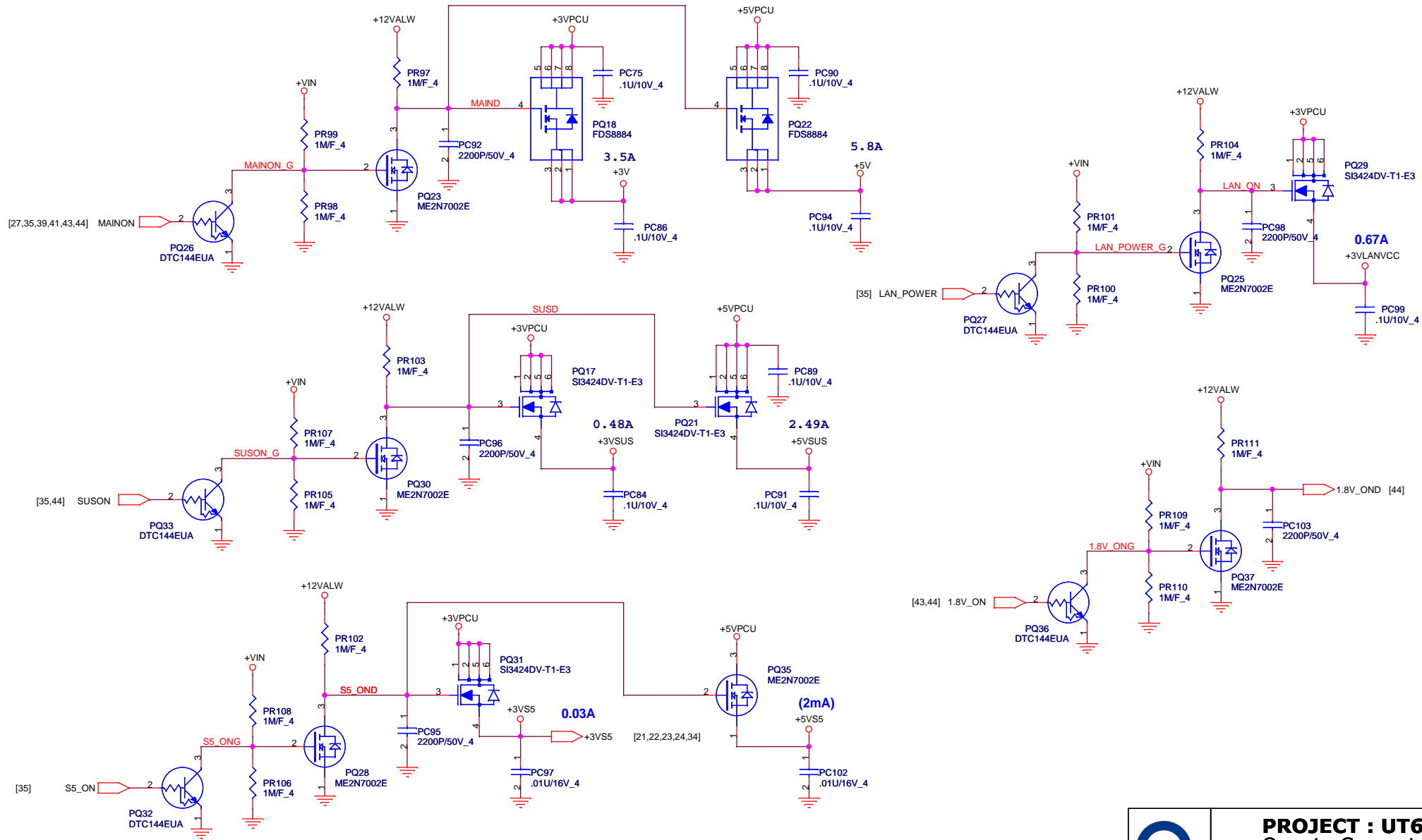
**PROJECT : UT6**  
 Quanta Computer Inc.

Size B	Document Number	Rev
	VGA CORE OZ8118	3A
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**PROJECT : UT6**  
**Quanta Computer Inc.**

Size B	Document Number <b>1.8V/DDR_VTER/+1.8v/+1.1V</b>	Rev 3A
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Quanta Computer Inc.

Size	Document Number	Rev
B	DISCHARGE/3VS5/5VS5/LAN	3A

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	Voltage level	AC MODE				DC MODE			
		S0	S3	S4	S5	S0	S3	S4	S5
+3VPCU	3.3V +/- 5%	V	V	V	V	V	V	V	V
+5VPCU	5V +/- 5%	V	V	V	V	V	V	V	V
+3VRTC	3.3V +/- 5%	V	V	V	V	V	V	V	V
+3VS5	3.3V +/- 5%	V	V	V	V	V	V		
+5VS5	5V +/- 5%	V	V	V	V	V	V		
+3VSUS	3.3V +/- 5%	V	V			V	V		
+5VSUS	5V +/- 5%	V	V			V	V		
+1.8VSUS	1.8V +/- 5%	V	V			V	V		
+0.9VSMVTT	0.9V +/- 5%	V	V			V	V		
+1.5V	1.5V +/- 5%	V				V			
+1.05V	1.05V +/- 5%	V				V			
+VCORE	0.9~1.15V	V				V			
+VGA_CORE	0.9~1.2V	V				V			
+VGA1.1V	1.1V +/- 5%	V				V			
+1.8V	1.8V +/- 5%	V				V			
+3VLAVCC	3.3V +/- 5%	V				V			