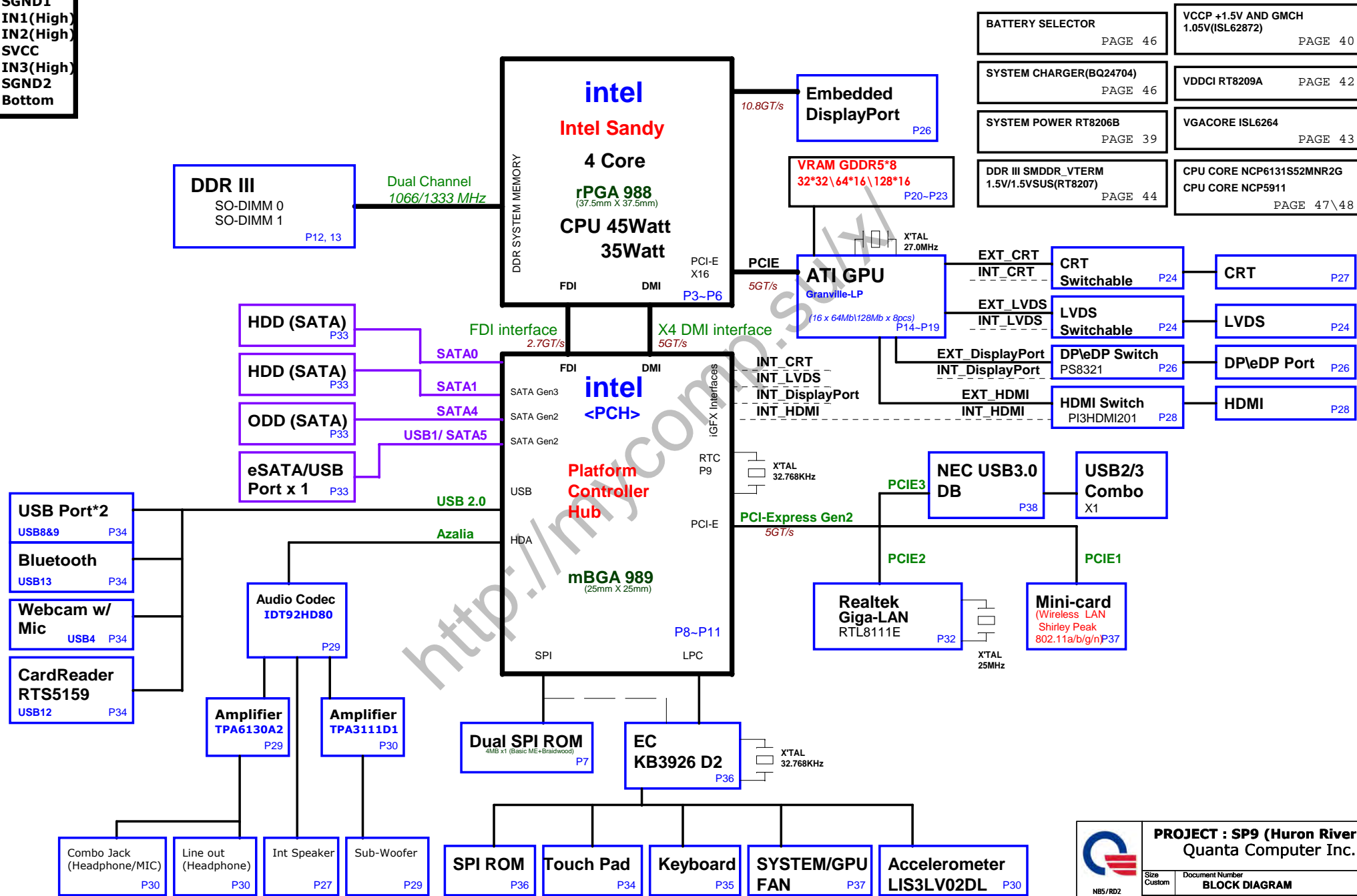
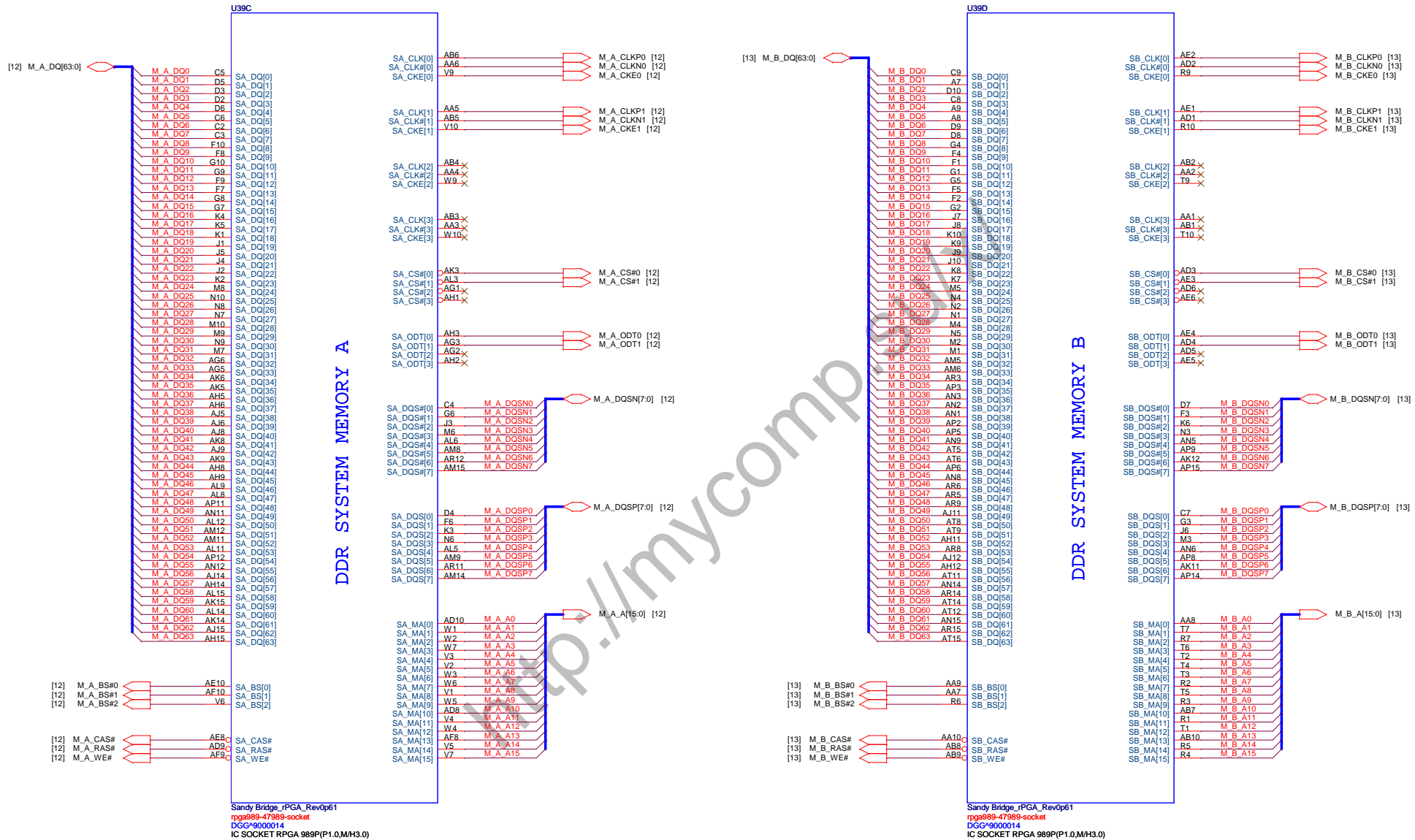


LAYER 1 : TOP
LAYER 2 : SGND1
LAYER 3 : IN1(High)
LAYER 4 : IN2(High)
LAYER 5 : SVCC
LAYER 6 : IN3(High)
LAYER 7 : SGND2
LAYER 8 : Bottom

SP9 BLOCK DIAGRAM

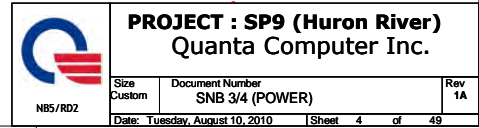
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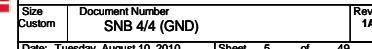




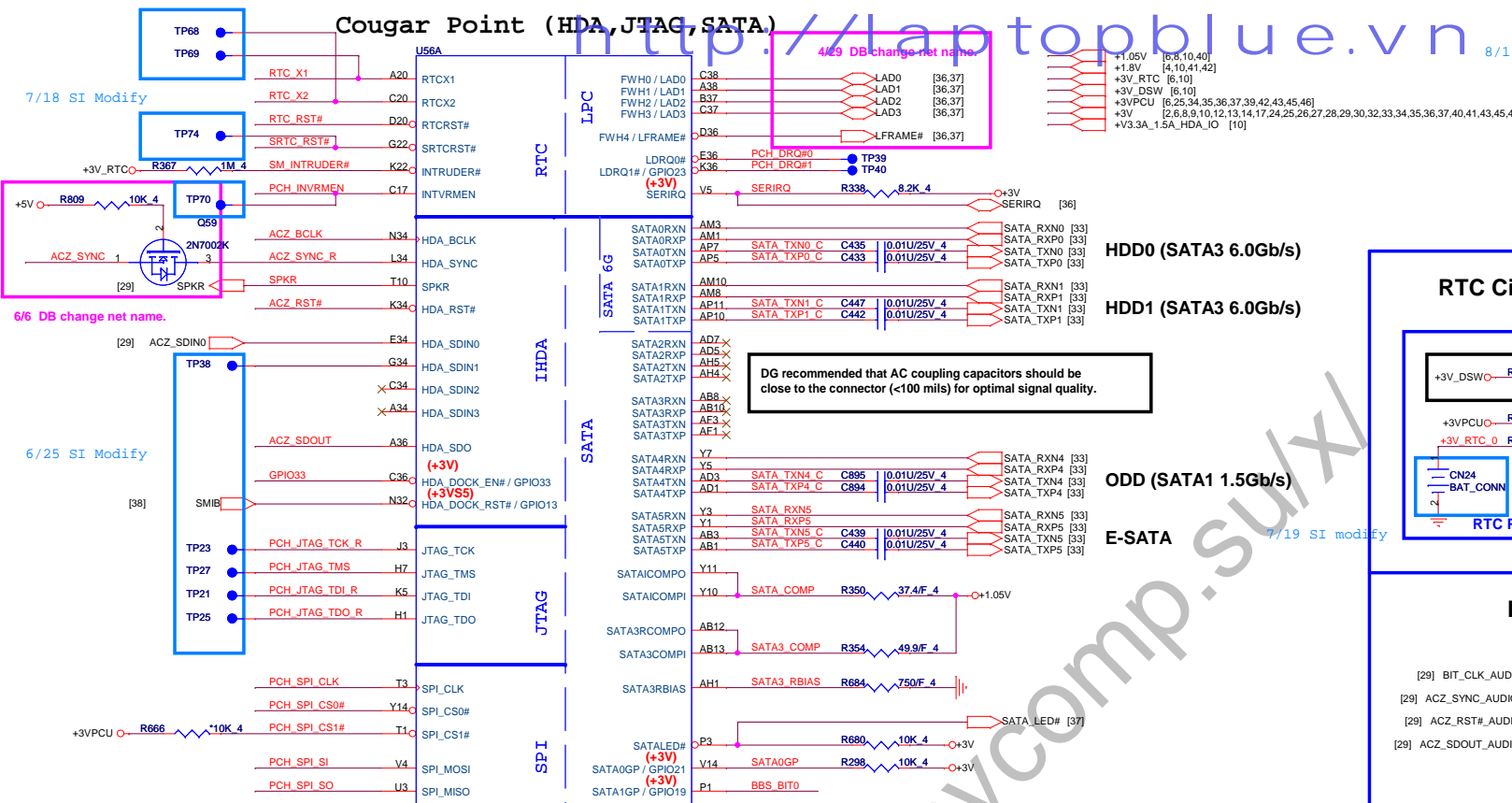
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DGG-9000014
IC SOCKET RPGA 989P(P1.0,MH3.0)

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rpg989-47989-socket
DGG-9000014
IC SOCKET RPGA 989P(P1.0,MH3.0)

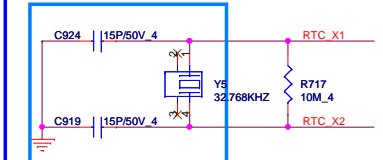




Cougar Point (HDA, JTAG, SATA)

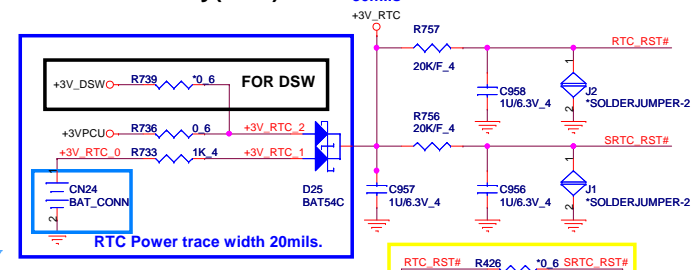


RTC Clock 32.768KHz

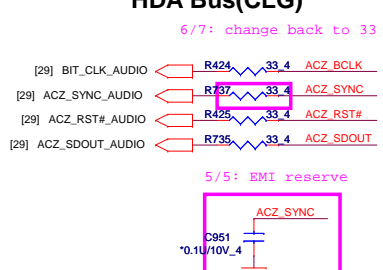


07

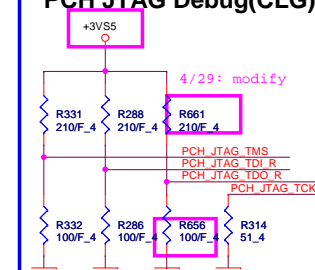
RTC Circuitry(RTC)



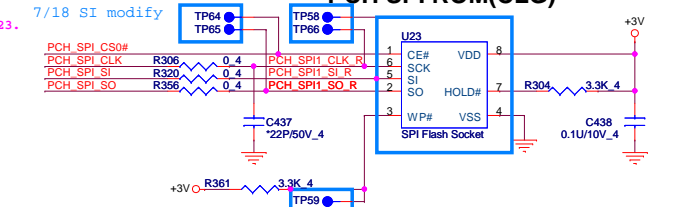
HDA Bus(CLG)



PCH JTAG Debug(CLG)



PCH SPI ROM(CLG)



Vender	Size	P/N
EON	4MB	AKE39FN0Q00 (EN25F32-100HIP)
Winbond	4MB	AKE391PON00 (W25Q32BVSSIG)
Socket		DG008000031

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	Different from Calpella No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	SPKR R660 *1K 4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R749 R746 *1K 4 +3V PCI_GNT3# [8]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R716 330K 4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R727 1K 4 GPIO33_E [36]
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK		
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	R667 R752 *1K 4 BBS_BIT0 [8]
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	USE GPIO PIN +1.8V R691 *1K 4 NV_ALE [8]
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V R678 2.2K 4 R694 4.7K 4 NV_CLE [8]
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3VSSO R734 *1K 4 ACZ_SYNC_R 5/4 add
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	ACZ_SDOUT R738 *1K 4 +V3.3A_1.5A_HDA_IO
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	R703 *1K 4 4/29 reserve. ICC_EN# [9]
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R693 *1K 4 PLL_ODVR_EN [9]
SPI_MOSI	ITPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R308 1K 4 +3V

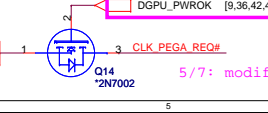
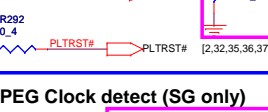
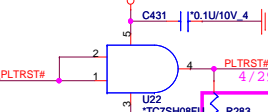
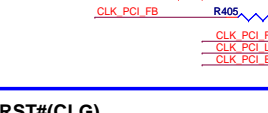
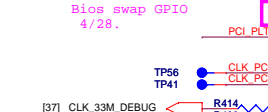
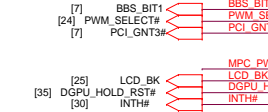
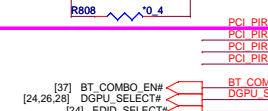
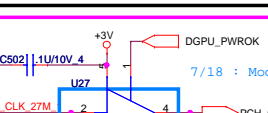
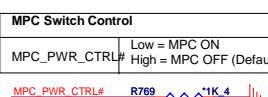
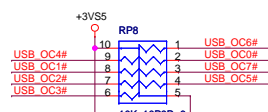
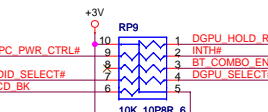
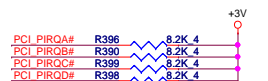
NBS/RD2

PROJECT : SP9 (Huron River)
Quanta Computer Inc.

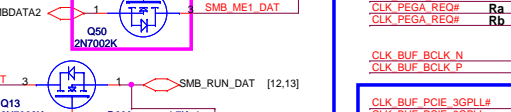
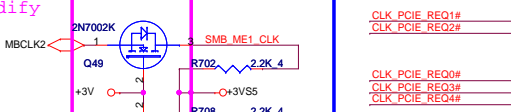
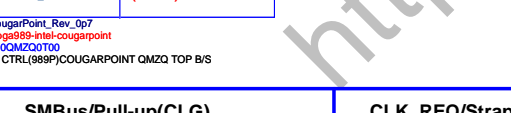
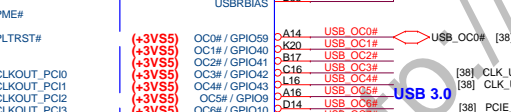
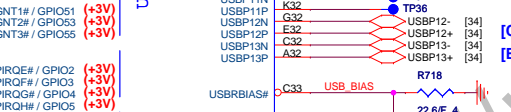
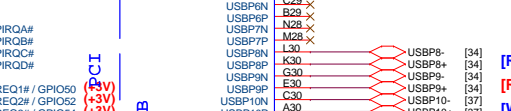
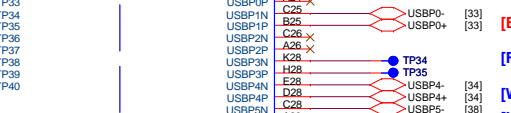
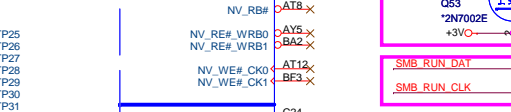
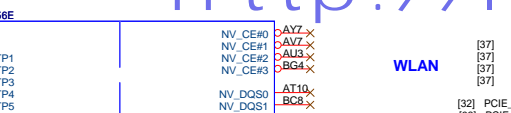
Size Custom Document Number PCH 2/6 (SATA/HDA/SPI) Rev 1A

Date: Tuesday, August 10, 2010 Sheet 7 of 49

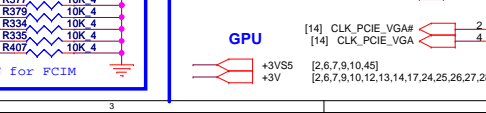
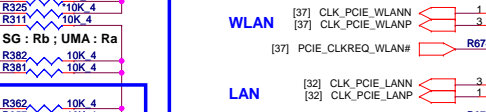
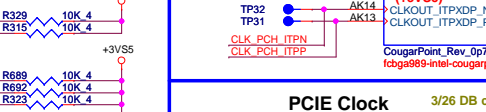
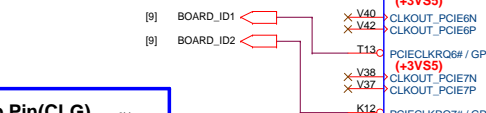
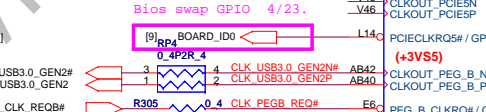
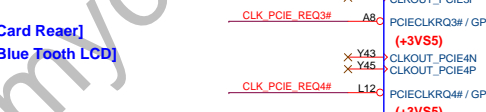
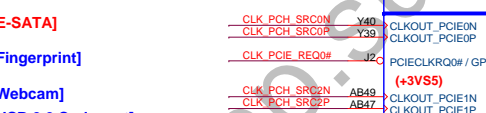
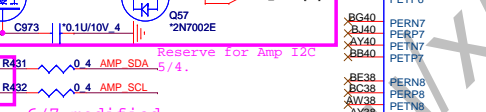
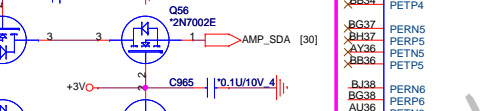
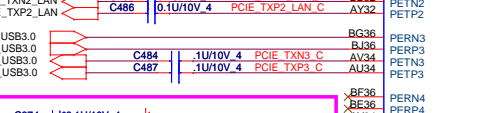
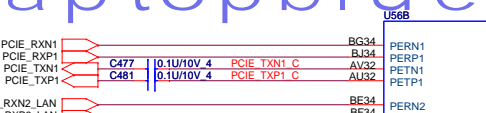
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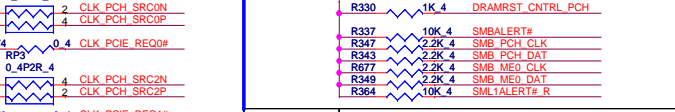
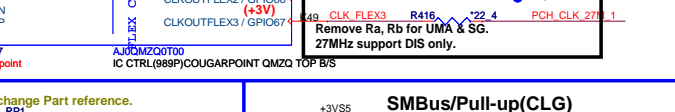
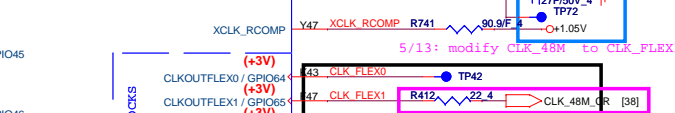
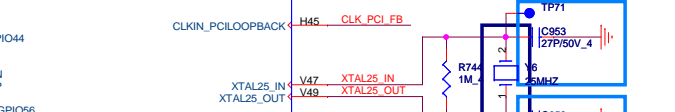
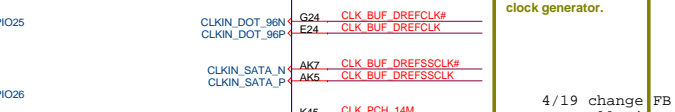
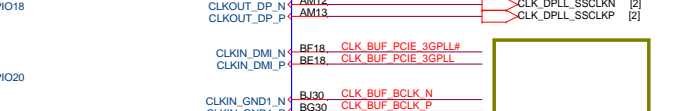
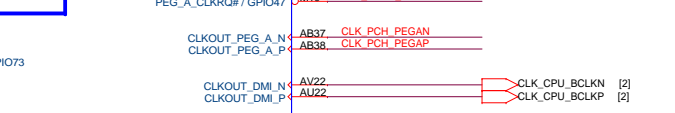
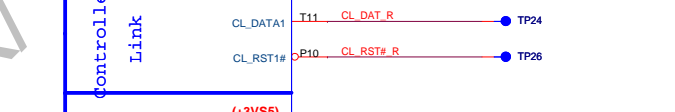
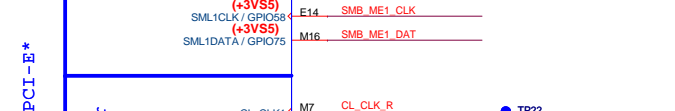
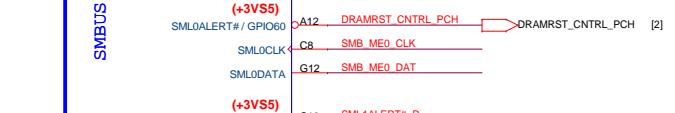
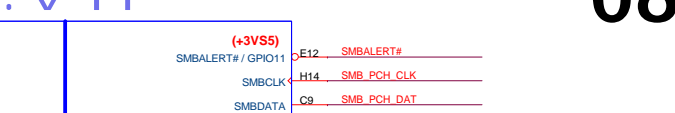
Cougar Point-M (PCI, USB, NVRAM)

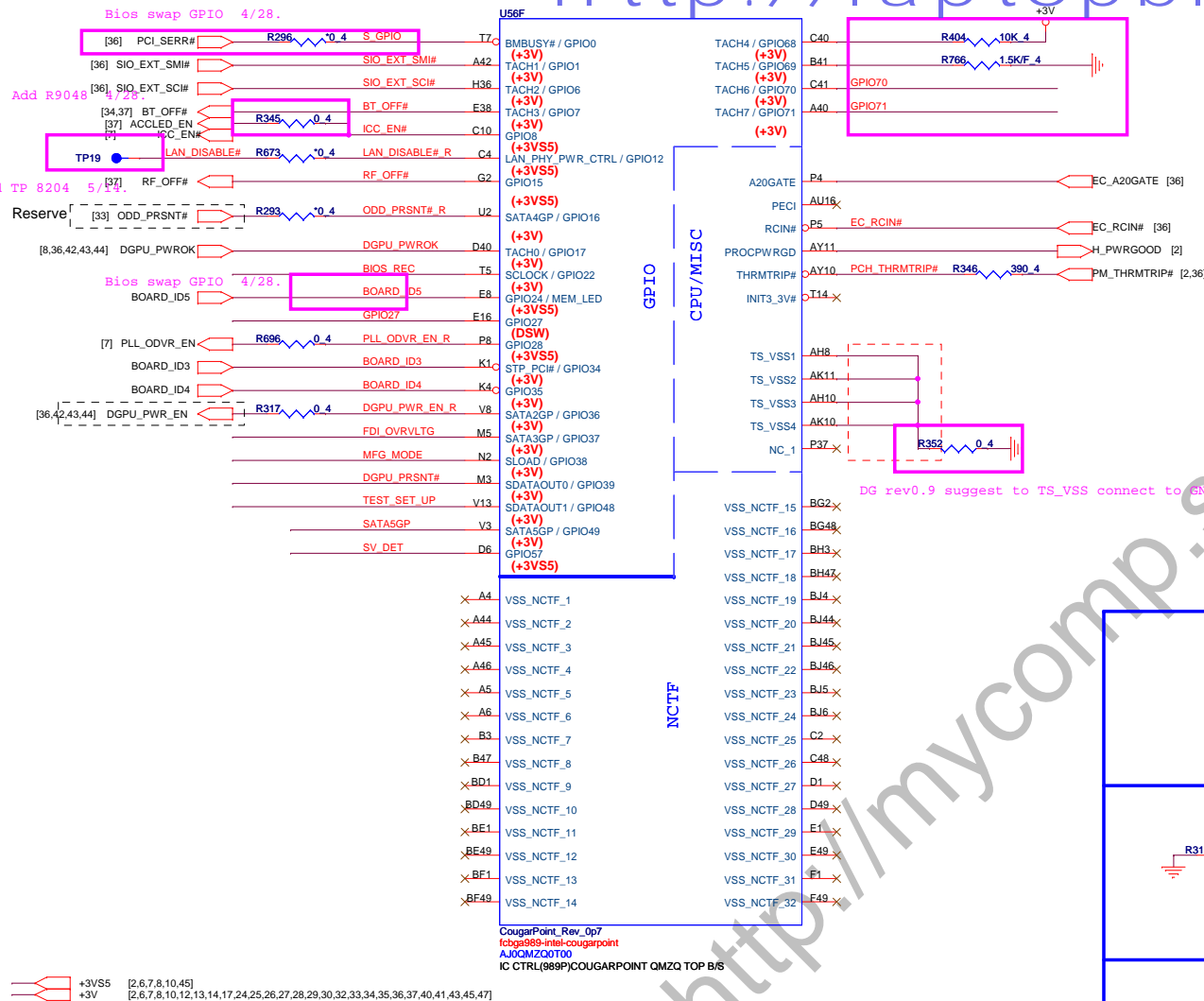


Cougar Point-M (PCI-E, SMBUS, CLK)



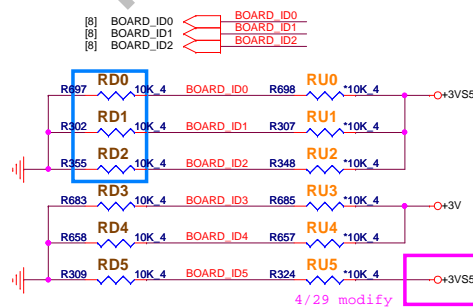
Cougar Point-M (PCI-E, SMBUS, CLK)



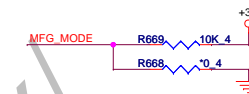


Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
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SP9 3D	0	0	0	0	0	1

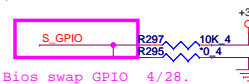
8/2 SI Modify



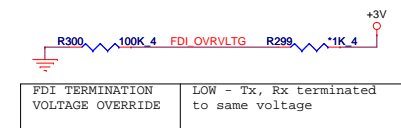
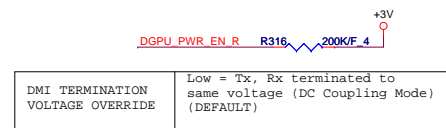
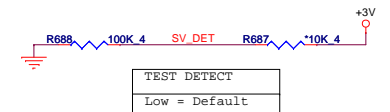
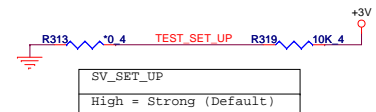
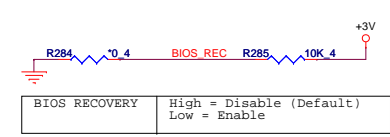
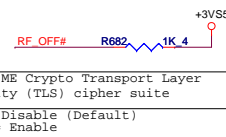
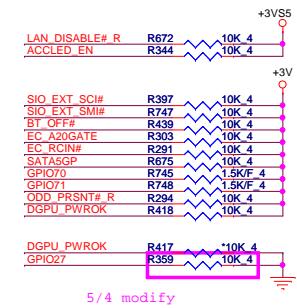
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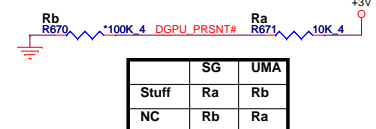
SGPIO



GPIO Pull-up/Pull-down(CLG)



GFX Present



PROJECT : SP9 (Huron River)

Quanta Computer Inc.

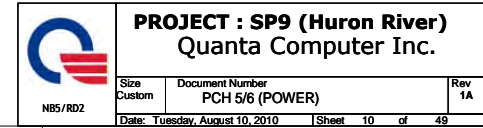
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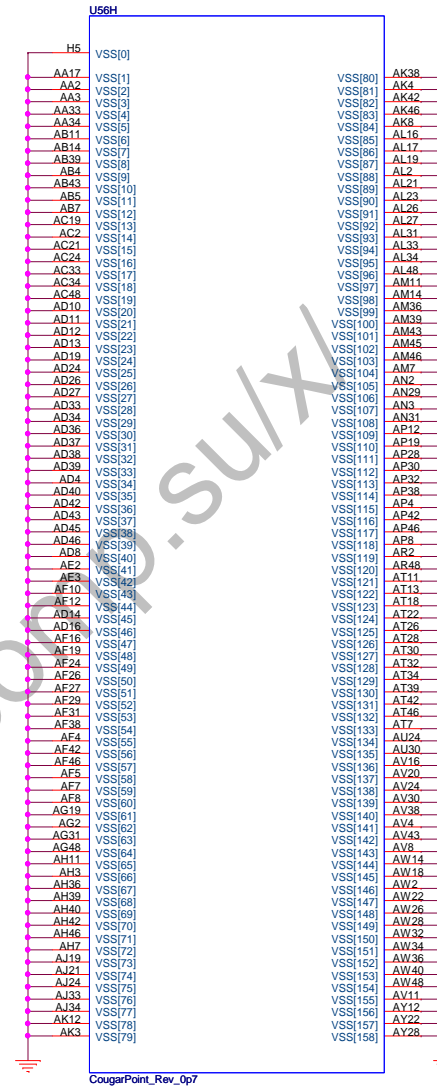
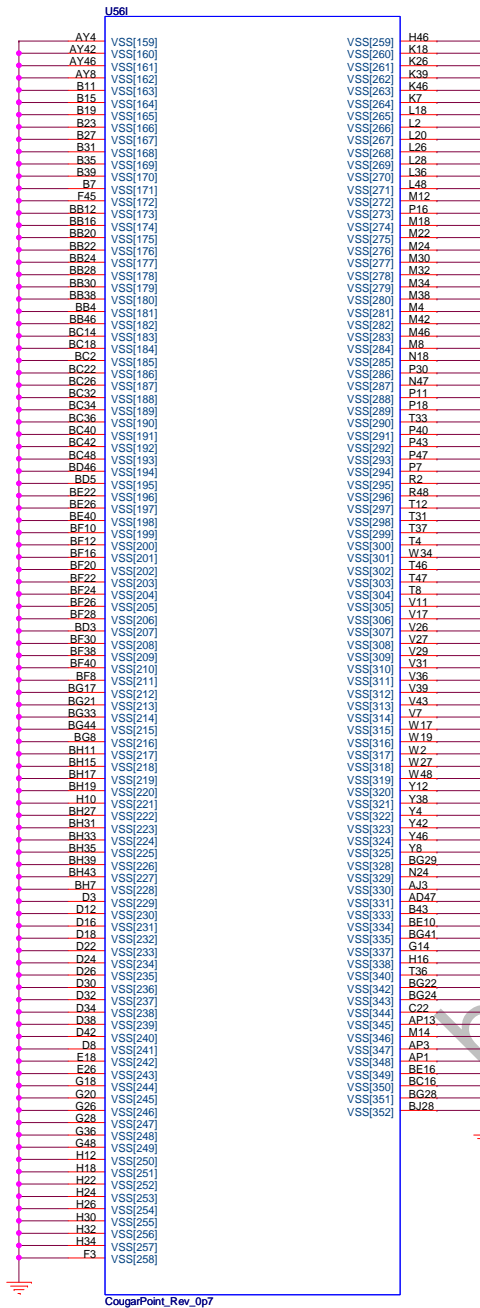
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Rev 1A

Date: Tuesday, August 10, 2010

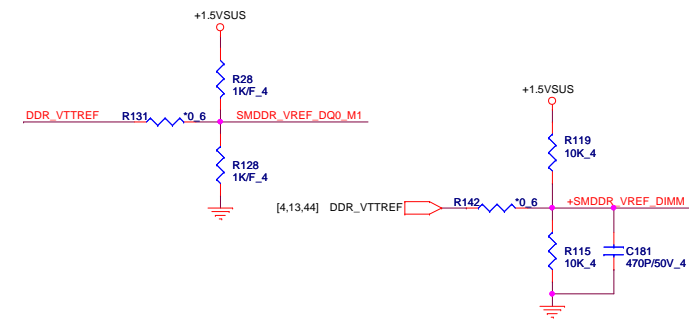
Sheet 9 of 49

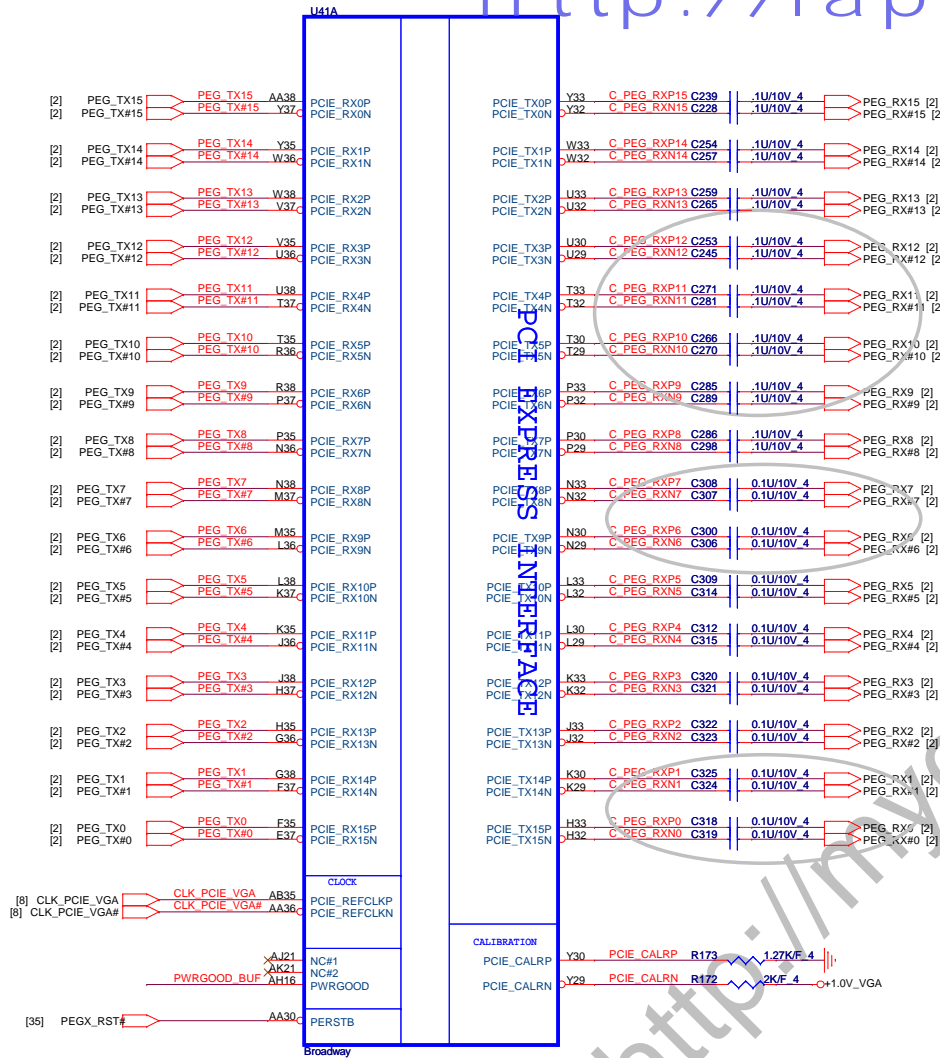




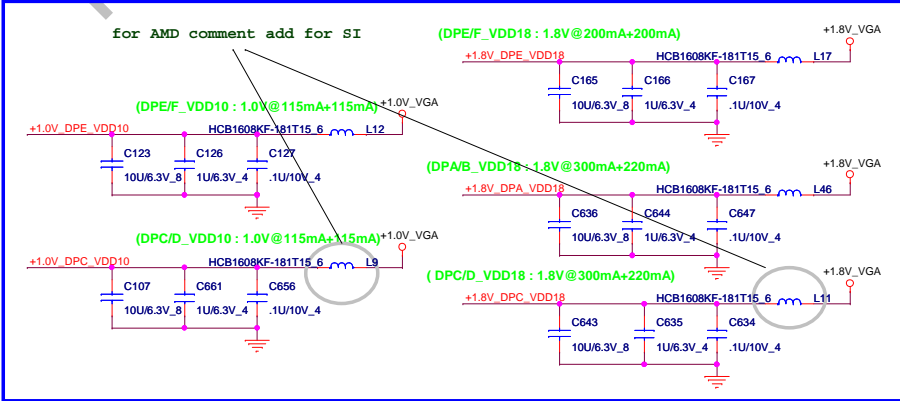
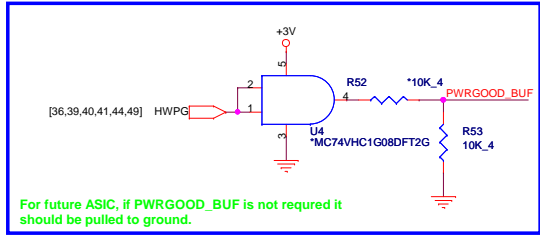
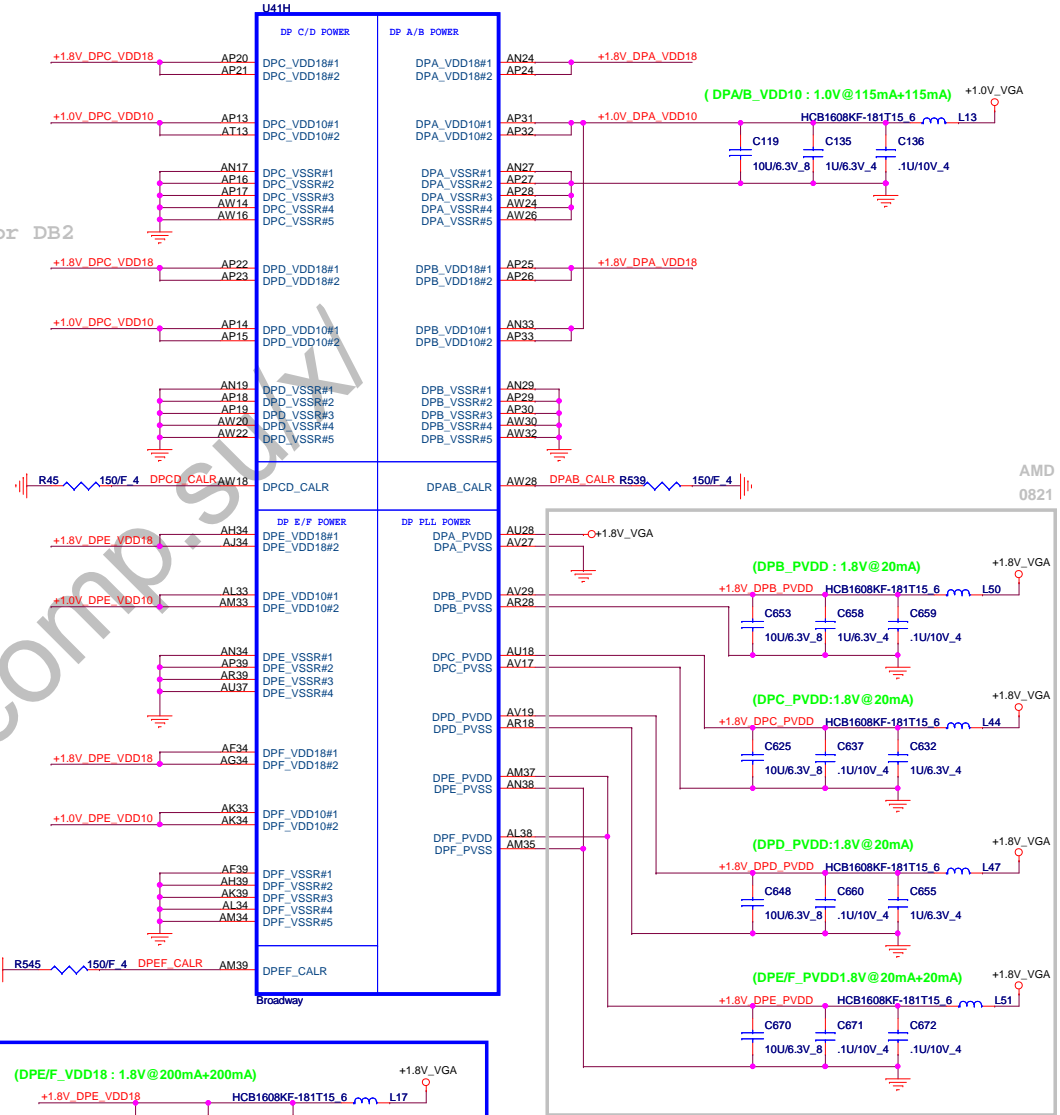


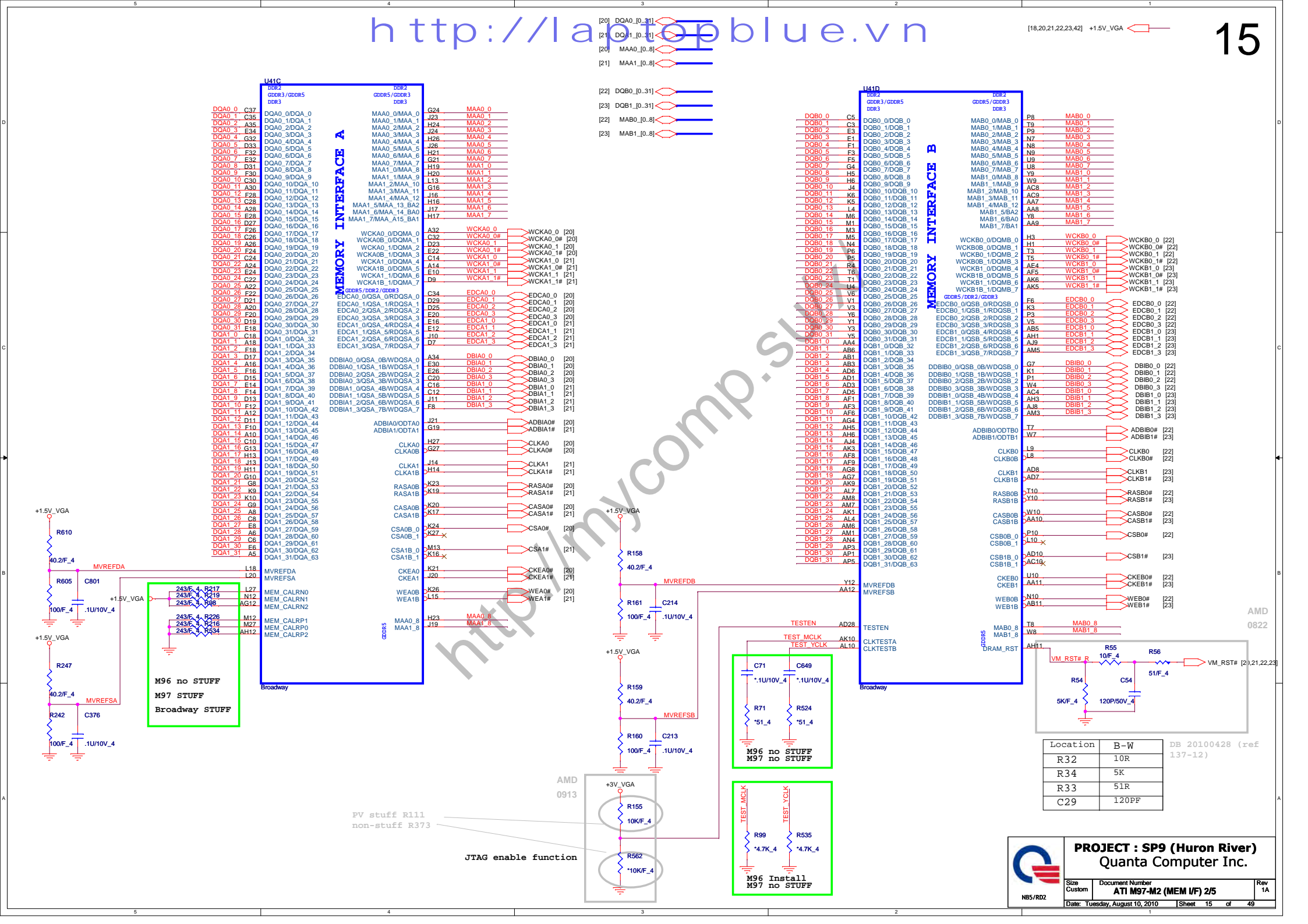
VREF DQ0 M1 Solution






for DB2



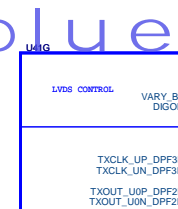


Location	B-W	DB 20100428 (ref 137-12)
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R34	5K	
R33	51R	
C29	120PF	

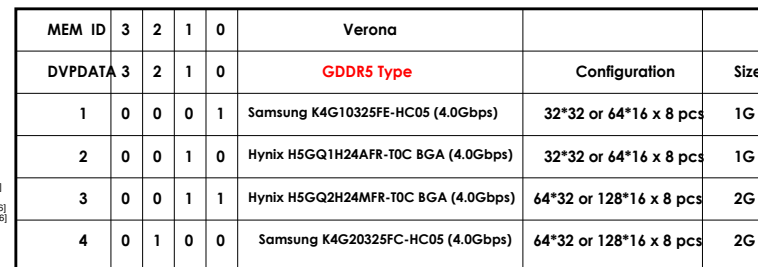


PROJECT : SP9 (Huron River)
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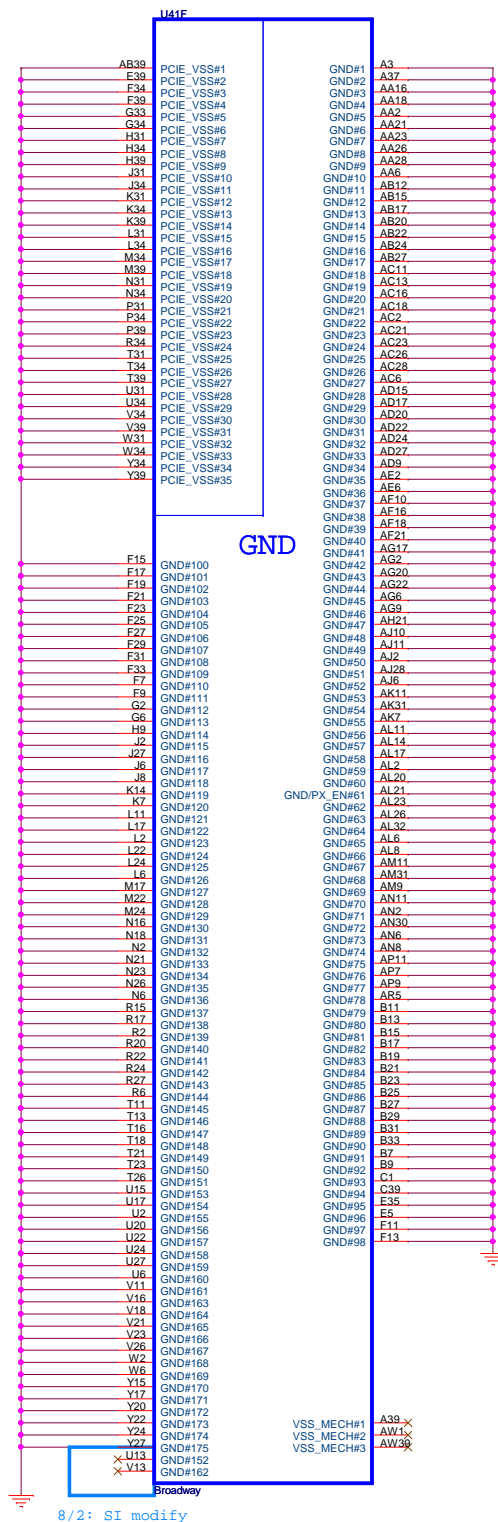
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Date: Tuesday, August 10, 2010	Sheet 15 of 49	



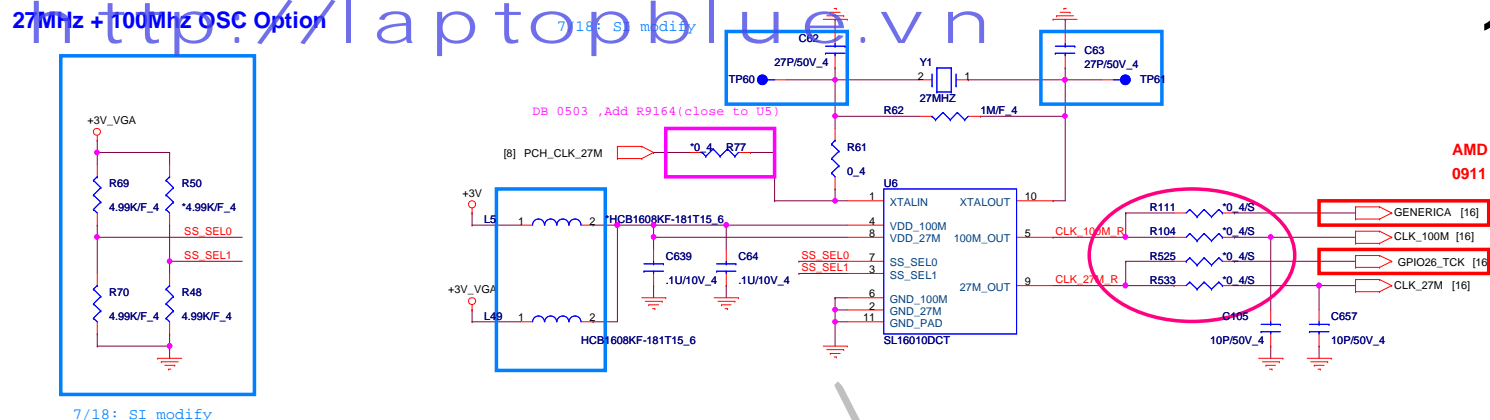
5/11 change net name



MEM ID	3	2	1	0	Verona		
DVPDATA	3	2	1	0	GDDR5 Type	Configuration	Size
1	0	0	0	1	Samsung K4G10325FE-HC05 (4.0Gbps)	32*32 or 64*16 x 8 pcs	1G
2	0	0	1	0	Hynix H5GQ1H24AFR-T0C BGA (4.0Gbps)	32*32 or 64*16 x 8 pcs	1G
3	0	0	1	1	Hynix H5GQ2H24MFR-T0C BGA (4.0Gbps)	64*32 or 128*16 x 8 pcs	2G
4	0	1	0	0	Samsung K4G20325FC-HC05 (4.0Gbps)	64*32 or 128*16 x 8 pcs	2G

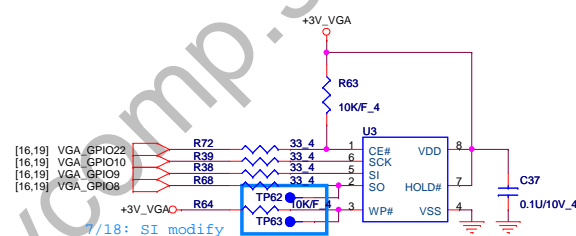


8/2: SI modify



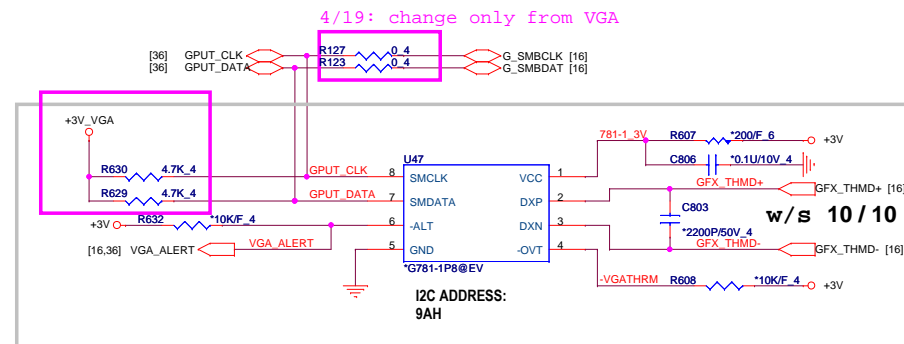
7/18: SI modify

Ext EEPROM



7/18: SI modify

Thermal Sensor

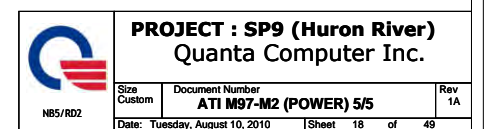


I2C ADDRESS:
9AH

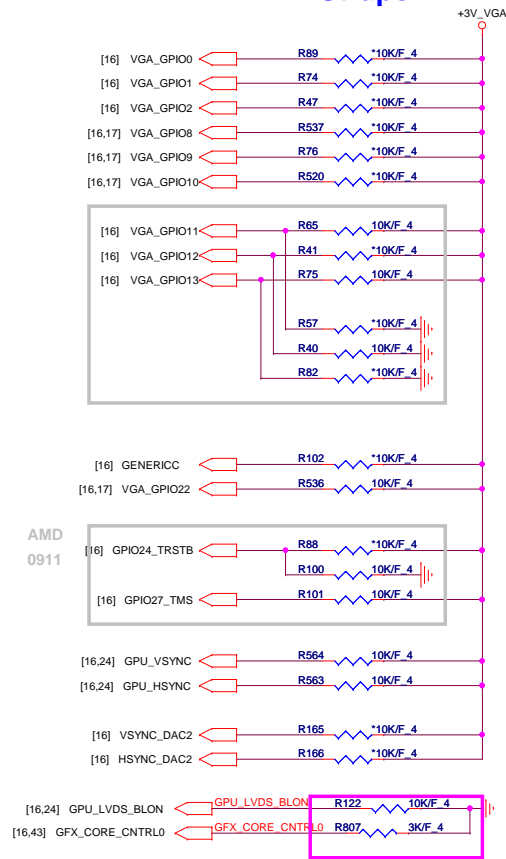


PROJECT : SP9 (Huron River)
Quanta Computer Inc.

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Straps



Overlap pads to save space and to prevent assembly of both resistors.

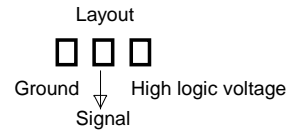
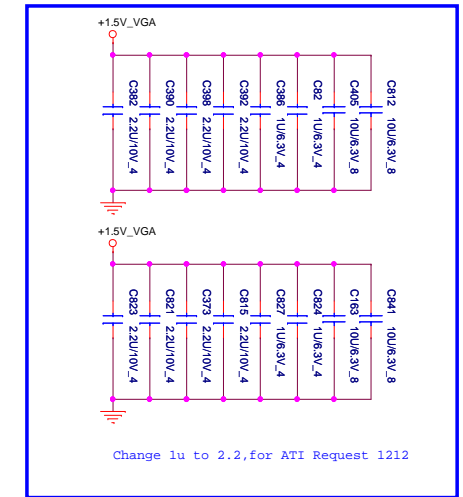


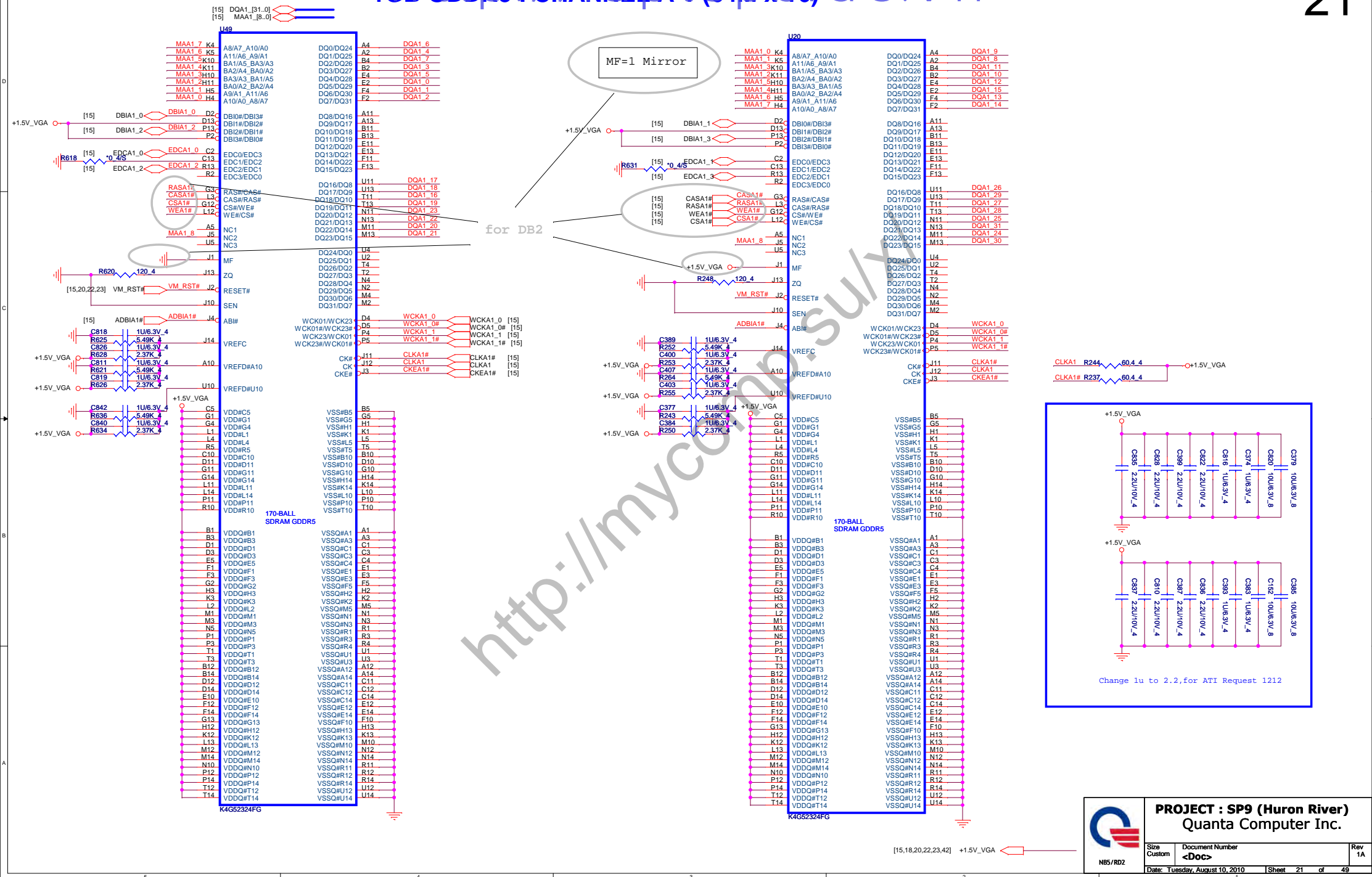
Table 3-34 ROM Configurations

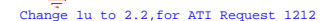
Manufacturer	Part Number	Size	CONFIG[2:0]
Atmel	AT25F512	512 kbit	001
	AT25F512A	512 kbit	010
	AT25F1024	1 Mbit	011
	AT25F1024A	1 Mbit	011
	AT25F2048	2 Mbit	011
	AT25F4096	4 Mbit	011
ST Microelectronics	M25P05A	512 kbit	100
	M25P10A	1 Mbit	101
	M25P20	2 Mbit	101
	M25P40	4 Mbit	101
	M25P80	8 Mbit	101
Silicon Storage Technology	SST25VF512	512 kbit	010
	SST25VF010	1 Mbit	011
	SST25VF020	2 Mbit	011
	SST25VF040	4 Mbit	011
Winbond Electronics Corporation	W45B512	512 kbit	110
	W45B012	1 Mbit	111
YMC	Y25LF05	512 kbit	010
	SA25C020	2 Mbit	011
PMC	Pm25LV512	512 kbit	100
	Pm25LV010	1 Mbit	101

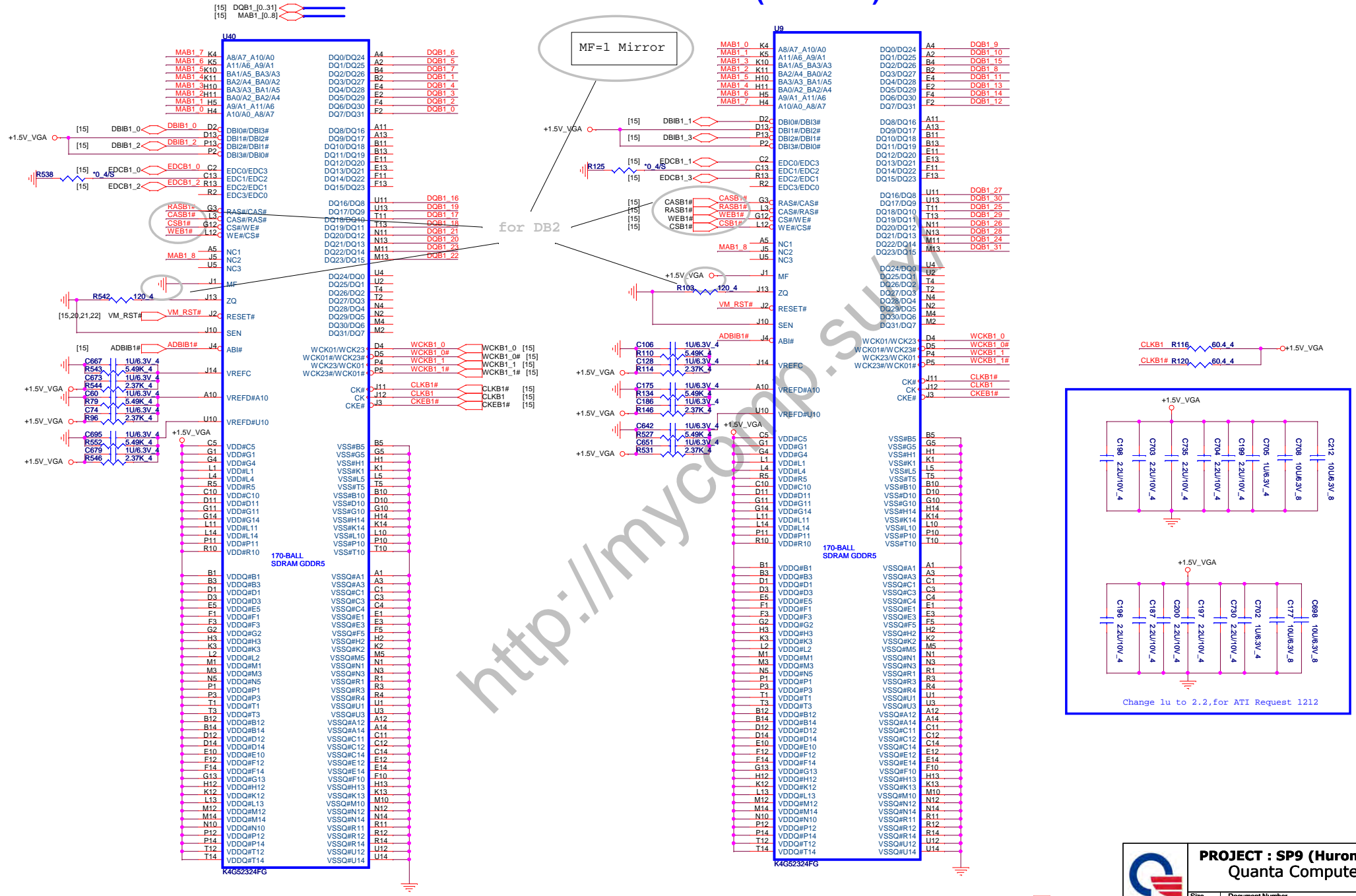
Default

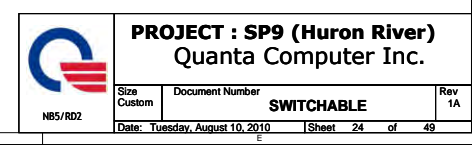
Strap Name	Pin	Straps Description	Default Value
TX_PWRS_ENB	GPIO0	GPIO[1:0]:Recommend to pulling up for PICE setting. GPIO_0:PCIE full TX output swing	
TX_DEEMPH_EN	GPIO1	GPIO_1:PCIE Transmitter DE-EMPHASIS enabled	
BIF_GEN2_EN	GPIO2	GPIO_2:System is using PCIE GEN1 can be let it NC(ASIC internal pull down) if Gen2 just pull up for PCIE 5GT/s support. (0=PCIE GNE1,2.5GT/s ; 1=PCIE GNE2,5GT/s)	
STRAP_BIF_CLK_PM_EN	GPIO8		
CONFIG[3] CONFIG[2] CONFIG[1] CONFIG[0]	GPIO9 GPIO13 GPIO12 GPIO11		
BIOS_ROM_EN	GPIO22	BIOS_ROM_EN(GPIO22)=1, then Config[2:0]=GPIO[13:12:11] defines the ROM type. (See table as below)	
AUDIO[0]	VSUVC		
AUD(1)	HSUVC		
VSUVC_DAC2	V2SUVC		
HSUVC_DAC2	H2SUVC		
	GENERICC		

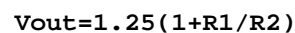
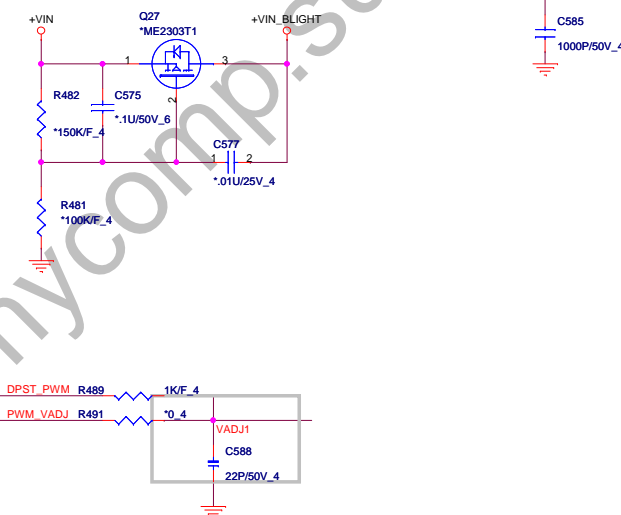
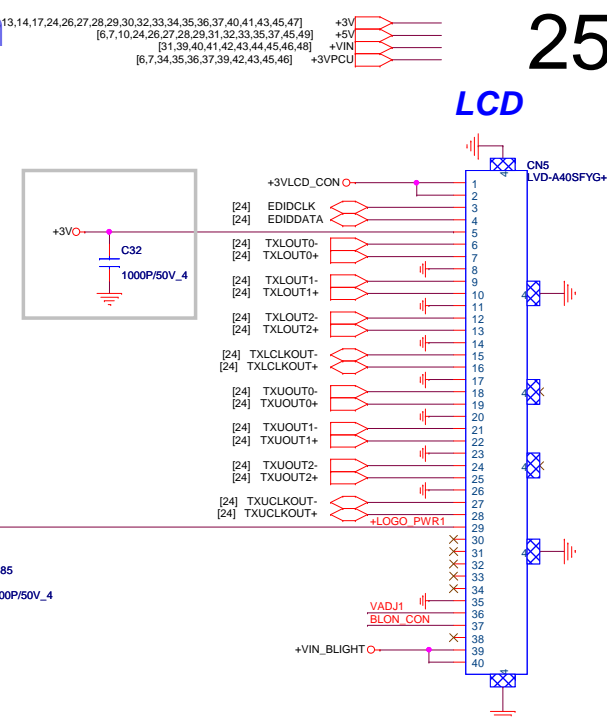
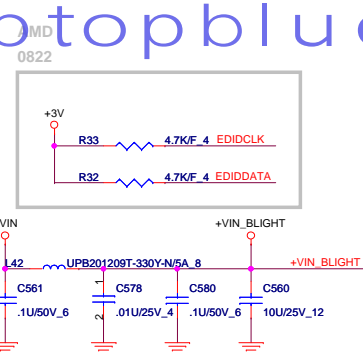










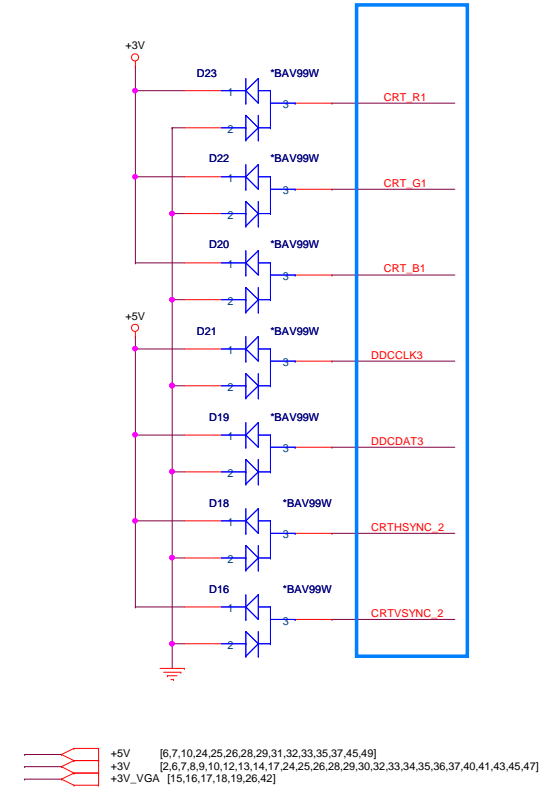
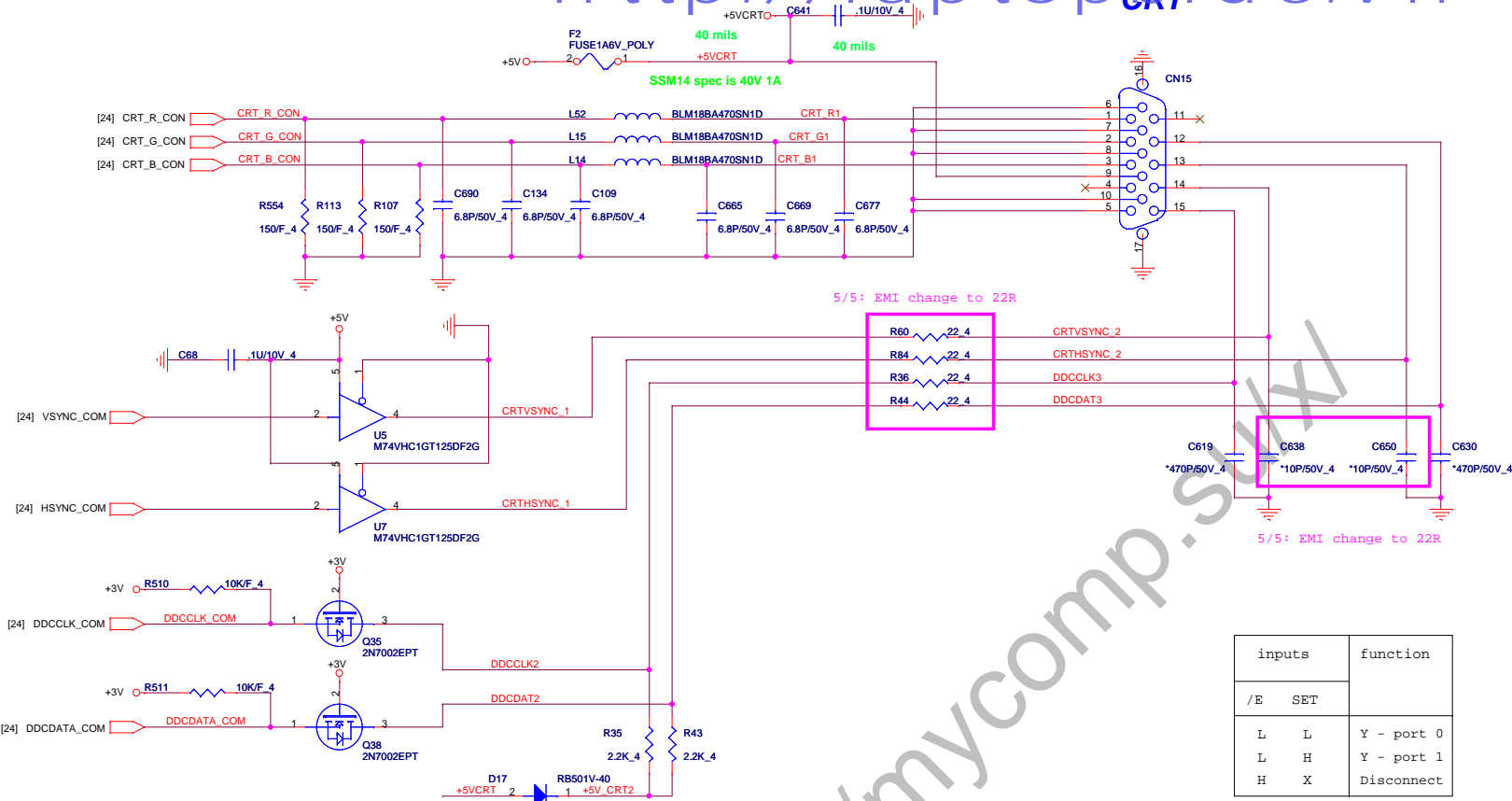




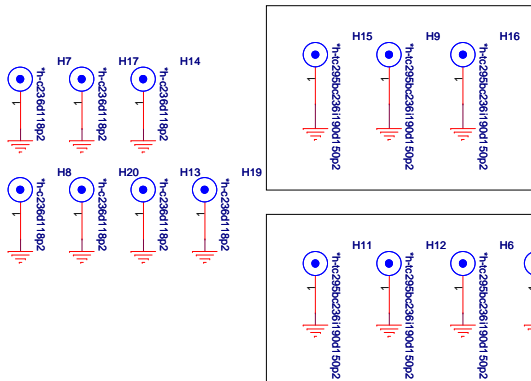
DP_CFG_OUT	Output configuration
L	Output is tracking DPCD register setting (auto interception)
H	Output swing level fixed at 600mV and no pre-emphasis
M	Output swing level is fixed at 400mV and no pre-emphasis



DP_AEQ#_INx	Automatic RX equalization enable
L	Disable input automatic equalization
H	Enable input automatic equalization



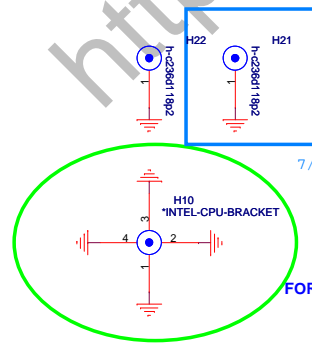
for GPU



for CPU

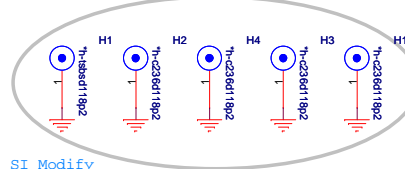
Modify H5\H6, H11\H12\H13\H16\H17, H15 at 0506

SI ME change Footprint



FOR LAYOUT

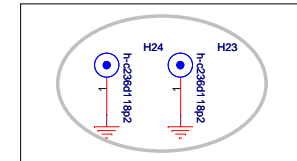
SI for ME change footprint

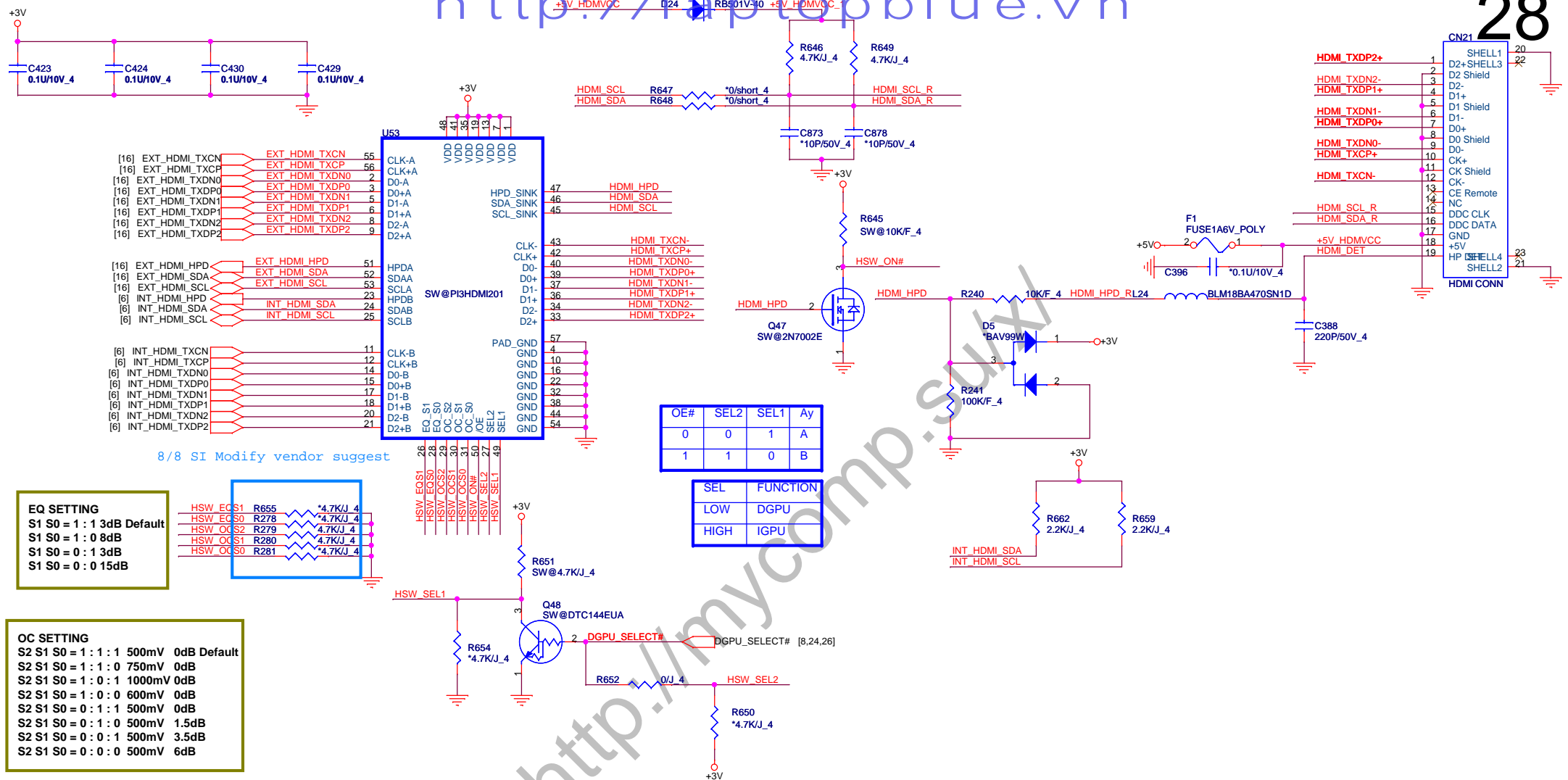


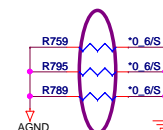
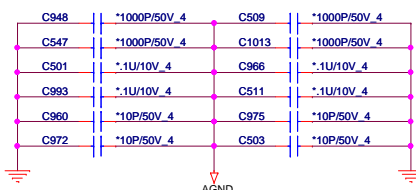
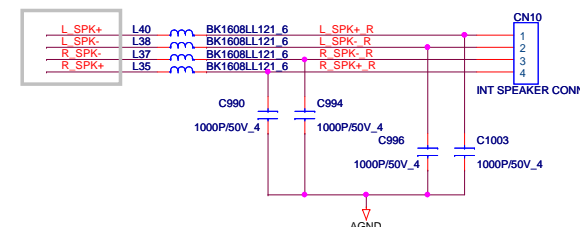
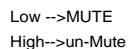
7/18 SI Modify

HOLDS

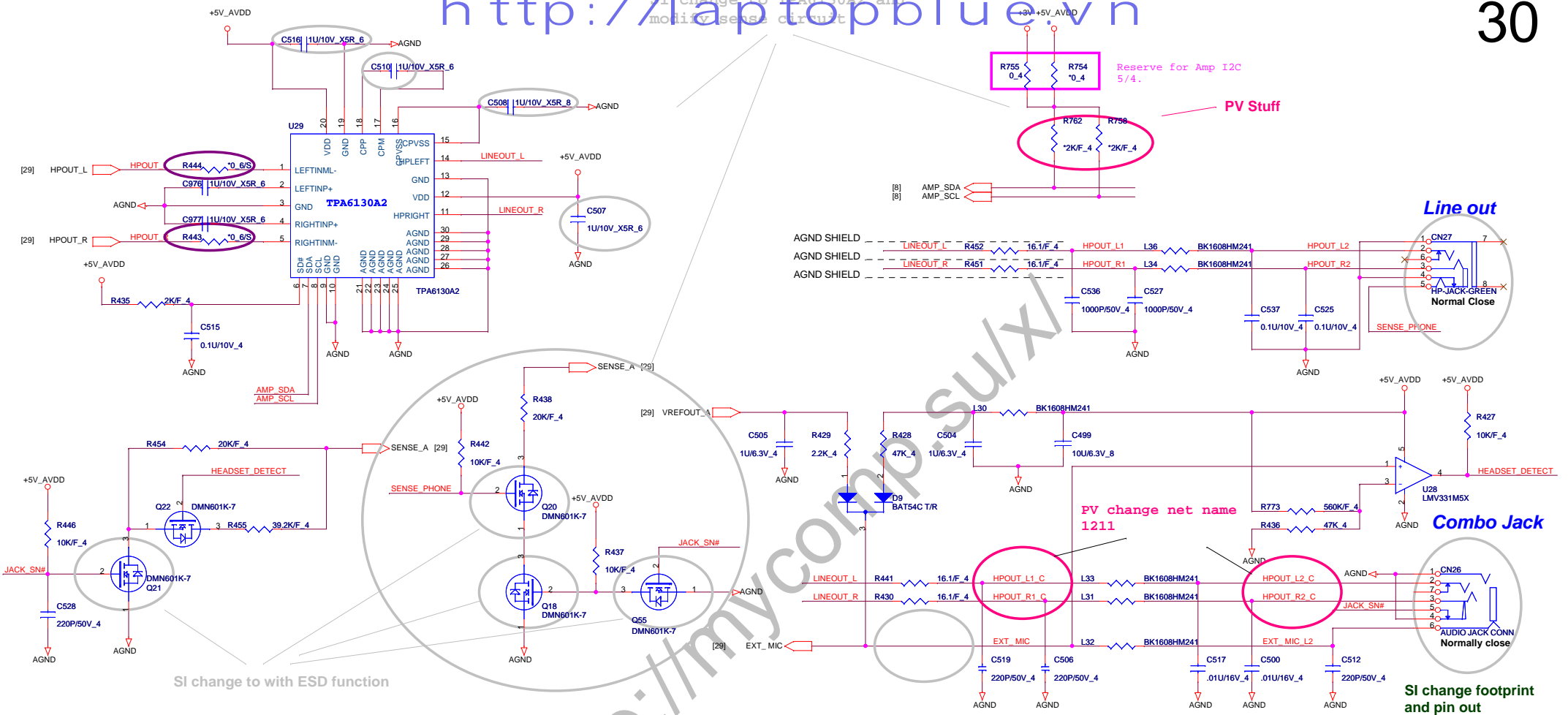
SI add for PCH hole







http://laptopblue.vn



SUBWOOFER

http://laptopblue.vn

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PV change R575 from 20K to 10K for HP request

SI add LDO for SUBWOOFER power

Change 4EQ to 2EQ

for PV

Sub-Woofer power

for DB2

7/18 SI Modify

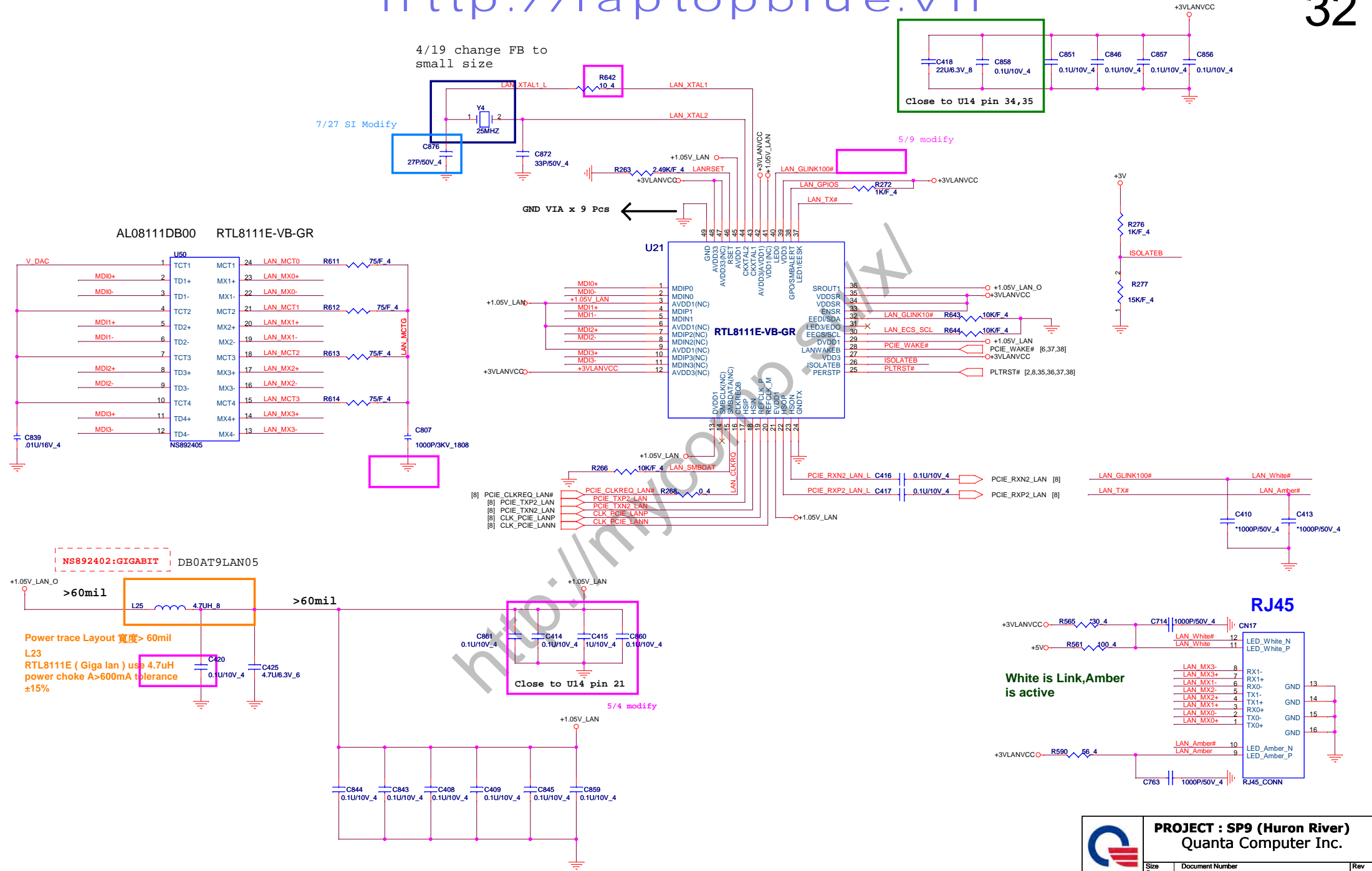
close to Connect

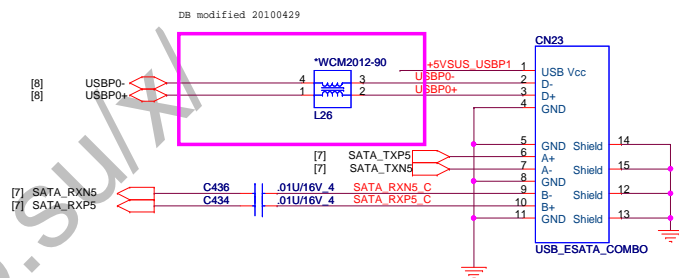
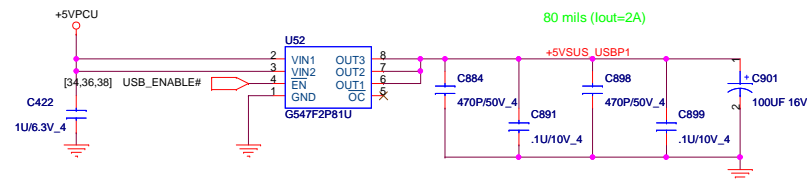
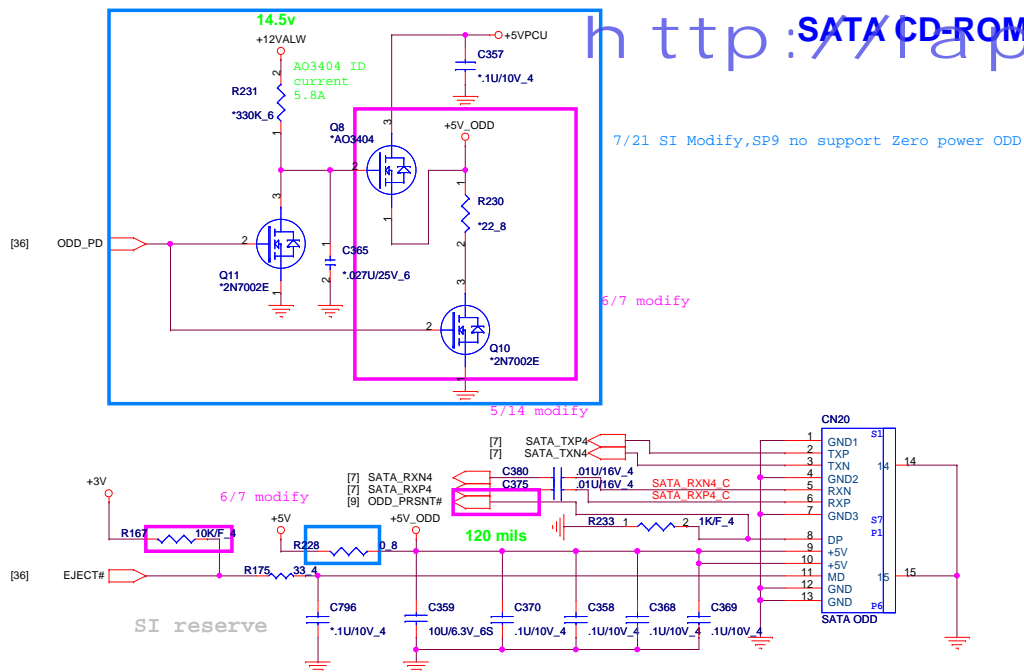
MV add R317

GAIN1	GAIN0	dB
0	0	20
0	1	26
1	0	32
1	1	36

SI change type

+3V [2,6,7,8,9,10,12,13,14,17,24,25,26,27,28,29,30,32,33,34,35,36,37,40,41,43,45,47]
+5V_AVDD [29,30]
+VIN [25,39,40,41,42,43,44,45,46,48]

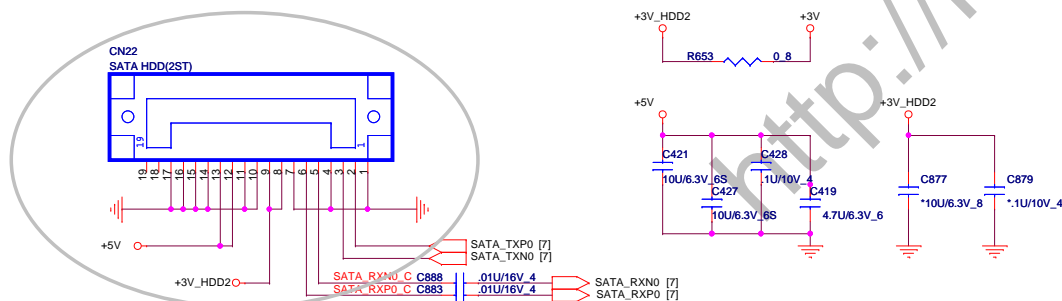




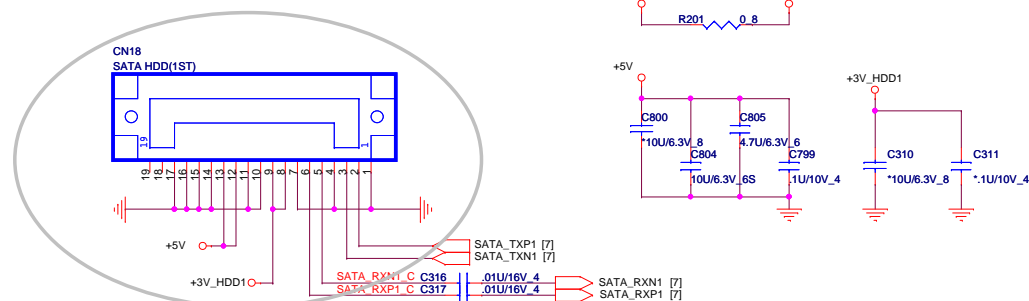
SATA HDD #1

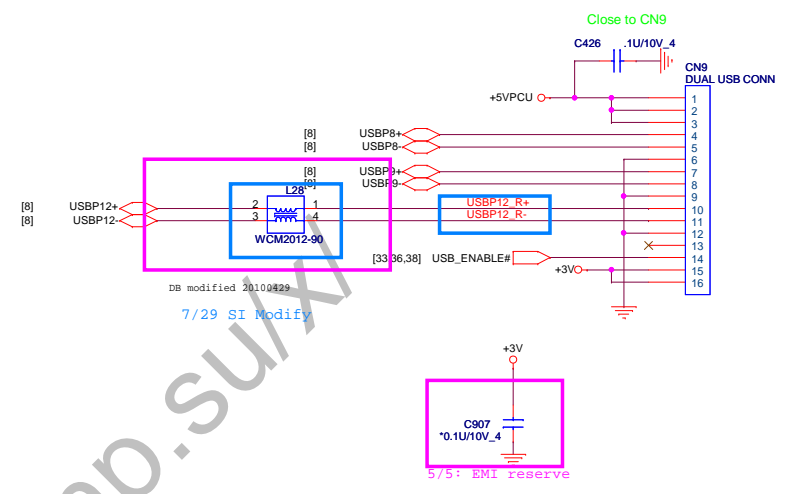
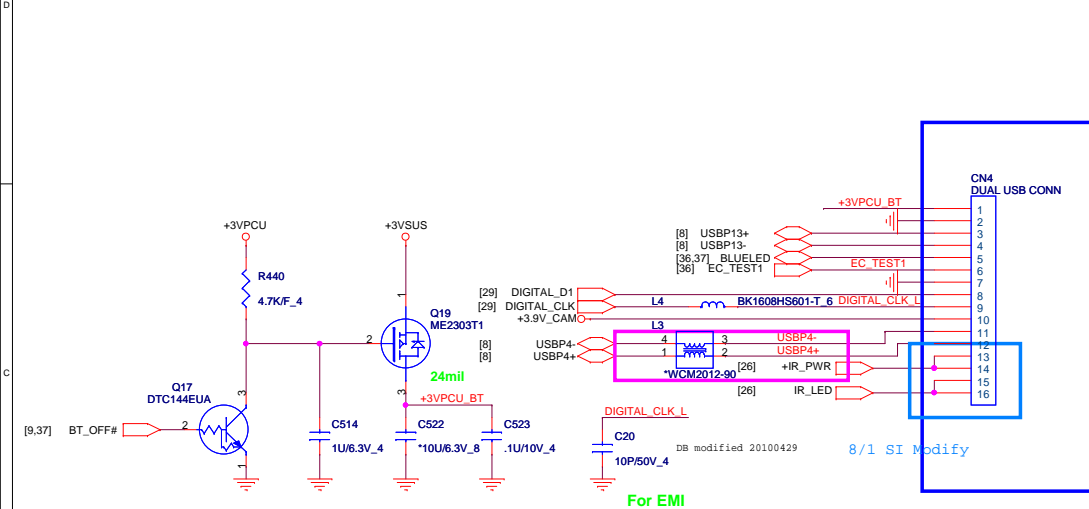
SATA HDD #2

SI change pin define and footprint (the same AX)



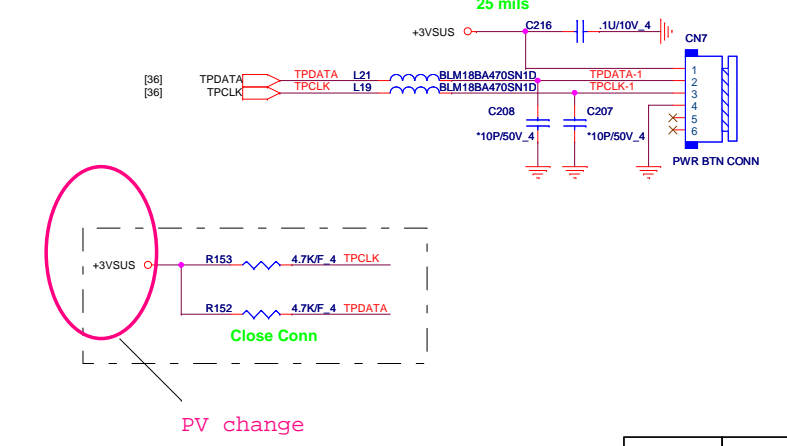
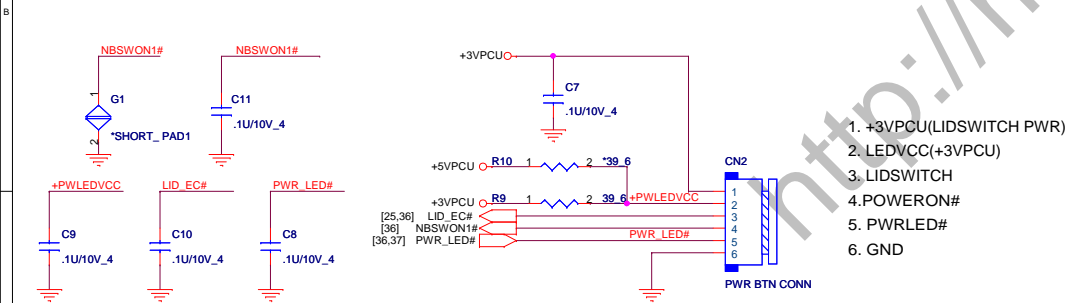
SI change pin define and footprint (the same AX)

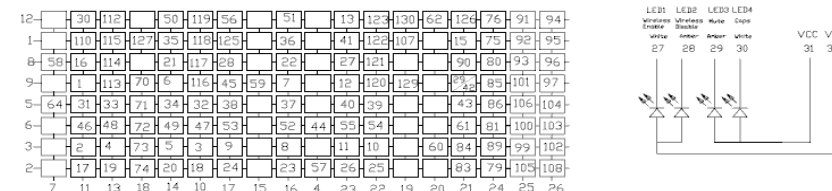
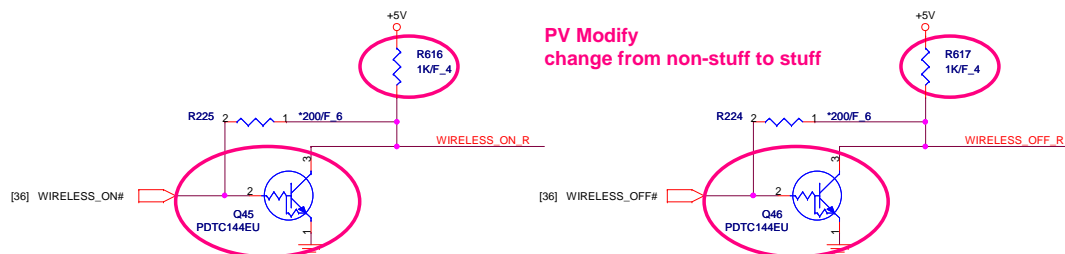
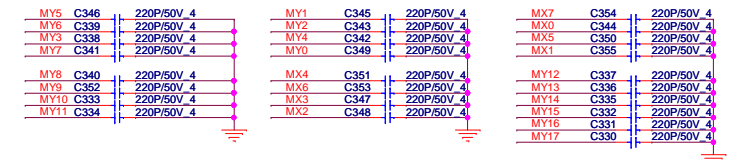
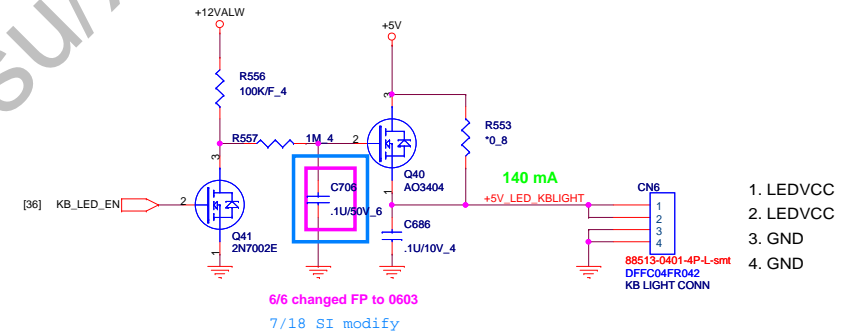
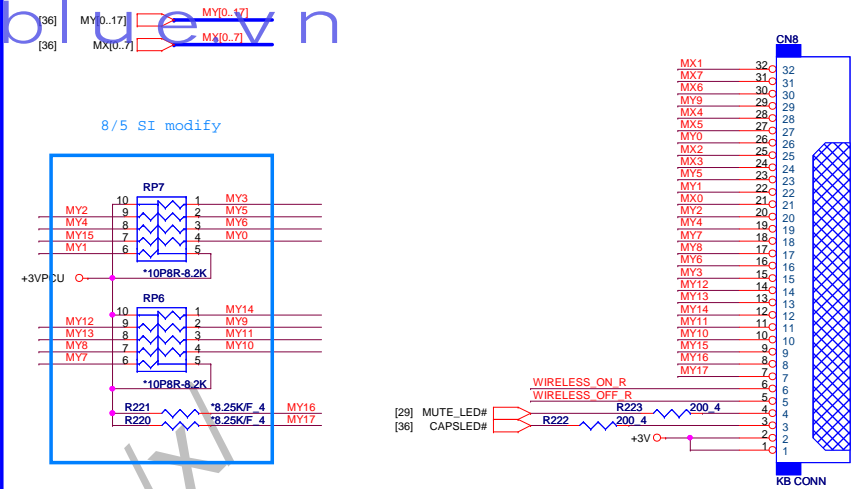
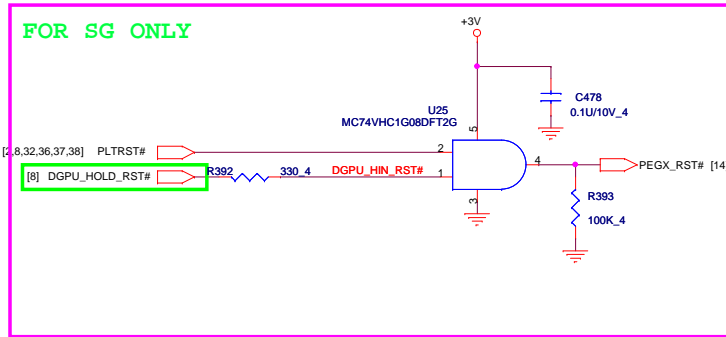


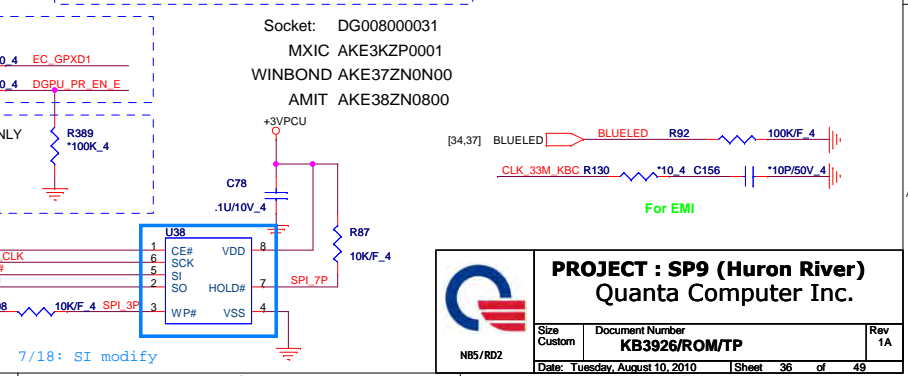


Power Button

Touch Pad Button







	GPIO41
SI	1
PV	0




R387 0.4 DGPU_PR_EN_E


BIOS_CS#
BIOS_SPI_CLK

--	--

7/18: SI modify

Socket: DG008000031
MXIC AKE3KZP0001
WINBOND AKE37ZN0N00
AMIT AKE38ZN0800

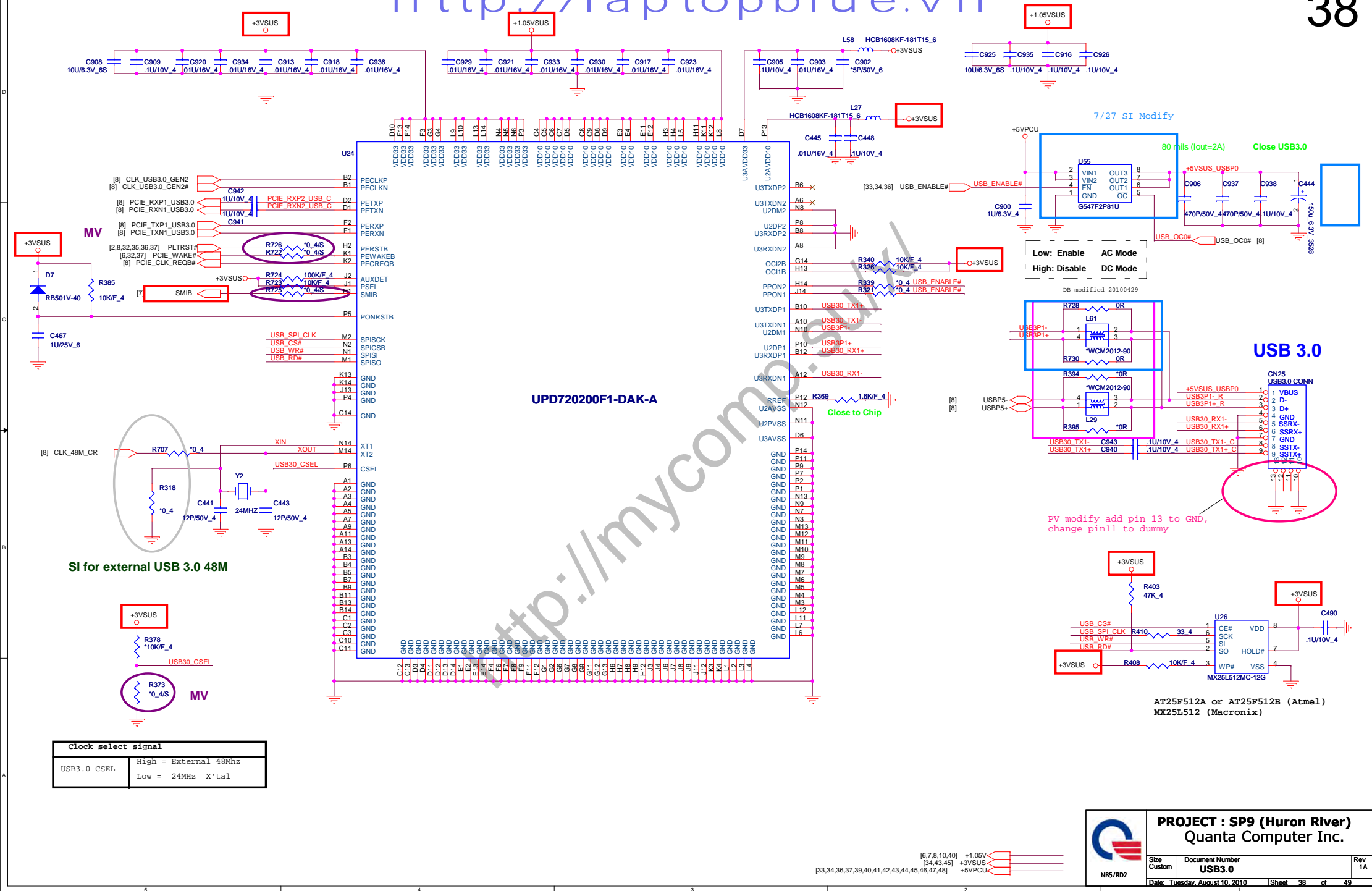
[34,37] BLUELED BLUELED R92 100K/F 4
CLK 33M KBC R130  *10 4 C156  *10P/50V 4 

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Size	Document Number
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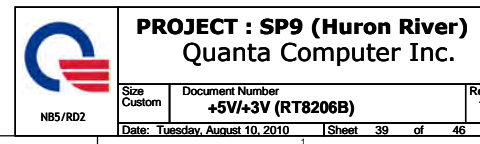
NB5/RD2	Custom	KB3926/ROM/TP
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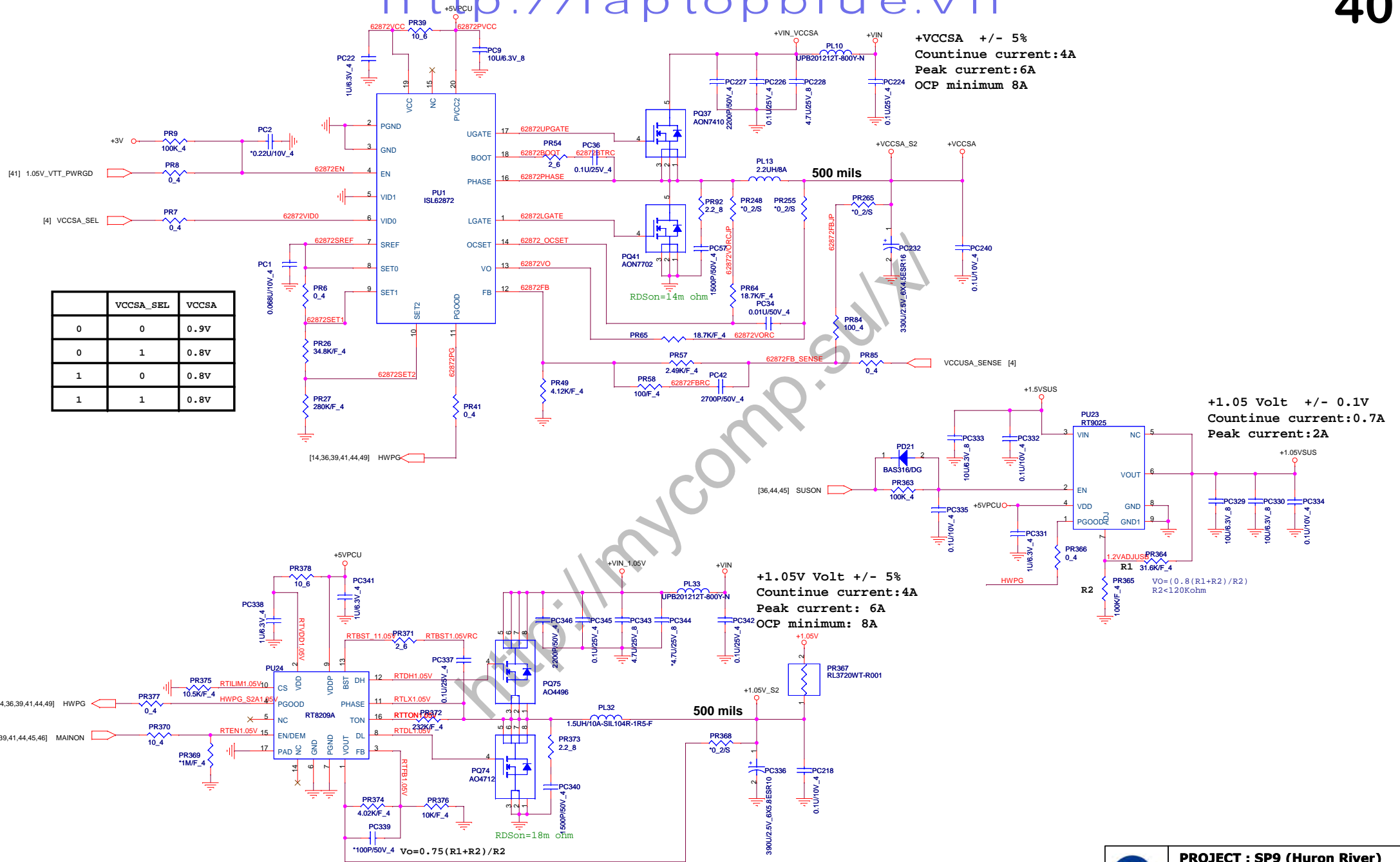
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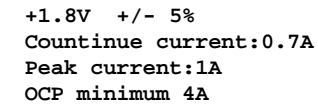
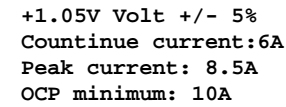


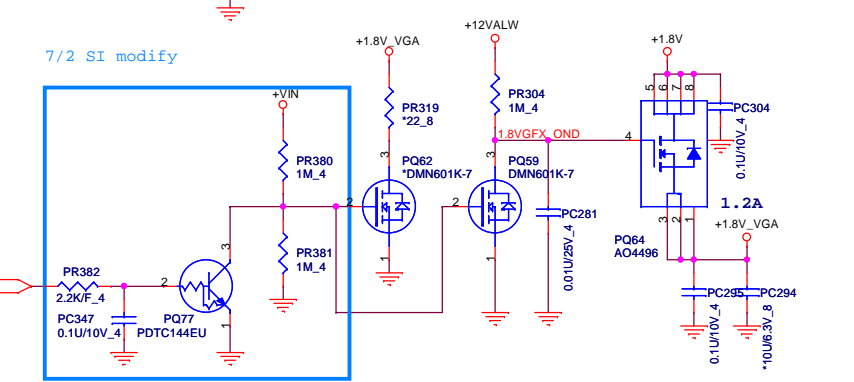
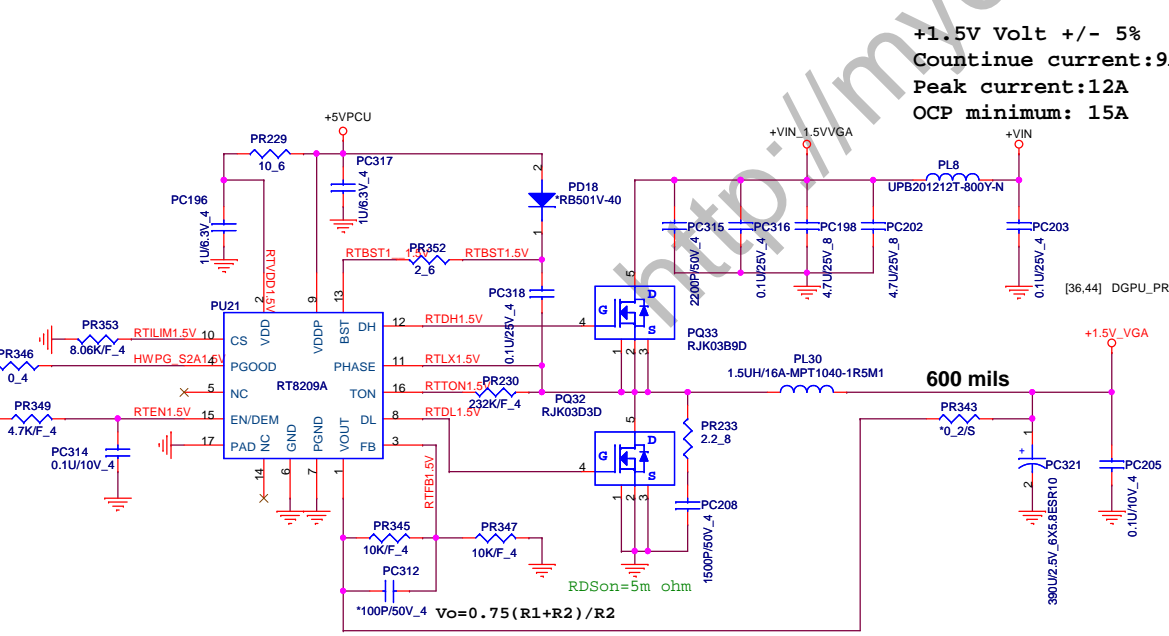
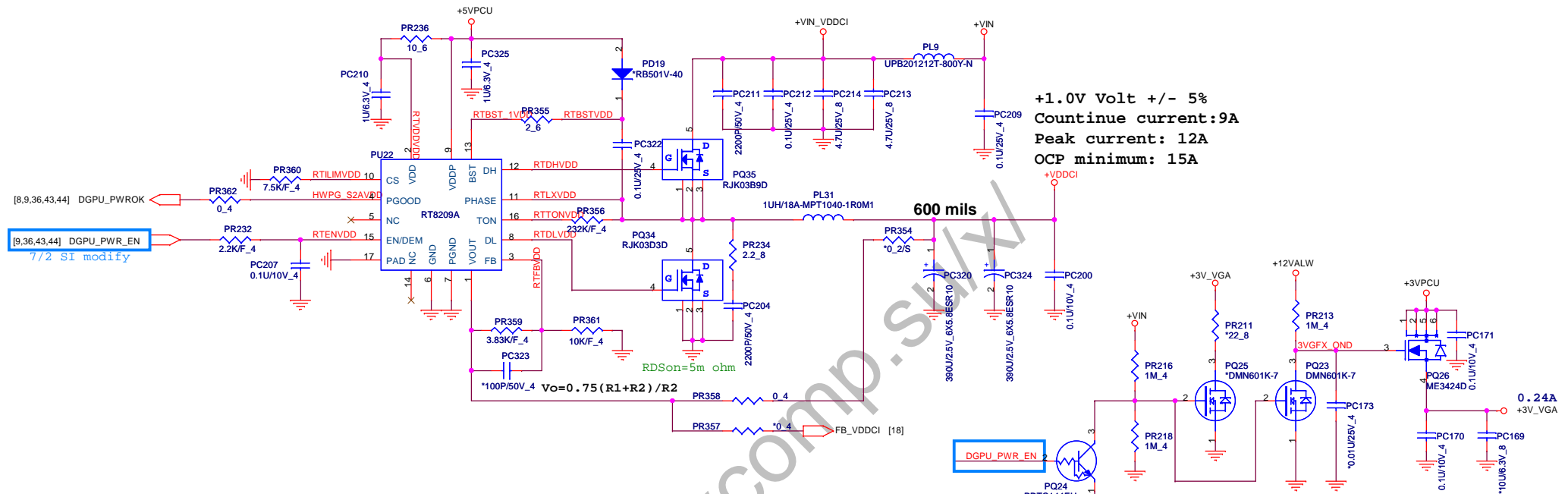
+5V +/- 5%
Continue current:5A
Peak current :6A
OCP minimum :7.5A

+3.3V +/- 5%
Continue current:5A
Peak current:6A
OCP minimum 7.5A





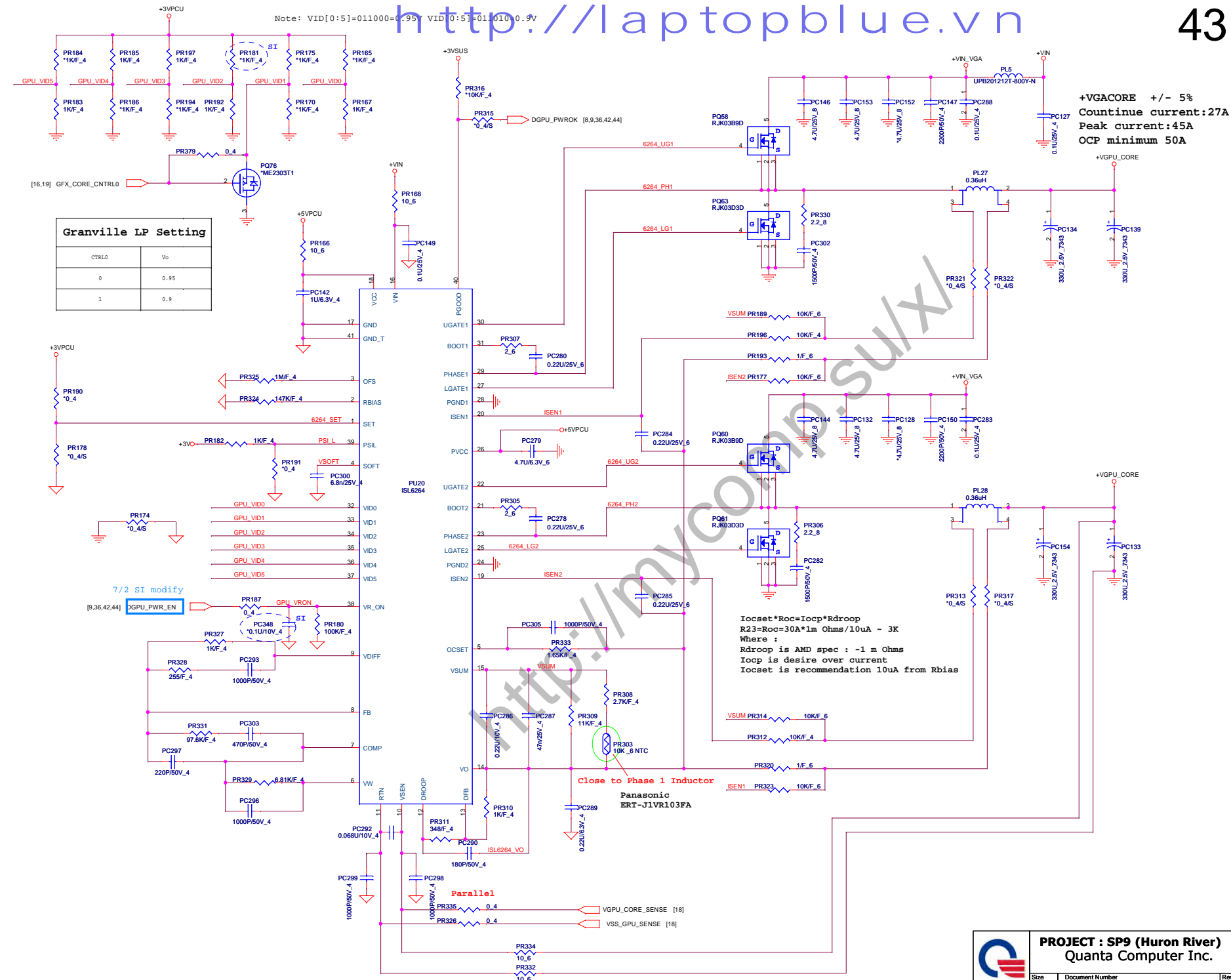




Note: VID[0:5]=011000=0.95 V ID[0:5]=011010=0.9V

Granville LP Setting

CTRL0	V0
0	0.95
1	0.9



+VGACORE +/- 5%
Countinue current:27A
Peak current:45A
OCP minimum 50A

$I_{ocset} \cdot R_{oc} = I_{ocp} \cdot R_{droop}$
 $R_{23} = R_{oc} = 30A \cdot 1m \text{ Ohms} / 10uA \sim 3K$
 Where :
 Rdroop is AMD spec : -1 m Ohms
 Iocp is desire over current
 Iocset is recommendation 10uA from Rbias

Close to Phase 1 Inductor
Panasonic
ERT-J1VR103FA

Parallel
VGPU_CORE_SENSE [18]
VSS_GPU_SENSE [18]

	PROJECT : SP9 (Huron River) Quanta Computer Inc.
---	--



8/3 SI modify

Countinue Peak current

1.5V V_{SUS}

PC206 100/6.3V_8

PC199 0.1u/10V_4

PC194 100/6.3V_8

PC195 100/6.3V_8

PC193 0.1u/10V_4

PC201 100/6.3V_4

PC197 1u/6.3V_1

PR235 10K/F_4

PR231 100K/F_4

PR227 26.7K/F_4

PR228 100K/F_4

R1 26.7K/F_4

R2 100K/F_4

VIN 3

NC 5

VOUT 6

EN 2

VDD 4

PGOOD 1

GND 8

GND1 9

5V PCU

1.0V V_{GA}

[9,36] DGPU_PWR_EN

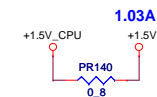
[36,42,43] DGPU_PR_EN

[8,9,36,42,43] DGPU_PWROK

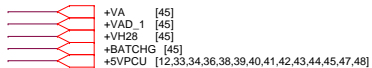
1.2V ADJ1

VO = (0.8(R1+R2)/R2)

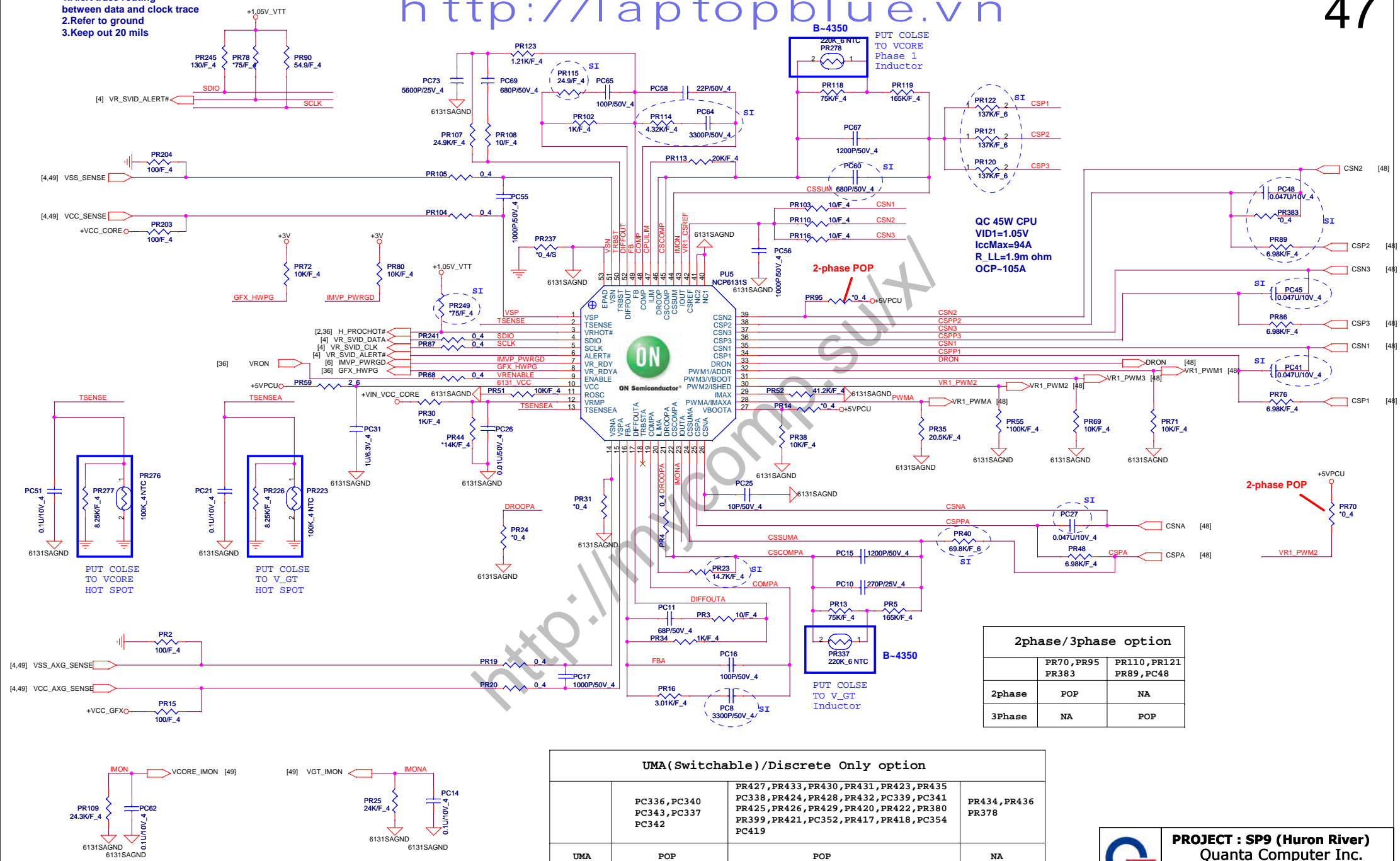
R2 < 120Kohm



Do Not add test pad on BATDIS_G signal



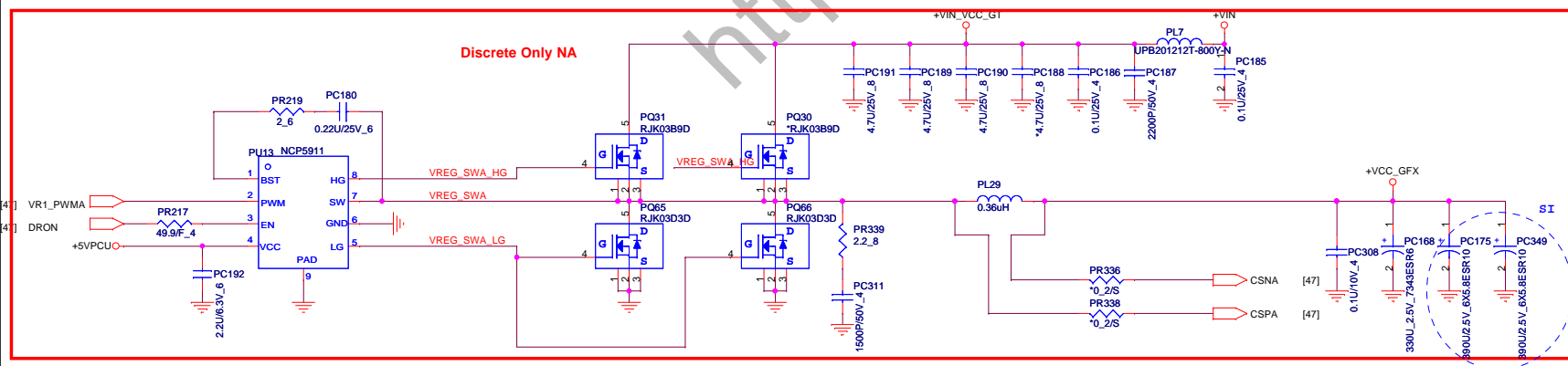
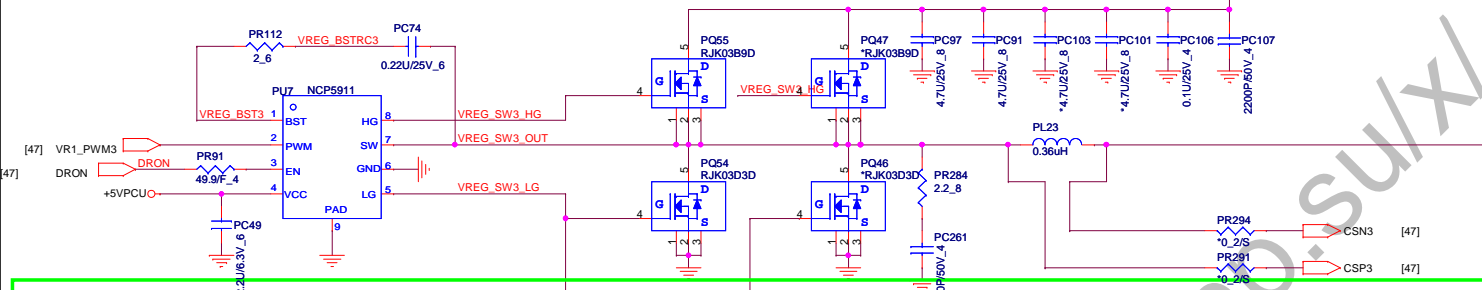
- 1.Alert trace routing between data and clock trace
- 2.Refer to ground
- 3.Keep out 20 mils

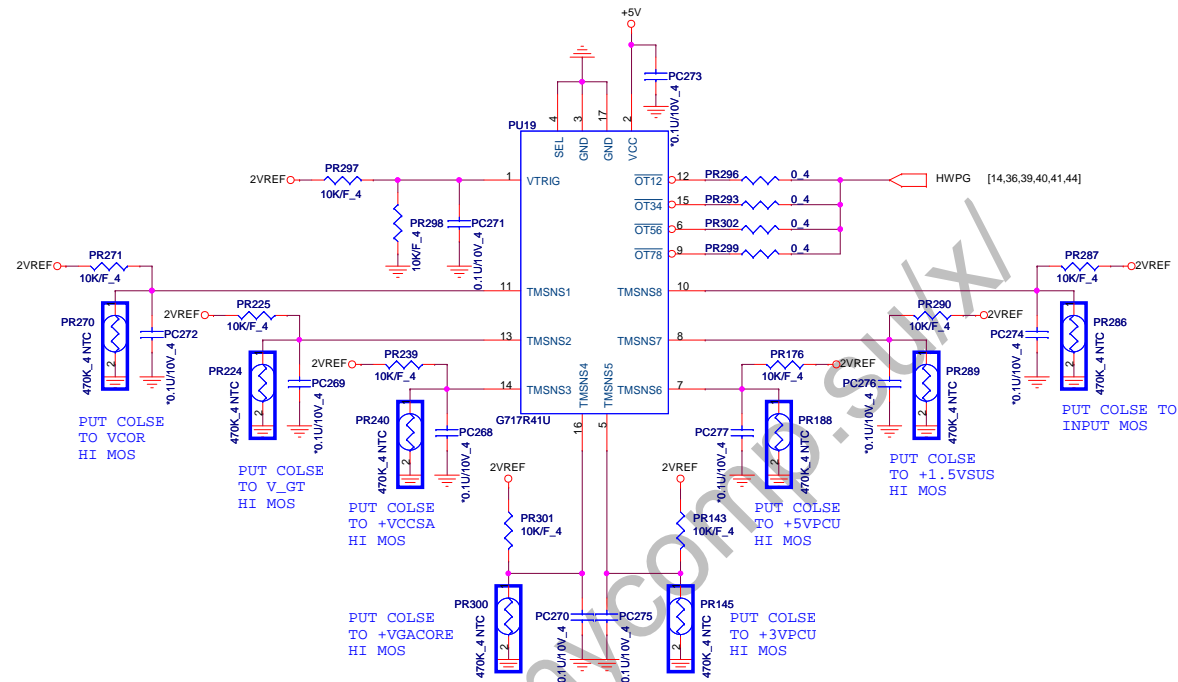


2phase/3phase option		
	PR70,PR95 PR383	PR110,PR121 PR89,PC48
2phase	POP	NA
3Phase	NA	POP

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 Quanta Computer Inc.

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Vender	Size	P/N
EON	128KB	512KB
Winbond	128KB	512KB
Socket		