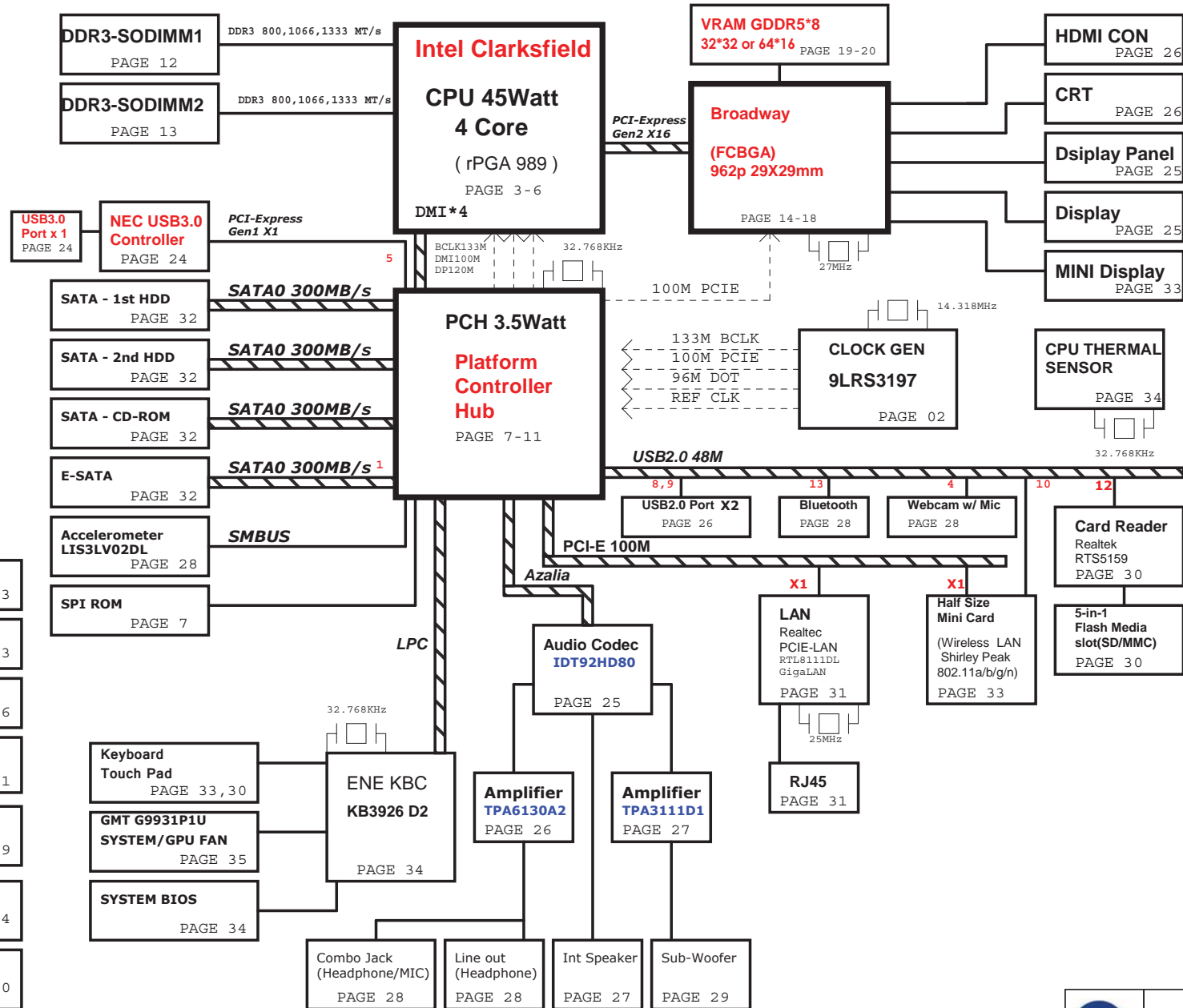


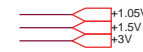
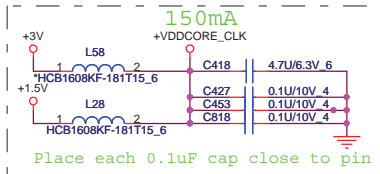
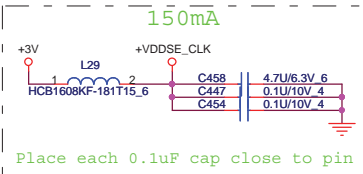
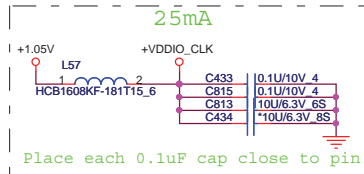
PCB STACK UP

Discrete 6L

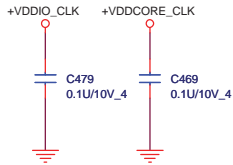
LAYER 1 : TOP
 LAYER 2 : SGND
 LAYER 3 : IN1(High)
 LAYER 4 : IN2(High)
 LAYER 5 : SVCC
 LAYER 6 : Bottom

SP8 BLOCK DIAGRAM



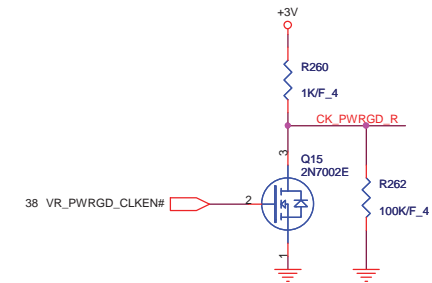
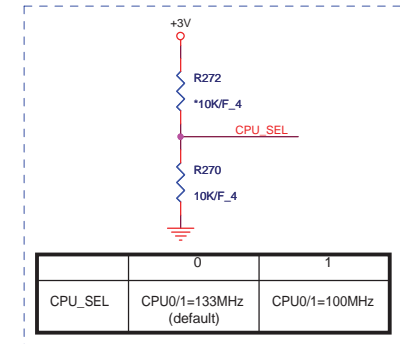
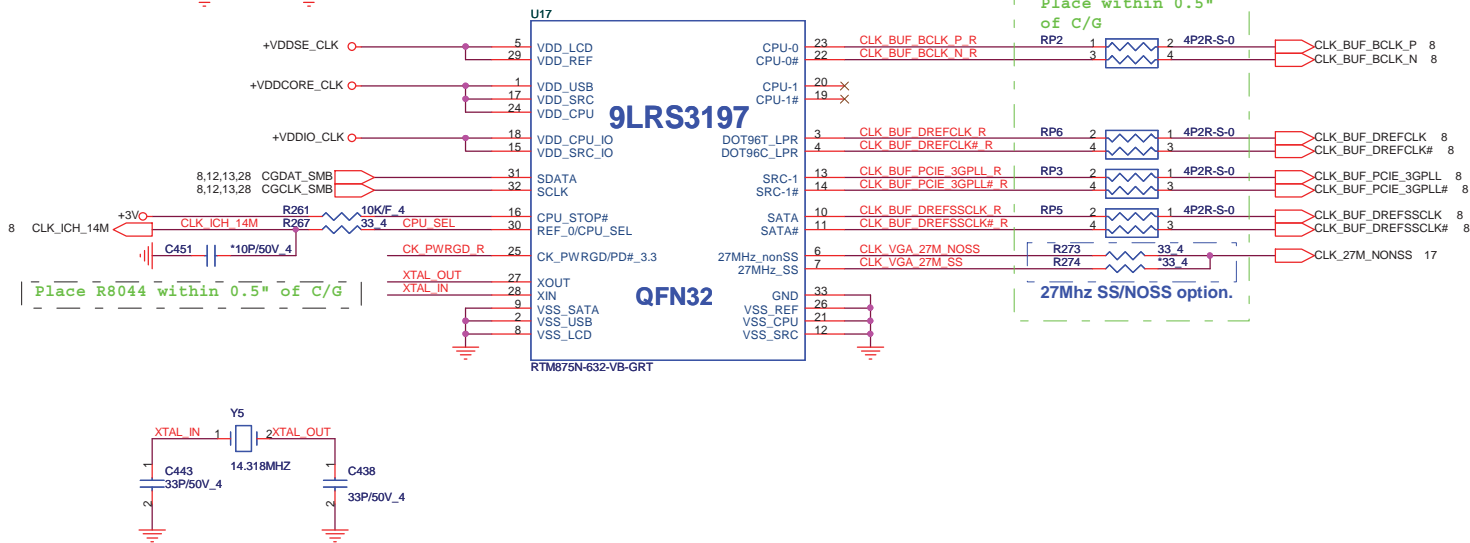


7,8,9,11,37,38
35,42
3,7,8,9,10,11,12,13,14,17,25,26,27,28,30,31,32,33,34,35,38,40,42



SI Add C479 and C469 for EMI request

change to power saving
CLK need change to +1.5V
support



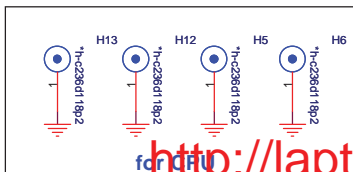
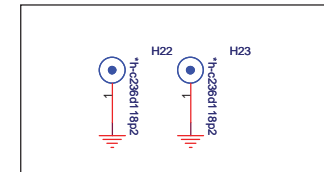
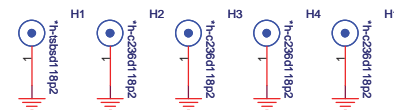
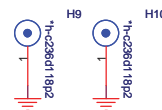
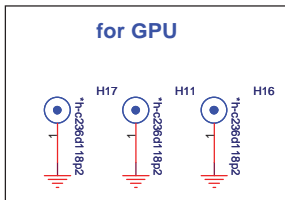
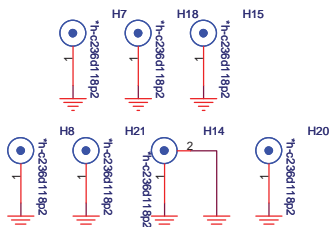
HOLDS

for GPU

SI ME change Footprint

SI for ME change footprint

SI add for PCH hole

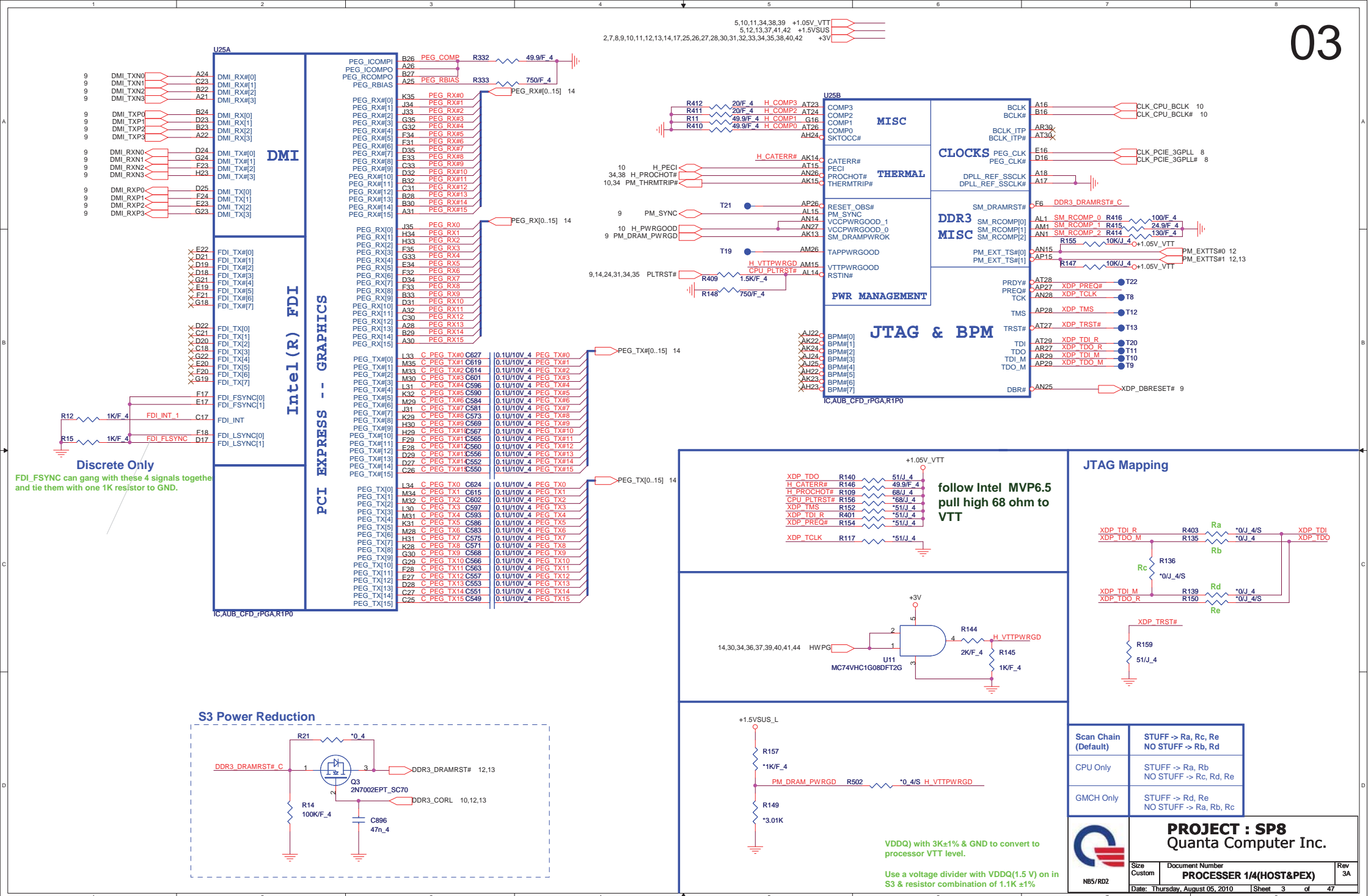


<http://laptop-motherboard-schematic.blogspot.com/>

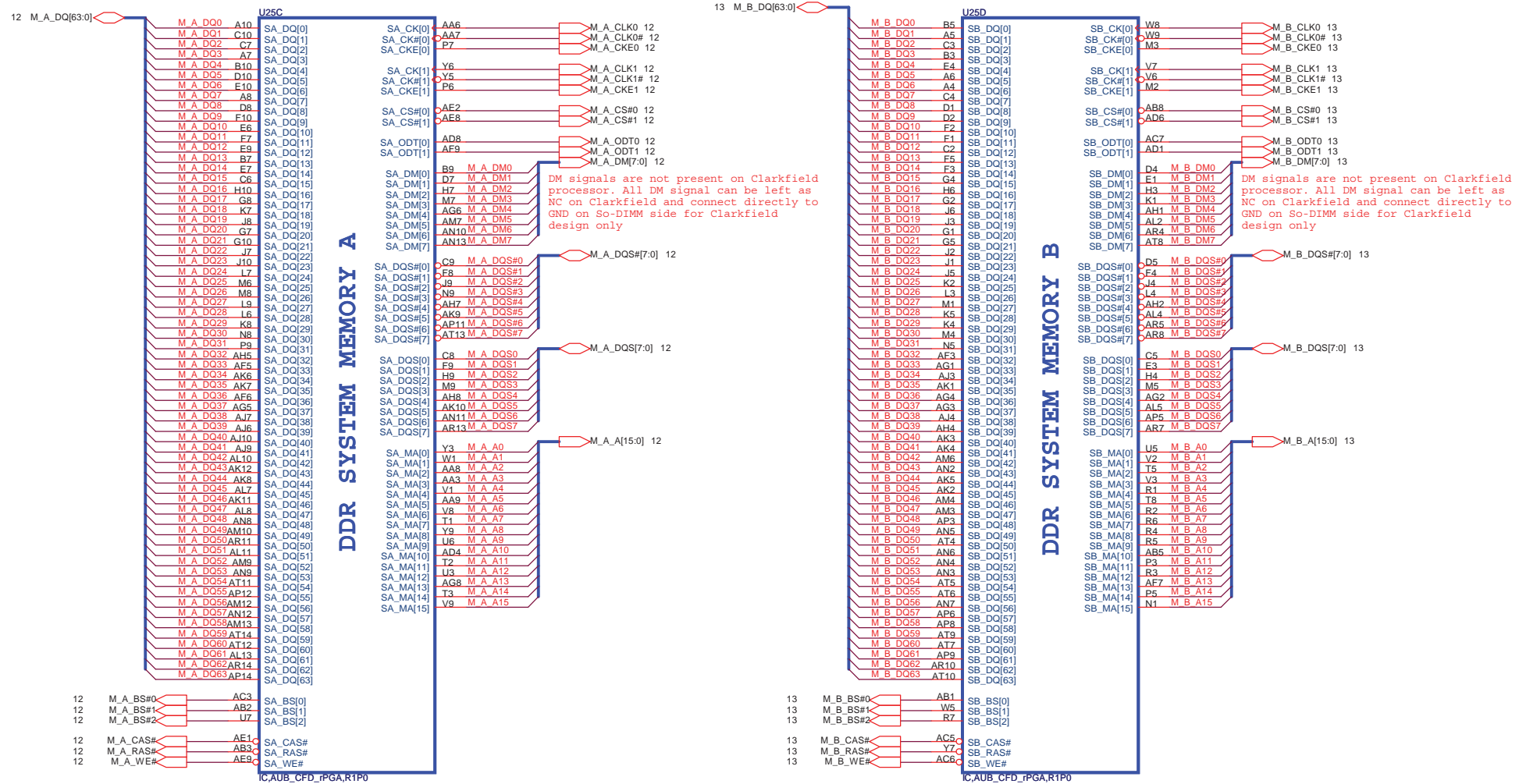


PROJECT : SP8
Quanta Computer Inc.

Size Custom	Document Number	Rev 3A
	Clock Gen(9LRS3197)/HOLES	
Date: Thursday, August 05, 2010	Sheet 2 of 47	

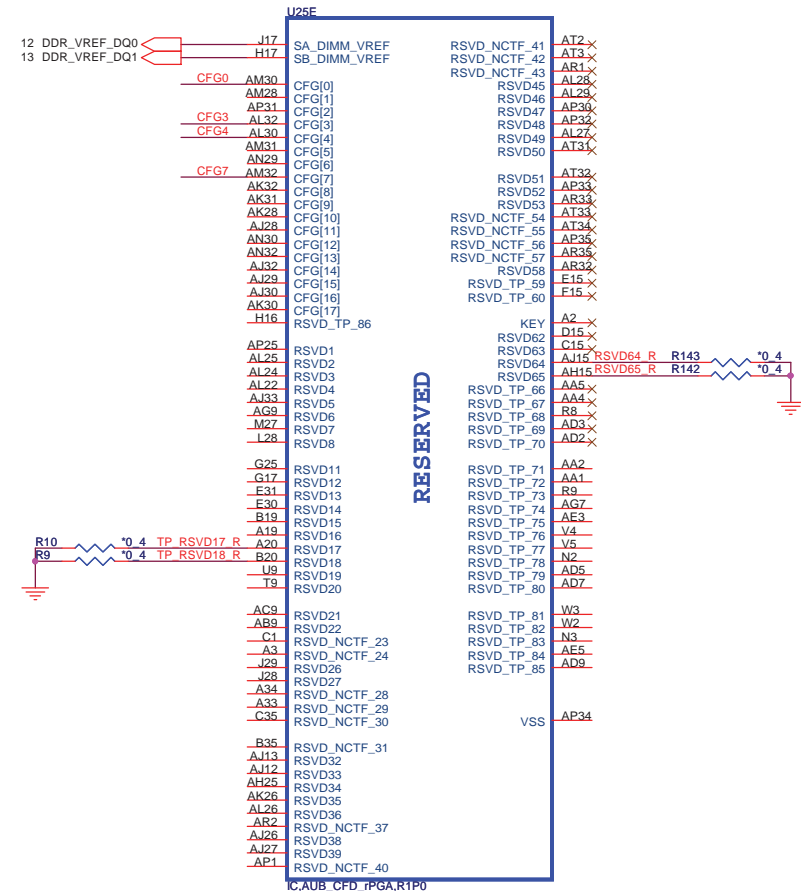
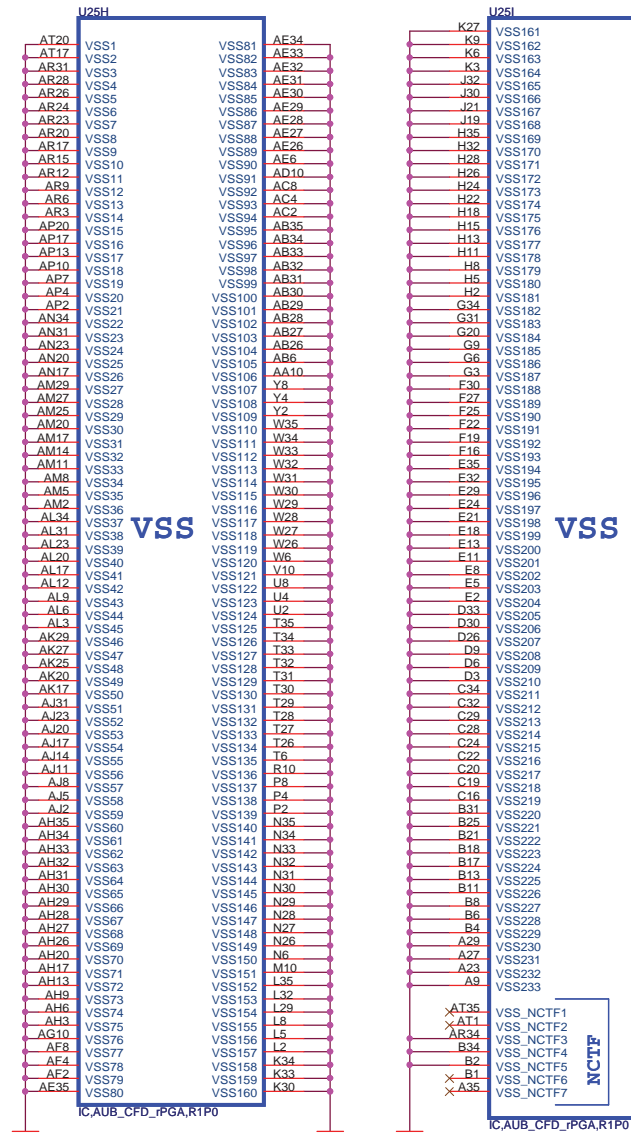


AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



For Discrete only



CFG[1:0] - PCI_Epress Configuration Select
 * 11= 1 x 16 PEG
 * 10= 2 x 8 PEG



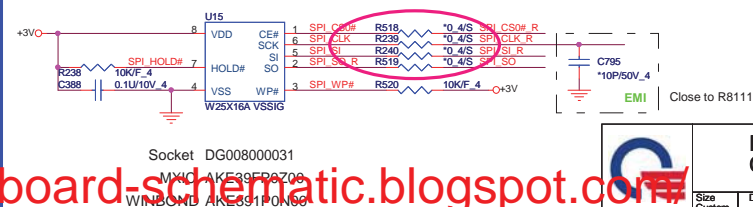
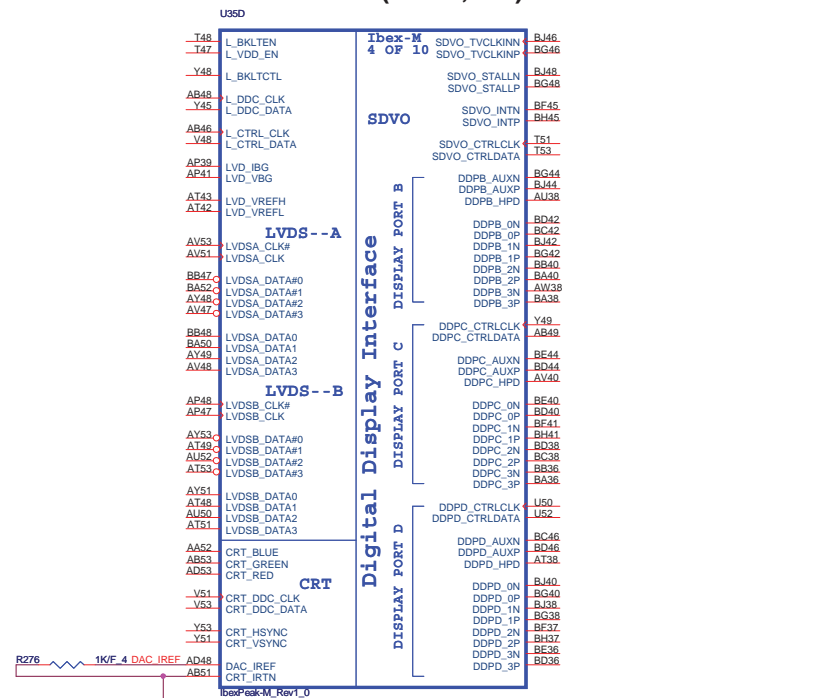
PROJECT : SP8
Quanta Computer Inc.

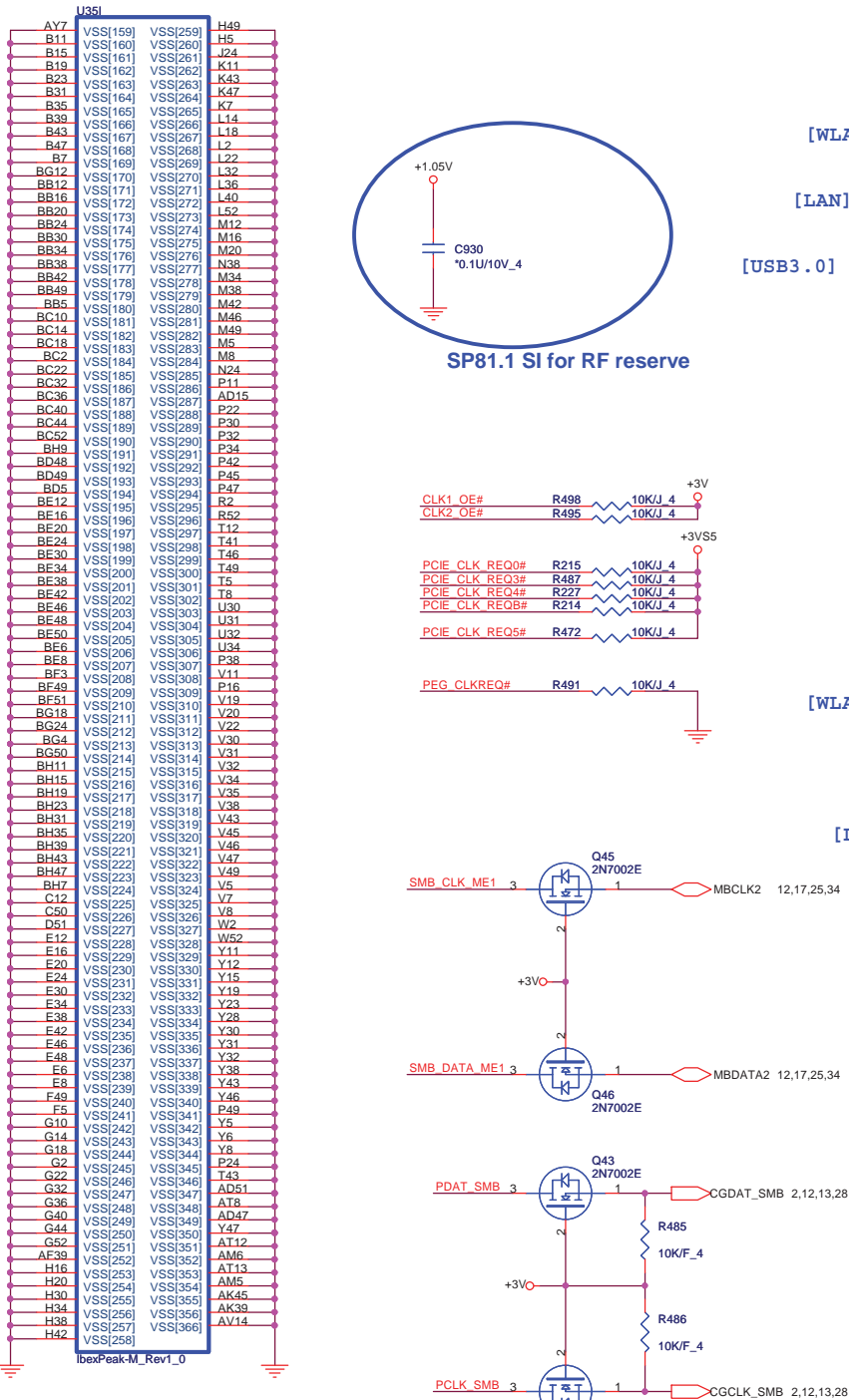
Size Custom Document Number
PROCESSOR 4/4 (GND)
 Date: Thursday, August 05, 2010 Sheet 6 of 47

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

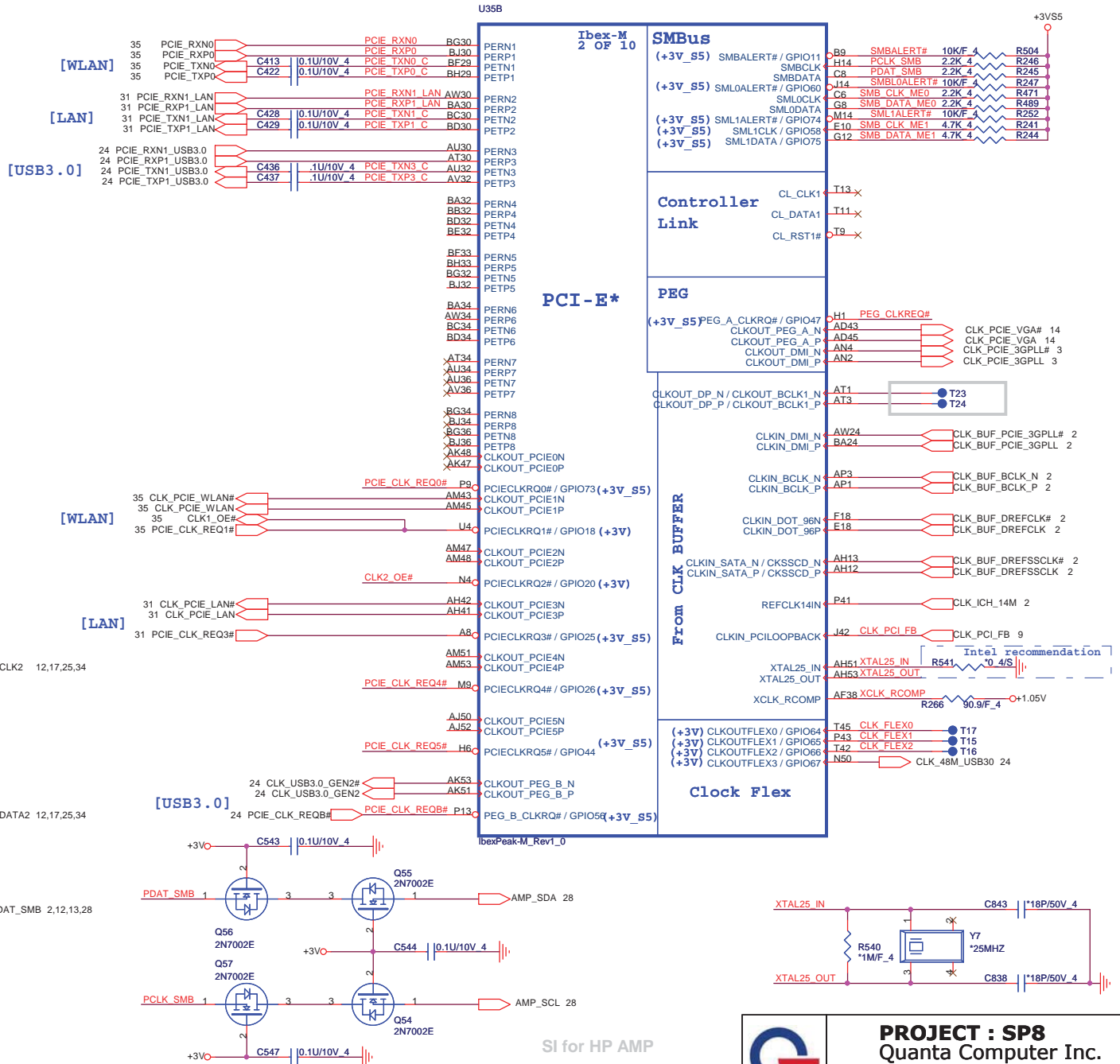
<http://laptop-motherboard-schematic.blogspot.com/>

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



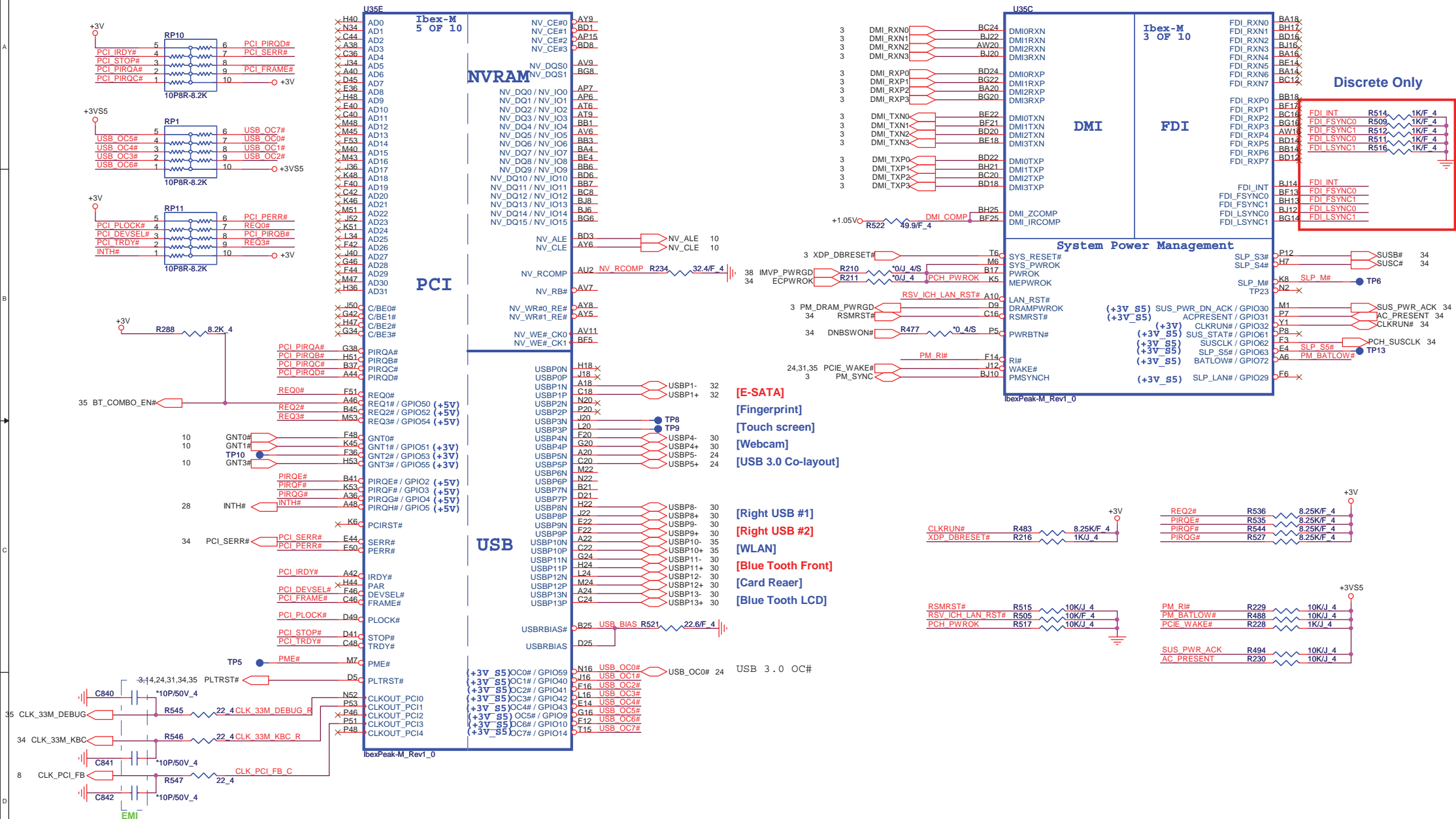


IBEX PEAK-M (PCI-E,SMBUS,CLK)



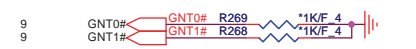
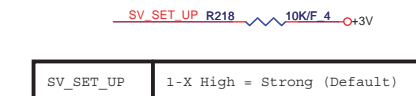
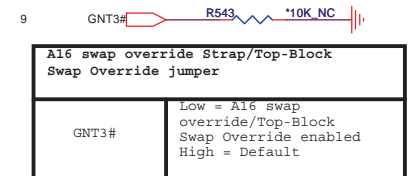
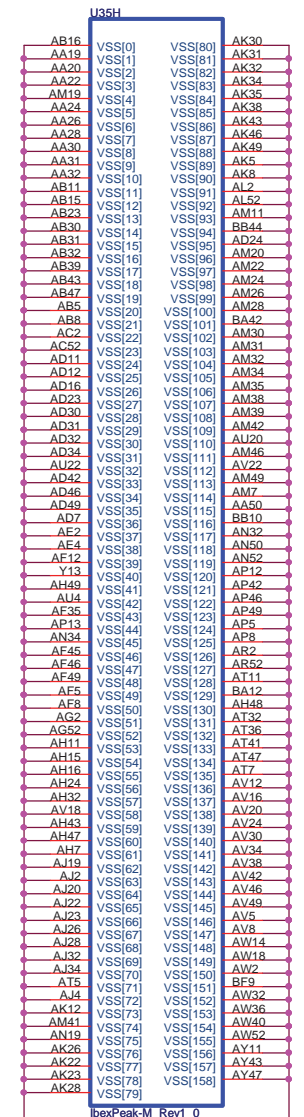
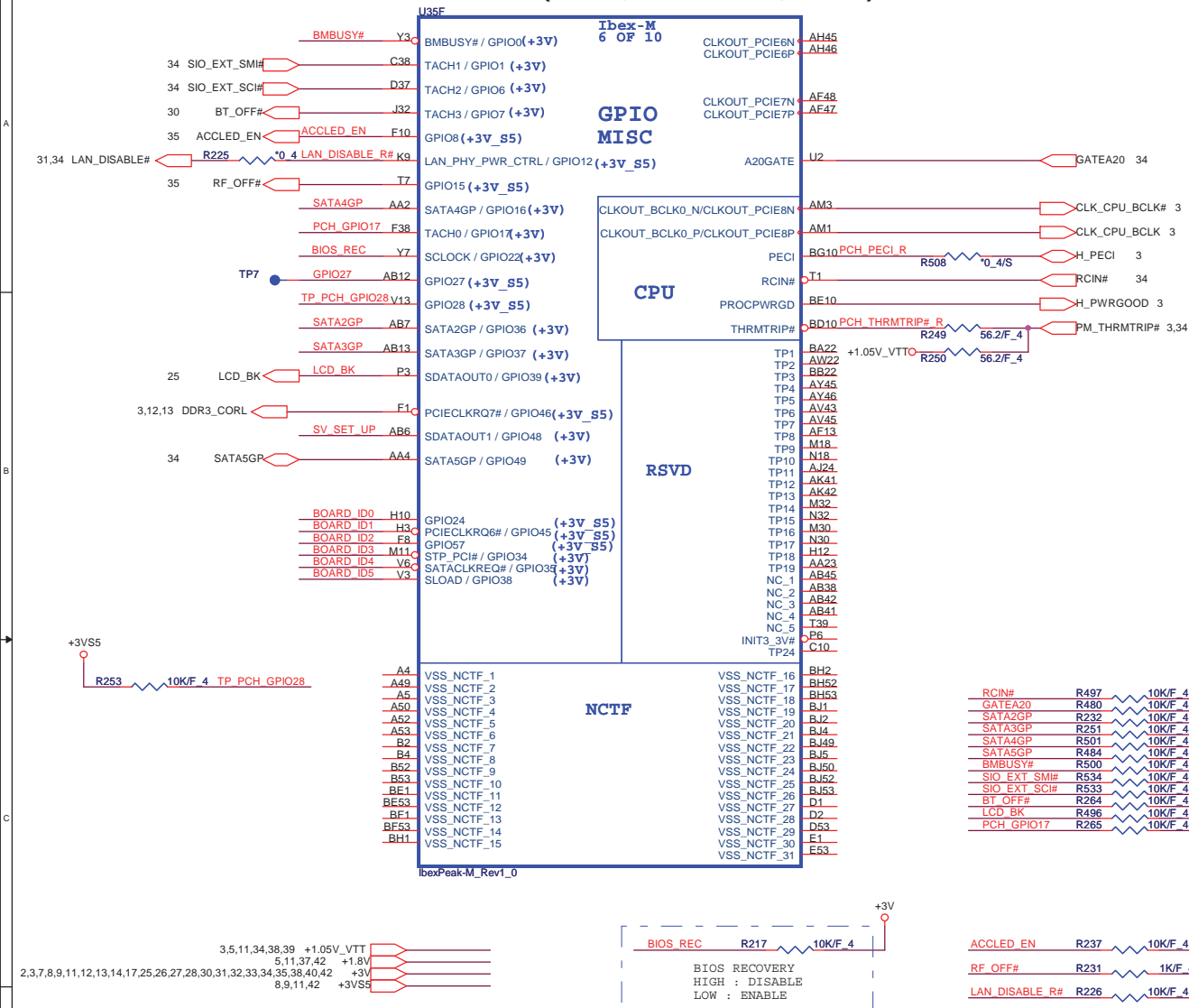
IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (DMI,FDI,GPIO)



IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

IBEX PEAK-M (GND)



Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SP1



Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH



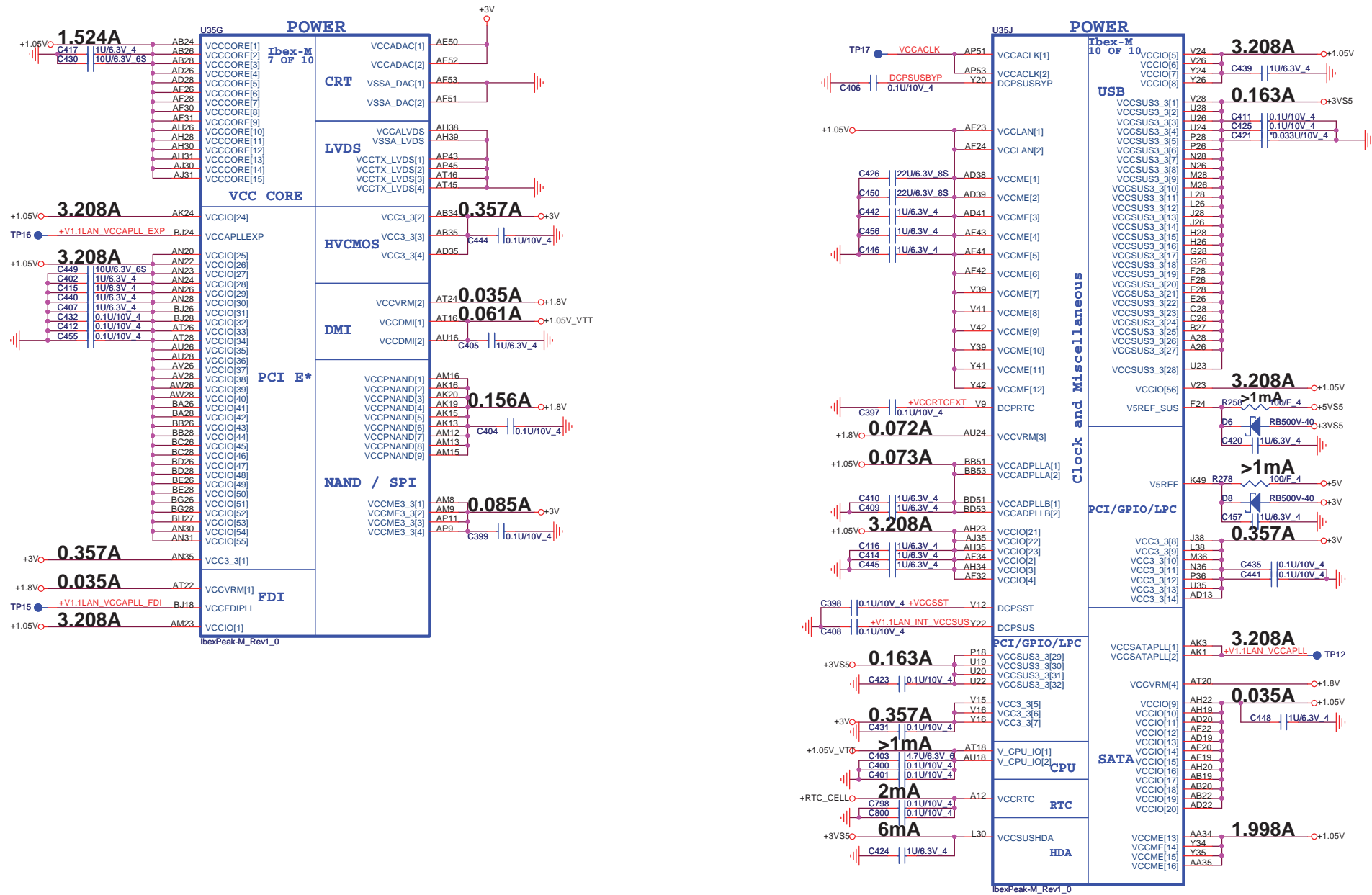
PROJECT : SP8		
Quanta Computer Inc.		
Size Custom	Document Number	Rev 3A
	PCH 4/5 (GPIO & Strap)	
Date: Thursday, August 05, 2010	Sheet 10 of 47	

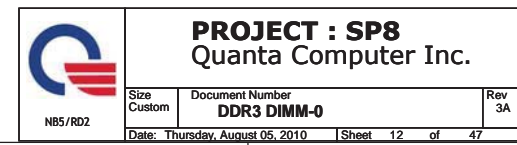
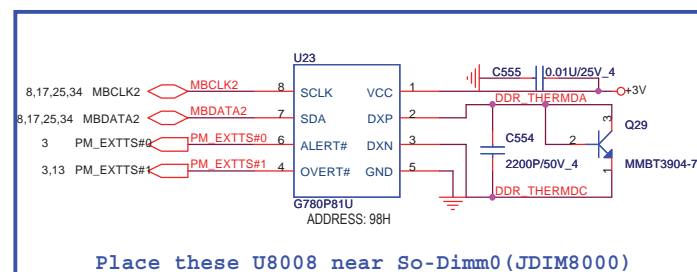
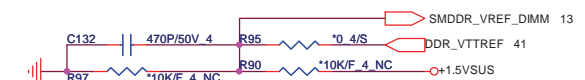
BOARD ID SETTING

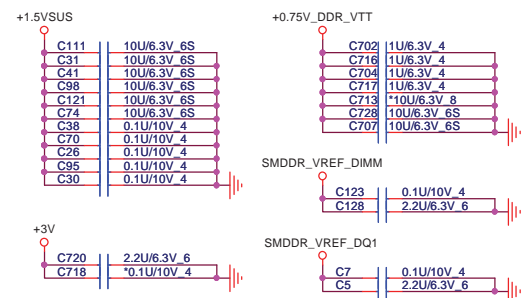
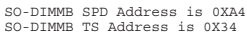
Board ID	ID5	ID4	ID3	ID2	ID1	ID0
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RD1 (0)	RU0 (1)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RD0 (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RU0 (1)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RD0 (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RU0 (1)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RD0 (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RU0 (1)

Board ID	ID0	ID1	ID2	ID3	ID4	ID5
	GPIO 24	GPIO 45	GPIO 57	GPIO 34	GPIO 35	GPIO 38
SP8	0	0			0	0
SP8 1.1	0	0			1	0
Discrete			0	0		
Reserve			0	0		
ROM Size				0= 4M		

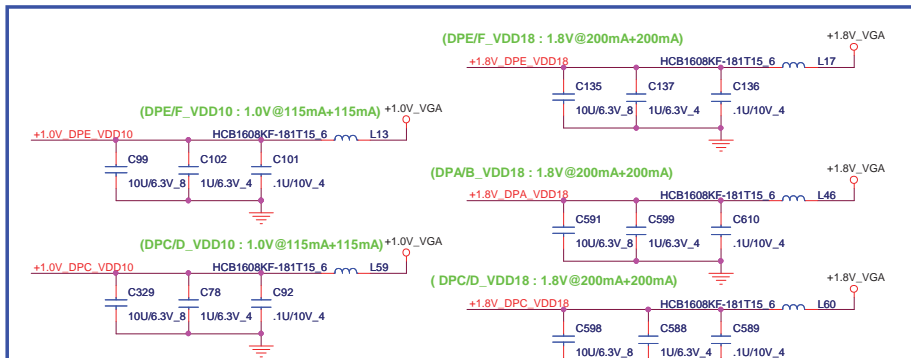
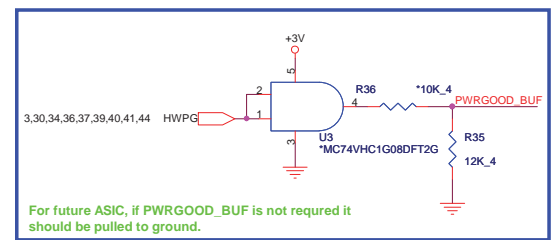
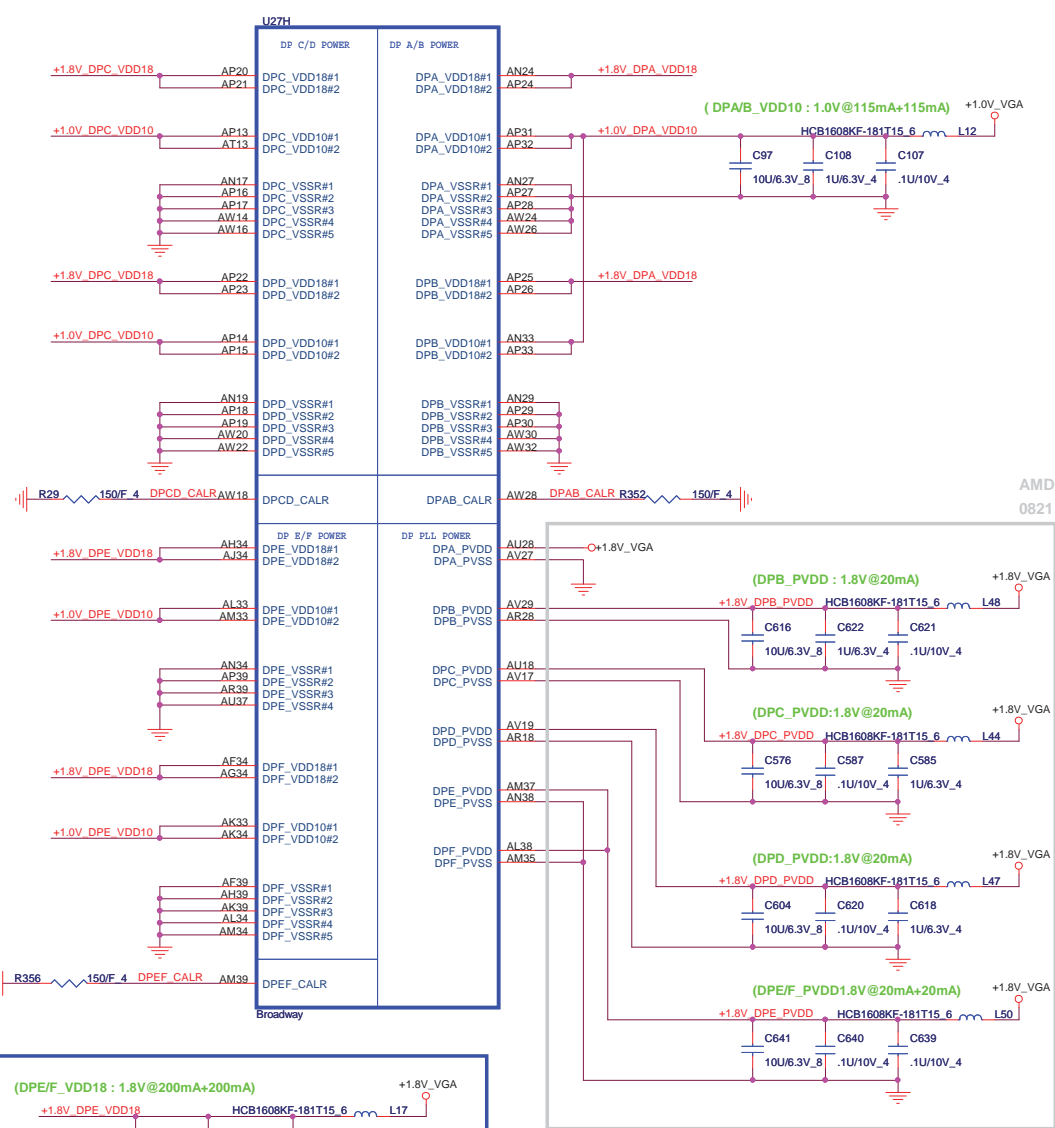
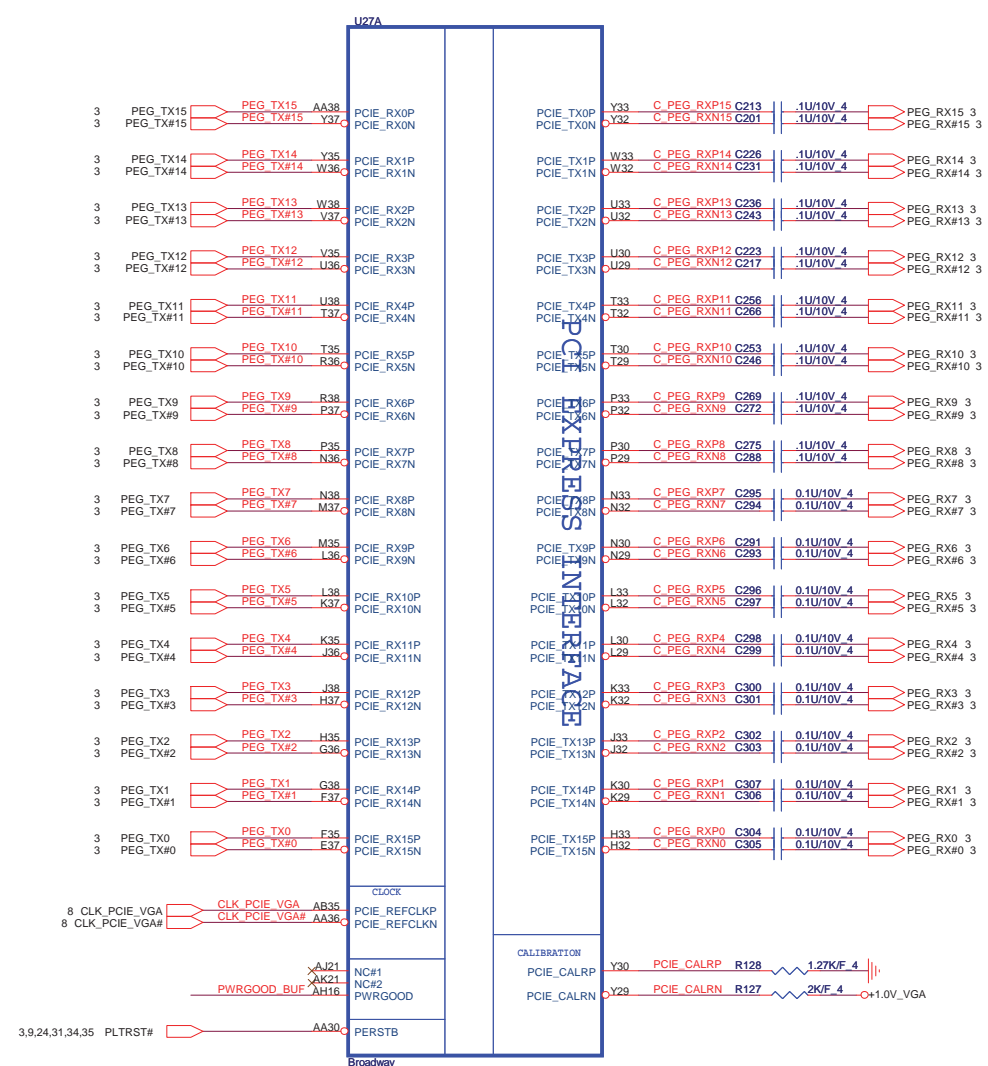


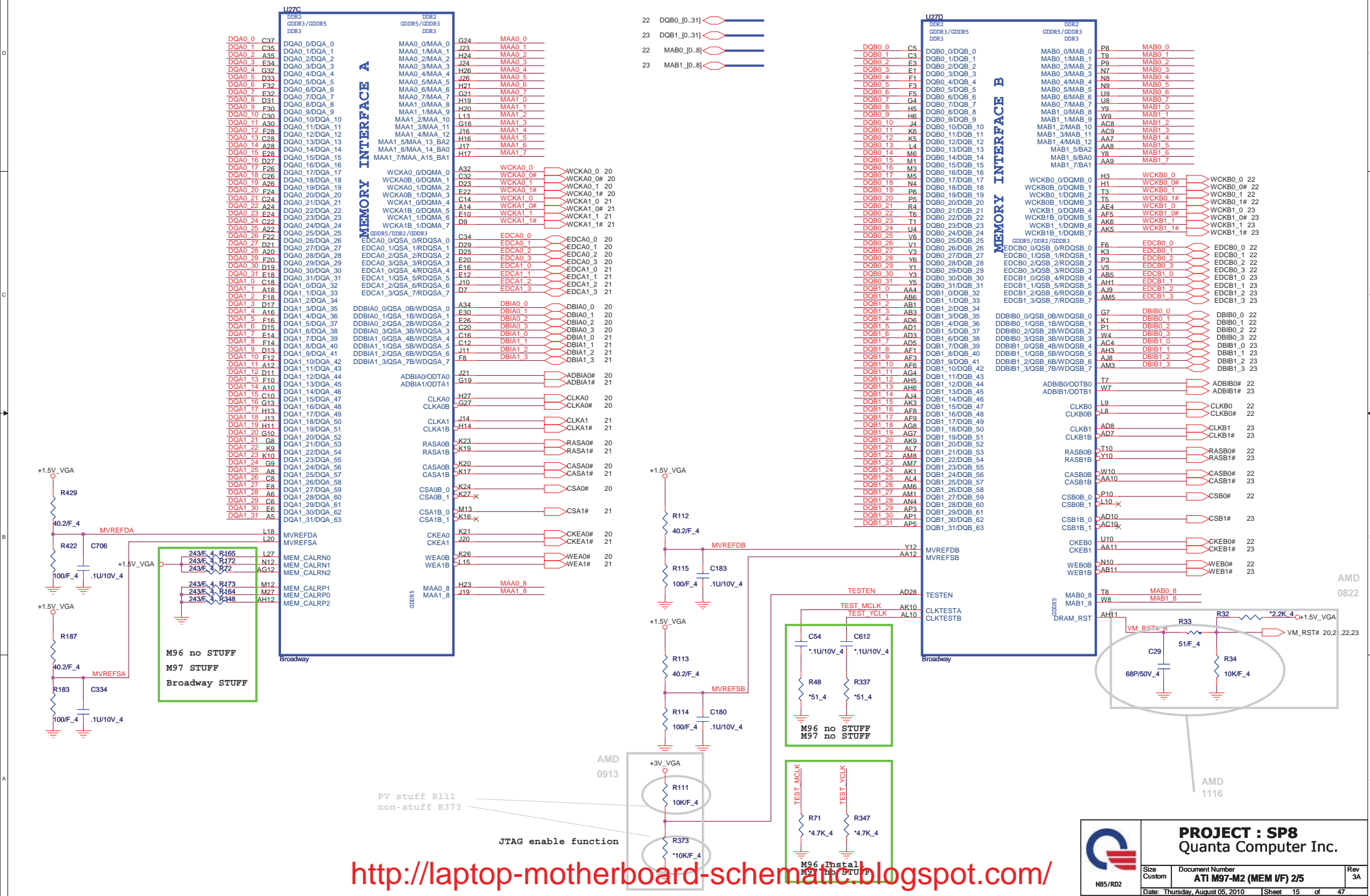


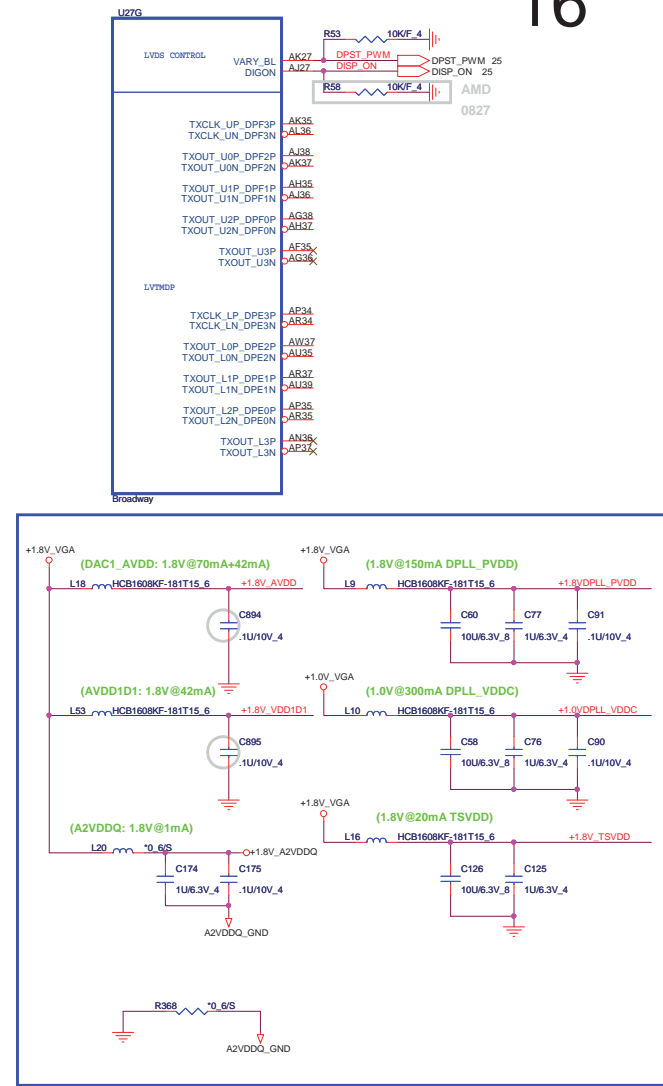




Size Custom	Document Number DDR3 DIMM-1	Rev 3A
Date: Thursday, August 05, 2010		Sheet 13 of 47



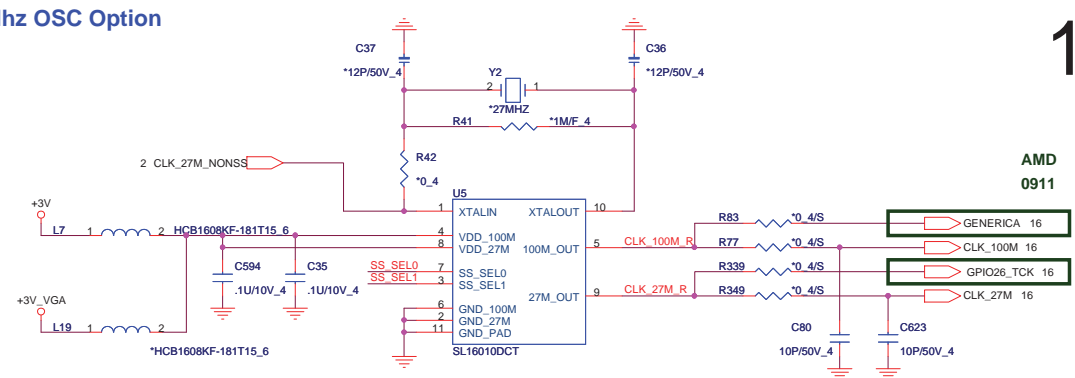
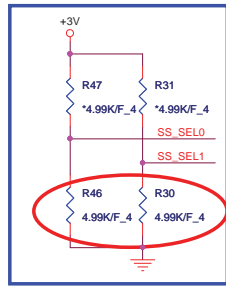




MEM ID	3	2	1	0	Verona		
DVPDATA	3	2	1	0	DDR5 Type	Configuration	Size
1	0	0	0	1	Samsung K4G10325FE-HC05 (4.0Gbps)	32*32 or 64*16 x 8 pcs	1G
2	0	0	1	0	Hynix H5GQ1H24AFR-T0C BGA (4.0Gbps)	32*32 or 64*16 x 8 pcs	1G
3	0	0	1	1			

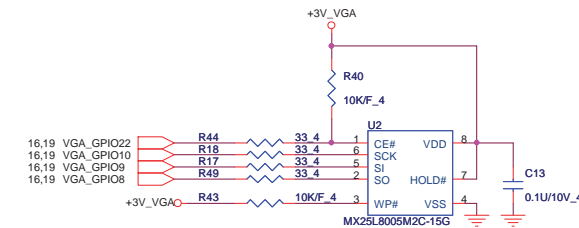
AMD
0911

27MHz + 100MHz OSC Option

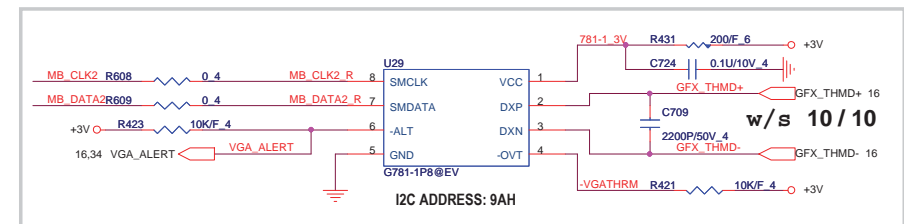
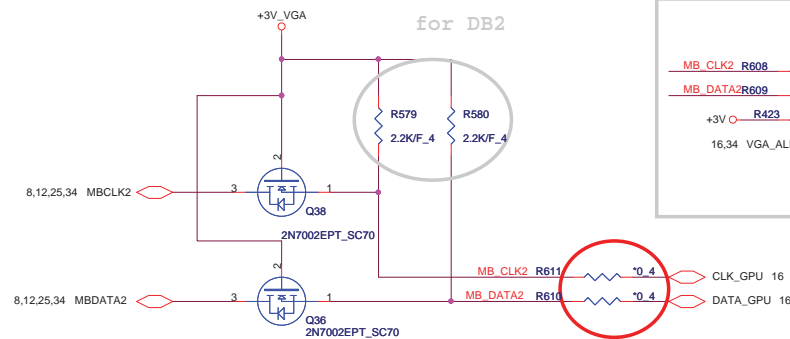


SS_SEL1	SS_SEL0	Spread Percent (%) SS_CLK (PIN 5)
LOW	LOW	Spread Off
LOW	Middle	-0.5%
LOW	High	-2.5%
Middle	LOW	-0.25%
Middle	Middle	-0.75%
Middle	High	-1.0%
High	LOW	-1.5%
High	Middle	-2.0%
High	High	-3.0%

Ext EEPROM



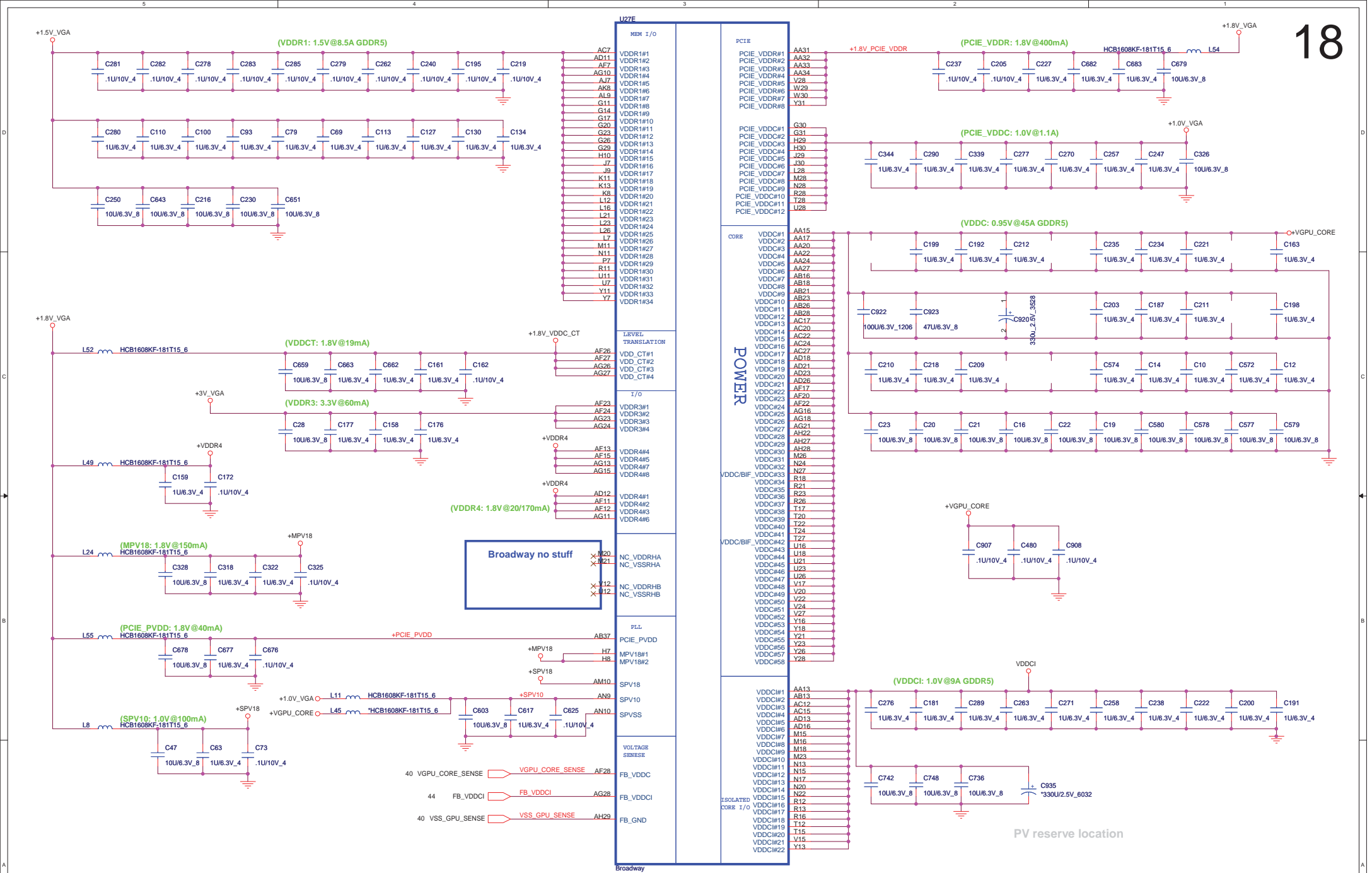
Thermal Sensor



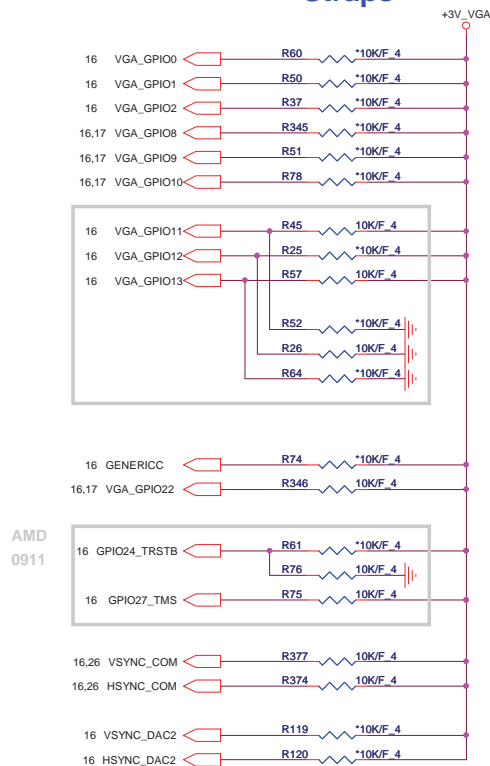
PROJECT : SP8
Quanta Computer Inc.

Size Custom	Document Number ATI M97(GND&Str&Ther)4/5	Rev 3A
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<http://laptop-motherboard-schematic.blogspot.com/>



Straps



Overlap pads to save space
and to prevent assembly of
both resistors.

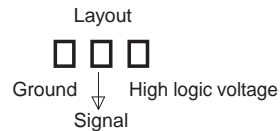


Table 3-34 ROM Configurations

Manufacturer	Part Number	Size	CONFIG[2:0]
Atmel	AT25F512	512 kbit	001
	AT25F512A	512 kbit	010
	AT25F1024	1 Mbit	011
	AT25F1024A	1 Mbit	011
	AT25F2048	2 Mbit	011
	AT25F4096	4 Mbit	011
ST Microelectronics	M25P05A	512 kbit	100
	M25P10A	1 Mbit	101
	M25P20	2 Mbit	101
	M25P40	4 Mbit	101
	M25P80	8 Mbit	101
Silicon Storage Technology	SST25VF512	512 kbit	010
	SST25VF010	1 Mbit	011
	SST25VF020	2 Mbit	011
	SST25VF040	4 Mbit	011
Winbond Electronics Corporation	W45B512	512 kbit	110
	W45B012	1 Mbit	111
YMC	Y25LF05	512 kbit	010
	SA25C020	2 Mbit	011
PMC	Pm25LV512	512 kbit	100
	Pm25LV010	1 Mbit	101

Default

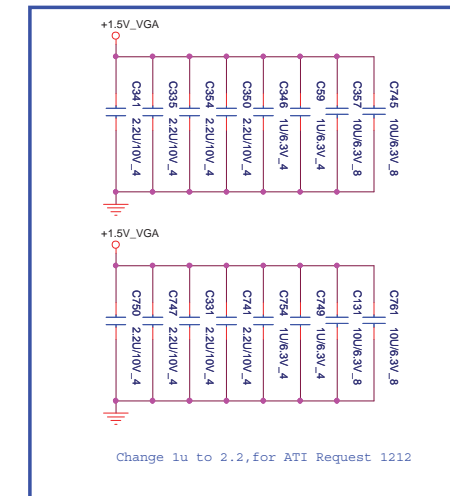
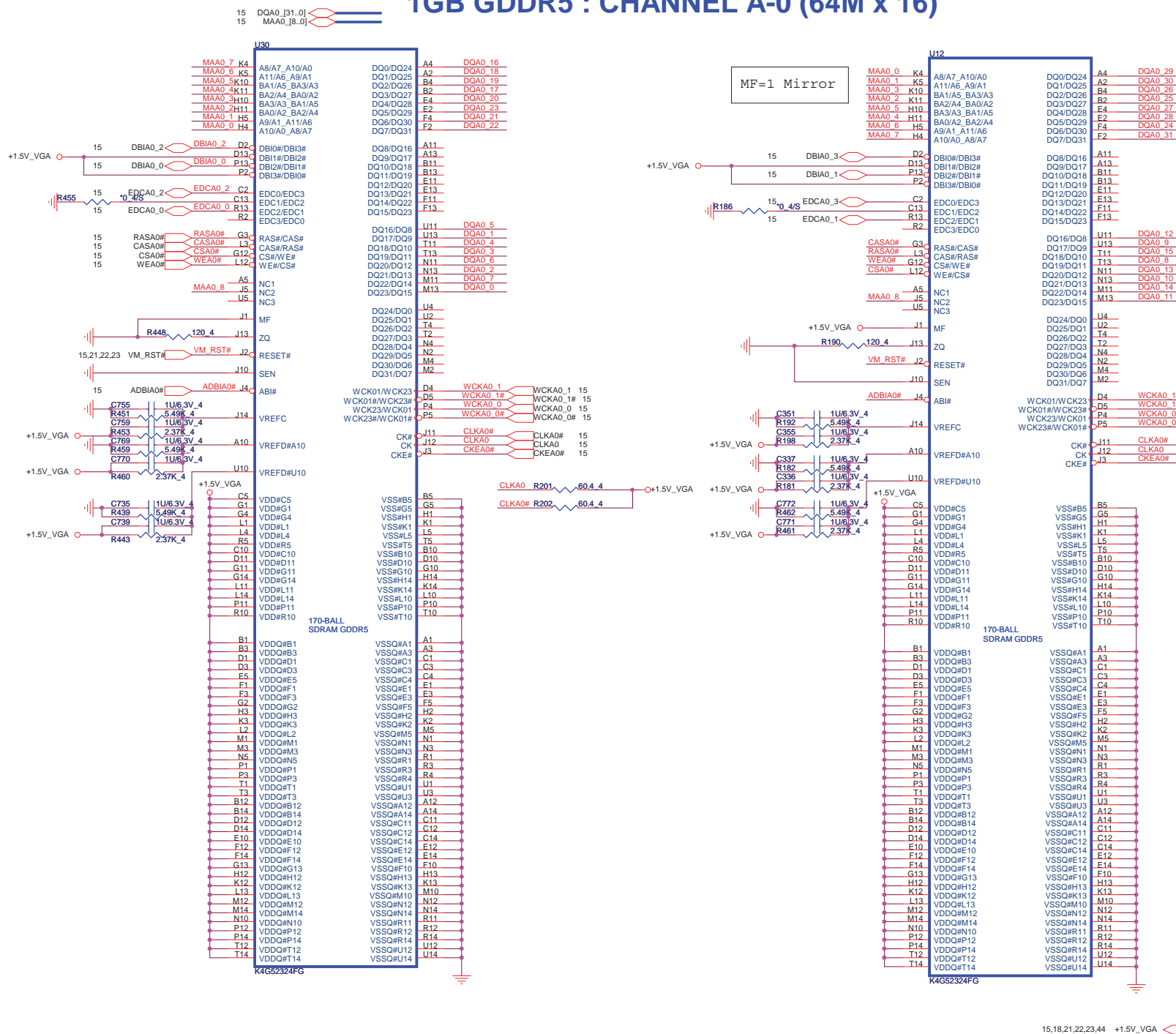
Strap Name	Pin	Straps Description	Default Value
TX_PWRS_ENB	GPIO0	GPIO[1:0]:Recommend to pulling up for PICE setting. GPIO_0:PCIE full TX output swing	
TX_DEEMPH_EN	GPIO1	GPIO_1:PCIE Transmitter DE-EMPHASIS enabled	
BIF_GEN2_EN	GPIO2	GPIO_2:System is using PCIE GEN1 can be let it NC(ASIC internal pull down) if Gen2 just pull up for PCIE 5GT/s support. (0=PCIE GNE1,2.5GT/s ; 1=PCIE GNE2,5GT/s)	
STRAP_BIF_CLK_PM_EN	GPIO8		
CONFIG[3] CONFIG[2] CONFIG[1] CONFIG[0]	GPIO9 GPIO13 GPIO12 GPIO11		
BIOS_ROM_EN	GPIO22	BIOS_ROM_EN(GPIO22)=1, then Config[2:0]=GPIO[13:12:11] defines the ROM type. (See table as below)	
AUDIO[0]	VSYNC		
AUD(1)	HSYNC		
VSYNC_DAC2	V2SYNC		
HSYNC_DAC2	H2SYNC		
	GENERICC		



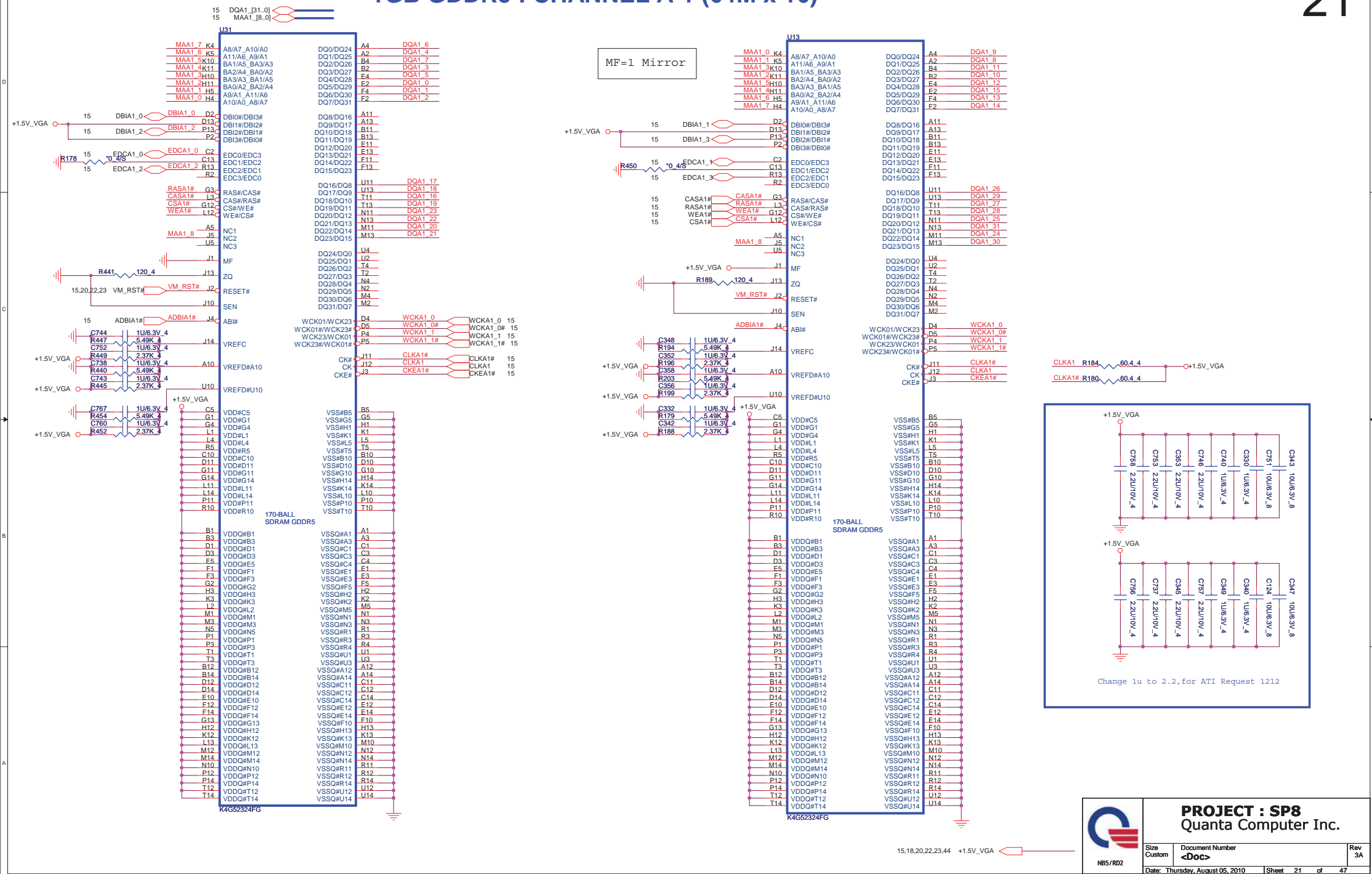
PROJECT : SP8
Quanta Computer Inc.

Size Custom Document Number
VGA Core/+1.8VGFX/1.0VGFX Rev 3A
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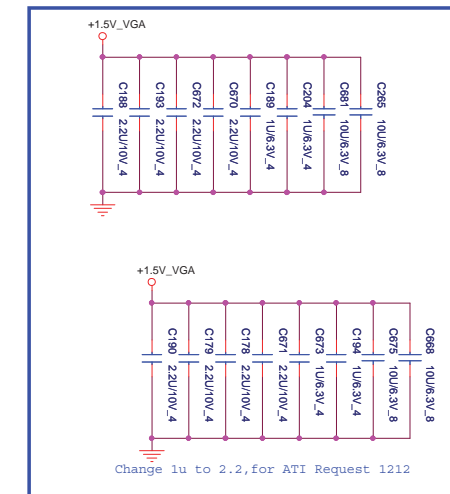
1GB GDDR5 : CHANNEL A-0 (64M x 16)



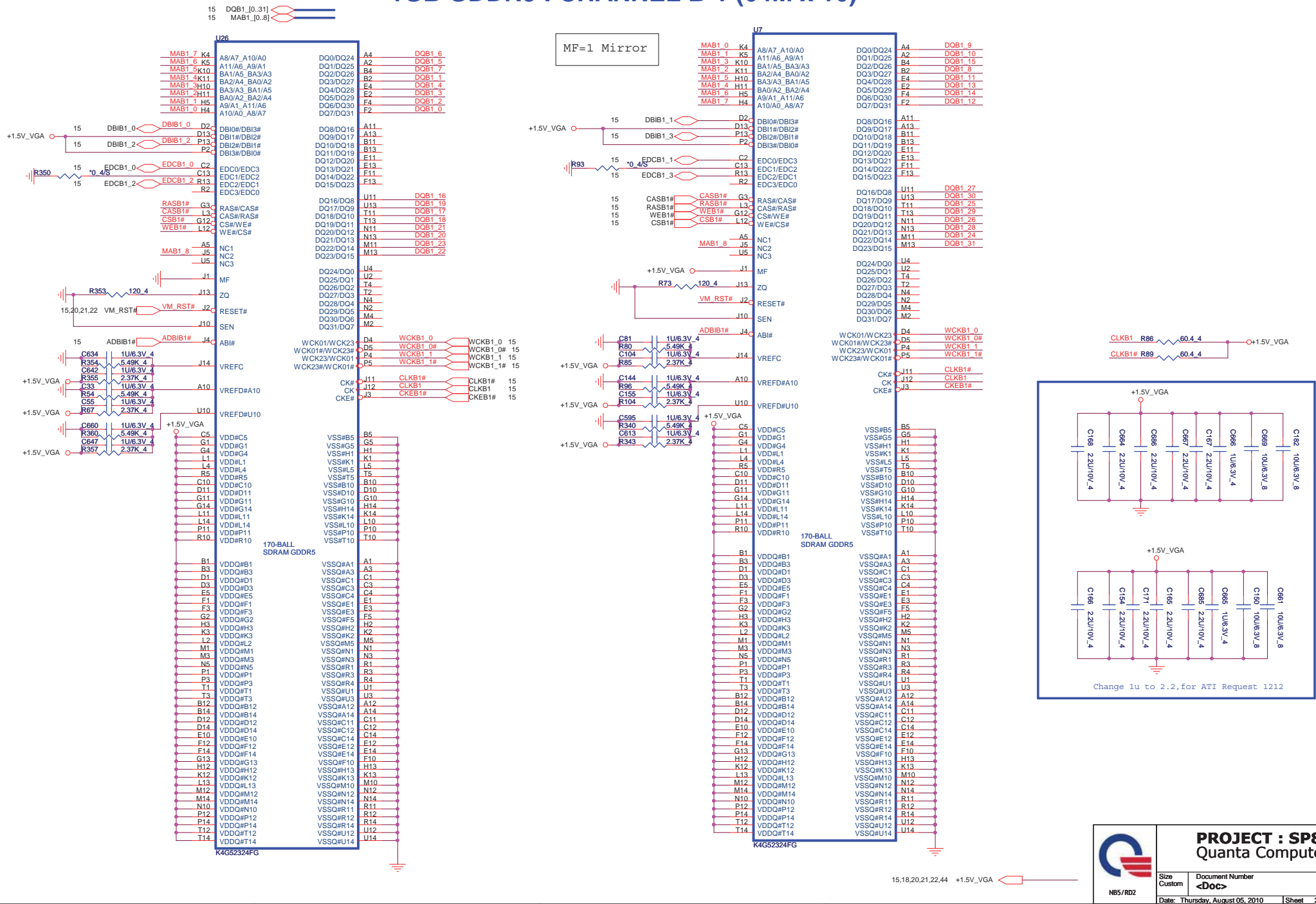
1GB GDDR5 : CHANNEL A-1 (64M x 16)

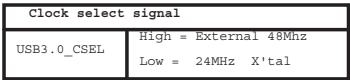



1GB GDDR5 : CHANNEL B-0 (64M x 16)

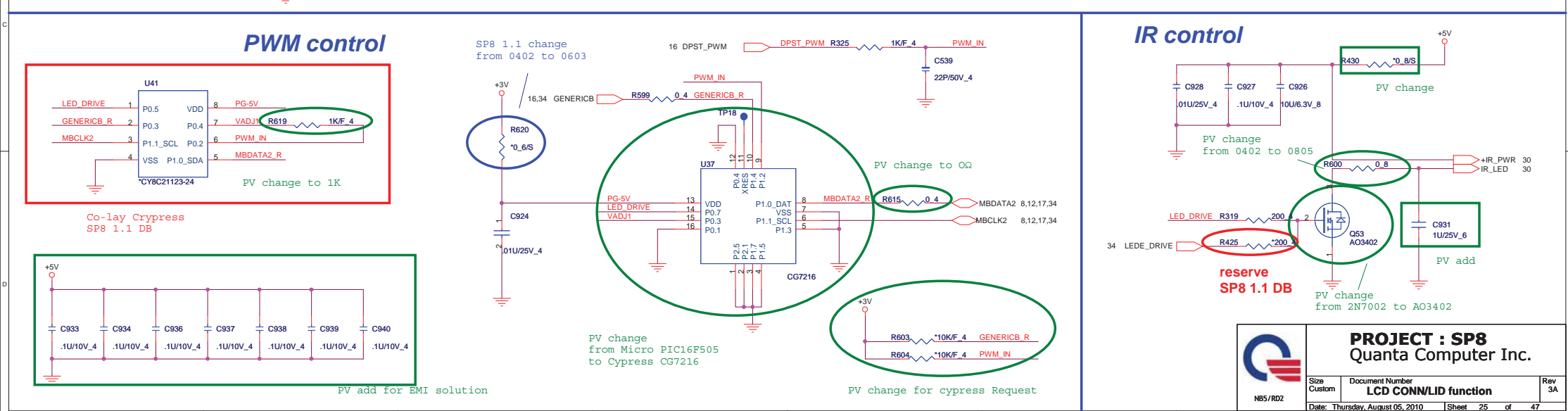


1GB GDDR5 : CHANNEL B-1 (64M x 16)

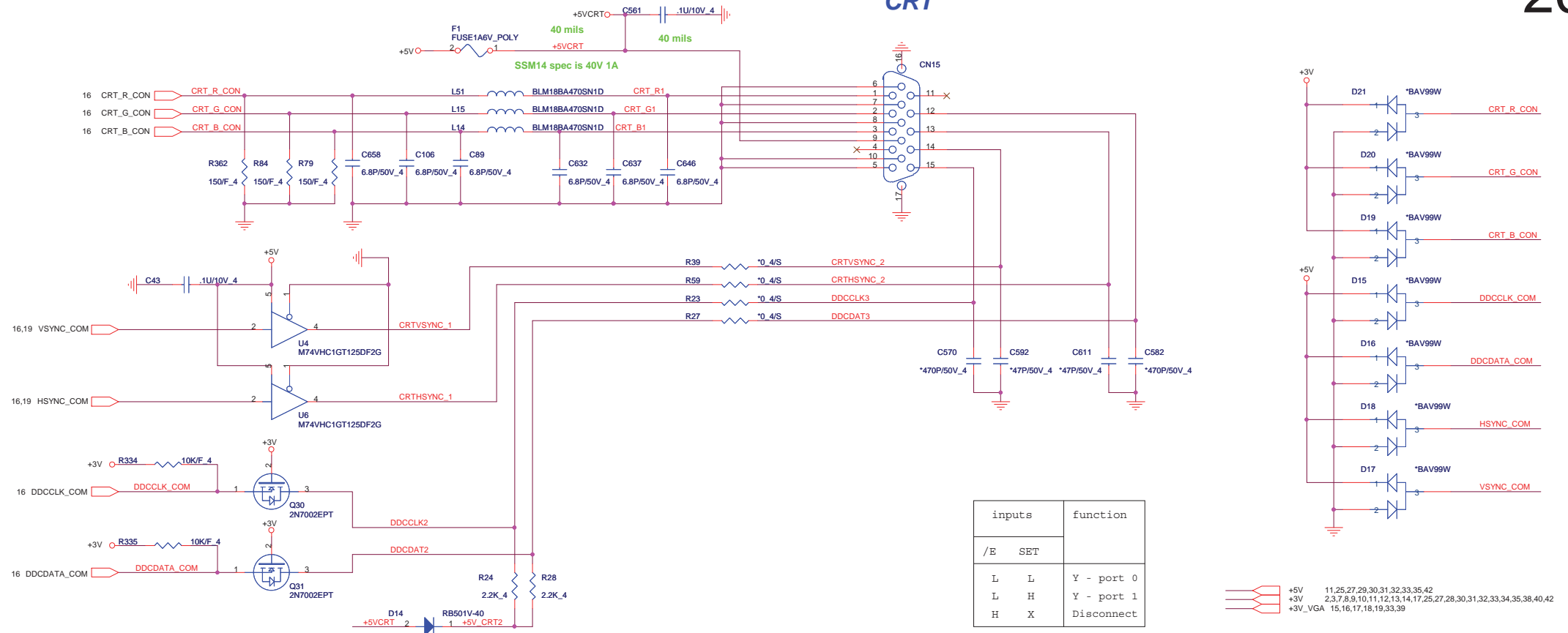




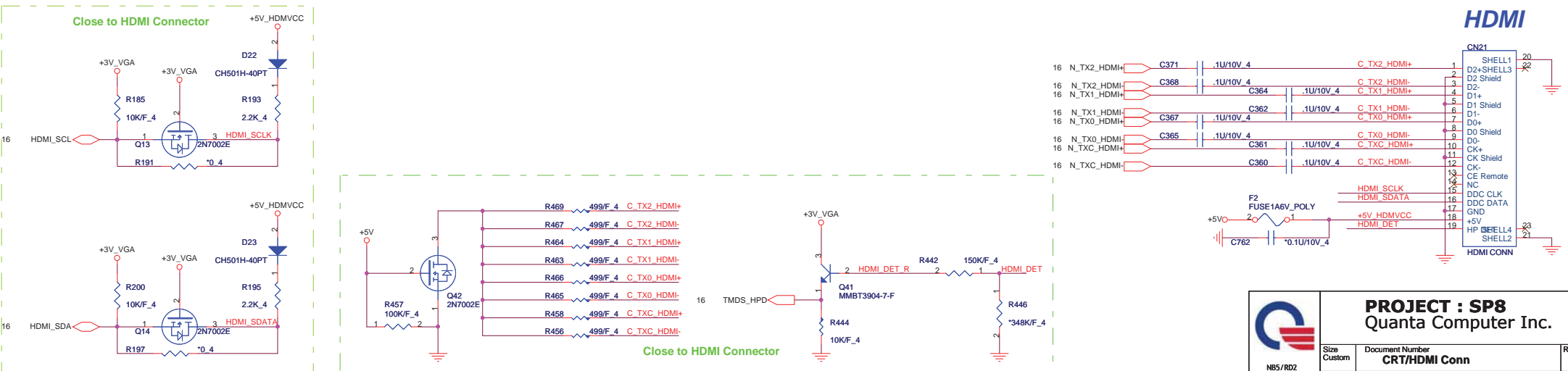
 NBS/RDZ	PROJECT : SP8 Quanta Computer Inc.		
	Size Custom	Document Number USB3.0	Rev 3A
	Date: Thursday, August 05, 2010	Sheet 24 of 47	

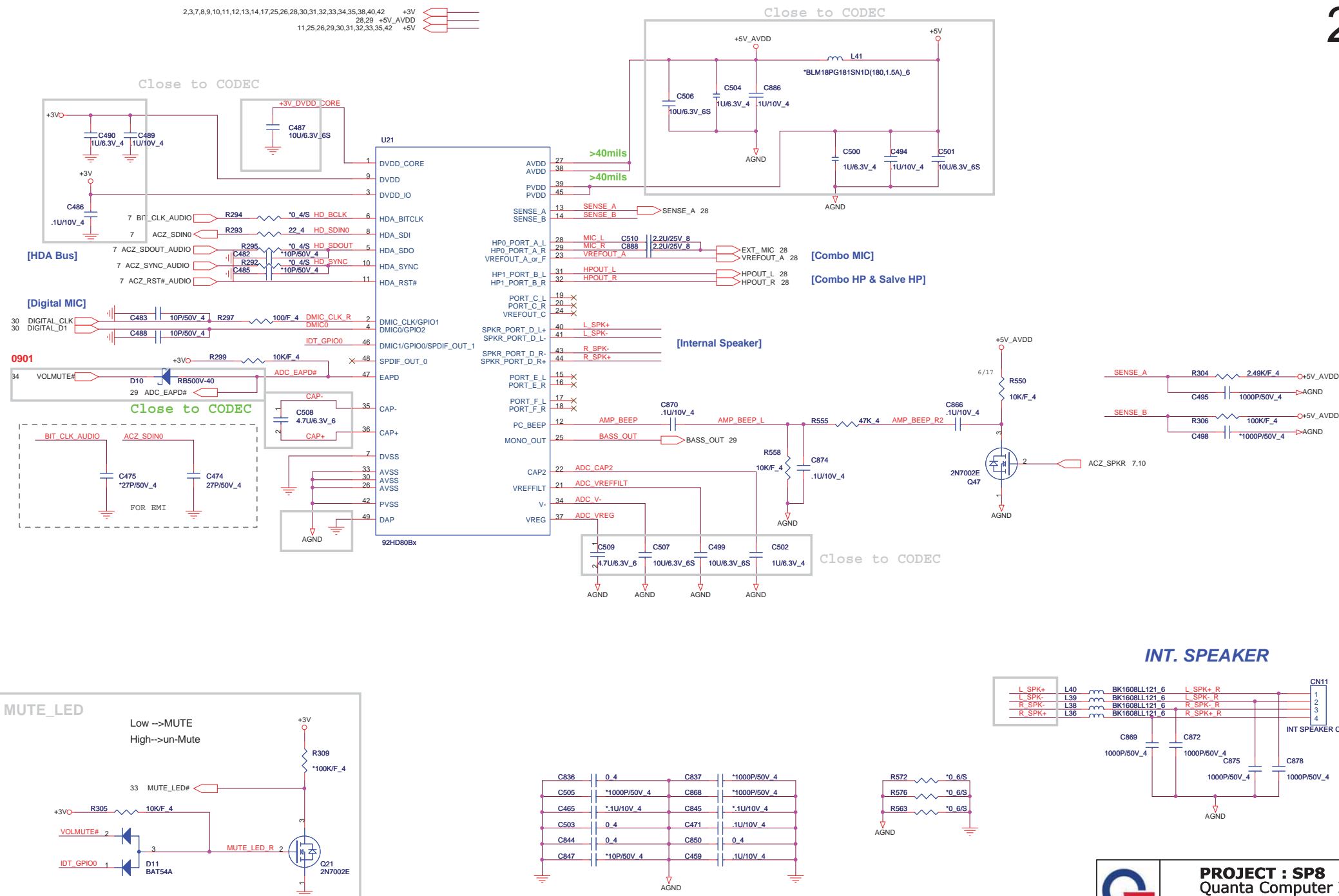


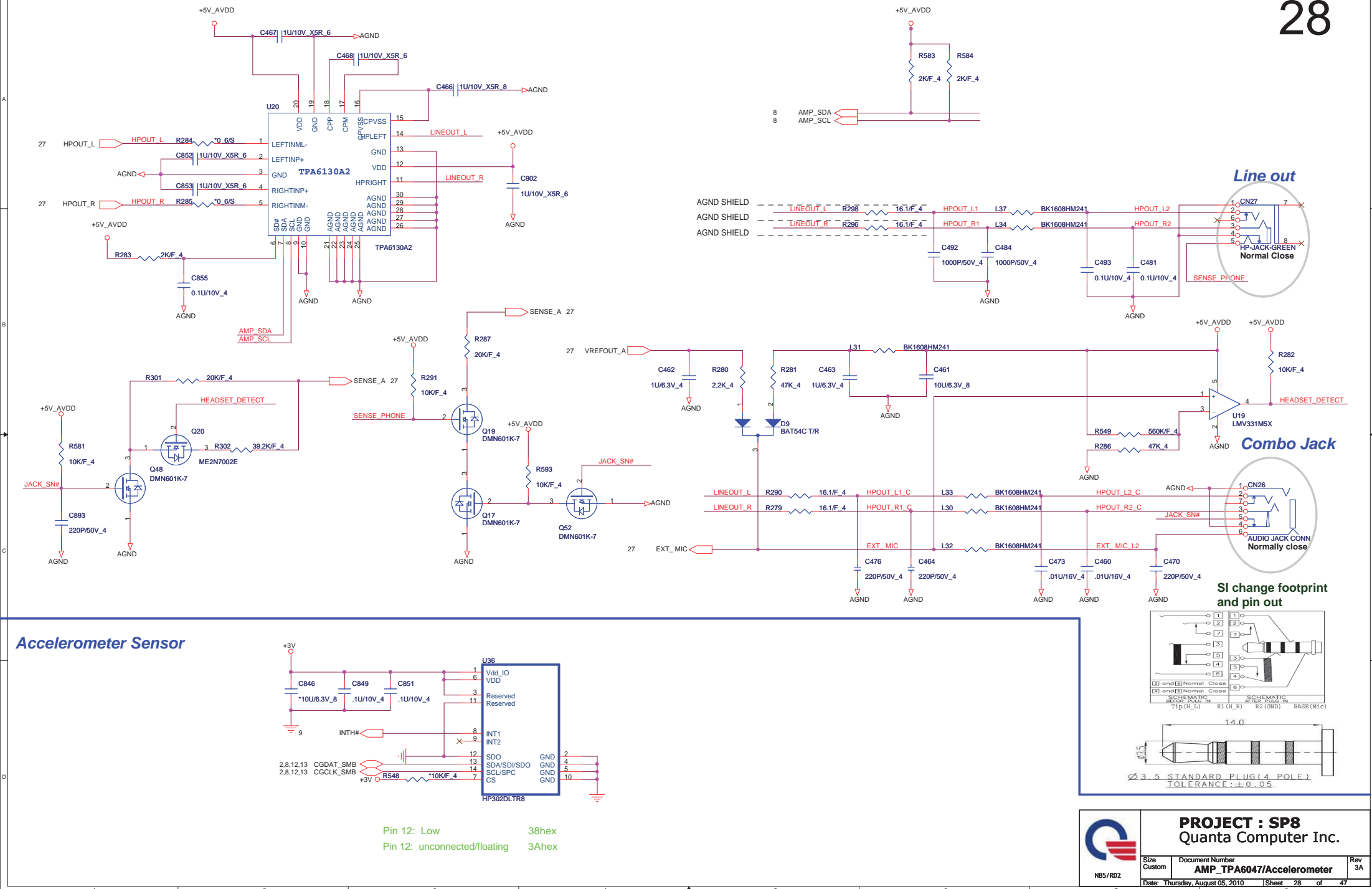
CRT



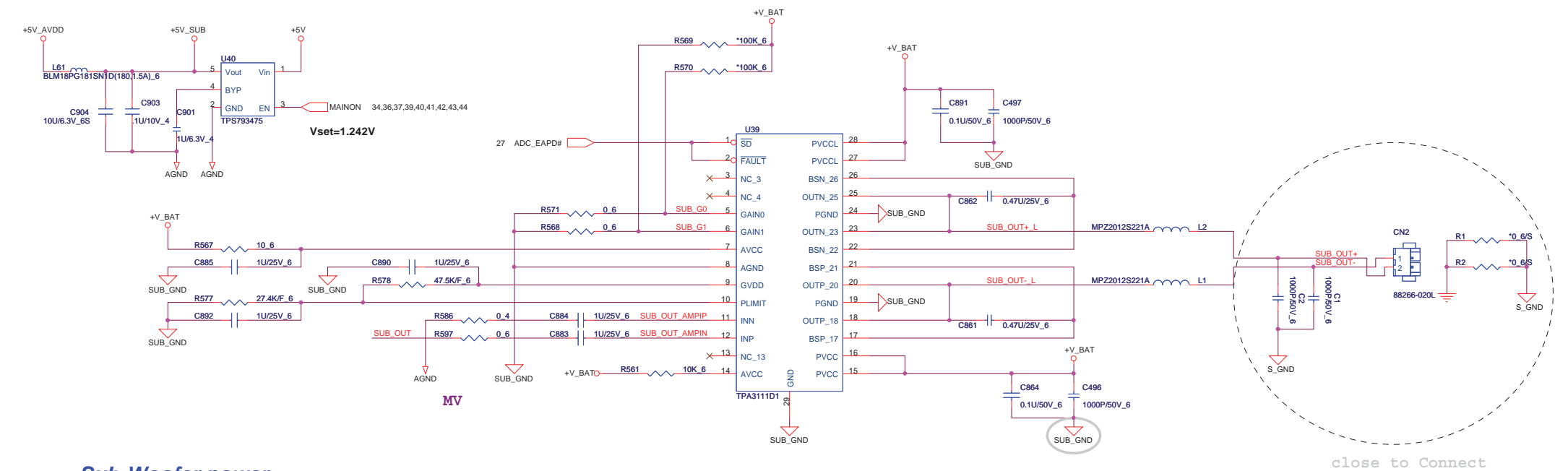
HDMI



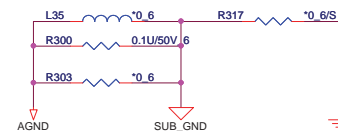
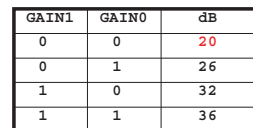





29

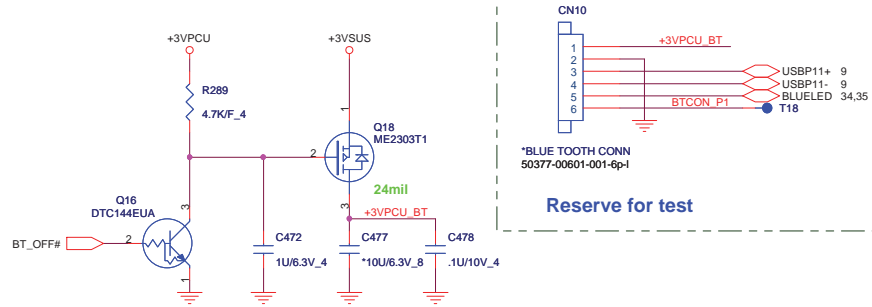


close to Connect

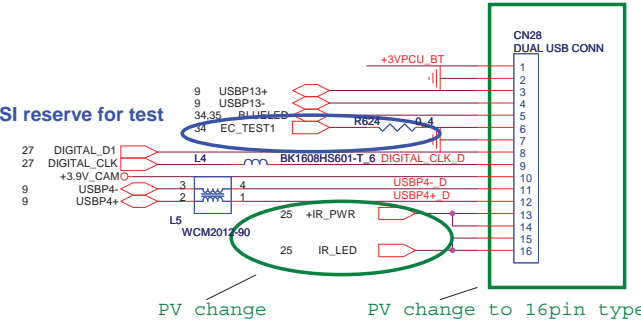


 NBS/RDZ	PROJECT : SP8 Quanta Computer Inc.		
	Size Custom	Document Number SUBWOOFER (EQ & AMP.)	Rev 3A
Date: Thursday, August 05, 2010		Sheet 29 of 47	

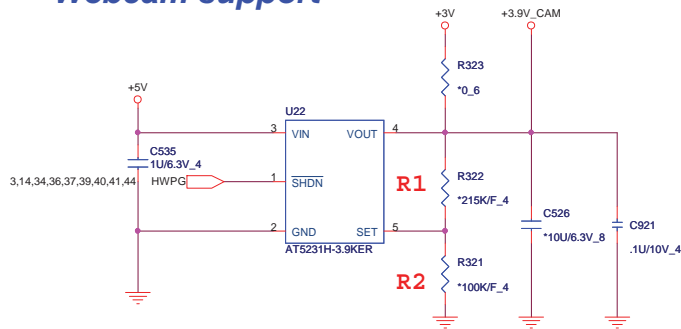
Bluetooth



SP8 1.1 SI reserve for test

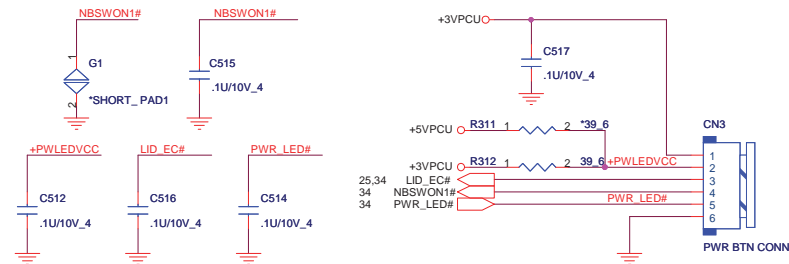


Webcam support



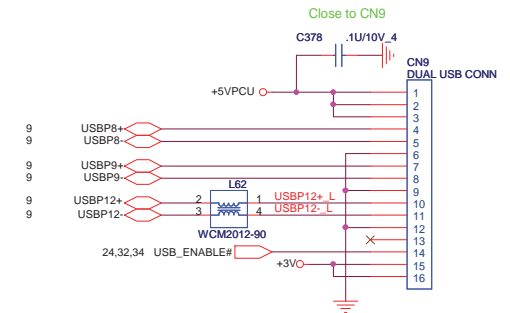
$$V_{out} = 1.25 (1 + R1/R2)$$

Power Button

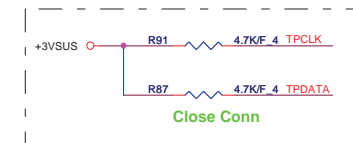
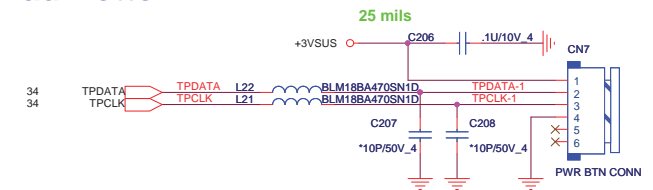



1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

Ext USB & Card Reader

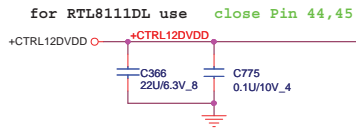


Touch Pad Button

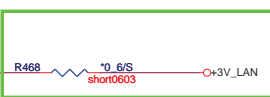


 NBS/RD2	PROJECT : SP8 Quanta Computer Inc.	
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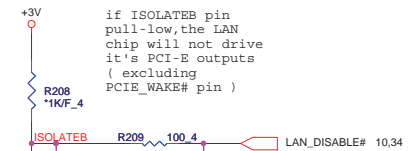
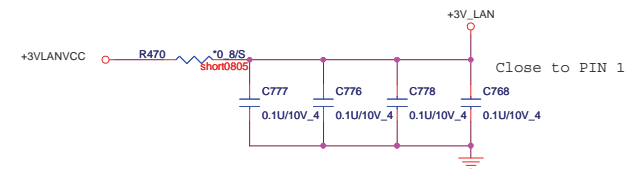
T : Stuffed for RTL8111DL(10/100/1000)



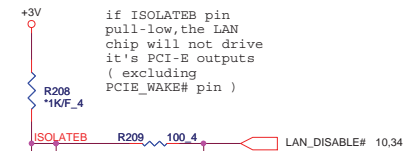
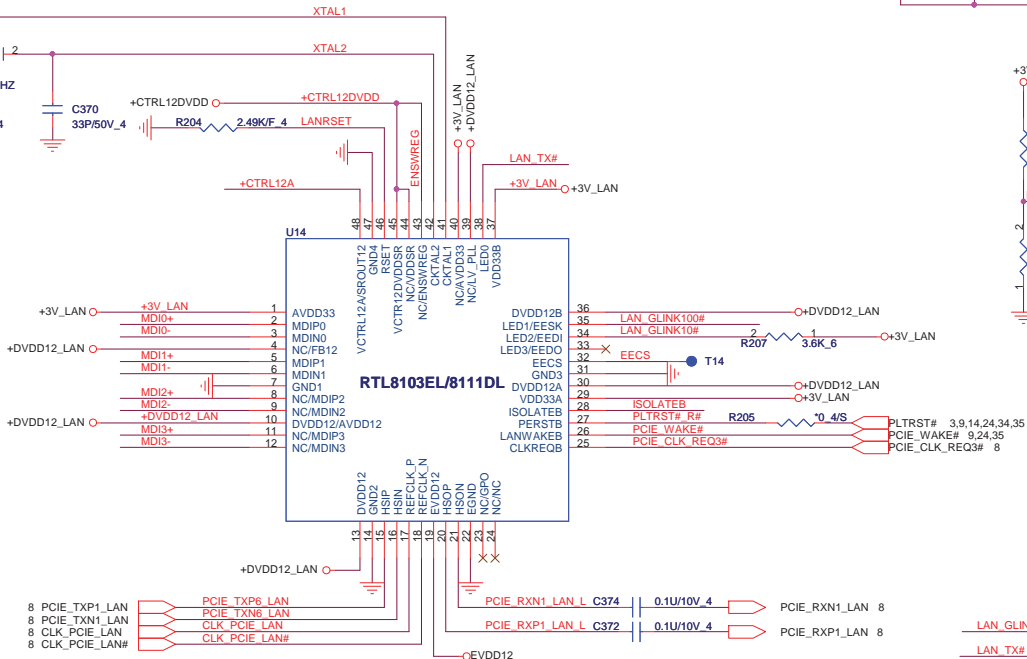
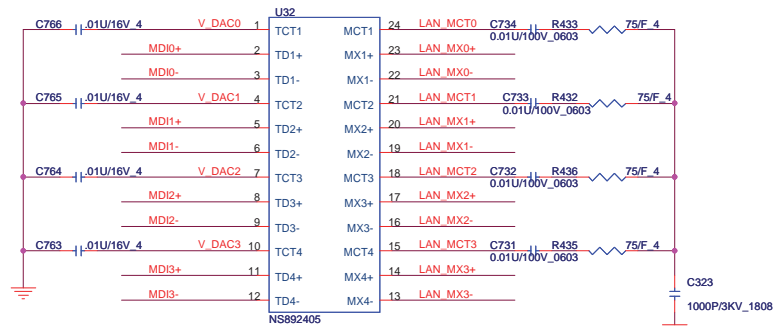
for RTL8111DL use



Remove R3571,R3573
R3571 and R3573 are used in RTL8111DL, remove R3573 if switching regulator is enable, Remove R3571 external power is used.

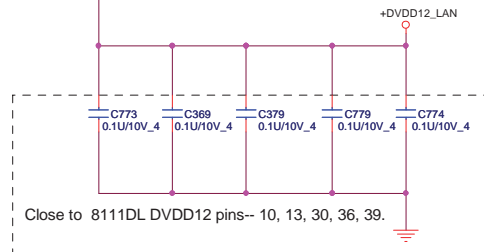
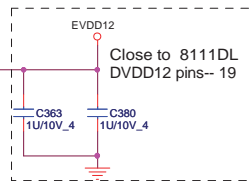
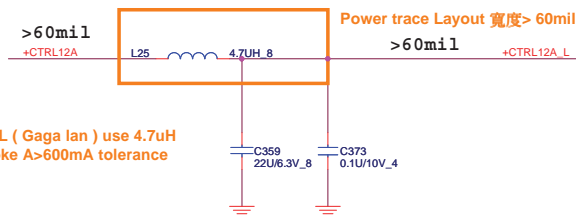


AL08111DB00 RTL8111DL-GR

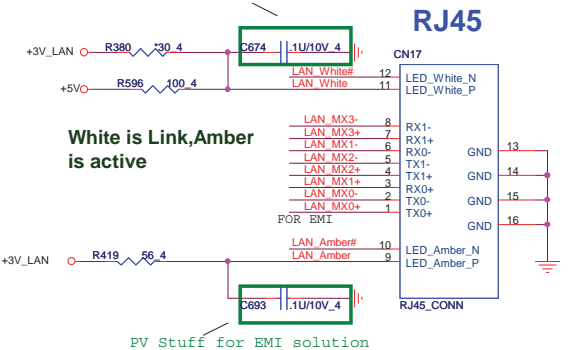


NS892402:GIGABIT DB0AT9LAN05

L23
RTL8111DL (Gaga lan) use 4.7uH
power choke A>600mA tolerance
±15%



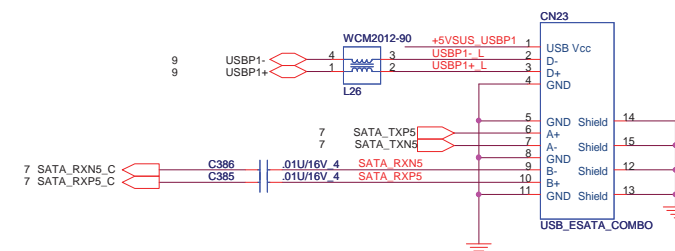
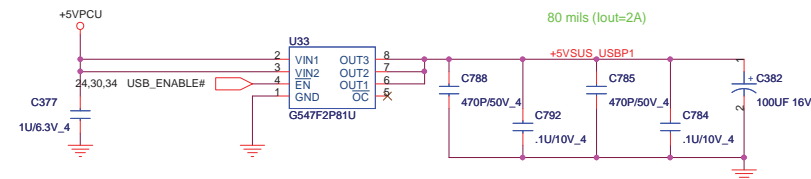
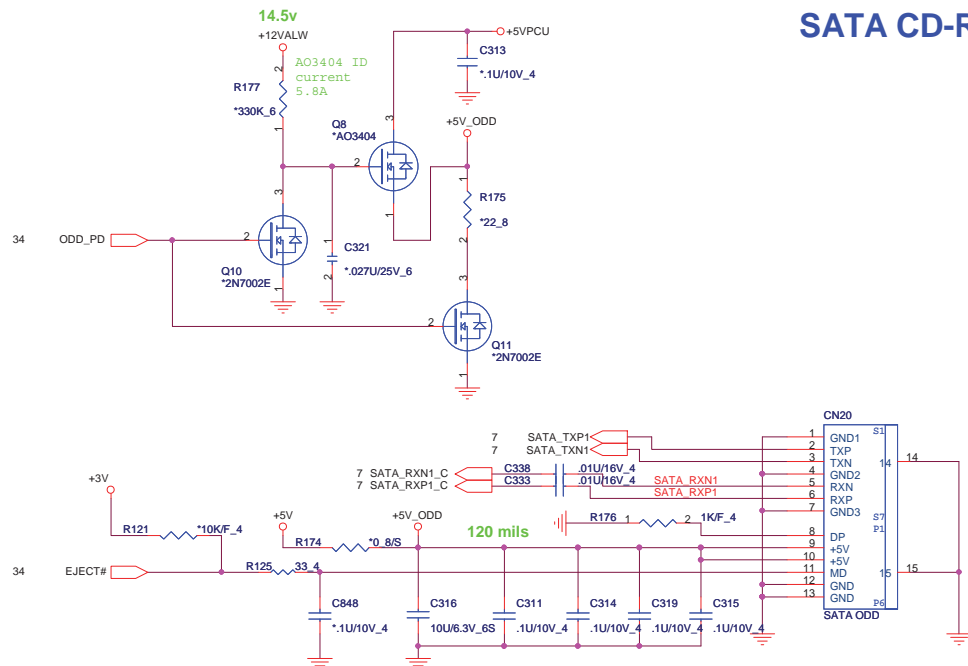
PV Stuff for EMI solution



PV Stuff for EMI solution

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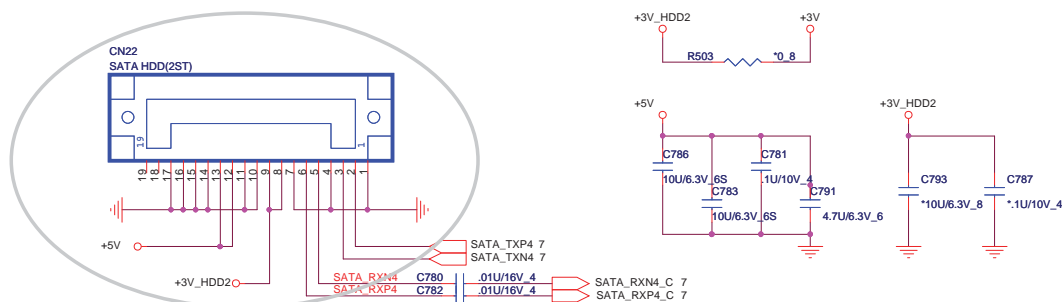
E-SATA



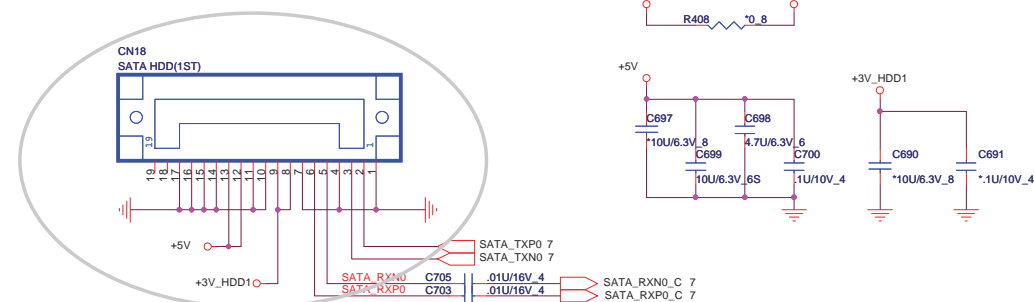
SATA HDD #1

SATA HDD #2

SI change pin define and footprint (the same AX)



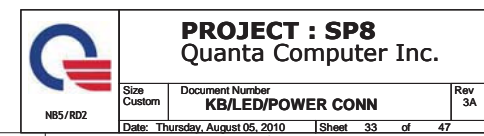
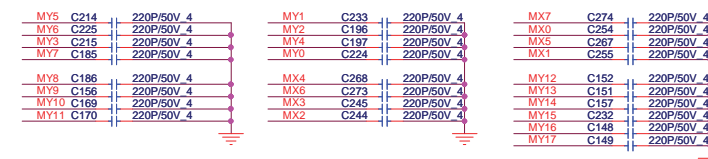
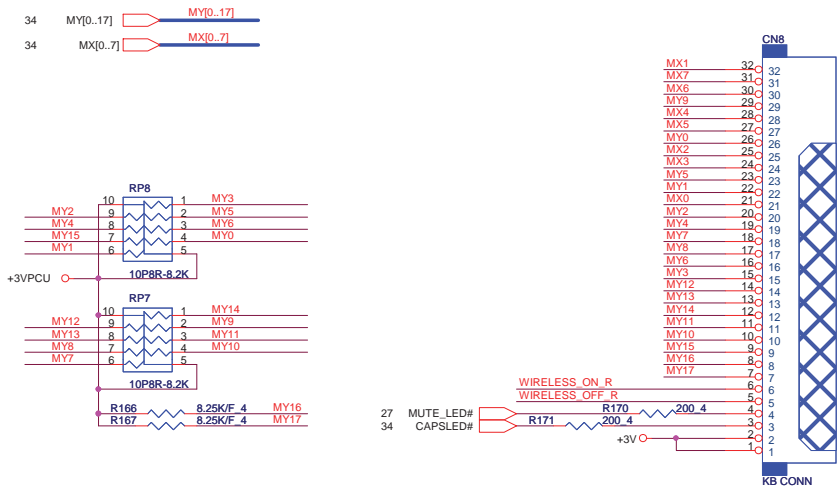
SI change pin define and footprint (the same AX)

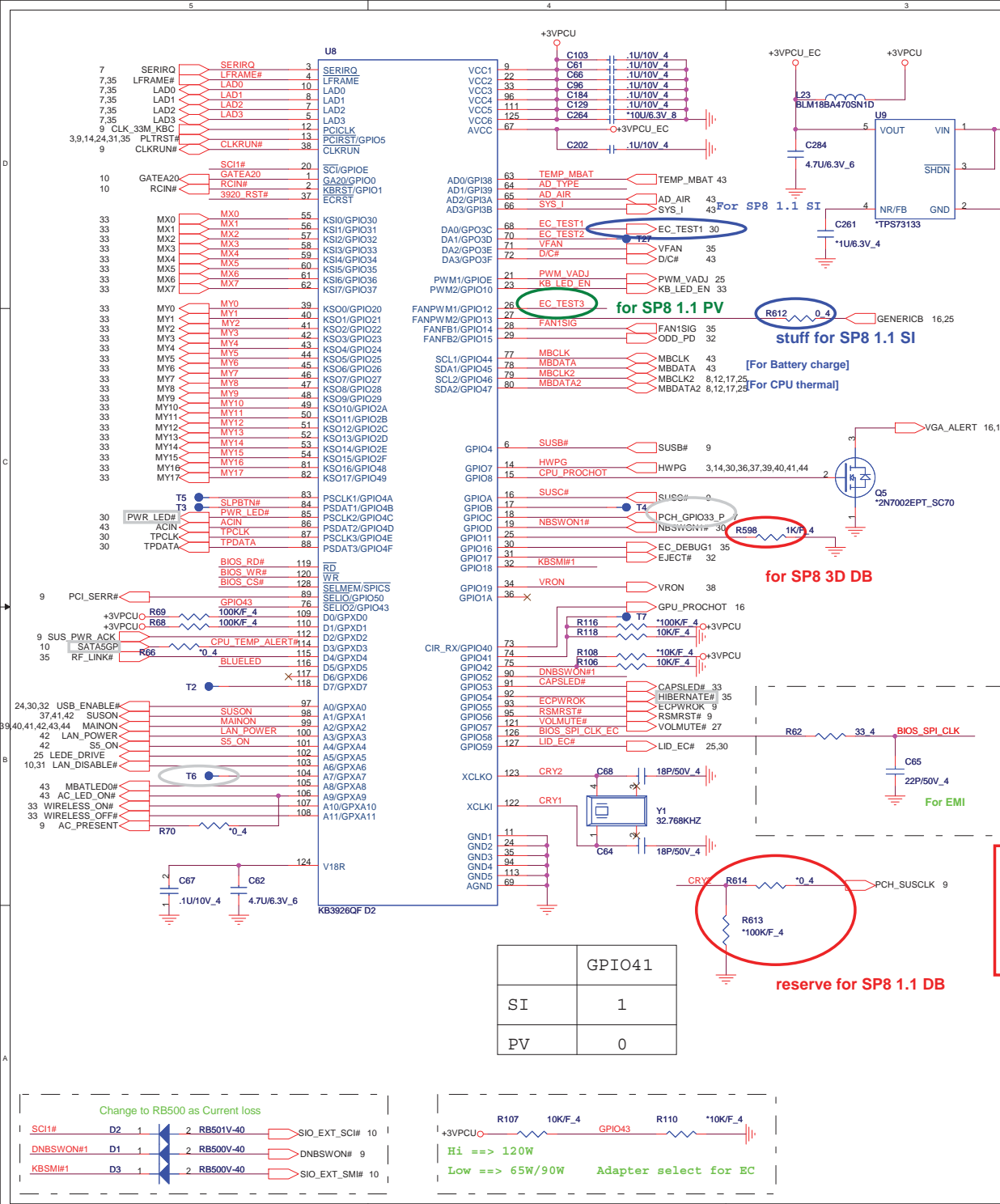


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Quanta Computer Inc.

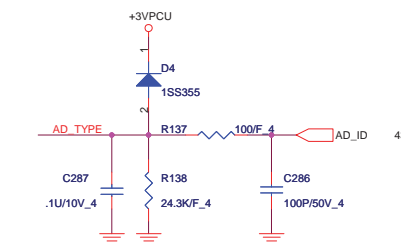
Size Custom	Document Number ODD/HDD/ONFI	Rev 3A
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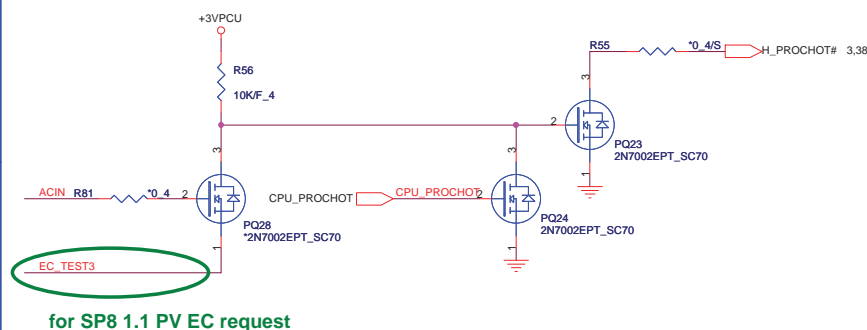




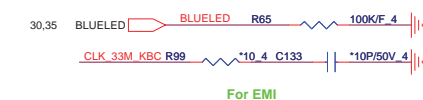
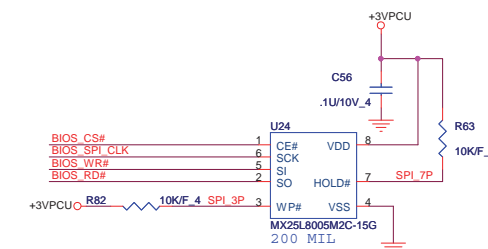
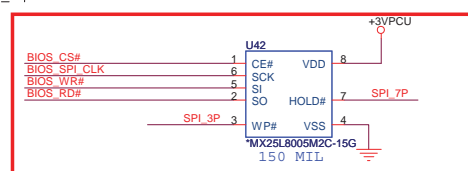
Adapter Type



R273
64.9K -->65W CS36492FB17
33.2K -->90W CS33322FB13
Change to 1SS355 as Current loss



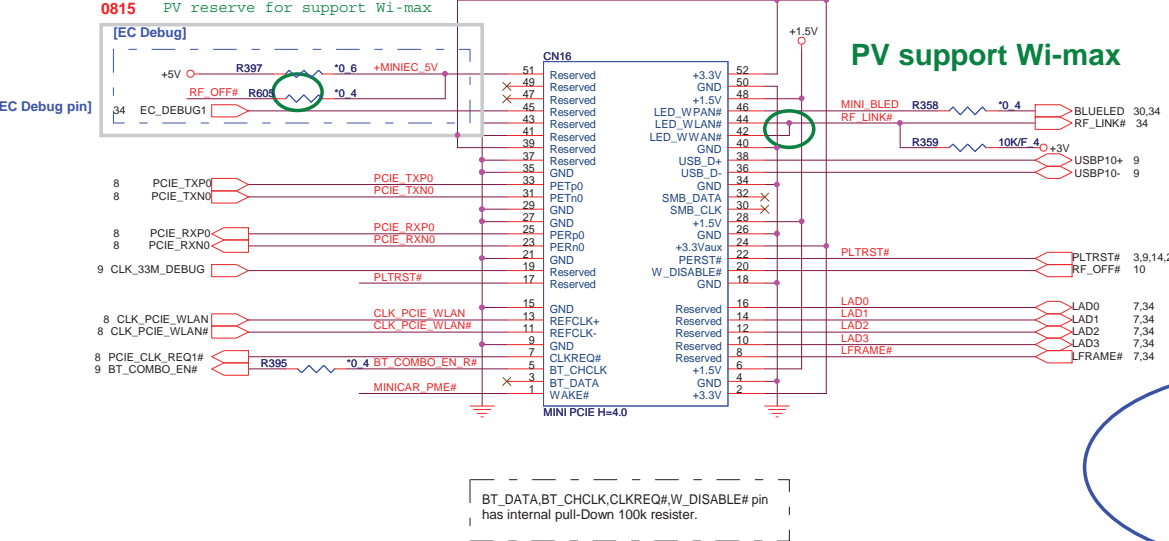
CO-LAYOUT SP8 1.1 DB



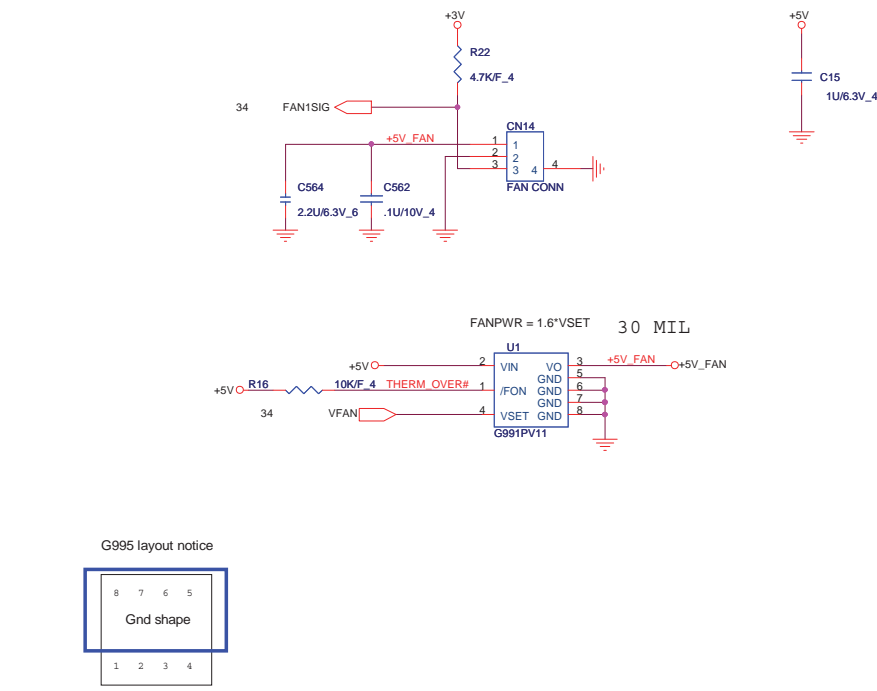
PROJECT : SP8
Quanta Computer Inc.

Size Custom	Document Number KB3926/ROM/TP	Rev 3A
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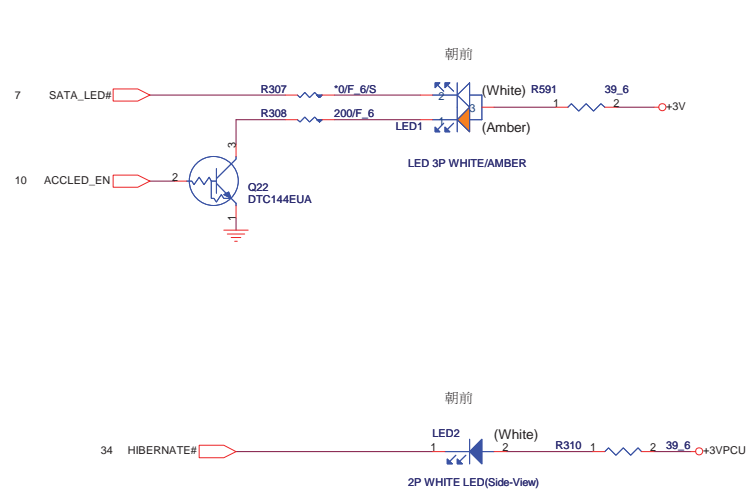
Mini PCI-E Card 1 WLAN



CPU FAN



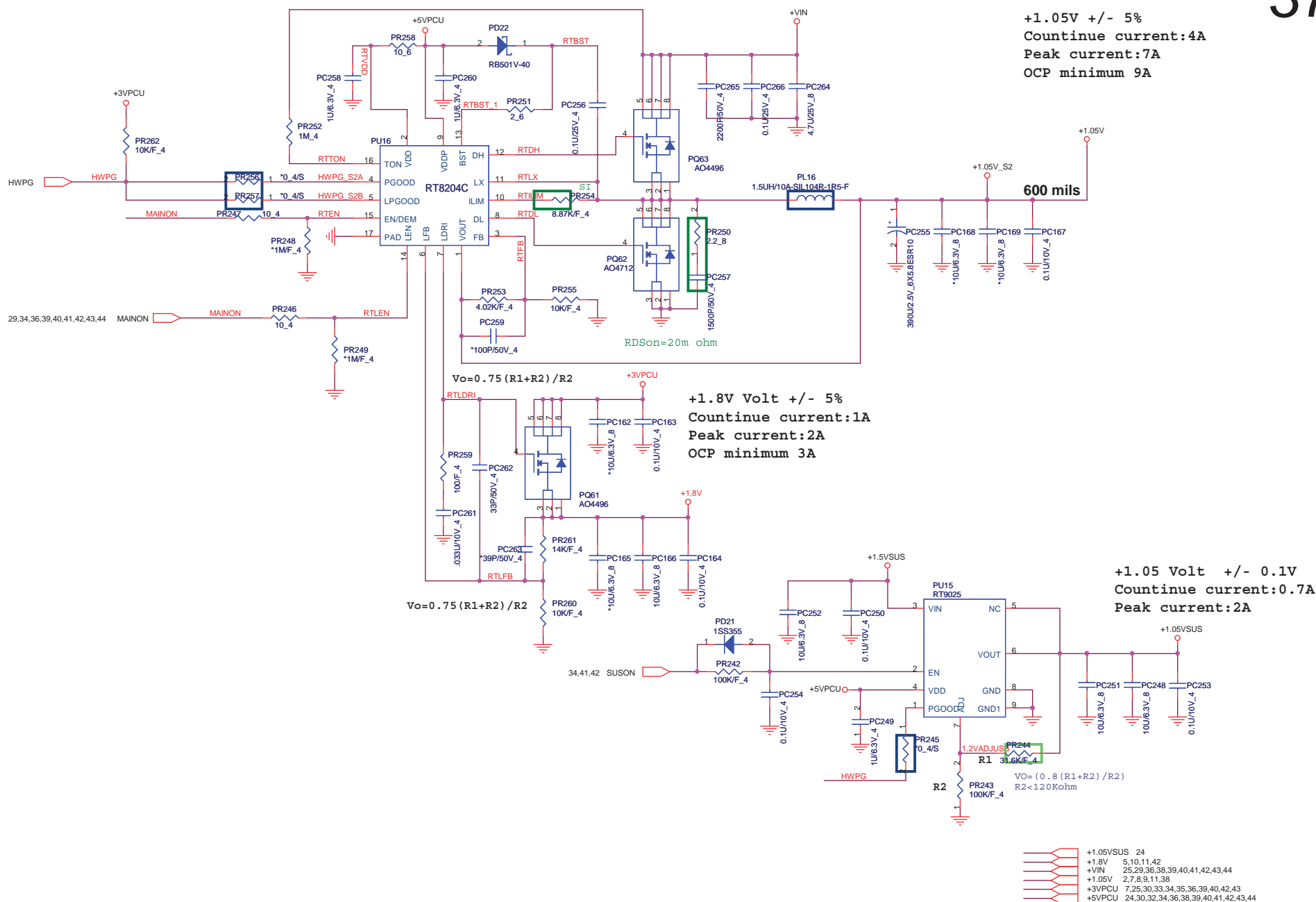
LED



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	Quanta Computer Inc.		
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4.7U25V
+3.3V +/- 5%
Continue current:5A
Peak current:6A
OCP minimum 7.5A

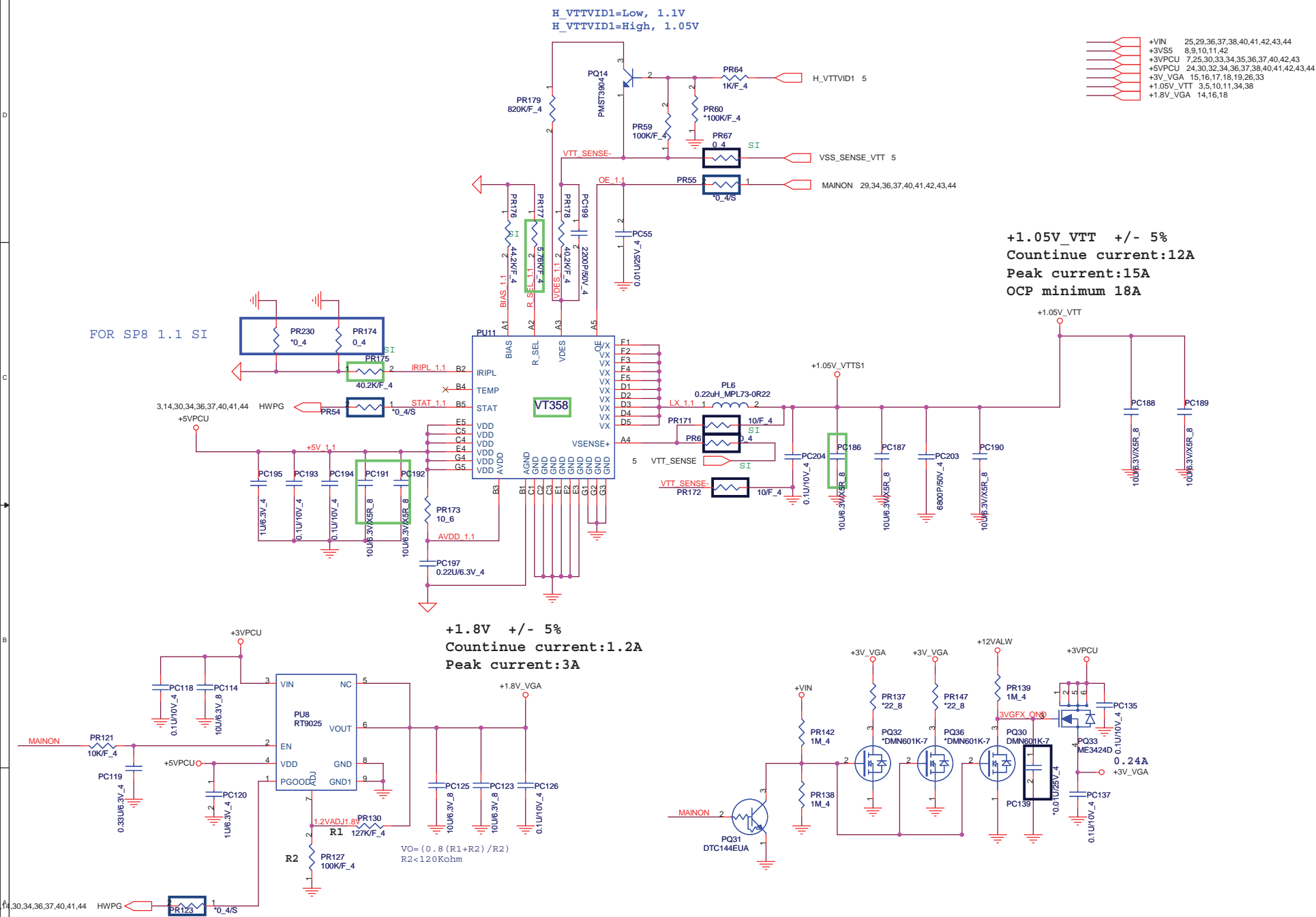




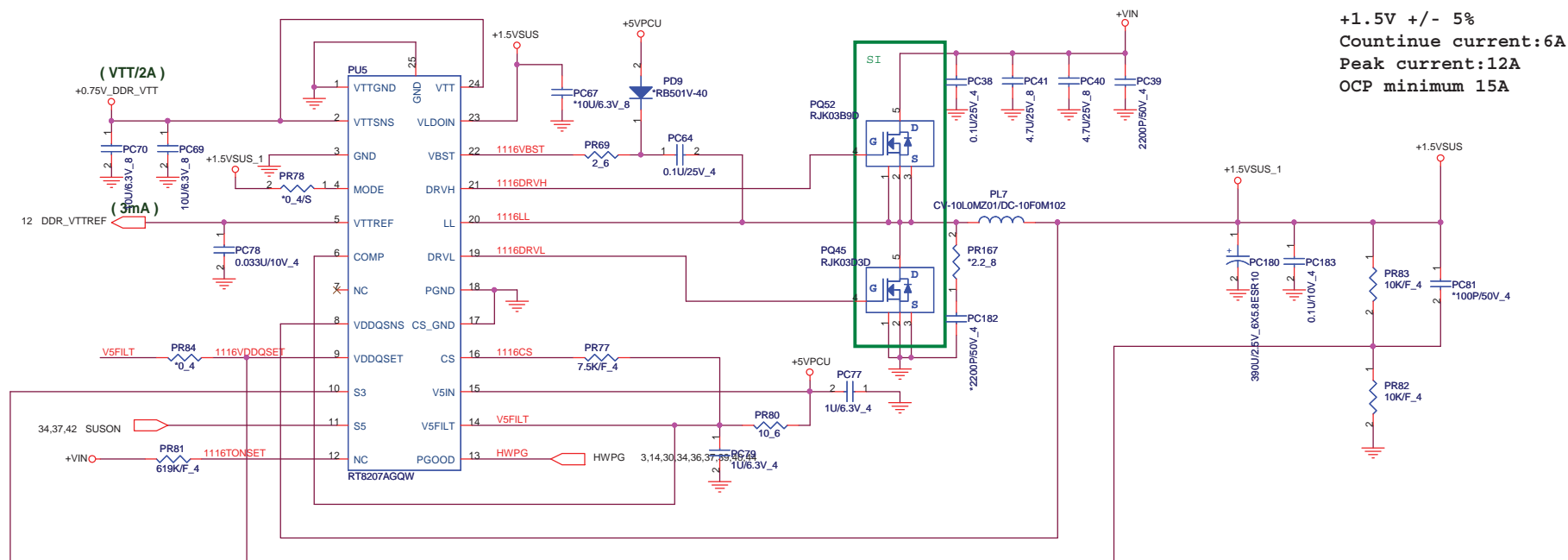


Size Custom	Document Number CPU Core (ADP3212)	Rev 3
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+3V	2,3,7,8,9,10,11,12,13,14,17,25,26,27,28,30,31,32,33,34,35,40,42
+VIN	25,29,36,37,39,40,41,42,43,44
+1.05V	2,7,8,9,11,37
+5VPCU	24,30,32,34,36,37,39,40,41,42,43,44
+VCOE 5	
+1.05V VTT	35,36,39,40

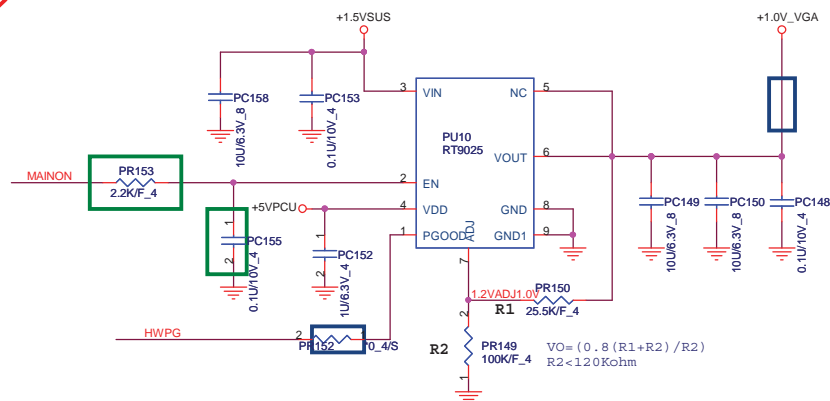






need to stuff for S3 and PR263 change to 100K

+1.0V +/- 5%
Countinue current:1.7A
Peak current:3A



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Quanta Computer Inc.

Size Custom	Document Number DDR3 (RT8207)	Rev 3A
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