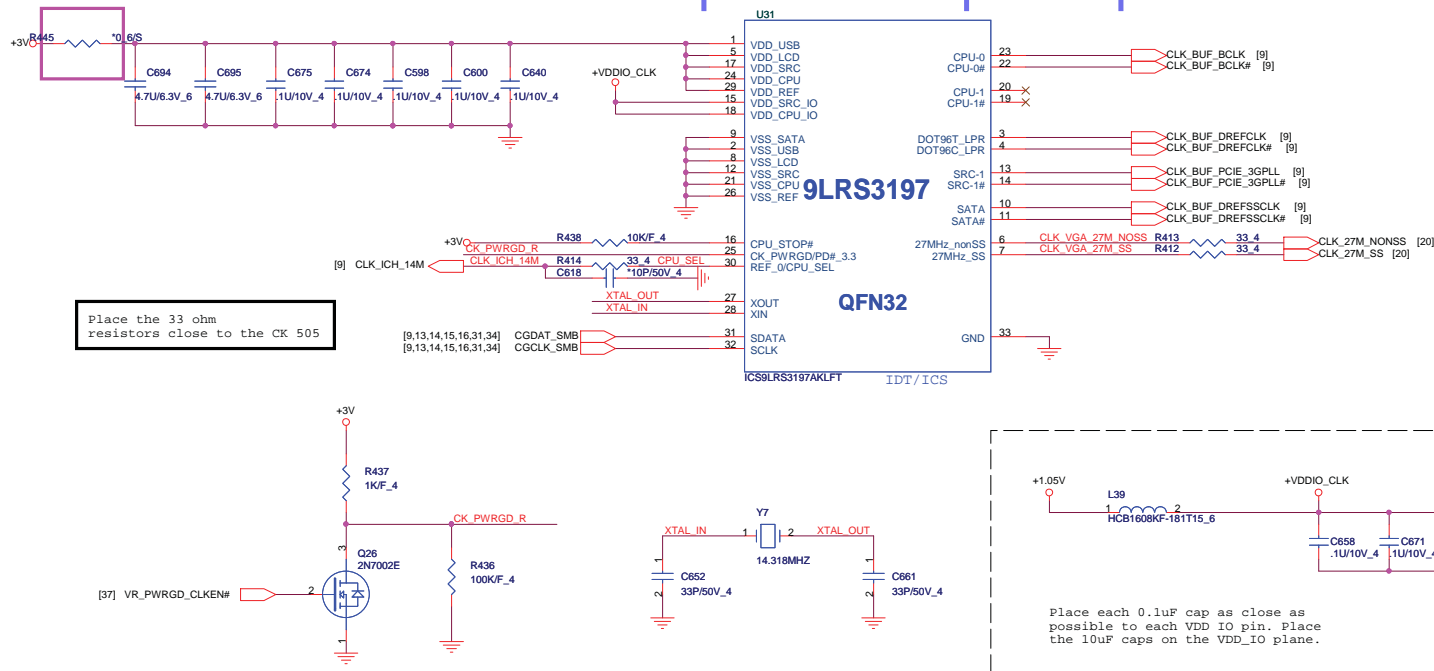




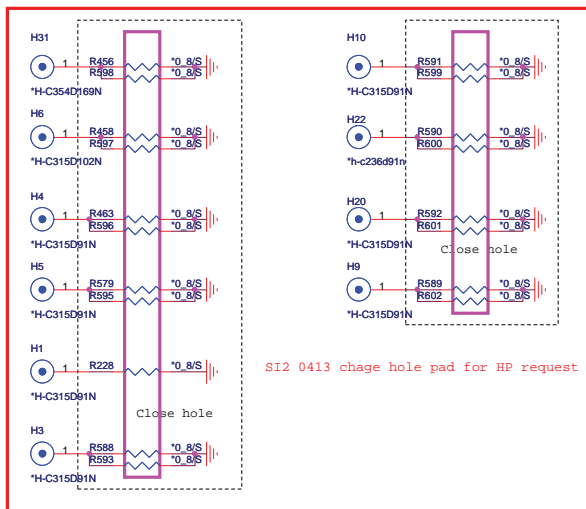
PROJECT : SP7
Quanta Computer Inc.

Size Custom	Document Number Block Diagram	Rev 1A
Date: Friday, July 10, 2009		Sheet 1 of 42

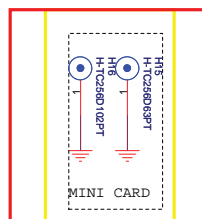


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

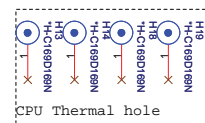
M/B Screw Hole



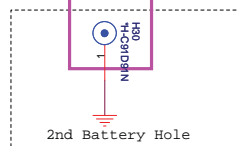
MINI CARD



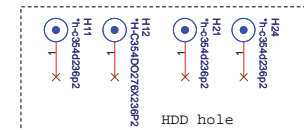
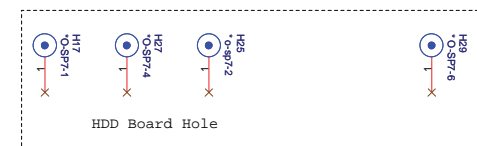
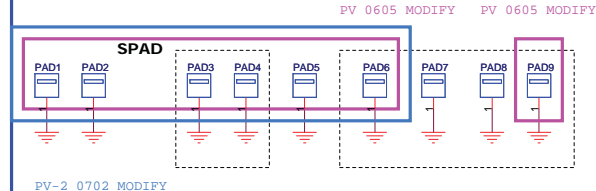
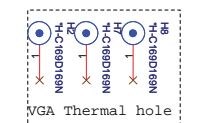
CPU Thermal hole



2nd Battery Hole

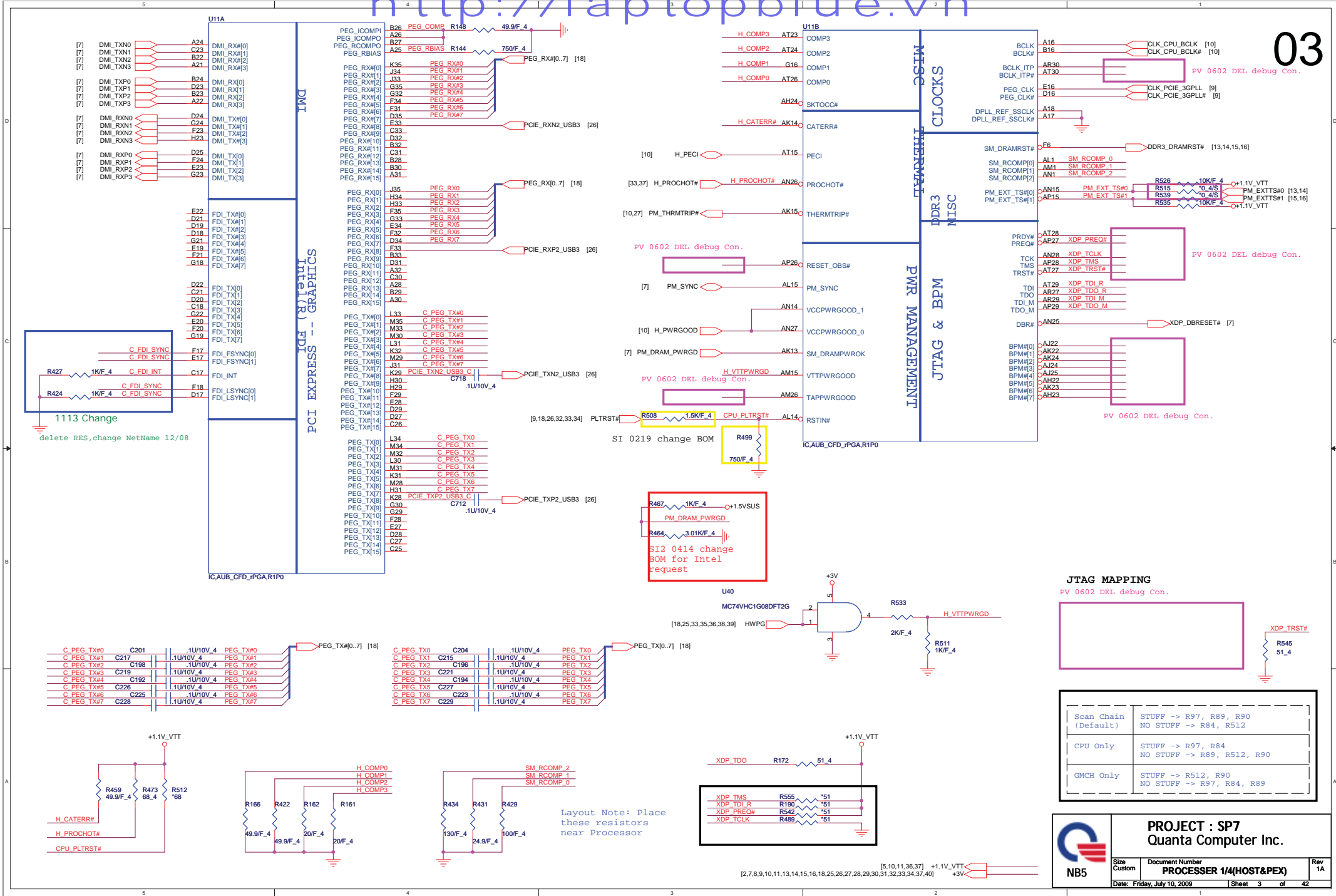


VGA Thermal hole



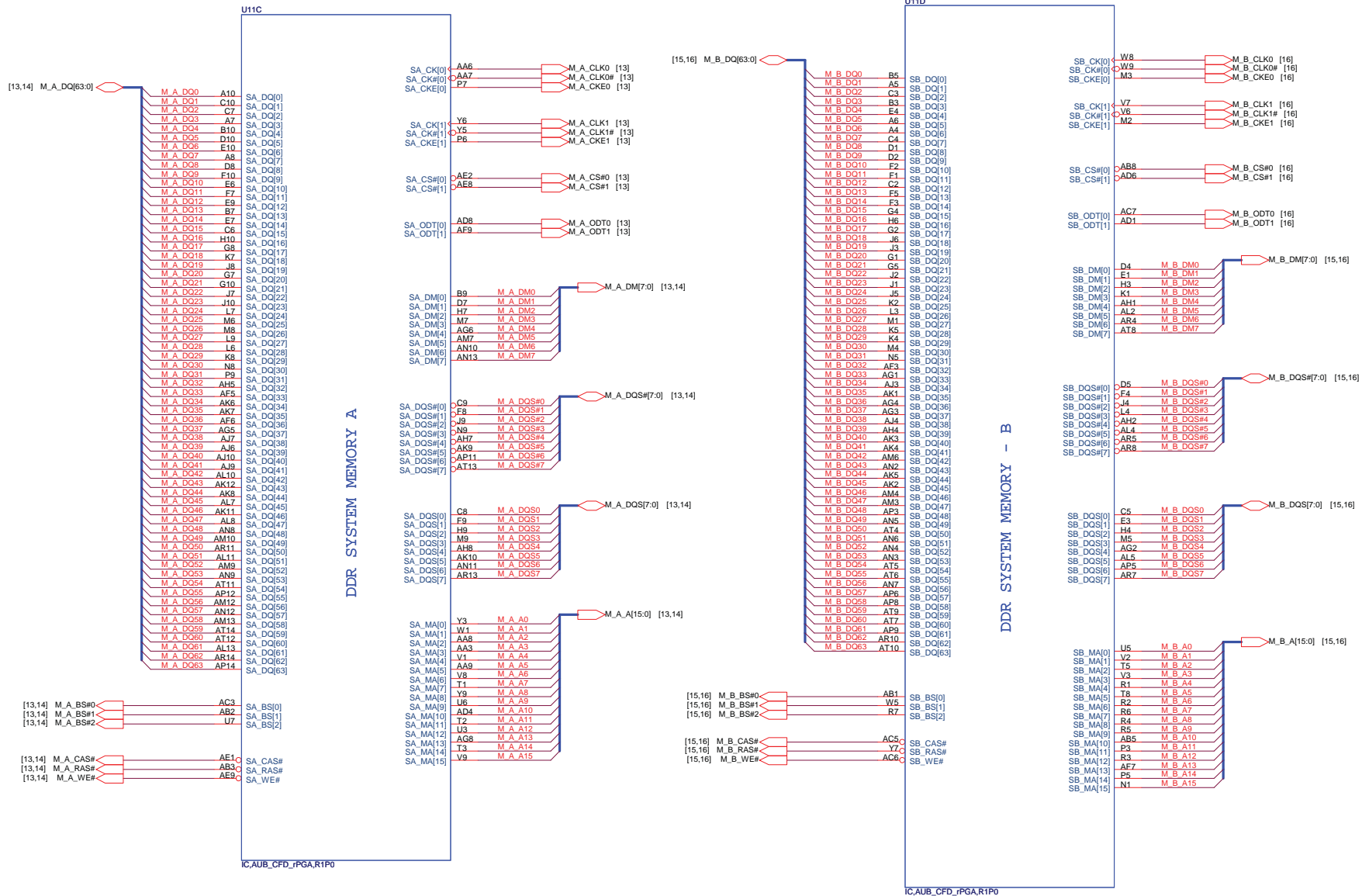
	PROJECT : SP7 Quanta Computer Inc.	
	Size Custom	Document Number CLOCK & Screw Holes
	Date: Friday, July 10, 2009	Sheet 2 of 42

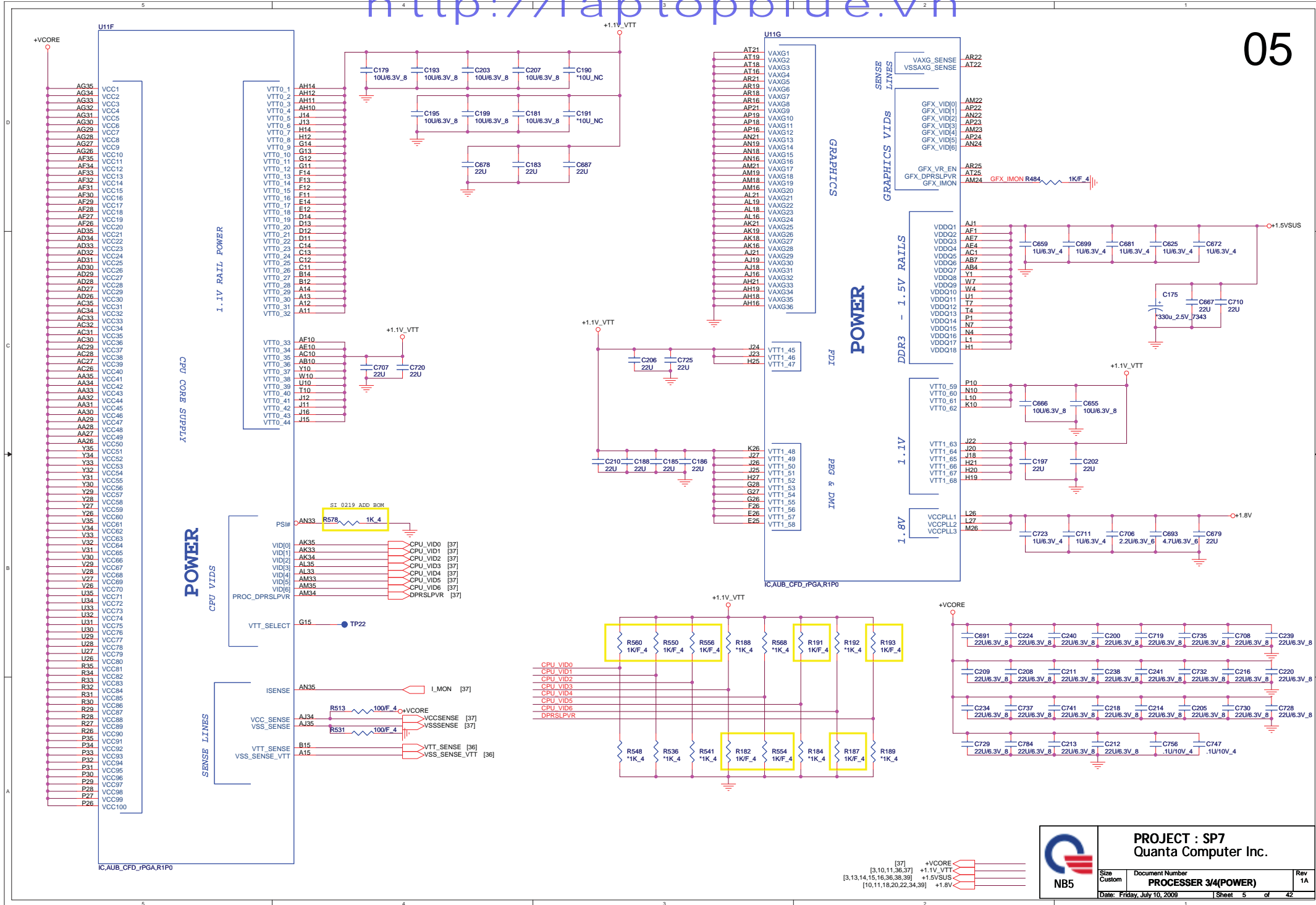
[3,7,8,9,10,11,13,14,15,16,18,25,26,27,28,29,30,31,32,33,34,37,40]
[7,8,9,11,26,27,36,37]



AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

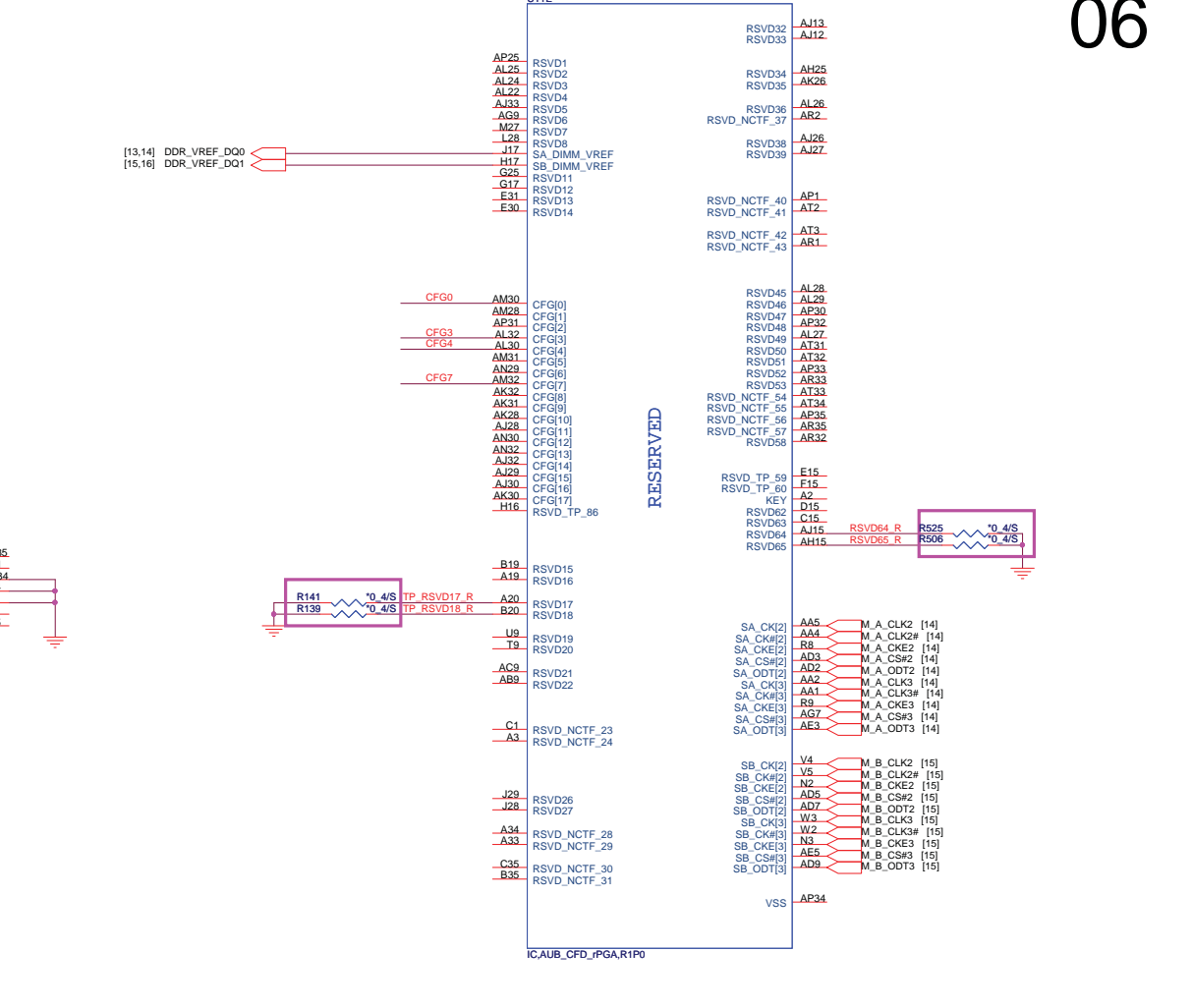
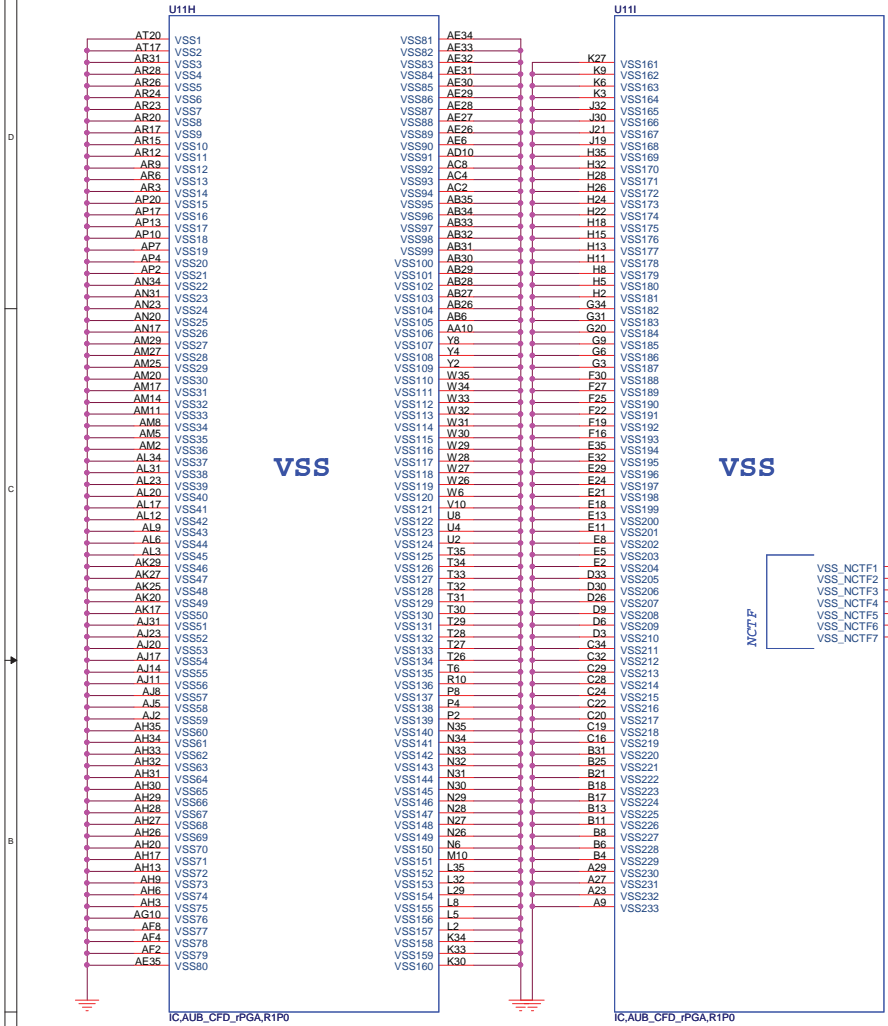
04



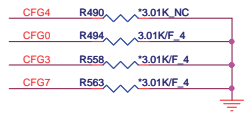


AUBURNDALE/CLARKSFIELD PROCESSOR (GND)


AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



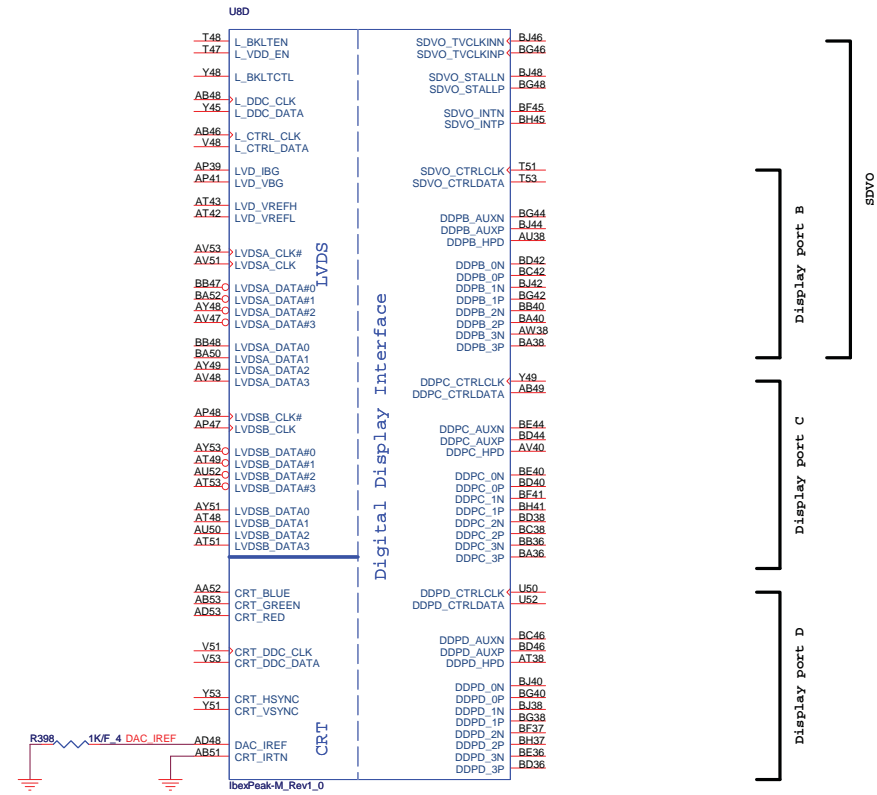
	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed



PROJECT : SP7
Quanta Computer Inc.

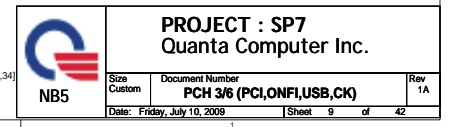
Size Custom	Document Number PROCESSOR 4/4(GND)	Rev 1A
Date: Friday, July 10, 2009	Sheet 6 of 42	

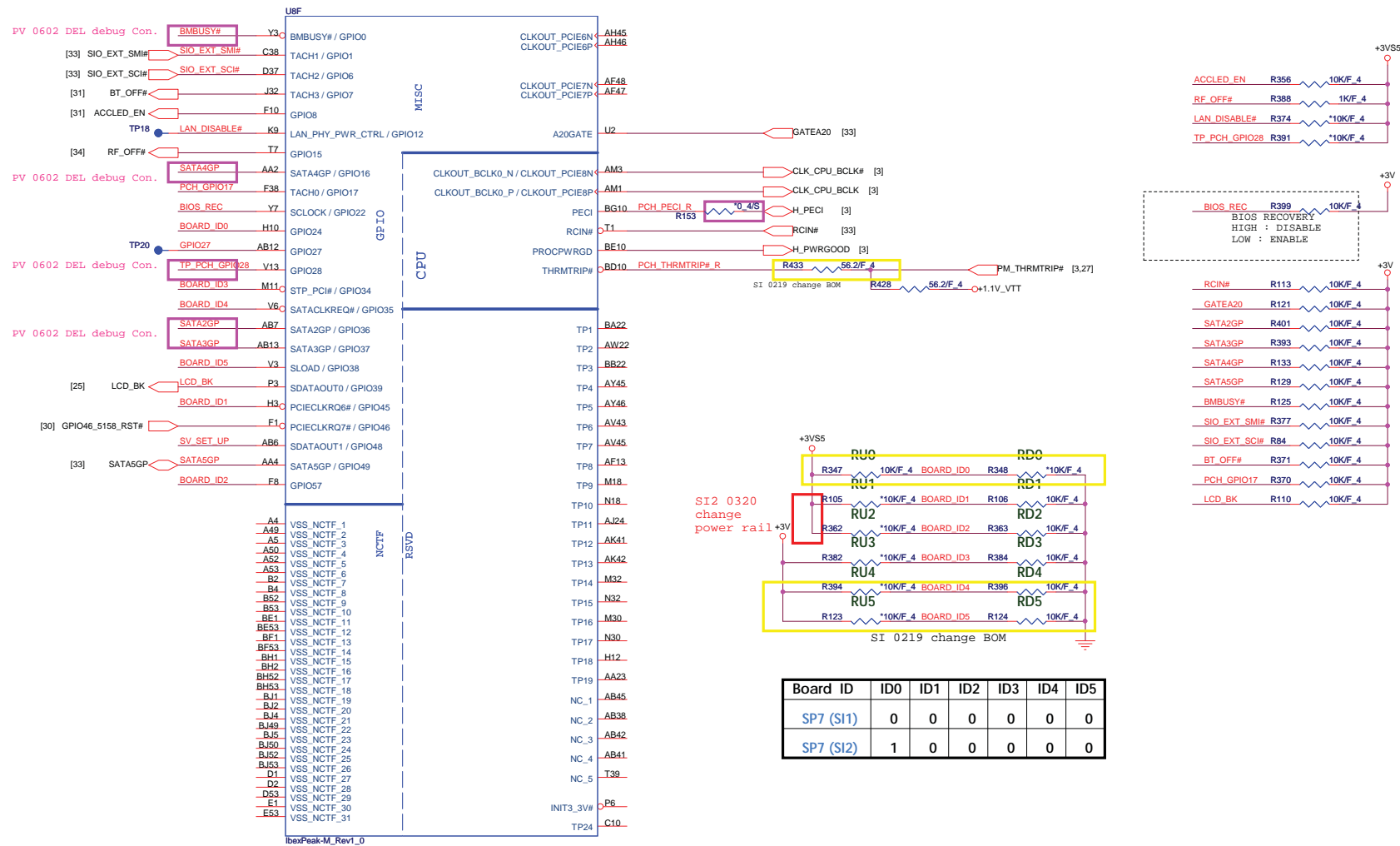
SDVO



[2,3,7,9,10,11,13,14,15,16,18,25,26,27,28,29,30,31,32,33,34,37,40] +1.05V
[2,3,7,9,10,11,13,14,15,16,18,25,26,27,28,29,30,31,32,33,34,37,40] +3V
[13,15,25,31,33,34,35,36,38,39,40,41,42] +3VPCU

IBEX PEAK-M (PCI-E, SMBUS, CLK)





Al6 swap override Strap/Top-Block Swap Override jumper

GNT3#

Low = Al6 swap override/Top-Block Swap Override enabled
High = Default

SV_SET_UP

1-X High = Strong (Default)

R364

BT_COMBO_EN# [8,34]

Boot BIOS Strap

PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

Danbury Technology Enabled

NV_ALE

High = Enable
Low = Disable

DMI Termination Voltage

NV_CLE

Set to Vcc when LOW
Set to Vcc/2 when HIGH

No Reboot Strap

R128

ACZ_SPKR [8,28,29]

PROJECT : SP7

Quanta Computer Inc.

Size Custom

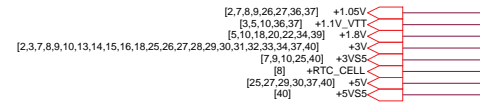
Document Number

PCH 4/6 (GPIO & Strap)

Date: Friday, July 10, 2009

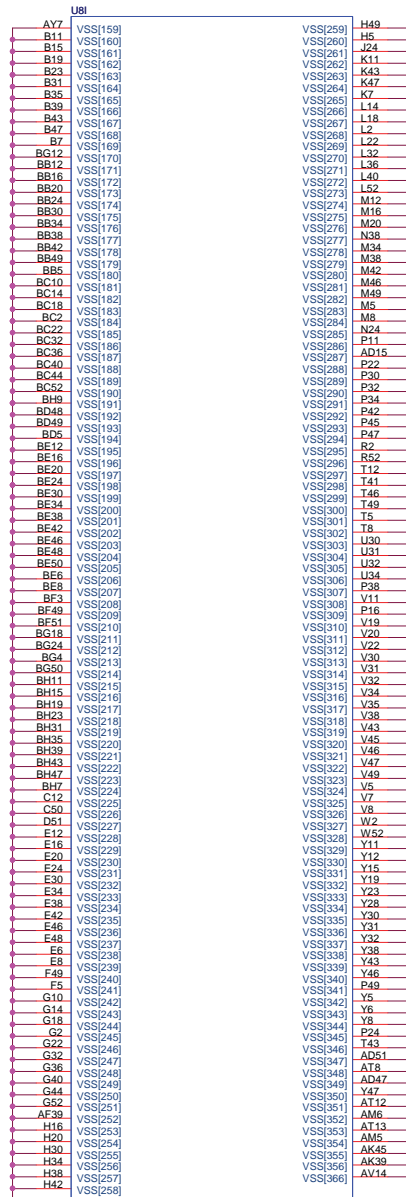
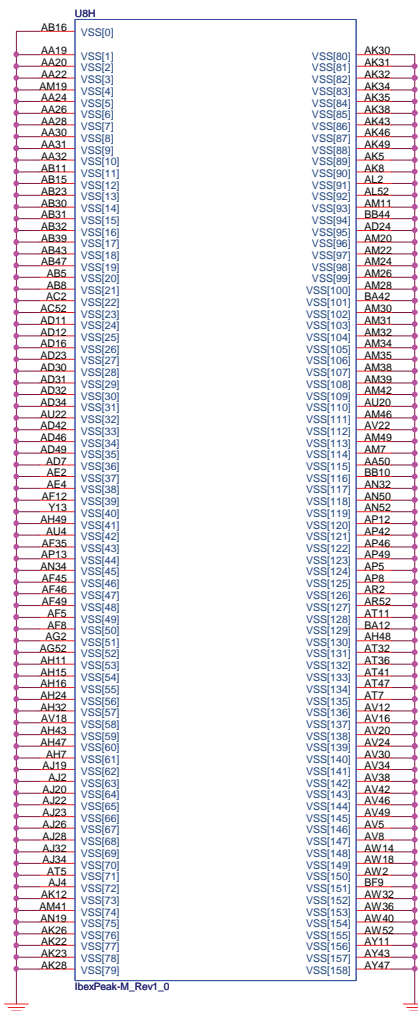
Sheet 10 of 42

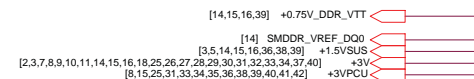
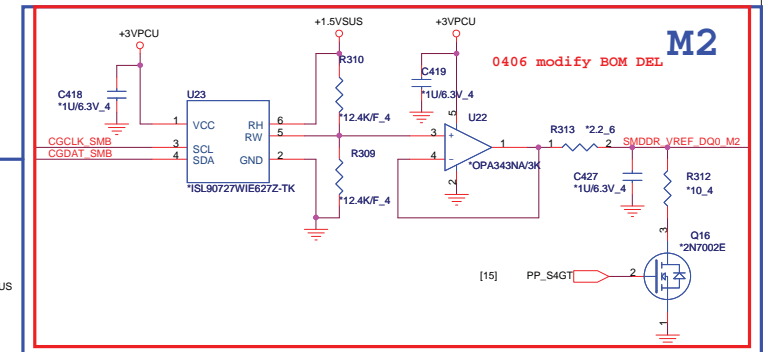
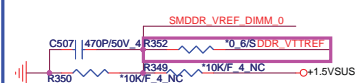
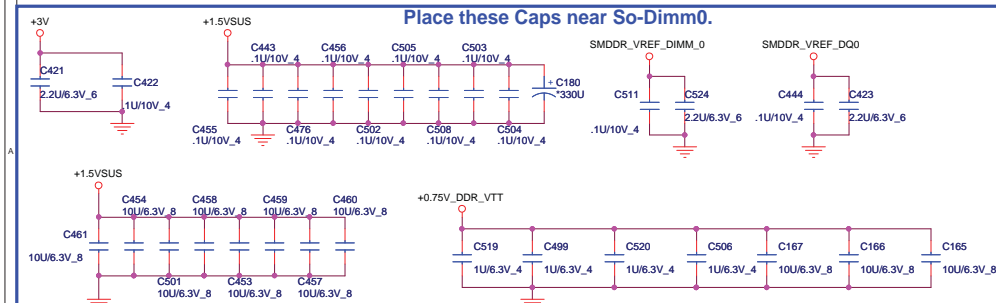
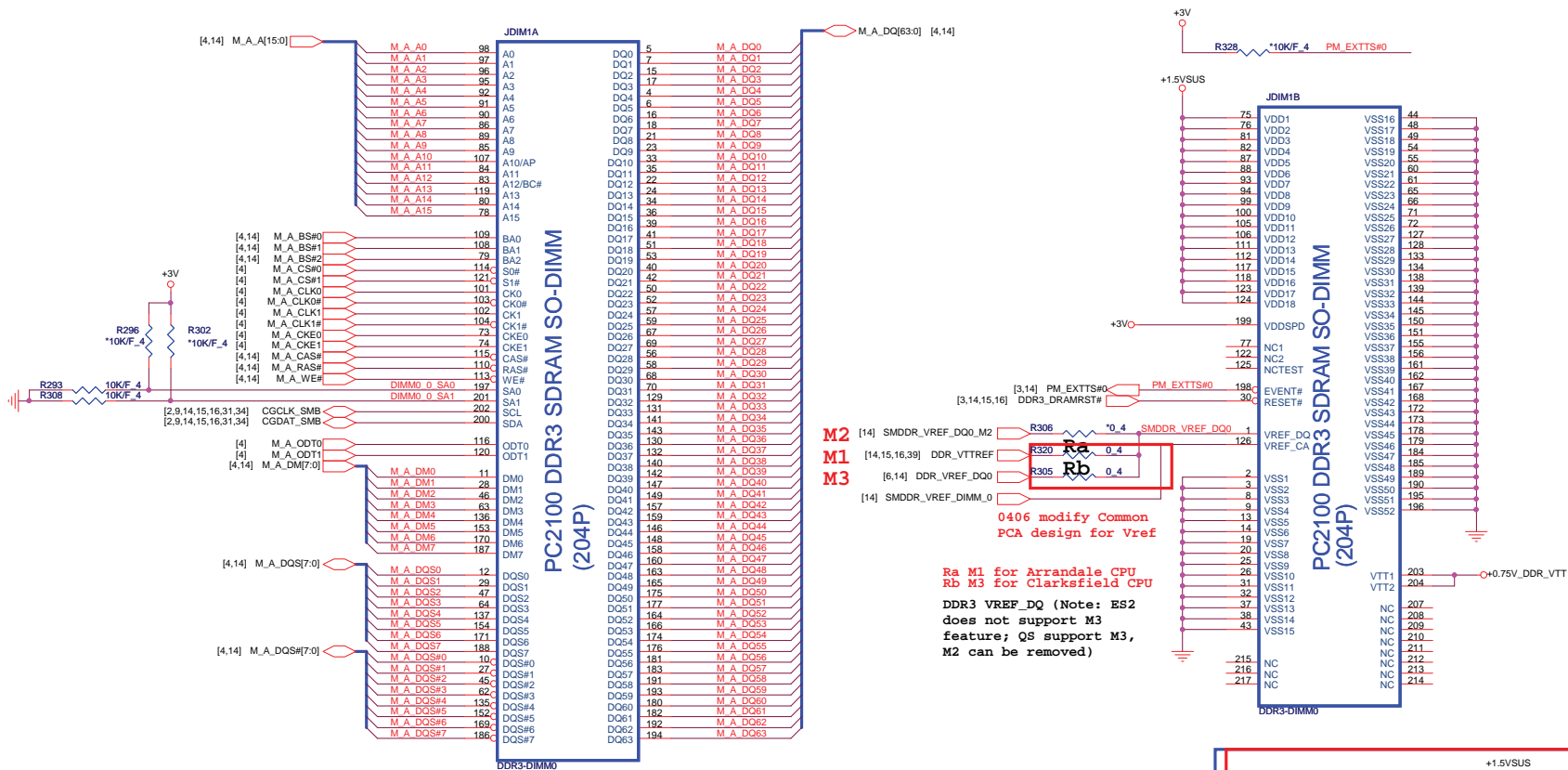
Rev 1A



Move to Page 37

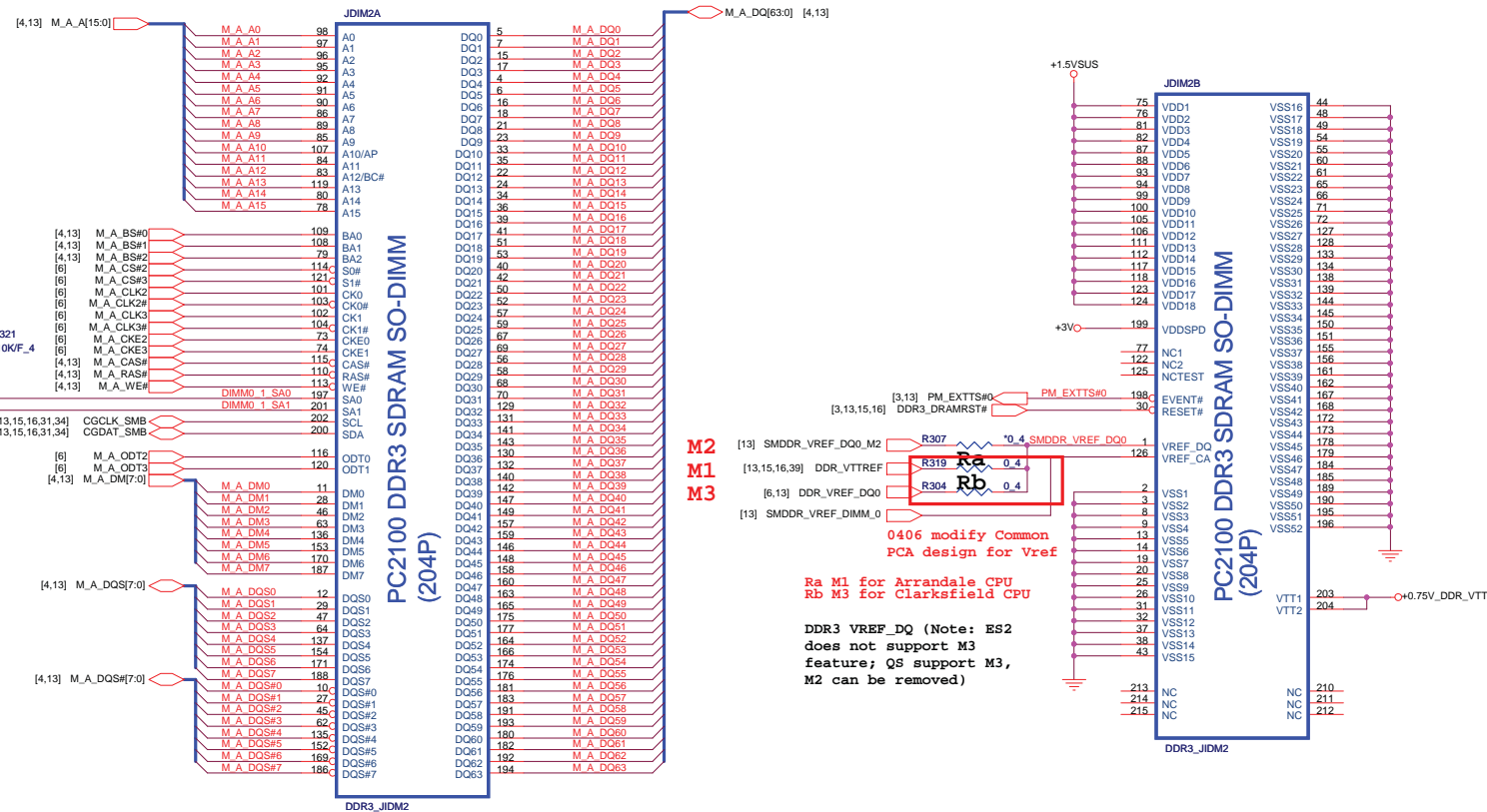
IBEX PEAK-M (GND)



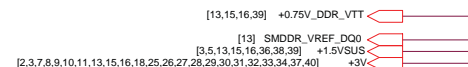
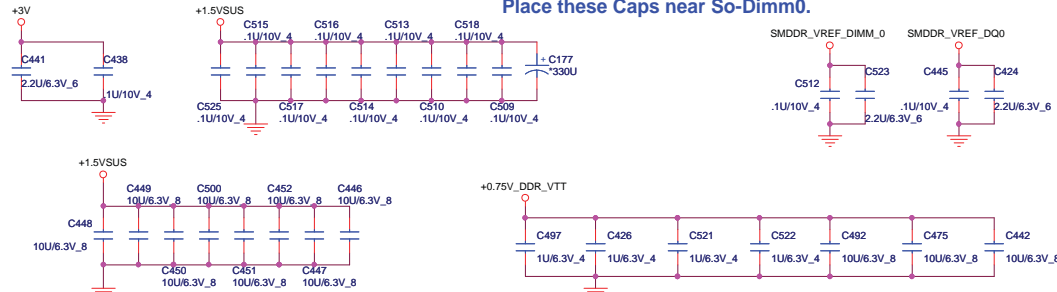


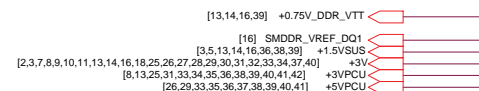
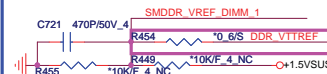
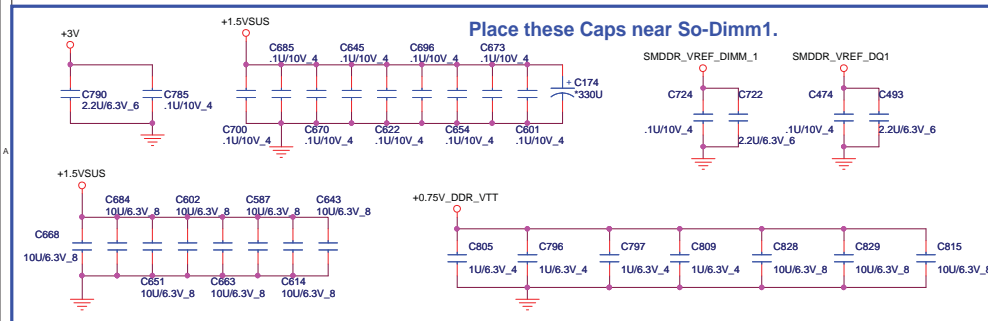
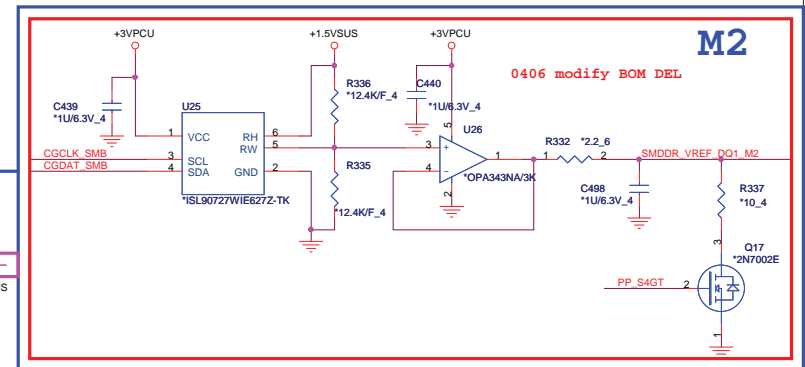
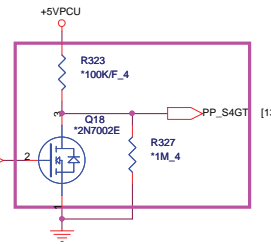
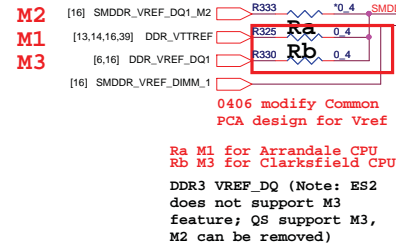
DDR3 -SODIMM 2 A1

14



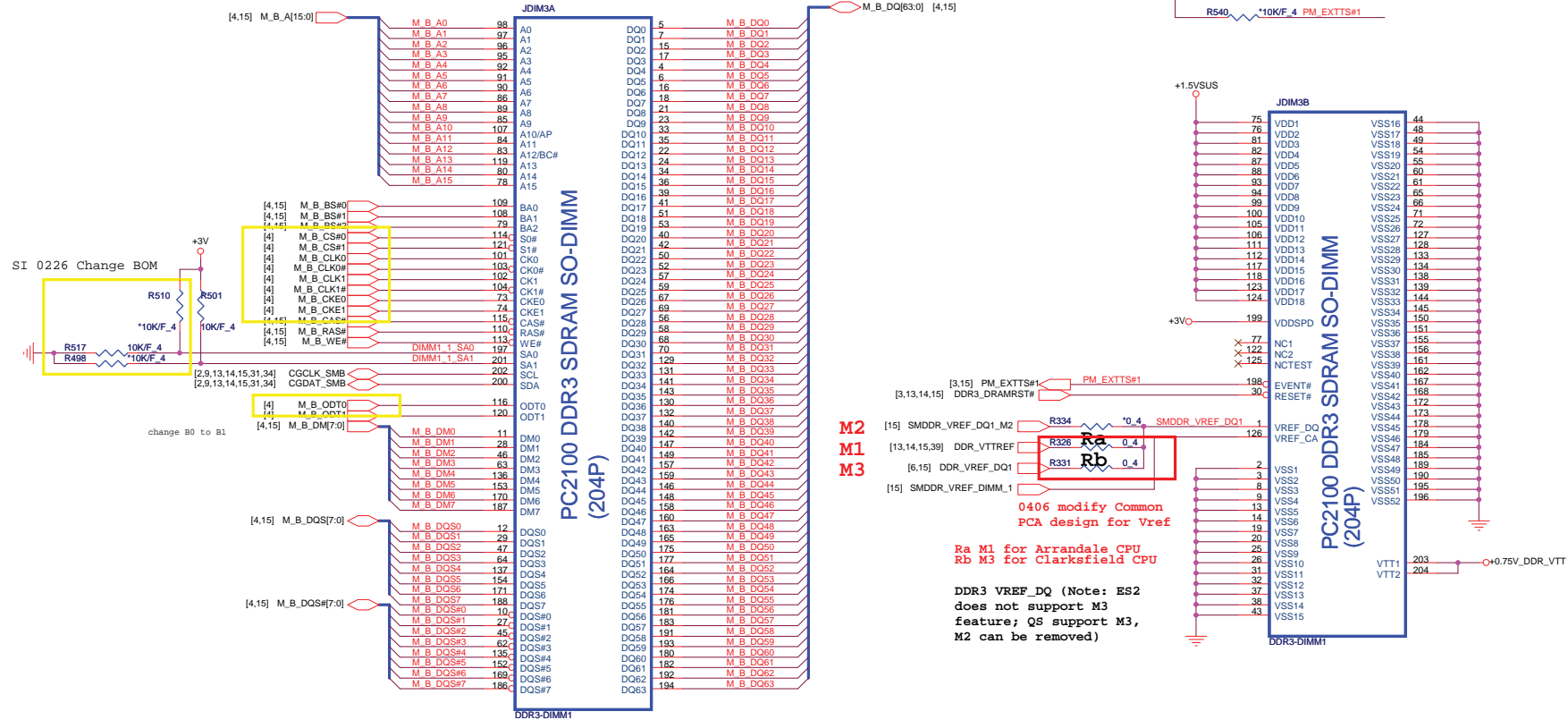
Place these Caps near So-Dimm0.



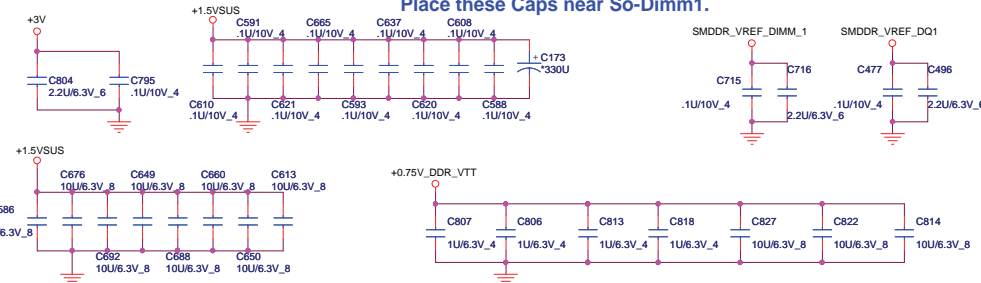


DDR3 -SODIMM 4 B0


16



Place these Caps near So-Dimm1.



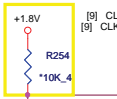
[2,7,8,9,11,26,27,36,37] +1.05V<
[3,5,10,11,36,37] +1.1V_VTT<
[2,3,7,8,9,10,11,13,14,15,16,18,25,26,27,28,29,30,31,32,33,34,37,40] +3V<
[7,9,10,11,25,40] +3VS5<

	PROJECT : SP7 Quanta Computer Inc.		
	Size Custom	Document Number XDP	Rev 1A
DateFriday, July 10, 2009		Sheet 17 of 42	

PCI EXPRESS INTERFACE

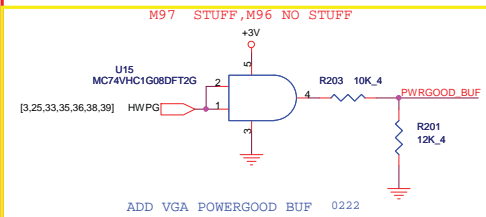


R254 no stuff, SI-1 stage

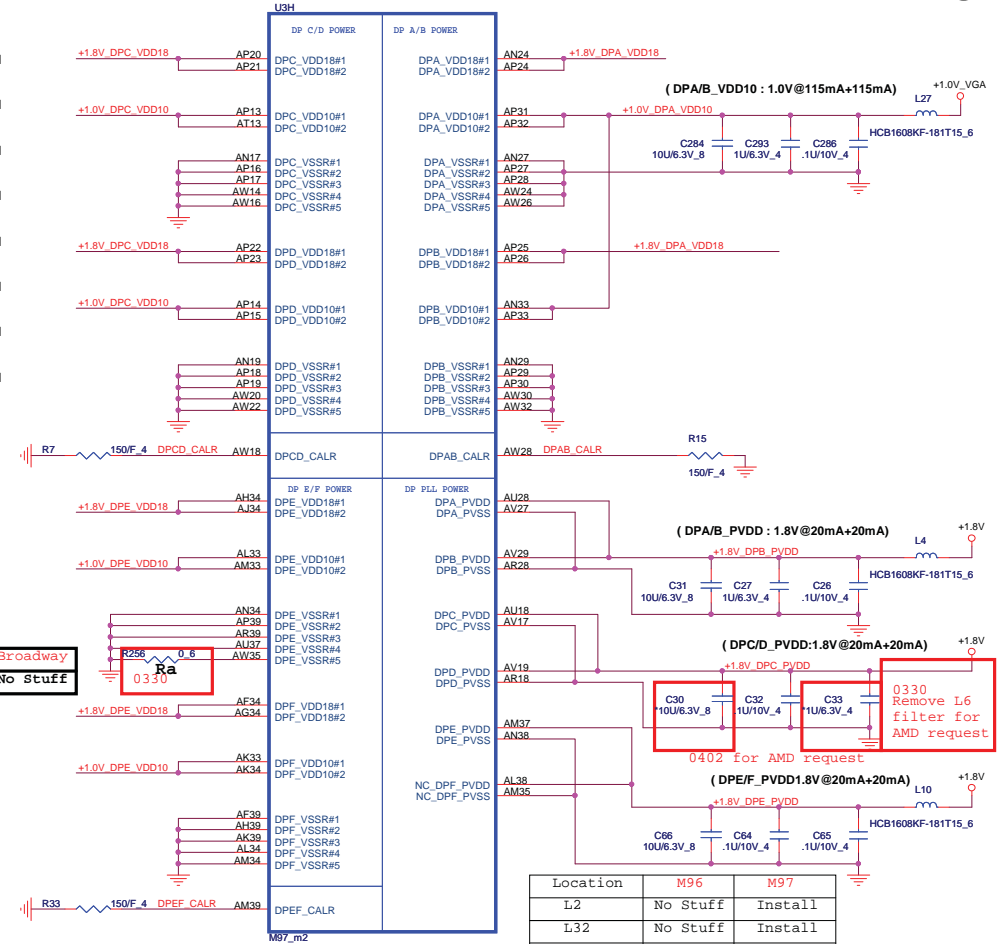


For Broadway, Madison and Park the PWRGOOD ball must be connected to ground

For M97 ONLY
For future ASIC, PWRGOOD_BUF not required should be pulled to ground



	M97	Broadway
Ra	Stuff	No Stuff



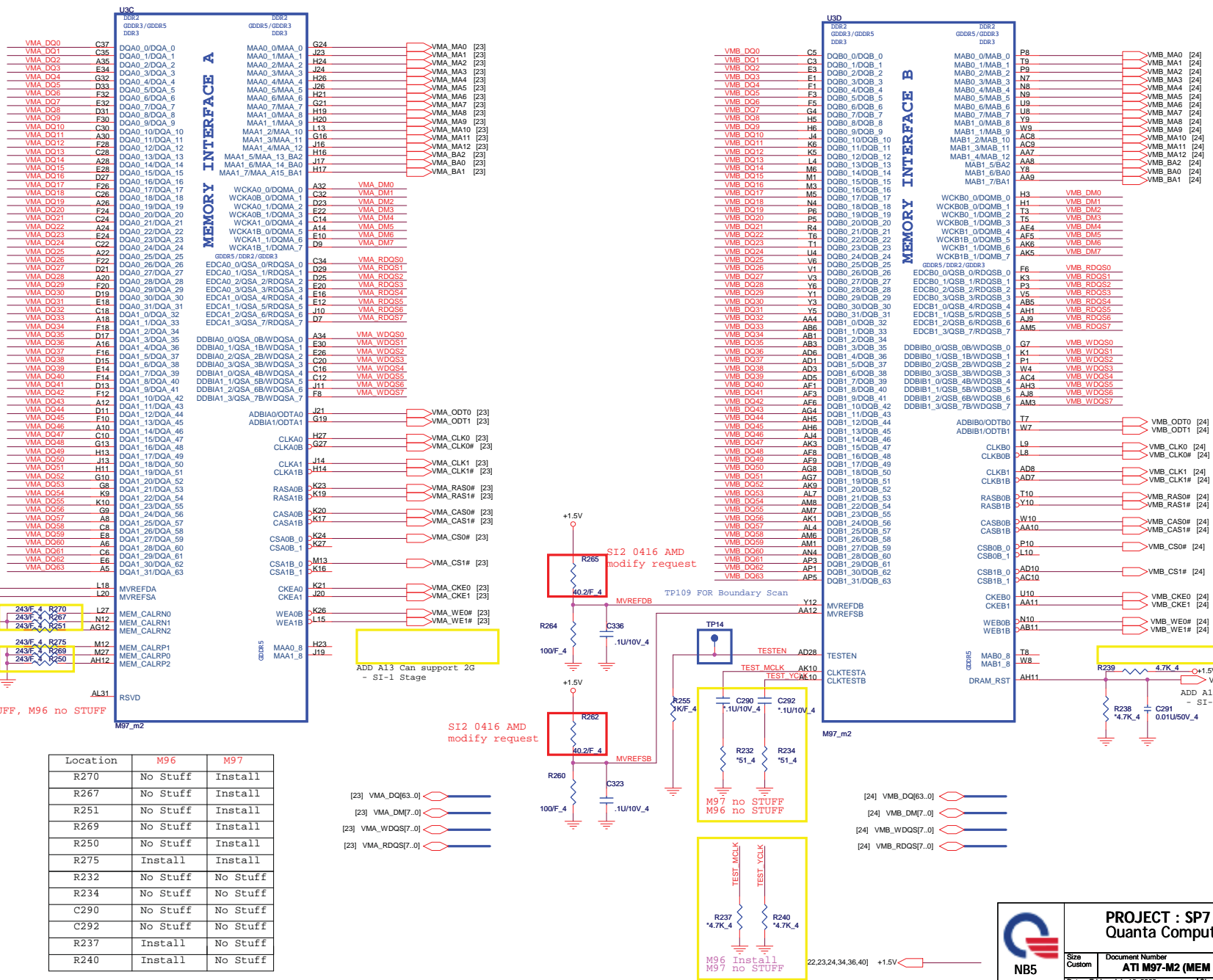
Location	M96	M97
L2	No Stuff	Install
L32	No Stuff	Install
C7	No Stuff	Install
C6	No Stuff	Install
C22	No Stuff	Install
C273	No Stuff	Install
C279	No Stuff	Install
C280	No Stuff	Install
U15	No Stuff	No Stuff
R203	No Stuff	No Stuff
R201	No Stuff	No Stuff
R254	No Stuff	Install
C245	No Stuff	Install

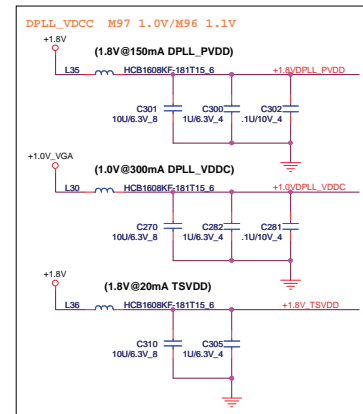
[2,3,7,8,9,10,11,13,14,15,16,25,26,27,28,29,30,31,32,33,34,37,40] +1.0V_VGA
[5,10,11,20,22,34,39] +1.8V
[3,25,33,35,36,38,39] +3V

PROJECT : SP7
Quanta Computer Inc.

Size Custom Document Number **ATI M97-M2 (PCIe I/F) 1/5** Rev 1A

Date: Friday, July 10, 2009 Sheet 18 of 42





MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Hinxy	64*16-800MHZ	H5TQ1G63BFR-12C
0001	Samsung	64*16-800MHZ	K4W1G1646E-HC12
0010	Samsung	64*16-900MHZ	K4W1G1646E-HC11
0011		Reserved	Reserved
0100		Reserved	Reserved
0101		Reserved	Reserved
0110		Reserved	Reserved
1000		Reserved	Reserved
1001		Reserved	Reserved
1010		Reserved	Reserved
1011		Reserved	Reserved
1100		Reserved	Reserved
1101		Reserved	Reserved
1110		Reserved	Reserved
1111		Reserved	Reserved

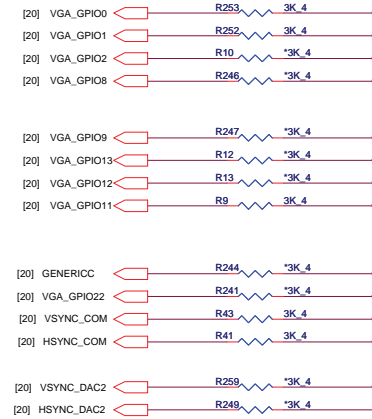
GPI015	GPI020	+VGCORE
Low	Low	0.85V
Low	High	0.90V
High	Low	0.95V
High	High	1.00V

GPIO6	+VDDCI
High	1.07V
Low	1.12V

USB

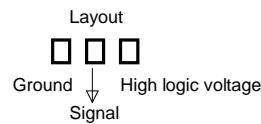
STRAPS

+3V_VGA



Location	M96	M97
pull-up for straps	10K (CS31002FB26)	3K (CS23002FB11)

Overlap pads to save space and to prevent assembly of both resistors.



Strap Name	Pin	Straps description	Default Value
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	1
STRAP_BIF_CLK_PM_EN	GPIO8	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
CONFIG[3] CONFIG[2] CONFIG[1] CONFIG[0]	GPIO9 GPIO13 GPIO12 GPIO11	GPIOs 13, 12, 11 (config 3.2.1.0): a- If BIOS_ROM_EN = 1, then Config[3:0] defines the ROM Type: b- If BIOS_ROM_EN = 0, then Config[3:0] defines the Aperture size: Size of the primary memory apertures claimed in PCI configuration space 000 = 128MB 001 = 256MB 010 = 512MB 011 = 1GB 100 = 2GB 101 = 4GB 110 = 8GB 111 = 16GB	0001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0
AUDIO[0]	VSYNC		0
AUD(1)	HSYNC	HSYNC - HDMI_EN HDMI connector presence. 0 ? No HDMI connector is present on PCB 1 - HDMI connector is present on the PCB HDMI	1
VSYNC_DAC2	V2SYNC	If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host Interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0
HSYNC_DAC2	H2SYNC		0
GENERICC			0

GND

VSS_MECH#1
VSS_MECH#2
VSS_MECH#3

M97_m2



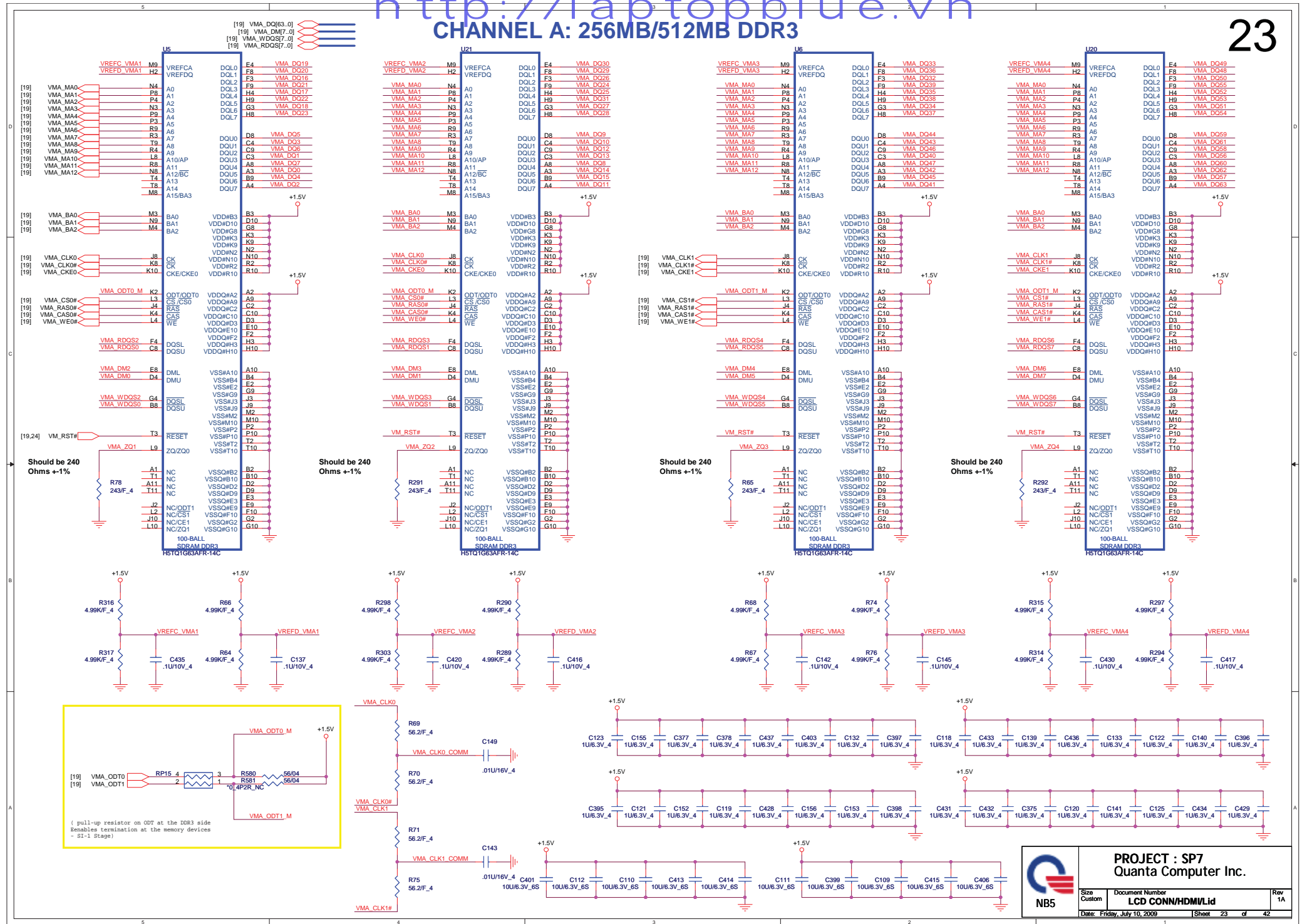
PROJECT : SP7
Quanta Computer Inc.

Size Custom	Document Number ATI M97(GND&Str&Ther)4/5	Rev 1A
Date: Friday, July 10, 2009	Sheet 21 of 42	

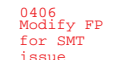
[20,22,25,40] +3V_VGA

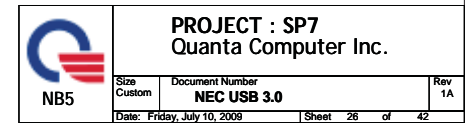


Size Custom	Document Number ATI M97-M2 (POWER) 5/5	Rev 1A
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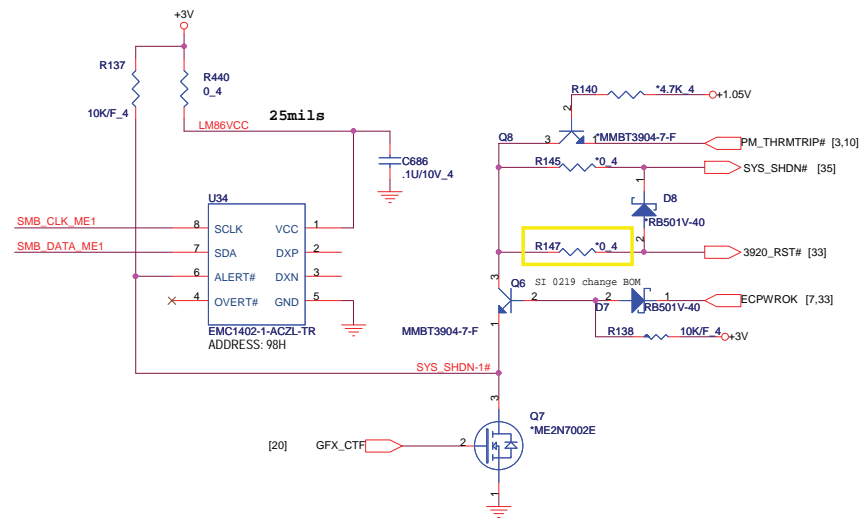




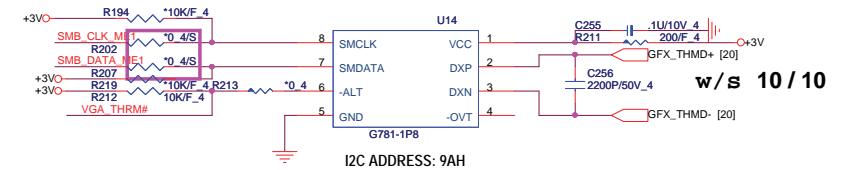




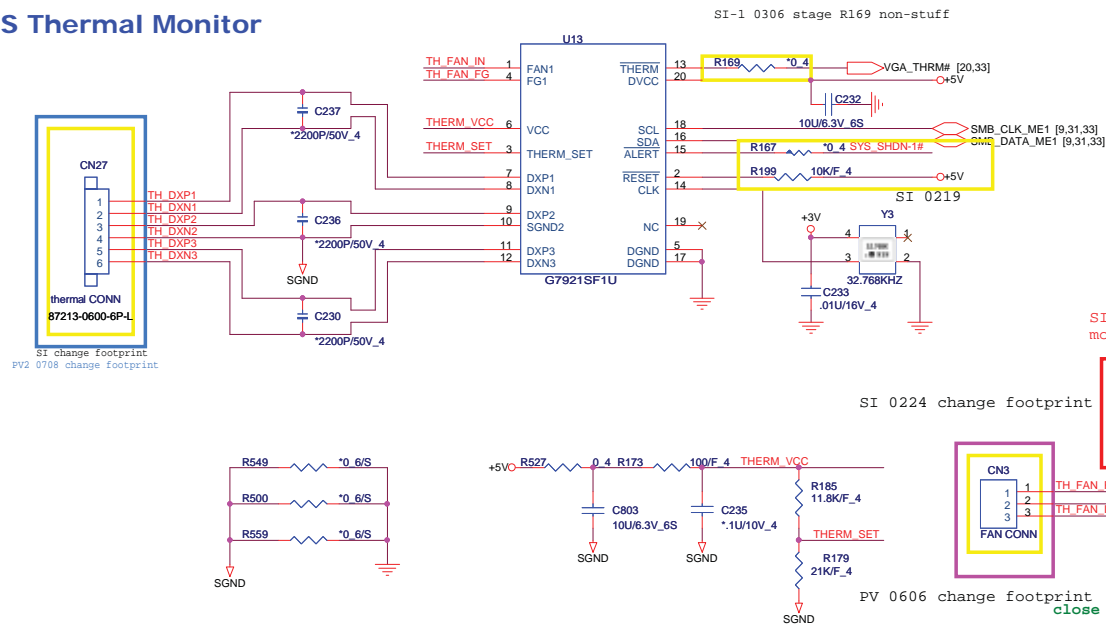
CPU THERMAL MONITOR



GPU Thermal Sensor

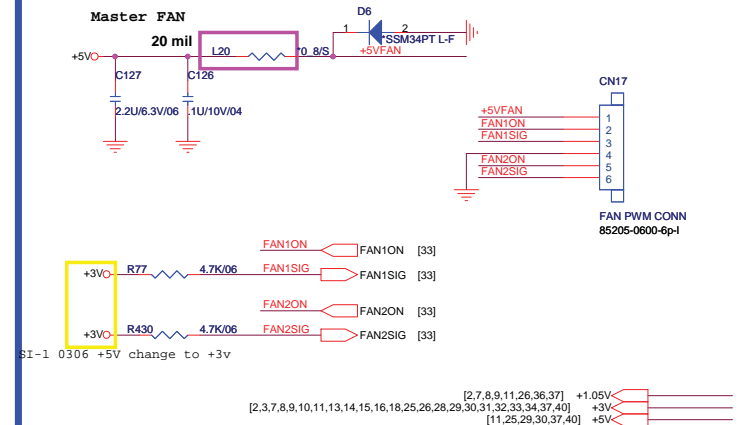


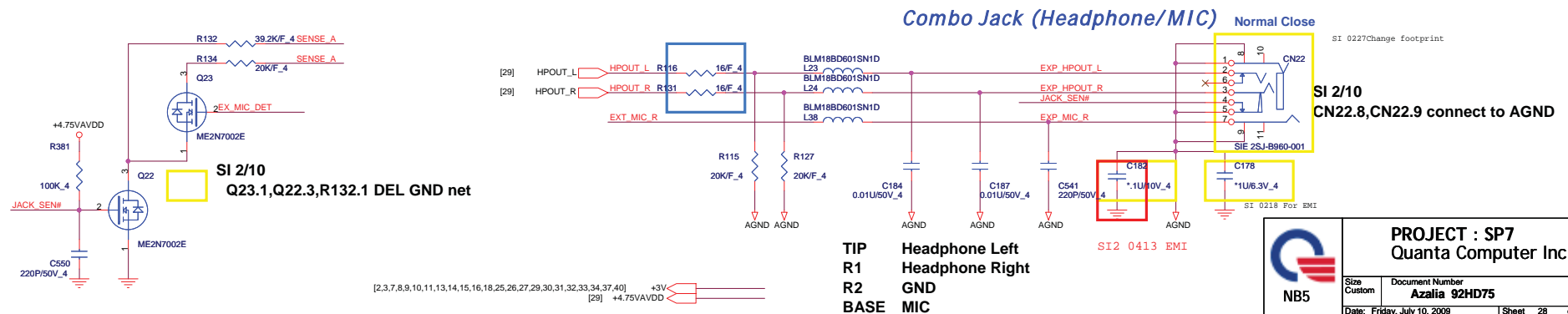
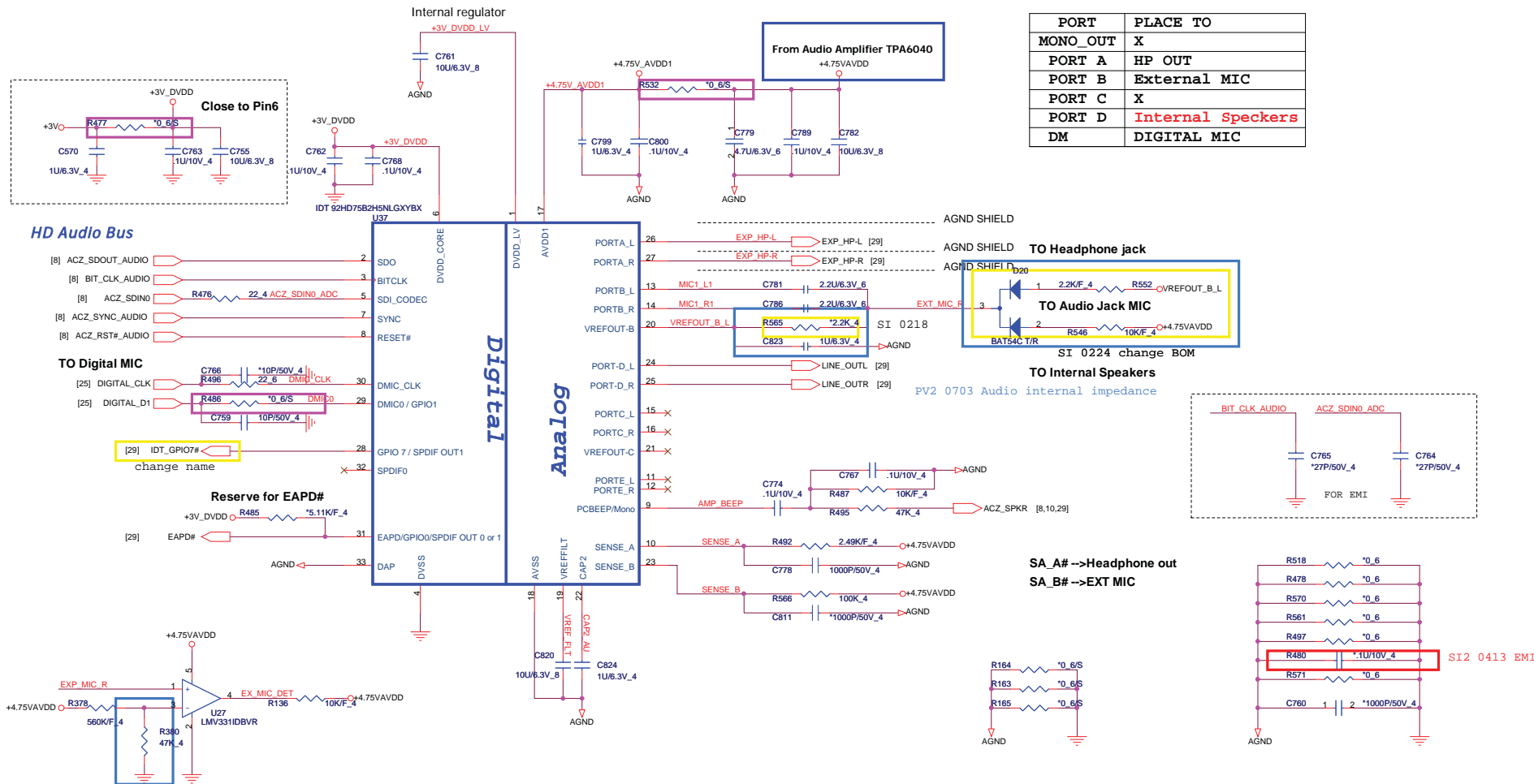
SYS Thermal Monitor



CPU FAN1/2 CONN

RPM Control





Low -->un-MUTE
High-->Mute

Change R401 from 10K to 100K

[31,33] MUTE_LED

+5VPCU

R483
100K/F_4

Change R401 from 10K to 100K

[31,33] MUTE_LED

+3V

R488
10K/F_4

VOLMUTES# 2

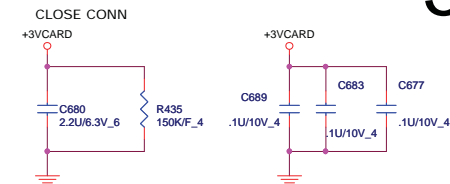
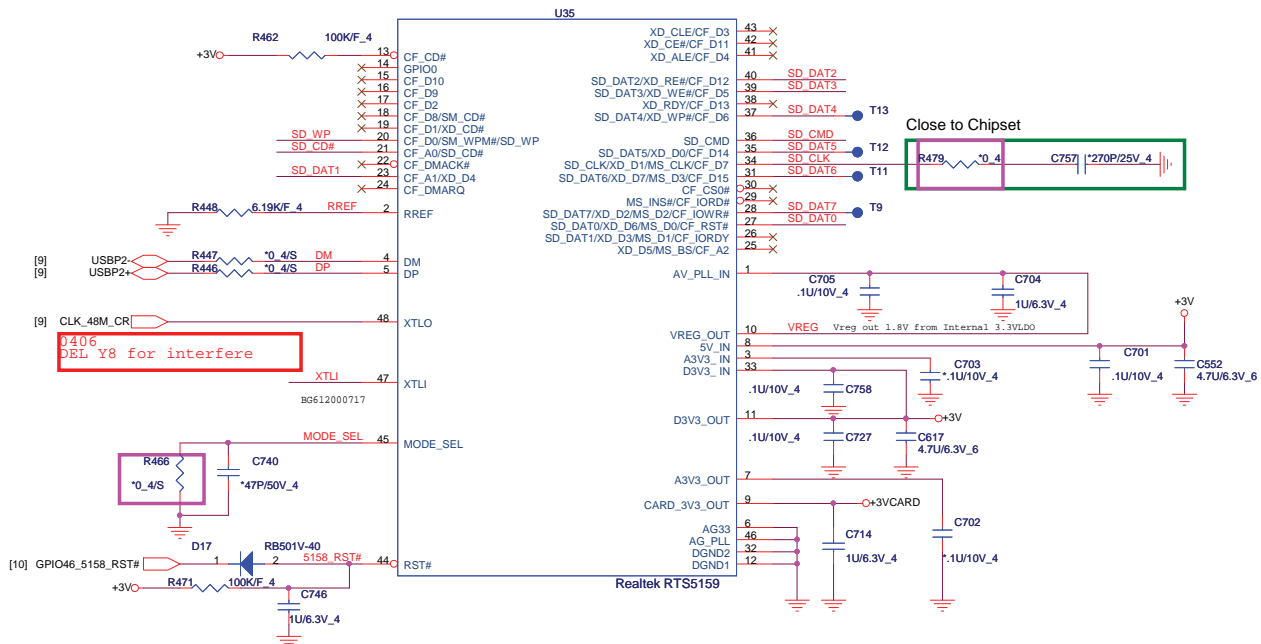
D19
BAT54A

MUTE_LED_R 2

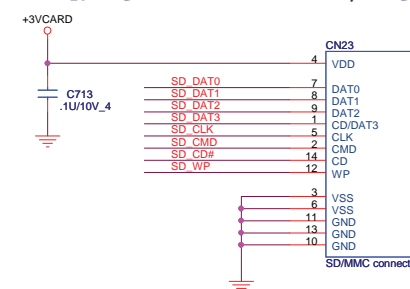
Q31
ME2N7002E

28] IDT_GPIO7#

0216 change name



2 IN1 CARD READER SD/MMC

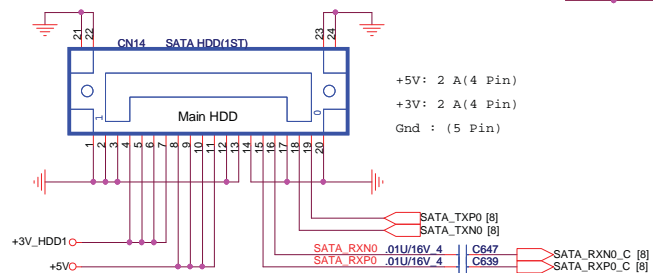


SATA 1.8"/2.5" HDD CONNECTOR

DFHD20MR005

MASTER

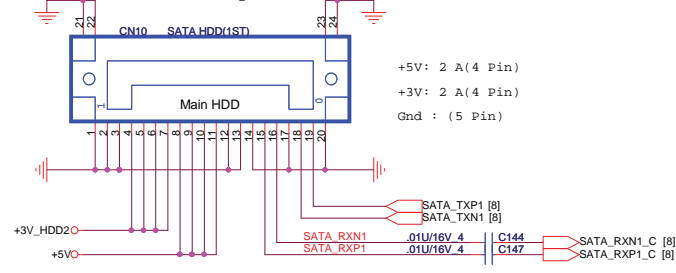
DC Current rating: 0.5 A



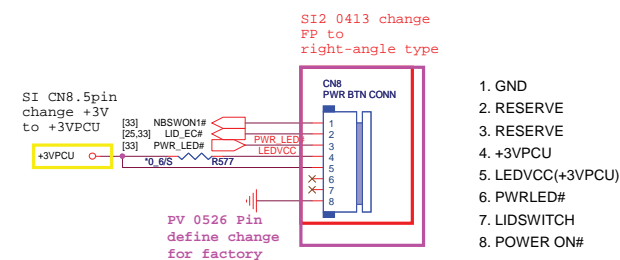
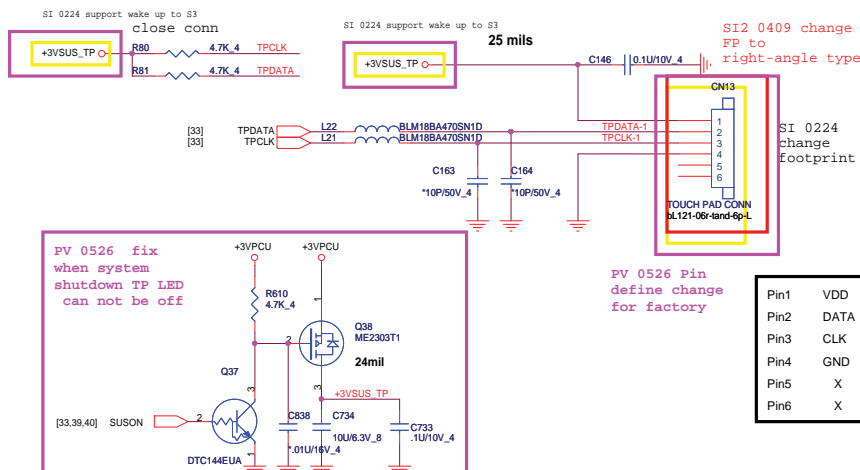
SSD(1) 1.8" CONNECTOR

SLAVE

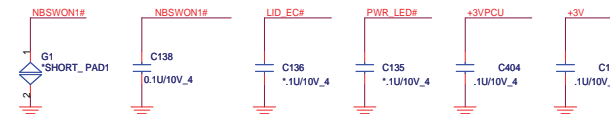
DC Current rating: 0.5 A



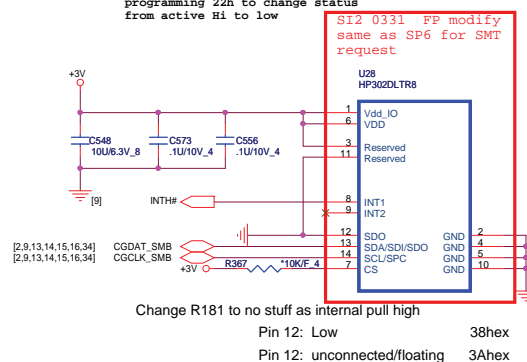
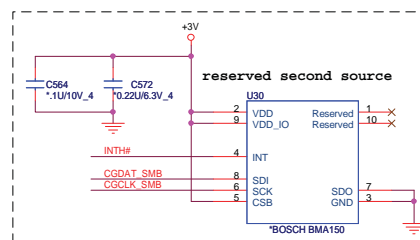
TOUCH PAD CONNECTOR



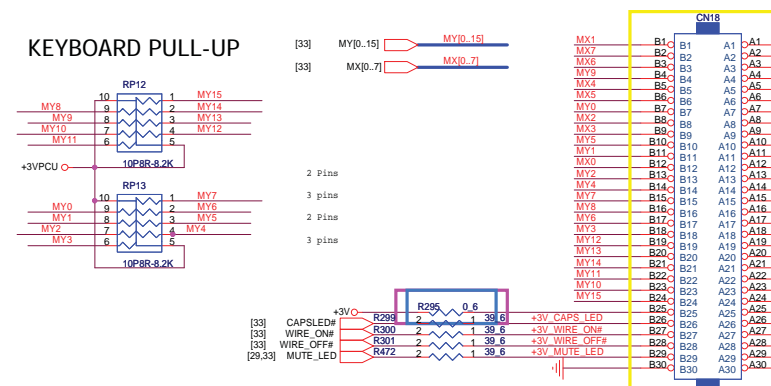
POWER BOTTON CONNECT



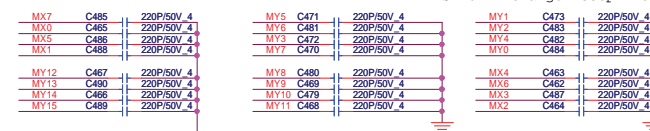
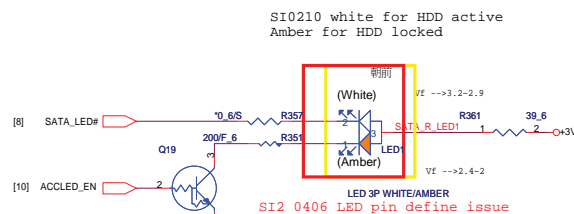
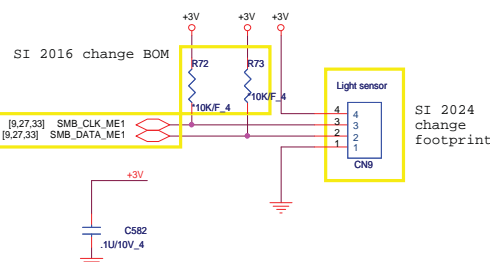
SGT-LIS302DLTR interrupt pin default
is low / active Hi , BIOS need to
programming 22h to change status
from active Hi to low

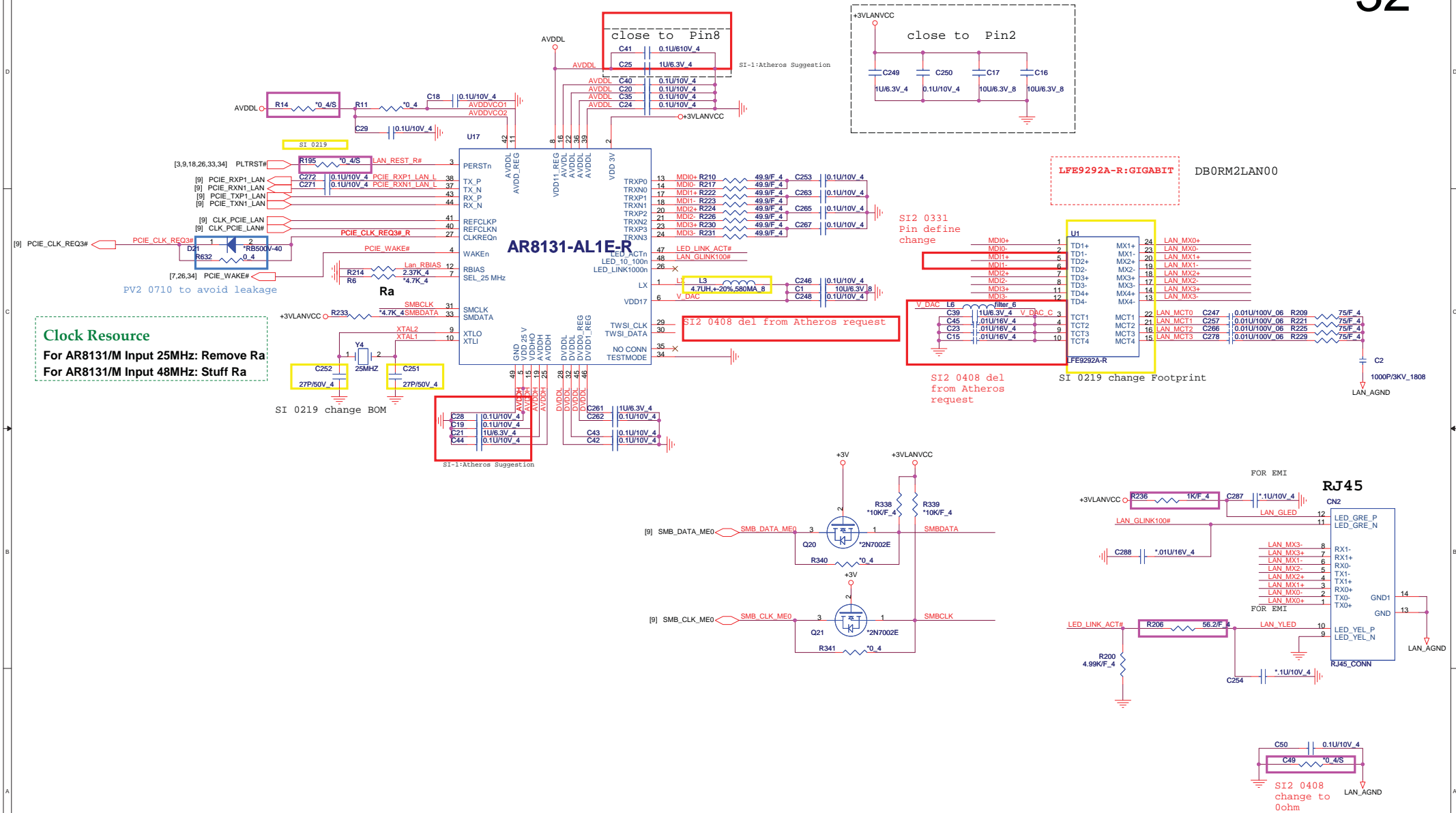


KEYBOARD PULL-UP



LED

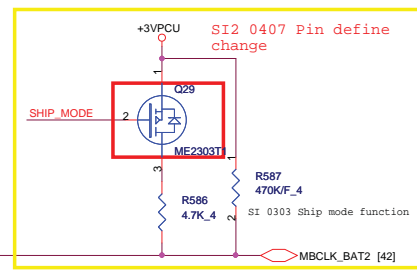
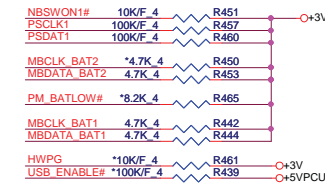




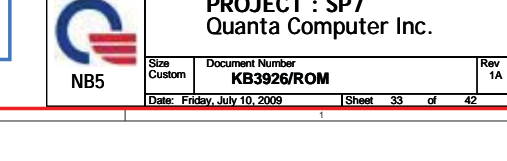
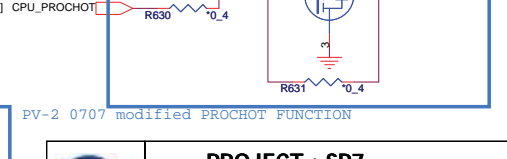
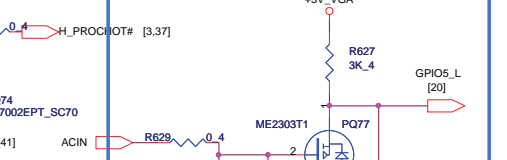
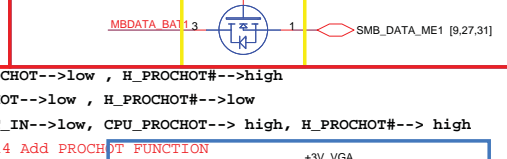
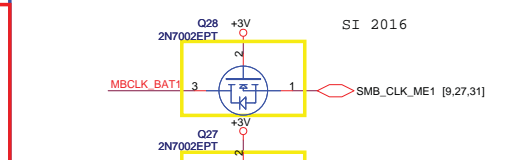
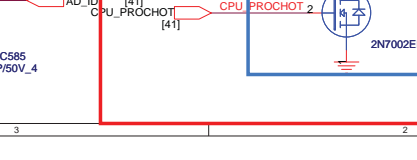
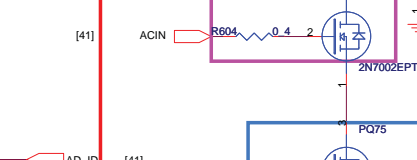
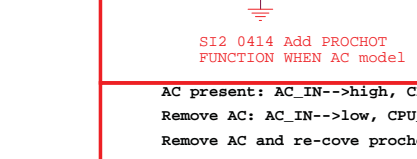
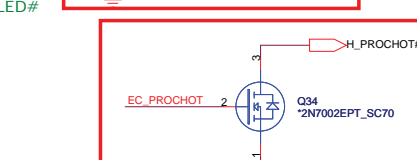
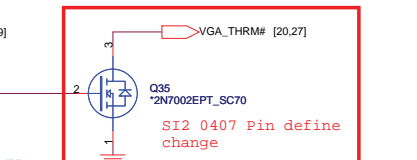
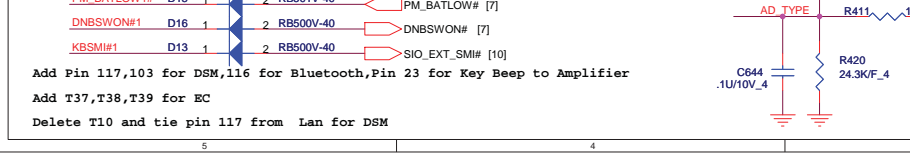
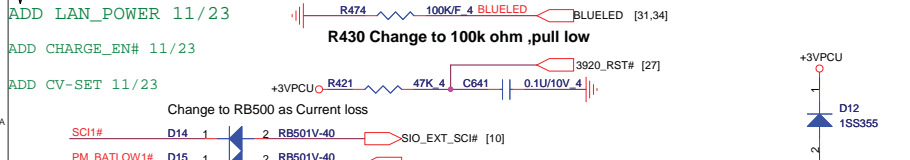
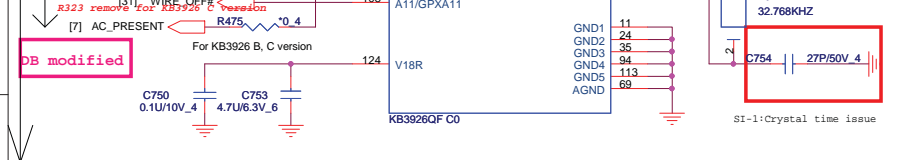
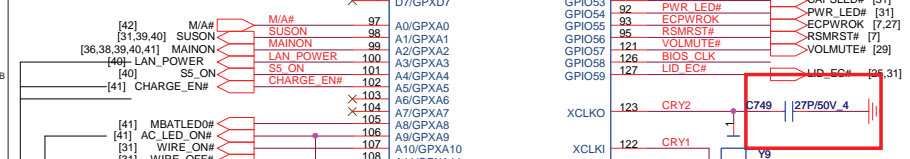
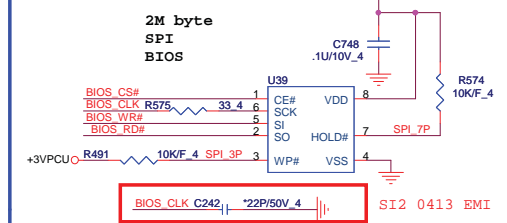
Change U20 layout footprint
to LQFP128-16X16-4-AA1

[15,26,29,35,36,37,38,39,40,41]
[8,13,15,25,31,34,35,36,38,39,40,41,42]
[2,3,7,8,9,10,11,13,14,15,16,18,25,26,27,28,29,30,31,32,34,37,40]

+5VPCU-
+3VPCU-
+3V

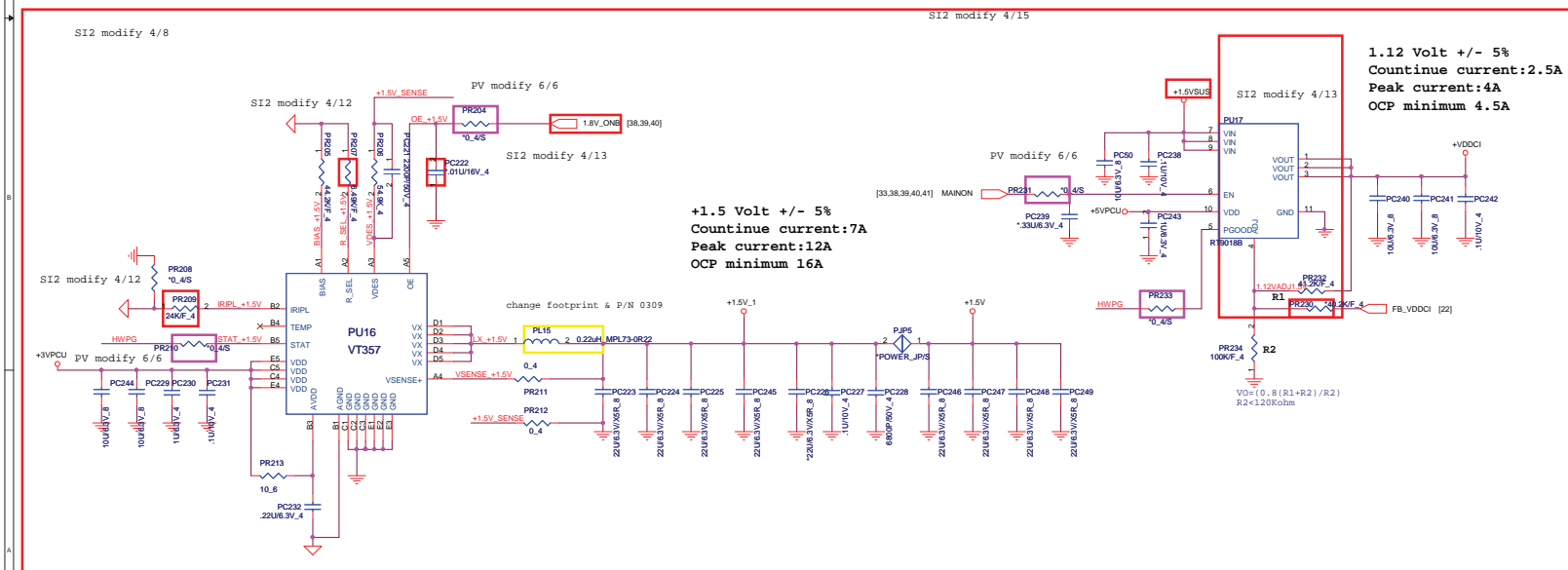
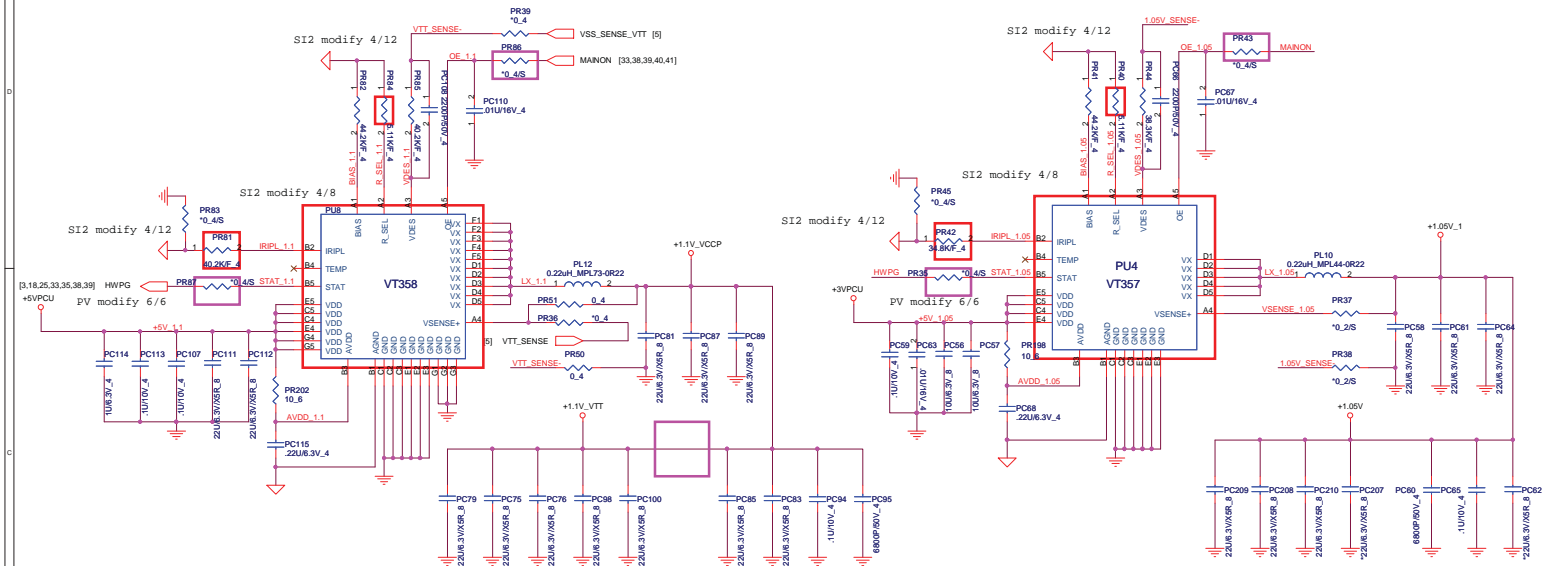


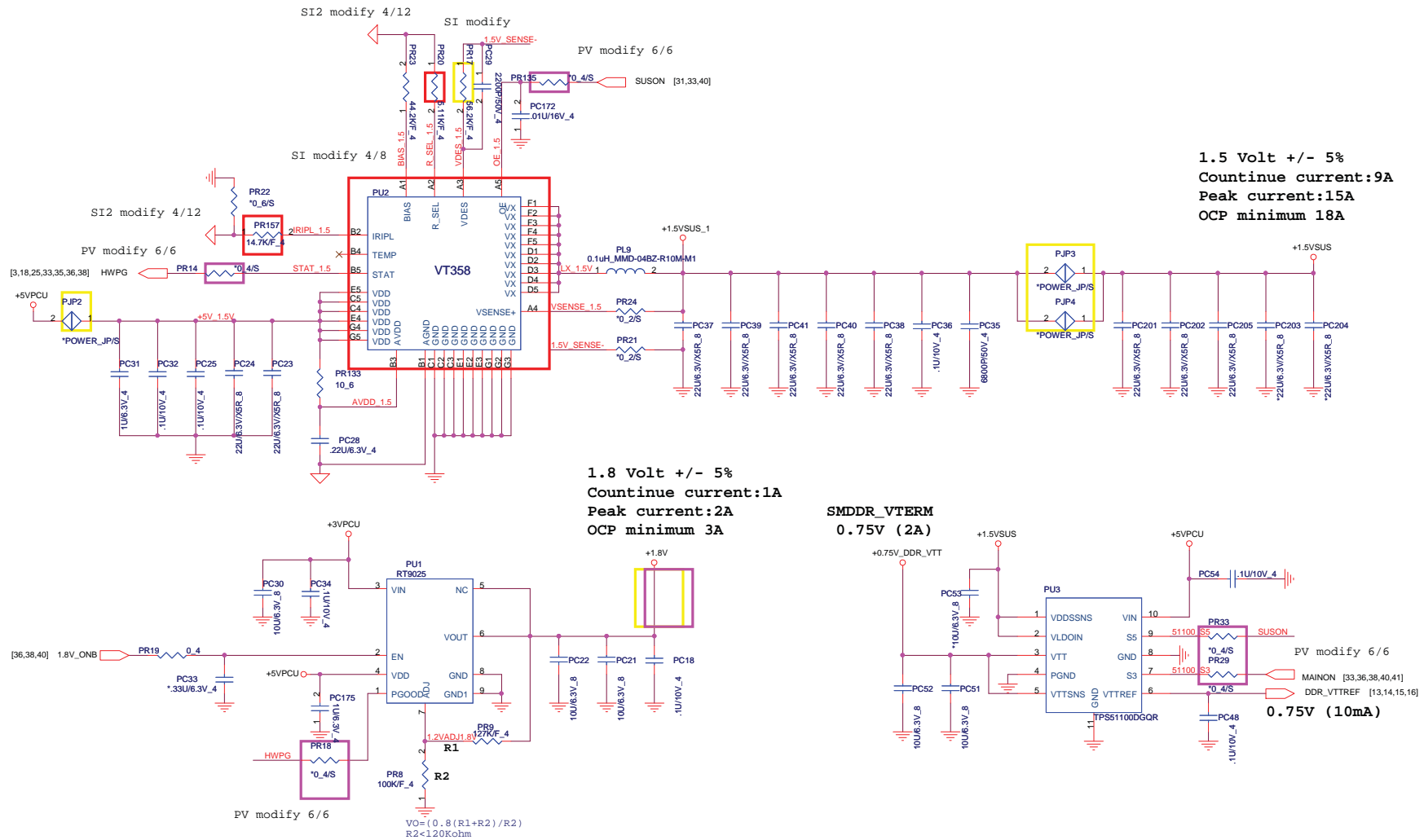
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AMIC AKE38ZN0800
MXIC AKE38FP0200
WINBOND AKE38ZP0N01
EON AKE38ZA0Q00

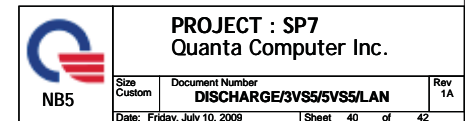


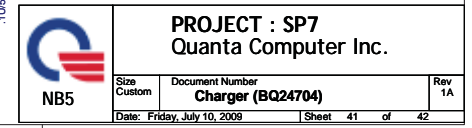
PROJECT : SP7
Quanta Computer Inc.
NB5
Size Custom
Document Number KB3926/ROM
Date: Friday, July 10, 2009
Sheet 33 of 42
Rev 1A













PROJECT : SP7
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Size Custom	Document Number BATTERY SELECTOR	Rev 1A
Date: Friday, July 10, 2009	Sheet 42 of 42	