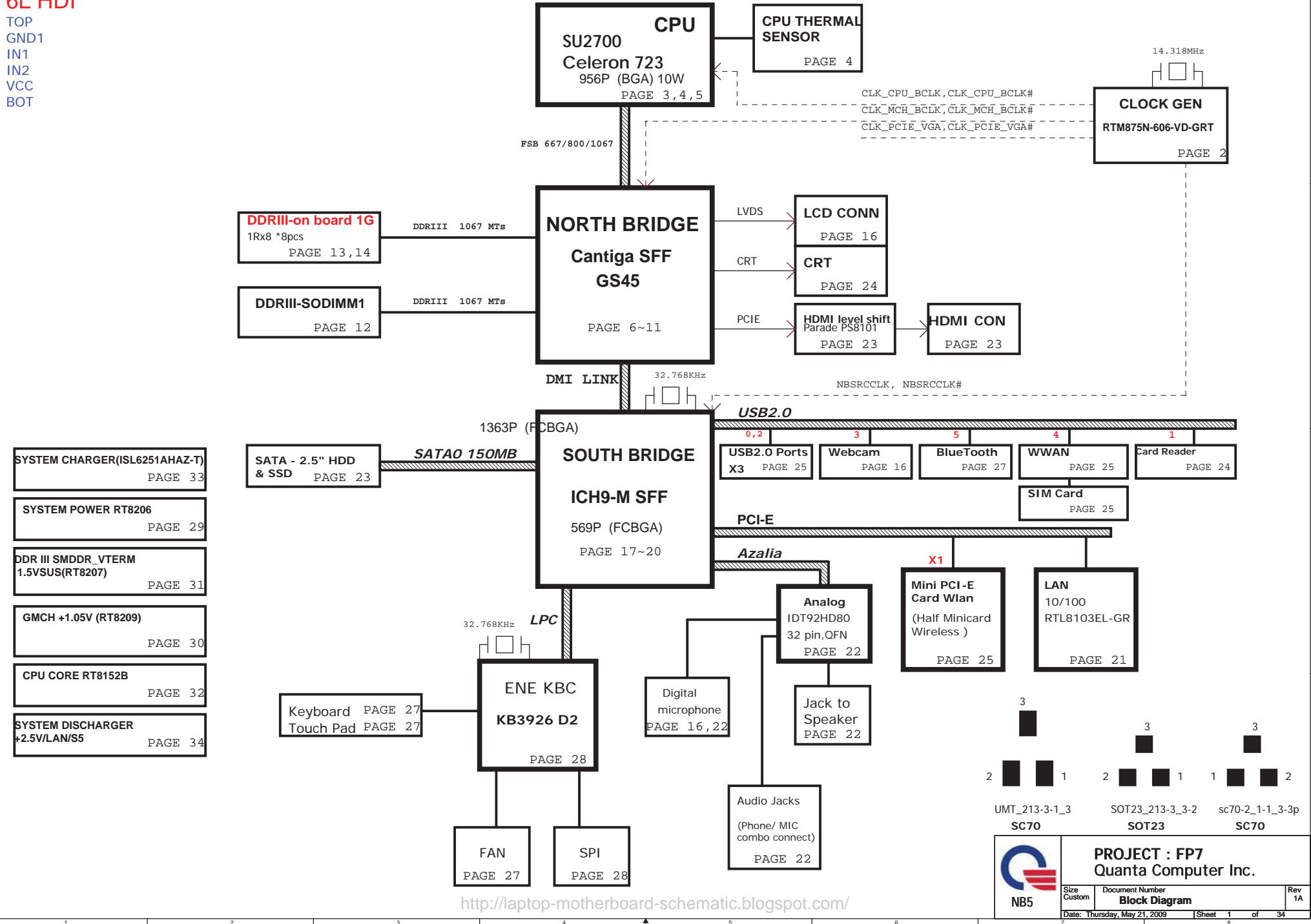


FP7 (CULV) BLOCK DIAGRAM

01

PCB STACK UP
6L HDI

TOP
GND1
IN1
IN2
VCC
BOT



<http://laptop-motherboard-schematic.blogspot.com/>

5/13

5

4

3

2

1

1.Del Vcc_HDA R5234 (short0402)

2.C5533, C5541, C5205, C5291, R5233 咽枯 BGA 條啾 ,叫 ㄟfoot print磊PAD 確 よ

3.op6v-0513 update net import 瓜,叫腊T ㄟ ン swap pin

4.PR158 net change from +5VSUS to +3VSUS.

5.PR182 net change from +10VALW to +15VALW.

6.NET NAME Change from R_CLK_VAG_OE# to R_CLK_WWAN_OE#.

7.NET NAME Change from CLK_VGA_OE# to CLK_WWAN_OE#.

8.New add R8 ,R9, R10 ⇐ CRT_R,CRT_G,CRT_B for EMI

5/14

1.New add C7362 C7366 C7357 C7378 C7379 C7367 for CRT RGB EMI

2.New add GND PAD Footprint SPAD-RE170x945

3.del T5007,T5037,T5039,T5044.

5/15

1.update power schematic for LV cup 笨潰.

5/18

1.update rename.

2.Del H7034,H7033.

3.C7354 and C7359 璫 ン.

4.NEW ADD KBC test PAD on GPXA and GPXD

5.Change footprint CN14,CN3,CN4,CN5,CN7,CN9,PL4,PL5,PL6

6.New add C557 for EMI.

7.R124 Footprint change to RC0402

8.Change LAN from G to 10/100(传Transformer)

9.WWAN-->New add R368,R360,C512,C513,C522.

10.DEL NET-->MDI2+,MDI2-,MDI3+,MDI3-.

11.ADD R734,C534,R378,RC523 for HSYNCcmVSYNC.

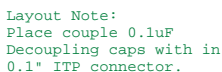
<http://laptop-motherboard-schematic.blogspot.com/>

Title			
<Title>			
Size	Document Number		Rev
A3	<Doc>		<Rev Co
Date:	Thursday, May 21, 2009	Sheet	1 of 1



27M_SEL PIN13	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDDT_100	SRCT1/LCDDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33



Signal	ITP disable guidelines
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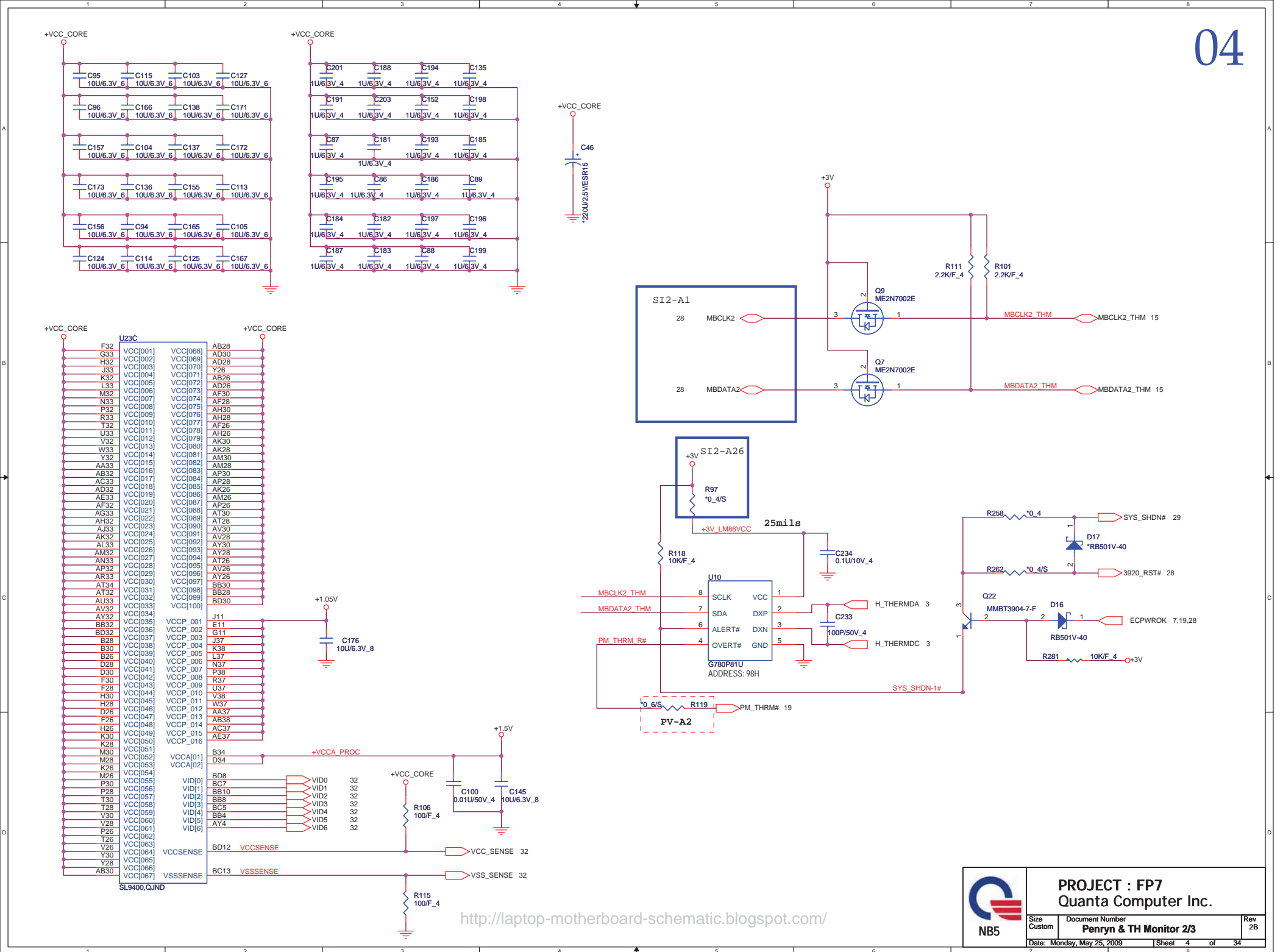
*PAD T14 CPU_TEST3
*PAD T40 CPU_TEST5
*PAD T27 CPU_TEST6

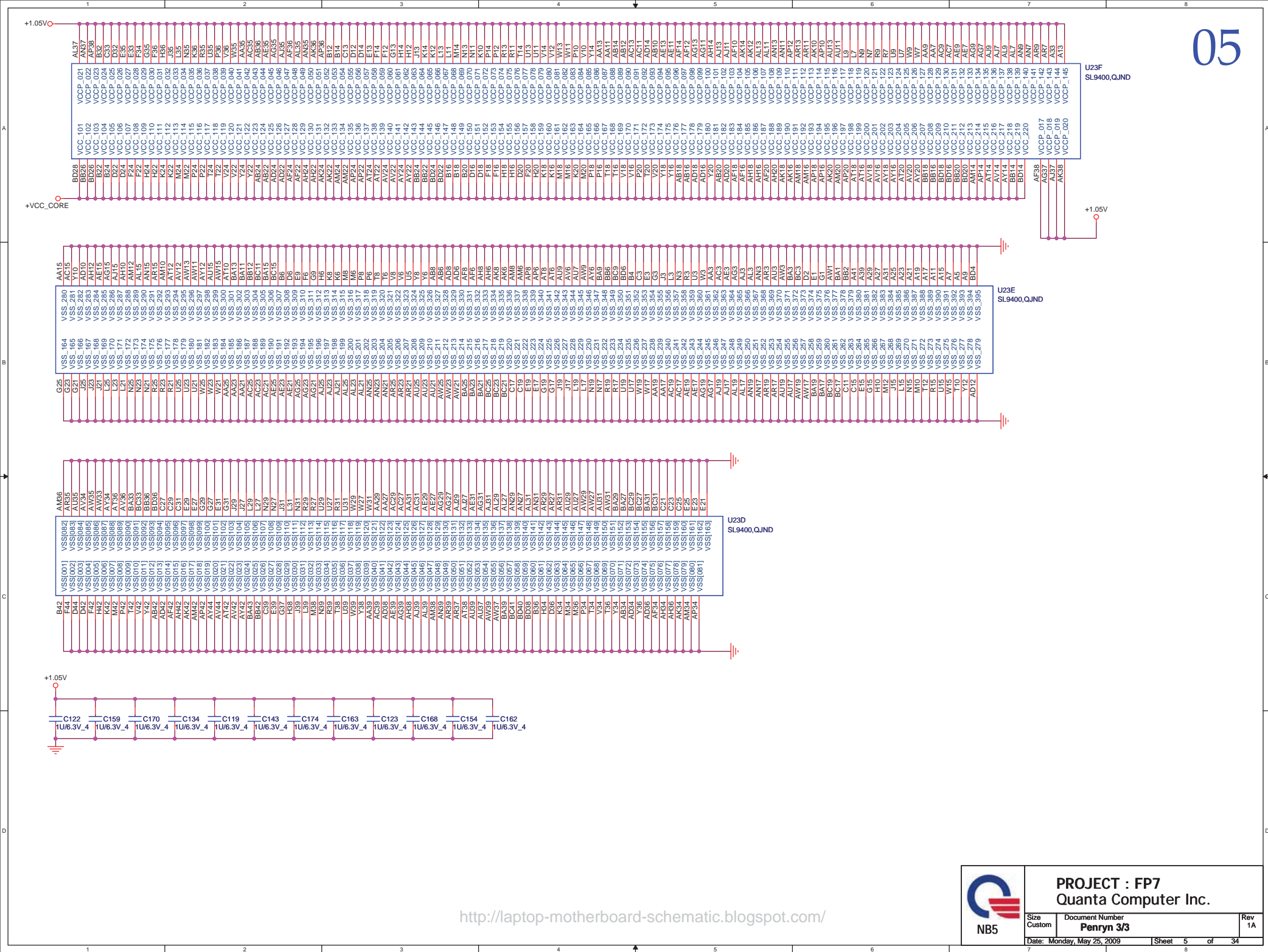
For the purpose of testability, route these signals through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.



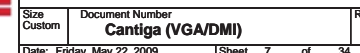
Size Custom	Document Number Penryn (HOST BUS) 1/3
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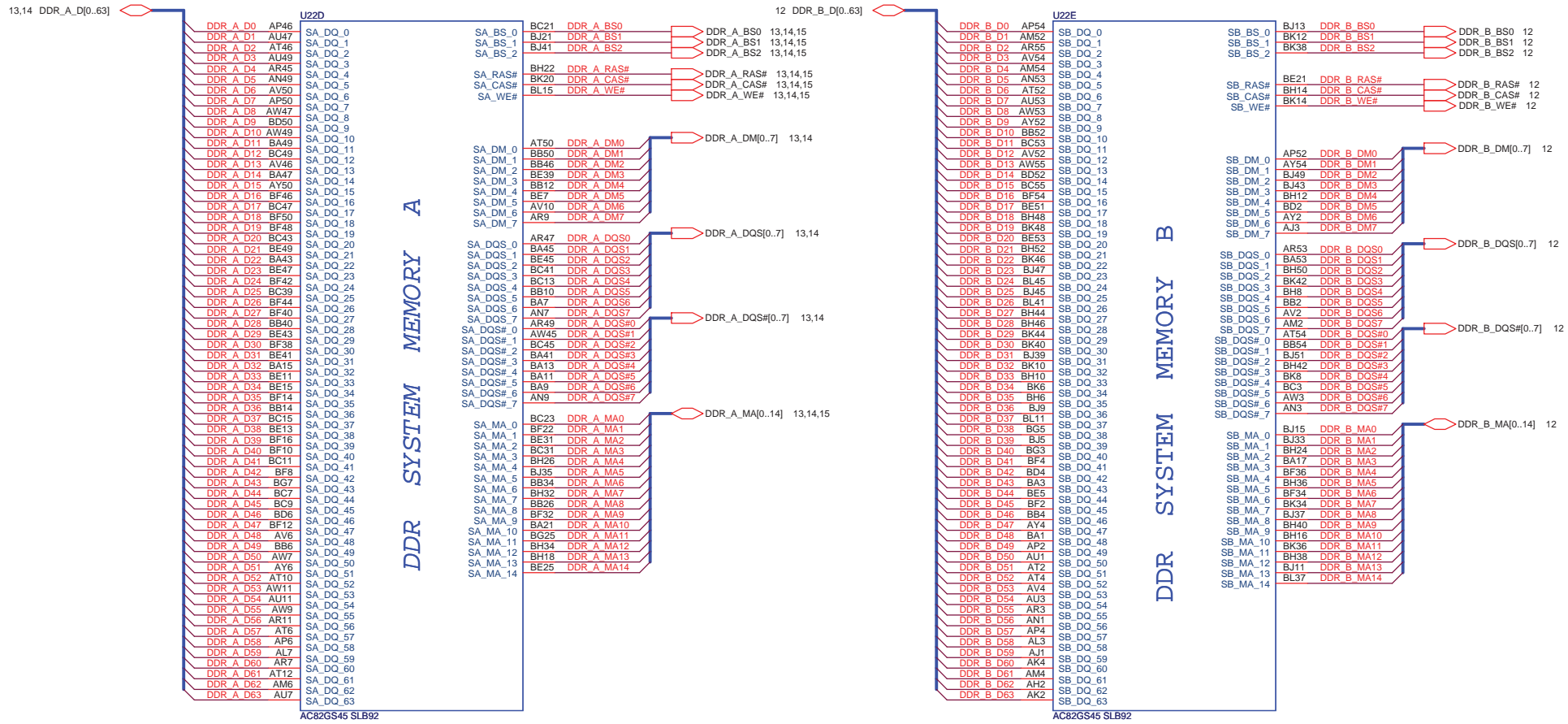
Date: Monday, May 25, 2009	Sheet 3 of 34
----------------------------	---------------









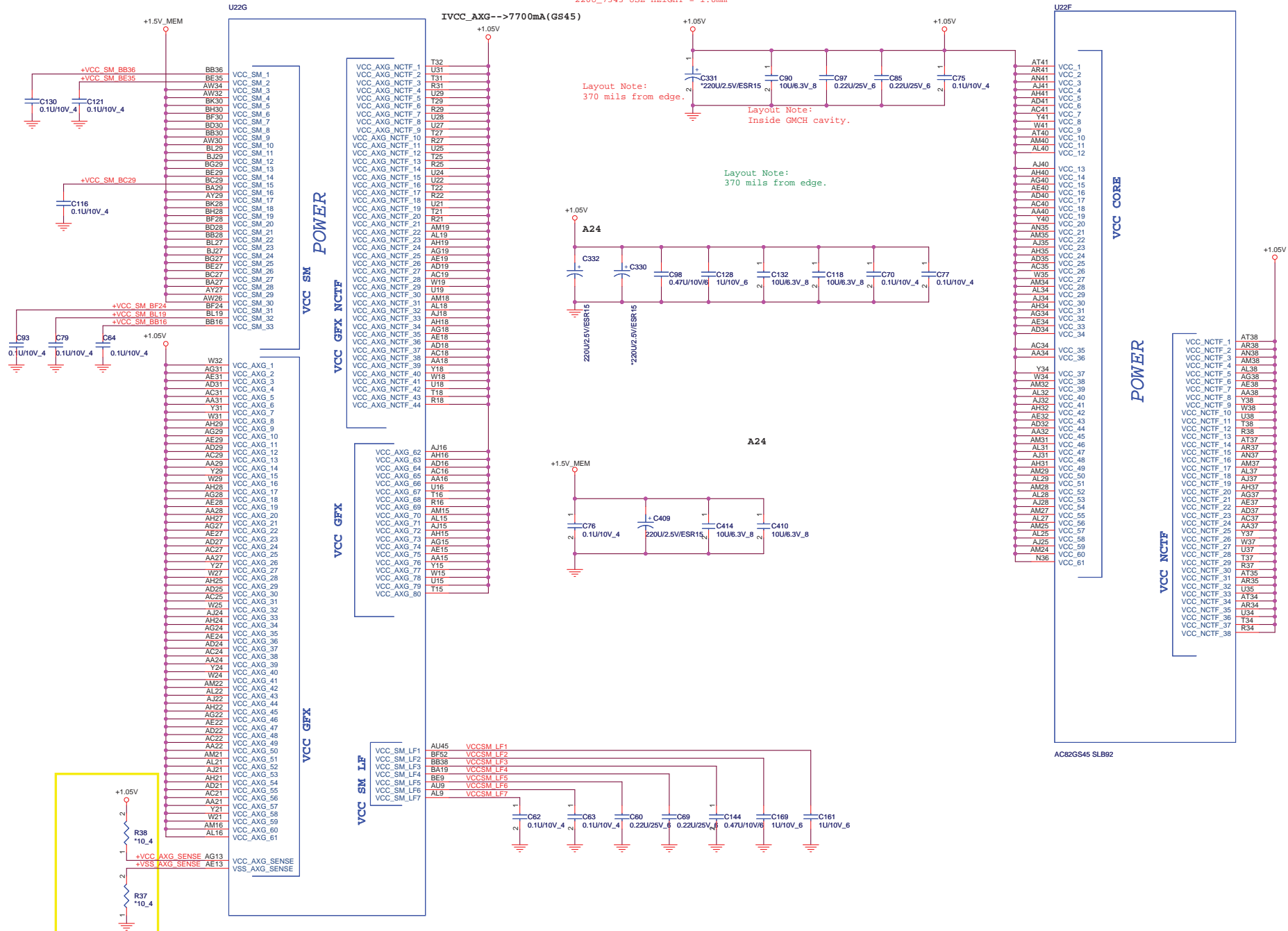


 NB5	PROJECT : FP7 Quanta Computer Inc.	
	Size Custom Document Number Cantiga (DDR interface)	Rev 1A
	Date: Thursday, May 21, 2009 Sheet 8 of 34	

Ivcc_sm (DDR3,1.5V,1066MTs) -->4140mA

220U_7343 USE HEIGHT = 1.8mm

IVCC_AXG-->7700mA(GS45)

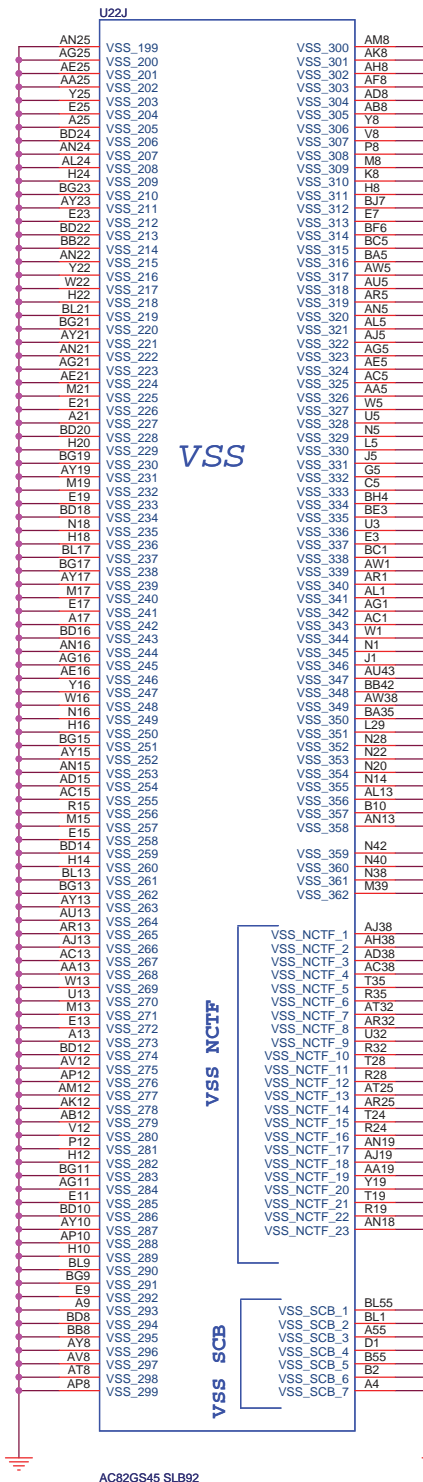
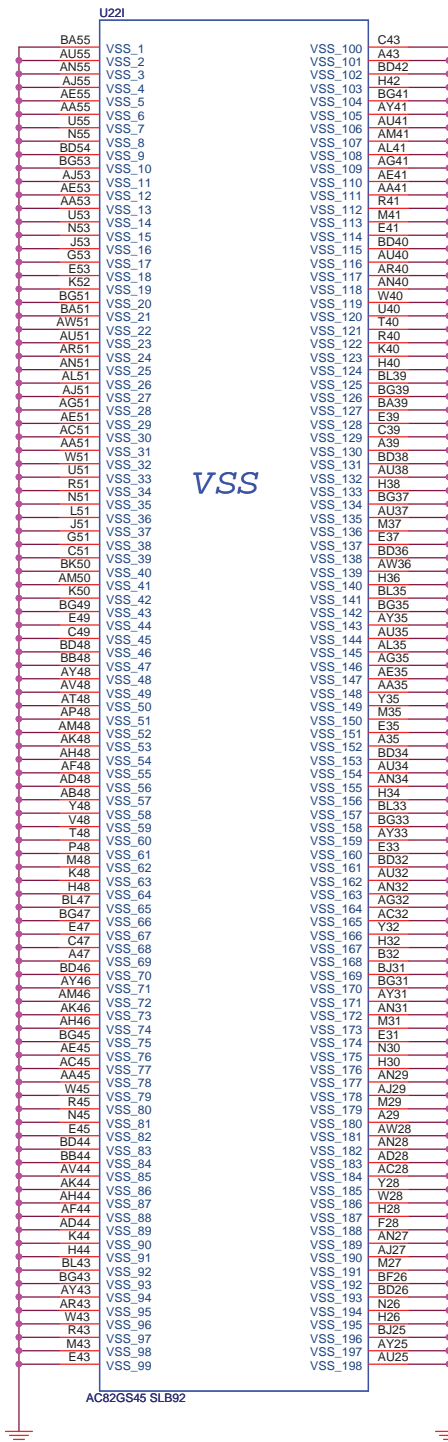

<http://laptop-motherboard-schematic.blogspot.com/>


PROJECT : FP7
Quanta Computer Inc.

Size Custom Document Number
NB5 Cantiga (Vcc)
Date: Thursday, May 21, 2009 Sheet 9 of 34 Rev 1A



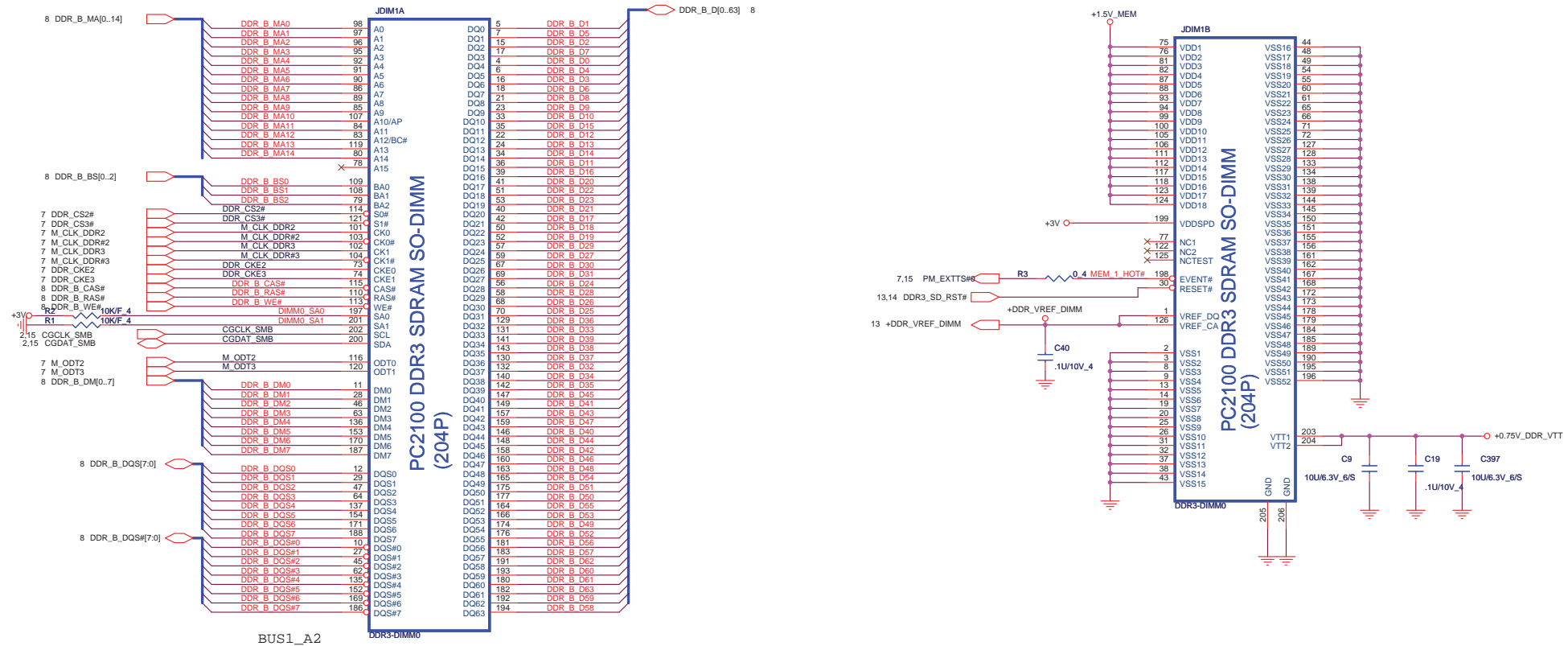
Size Custom	Document Number Cantiga (Power)	Rev 1A
Date: Thursday, May 21, 2009		Sheet 10 of 34



NB5

PROJECT : FP7
Quanta Computer Inc.

Size Custom	Document Number Cantiga (Vss)	Rev 1A
Date: Thursday, May 21, 2009	Sheet 11 of 34	

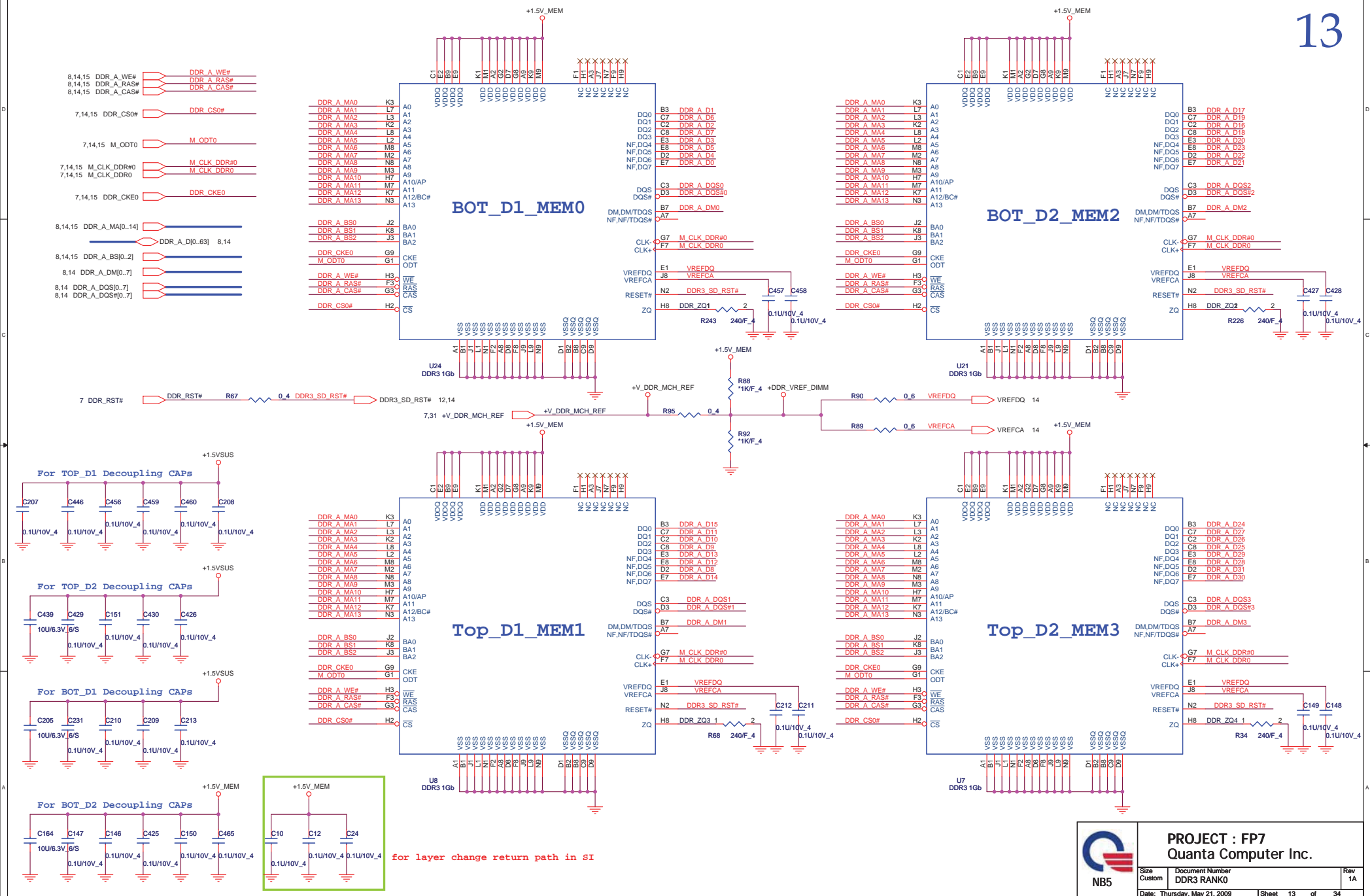


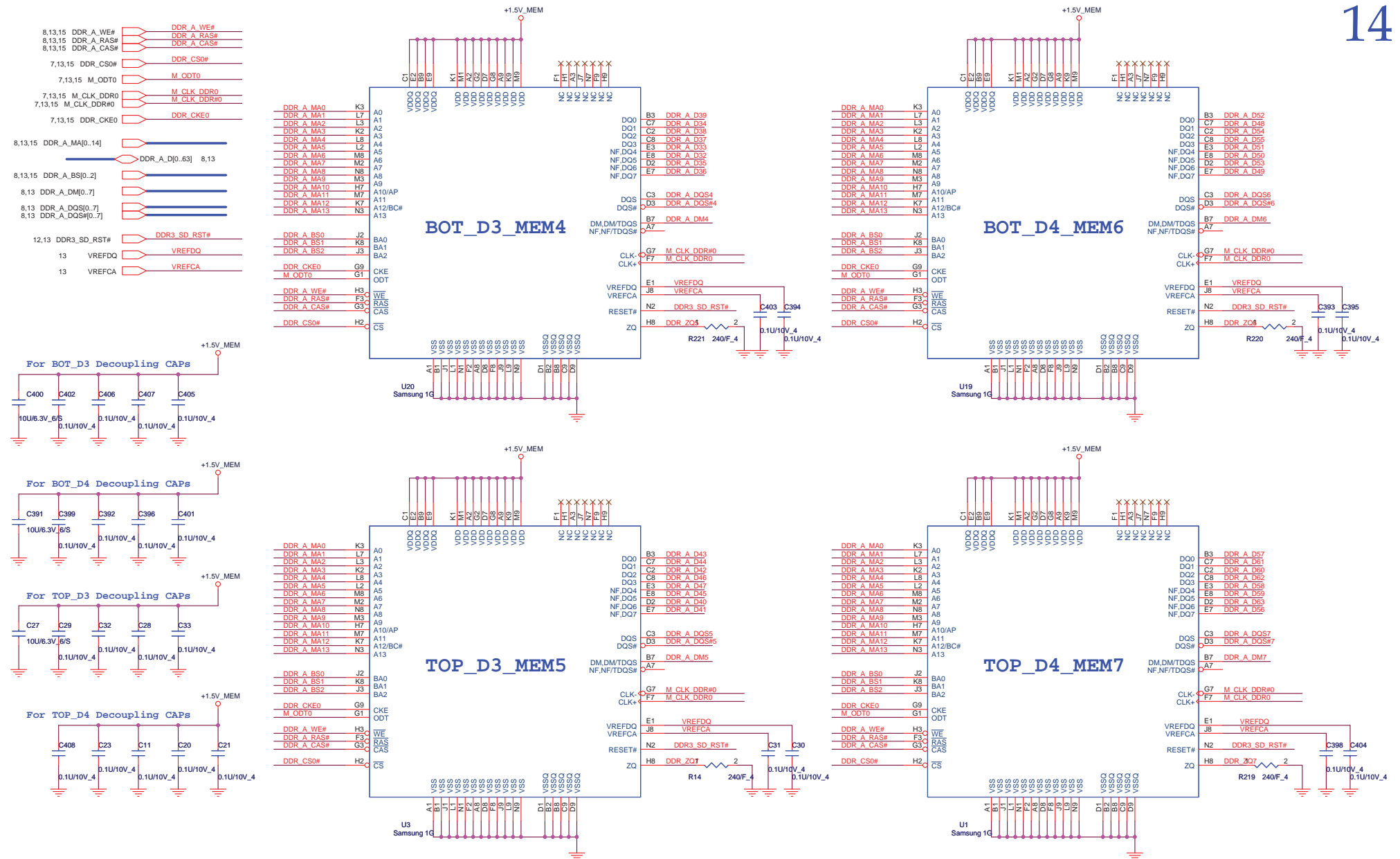
MEM delay circuit deleted by
DG-03328-001-V15

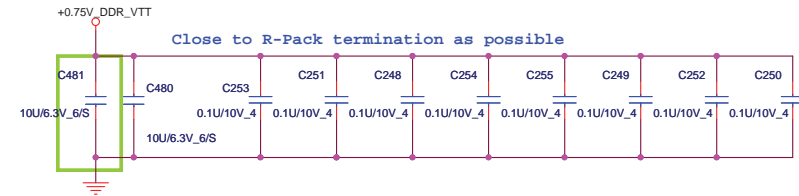
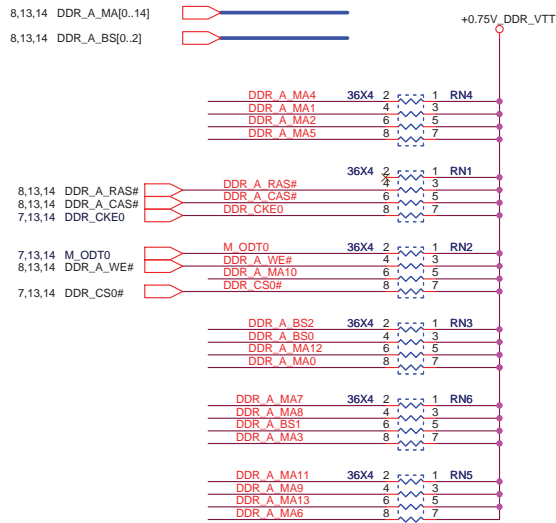


PROJECT : FP7
Quanta Computer Inc.

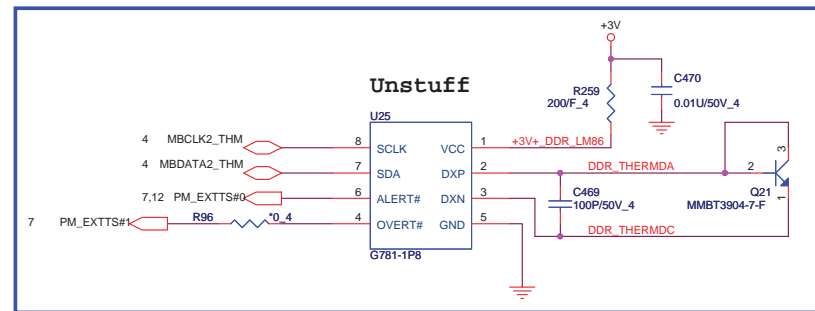
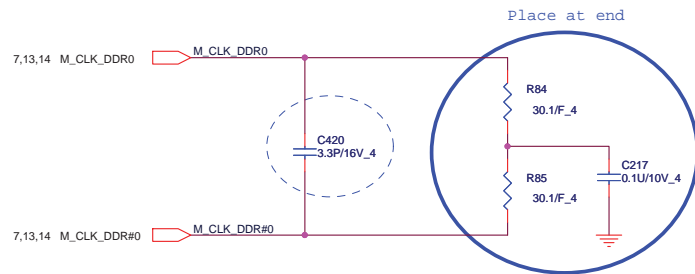
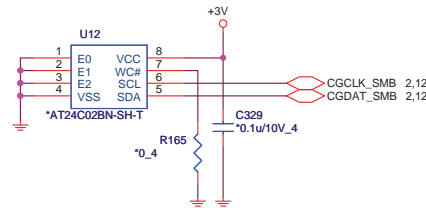
Size Custom	Document Number DDR3 SO-DIMM(200P)	Rev 1A
Date: Thursday, May 21, 2009		Sheet 12 of 34



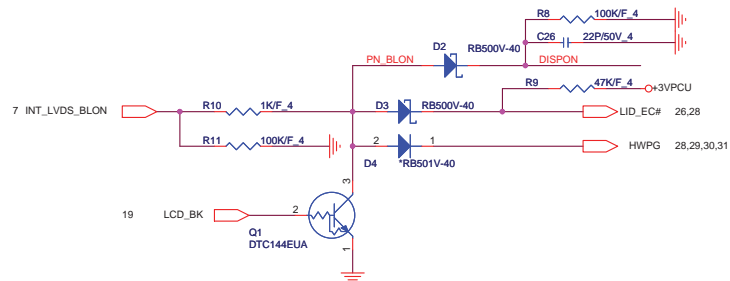




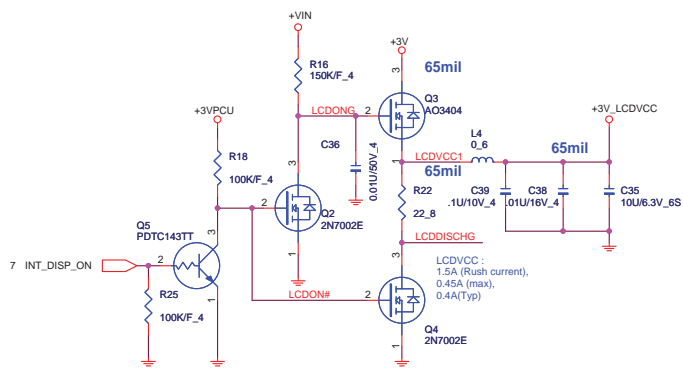
change C434 footprint to 0603



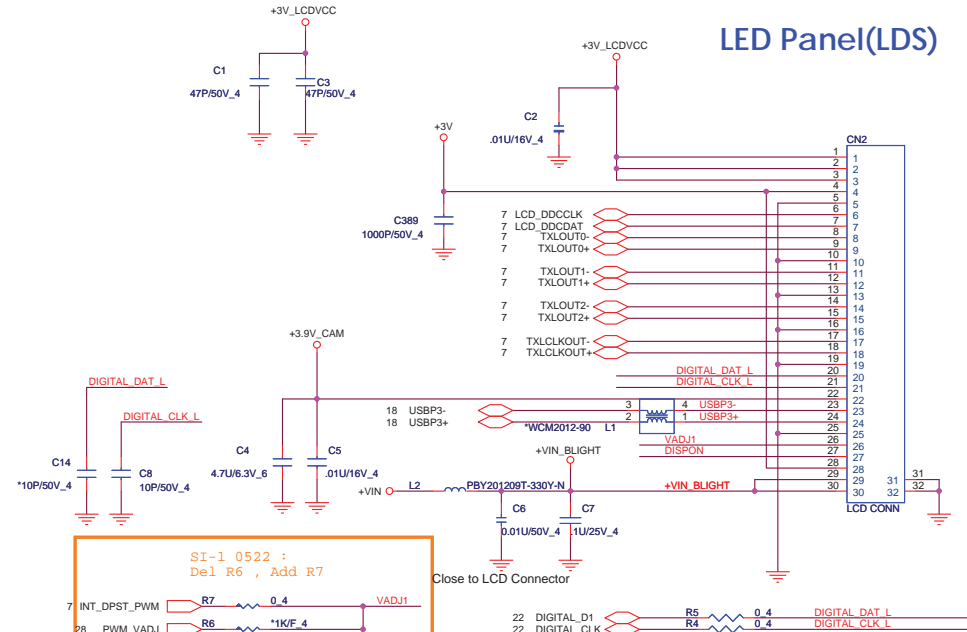
Backlight Control(LDS)



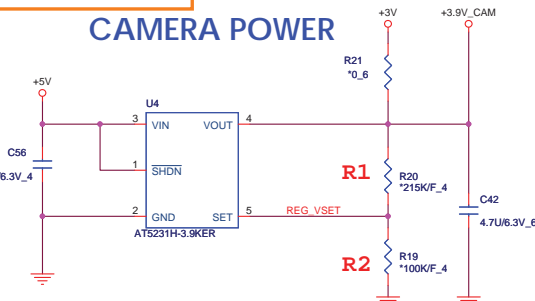
LCD POWER SWITCH




Request by HP RF(47Px2)

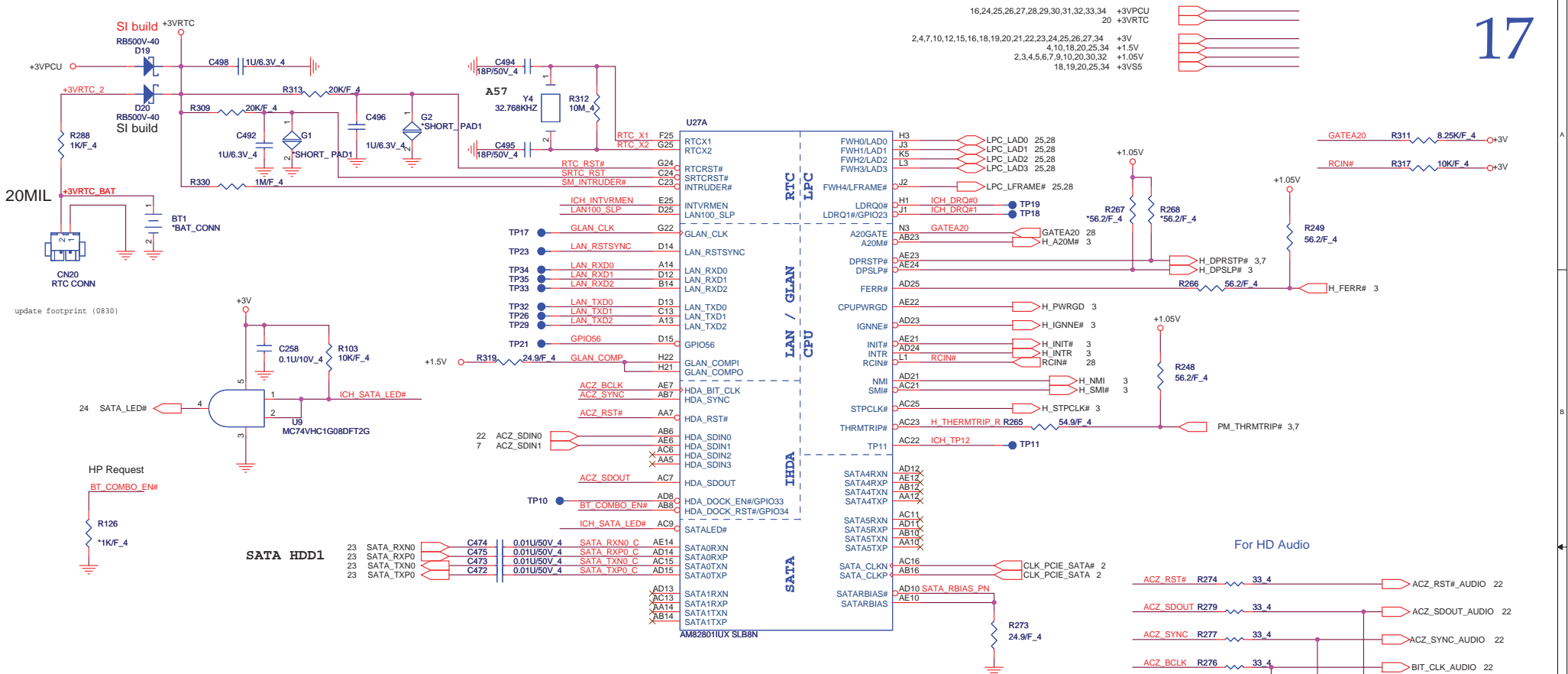


CAMERA POWER



$$V_{out} = 1.25(1 + R1/R2)$$

		PROJECT : FP7	
		Quanta Computer Inc.	
Size	Document Number	LED Panel / Camera	
Custom	LED Panel / Camera		
Date: Monday, May 25, 2009	Sheet 16 of 34	Rev 1A	



SB Strap

SB Strap

ICH9-M Internal VR Enable strap
(Internal VR for VccSus1_05, VccSus1_5 and VccCL1_5)

ICH9-M LAN100_SLP Strap
(Internal VR for VccLAN1_05 and VccCL1_05)

INTVRMEN

Low = Internal VR disable
High = Internal VR enable(Default)

LAN100_SLP

Low = Internal VR disable
High = Internal VR enable(Default)

XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIE port config bit 1

ICH9 Boot BIOS select

STRAP	PCI_GNT0#	SPL_CS#1
SPI	0	1
PCI	1	0
LPC	1	1

(default)

A16 swap override strap

PCI_GNT#3	Low = A16 swap override enabled Hi = Default

No Reboot Strap

ACZ_SPKR	Low: Default Hi: No reboot

TPM physical presence

ICH_GPIO57	Low: Default

Size Custom

Document Number

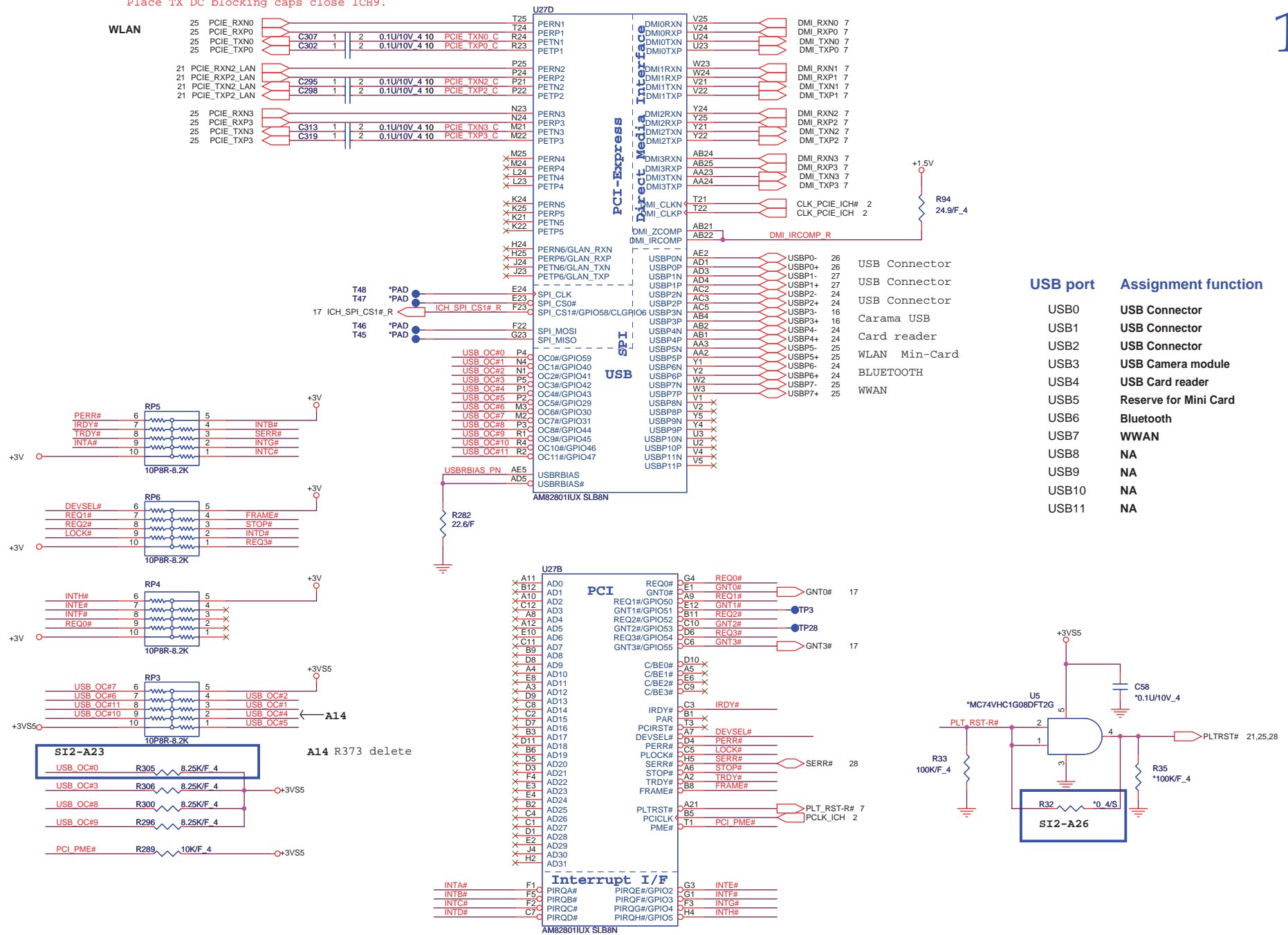
ICH9 (SATA/CPU)

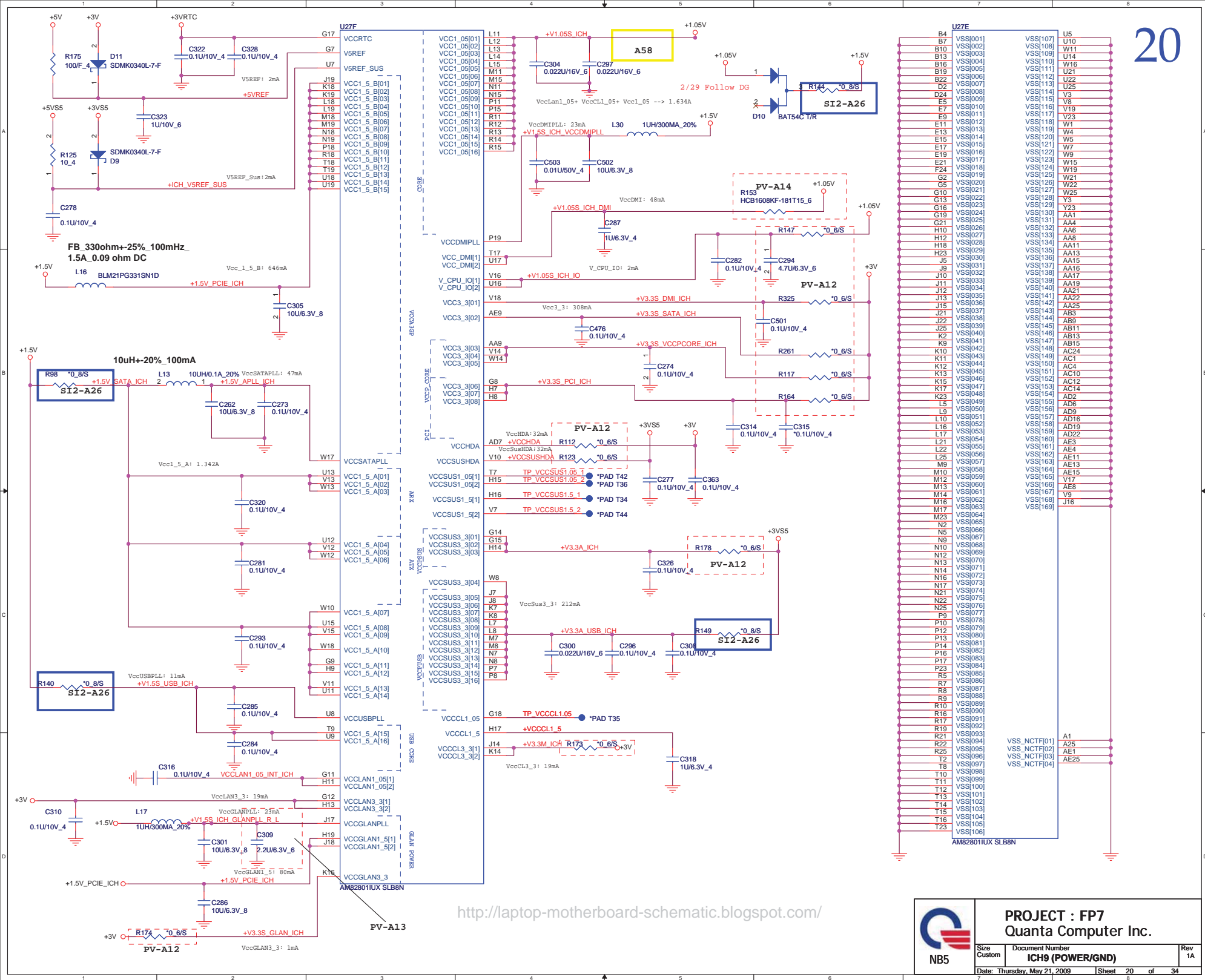
Date: Thursday, May 21, 2009

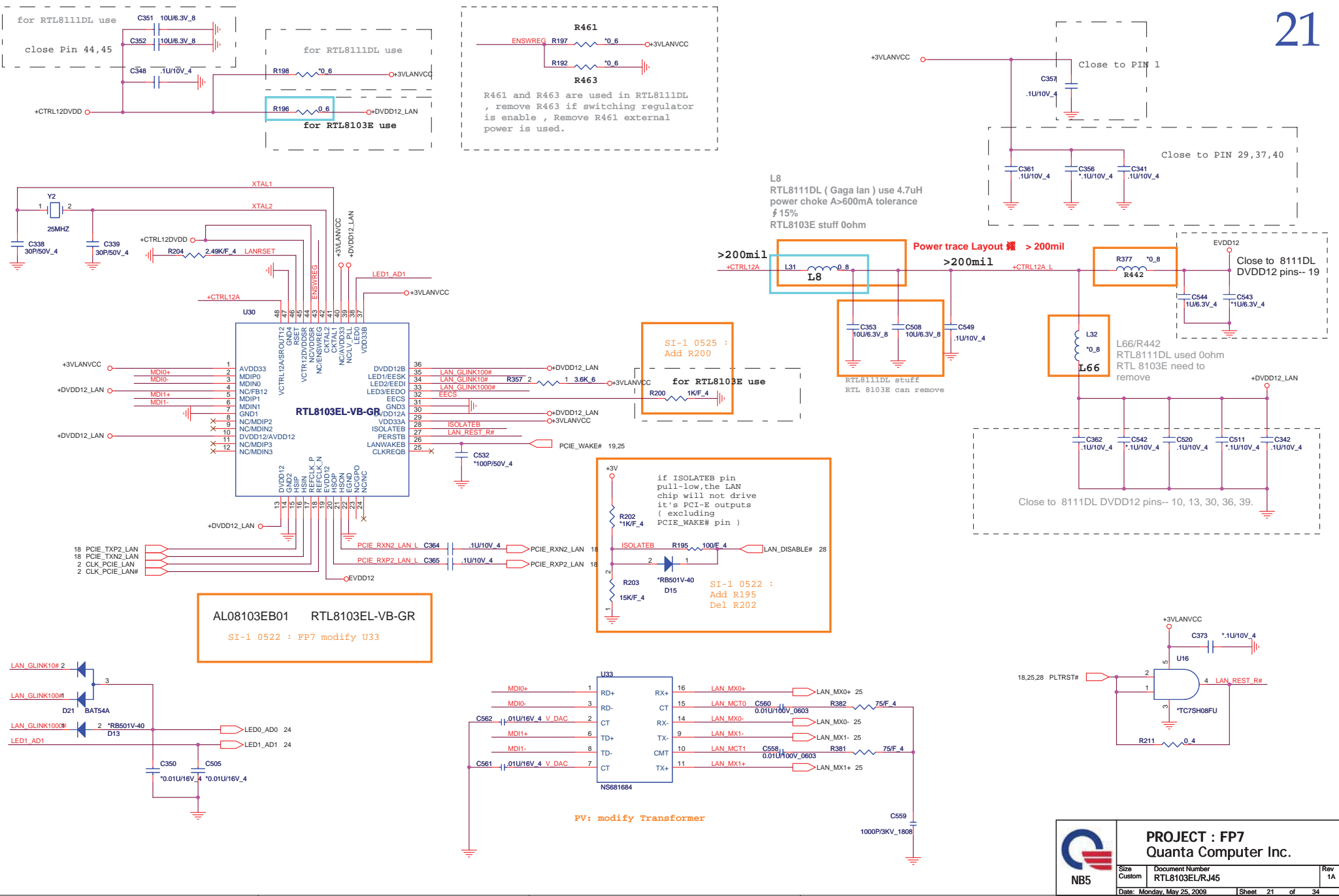
Sheet 17 of 34

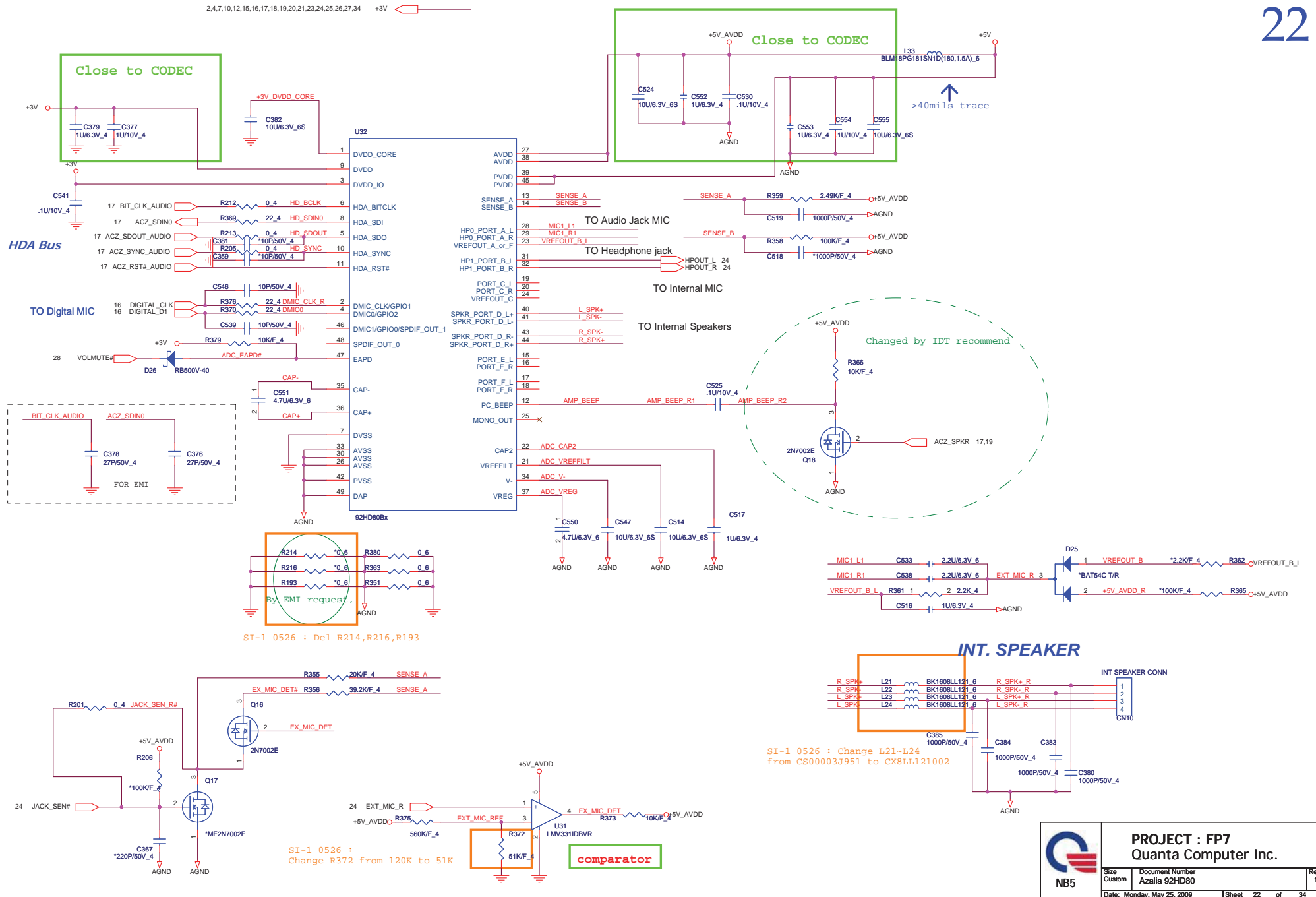
Rev 1A

Place TX DC blocking caps close ICH9.

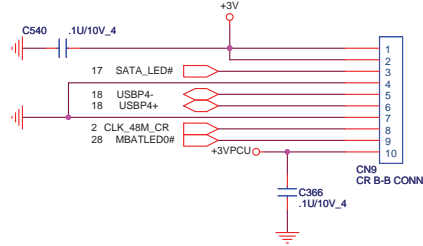




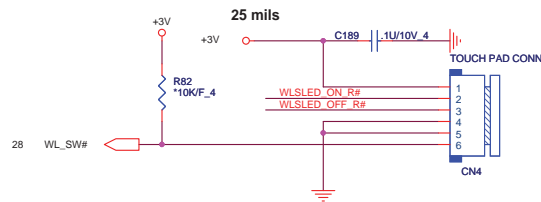




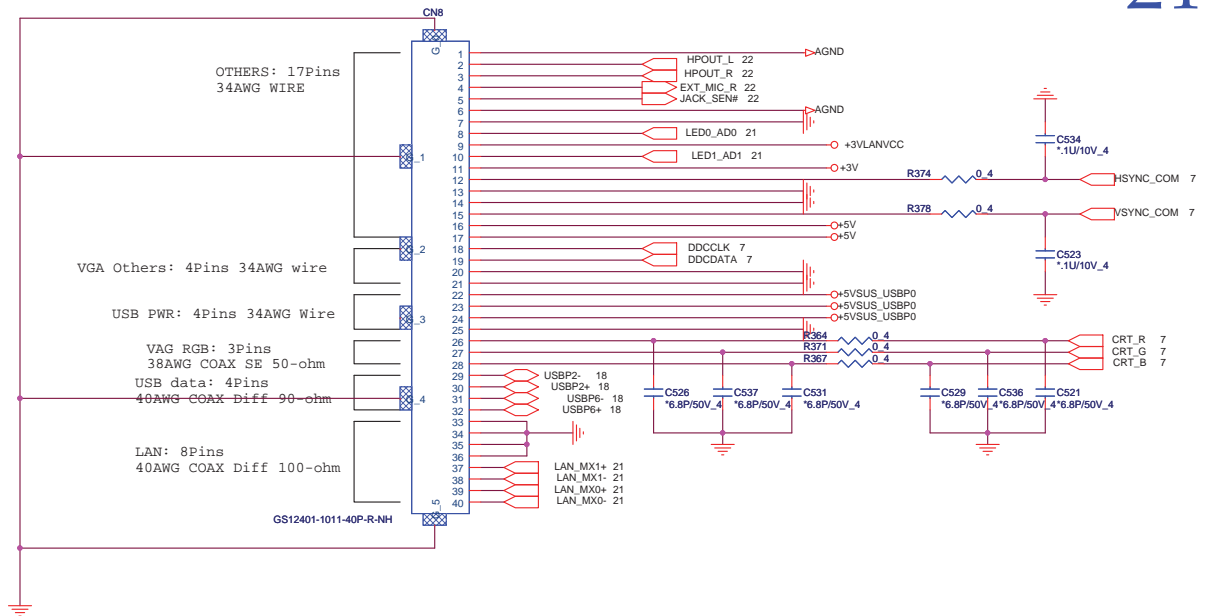
CardReader CONN.



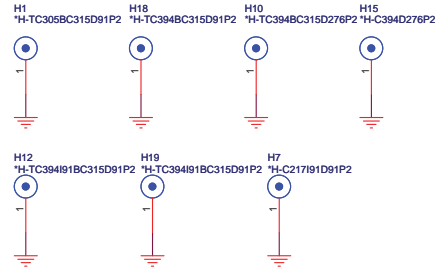
WL CTRL CONN.



I/O Board CONN.



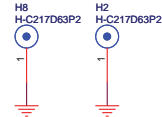
PCB Screws



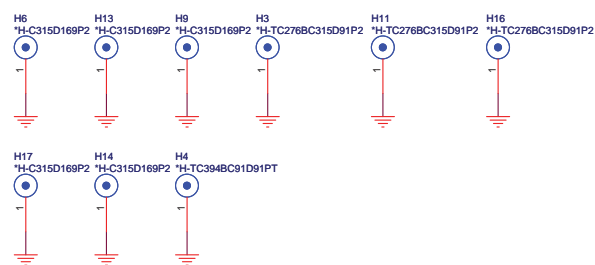
FAN Hole



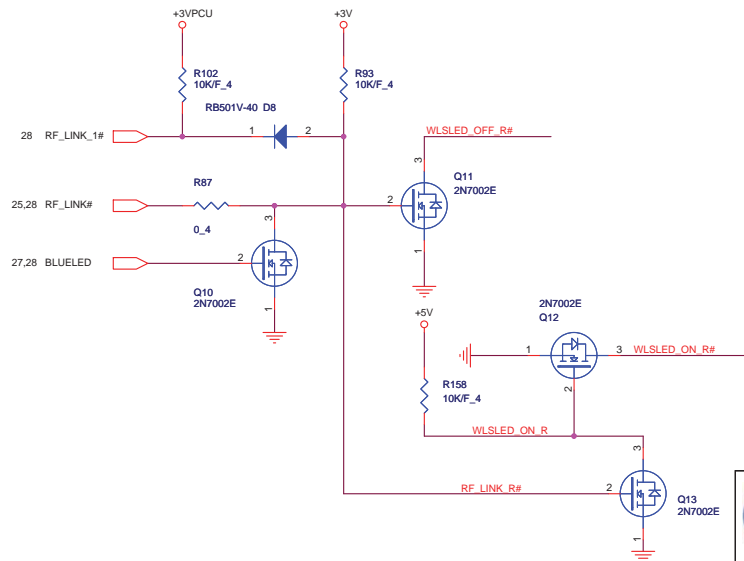
FAN SCREW HOLE




BRACKET

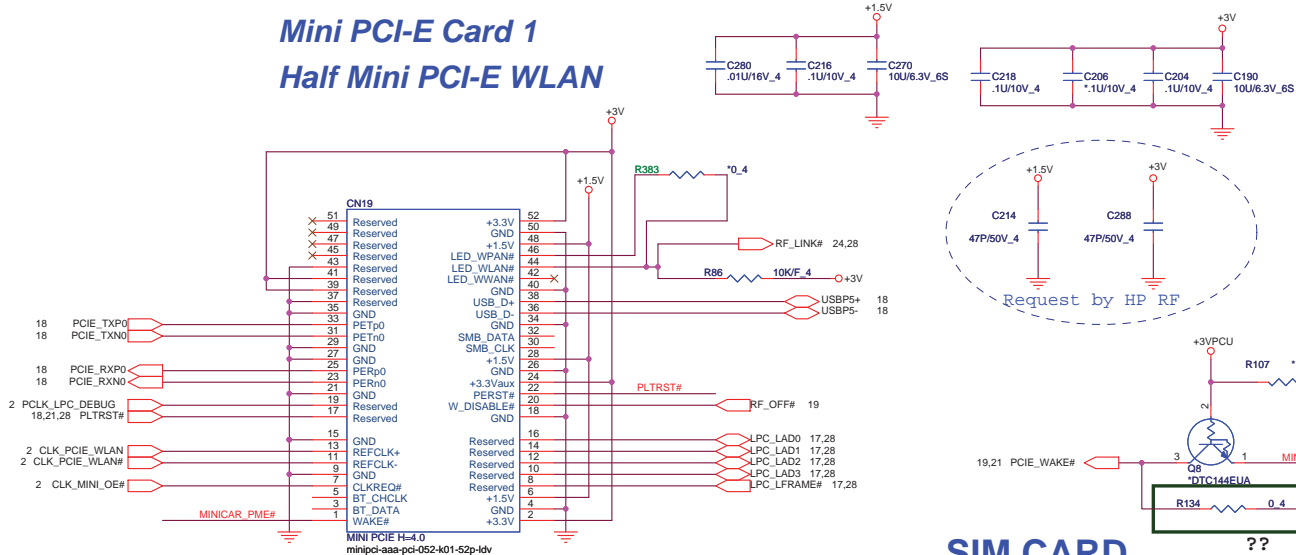


GND PAD



		PROJECT : FP7	
		Quanta Computer Inc.	
Size	Custom	Document Number	CR DB CONN
Date:	Thursday, May 21, 2009	Sheet	24 of 34
		Rev	1A

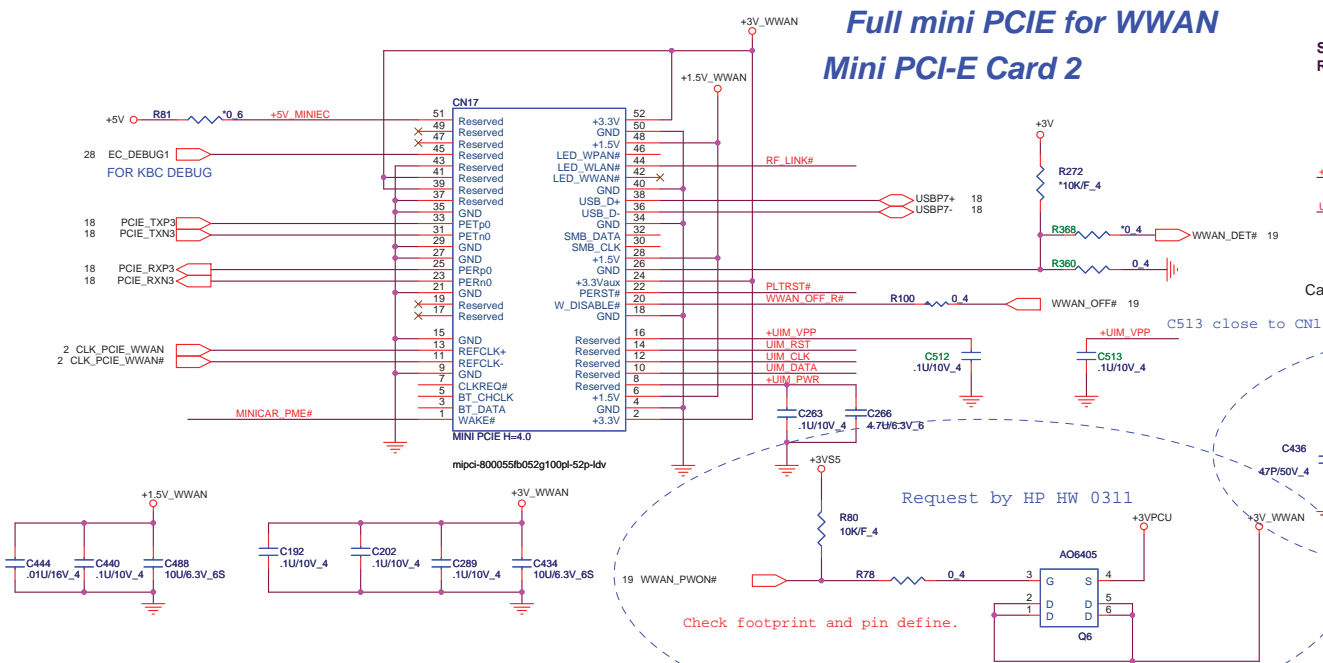
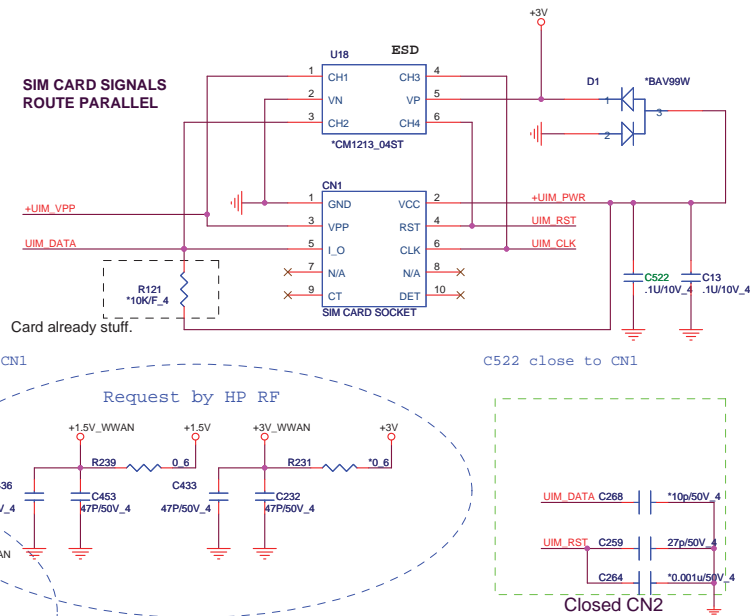
Mini PCI-E Card 1
Half Mini PCI-E WLAN



The value of the capacitor is suggest by Siemens HQ expert.
For against 900MHz RF interference. The value of capacitor is 27pF.
For against 1800MHz RF interference. The value of capacitor is 10pF.
1nF/10nF value capacitor use for against ESD purpose.

SIM CARD

Full mini PCIE for WWAN
Mini PCI-E Card 2

SIM CARD SIGNALS
ROUTE PARALLEL

Card already stuff.

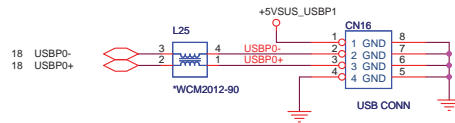
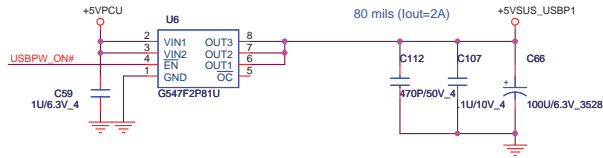
Request by HP RF



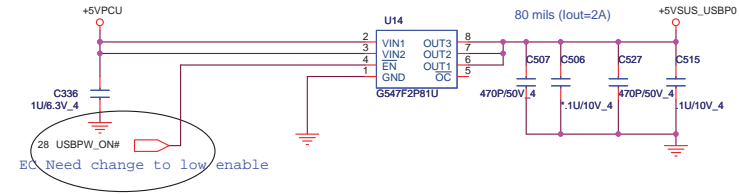
PROJECT : FP7
Quanta Computer Inc.

Size Custom	Document Number MINI PCIE (WLAN/WWAN)	Rev 1A
Date: Thursday, May 21, 2009		Sheet 25 of 34

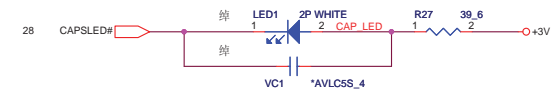
1x Left side USB PORT



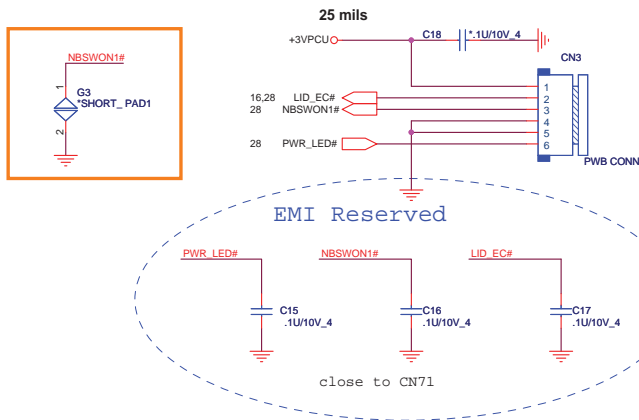
For Right 2xUSB Ports PWR



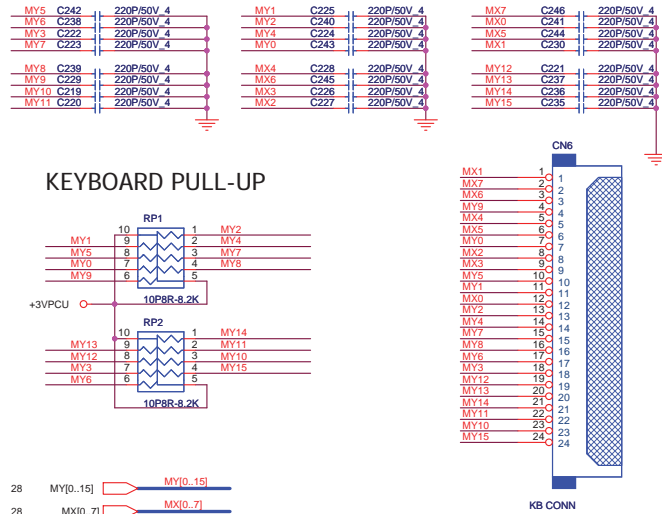
CAPS LEDs



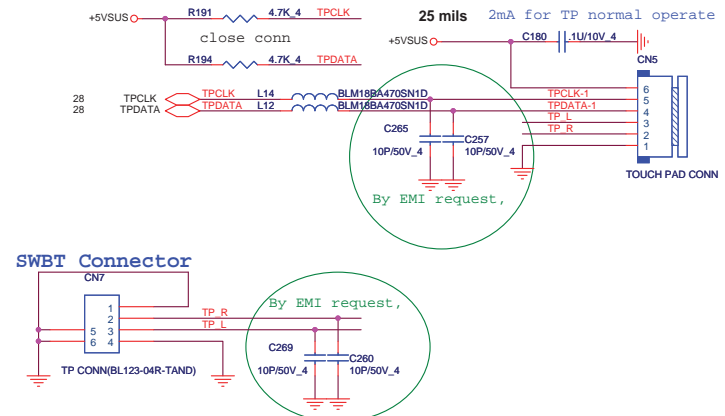
PWR BT CONN.



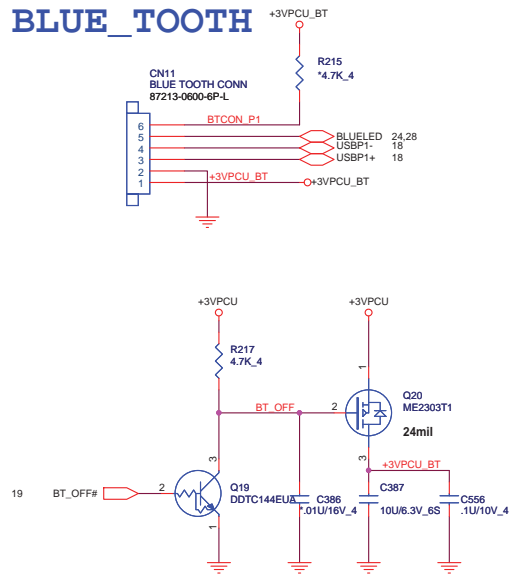
Keyboard (KBC)



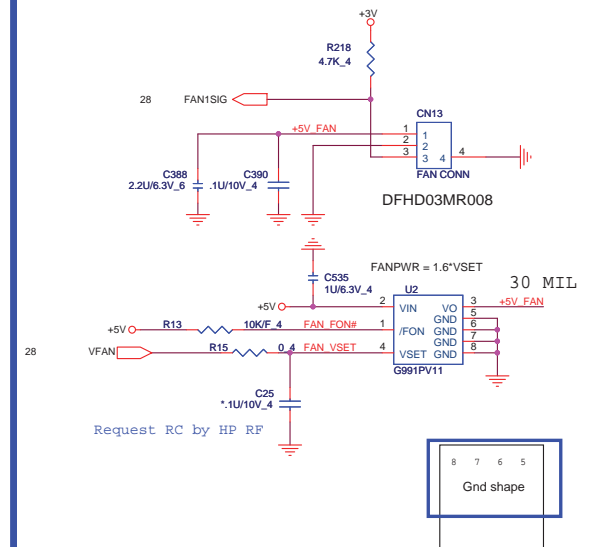
Touch Pad CONNECTOR(TBD)



BLUE_TOOTH



CPU FAN

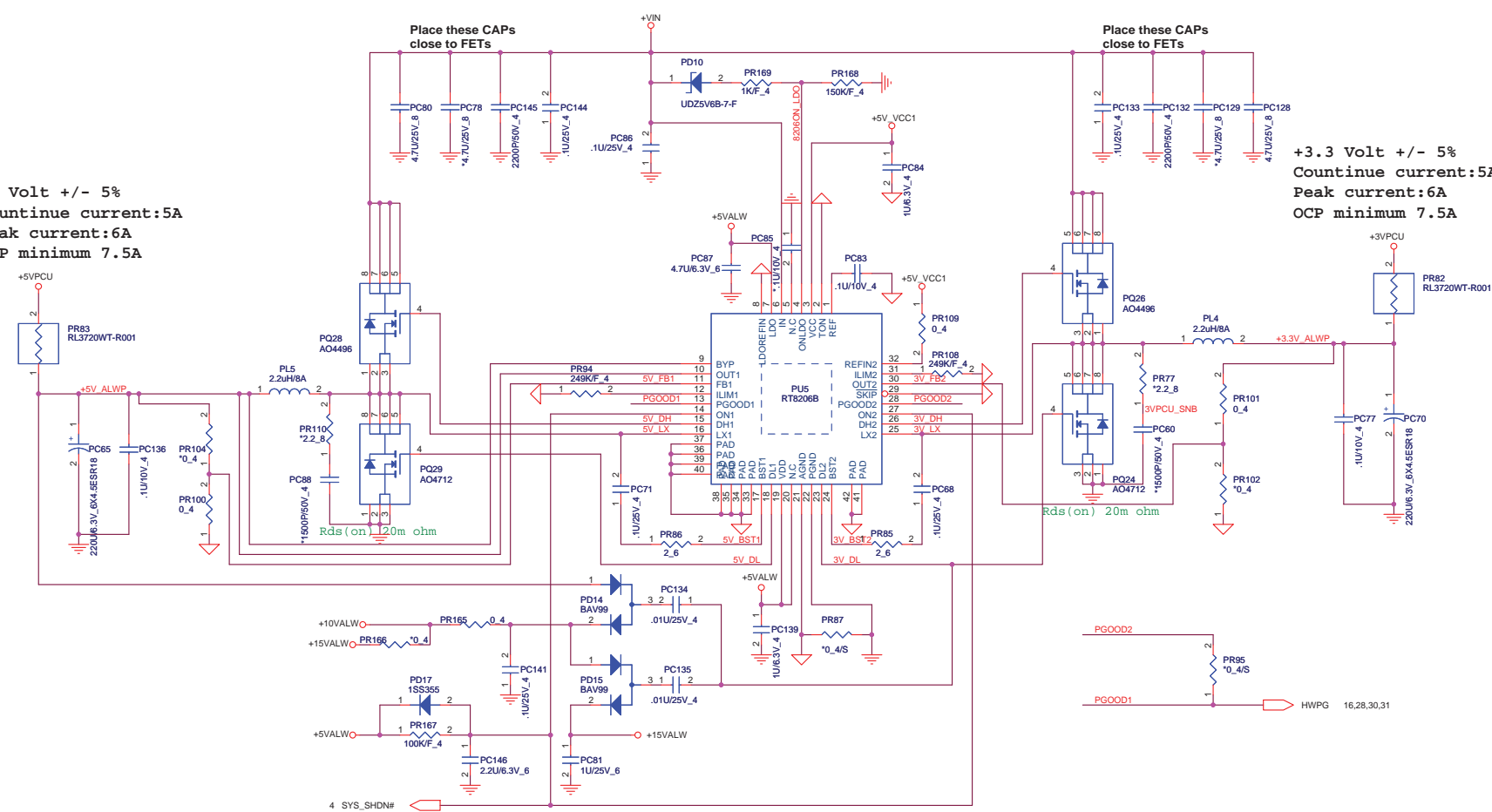


	PROJECT : FP7 Quanta Computer Inc.		
	Size Custom	Document Number KB/B7/TP/CPU FAN	Rev 1A
	Date: Thursday, May 21, 2009	Sheet 27 of 34	



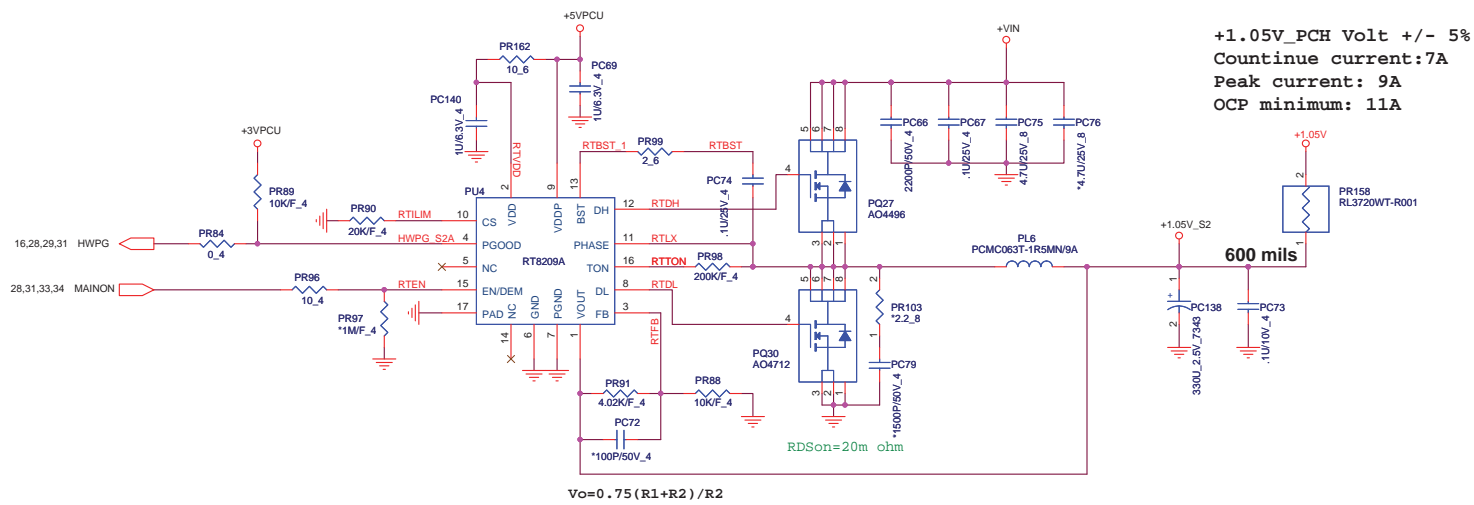
+5 Volt +/- 5%
Countinue current:5A
Peak current:6A
OCP minimum 7.5A

+3.3 Volt +/- 5%
Countinue current:5A
Peak current:6A
OCP minimum 7.5A



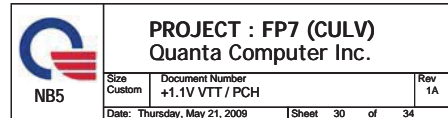
PROJECT : FP7 (CULV)
Quanta Computer Inc.

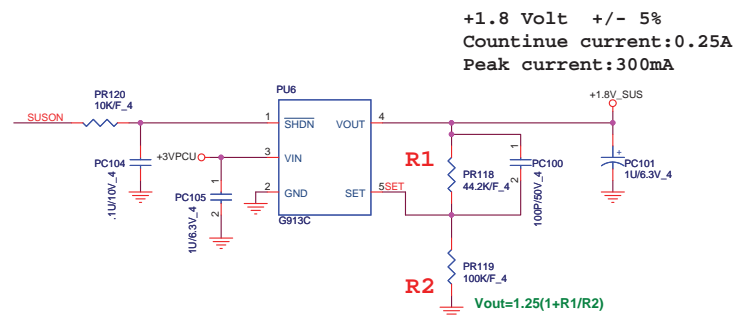
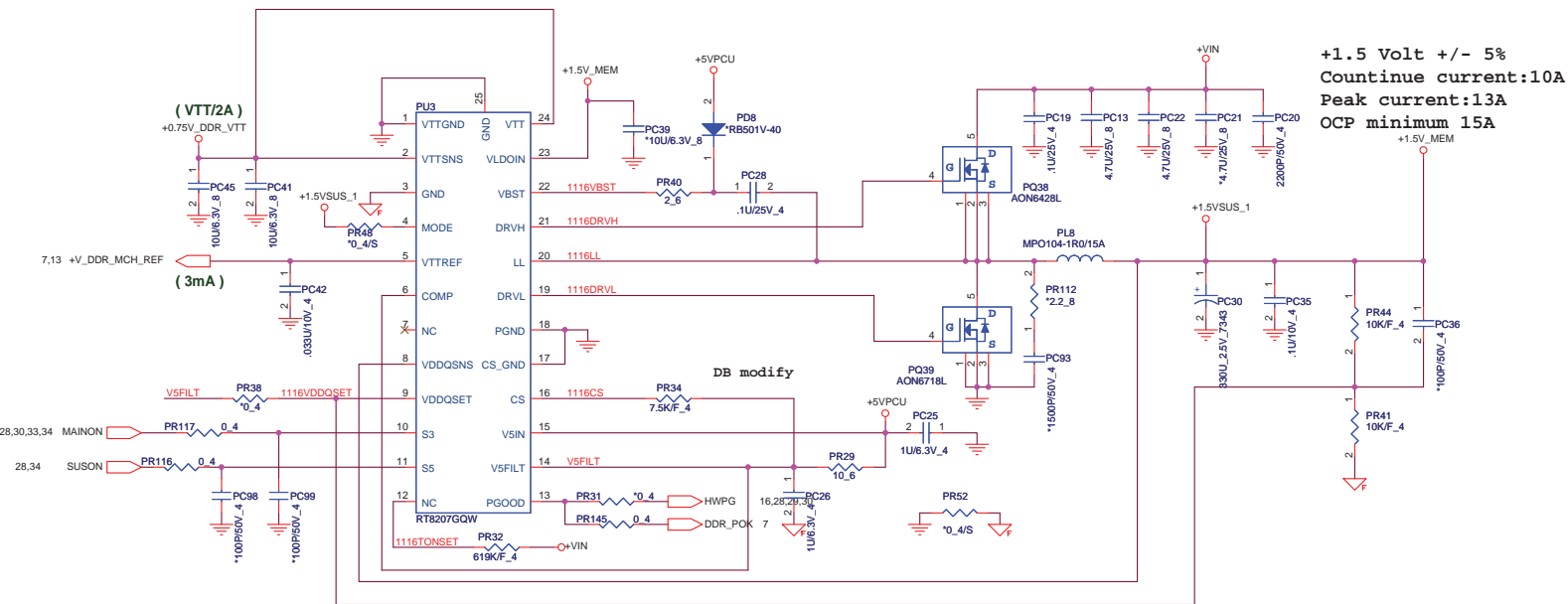
Size Custom	Document Number +5V/+3V (RT8206B)	Rev 1A
Date: Thursday, May 21, 2009 Sheet 29 of 34		




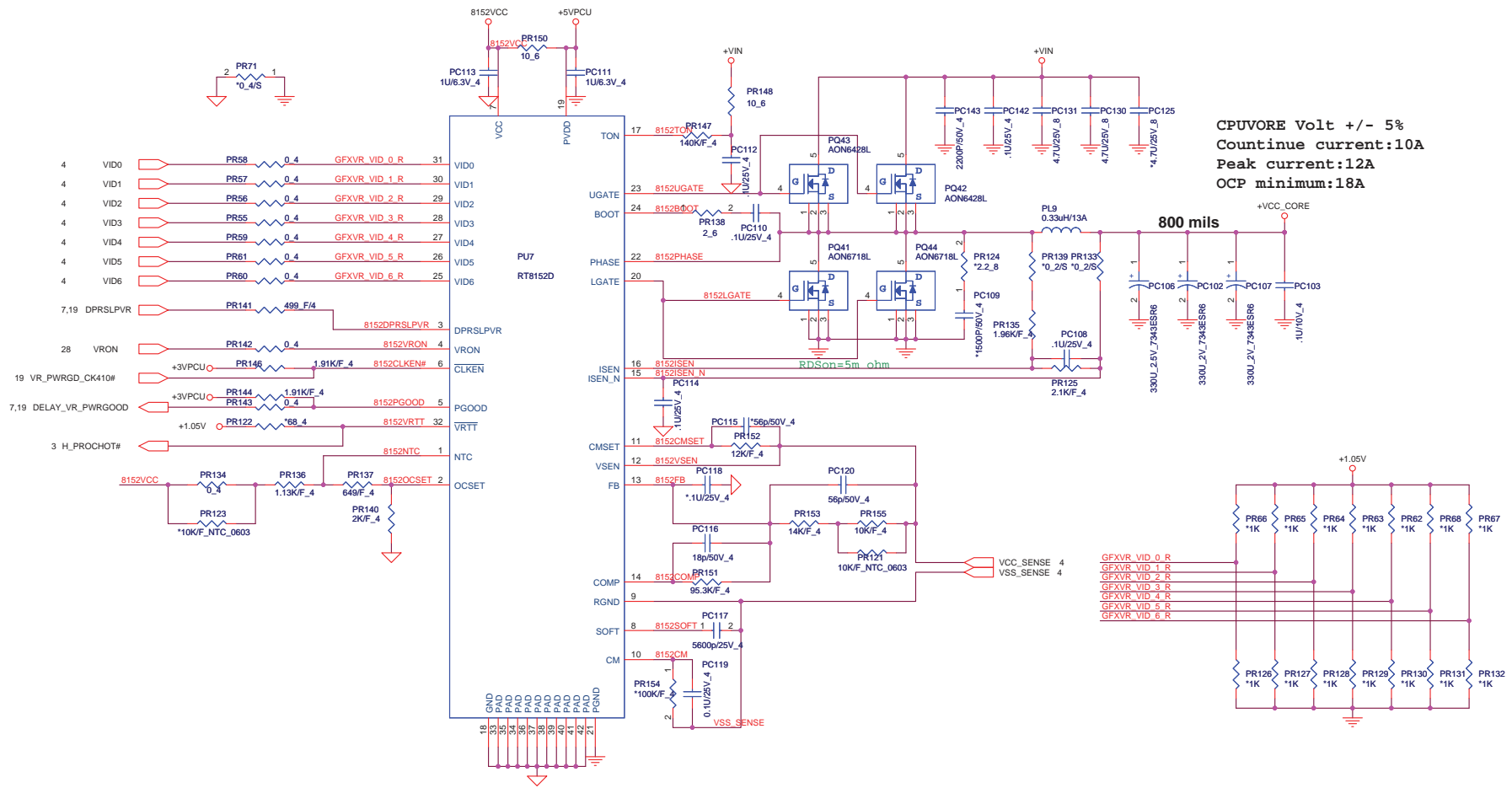
```
+1.05V_PCH Volt +/- 5%
Countinue current:7A
Peak current: 9A
OCP minimum: 11A
```

$$V_o = 0.75(R_1 + R_2) / R_2$$





	PROJECT : FP7 (CULV) Quanta Computer Inc.		
	Size Custom	Document Number DDR3 (RT8207)	Rev 1A
	Date: Thursday, May 21, 2009	Sheet 31 of 34	

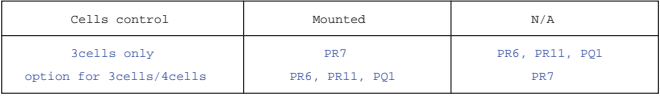


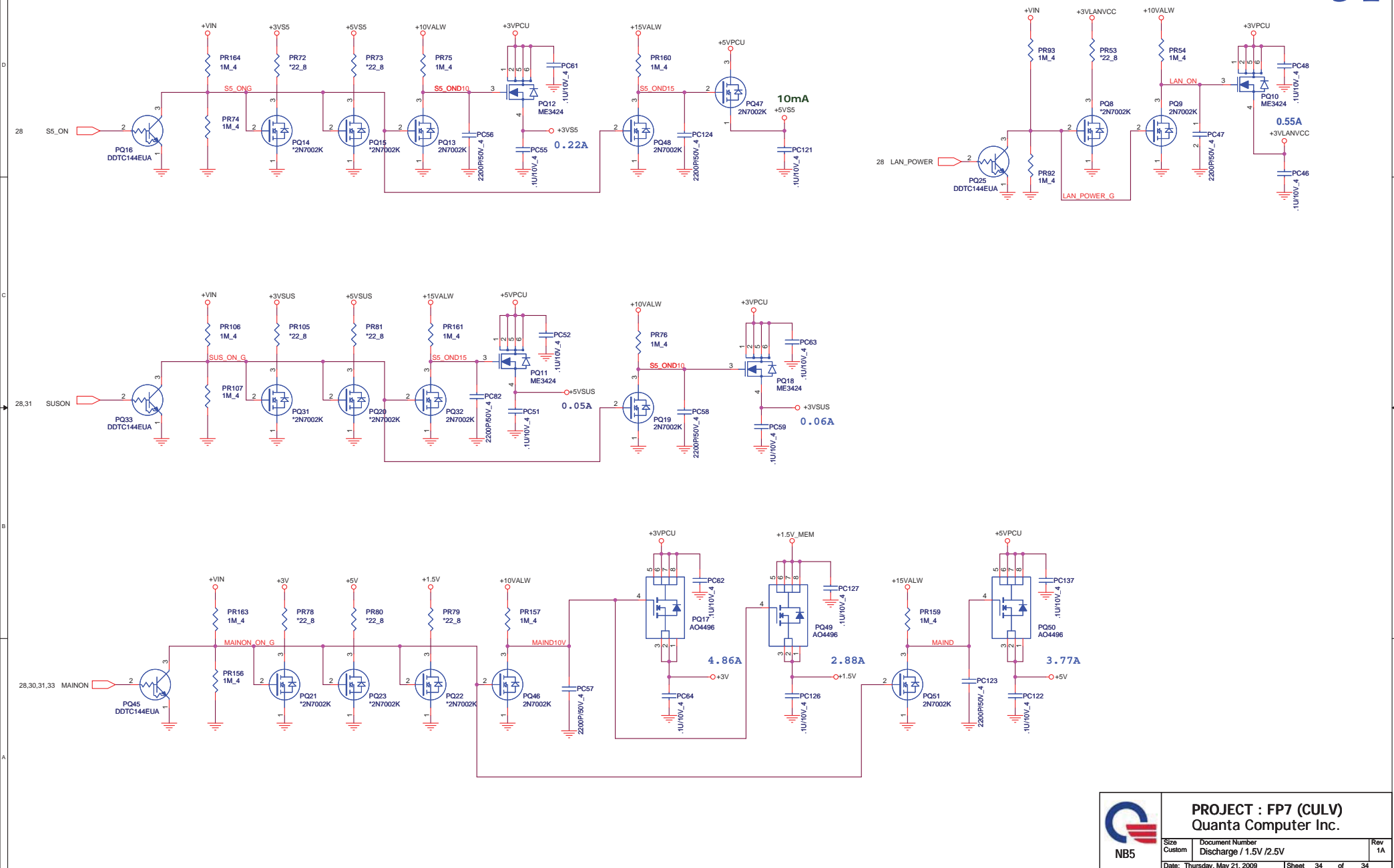
CPU TYPE	PL9	PC102	PC107	PR135	PR125	PR151	PR140	PR137	PR136	PQ43, PQ44
LV	0.33uH_DC+33K0M000	ESR6_CH733RM8831	ESR6_CH733RM8831	1.96K_CS21962FB08	2.1K_CS22102FB12	95.3K_CS39532FB03	2K_CS22002FB19	649_CS16492FB13	1.13K_CS21132FB13	POP
CULV	0.82uH_DC+82D0M000	ESR9_CH733RY8802	NA	2.49K_CS22492FB22	2.49K_CS22492FB22	191K_CS41912FB17	1.5K_CS21502FB14	330_CS13302FB11	715_CS17152FB17	NA




PROJECT : FP7 (CULV)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VCore (RT8152A)	1A
Date: Thursday, May 21, 2009	Sheet 32 of 34	





		PROJECT : FP7 (CULV)	
		Quanta Computer Inc.	
Size	Custom	Document Number	Discharge / 1.5V / 2.5V
Date:	Thursday, May 21, 2009	Sheet	34 of 34
Rev		1A	