

Compal Confidential

Buffalo 10BL

LA-5122P Schematics Document

Intel Pine View Processor/ Tiger point

2010-03-30

REV: 1.0

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Model Name : PAV10

File Name : LA-5122P

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PCIeMini Card
WLAN
PCIe port 6
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USB
5V 480MHz

PCIe 1x [2,4]
1.5V 2.5GHz(250MB/s)

PCIe 1x
1.5V 2.5GHz(250MB/s)

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HD Audio
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MIC CONN
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Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.89VS	0.89VS GFX support voltage	ON	OFF	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	VCCP switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.5V	1.5V power rail for DDR	ON	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
+3V_SB	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_WLAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	ON	OFF	OFF
+5VALW	5V always on power rail	ON	OFF	ON	OFF
+5V_SB	5V power rail for SB	ON	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF	ON
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BTO Option Table

Function	Mini PCI-E SLOT				CAMERA & MIC		BLUE TOOTH	STAR	shor 0 ohm
description									
explain	Wi-Fi	WiMax	3GGPS	3G	CAMERA	MIC	BLUE TOOTH	POWER SAVING	0 ohm no pop
BTO	WLAN@	WIMAX@	3GGPS@	3G@	CAM@	MIC@	BT@	STAR@	MP@

Function	CPU		
description			
explain	MP CPU		
BTO	MP_455@		

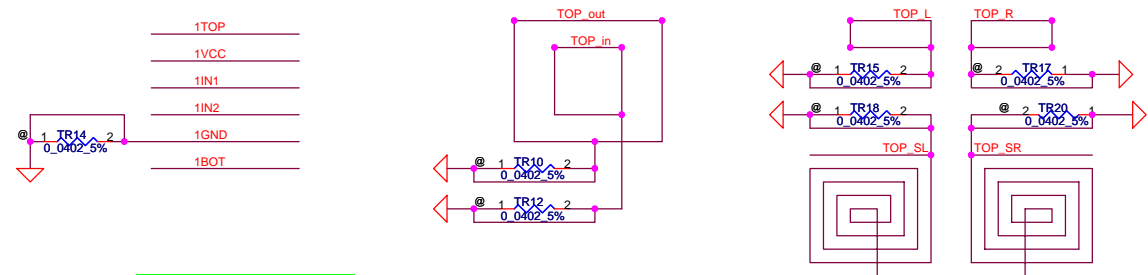
EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	EMC1402	1001 010X b

EC SM Bus2 address

ICH7M SM Bus address

Device	Address
Clock Generator (SLG8SP56VTR)	1101 001Xb
DDR DIMMA	1010 000Xb



3/23~3/30 Before PVT SMT

4/13~4/21 after PVT SMT

4/16 Short PAD

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Buffalo Power Map

Ipeak=5A, Imax=3.5A, Iocp min=5.2A

DESIGN CURRENT 508mA

+3VALWP +-5%

** The SW just is reserved.
The power passes by jump or
0-ohm resistor.

SBPWR_EN#

** SI3456BDV

DESIGN CURRENT 45mA

+3V_SB

WOL_EN#

** P-CHANNEL
AO-3413

DESIGN CURRENT 3010mA

+3V_LAN

Ipeak=5A, Imax=3.5A, Iocp min=5.08A

+5VALWP +-5%

SBPWR_EN#

** 2N7002DW

DESIGN CURRENT 10mA

+5V_SB

SUSP

N-CHANNEL

SI4800

DESIGN CURRENT 2851mA

+5VS

SUSP

N-CHANNEL

SI4800

DESIGN CURRENT 9314mA

+3VS

ENVDD

P-CHANNEL
AO-3413

DESIGN CURRENT 450mA

+LCD_VDD

SUSP#

SY8033BDBC

DESIGN CURRENT 2600mA

+0.89VSP

SUSP#

TPS51117RGYR

Ipeak=6A, Imax=4.2A, Iocp min=7.18A

DESIGN CURRENT 7301mA

+1.05VSP +-5%

VR_ON

ISL6261ACRZ-T

DESIGN CURRENT 3127mA

+CPU_CORE

SYSON

RT8209BGQW

Ipeak=5A, Imax=3.5A, Iocp min=5.8A

DESIGN CURRENT 1720mA

+1.5VP +-5%

SUSP#

IREF8113PBF

DESIGN CURRENT 2500mA

+1.5VSP

SUSP

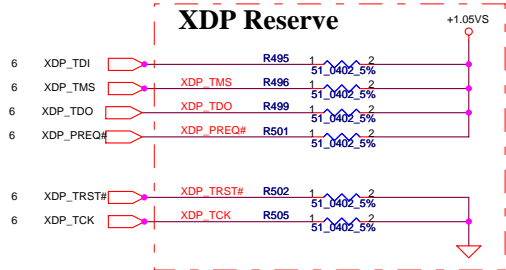
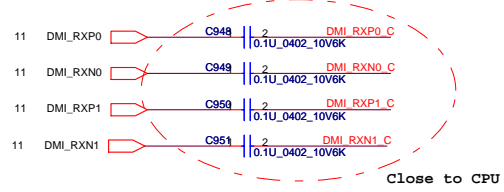
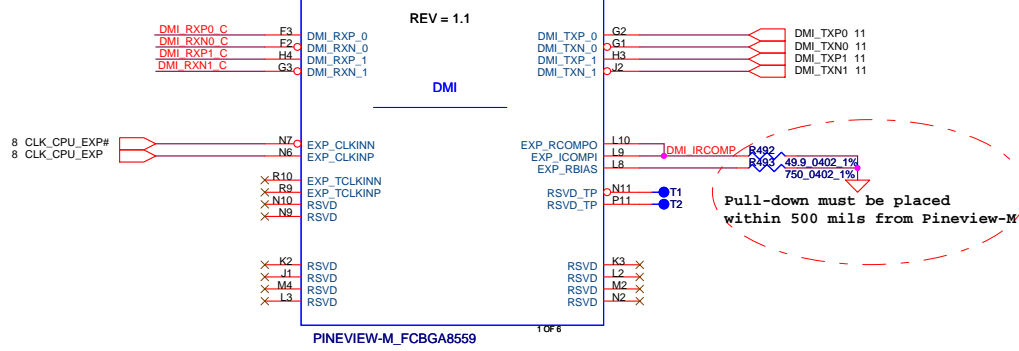
APL5331KAC

DESIGN CURRENT 900mA

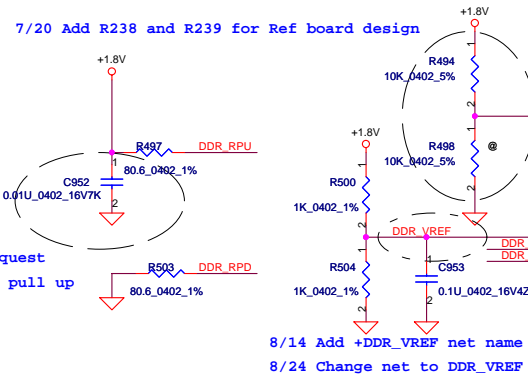
+0.75VSP

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4/23 U1 , CPU change p/n by Jordan command: SA00003WA00->SA00003WAA0



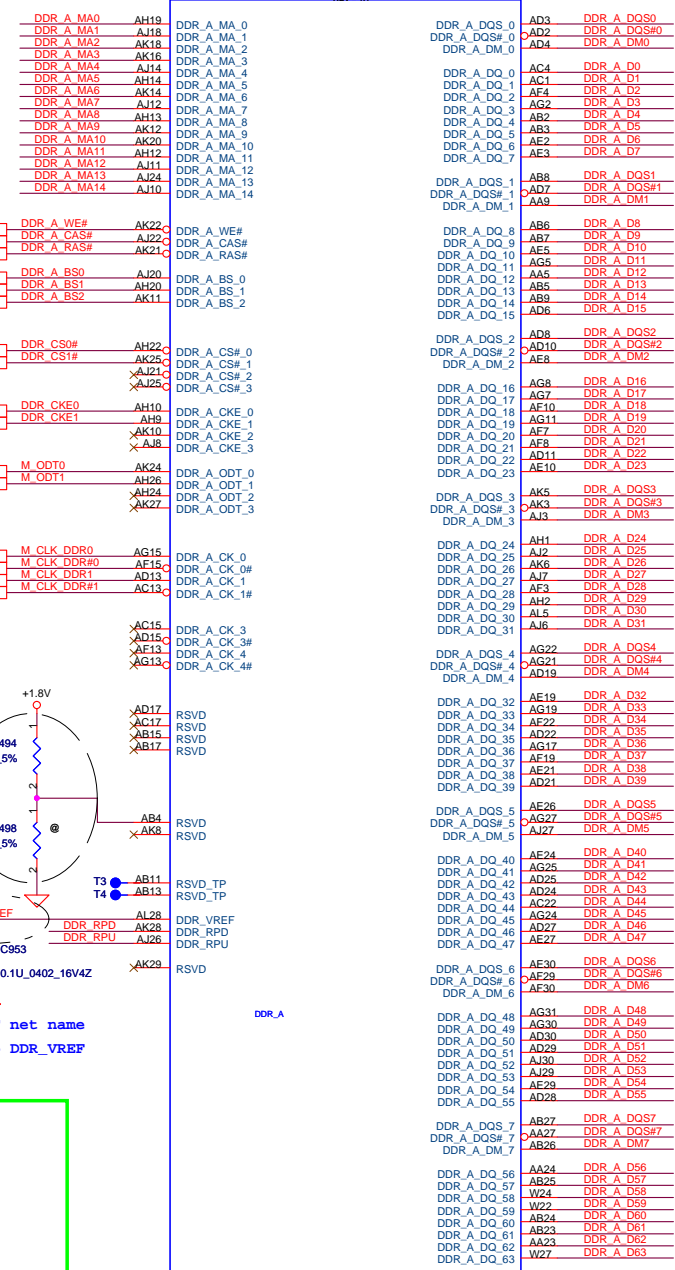
7/21 Add C302 to GND for Intel request
7/27 Change C302 to GND for +1.8V pull up

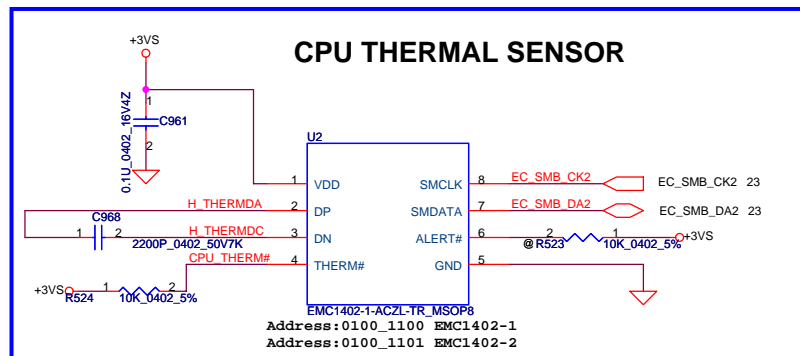
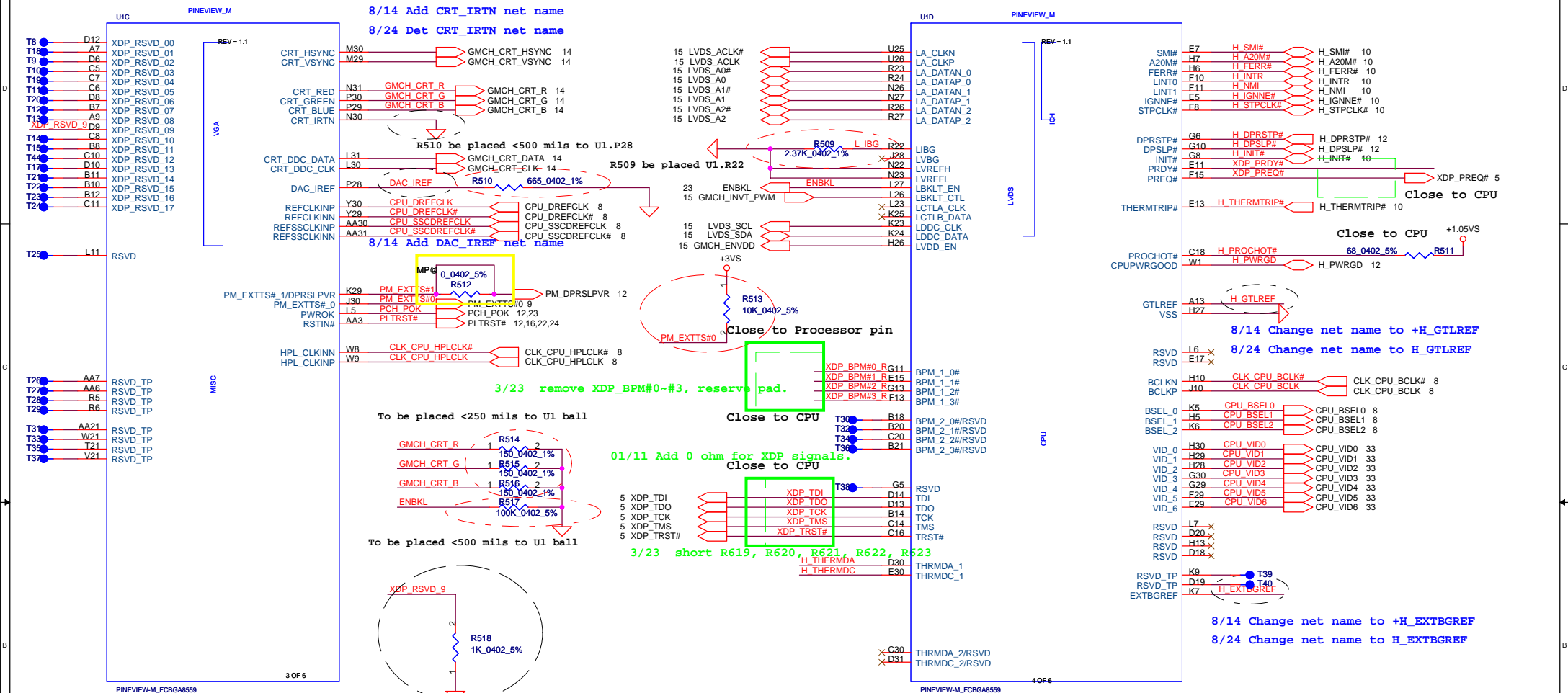


3/23 remove XDP connector
3/23 R506, R507, R508, JXDP1 removed

3/23 D45, D46 removed

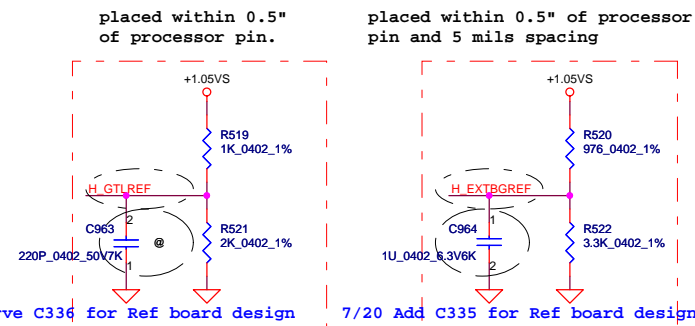
Place diff CPU side
10/19 Change footprint T5, T6 and T7 from TPC24 to TPC12





H_DPRSTP#	C954	1	②	220P_0402_50V7K
H_DPSLP#	C955	1	②	220P_0402_50V7K
H_PWRGD	C956	1	②	220P_0402_50V7K
H_A20M#	C957	1	②	220P_0402_50V7K
H_IGNNE#	C958	1	②	220P_0402_50V7K
H_INIT#	C959	1	②	220P_0402_50V7K
H_INTR	C960	1	②	220P_0402_50V7K
H_FERR#	C962	1	②	220P_0402_50V7K
H_NMI	C965	1	②	220P_0402_50V7K
H_SMI#	C966	1	②	220P_0402_50V7K
H_STPCLK#	C967	1	②	220P_0402_50V7K

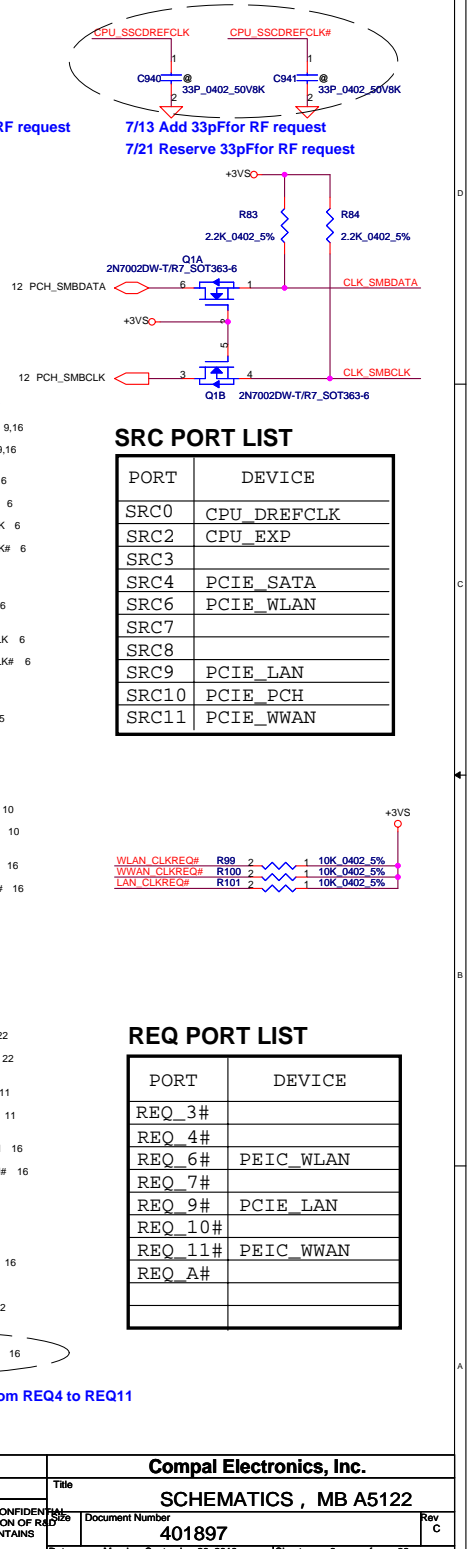
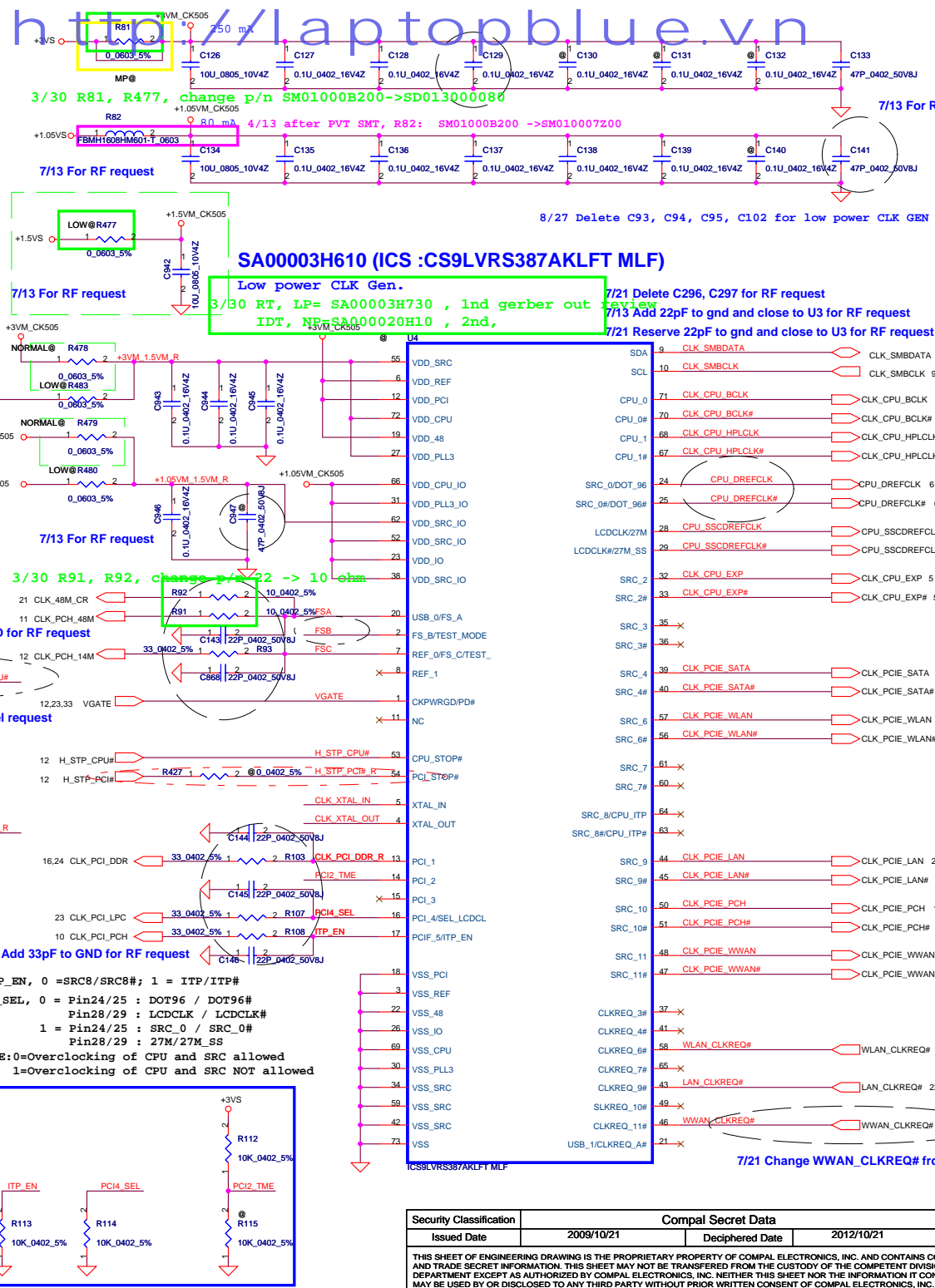
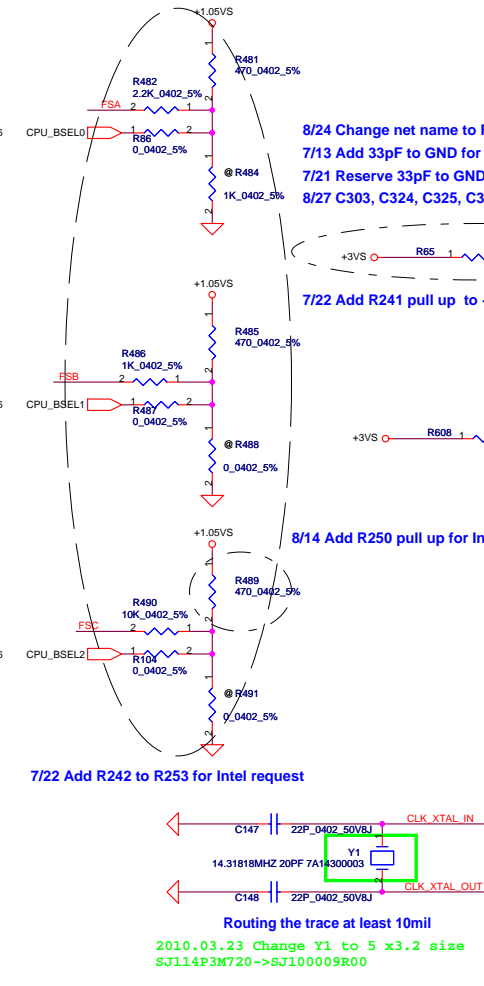
ESD request



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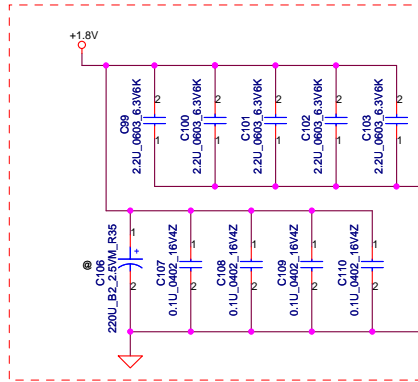
FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						
Reserved								

	Normal Power	Low Power
R477	@	Stuff
R478	Stuff	@
R479	Stuff	@
R480	@	Stuff
R483	@	Stuff

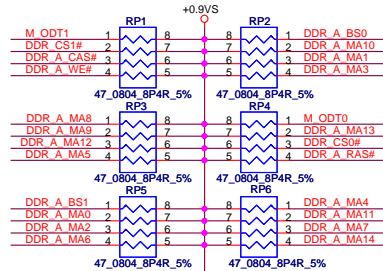
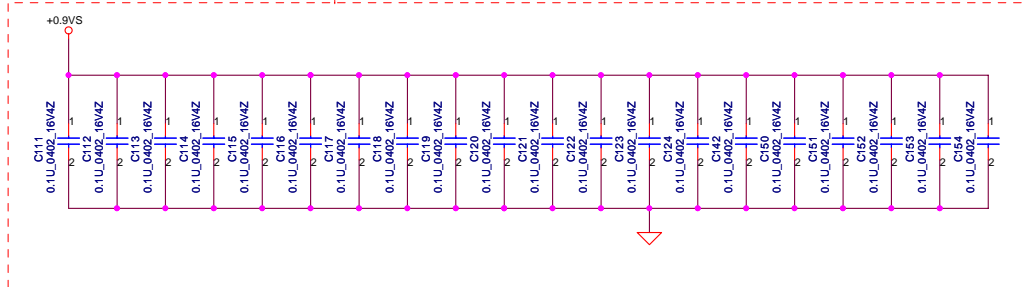


5 DDR_A_DQS#[0..7]
5 DDR_A_D[0..63]
5 DDR_A_DM[0..7]
5 DDR_A_DQS[0..7]
5 DDR_A_MA[0..14]

Layout Note:
Place near JDDR1



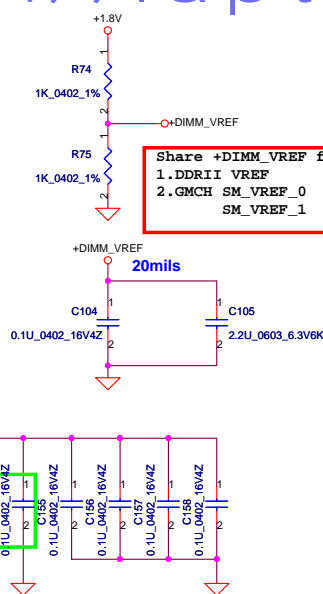
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



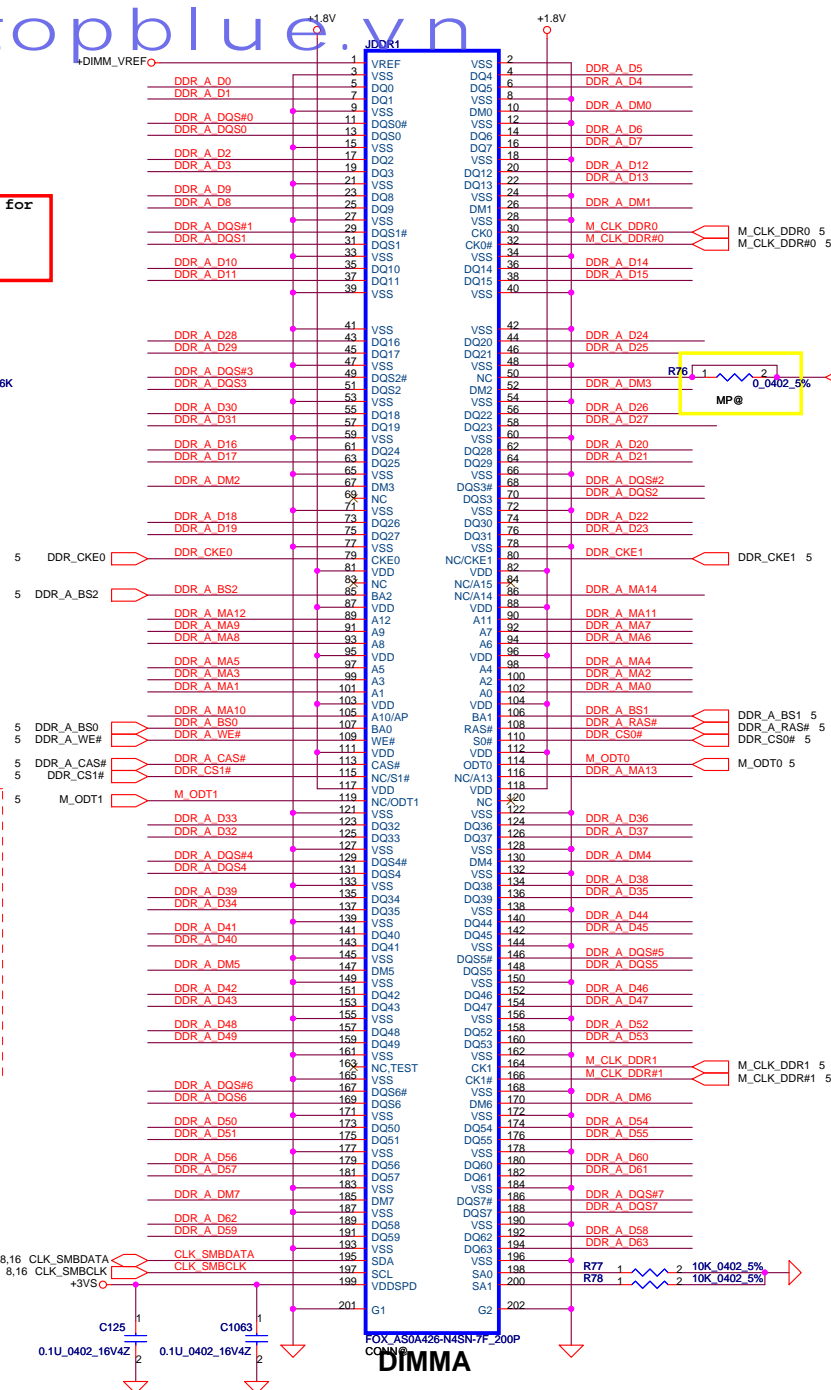
Layout Note:
Place these resistor closely DIMMA, all trace length < 1000 mil

Layout Note:
Place these resistor closely DIMMA, all trace length Max=1000 mil

Add 4PCS CAP on 1.8V for EMI request
3/27 add C203, C204 for EMI request

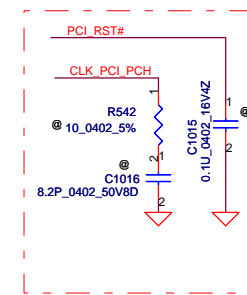
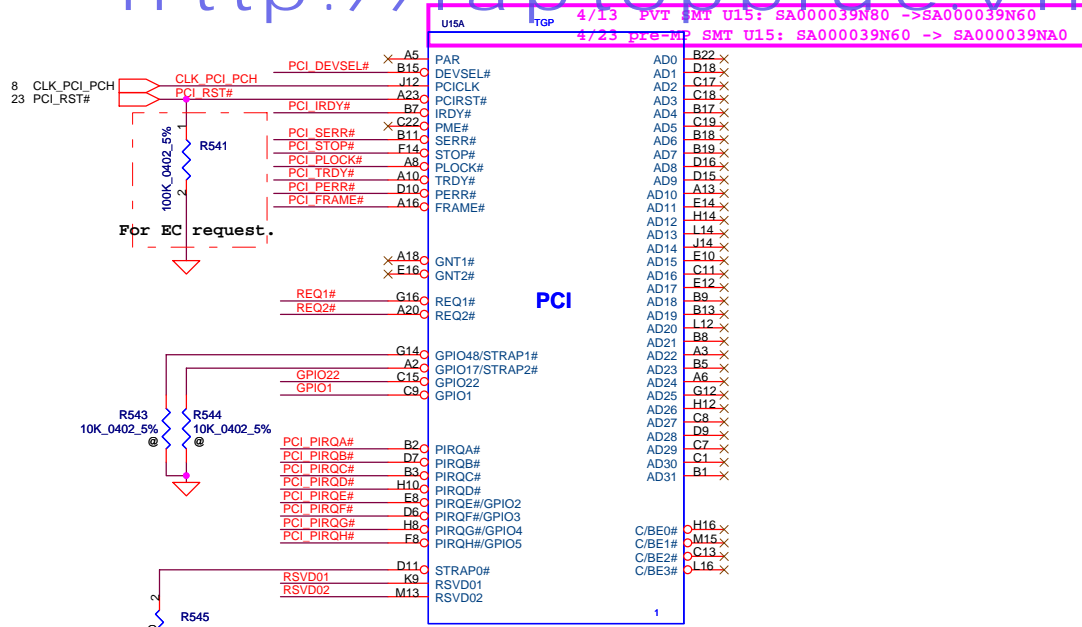
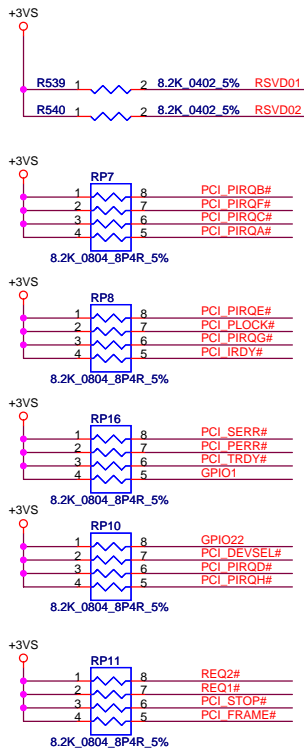


Share +DIMM_VREF for
1.DDR1 VREF
2.GMCH SM_VREF_0
SM_VREF_1

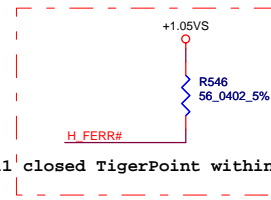


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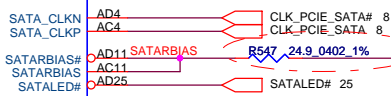
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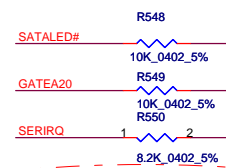
For EMI, close to TigerPoint



R111 closed TigerPoint within 1"

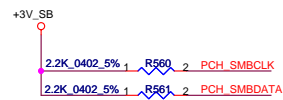


Please closed Tiger point PIN within 500 mils

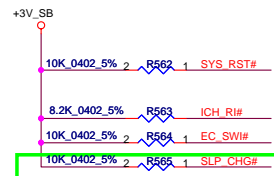
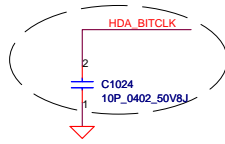


R110 to be within 1" from the Tiger Point chipset.

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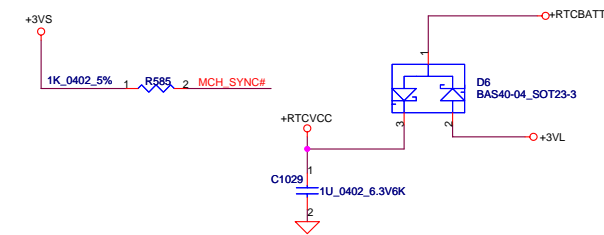
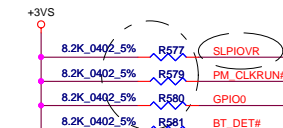
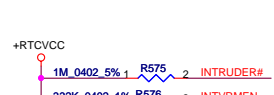
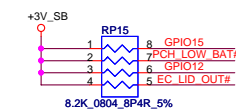
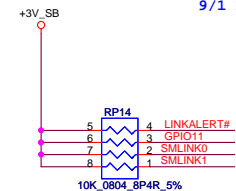


7/2 For EMI, Close to TigerPoint
9/1 C207 change to SE071100J80 for EMI request.

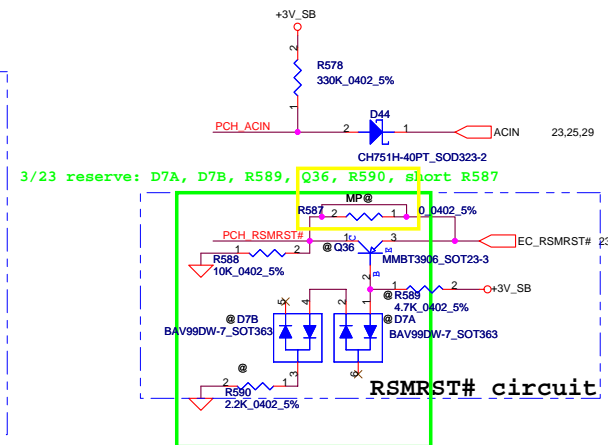
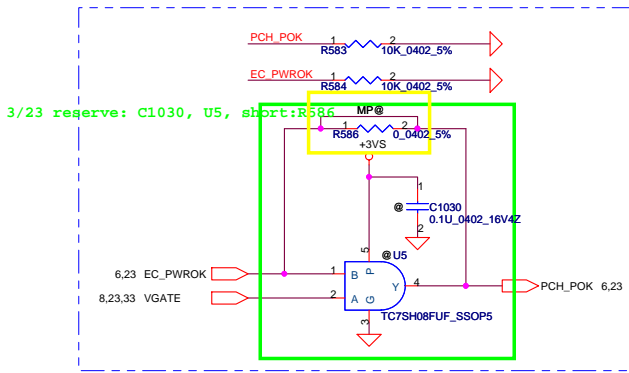
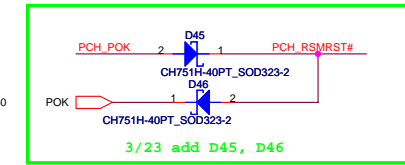
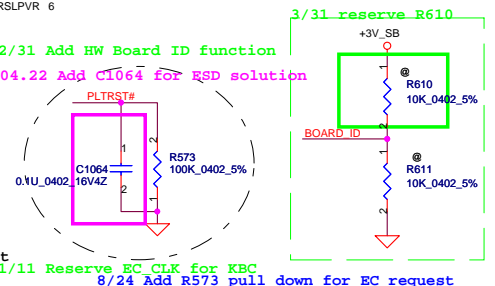
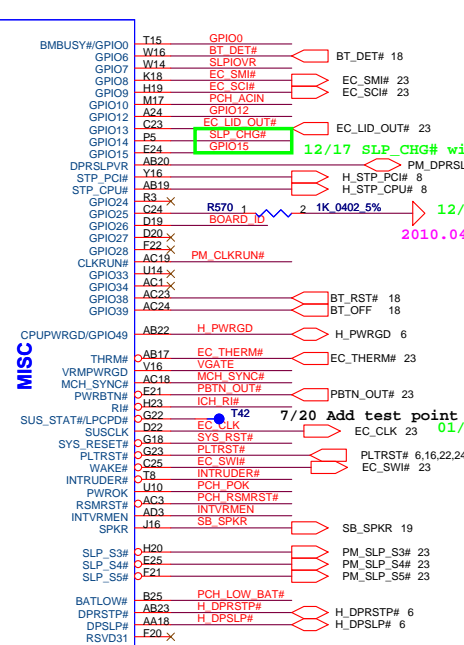
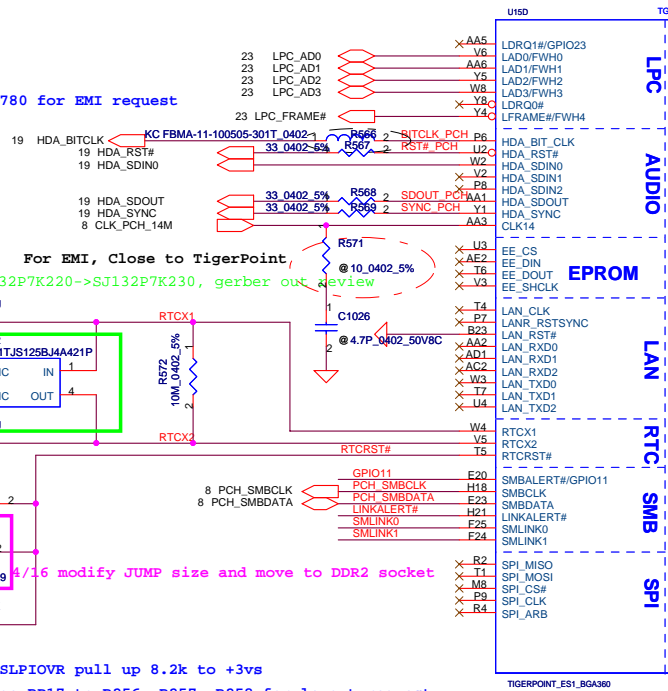


12/17 Add Pull high Resistor for GPIO14

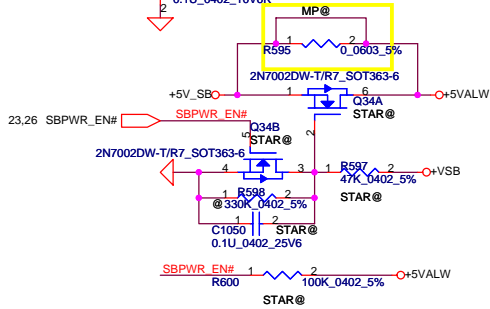
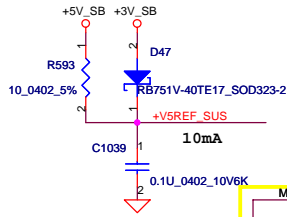
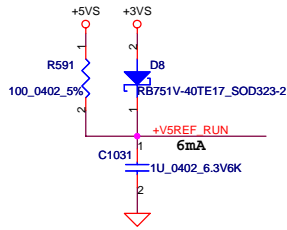
9/1 R125 change to SM010027780 for EMI request



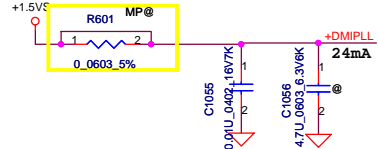
7/21 Change C156 to 1u for Intel request



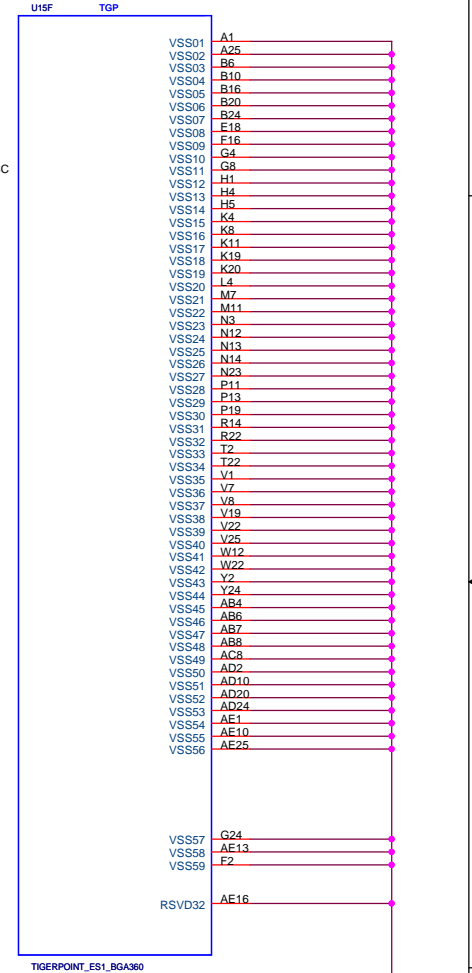
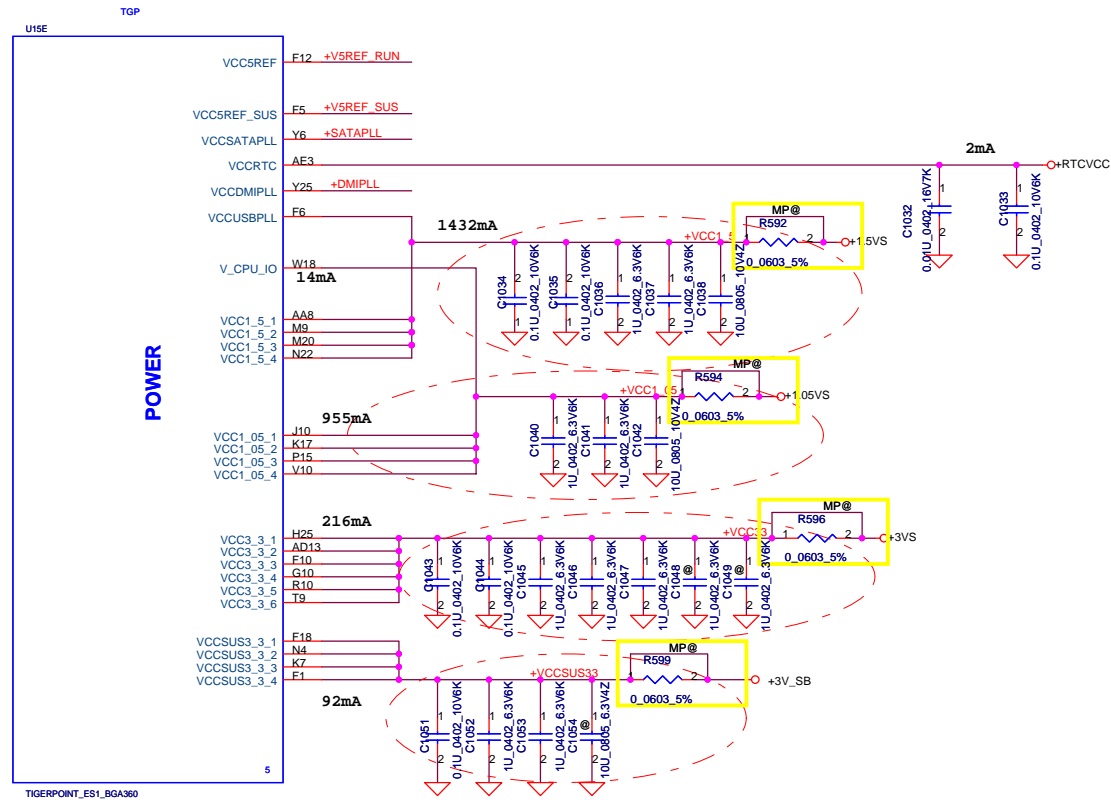
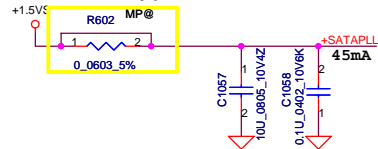
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Place closely pin Y25 within 100mlis.

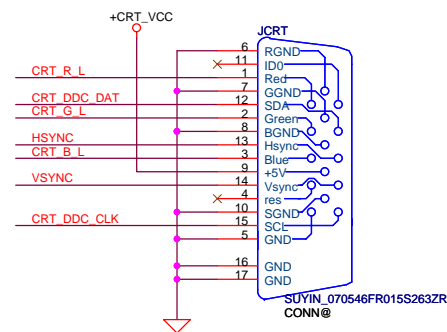
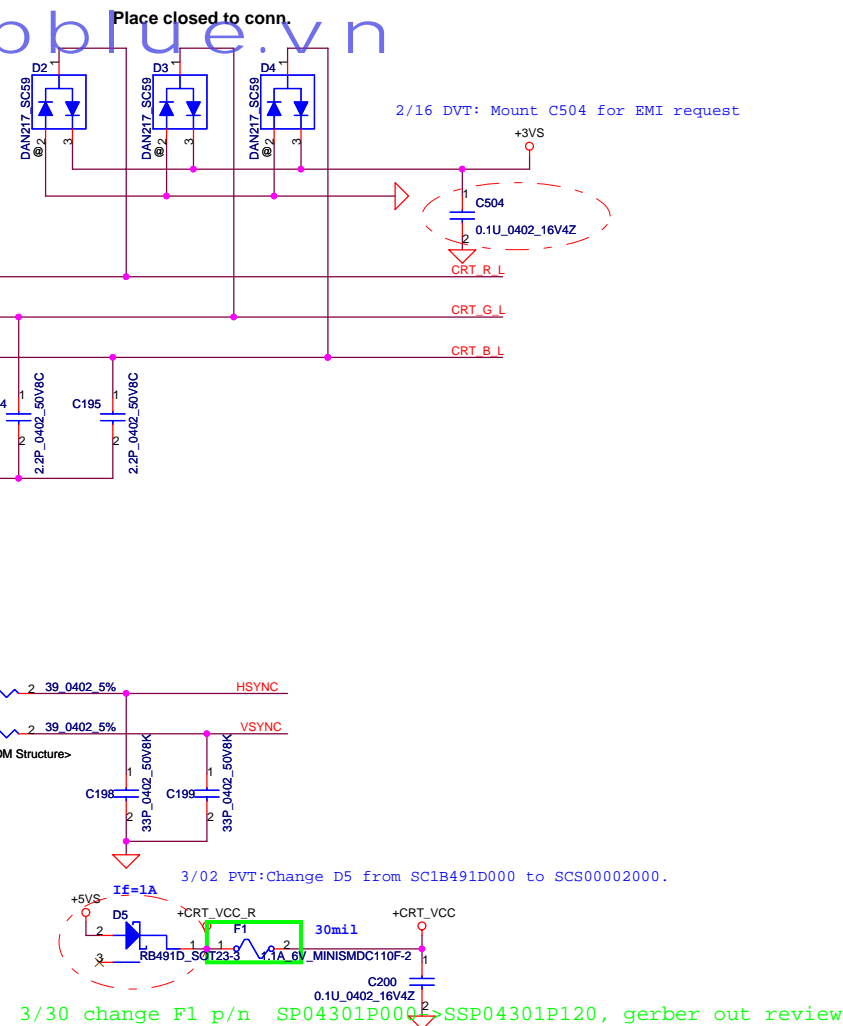


Place closely pin Y6 within 100mlis.



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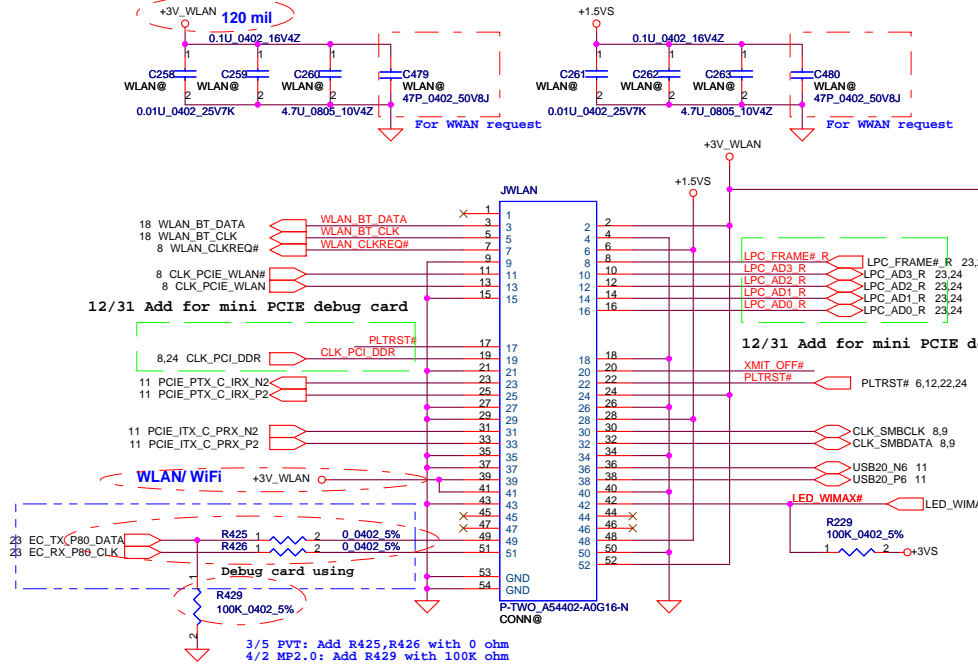
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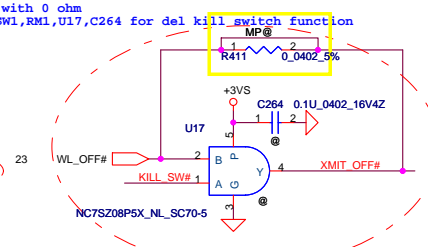
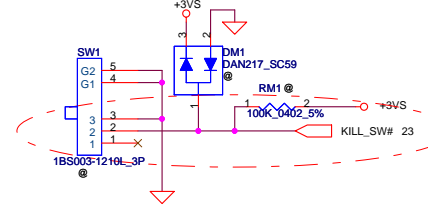
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Mini-Express Card for WLAN/WiMax

2/25 PVT:Mount C479,C480 with 47pf
3/16 PVT:Add BOM Config of C481,C482 to WLAN@

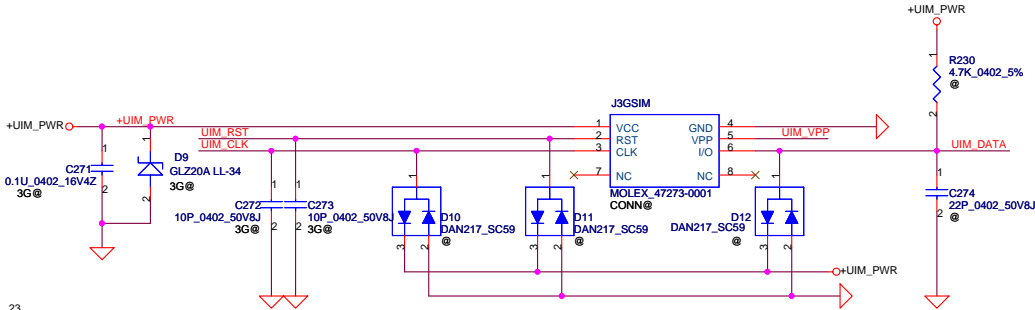
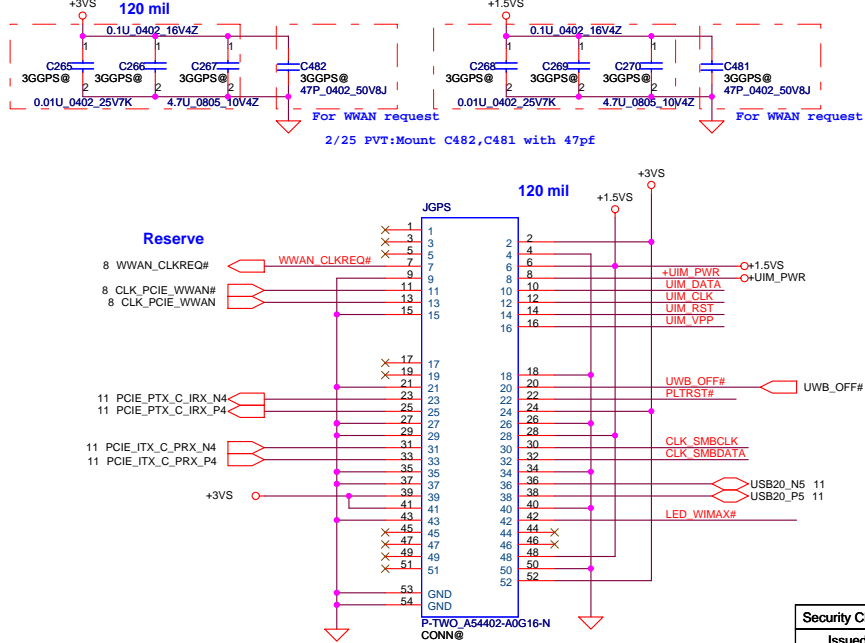


Kill SWITCH

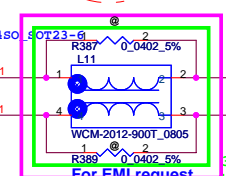
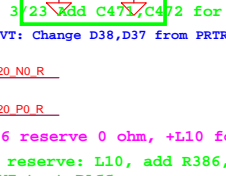
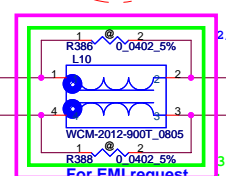
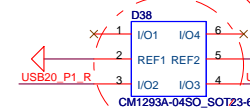
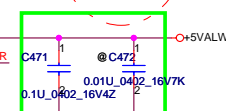
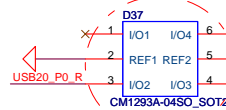
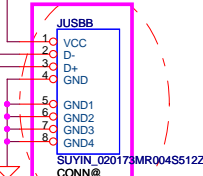
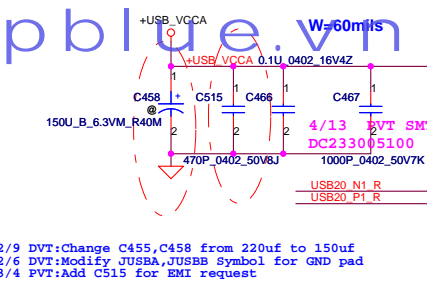
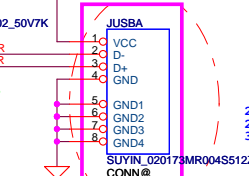
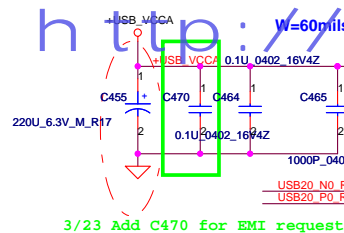


Mini-Express Card for 3G/GPS

3G current need to 2750mA
3/16 PVT:Add BOM Config of C481,C482 to 3G/GPS@



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4/26 reserve 0 ohm, +L10 for EMI request
3/23 reserve: L10, add R386, R388
by EMI test PASS

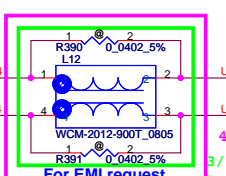
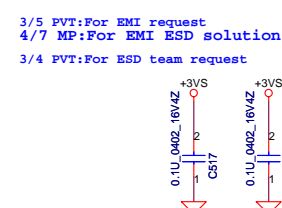
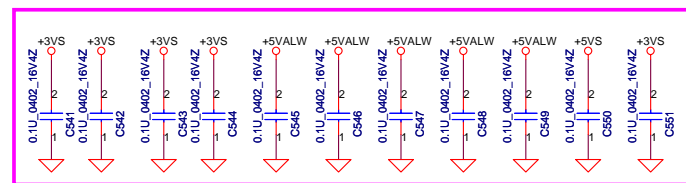
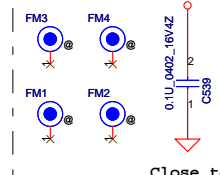
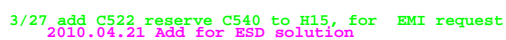
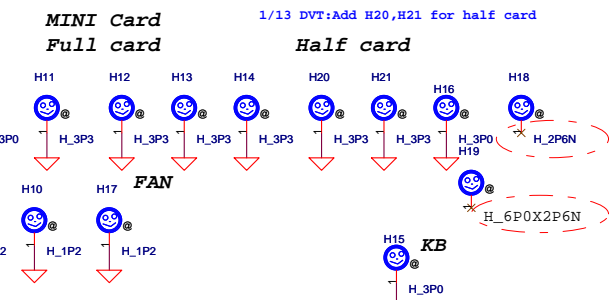
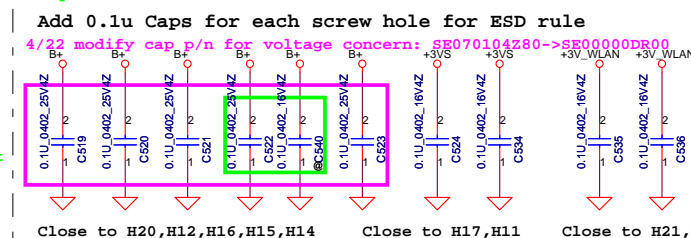
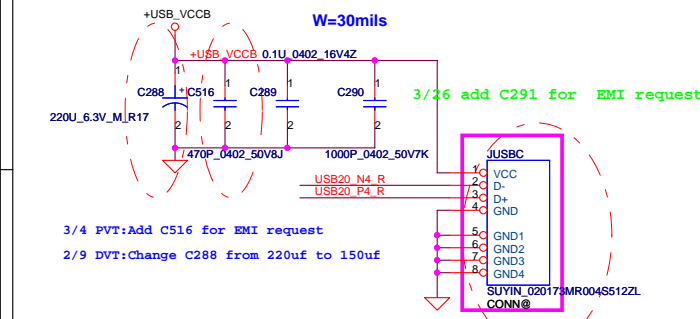
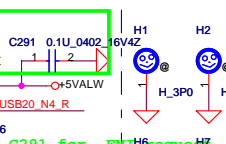
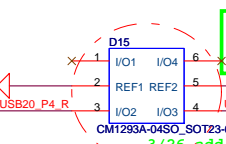
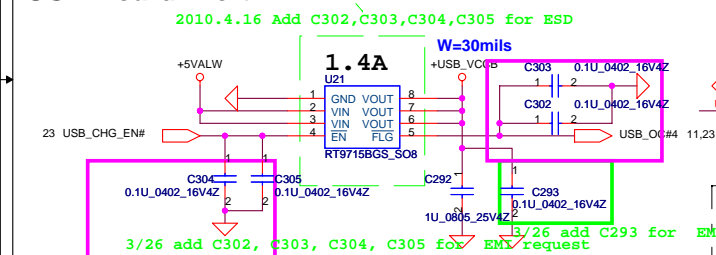
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4/26 reserve 0 ohm, +L11 for EMI request
3/23 reserve: L11, add R387, R389
by EMI test PASS

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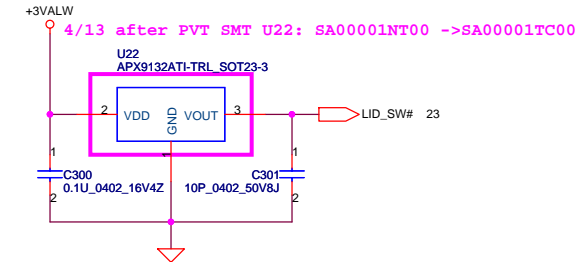
2/3 DVT: Change D15 from PRTR5V0U2X SOT143-4 to CM1293A-04SO SOT23-6



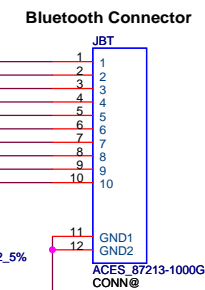
4/26 reserve 0 ohm, +L12 for EMI req.
3/23 reserve: L12, add R390, R391
by EMI test PASS

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http://laptopblue.vn

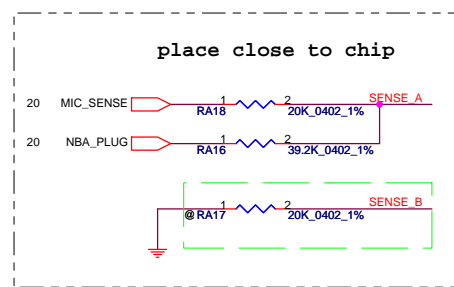
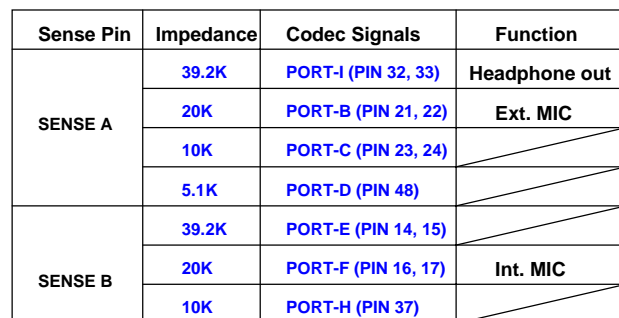


1/22 DVT:Change R238 from 10K to 47K
Add C499 with 0.01uF



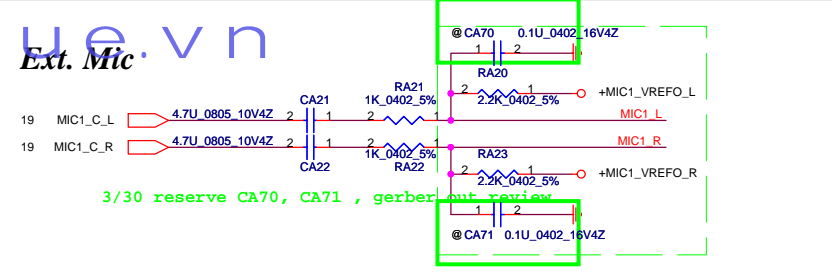
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http://laptools.blue.v

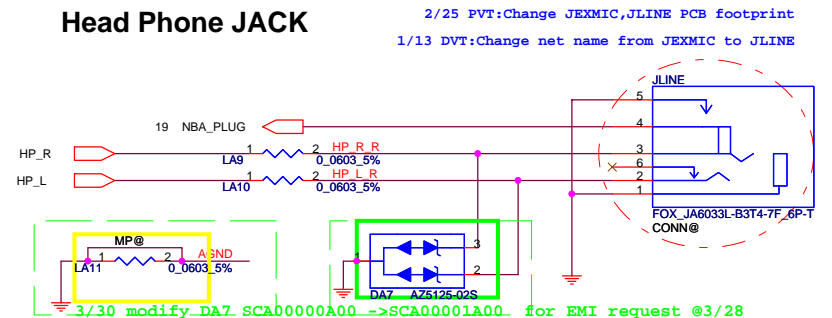
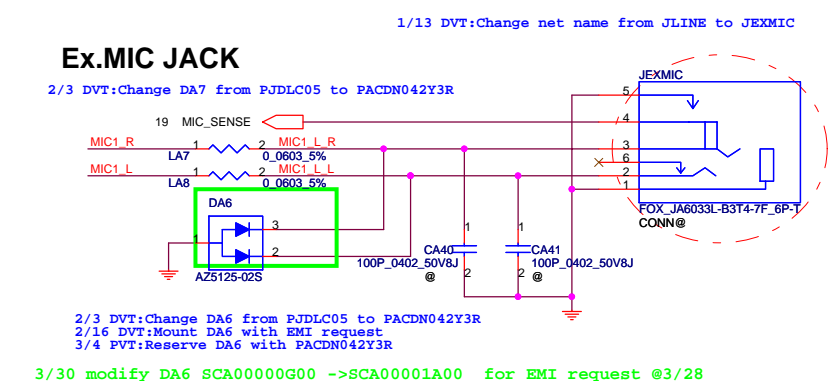
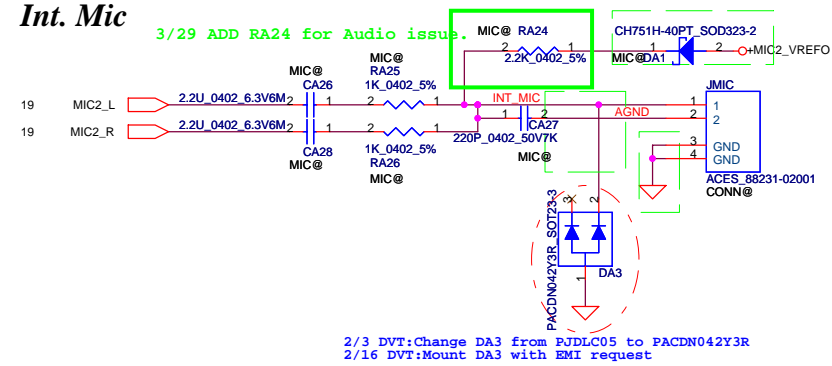


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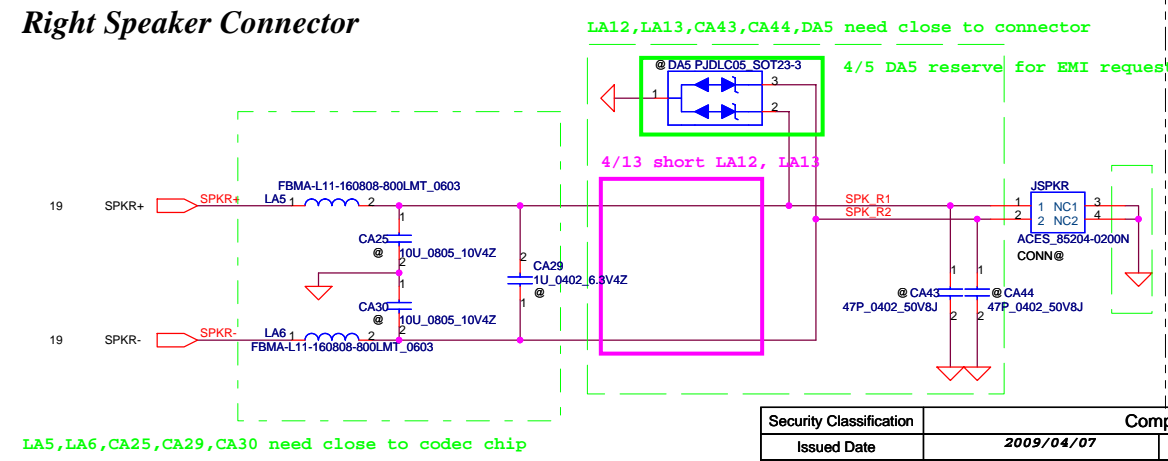
Ext. Mic



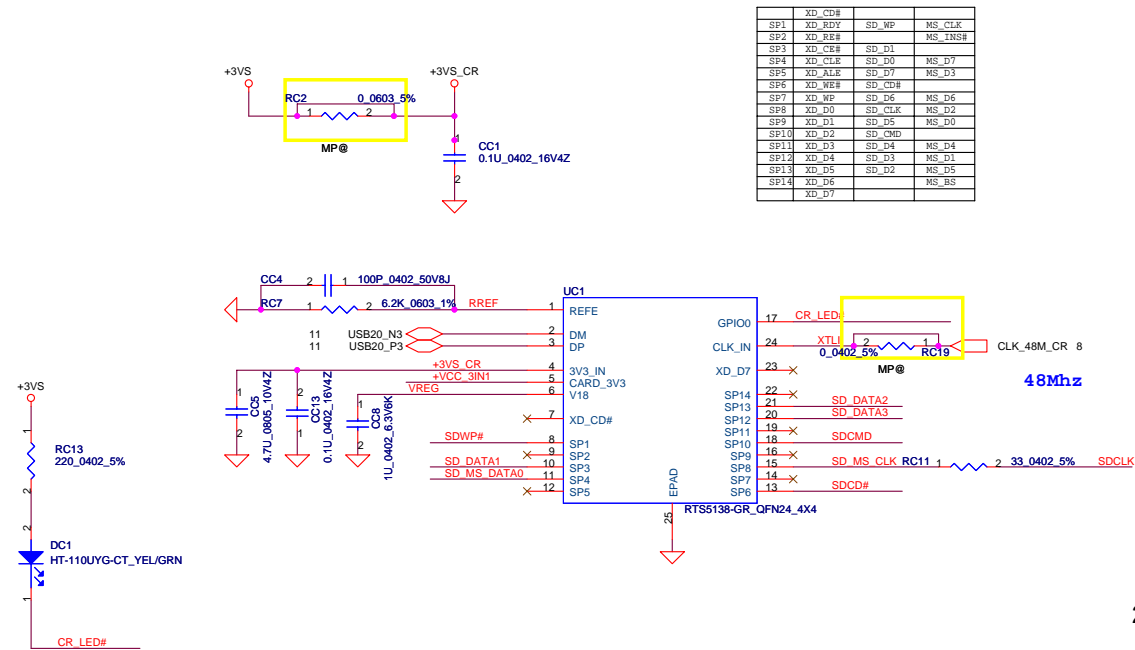
Int. Mic



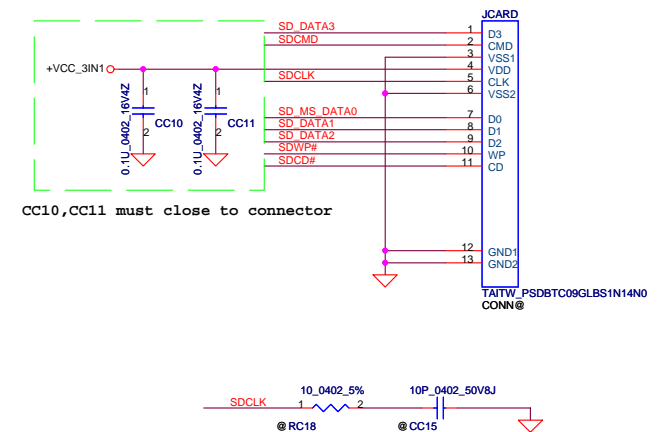
Right Speaker Connector



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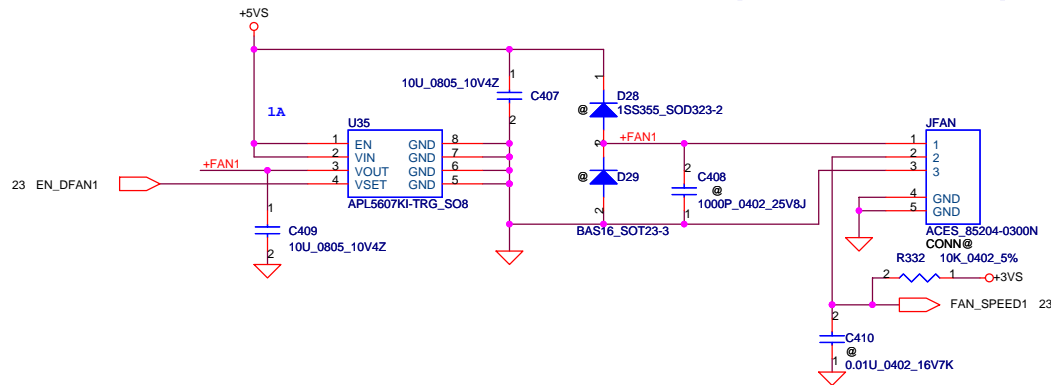
2 in 1 Card Reader



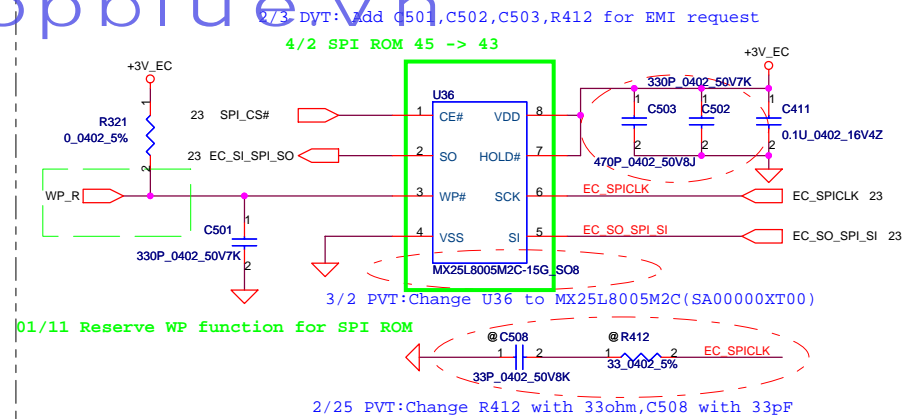
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FAN Control Circuit

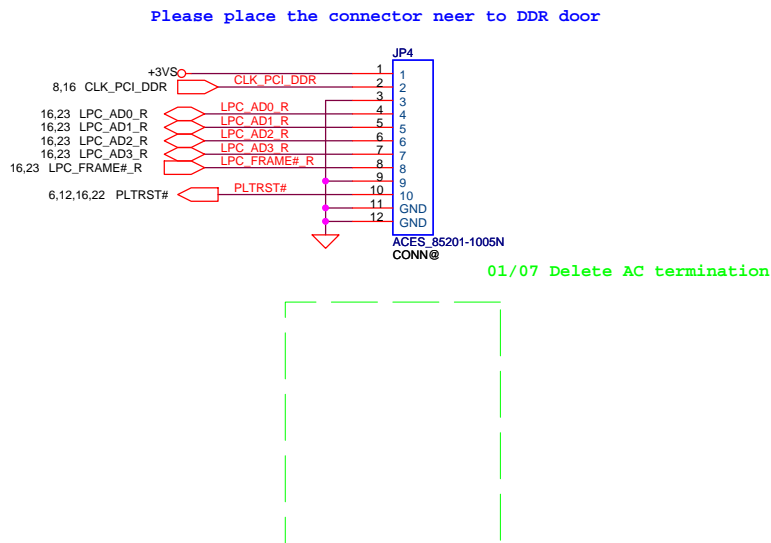
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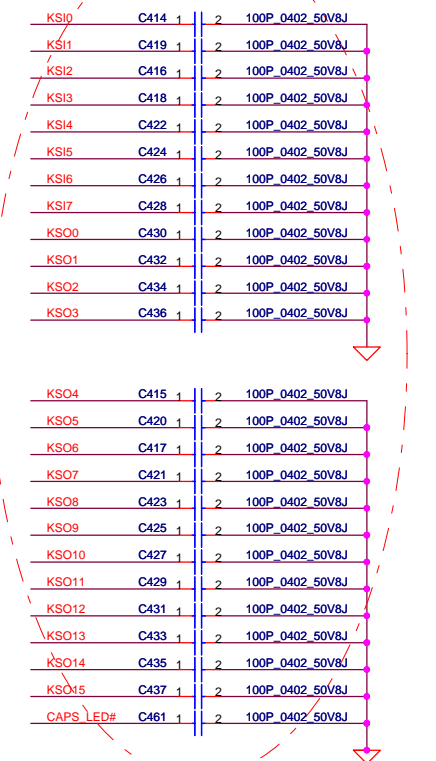
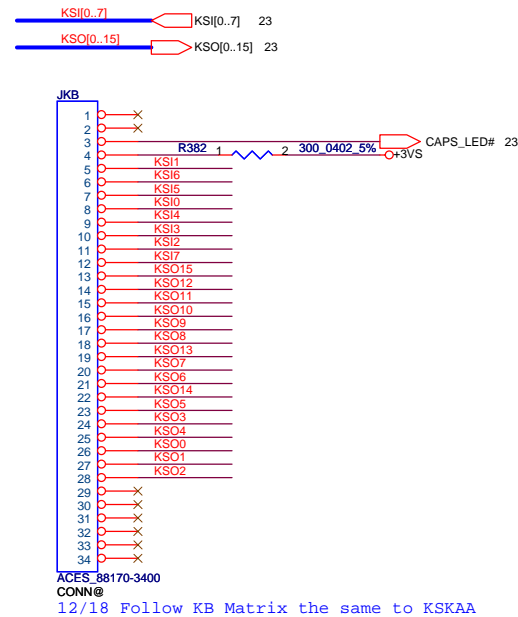
SPI Flash (8Mb*1)



LPC Debug Port



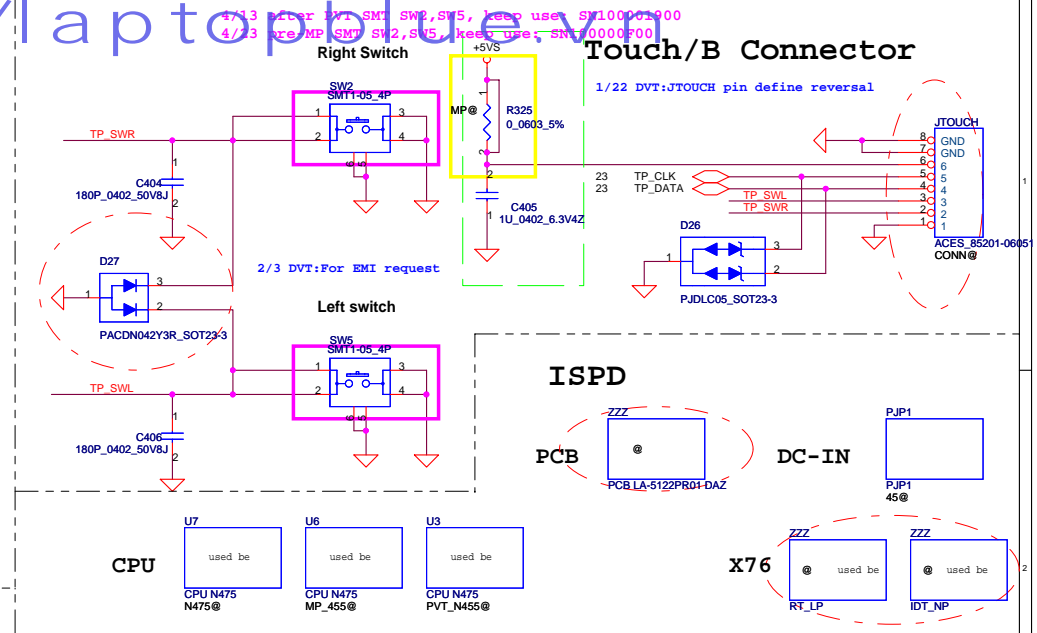
KEYBOARD CONN.



3/4 PVT:Mount C414-C437,C461 for EMI request

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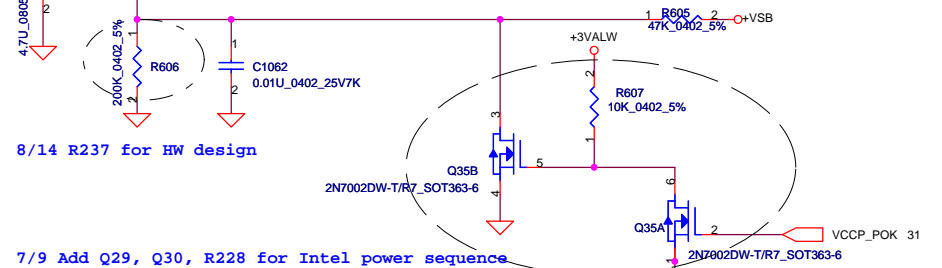
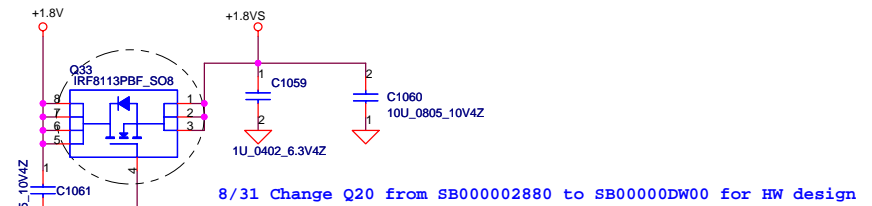
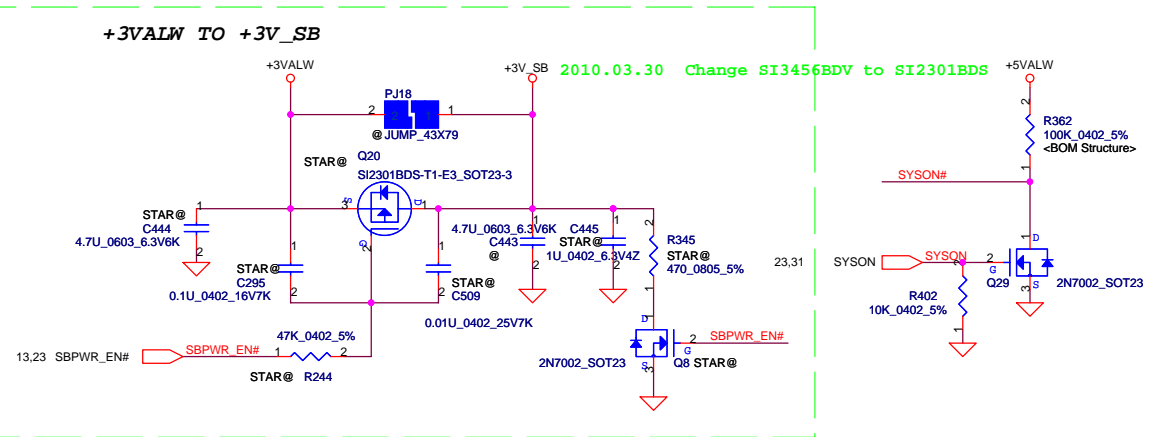
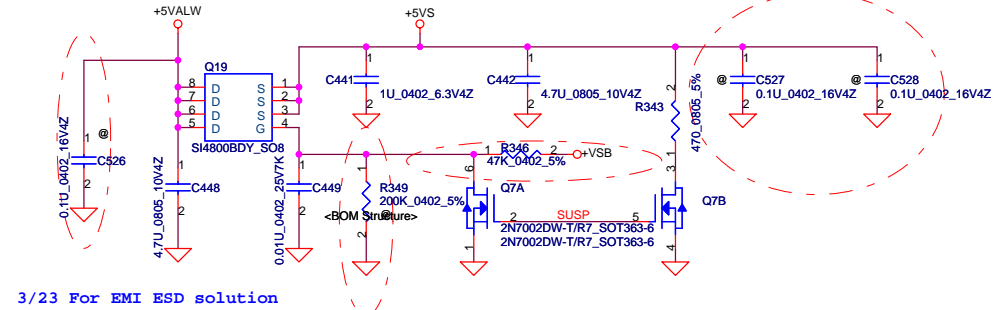
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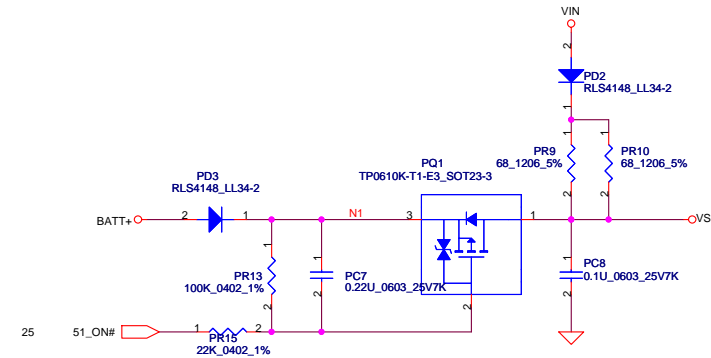
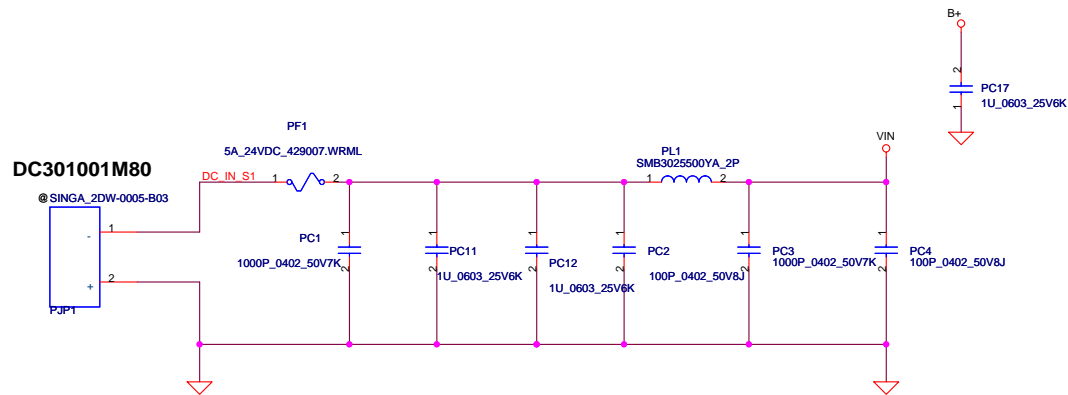
$V_F = 1.9V (typ), 2.4V (max)$
 $I_F = 20mA (max)$

+3VS — 1 — R333 — 2 — 220_0402 5% — 2 — D30 — 1 — WL_BT_LED# 23
 WLAN@ HT-110UD 1204_AMBER WLAN@

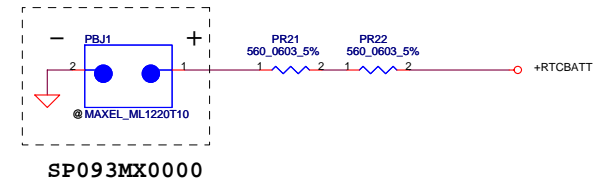
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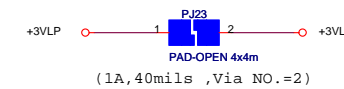
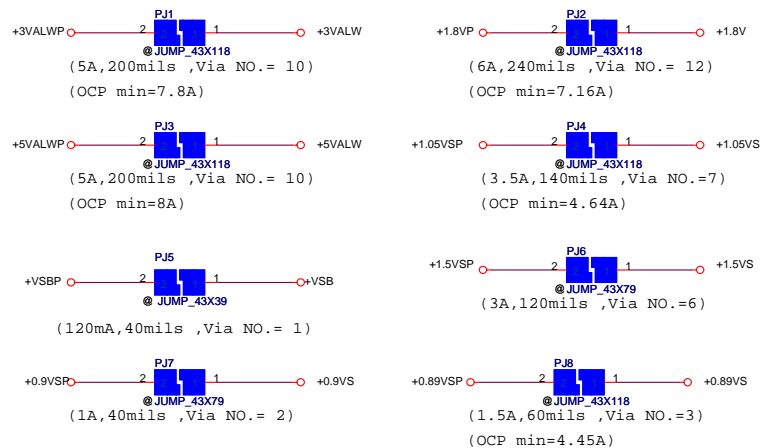
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RTC Battery



SP093MX0000



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				Rev	C

PH1 under CPU bottom side :

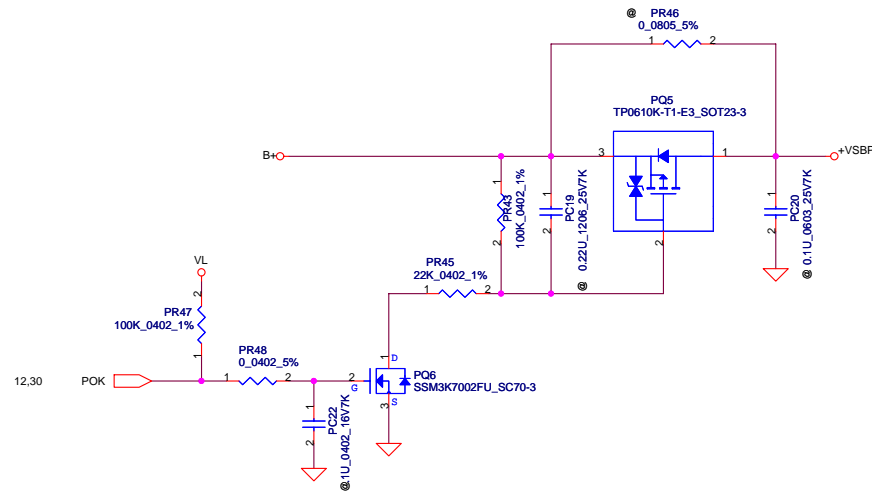
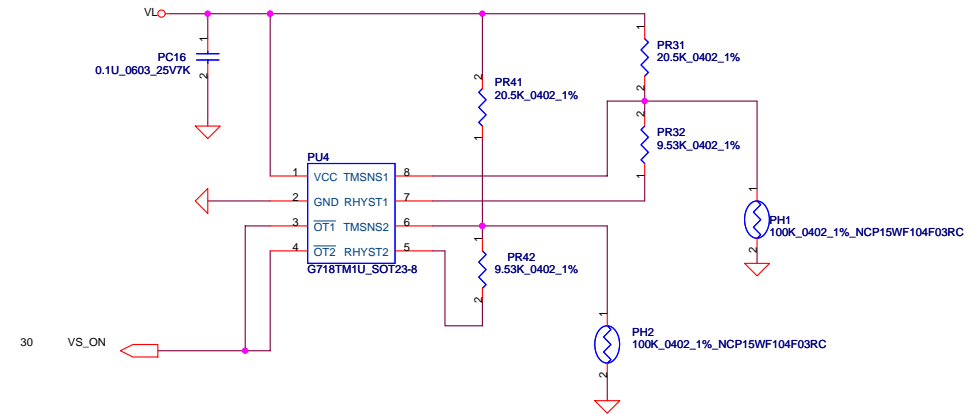
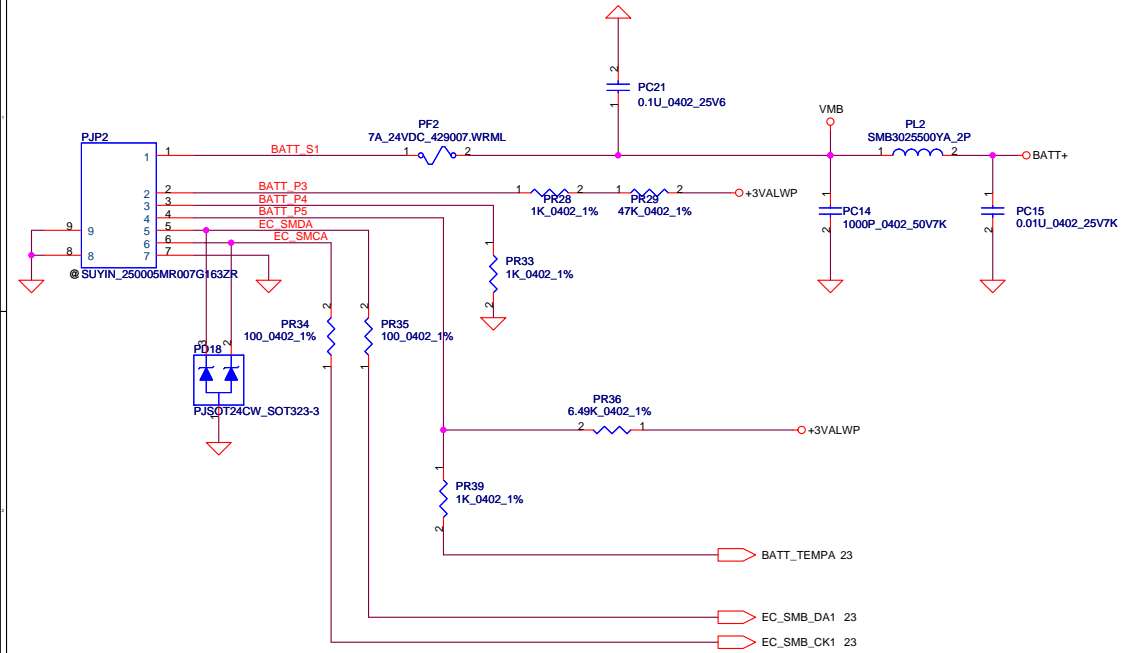
CPU thermal protection at 92 degree C

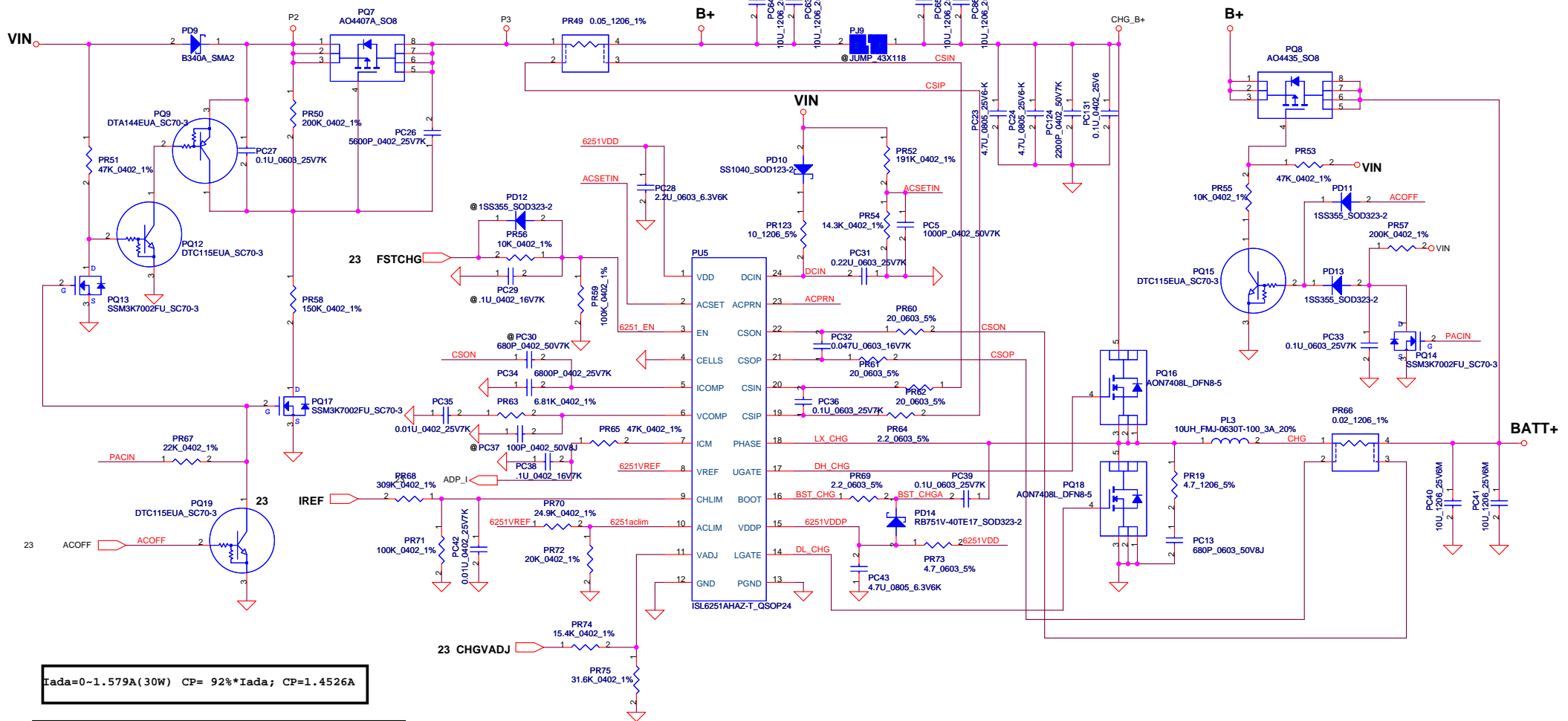
Recovery at 57 degree C

PH2 near main Battery CONN :

BAT. thermal protection at 92 degree C

Recovery at 57 degree C



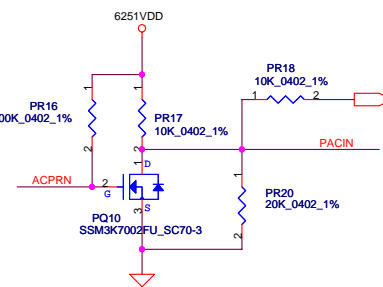


$$I_{ada} = 0 - 1.579A (30W) \quad CP = 92\% \cdot I_{ada}; \quad CP = 1.4526A$$

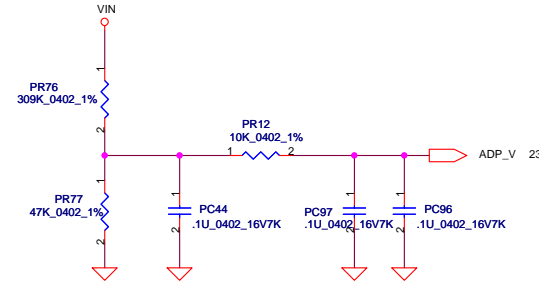
CP mode
 $V_{aclim} = 2.39 \cdot (20K // 152K) / (24.9K // 152K + 20K // 152K) = 1.0817V$
 $I_{input} = (1/0.05) \cdot ((0.05 \cdot V_{aclim}) / 2.39 + 0.05)$
 where $V_{aclim} = 1.0817V$, $I_{input} = 1.4526A$

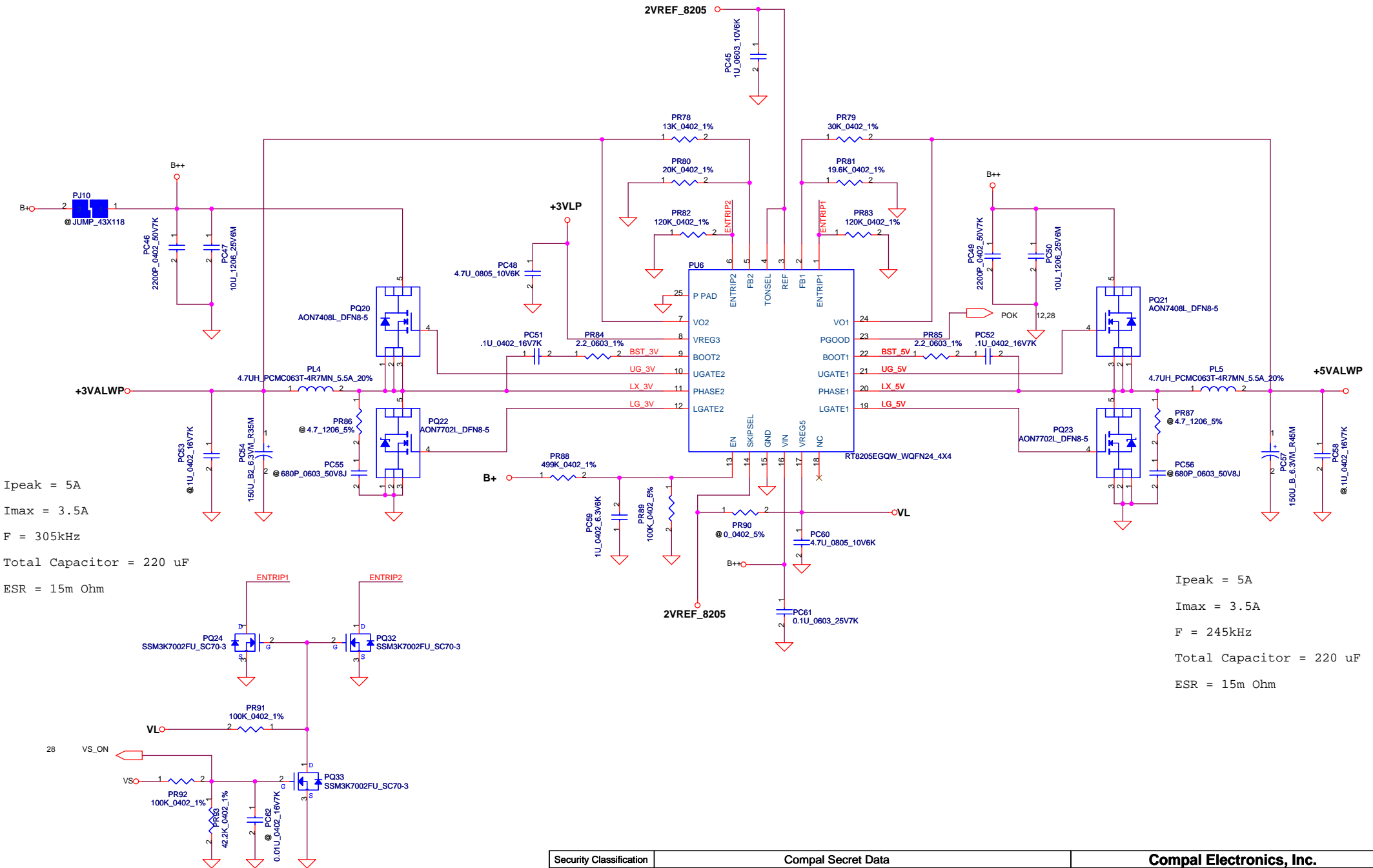
CC=0.25A-2A
 IREF=1.648*Icharge
 IREF=0.412V-3.296V
 VCHLIM need over 95mV

CHGVADJ=(Vcell-4)*9.445	
Vcell	CHGVADJ
4V	0V
4.2V	1.89V
4.35V	3.3V



Vin Detector
 High 18.089V
 Low 17.44V

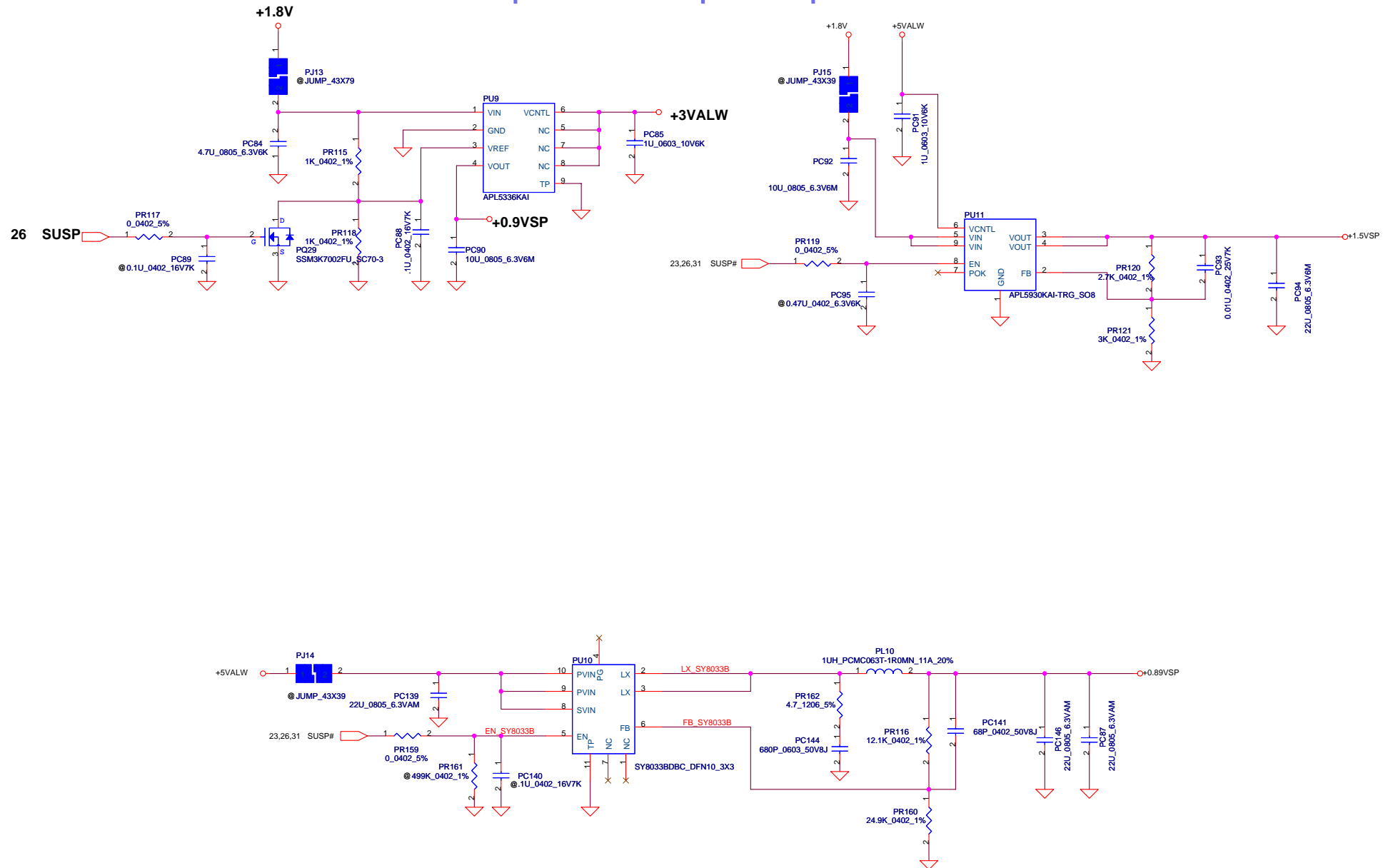




Ipeak = 5A
 Imax = 3.5A
 F = 305kHz
 Total Capacitor = 220 uF
 ESR = 15m Ohm

Ipeak = 5A
 Imax = 3.5A
 F = 245kHz
 Total Capacitor = 220 uF
 ESR = 15m Ohm

Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2009/10/07		Deciphered Date		2012/10/07		Title	
										SCHEMATICS , MB A5122	
										401897	
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Issued Date	2009/10/07	Deciphered Date	2012/10/07	Title
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Version Change List (P. I. R. List) for Power Circuit

ist) for Power Circuit

	<i>Item</i>	<i>Page#</i>	<i>Title</i>	<i>Date</i>	<i>Request Owner</i>	<i>Issue Description</i>	<i>Solution Description</i>	<i>Rev.</i>
1	PC21	PD18		20100205	PWR	Layout space not enough	change to small type	
	PC141			20100317	PWR	SY8033B needs the feed forward cap for a better load transient and stability.	Add 68p cap.	
	PC63	PC64	PC65 PC86	20100324	EMI	EMI request	Add 10u cap. x4	
2								
3								
4								

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Issued Date	2007/08/02	Deciphered Date	2008/08/02	Title	
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PIR (Product Improve Record)

KAVAA LA-5121P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1

http://laptopblue.vn

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE

08/12/30				
(1) P30			Mount R361 with 100K ohm	For SUSP pull high
08/12/26				
N0	PAGE		MODIFICATION LIST	PURPOSE
(1) P29			Add U1(SA000036K00)forN280 CPU	
08/12/25				
(1) P27			Del R398 with 0 ohm and U32.10 link to GND	For customer recommend
(2) P31			Change H3 link to GNDA	For EMI request
08/12/24				
N0	PAGE		MODIFICATION LIST	PURPOSE
(1) P27			Change U32.7 link to +3VS_HDP	
			Change U32.9 no connect	
08/12/23				
(1) P16			Add U15A.AF7 and U15A.AE7 link to GND	The unused STAT port RX signals must be properly tied to ground
08/12/22				
(1) P15			Change C203.1 Net name from PLTRST#_R to PLTRST#	
(2) P12			Reserve C868 with 10P	For Custome request
(3) P13			Reserve C871 with 10P	For Custome request
(4) P25			Reserve RC21 with 10 ohm and CC16 with 10P	For Custome request
08/12/21				
(1) P16			Change C209 Package from 0603 to 0402	For layout pacement limit
(2) P18			Change C222 Package from 0603 to 0402	For layout pacement limit
			Change C219 Package from 0603 to 0402	For layout pacement limit
(3) P25			Mount RC20 with 0 ohm	For CLK 48Mhz
08/12/18				
(1) P4			Reserve C484-C495 with 180p	For debug
(2) P6			Add R403-R405 with 1K ohm	For CPU CLK link to NB
(3) P10			Change package C61,C62,C68,C78,C79 from 0603 to 0402	For layout pacement limit
			Change package C74,C75 from D2 to B2	For layout pacement limit
(4) p11			Del C124 with 2.2U	
(5) P12			Del R85,R87,R88,R89,R92,R94,R95,R96,R102,R105,R106,R109	For CPU BSELE0-2 link to CLK Gen
			Change R90,R91 from 33 ohm to 22 ohm	For damping resistor when loading is two device
			Chagne net name FSB to CPU_BSEL1	For CPU link to CLK Gen
			Del R110,R111 with 10K ohm	For UMA platform not need to reserve
(6) P13			Change Net name R117.1 from +3V_SB to +3VS	For layout pacement
			Change C183 link from GND to +3VS	For layout pacement
			Change JLVDS pin2 from +LEDVDD to +LCDVDD_L	For LCD power consumption
(7) P14			Change C190~195 to 2.2P	For EMI request
(8) P15			Change package to 8P4R with 8.2K	For layout pacement limit
			Del U16,R180,C206	
(9) P16			Del R190 with 8.2Kohm	For customer request
			Change R189 from 4.7K to 10K ohm	
			Change Net name from IDE_DIORDY to IDE_DIORDY_IRQ	
(10) P17			Change R216 from 100K to 330K ohm	For ACIN issue
			Add R215,R406,Q31,R408,D43,R409	For leakage current of RSMRST# Circuit
			Add R410,D44	For EC leakage current to SB
(11) P18			Add R496 with 0.1U	For soft start
(12) P18			Add L15 with MBK1608121YZF_0603	For Ripple
(13) P20			Change C455,C458,C222 from D2 to B2 with 220U	For layout placeemnt limit
			Change U21.4 from USB_EN# to USB_CHG_EN#	For customer request
			Add U21.5 link to U29.74	
(14) P21			Del Q17 with 2N7002	For cost down
			Change R237.1 from +5VS to +3VS	
			Chagne C294.2 from GND to +3VS	
(15) P22			Reserve PU19	
(16) P24			Del CL6 with 10U	
			Change UL3 from HD-024A to NS681680	For cost down
(17) P25			Reserve CC9,CC12,YC1	
			Mount RC19 for 48Mhz	
			Mount RC20 For 48Mhz	
(18) P26			Del R304 with 10K ohm	
			Change R307 from 100K to 330K ohm	
			R243 please close to EC	
			Add Net Name USB_CHG_EN#	
			Del D22,R310,R311	
(19) P27			Change U31 P/N from SA000030500 to SA000035U00	
(20) P28			Chagne U36 ROM Size from 16M*1 to 8M*1	
			JBK KB Matrix the same to KSKAA	
			Del JP2	
(21) P29			Change R370,R371,R372,R375,R383,R384,R374,R333 from 120 ohm to 220 ohm	
			Del R325,R326	
(22) p30			Add R401,R402 with 10K ohm	

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Issued Date	2009/04/07	Deciphered Date	2012/10/21	Title	SCHMATICS , MB A5122
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				401897	C
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PIR (Product Improve Record)

KAVAA LA-S121P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1-->0.2

http://laptopblue.vn

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1)	1/13	10	Change D1 to CH751H-40PT_SOD323-2	For BOM simplify
2)	1/13	18	Change D7,D8 to CH751H-40PT_SOD323-2	For BOM simplify
3)	1/13	23	Change net name from JLINE to JEXMIC	For EXMIC JACK
4)	1/13	23	Change net name from JEXMIC to JLINE	For JLINE JACK
5)	1/13	29	Change JPOWER.3 net name from ON/OFFBTN# to ON/OFFBTN#_R	For PWR/B can't power on with battery mode
	1/13	30	Add H20,H21	For half card
6)	1/22	13	Change R117 from 47k to 100K ohm	For LCD Soft start reduce inrush current
			Change Q11 from SI2301BDS to A03413	For LCD Soft start reduce inrush current
			Add C498 with 0.01uF	For LCD Soft start reduce inrush current
7)	1/22	19	Change SW1.3 to dummy pin	For Kill switch issue
			Change SW1.1 to GND	For Kill switch issue
8)	1/22	21	Change R238 from 10K to 47K	For BT Soft start reduce inrush current
			Add C499 with 0.01uF	For BT Soft start reduce inrush current
9)	1/22	22	Del Net name AMP_SPK_R and AMP_SPK_L	For Mono SPK
			Add Net name AMP_SPK from UA2.37 to UA3.17	For Mono SPK
		23	Del CA32 with 0.033UF	For Codec output less than 0.9V
			Add RA38,RA40 with 1K ohm	For Codec output less than 0.9V
			Add RA39,RA41 with 9.09k ohm	For Codec output less than 0.9V
			Add CA43 with 1uF	For Codec output less than 0.9V
	1/22	27	Change U34 P/N from SA00000XZ50 to SA000037Y60	For G-sensor controller chip change
		29	JTOUCH pin define reversal	For ME request assembly easy
		30	Change R355 from 3.3K to 47K	For LAN Soft start reduce inrush current
			Add C500 with 0.01uF	For LAN Soft start reduce inrush current
10)	2/3	14	Reserve C504 with 0.1uF	For EMI request
	2/3	19	Add R411 with 0 ohm	Del Kill switch function
	2/3		Reserve SW1,RM1,U17,C264 for del kill switch function	Del kill switch function
	2/3	20	Change D15,D38,D37 from PRTR5V0U2X to CML293A-04SO	For EMI request
	2/3	23	Change DA3,DA6,DA7 from PJDLC05 to PACDN042Y3R	For EMI request
	2/3	28	Add C501,C502 with 330pF	For EMI request
			Add C503 with 470pF	For EMI request
			Add R412 with 10 ohm	For EMI request
			Add C508 with 6pF	For EMI request
	2/3	29	Add R413,R414,R415 with 0 ohm	For EMI request
			Reserve C505,C506,C507 with 0.1uF	For EMI request
			Change D27 from PJDLC05 to PACDN042Y3R	For EMI request
			Del D25 with PJDLC05	For EMI request
			Change R375 from 220 to 300 ohm	For White LED of PWR/B
			Change R375.1 Net name from +3VALW to +5VALW	For White LED of PWR/B
11)	2/4	22	Change CA14 from 100pF to 0.1uF	For SPK noise issue
			Add PJ20,PJ21	For customer request(Echo Peak Issue)
		24	Change UL3 from 16pin(SP050003N00) to 24pin(SP050003P00)	For EMI issue
12)	2/5	06	Add R416 with 0 ohm	For WWLAN request
			Reserve C511 with 22pF	For WWLAN request
		12	Reserve C509,C510 with 10p	For WWLAN request
		22	Reserve UA1,CA9,CA11	For cost down plan
	2/6		Modify JUSBA,JUSBB,JUSBC Symbol for GND pad	For GND pin
		10	Reserve C67 with 220uF	For Cost down plan
			Add C514 with 0.1uF	For ESD team request
		23	Change RA38,RA40 with 2K ohm	For Codec output less than 0.9V
			Change RA39,RA41 with 8.2K ohm	For Codec output less than 0.9V
		24	Change UL3 from NS681680(SP050003N00)to 8456E(SP050005V00)	For ESD fail issue
		30	Reserve +1.5VS,+1.05VS,+0.9VS,+1.8VS discharge circuit	For Cost down plan
		27	Reserve C867 with 0.22uF	For U33.4 NC pin
			Change U33 from APL5151-33BC to G9191-330T1U	For power sequence issues on HPC
	2/9	20	Change C455,C288 from 220uF to 150uF	
			Reserve C458 with 150uF	For Cost down plan
	2/11	22	Mount RA13 with 0 ohm	For EMI request open channel
		27	Change U31 from SA000035U00 to SA000039900	For Customer request version change
	2/16	14	Mount C504 with 0.1uF	For EMI request
		23	Mount DA3/DA6 with PACDN042Y3R	For EMI request
		17	Reserve C217,C218 with 0.1uF	For Reserve WWAN PCIE interface

PIR (Product Improve Record)

KAVAA LA-5121P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.2-->1.A

http://laptopblue.vn

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1)	2/25	4	Mount C484-C495 with 220pF	For EMI request
2)	2/25	6	Change Net name from ICH_POK to ICH_PWROK	For correcting power down sequence
3)	2/25	12	Change R81,R82 from 0 ohm to FBMH1608HM601-T_0603	For WWAN request
			Mount C133,C141 with 47pF	For WWAN request
			Mount C142,C143,C144,C145,C146,C868 with 22pF	For WWAN request
4)	2/25	13	Mount C871 with 10pF	For WWAN request
5)	2/25	15	Mount C203,C204 with 0.1uF	For WWAN request
6)	2/25	17	Change Net name from ICH_POK to ICH_PWROK	For correcting power down sequence
			Add R418 with 10K ohm	For correcting power down sequence
			Add U37 with TC7SH08FUF_SSOP5(SA007080100)	For correcting power down sequence
			Reserve R417 with 0 ohm	For correcting power down sequence
7)	2/25	19	Mount C479,C480,C481,C482 with 47pF	For WWAN request
8)	2/25	22	Mount RA31 with 22 ohm,CA34 with 10pF	For WWAN request
9)	2/25	23	Change JEXMIC,JLINE PCB footprint to JA6033L-B3T4-7F_6P-T	For ME request
10)	2/25	25	Mount CC16 with 10pF,RC21 with 10 ohm	For WWAN request
11)	2/25	26	Change U29.104 net name from ICH_POK to EC_PWROK	For correcting power down sequence
12)	2/25	28	Mount C508 with 33pF,R412 with 33 ohm	For WWAN request
13)	2/25	30	Reserve R349 with 200K ohm	For design change
			Change C447 from 0.01uF to 0.022uF	For design change
			Change R346 from 20K to 47K ohm	For design change
14)	3/2	14	Change D5 from SC1B491D000 to SCS00002000	For buyer recommend
		28	Change U36 to MX25L8005M2C(SA00000XT00)	For CLK frequency 75MHz
	3/2	30	Change H18 from H_3P0N to H_2P6N	For ME request
			H19 from H_6P0X3P0N to H_6P0X2P6N	For ME request
	3/4	08	Add GMCH_INV_T_PWM on U3.H30	For support DPST function
		13	Add R419 with 0 ohm	For support DPST function
			Reserve R420 with 0 ohm	For support DPST function
			Del JLVDS pin 2 for dummy pin	For prevent short B+
		23	Mount DA5 with PJDLC05	For EMI request
		23	Reserve DA6 with PJDLC05	For EMI request
		20	Add C515,C516 with 470pF	For EMI request
		28	Mount C414-C437,C461 with 100pF	For EMI request
		17	Add R421 with 330K ohm to +3VALW	For USB over current protect
		17	Add D45 with CH751H-40PT to USB_OC#0_2	For USB over current protect
		17	Change RP7.4 from USB_OC#0_2 to USB_OC#0_2_D	For USB over current protect
		17	Change U15.D3 from USB_OC#0_2 to USB_OC#0_2_D	For USB over current protect
		26	Add Net name to USB_OC#0_2	For USB over current protect
		29	Change R413,R414,R415 from 0 ohm to FBMA-10-100505-151T	For EMI request
		30	Add C517-C520 with 0.1uF	For ESD request
3/5		12	Reserve R427 with 0 ohm	For Silego source chip
			Add R428 with 10K ohm to +3VS	For Silego source chip
			Change U4.54 from H_STP_PCI# to H_STP_PCI#_R	For Silego source chip
3/5		17	Add R423,R424 with 0 ohm	For design change
			Reserve R410,R421 with 330 K ohm	For design change
			Reserve D44,D45 with CH751H-40PT	For design change
			Add R425,R426 with 0 ohm	For debug
		30	Reserve R422 with 0 ohm and PJ22 with JUMP_43X79	For EMI request
		30	Change H15 to Non-PTH hole	For design change
3/10		17	Change R214.2,U15.F20 from ICH_PCIE_WAKE# to EC_SWI#	For wakeup LAN function
		30	Add EC_SWI# and link to both U29.103 to U15.F20	For wakeup LAN function
3/10		22	Change CA18 from 10uF to 0.1uF	For Audio noise
3/16		16	Change L6,L7,L8 to NBQ100505T-800Y_0402	For High speed bead
		19	Change BOM config of C481,C482to 3GGPS@	For 3G/GPS solt
		19	Change BOM Config of C479,C480 to WLAN@	For WLAN/WiMax solt
		29	Change PCB P/N from DAZ08100100 to DAZ08100101	For PCB P/N Change
3/20		29	Del SW3,SW4 with SMT1-05_4P	For debug phase using
		29	Change PCB P/N from DAZ08100101 to DAZ08100103	For PCB P/N Change
3/27		14	Mount C200 with 0.1uF	For EMI request
		20	Mount C292 with 1uF	For EMI request
		29	Change R375 from 300 ohm to 220 ohm	For PWR/B LED light
		30	Mount R422 with 0 ohm	For EMI request

PIR (Product Improve Record)

KAVAA LA-5121P SCHEMATIC CHANGE LIST
REVISION CHANGE: 1.A-->2.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
4/2	16		Reserve C521 with 0.1uf	For EMI request
	17		Reserve C522 with 0.1uf	For EMI request
	17		Reserve C523 and C524 with 0.1uf	For EMI request
	26		Reserve C525 with 0.1uf	For EMI request
	30		Reserve C526 with 0.1uf	For EMI request
	30		Reserve C527 and C528 with 0.1uf	For EMI request
	30		Reserve C529 and C530 with 0.1uf	For EMI request
	30		Reserve C531,C532 and C533 with luf	For EMI request
	19		Add R429 with 100K ohm	For Mini card avoid the single collision problem
	30		Link H15.1 to PJ22.1 and R422.1	For EMI request
4/7	29		Change PCB P/N from DAZ08100103 to DAZ08100105	For PCB P/N Change

OAV10 LA-5122P SCHEMATIC CHANGE LIST
REVISION CHANGE: 2.0-->Buffalo 10BL

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
12/22	5~7		Change CPU to Pine Trail-M	Follow Buffalo 10BL SPEC
	10~13		Change SB to Tigerpoint	Follow Buffalo 10BL SPEC
	08		Follow LA-5841P CLK GEN pin define	For BIOS common design
	11		Follow LA-5841P USB port pin define	For BIOS common design
	11		SLP_CHG_M3/SLP_CHG_M4 will be no used	Buffalo 10BL no support SLP Charge
	12		SLP_CHG# will be no used	Buffalo 10BL no support SLP Charge and need to add R565 pull high to +3V_SB
	17		Remove SLP charge components	Buffalo 10BL no support SLP Charge
	24		Remove G-sensor components	Buffalo 10BL no support G-sensor
	12/27	09	Reserve 0.1u Caps near DDR2 connector	Follow Tempa Bay design
	12/31	08	Delete CLK_48M_CR CLK for Cardreader	Change RTS5159 to RTL8401
12/31	12		Add R610,R611 for HW Board ID function	Add HW board ID for BIOS setting
12/31	16		Add LPC interface signal in WLAN connector	For Mini card debug card can be used
12/31	17		Change USB power switch to RT9715	Follow Tempa Bay design
12/31	21		Change RTL8103EL and RTS5159 to RTL8401 combo chip	
01/05	20		Reserve one 0.1u cap near audio AMP bypass pin	For RF team request.
01/05	15		Change LVDS SCL/SDA pull high resistors to 2.2K	Follow Tempa Bay design
01/06	17		Add 0.1u Caps for each screw holes.	Follow A51 ESD design rule.
01/06	18		Delete Touch screen circuit	Buffalo 10BL won't support this function.
01/06	22		Reserve +3VL power for EC	To solve Buffalo 1.X wireless LAN driver issue.
01/06	22		Add R318,R319 for HW Board ID in EC pin 16.	Add HW board ID for BIOS setting
01/07	23		Delete AC termination for LPC debug port.	Base on EMI's issue list report, they won't need AC termination.
01/07	22		Delete TS_STOP, TS_RST signal.	Buffalo 10BL no support Touch Sreccn.
01/11	22		Reserve R320 0 ohm resistor.	Reserve write protect pin in EC pin17.
01/11	06		Add 0 ohm resistors for XDP signals.	Follow ESD team's desigh rule.
01/11	06		Change R151,R152 to 2.2K.	Follow Intel design guide
01/11	06		Reserve R322 for EC pin 122	Reserve EC_CLK for EC
01/19	5~9		Change DDRII to DDRIII	Follow Buffalo 10BL SPEC
01/25	08		Change CLK Gen to low power chip	For low power consumption design.
01/26	22		Change KBC to E0 version	For cost down plan.
01/28	19		Change audio codec to ALC259	For cost down plan.
02/02	21		Change cardreader to RTS5138	For cost down plan.
02/03	22		Change LAN to RTL8105E	For cost down plan.

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