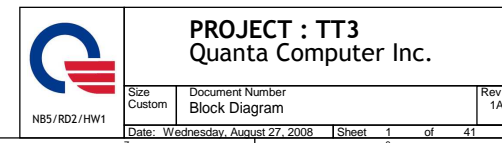


## LAYER 8 : BOT





## INDEX

Pg#	Description	NOTE
1	Schematic Block Diagram	
2	System Information	
3	Power sequence chart	
4	CLOCL GENERATOR	
5-7	AMD CPU S1G2 Griffin	
8-9	DDR II SO-DIMM	
10-13	RS780M	
14-18	SB700	
19	LCD CONNECTOR / LCD PWR / LID	
20	20--CRT,TV_OUT	
21	RTS5158E & CR SOCKET	
22	Azalia ALC268	
23	JACK/AMP_TPA0312	
24	Si3080 and MDC1.5 Connector	
25	Blue Tooth / USBX3 / TPM	
26	RTL8111C/RJ45	
27	LAN Power	
28	NEW CARD/SATA ODD/SATA HDD	
29	LED/KEYBOARD/SW	
30	KB3926/ROM/TP	
31	Mini CARD/Hole	
32	CABLE DOCKING/FAN	
33	3V/5V(MAX1631A)	
34	+1.2V/+1.1V (RT8204)	
35	+CPU_CORE ISL6265	
36	+1.8VSUS/+1.8V/+2.5V	
37	+1.1V/+1.2V_S5/+1.5V	
38	DISCHARGE	
39	Charger (ISL6251)	

\* --> Un-stuff (ex. \*1K/04)  
 04-- 0402 footprint  
 06-- 0603 footprint  
 08-- 0805 footprint  
 12-- 1206 footprint  
 F-- 1% tolerance

## Power &amp; Ground

Label	ACTIVE	Description	Control Signal
+VIN	S0, S3, S4, S5	AC ADAPTER (18.5V)	
+BATT	S0, S3, S4, S5	MAIN BATTERY + (6.2V-8.4V)	
+AVBAT	S0, S3, S4, S5	RTC & KBC POWER (3.3V)	
+12VALW	S0, S3, S4, S5	+12V	
+VCORE	S0	CPU CORE POWER (0.375-1.5V)	VRON
+CPUVDDNB	S0	CPU CORE POWER (1.375-1.5V)	VRON
+1.1V_NB	S0	+1.1 to +1.0 DYN	VRON
+1.1V	S0	+1.1V	VRON
+1.2VS5	S0, S3, S4, S5		S5_ON
+1.2V	S0	+1.2V	VRON
+3V	S0		MAINON
+3VSUS	S0, S3		SUSON
+3VS5	S0, S3, S4, S5		S5_ON
+3VPCU	S0, S3, S4, S5	ALWAYS POWER (3V)	
+5V	S0		MAIND
+5VSUS	S0, S3		SUSON
+5VPCU	S0, S3, S4, S5	ALWAYS POWER (5V)	
+1.5V	S0		MAIND
+1.8VSUS	S0, S3	DDR CORE POWER	SUSON
+1.8V	S0		MAINON
+2.5V	S0	CPU VDDA	VR2.5_ON
+0.9VSMVTT	S0	DDR COMMAND & CONTROL PULL UP POWER	MAINON
+0.9VSMVREF_DIMM	S0, S3	DDR REF POWER	SUSON
+AVDD	S0	AUDIO ANALOG POWER (5V)	MAINON
+3VLAVCC	S0, S3, S4, S5	LAN Power	LAN_ON
 GND	ALL PAGES	DIGITAL GROUND	
 AGND		AUDIO GND	

SMBUS	SMBUS function define
SMBCLK0 SMBDAT0	DDR / DDR THER / CLOCK GEN (+3V)
SMBCLK1 SMBDAT1	Mini Card (+3VS5)
SMBCLK2 SMBDAT2	New CARD (+3VS5)



NB5/RD2/HW1

**PROJECT : TT3**  
**Quanta Computer Inc.**

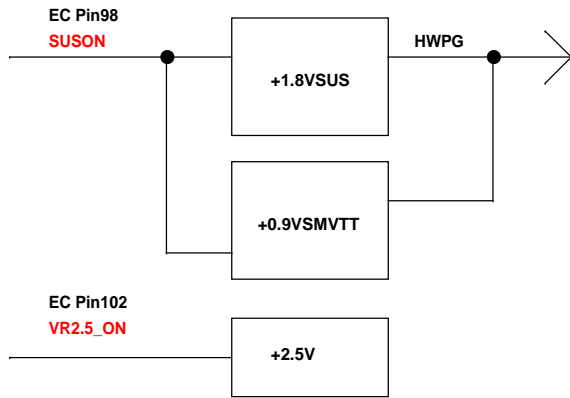
Size  
CustomDocument Number  
System InformationRev  
1A

Date: Wednesday, August 27, 2008 Sheet 2 of 41

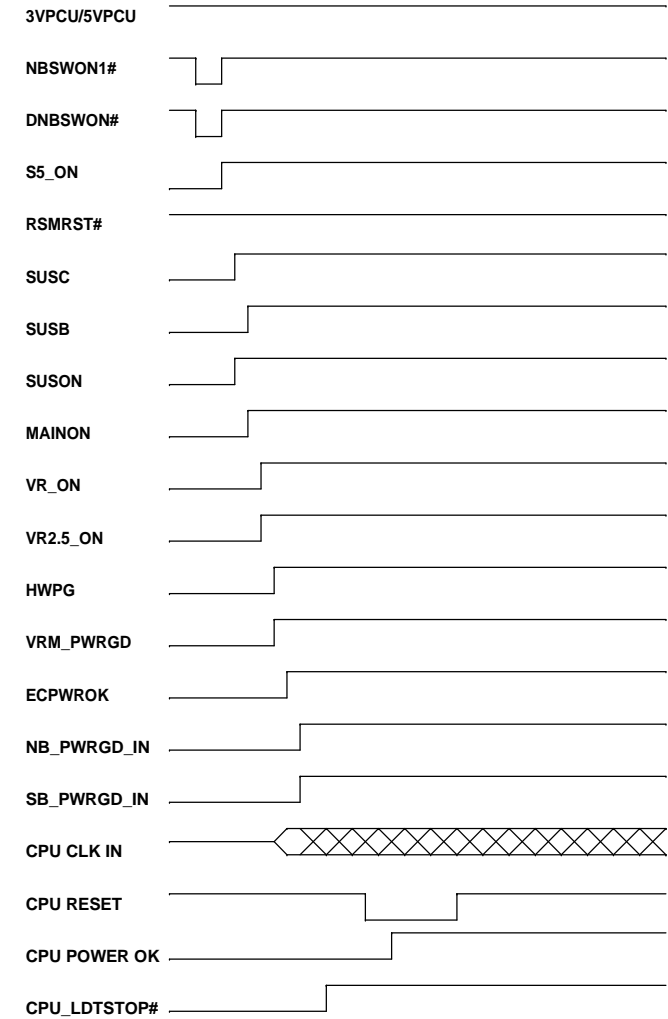
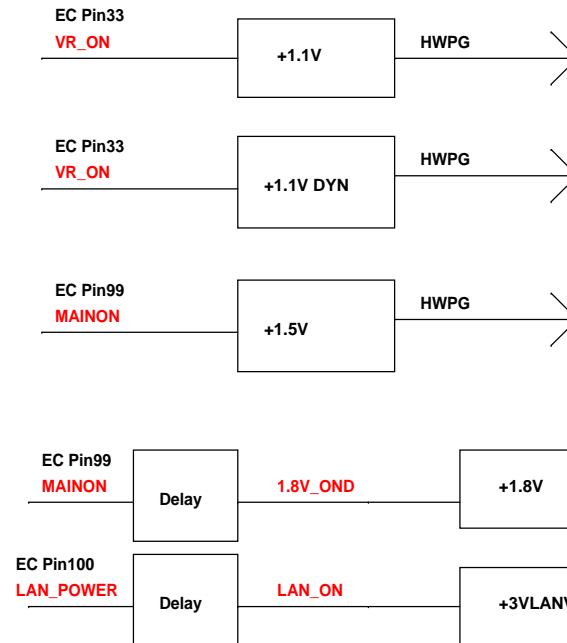
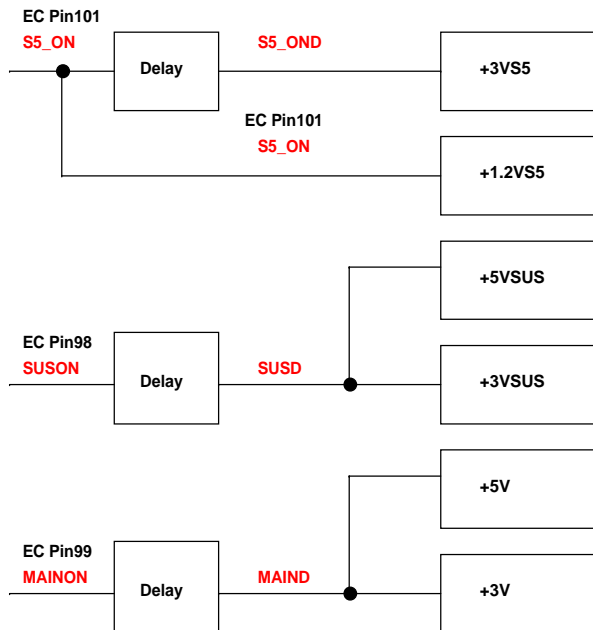
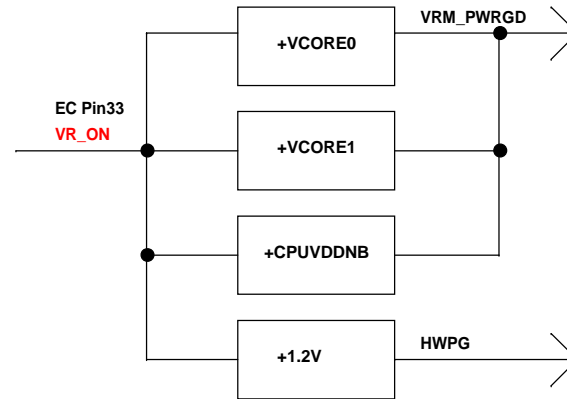
02



### CPU Power Group A



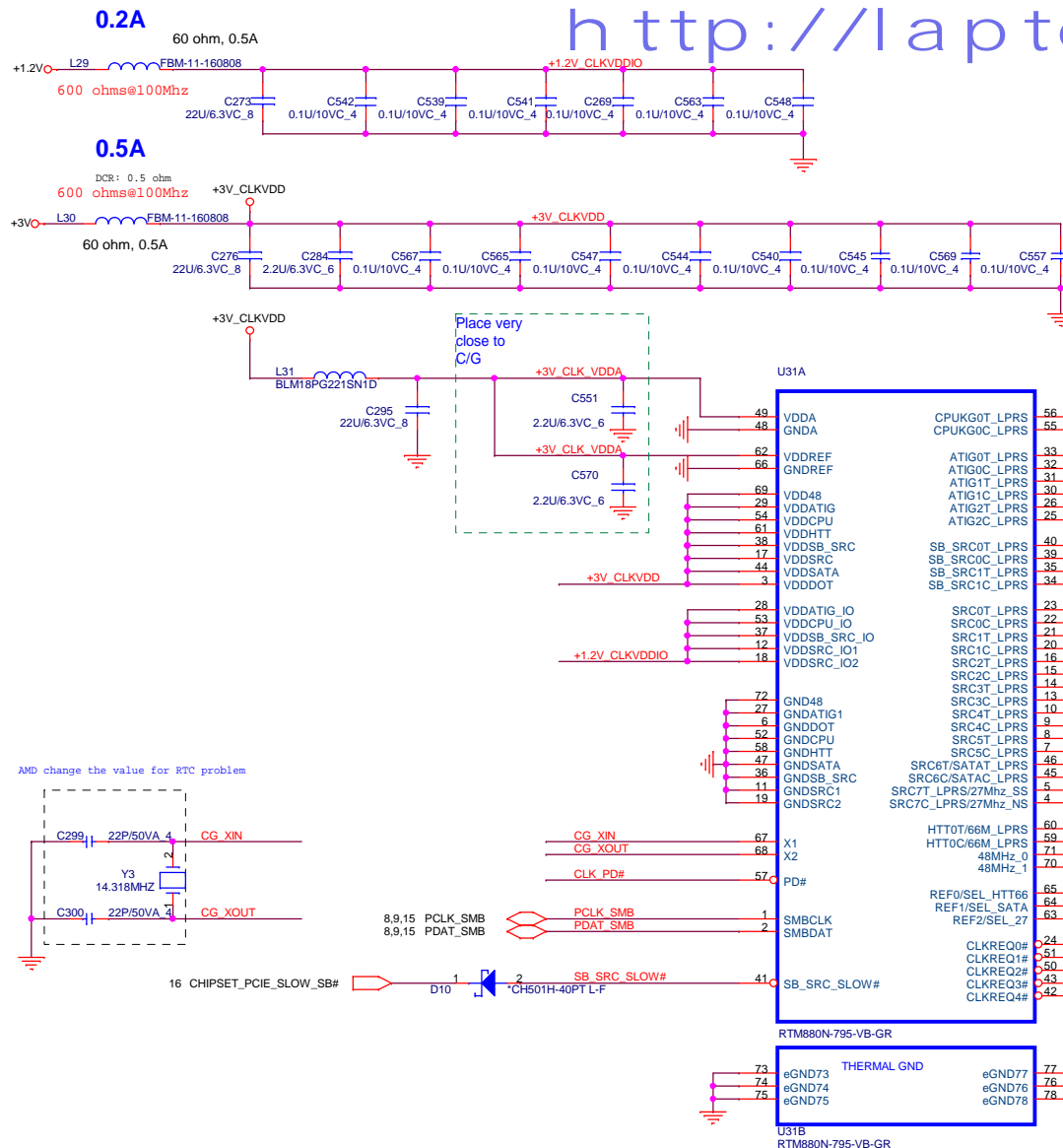
### CPU Power Group B





NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.



AMD change the value for RTC problem

Place within 0.5" of CLKGEN

EMI request

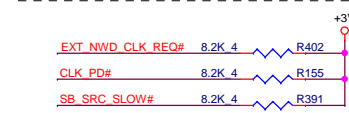
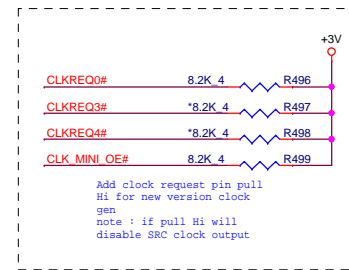
Wrong type bios can not write

when driven low SB\_SRC clocks slow only supported with to reduced setpoint custom CG IC

\* RS780 can be used as clock buffer to output two PCIe reference clocks  
By default, chip will configured as input mode, BIOS can program it to output mode.

\* default

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27	1*	27MHz non-spreading singled clock
	0	100 MHz spreading differential SRC clock



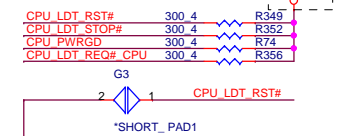
PROJECT : TT3  
Quanta Computer Inc.

Size Custom	Document Number Clock generator	Rev 1A
Date: Wednesday, August 27, 2008	Sheet 4	of 41





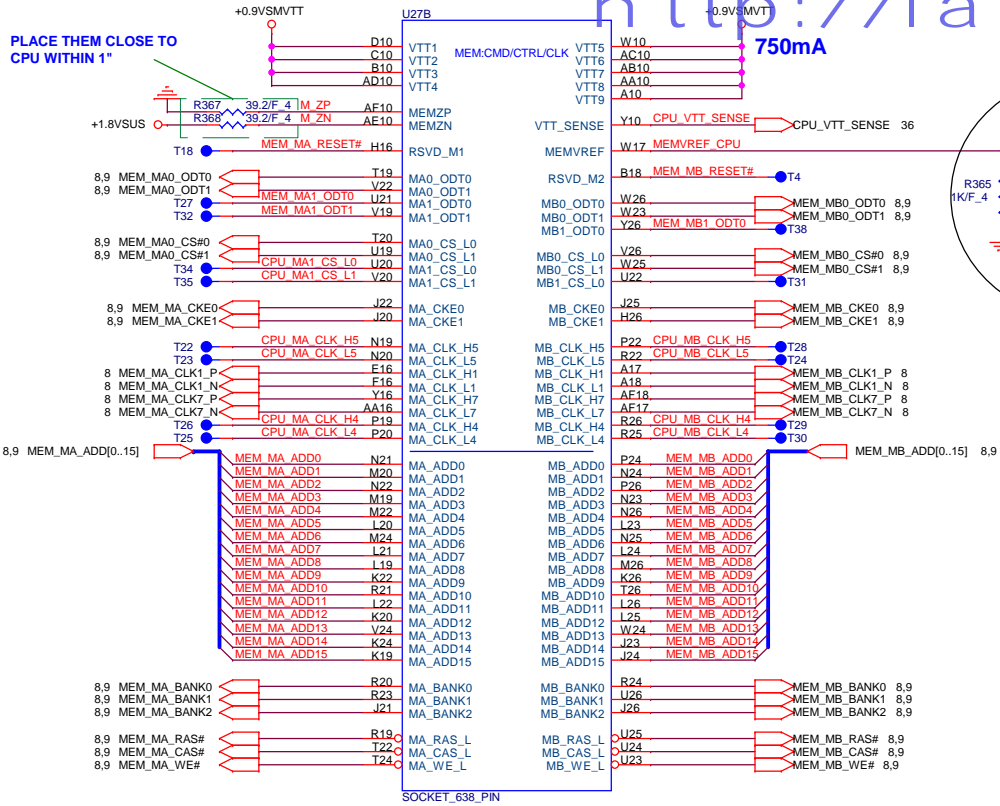
AMD use +1.8V



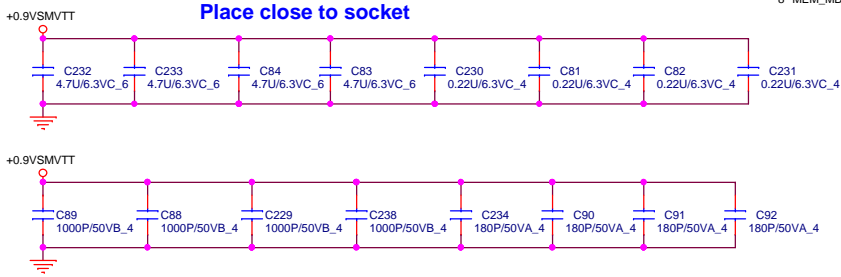
Size Custom	Document Number S1G2 HT,CTL I/F 1/3	Rev 1A
Date: Wednesday, August 27, 2008	Sheet 5 of 41	



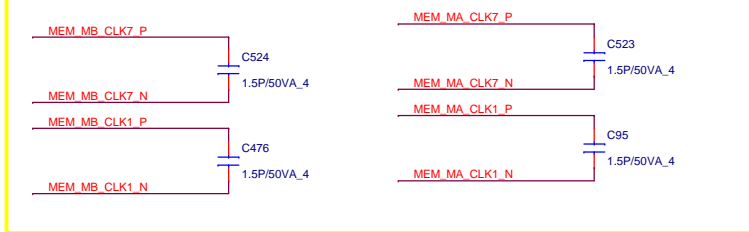
PLACE THEM CLOSE TO CPU WITHIN 1"



Place close to socket



Close to CPU within 1500 mils



+0.9VSMVTT 9,31,36  
+1.8VSUS 5,7,8,9,31,35,36,37

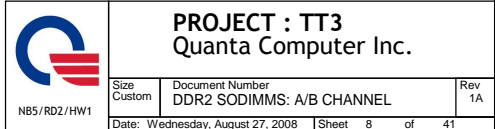


PROJECT : TT3  
Quanta Computer Inc.











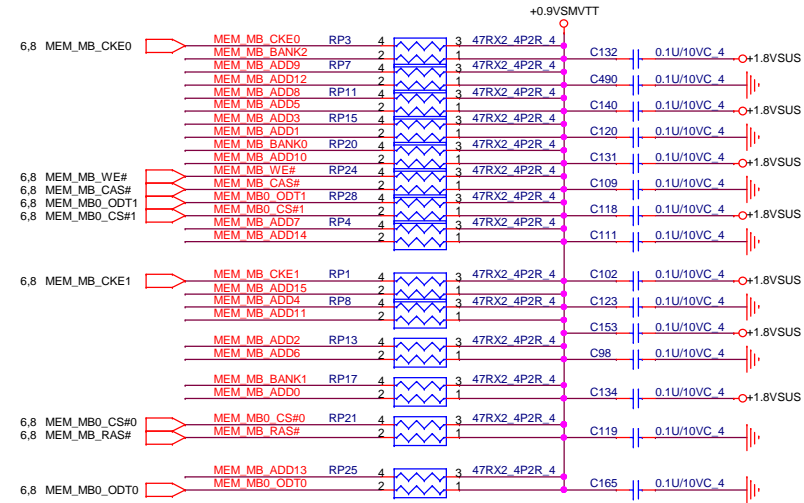
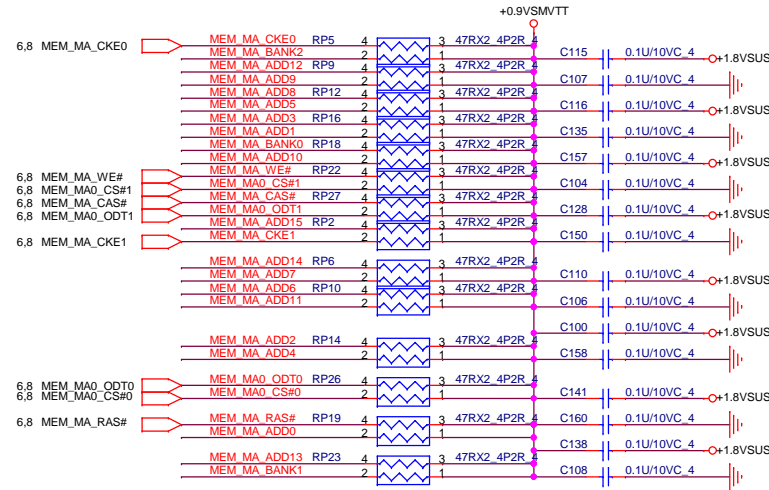
6,8 MEM\_MA\_ADD[0..15]  
6,8 MEM\_MA\_BANK[0..2]

MEM\_MA\_ADD[0..15]  
MEM\_MA\_BANK[0..2]

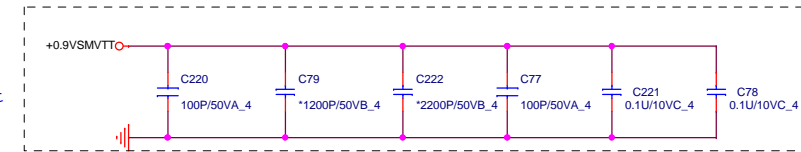
6,8 MEM\_MB\_ADD[0..15]  
6,8 MEM\_MB\_BANK[0..2]

MEM\_MB\_ADD[0..15]  
MEM\_MB\_BANK[0..2]

09



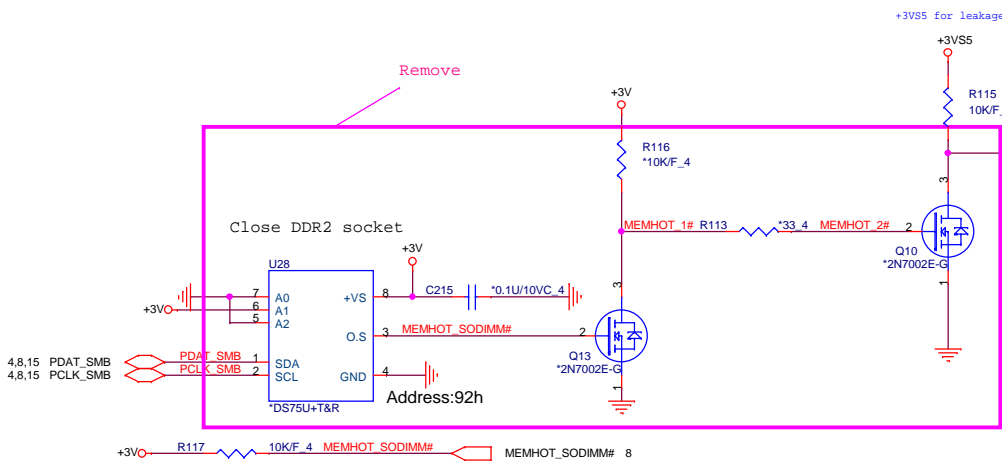
Emi request



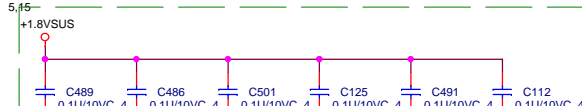
PLACE CLOSE TO PROCESSOR  
WITHIN 1.5 INCH



PLACE CLOSE TO PROCESSOR  
WITHIN 1.5 INCH



PLACE CLOSE TO SOCKET( PER EMI/EMC)



PLACE CLOSE TO SOCKET( PER EMI/EMC)



+0.9VSMVTT 6,31,36  
+1.8VSUS 5,6,7,8,31,35,36,37  
+3V 4,5,7,8,12,13,14,15,16,17,18,19,20,22,23,26,28,29,30,31,33,34,38



PROJECT : TT3  
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
DDR2 SODIMMS TERMINATIONS		
Date: Wednesday, August 27, 2008	Sheet 9 of 41	



HT_CPU_NB_CAD_H0	Y25	HT_RXCAD0P	D24	HT_NB_CPU_CAD_H0	D24
HT_CPU_NB_CAD_L0	Y24	HT_RXCAD0N	D25	HT_NB_CPU_CAD_L0	D25
HT_CPU_NB_CAD_H1	Y22	HT_RXCAD1P	E24	HT_NB_CPU_CAD_H1	E24
HT_CPU_NB_CAD_L1	V23	HT_RXCAD1N	E25	HT_NB_CPU_CAD_L1	E25
HT_CPU_NB_CAD_H2	V25	HT_RXCAD2P	E24	HT_NB_CPU_CAD_H2	E24
HT_CPU_NB_CAD_L2	V24	HT_RXCAD2N	E25	HT_NB_CPU_CAD_L2	E25
HT_CPU_NB_CAD_H3	U24	HT_RXCAD3P	F23	HT_NB_CPU_CAD_H3	F23
HT_CPU_NB_CAD_L3	U25	HT_RXCAD3N	F22	HT_NB_CPU_CAD_L3	F22
HT_CPU_NB_CAD_H4	T25	HT_RXCAD4P	H23	HT_NB_CPU_CAD_H4	H23
HT_CPU_NB_CAD_L4	T24	HT_RXCAD4N	H22	HT_NB_CPU_CAD_L4	H22
HT_CPU_NB_CAD_H5	P22	HT_RXCAD5P	J25	HT_NB_CPU_CAD_H5	J25
HT_CPU_NB_CAD_L5	P23	HT_RXCAD5N	J24	HT_NB_CPU_CAD_L5	J24
HT_CPU_NB_CAD_H6	P25	HT_RXCAD6P	K24	HT_NB_CPU_CAD_H6	K24
HT_CPU_NB_CAD_L6	P24	HT_RXCAD6N	K25	HT_NB_CPU_CAD_L6	K25
HT_CPU_NB_CAD_H7	N24	HT_RXCAD7P	K23	HT_NB_CPU_CAD_H7	K23
HT_CPU_NB_CAD_L7	N25	HT_RXCAD7N	K22	HT_NB_CPU_CAD_L7	K22

HT_CPU_NB_CAD_H8	AC24	HT_RXCAD8P	F21	HT_NB_CPU_CAD_H8	F21
HT_CPU_NB_CAD_L8	AC25	HT_RXCAD8N	G21	HT_NB_CPU_CAD_L8	G21
HT_CPU_NB_CAD_H9	AB25	HT_RXCAD9P	G20	HT_NB_CPU_CAD_H9	G20
HT_CPU_NB_CAD_L9	AB24	HT_RXCAD9N	I21	HT_NB_CPU_CAD_L9	I21
HT_CPU_NB_CAD_H10	AA24	HT_RXCAD10P	J21	HT_NB_CPU_CAD_H10	J21
HT_CPU_NB_CAD_L10	AA25	HT_RXCAD10N	J18	HT_NB_CPU_CAD_L10	J18
HT_CPU_NB_CAD_H11	Y22	HT_RXCAD11P	K17	HT_NB_CPU_CAD_H11	K17
HT_CPU_NB_CAD_L11	Y23	HT_RXCAD11N	L19	HT_NB_CPU_CAD_L11	L19
HT_CPU_NB_CAD_H12	W21	HT_RXCAD12P	M19	HT_NB_CPU_CAD_H12	M19
HT_CPU_NB_CAD_L12	W20	HT_RXCAD12N	L18	HT_NB_CPU_CAD_L12	L18
HT_CPU_NB_CAD_H13	V21	HT_RXCAD13P	M21	HT_NB_CPU_CAD_H13	M21
HT_CPU_NB_CAD_L13	V20	HT_RXCAD13N	P21	HT_NB_CPU_CAD_L13	P21
HT_CPU_NB_CAD_H14	U20	HT_RXCAD14P	P18	HT_NB_CPU_CAD_H14	P18
HT_CPU_NB_CAD_L14	U21	HT_RXCAD14N	M18	HT_NB_CPU_CAD_L14	M18
HT_CPU_NB_CAD_H15	U19	HT_RXCAD15P			
HT_CPU_NB_CAD_L15	U18	HT_RXCAD15N			

HT_CPU_NB_CLK_H0	T22	HT_RXCLK0P	H24	HT_NB_CPU_CLK_H0	H24
HT_CPU_NB_CLK_L0	T23	HT_RXCLK0N	H25	HT_NB_CPU_CLK_L0	H25
HT_CPU_NB_CLK_H1	AB23	HT_RXCLK1P	L21	HT_NB_CPU_CLK_H1	L21
HT_CPU_NB_CLK_L1	AA22	HT_RXCLK1N	L20	HT_NB_CPU_CLK_L1	L20

HT_CPU_NB_CTL_H0	M22	HT_RXCTL0P	M24	HT_NB_CPU_CTL_H0	M24
HT_CPU_NB_CTL_L0	M23	HT_RXCTL0N	M25	HT_NB_CPU_CTL_L0	M25
HT_CPU_NB_CTL_H1	R21	HT_RXCTL1P	P19	HT_NB_CPU_CTL_H1	P19
HT_CPU_NB_CTL_L1	R20	HT_RXCTL1N	R18	HT_NB_CPU_CTL_L1	R18

HT_RXCALP	C23	HT_TXCALP	B24	HT_TXCALN	B25
HT_RXCALN	A24	HT_TXCALN			

HT_RXCALP	C23	HT_TXCALP	B24	HT_TXCALN	B25
HT_RXCALN	A24	HT_TXCALN			

HT_RXCALP	C23	HT_TXCALP	B24	HT_TXCALN	B25
HT_RXCALN	A24	HT_TXCALN			

HT_RXCALP	C23	HT_TXCALP	B24	HT_TXCALN	B25
HT_RXCALN	A24	HT_TXCALN			

HT_RXCALP	C23	HT_TXCALP	B24	HT_TXCALN	B25
HT_RXCALN	A24	HT_TXCALN			

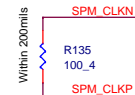
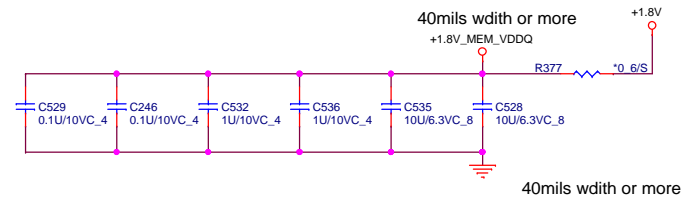
HT_RXCALP	C23	HT_TXCALP	B24	HT_TXCALN	B25
HT_RXCALN	A24	HT_TXCALN			

HT_RXCALP	C23	HT_TXCALP	B24	HT_TXCALN	B25
HT_RXCALN	A24	HT_TXCALN			

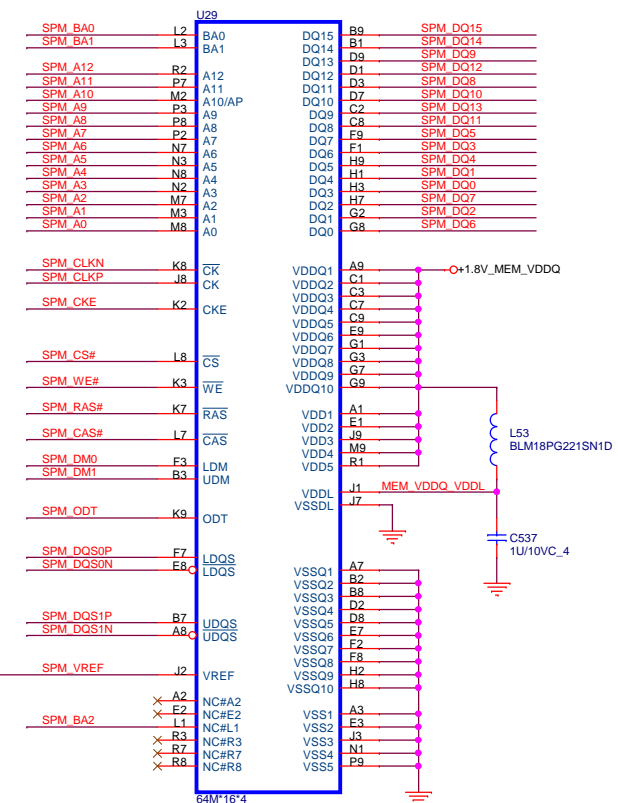
HT_RXCALP	C23	HT_TXCALP	B24	HT_TXCALN	B25
HT_RXCALN	A24	HT_TXCALN			

follow AMD  
check list to  
change part  
number 300 ohm  
to 301 ohm

HT_CPU_NB_CAD_H15_0	5	HT_CPU_NB_CAD_L15_0	5
HT_CPU_NB_CLK_H1_0	5	HT_CPU_NB_CLK_L1_0	5
HT_CPU_NB_CTL_H1_0	5	HT_CPU_NB_CTL_L1_0	5
HT_NB_CPU_CAD_H15_0	5	HT_NB_CPU_CAD_L15_0	5
HT_NB_CPU_CLK_H1_0	5	HT_NB_CPU_CLK_L1_0	5
HT_NB_CPU_CTL_H1_0	5	HT_NB_CPU_CTL_L1_0	5

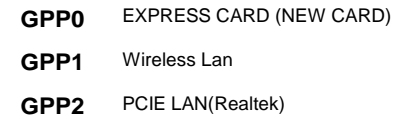


Close to U23



PROJECT : TT3  
Quanta Computer Inc.





Size B	Document Number RS780M-PCIE I/F 2/4	Rev 1A
Date: Wednesday, August 27, 2008		Sheet 11 of 41



Enables the Test Debug Bus using GPIO.

0 : Enable  
1 : Disable  
(RS780 use VSYNC#)

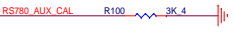


Enables Side port memory

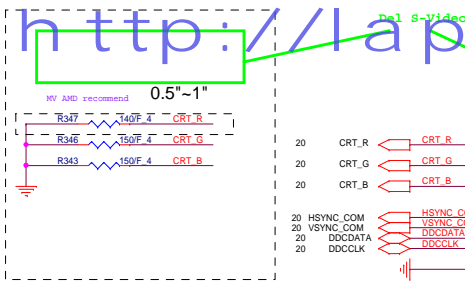
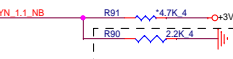
0 : Enable (RS780)  
1 : Disable (RS780)  
( RS780 use HSYNC#)



default values if not connected  
RS780:SUS\_STAT



AUX CAL Value need update



As output to the voltage  
regulator for PWM of  
RS780M core voltage.

PART 3 OF 6

CRT/OUT

PLL PWR

PM

CLOCKS

MIS.

TESTMODE

TESTMODE

TESTMODE

TESTMODE

TESTMODE

TESTMODE

TESTMODE

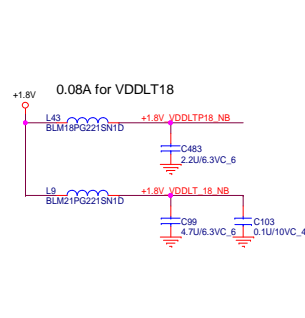
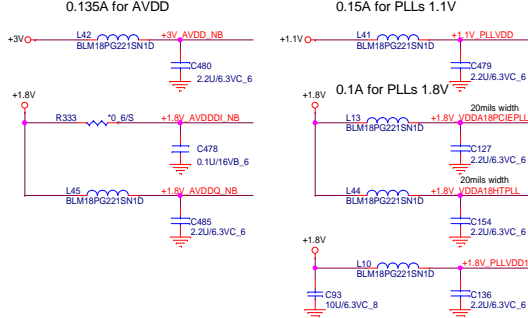
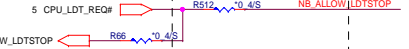
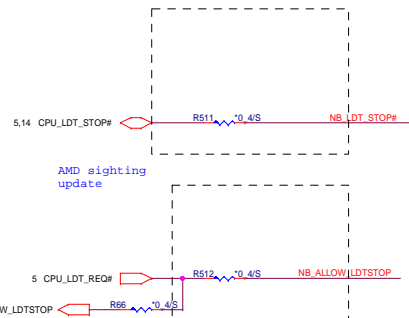
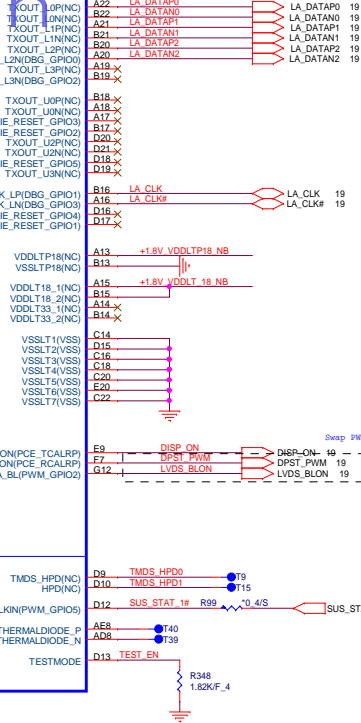
TESTMODE

TESTMODE

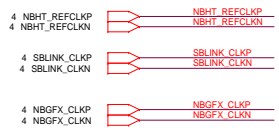
TESTMODE

TESTMODE

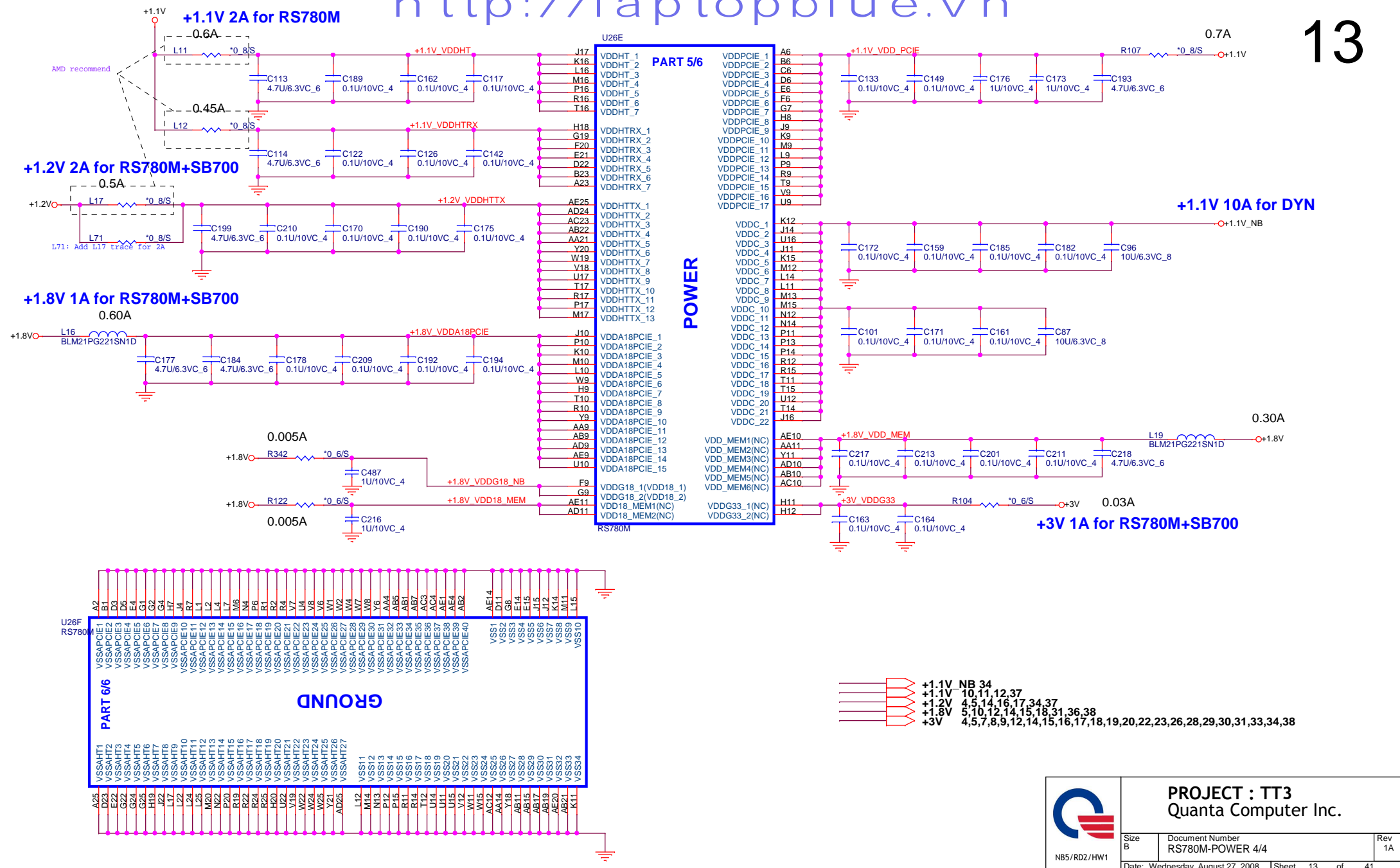
TESTMODE



+1.1V 10,11,13,37  
+1.8V 5,10,13,14,15,18,31,36,38  
+3V 4,5,7,8,9,13,14,15,16,17,18,19,20,22,23,26,28,29,30,31,33,34,38  
+12VALW 19,28,31,33,38



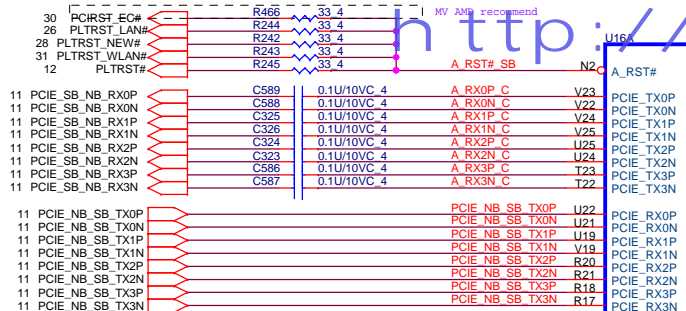




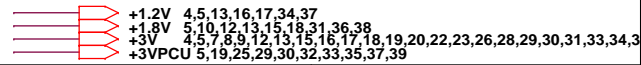
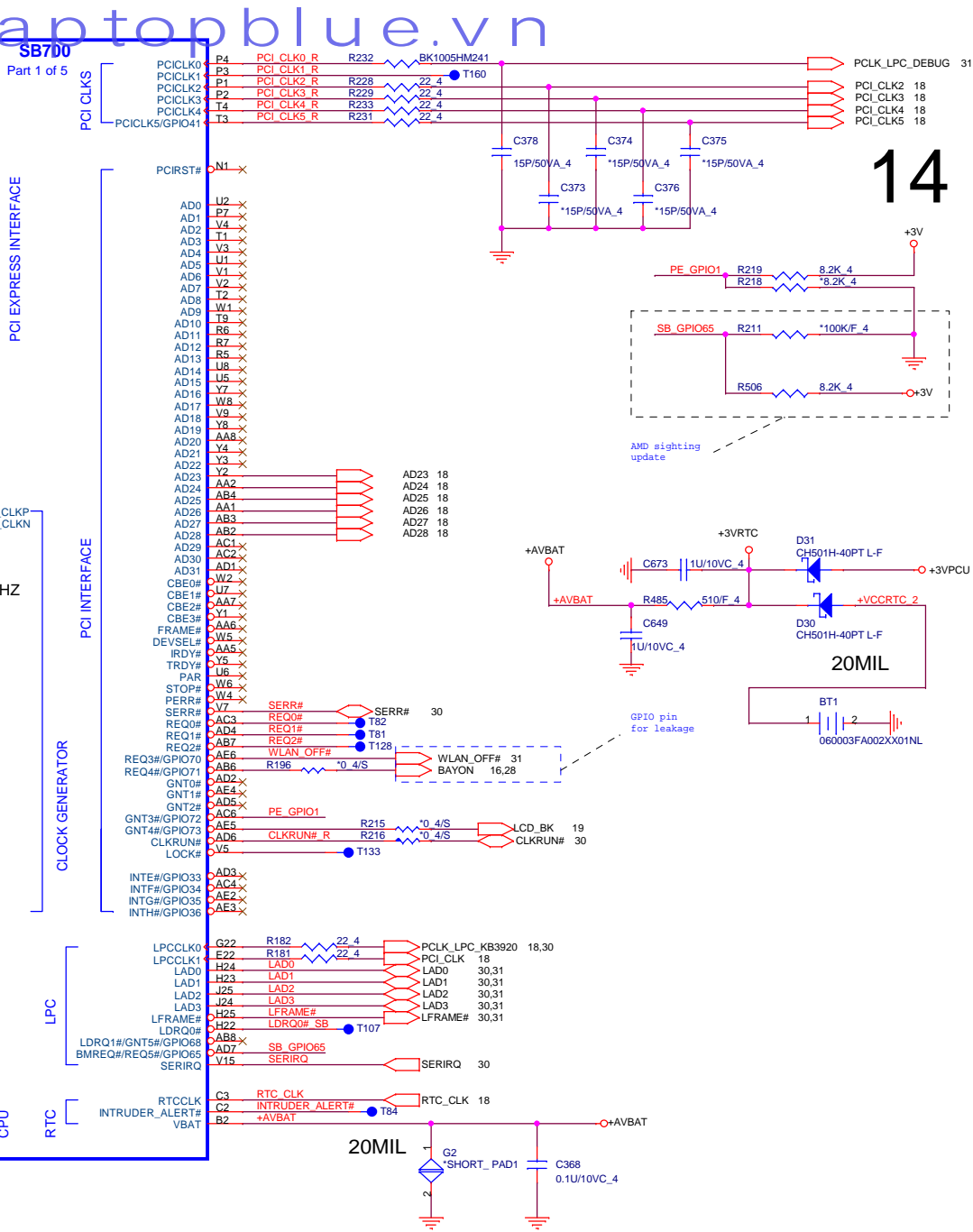
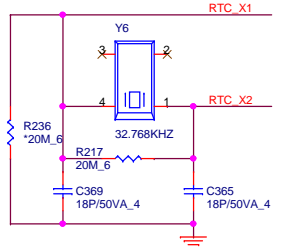
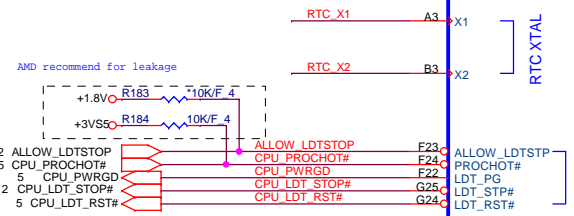
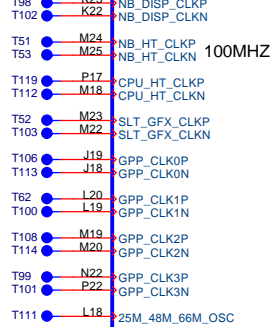
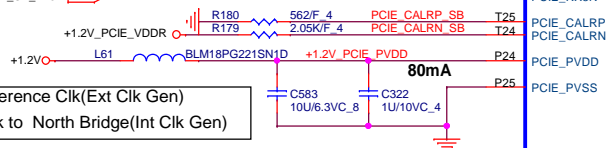
**PROJECT : TT3**  
Quanta Computer Inc.

Size B	Document Number RS780M-POWER 4/4	Rev 1A
Date: Wednesday, August 27, 2008	Sheet 13	of 41





- |  |
|--|
| 1.PCIE Reference Clk(Ext Clk Gen)          |
| 2. A-link Clk to North Bridge(Int Clk Gen) |



**PROJECT : TT3**  
Quanta Computer Inc.

Size Custom	Document Number SB700-PCIE/PCI/CPU/LPC 1/4	Rev 1A
Date: Wednesday, August 27, 2008		Sheet 14 of 41









PLACE SATA AC COUPLING  
CAPS CLOSE TO SB600

http://laptopblue.vn

16

## SATA1

28 SATA\_TXP0  
28 SATA\_TXN0

C353 0.01U/16VB 4  
C356 0.01U/16VB 4

SATA\_TXP0 C  
SATA\_TXN0 C

## SATA ODD

28 SATA\_RXP0  
28 SATA\_RXN0

C641 0.01U/16VB 4  
C639 0.01U/16VB 4

SATA\_RXP0 C  
SATA\_RXN0 C

28 SATA\_TXP1  
28 SATA\_TXN1

C351 0.01U/16VB 4  
C349 0.01U/16VB 4

SATA\_TXP1 C  
SATA\_TXN1 C

28 SATA\_RXN1  
28 SATA\_RXP1

C345 0.01U/16VB 4  
C346 0.01U/16VB 4

SATA\_RXN1 C  
SATA\_RXP1 C

## SB700

Part 2 of 5

SERIAL ATA

SATA PWR

HW MONITOR

ATA 66/100/133

SPI ROM

HW MONITOR

IDE\_IORDY#  
IDE\_IRQ#  
IDE\_A0  
IDE\_A1  
IDE\_A2  
IDE\_DACK#  
IDE\_DRQ#  
IDE\_IOR#  
IDE\_IOW#  
IDE\_CS1#  
IDE\_CS3#

IDE\_D0/GPIO15  
IDE\_D1/GPIO16  
IDE\_D2/GPIO17  
IDE\_D3/GPIO18  
IDE\_D4/GPIO19  
IDE\_D5/GPIO20  
IDE\_D6/GPIO21  
IDE\_D7/GPIO22  
IDE\_D8/GPIO23  
IDE\_D9/GPIO24  
IDE\_D10/GPIO25  
IDE\_D11/GPIO26  
IDE\_D12/GPIO27  
IDE\_D13/GPIO28  
IDE\_D14/GPIO29  
IDE\_D15/GPIO30

IF THERE IS NO IDE, TEST  
POINTS FOR DEBUG BUS  
IS MANDATORY

SPI\_DI/GPIO12  
SPI\_DO/GPIO11  
SPI\_CLK/GPIO47  
SPI\_HOLD#/GPIO31  
SPI\_CS#/GPIO32

LAN\_RST#/GPIO13  
ROM\_RST#/GPIO14

FANOUT0/GPIO3  
FANOUT1/GPIO48  
FANOUT2/GPIO49

FANIN0/GPIO50  
FANIN1/GPIO51  
FANIN2/GPIO52

TEMP\_COMM  
TEMPIN0/GPIO61  
TEMPIN1/GPIO62  
TEMPIN2/GPIO63  
TEMPIN3/TALERT#/GPIO64

VIN0/GPIO53  
VIN1/GPIO54  
VIN2/GPIO55  
VIN3/GPIO56  
VIN4/GPIO57  
VIN5/GPIO58  
VIN6/GPIO59  
VIN7/GPIO60

AVDD  
AVSS

BT\_OFF# 25  
CHIPSET\_PCIE\_SLOW\_SB# 4

BT\_COMBO\_EN# 31  
AMPBEEP\_EN 23

BOARDID0  
BOARDID1  
BOARDID2

fix leakage

5mA

+3V VDD\_HWM L67

+3V VDD\_HWM L67

+3V VDD\_HWM L67

+3V VDD\_HWM L67

+3V VDD\_HWM L67

+3V VDD\_HWM L67

+3V VDD\_HWM L67

+3V VDD\_HWM L67

+3V VDD\_HWM L67

+3V VDD\_HWM L67

+3V VDD\_HWM L67

+3V VDD\_HWM L67

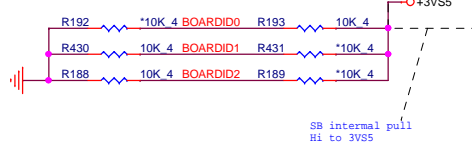
+3V VDD\_HWM L67

+3V VDD\_HWM L67

VRAM / Clock Gen	Samsung Realtek	Qimonda ICS	Hynix Silego
Board ID	(0.0.0)	(1.0.0)	(0.1.0)
BOARDID0	R192 Stuff	R193 Stuff	R192 Stuff
BOARDID1	R430 Stuff	R430 Stuff	R431 Stuff
BOARDID2	R188 Stuff	R188 Stuff	R188 Stuff

## DB2 MODIFY

## SYS BOARD ID

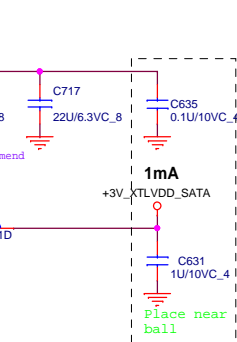
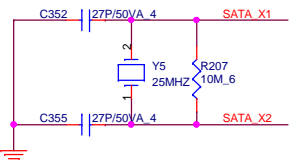
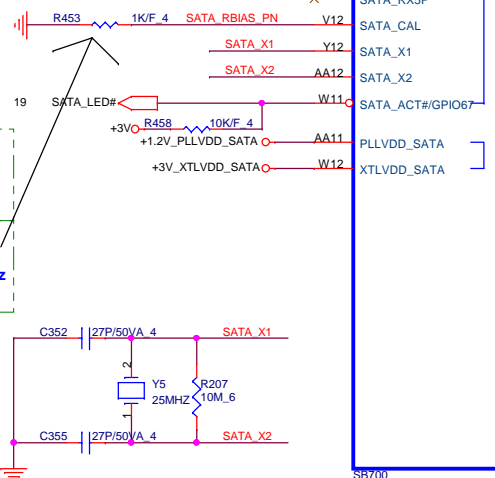


SB internal pull  
Hi to 3V55



PLACE SATA CAL  
RES VERY CLOSE  
TO BALL OF U600

NOTE:  
R635 IS 1K 1% FOR 25MHz  
XTAL, 4.99K 1% FOR 100MHz  
INTERNAL CLOCK



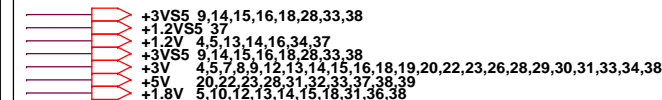
+1.2V 4,5,13,14,17,34,37  
+3V 4,5,7,8,9,12,13,14,15,17,18,19,20,22,23,26,28,29,30,31,33,34,38



PROJECT : TT3  
Quanta Computer Inc.

Size Custom	Document Number SB700-SATA/IDE/HWM/SPI 3/4	Rev 1A
Date: Wednesday, August 27, 2008	Sheet 16 of 41	

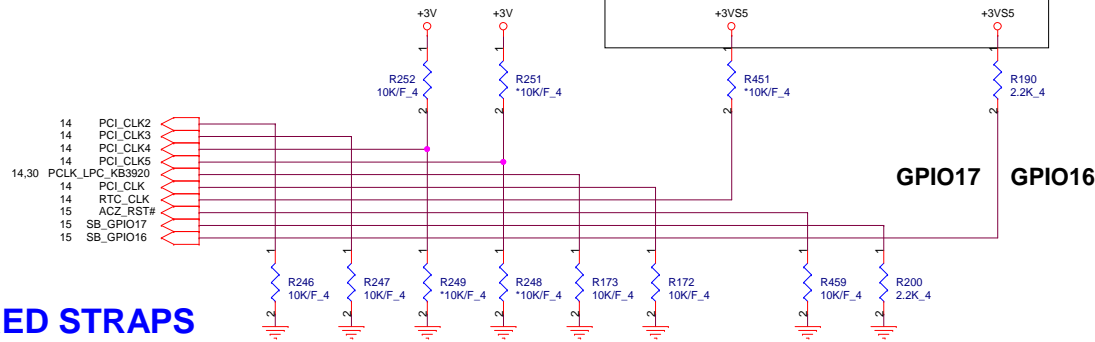






NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC\_CLK

It must ready before RSMRST#



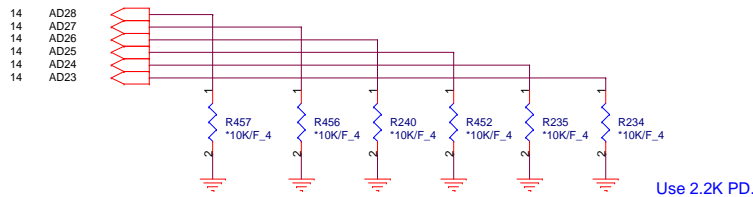
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

## REQUIRED STRAPS

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	PCLK_LPC_KB3920	PCI_CLK	RTC_CLK	AZ_RST#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	EC ENABLED	CLKGEN ENABLED	INTERNAL RTC	ENABLE PCI MEM BOOT	ROM TYPE: H, H = Reserved  H, L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI MEM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM	DEFAULT

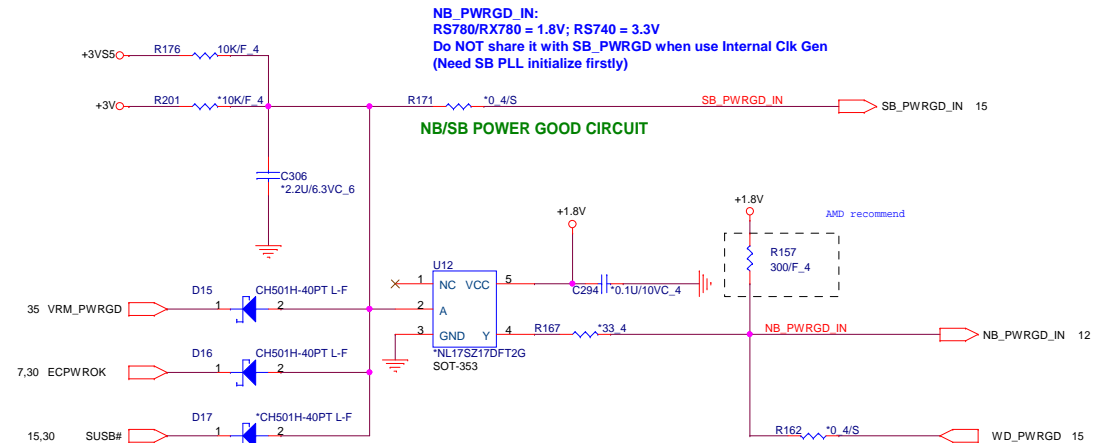
## DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI\_AD[28:23]



Use 2.2K PD.

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353  
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5

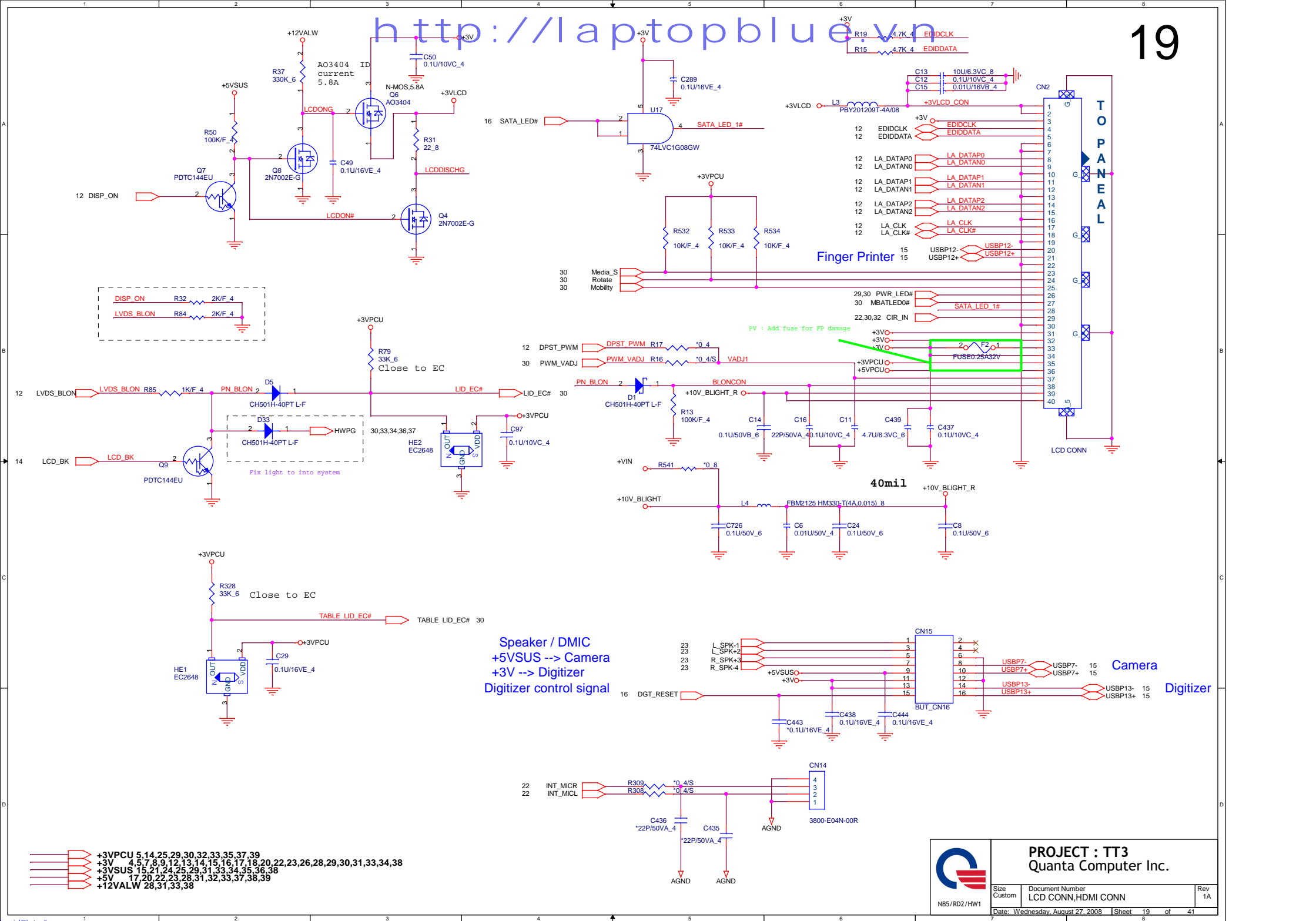


PROJECT : TT3  
Quanta Computer Inc.

Size Custom Document Number SB700-STRAPS.PWRGD Rev 1A  
Date: Wednesday, August 27, 2008 Sheet 18 of 41

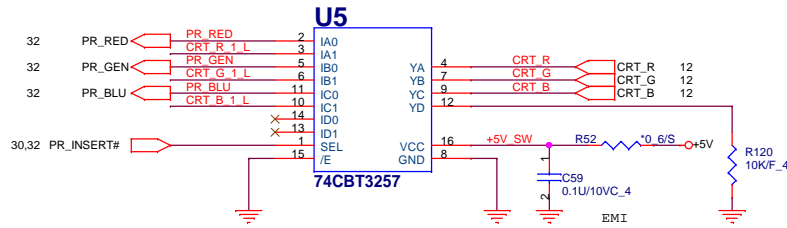
+1.8V 5,10,12,13,14,15,31,36,38  
+3V 4,5,7,8,9,12,13,14,15,16,17,19,20,22,23,26,28,29,30,31,33,34,38  
+3VS5 9,14,15,16,17,28,33,38





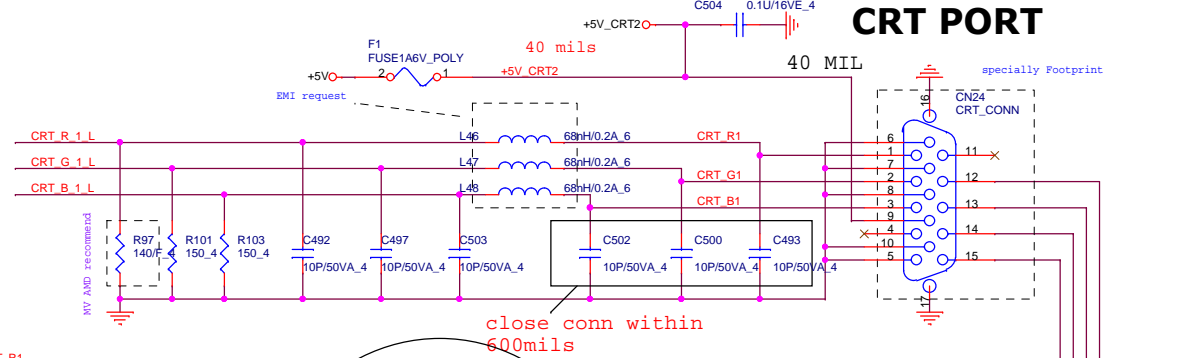


# CRT SWITCH

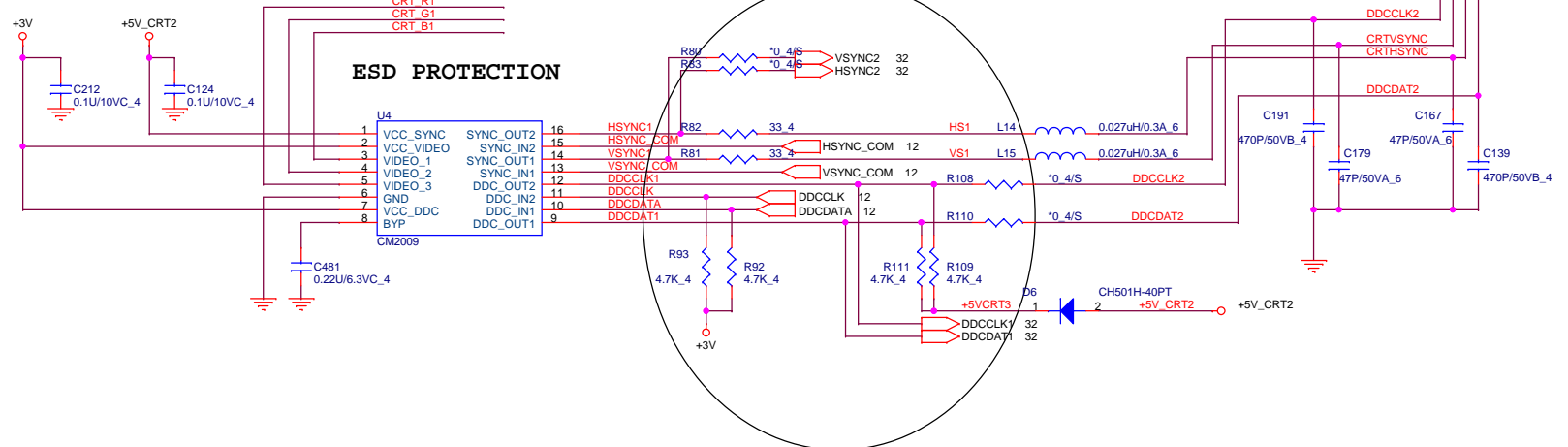


inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

# CRT PORT



# ESD PROTECTION



Del S-Video

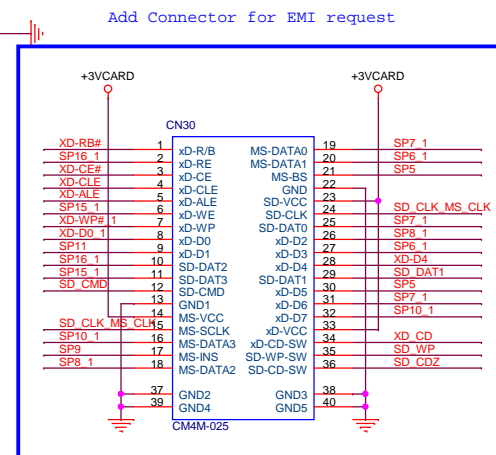
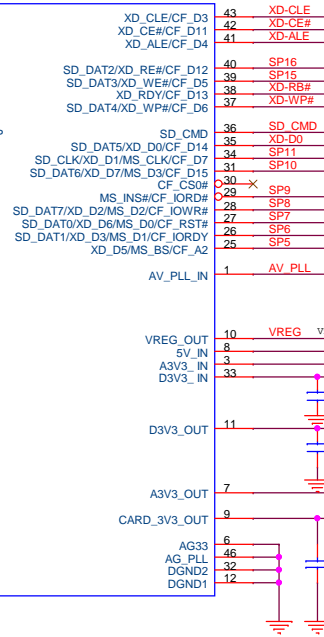
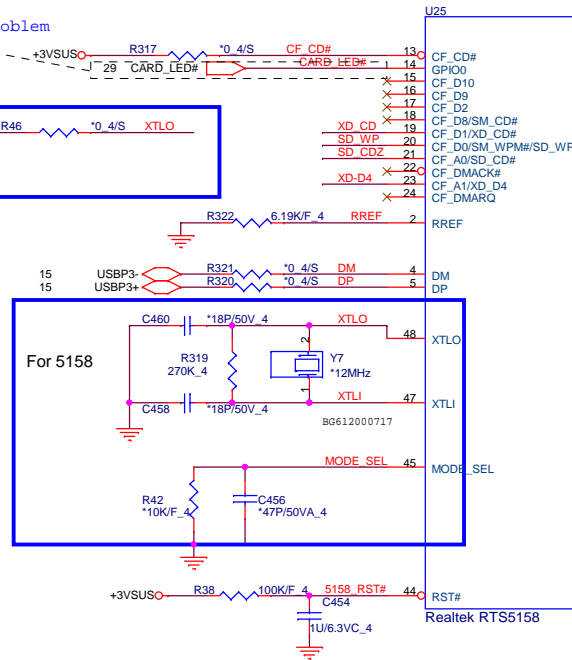
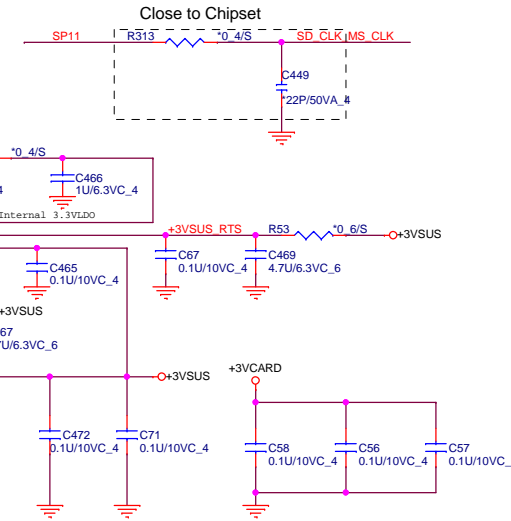


+3V +5V 4,5,7,8,9,12,13,14,15,16,17,18,19,22,23,26,28,29,30,31,33,34,38 17,22,23,28,31,32,33,37,38,39



	SD/MMC	MS	XD
SP0			
SP1			XD CD#
SP2	SD WP		
SP3	SD CD#		
SP4			XD D4
SP5		MS BS	XD D5
SP6		MS D1	XD D3
SP7	SD DAT0	MS D0	XD D6
SP8	SD DAT7	MS D2	XD D2
SP9		MS INS#	
SP10	SD DAT6	MS D3	XD D7
SP11	SD CLK	MS SCLK	XD D1
SP12	SD DAT5		XD D0
SP13	SD DAT4		XD WP#
SP14			XD R/B#
SP15	SD DAT3		XD WE#
SP16	SD DAT2		XD RE#
SP17			XD ALE
SP18			XD CE#
SP19			XD LE

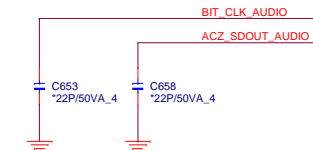
Size Custom	Document Number RT5158 CARD READER CONTROLLER	Rev 1A
Date: Wednesday, August 27, 2008		Sheet 21 of 41







### Add Connector for EMI request

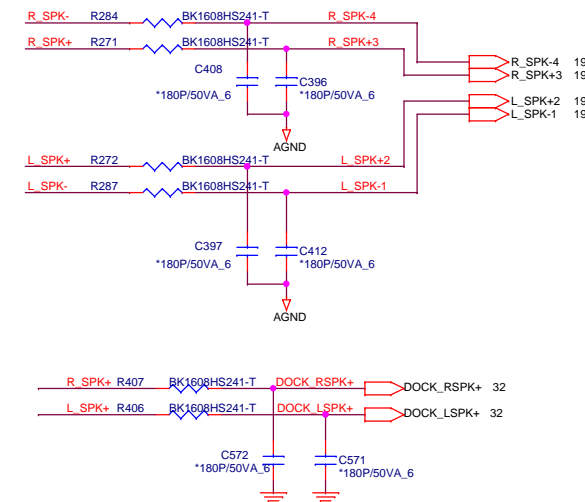
➤ +3VSUS 15,24,25,29,31,33,34,35,36,38





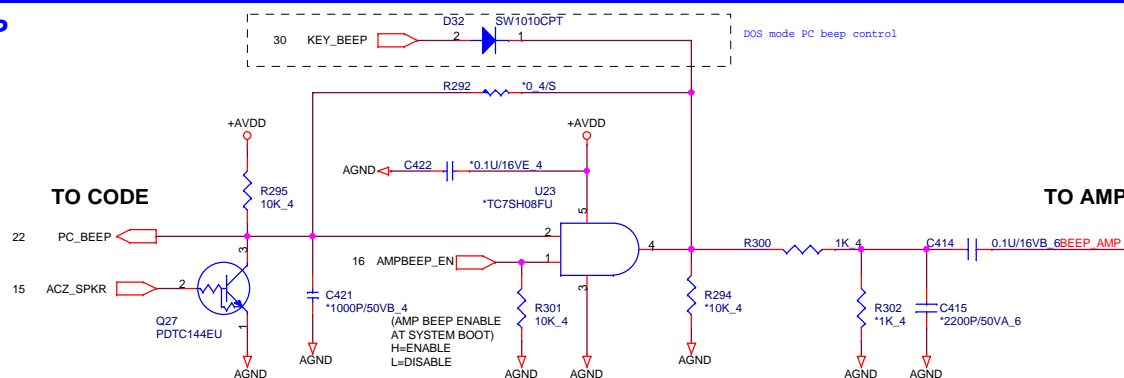

 +3V 4,5,7,8,9,12,13,14,15,16,17,18,19,20,23,26,28,29,30,31,33,34,38  

 +5V 17,20,23,28,31,32,33,37,38,39  

 +AVDD 23  

 +5VPCU 19,28,29,30,33,34,35,36,37



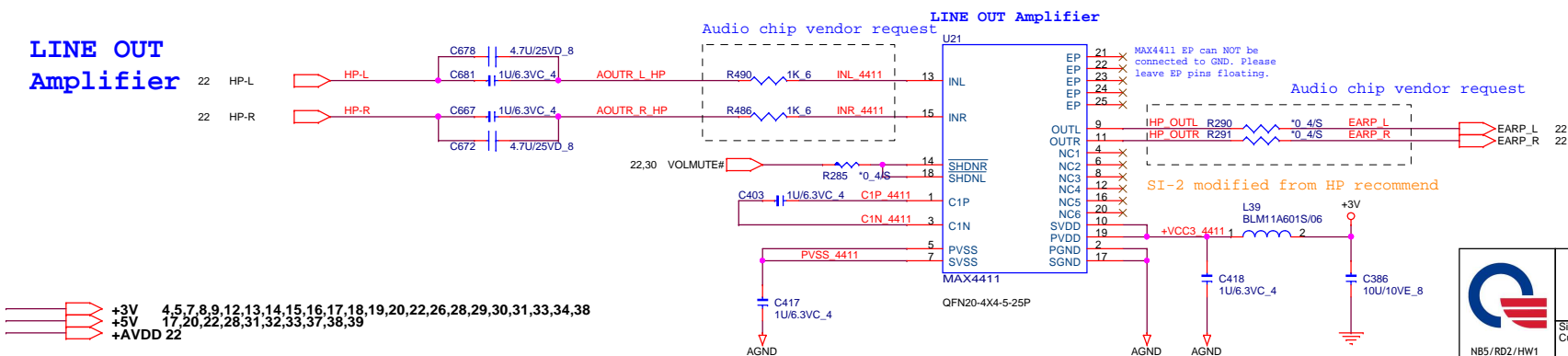


## AUDIO AMPLIFIER

**PCSPK BEEP**



LINE OUT  
Amplifier

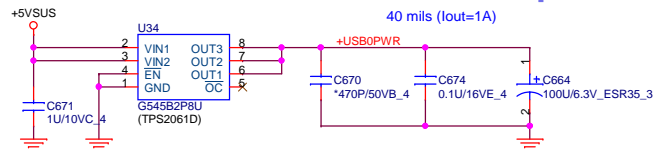




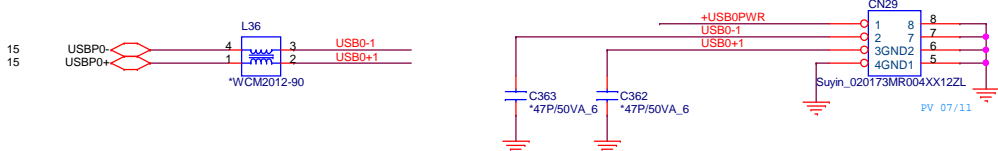




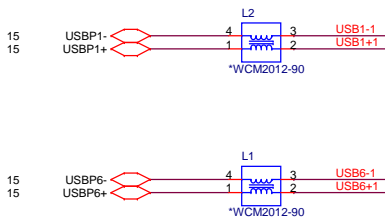
## USBX1



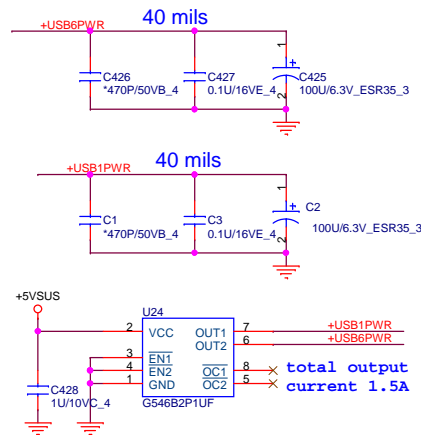
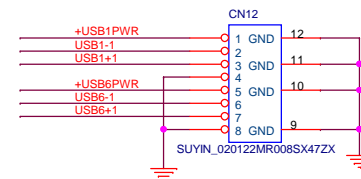
## USB 0



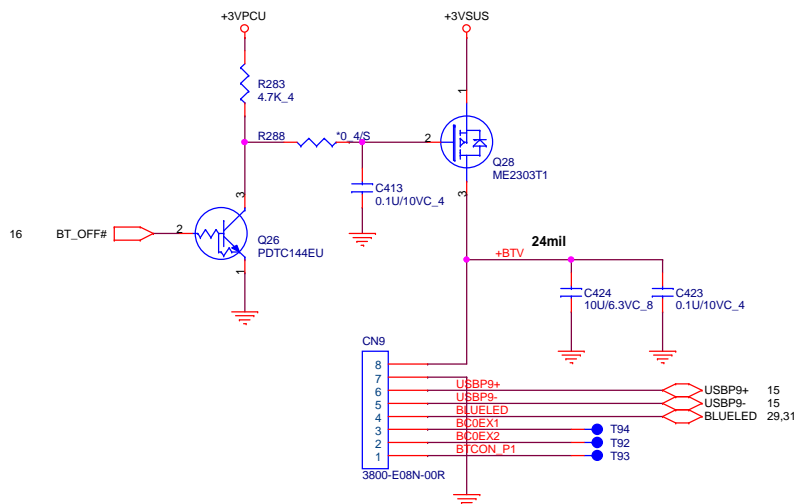
## USBX2



## USB 1 & 6



## BLUETOOTH



+3VPCU 5,14,19,29,30,32,33,35,37,39  
 +3VSUS 15,21,24,29,31,33,34,35,36,38  
 +5VSUS 19,30,32,33,38



**PROJECT : TT3**  
 Quanta Computer Inc.

Size Custom	Document Number Blue Tooth/USBX3	Rev 1A
Date: Wednesday, August 27, 2008	Sheet 25 of 41	



for 93C56 used. NC II 93C46 is u

26



EB | R395 | \*0.4 | LAN\_DISABLE# | 3C

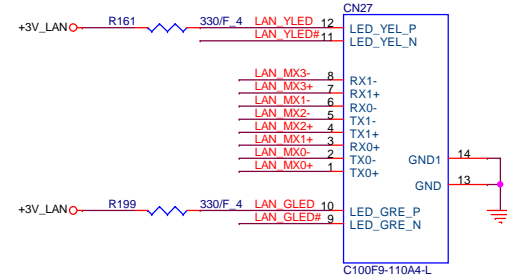
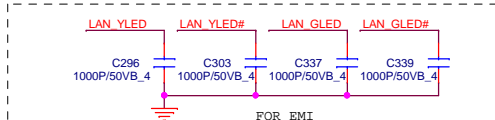
If disable DSM mode remove R395

LAN\_TX# D14 1 2 CH501H-40PT LAN\_YLED#

LAN\_GLINK10# D12 1 2 CH501H-40PT

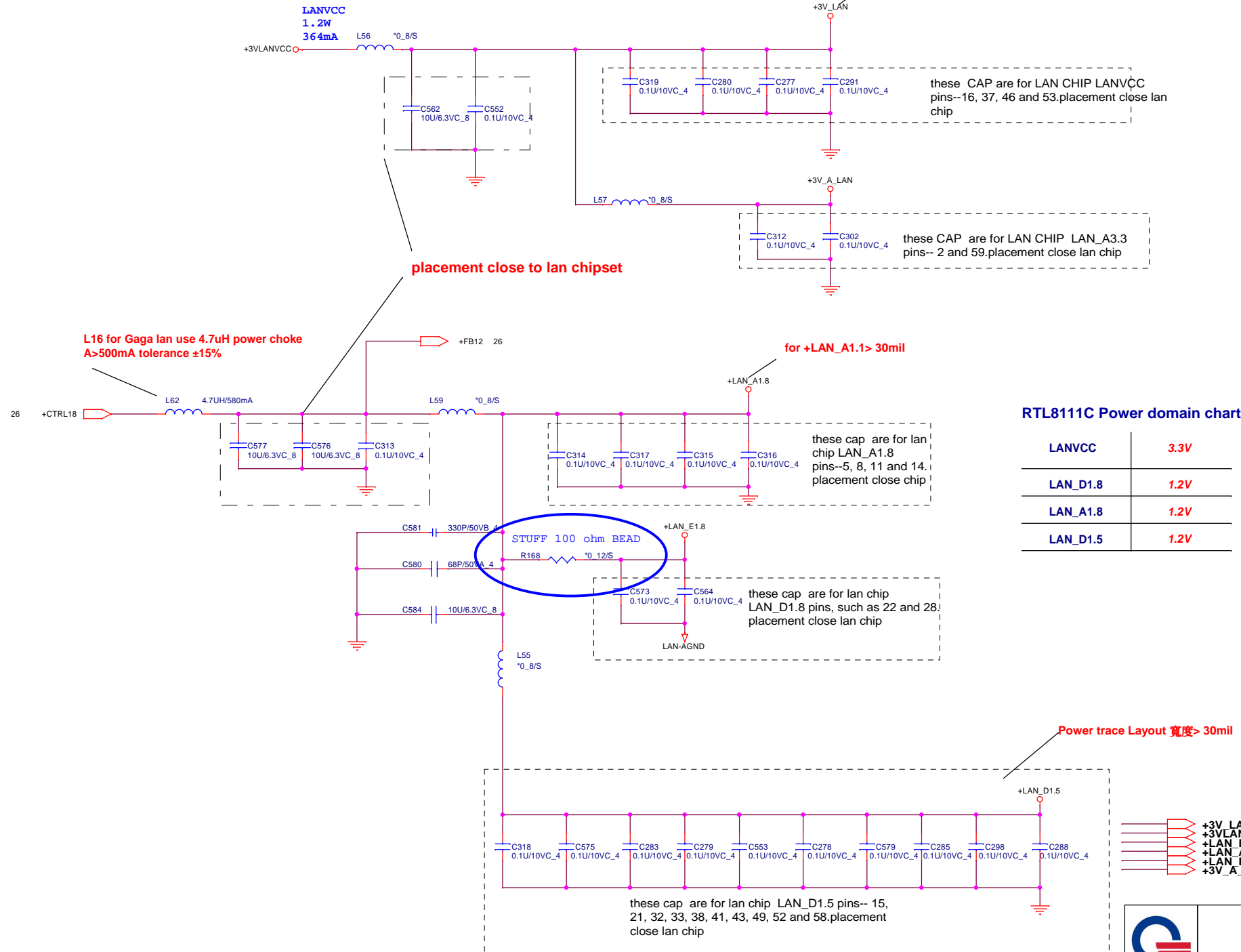
LAN\_GLINK100# D13 1 2 CH501H-40PT

LAN\_GLINK1000# D11 1 2 CH501H-40PT LAN\_GLED#



+3V\_LAN 27  
+3V\_LANVCC 27,33,38  
+LAN\_D1.5 27  
+LAN\_A1.8 27





RTL8111C Power domain chart

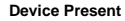
LANVCC	3.3V
LAN_D1.8	1.2V
LAN_A1.8	1.2V
LAN_D1.5	1.2V

+3V\_LAN26  
+3VLANVCC26,33,38  
+LAN\_D1.526  
+LAN\_A1.826  
+LAN\_E1.826  
+3V\_A\_LAN26

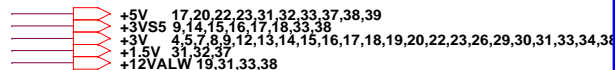


**PROJECT : TT3**  
**Quanta Computer Inc.**





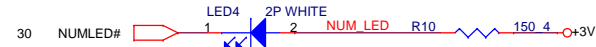
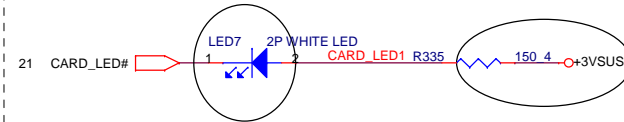
## SATA CONNECTOR



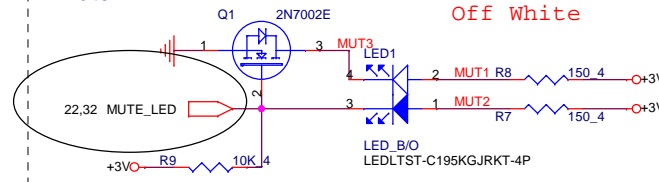
Size Custom	Document Number <b>NEW CARD/SATA ODD/SATA HDD</b>	Rev 1A
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Num lock LED

[illegible]

The diagram illustrates the keyboard controller interface. On the left, the CPU side shows two 32-bit data buses: `MY[0..15]` and `MX[0..7]`. These are connected to the `RP29` and `RP30` registers, which are 10KX8 10P8R. The `RP29` register is connected to the `MY` array (MY1 to MY9) and the `MX` array (MX1 to MX9). The `RP30` register is connected to the `MY` array (MY10 to MY15) and the `MX` array (MX10 to MX15). A `+3VPCU` supply is connected to the `10` pin of both registers. On the right, the keyboard side shows a 24-pin connector labeled `KEYBOARD`. The pins are numbered 1 to 24 and are connected to the `MX` array (MX1 to MX24) and the `MY` array (MY1 to MY24). The `KEYBOARD` label is at the bottom right.



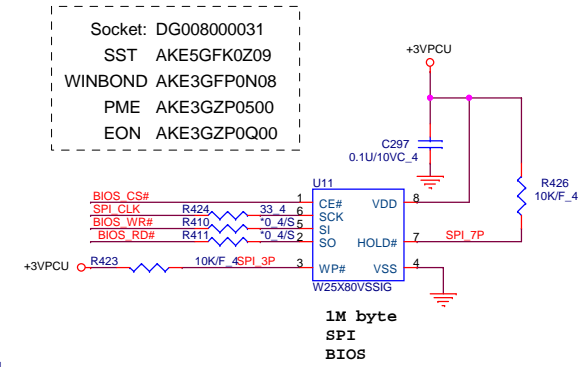
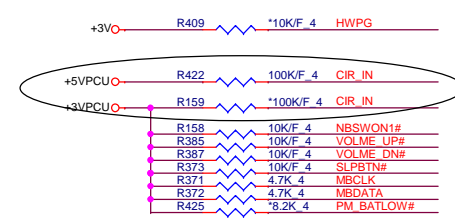
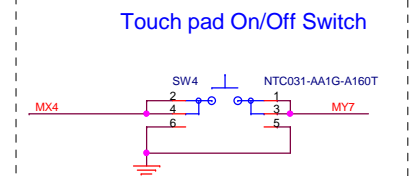
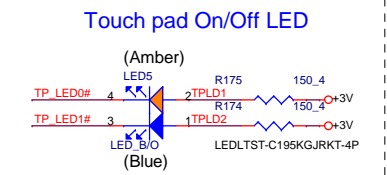
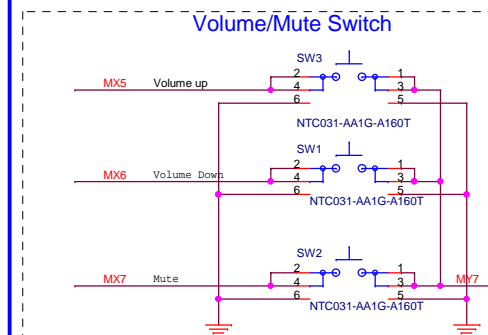
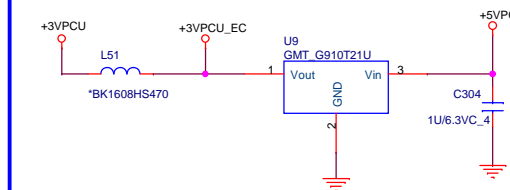
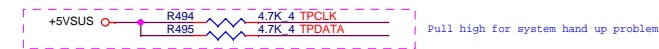
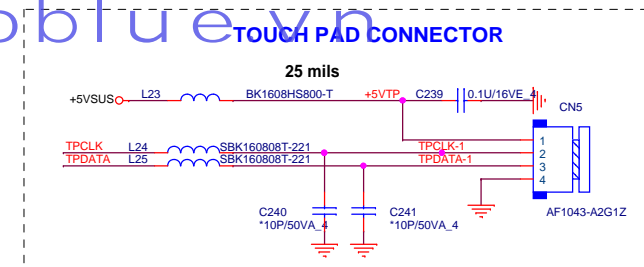
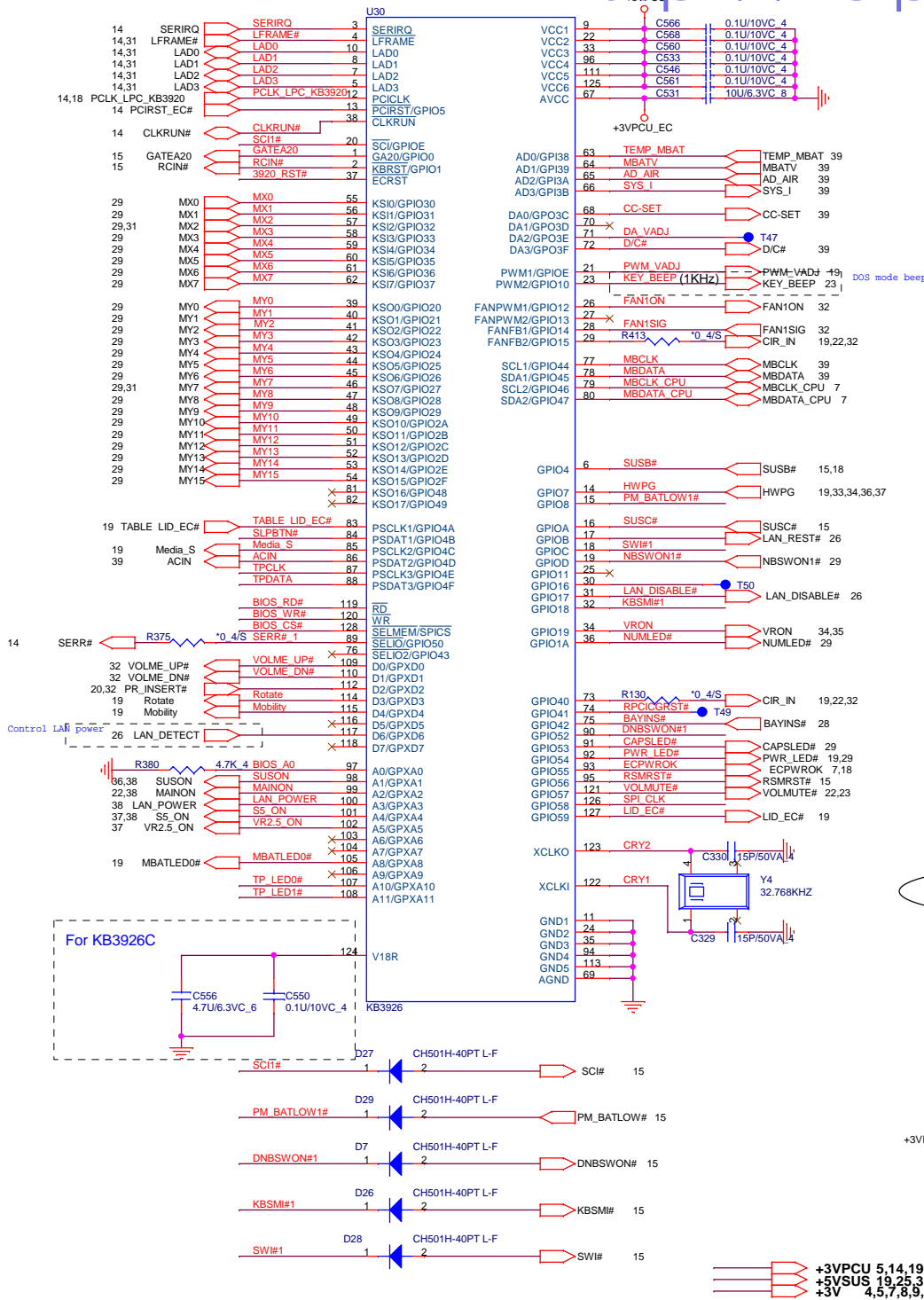

 +5VPCU 19,22,28,30,33,34,35,36,37  

 +3V 4,5,7,8,9,12,13,14,15,16,17,18,19,20,22,23,26,28,30,31,33,34,38  

 +3VSUS 15,21,24,25,31,33,34,35,36,38



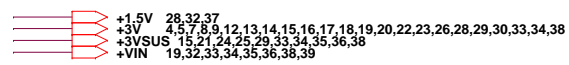
**PROJECT : TT3**  
Quanta Computer Inc.

Size B	Document Number LED/KEYBOARD/SW	Rev 1A
Date: Wednesday, August 27, 2008	Sheet 29 of 41	

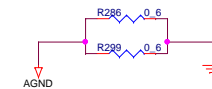
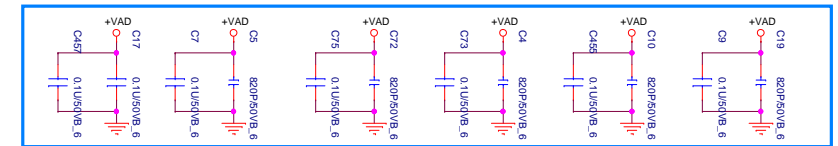
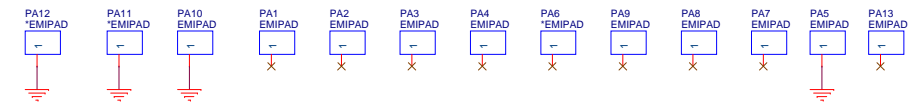
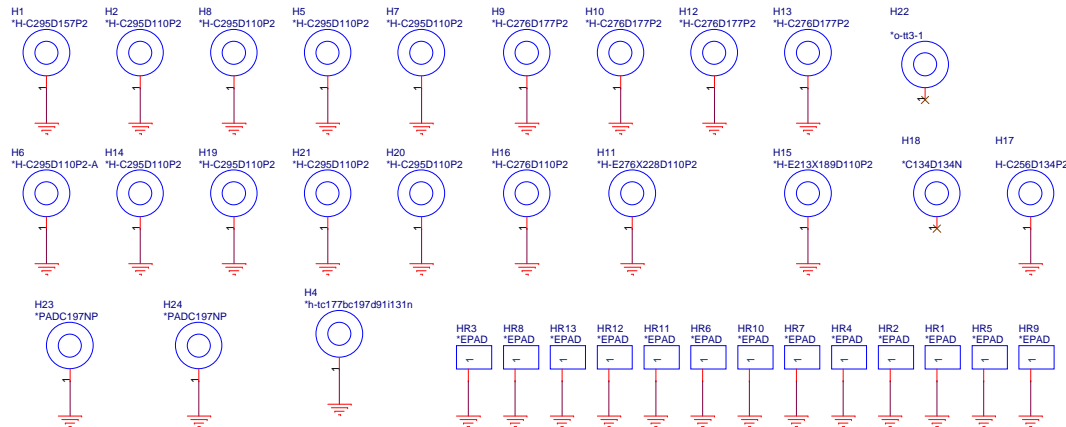
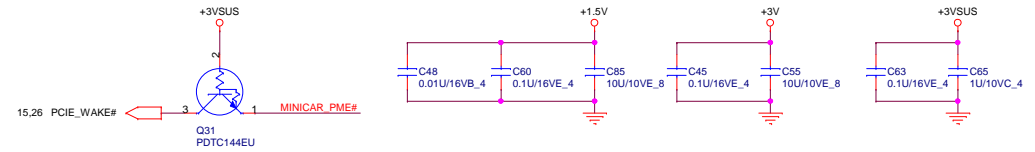
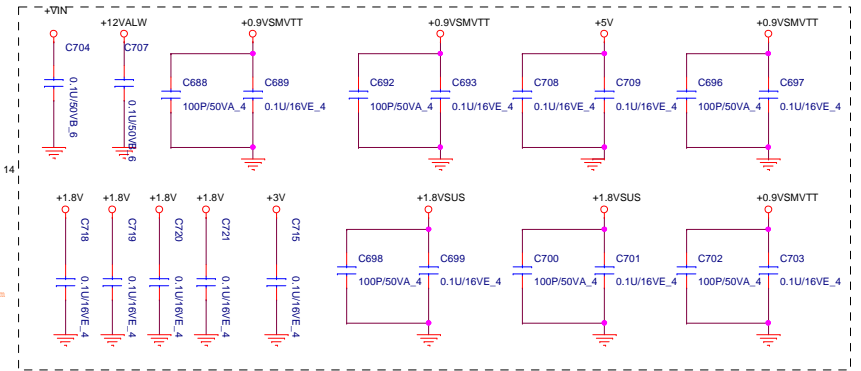
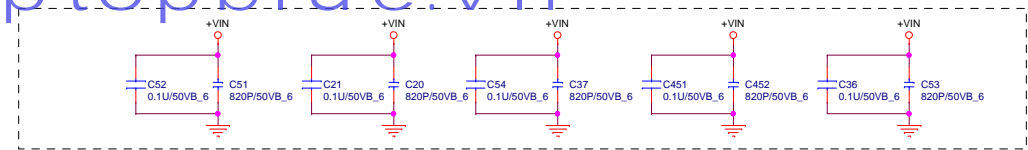
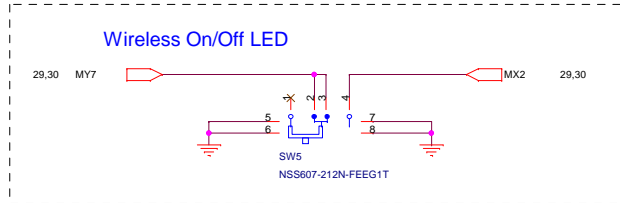
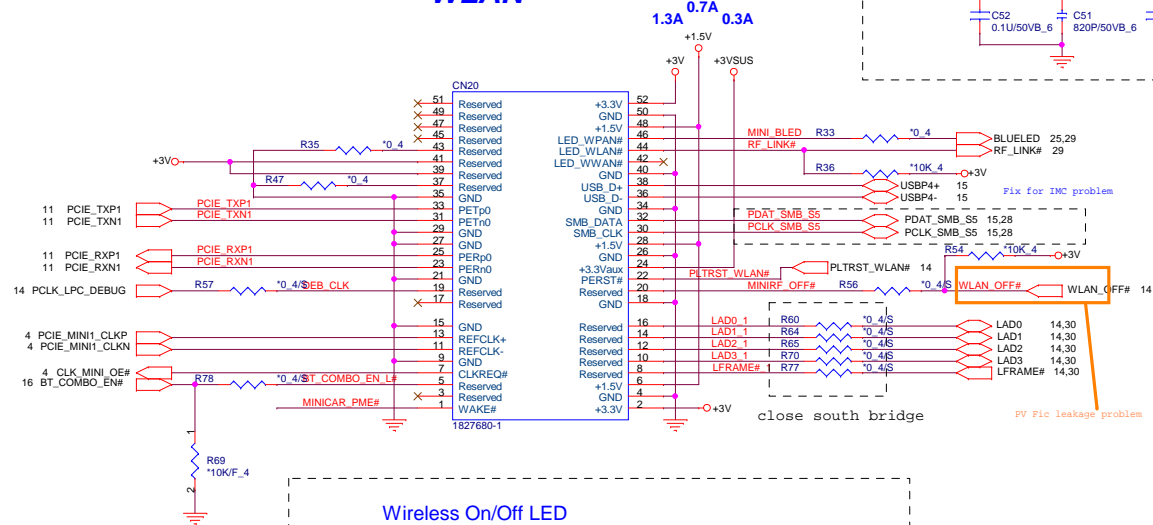








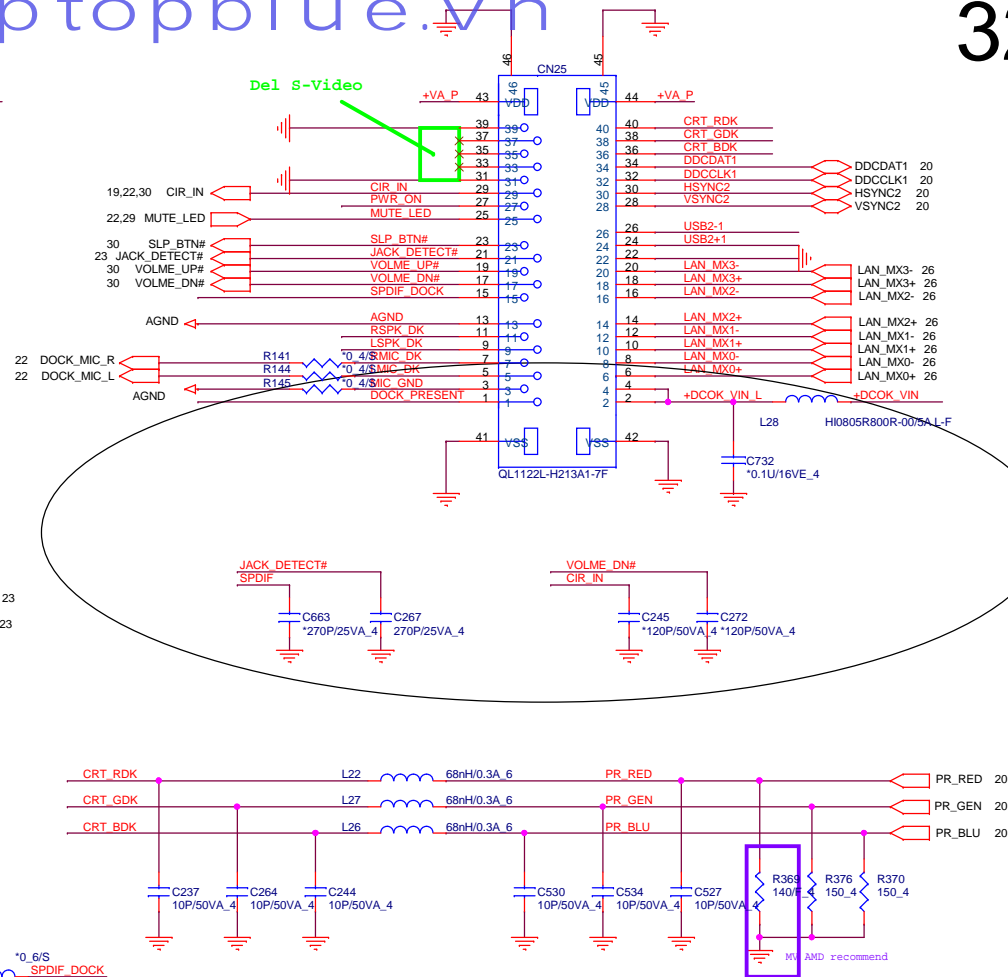
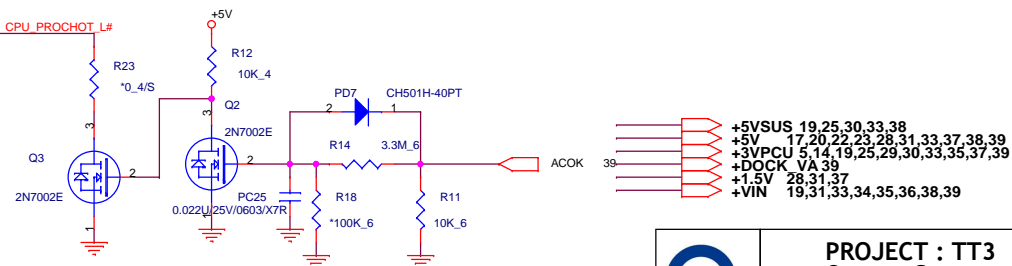
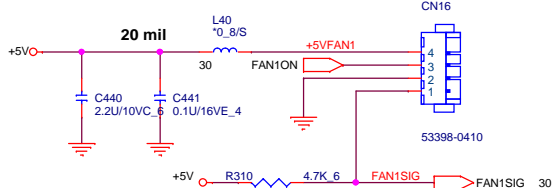
### Mini PCI-E Card 1 WLAN



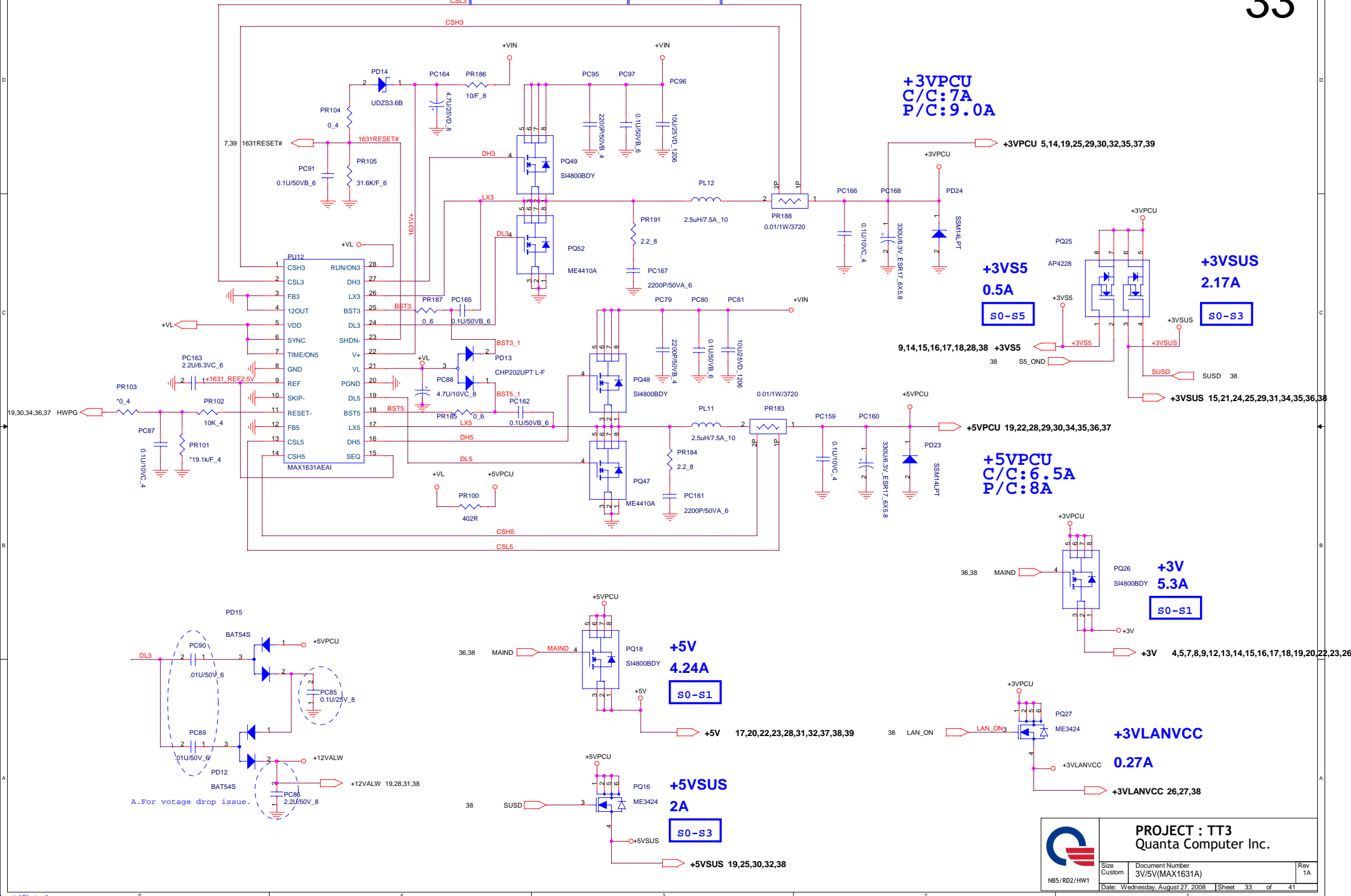
**PROJECT : TT3**  
Quanta Computer Inc.

Size Custom	Document Number Mini CARD/Hole	Rev 1A
Date: Wednesday, August 27, 2008		Sheet 31 of 41











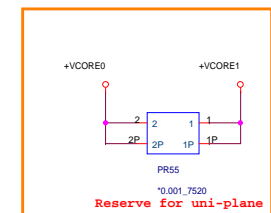
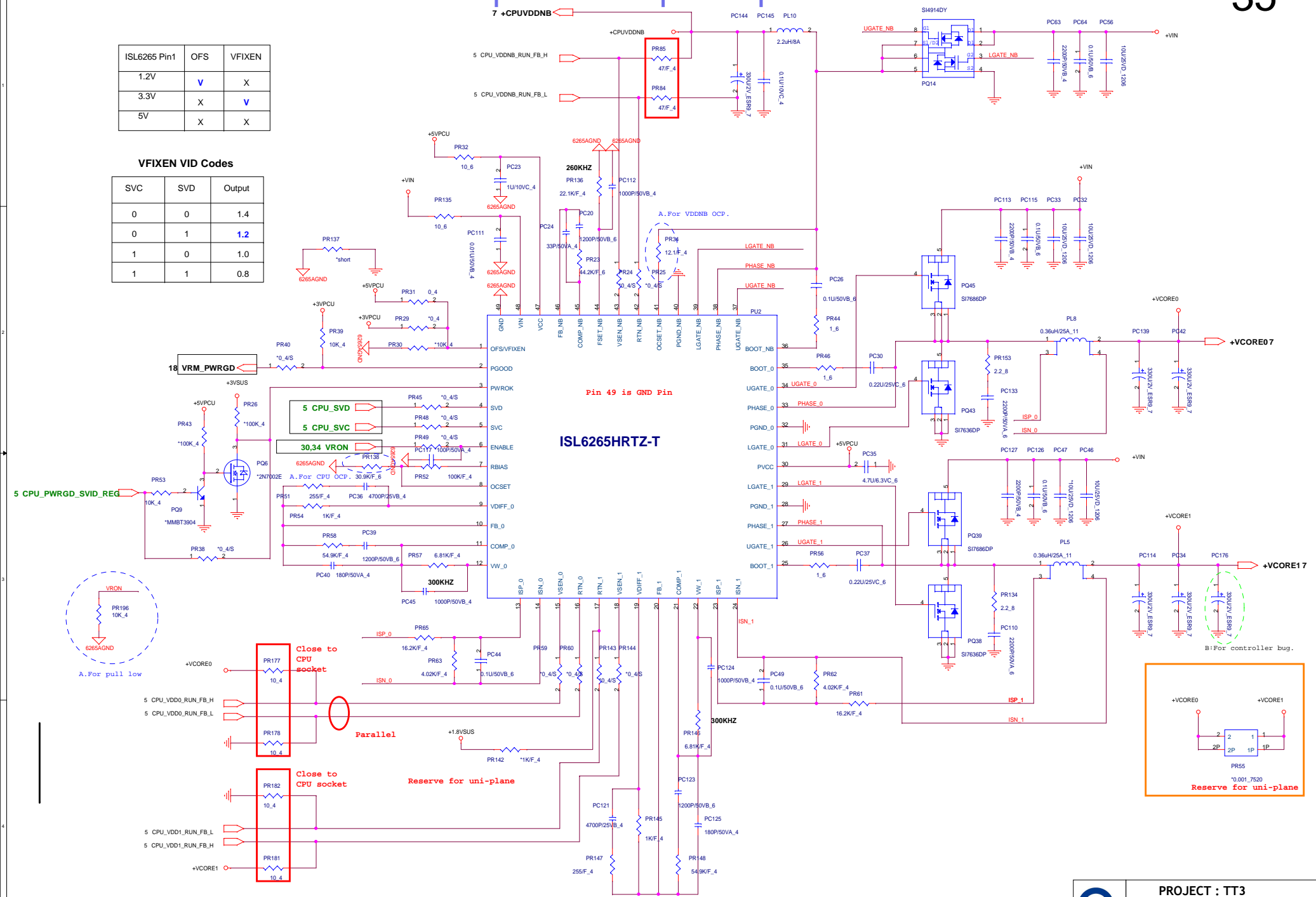




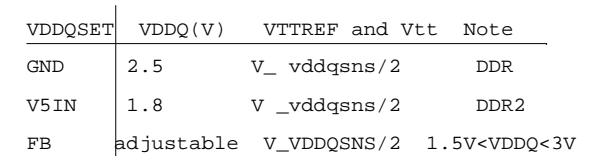
ISL6265 Pin1	OFS	VFIXEN
1.2V	<b>V</b>	X
3.3V	X	<b>V</b>
5V	X	X

### VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



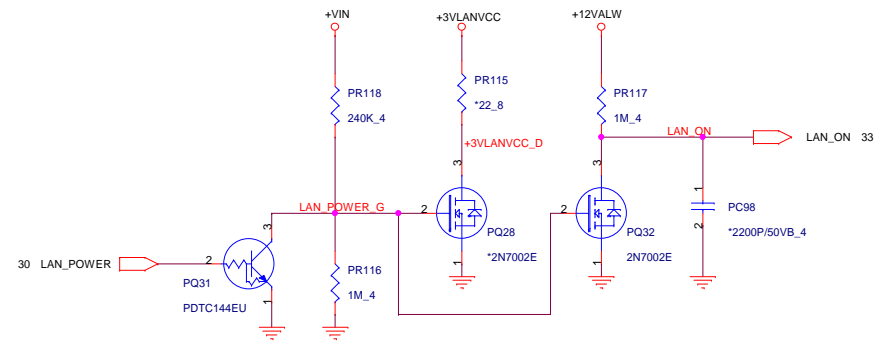
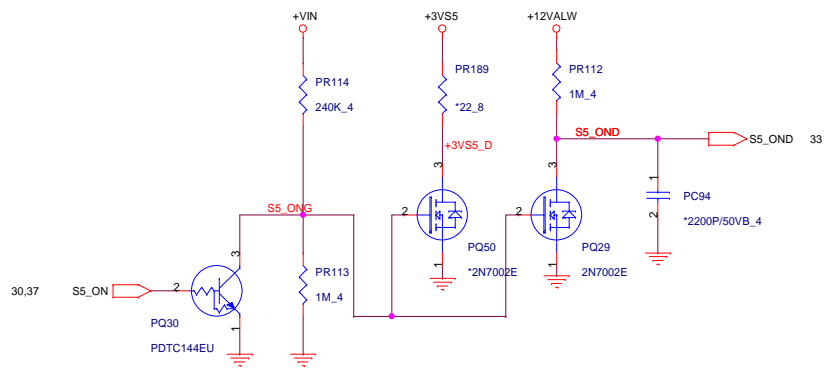
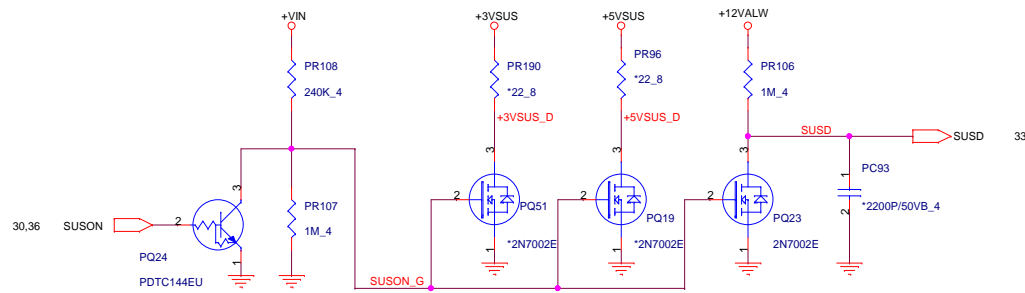
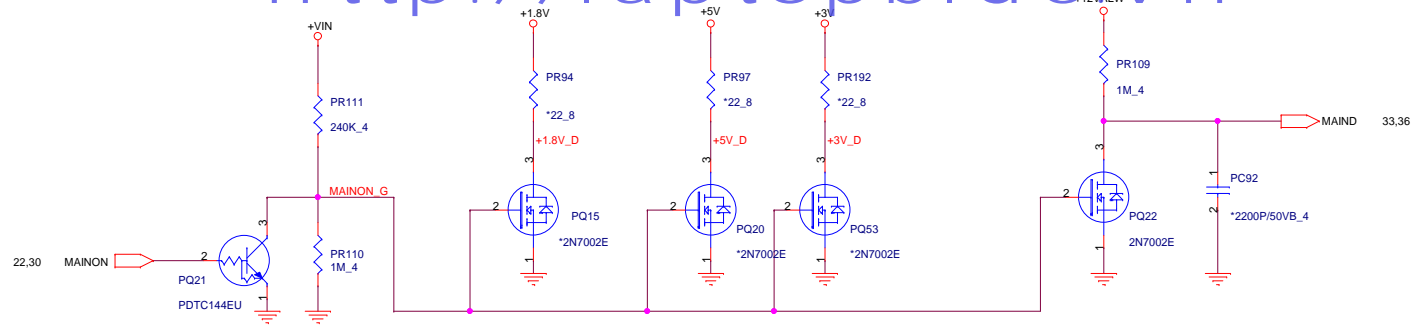














MP:For EC damage.

