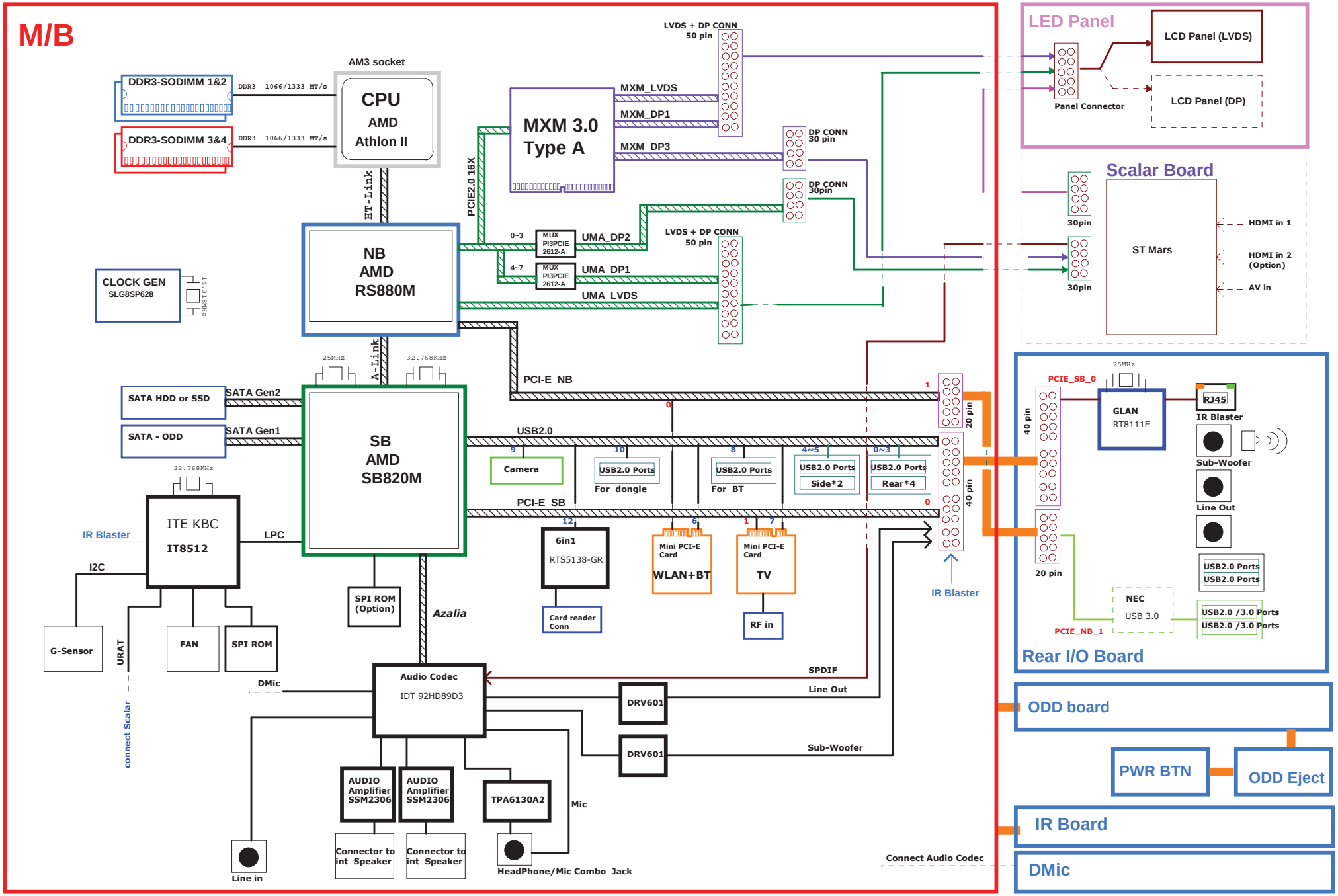
M3 System Block Diagram



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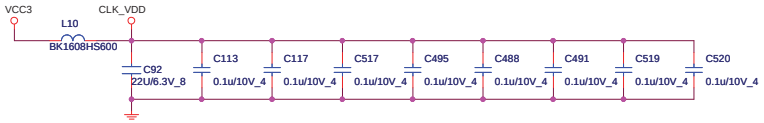
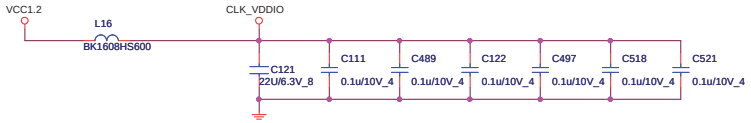
PROJECT : ZN8

Size	Document Number	Rev
	System Block Diagram	A

Date: Monday, March 22, 2010 Sheet 1 of 43

CLK_GEN_SLG8SP628





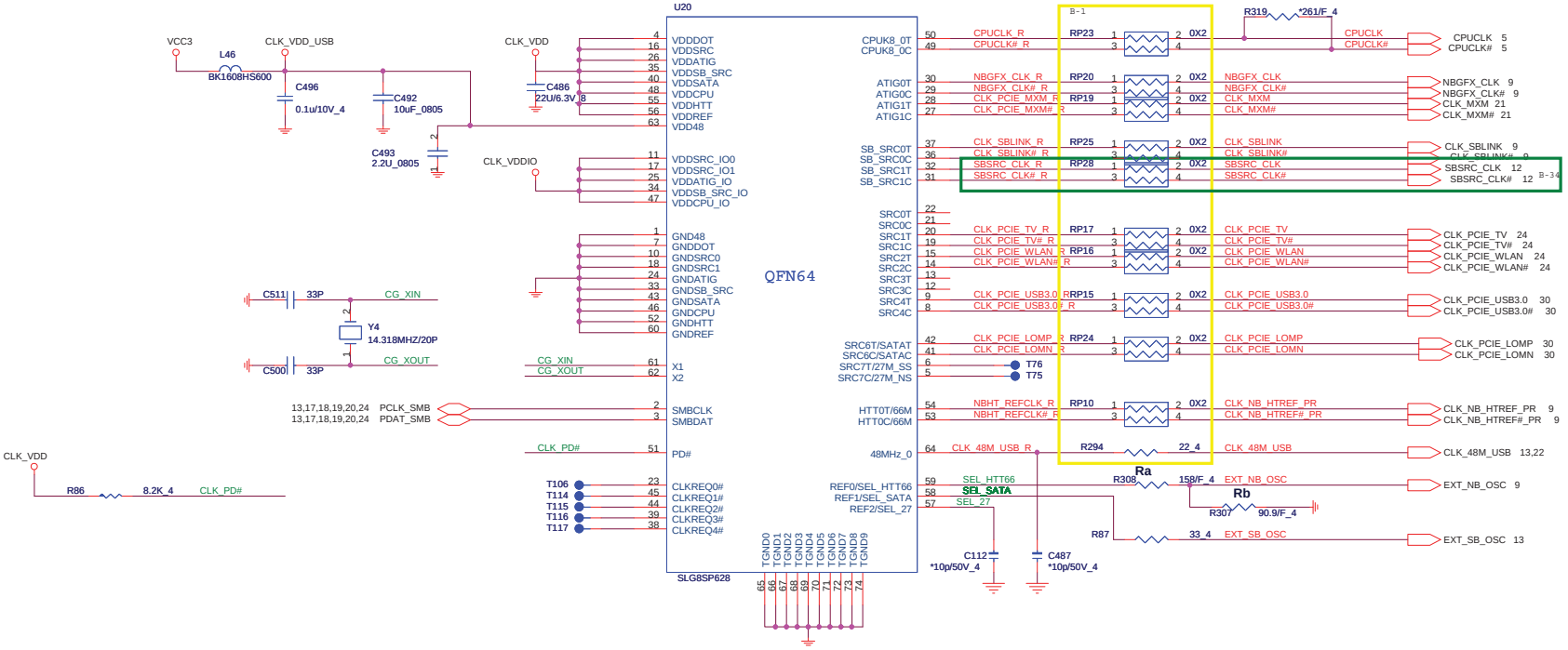
Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.

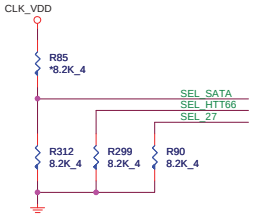
Place within 0.5" of CLKGEN

ICS9LPRS480 P/N : ALPRS480000

SLG8SP628 P/N : AL8SP628000

RTM880N-796 P/N : AL000880000





To CPU	200 Mhz	
To NB	RS880M for VGA	
To NB To SB	100 Mhz	
To LAN Controller To Mini PCIE Slot(TV) To Mini PCIE Slot(WLAN) To 6 in 1 Controller To USB 3.0	100 Mhz	
To NB HT BUS	100 Mhz	
To SB USB	48 Mhz	
To NB		

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27	1	27MHz and 27M SS outputs
	0*	100 MHz SRC clock

* default

CLOCK INPUT TABLE

CLOCKS	RS780
HT_REFCLKP	100M DIFF
HT_REFCLKN	100M DIFF
REFCLK_P	14M SE (1.1V)
REFCLK_N	vref
GFX_REFCLK	100M DIFF(IN/OUT)*
GPP_REFCLK	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF

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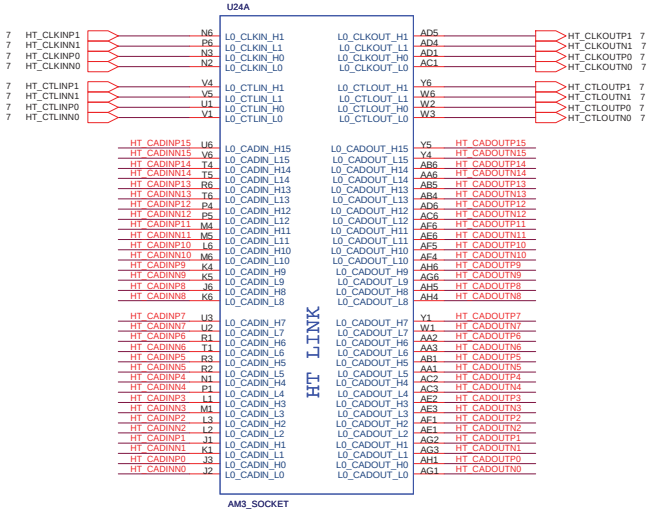
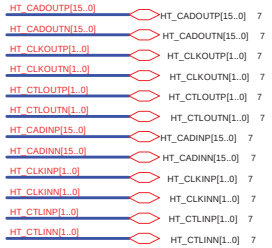
PROJECT : ZN8

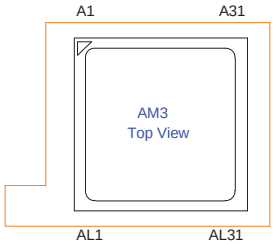
Size	Document Number	Rev
	Clock Generator	1A

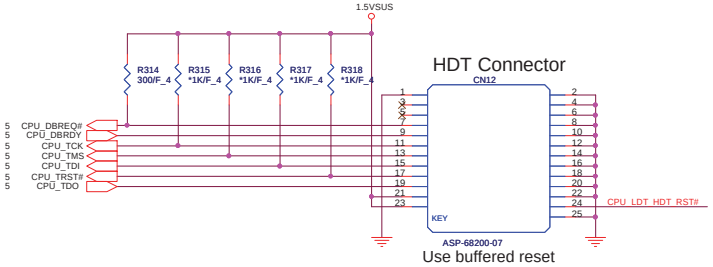
Date: Monday, March 22, 2010 Sheet 2 of 43

CPU HyperTransport and Debug



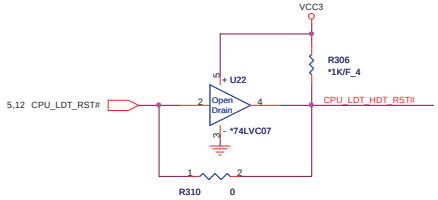






Use buffered reset

HDT Header

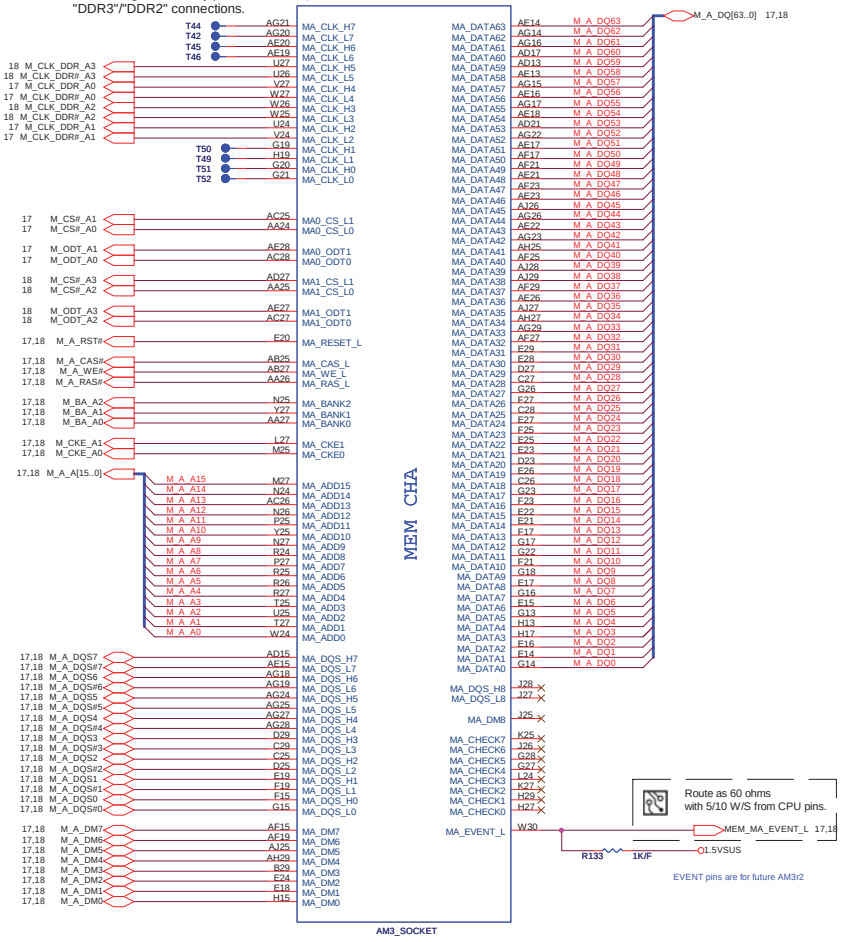


Quanta Computer Inc.		
PROJECT : ZN8		
Size	Document Number: CPU HyperTransport and Debug	Rev: 1A
Date: Monday, March 22, 2010	Sheet 3 of 40	

CPU Memory

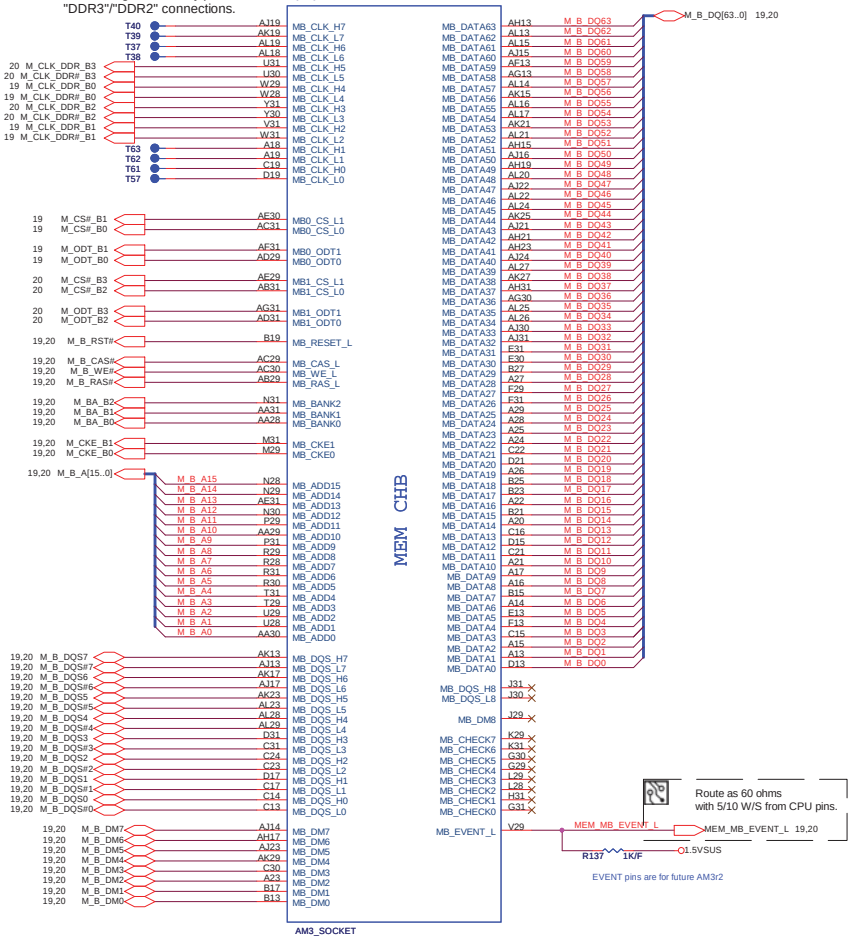
DDR3 Memory Interface A

Pin naming for memory pins indicate "DDR3"/"DDR2" connections.

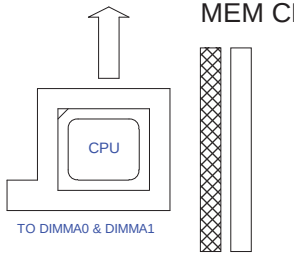


DDR3 Memory Interface B

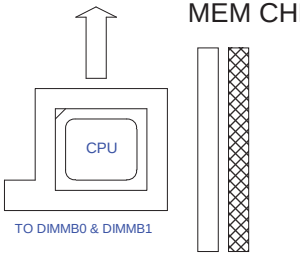
Pin naming for memory pins indicate "DDR3"/"DDR2" connections.



MEM CHA



MEM CHB



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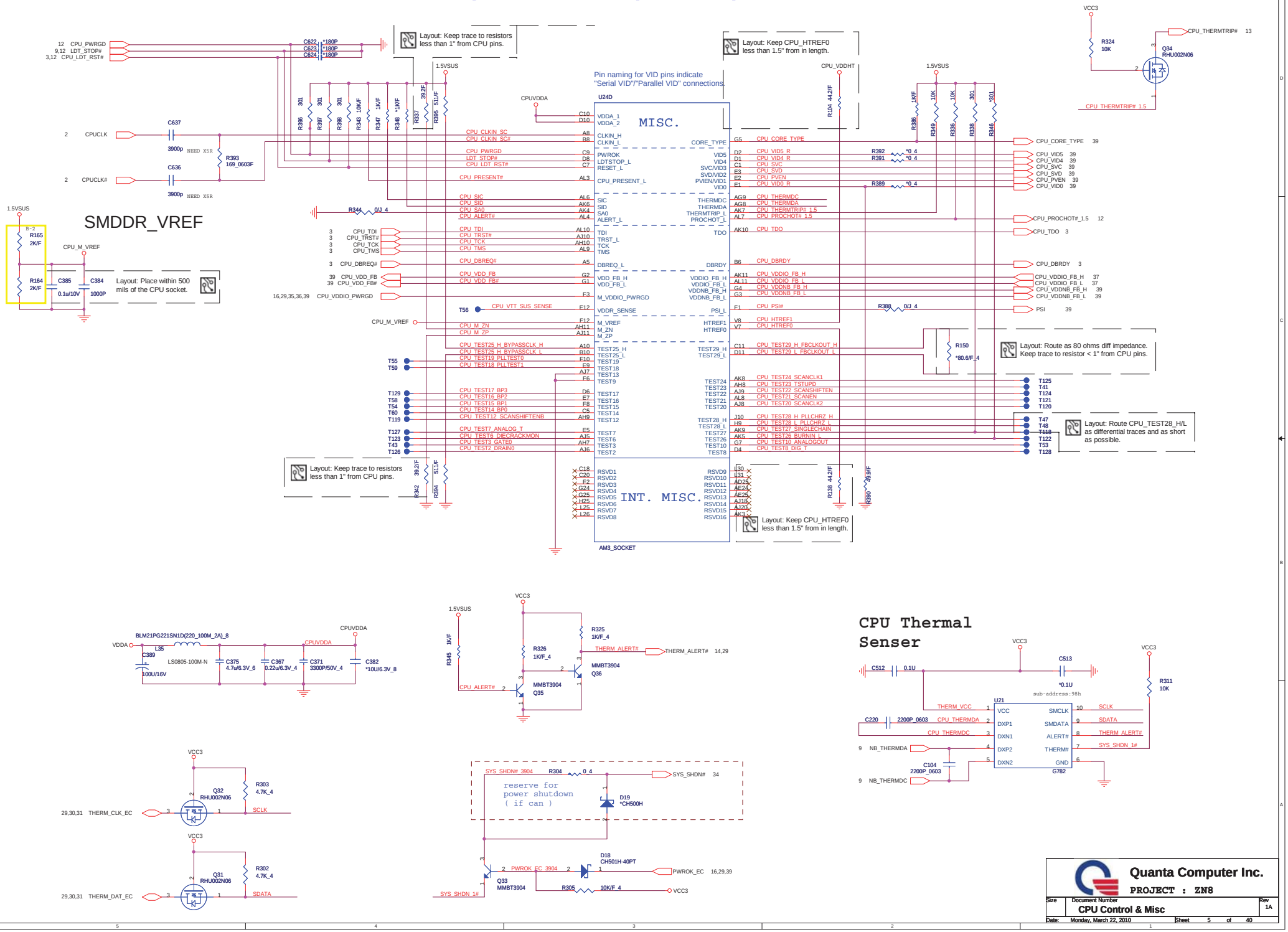
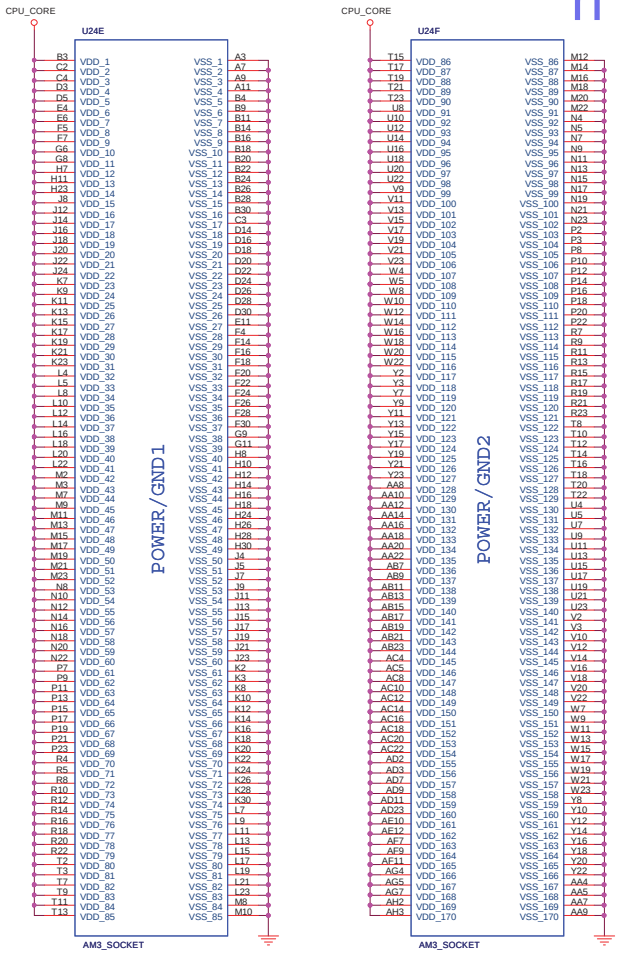
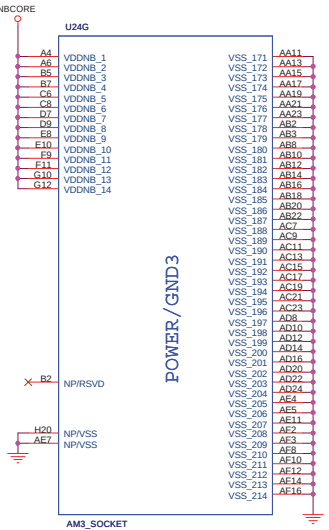
PROJECT : ZN8			
Size	Document Number: CPU Memory		Rev: 1A
Date: Monday, March 22, 2010		Sheet 4 of 40	

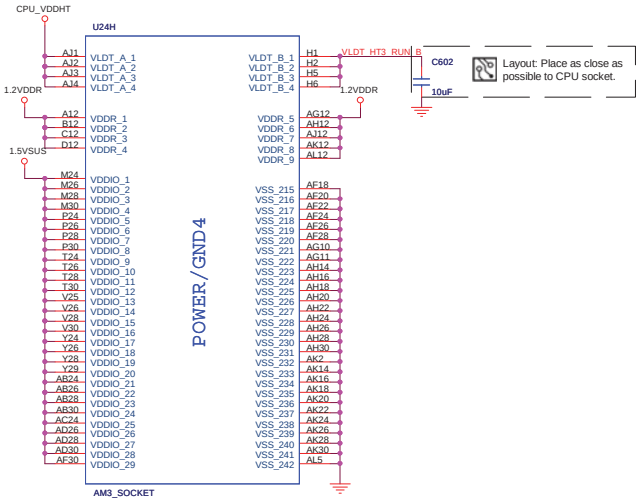
CPU Control and Miscellaneous

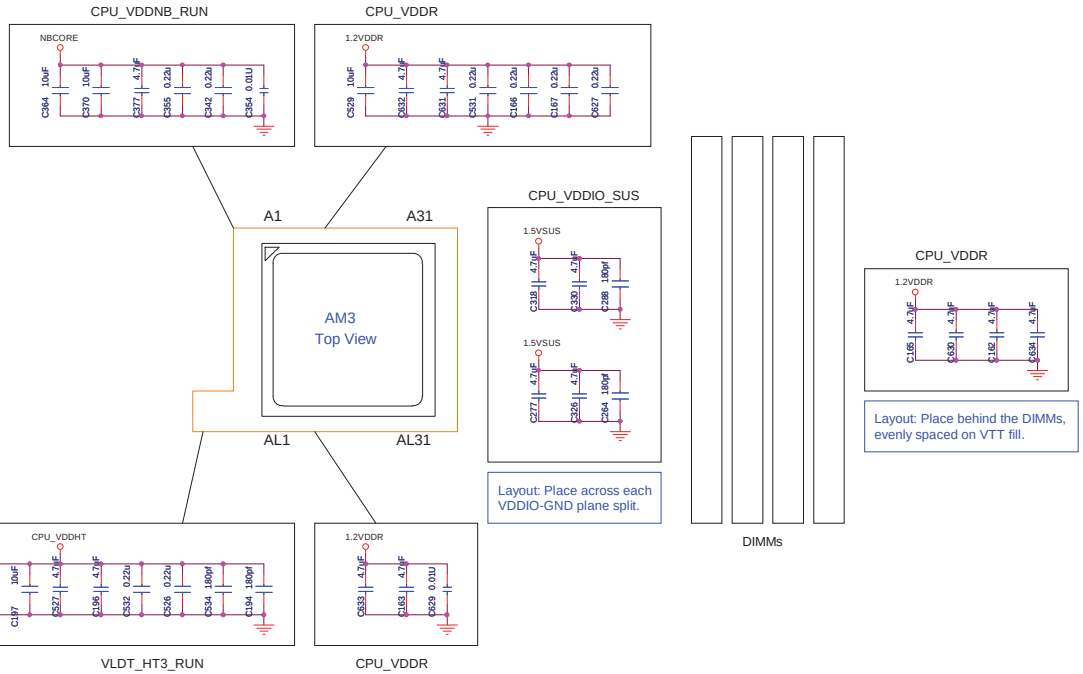


Processor Power and Ground

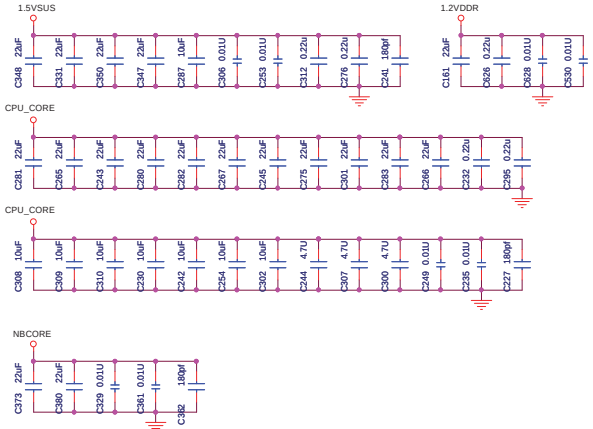




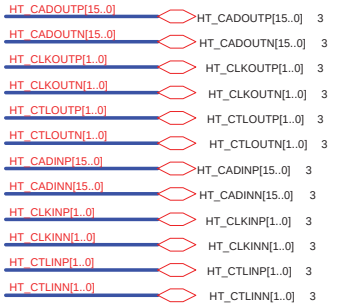




Bottom Side Decoupling



Quanta Computer Inc.			
PROJECT : ZN8			
Size	Document Number: CPU Power & GND		Rev: 1A
Date: Monday, March 22, 2010		Sheet 6 of 40	



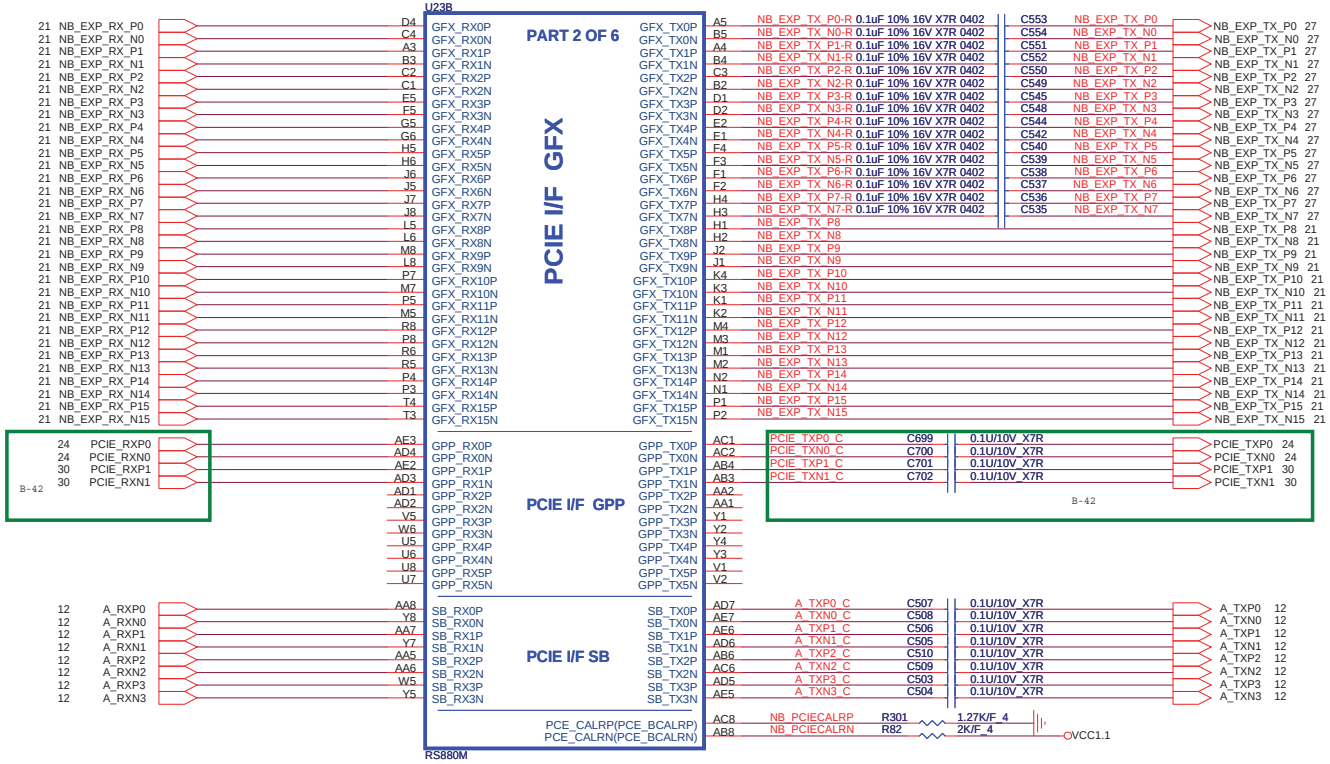
signals	RS880M
HT_TXCALP	R430 301 ohm 1%
HT_TXCALN	
HT_RXCALP	R434 301 ohm 1%
HT_RXCALN	

Quanta Computer Inc.

PROJECT : ZN8

Size	Document Number	Rev
	RS880M-HT Link I/F	1A

Date: Monday, March 22, 2010 Sheet 7 of 40



Enables Debug Bus acess
through memory I/O pads and GPIO.
0 : Enable RS880M , Default
1 : Disable RS880M
(RX881 use DAC_VSYNC)

INT_CRT_VSYNC_NB R357 3K/J_4 VCC3
R352 *3K/J_4

Indicates if memory Side port
is available or not
0: Reserved
1: Required setting. Select with a pull-up
resistor on the strap
(RX881 use DAC_HSYNC)

INT_CRT_HSYNC_NB R356 3K/J_4 VCC3

140ohm CS11402FB19

U23C
RS880M
PART 3 OF 6

CRT/TVOUT
PLL PWR
LVTM
PM
CLOCKs
MIS.

AVDD1(NC)	F12	TXOUT_L0P(NC)	A22
AVDD2(NC)	E12	TXOUT_L0N(NC)	B22
AVDDDI(NC)	F14	TXOUT_L1P(NC)	A21
AVSSDI(NC)	G15	TXOUT_L1N(NC)	B21
AVDDQ(NC)	H15	TXOUT_L2P(NC)	B20
AVSSQ(NC)	H14	TXOUT_L2N(DBG_GPIO0)	A20
		TXOUT_L3P(NC)	A19
C_Pr(DFT_GPIO5)	E17	TXOUT_L3N(DBG_GPIO2)	B19
Y(DFT_GPIO2)	F17		
COMP_Pb(DFT_GPIO4)	F15	TXOUT_U0P(NC)	B18
		TXOUT_U0N(NC)	A18
RED(DFT_GPIO0)	G18	TXOUT_U1P(PCIE_RESET_GPIO3)	A17
REDb(NC)	G17	TXOUT_U1N(PCIE_RESET_GPIO2)	B17
GREEN(DFT_GPIO1)	E18	TXOUT_U2P(NC)	D20
GREENb(NC)	F18	TXOUT_U2N(NC)	D21
BLUE(DFT_GPIO3)	E19	TXOUT_U3P(PCIE_RESET_GPIO5)	D18
BLUEb(NC)	F19	TXOUT_U3N(NC)	D19
DAC_HSYNC(PWM_GPIO4)	A11	TXCLK_LP(DBG_GPIO1)	B16
DAC_VSYNC(PWM_GPIO6)	B11	TXCLK_LN(DBG_GPIO3)	A16
DAC_SCL(PCE_RCALRN)	F8	TXCLK_UP(PCIE_RESET_GPIO4)	D16
DAC_SDA(PCE_TCALRN)	E8	TXCLK_UN(PCIE_RESET_GPIO1)	D17
DAC_RSET(PWM_GPIO1)	G14		
PLLVDD(NC)	A12	VDDLTP18(NC)	A13
PLLVDD18(NC)	D14	VSSLTP18(NC)	B13
PLLVSS(NC)	B12	VDDLT18_1(NC)	A15
VDDA18HTPLL	H17	VDDLT18_2(NC)	B15
VDDA18PCIEPLL1	D7	VDDLT33_1(NC)	A14
VDDA18PCIEPLL2	E7	VDDLT33_2(NC)	B14
SYSRESETb	D8	VSSLT1(VSS)	C14
POWERGOOD	A10	VSSLT2(VSS)	D15
LDTSTOPb	C10	VSSLT3(VSS)	C16
ALLOW_LDTSTOP	C12	VSSLT4(VSS)	C18
		VSSLT5(VSS)	C20
HT_REFCLKP	C25	VSSLT6(VSS)	E20
HT_REFCLKN	C24	VSSLT7(VSS)	C22
REFCLK_P/OSCIN(OSCIN)	E11	LVDS_DIGON(PCE_TCALRP)	E9
REFCLK_N(PWM_GPIO3)	F11	LVDS_BLON(PCE_RCALRP)	F7
GFX_REFCLKP	T2	LVDS_ENA_BL(PWM_GPIO2)	G12
GFX_REFCLKN	T1		
GPP_REFCLKP	U1		
GPP_REFCLKN	U2		
GPPSB_REFCLKP(SB_REFCLKP)	V4		
GPPSB_REFCLKN(SB_REFCLKN)	V3		
I2C_CLK	B9	TMDS_HPD(NC)	D9
I2C_DATA	A9	HPD(NC)	D10
DDC_CLK0/AUX0P(NC)	A8		
DDC_DATA0/AUX0N(NC)	B8	SUS_STAT#(PWM_GPIO5)	D12
DDC_CLK1/AUX1P(NC)	B7		
DDC_DATA1/AUX1N(NC)	A7	THERMALDIODE_P	AE8
		THERMALDIODE_N	AD8
STRP_DATA	B10		
RSVD	G11	TESTMODE	D13
AUX_CAL(NC)	C8		

20mA
120mA

+3V_AVDD_NB
+1.8V_AVDDDI_NB
+1.8V_AVDDQ_NB
+1.1V_PLLVDD
+1.8V_PLLVDD18
+1.8V_VDDA18HTPLL
+1.8V_VDDA18PCIEPLL

28 INT_CRT_RED R364 *0/short_4 INT_CRT_RED_R
R353 140/F_4
28 INT_CRT_GREEN R365 *0/short_4 INT_CRT_GRE_R
R354 150/F_4
28 INT_CRT_BLU R366 *0/short_4 INT_CRT_BLU_R
R355 150/F_4
10,28 INT_CRT_HSYNC R361 *0/short_4 INT_CRT_HSYNC_NB
10,28 INT_CRT_VSYNC R362 *0/short_4 INT_CRT_VSYNC_NB
28 INT_CRT_DDCDAT R371 *0/short_4 INT_DDCDAT_NB
28 INT_CRT_DDCCLK R370 *0/short_4 INT_DDCCLK_NB
R115 715/F_6 DAC_RSET_NB

B-66
12 A_RST#_SB
16 NB_PWRGD
R111 0_2
NB_RST#_IN
NB_PWRGD
NB_LDT_STOP#
NB_ALLOW_LDTSTOP

2 CLK_NB_HTREF_PR
2 CLK_NB_HTREF#_PR
2 EXT_NB_OSC
RP27 4 3 0_4P2R_4 2 1 B-3
NB_REFCLK_N
R313 *4.7K
R309 *4.7K
B-36
2 NBGFX_CLK
2 NBGFX_CLK#

VCC1.1 B-35 R373 150/F_4 R375 150/F_4
for EXT Gen.

For A11 version
R335 *49.9/F_4 CLK_SBLINK
R333 *49.9/F_4 CLK_SBLINK#

2 CLK_SBLINK
2 CLK_SBLINK#

B-4 21,26 LCD_CLK
21,26 LCD_DAT

26 DP_AUX0P
26 DP_AUX0N
26 DP_AUX1P
26 DP_AUX1N

VCC3
R360 4.7K/J_4
R359 4.7K/J_4
EDID_CLK EDID_CLK
EDID_DATA

R374 *2K/F STRP_DATA
VCC3
R372 *2K/F

T36
R358 150R RS880_AUX_CAL

DDR3 based CPU : Level shifted to 1.8 V on the Northbridge side using an open-drain buffer and pulled up to 1.8V_S0 through a 2.2k Ohm 5% resistor on the Northbridge side.

VCC1.8
R119 1K/F_4
VCC1.8
+ U8
5,12 LDT_STOP#
2 Open Drain 4
3 - 74LVC07
NB_LDT_STOP#

R121 1K/F_4 VCC1.8
12 ALLOW_LDTSTOP
R120 *0/short_4 NB_ALLOW_LDTSTOP

ALLOW_LDTSTOP	OC
LDT_STOP#	3.3V Input

* Although defined as 3.3V I/Os, a 1.8V signaling level is supported on LDT_STOP#/ALLOW_LDTSTOP given that Vih is 1.4V. 3.3V to 1.8V level translation is not required.

VCC1.8
VDDA18PCIEPLL -PCIE PLL
L27 BLM18PG221SN1D _6 20mils width +1.8V_VDDA18PCIEPLL
C198 2.2U/6.3V_6

VDDA18HTPLL -HT LINK PLL
L17 BLM18PG221SN1D _6 20mils width +1.8V_VDDA18HTPLL
C193 2.2U/6.3V_6

A13 +1.8V_VDDLTP18_NB
B13
A15 +1.8V_VDDLT_18_NB
B15
A14
B14
C14
D15
C16
C18
C20
E20
C22

R107 *0/short_4 INT_LVDS_PWREN 27
R112 *0/short_4 INT_LVDS_BRIGHT 27
R113 *0/short_4 INT_LVDS_BLON 27
R108 4.7K
R106 4.7K
R109 4.7K

RS880M DEBUG PIN MAPPING

DEBUG_OUT0	LVDS_DIGON
DEBUG_OUT1	LVDS_ENA_BL
DEBUG_OUT2	LVDS_BLON
DEBUG_OUT3	TMDS_HPD
DEBUG_OUT4	AUX1N
DEBUG_OUT5	AUX1P
DEBUG_OUT6	HPD
DEBUG_OUT7	AUX_CAL

D9 DP2_HPD 26
D10 DP_HPD 26
D12 R127 *0/short_4 SUS_STAT# 13
SUS_STAT#_R 10
AE8 NB_THERMDA NB_THERMDA 5
AD8 NB_THERMDC NB_THERMDC 5
D13 TEST_EN R122 1.8K/F_4

VCC3 L33 BLM18PG181SN1D(180,1.5A)_6 +3V_AVDD_NB
AVDD-DAC Analog
C238 2.2U/6.3V_6

VCC1.1 BLM18PG181SN1D(180,1.5A)_6 L28 +1.1V_PLLVDD
PLLVDD - Graphics PLL
C222 2.2U/6.3V_6

VCC1.8 PLLVDD18 - Graphics PLL
L29 BLM18PG181SN1D(180,1.5A)_6 +1.8V_PLLVDD18
C233 10U/6.3V_8
C203 0.1U/10V_4

VCC1.8
R117 0/J_6 +1.8V_AVDDDI_NB
AVDDI-DAC Digital
C223 0.1U/10V_4

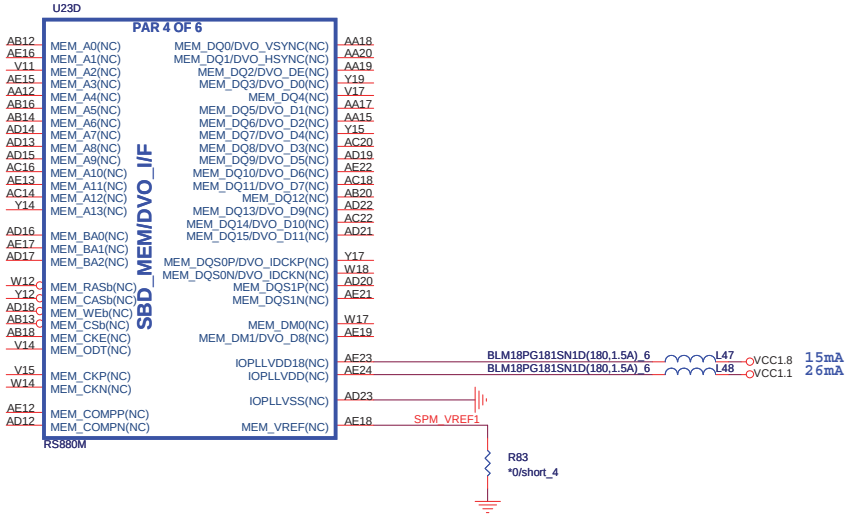
BLM18PG181SN1D(180,1.5A)_6 L30 +1.8V_AVDDQ_NB
AVDDQ-DAC Bandgap Reference
C224 0.1U/10V_4

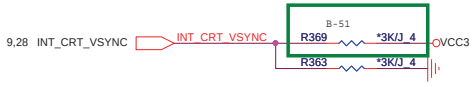
VCC1.8
BLM18PG181SN1D(180,1.5A)_6 L32 +1.8V_VDDLTP18_NB
C234 2.2U/6.3V_6
VDDLTP18 - LVDS or DVI/HDMI PLL

BLM21PG221SN1D(220,100M,2A)_8 L31 +1.8V_VDDLT_18_NB
C202 4.7U/6.3V_6
C221 2.2U/6.3V_6
C200 0.1U/10V_4
VDDLT18 - LVDS or DVI/HDMI digital

Quanta Computer Inc.
PROJECT : ZN8

Size	Document Number	Rev
	RS880M-System I/F	1A
Date: Monday, March 22, 2010	Sheet 9 of 40	

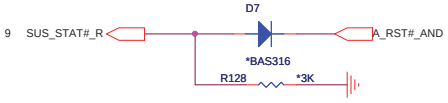




STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.

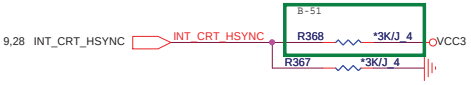
RS880M	
1 Disable	
0 Enable	



DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected



RS880M: Enables Side port memory

RS880M:HSYNC#

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]

Quanta Computer Inc.
PROJECT : ZN8

Size	Document Number	Rev
	RS880M-Spmem/Straps	1A

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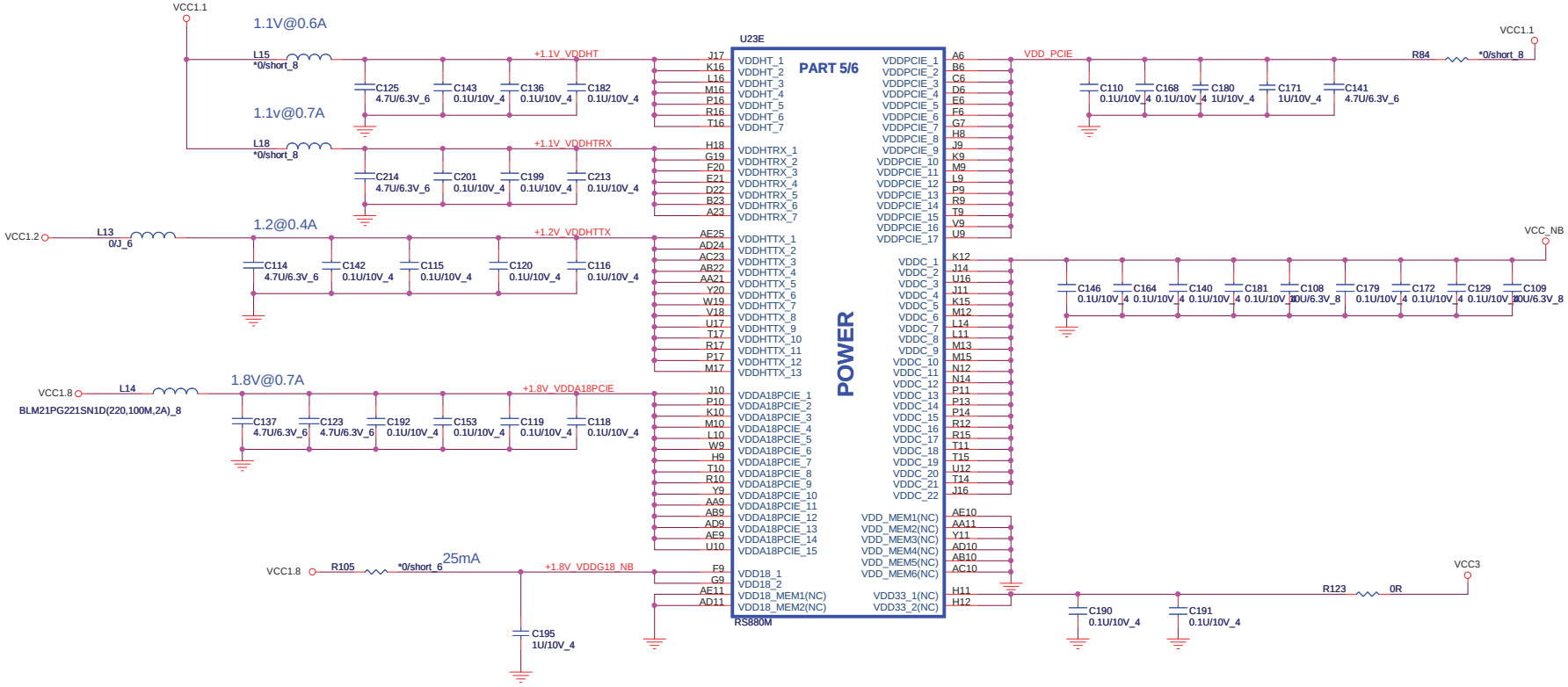
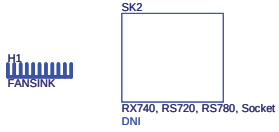
RS880M POWER TABLE

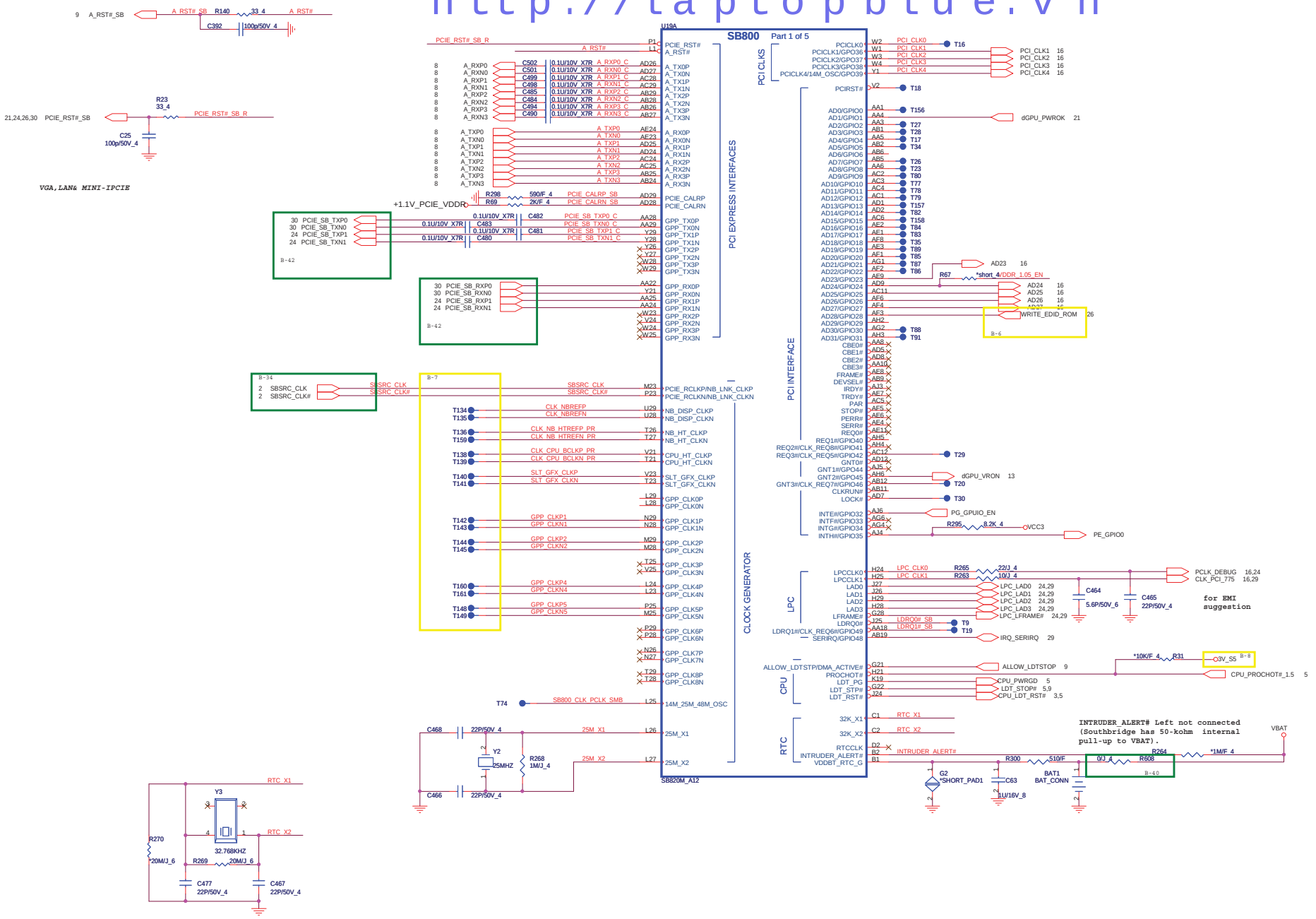
PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVDD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVDD	+1.1V
VDD18_MEM	+1.8V	PLLVDD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDLT18	+1.8V
IOPLLVDD18	+1.8V	VDDLT33	NC





Quanta Computer Inc.
PROJECT : ZN8

Size	Document Number	Rev
	RS880M-Power	1A
Date: Monday, March 22, 2010	Sheet 11 of 40	



Quanta Computer Inc.

PROJECT : ZN8

Size	Document Number	Rev
	SB820-PCIE/PCI/CPU/LPC 1/4	1A

Date: Monday, March 22, 2010 Sheet 12 of 40

NC only ,Can't be install

3V_S5 R41 *2.2K/J_4 SB_TEST0
R37 *2.2K/J_4 SB_TEST1
B-8 R51 *2.2K/J_4 SB_TEST2

3V_S5 B-48 R609 *2.2K/J_4 PCIE_WAKE#

VCC3 R73 2.2K/J_4 PCLK_SMB
R74 2.2K/J_4 PDAT_SMB
SCL0/SDATA0 is 3V tolerance AMD datasheet define it
Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer

3V_S5 B-8 R36 2.2K/J_4 SB_SMBCLK1
R47 2.2K/J_4 SB_SMBDATA1
SCL1/SDATA1 is 3V/S5 tolerance AMD datasheet define it

3V_S5 B-8 R33 2.2K/J_4 SB_SCLK2
R32 2.2K/J_4 SB_SDATA2
R186 *2.2K/J_4 DNBSWON#
SCL2/SDATA2 is 3V/S5 tolerance AMD datasheet define it

VCC3 R52 *4.7K/J_4 SUS_STAT#

VCC3 B-9 R80 100K/F_6
dGPU_VRON 2ms MXM_PWR_EN
21 MXM_PWREN
29 MXMPWR_EN MXMPWR_EN
12 dGPU_VRON
D5 RB501V-40
C107 0.1u/10V_4
D4 *SW@RB501V-40
>1mS delay is required between all MXM power rail stable and MXM_PWREN(enables the module internal power)

CN1 3V_S5 C23 10P/50V_4
SB_JTAG_TCK
SB_JTAG_TDO
SB_JTAG_TDI
SB_TEST1
SB_JTAG_RST#
*S/W JTAG DEBUG
SB JTAG

41 ACZ_SDOUT_AUDIO ACZ_SDOUT_AUDIO R273 33/J_4 ACZ_SDOUT
21 MXM_SDOUT_HDMI MXM_SDOUT_HDMI R249 33_4C478 *10P/50V_4
41 ACZ_SYNC_AUDIO ACZ_SYNC_AUDIO R277 33/J_4 ACZ_SYNC
21 MXM_SYNC_HDMI MXM_SYNC_HDMI R247 33_4C479 *10P/50V_4
41 ACZ_BITCLK_AUDIO ACZ_BITCLK_AUDIO R271 33/J_4 ACZ_BCLK
21 MXM_BIT_CLK_HDMI MXM_BIT_CLK_HDMI R248 33_4C75 10P/50V_4
41 ACZ_RST#_AUDIO ACZ_RST#_AUDIO R281 33/J_4 ACZ_RST#
21 MXM_RST#_R MXM_RST#_R R250 33_4
ACZ_SDIN0 ACZ_SDIN0 41
ACZ_SDIN1 ACZ_SDIN1 21
If the VDDIO_AZ_S power rail is configured for 1.5V_S5 then AZ_SDIN[3:0] can not be connected to 3.3-V devices.

2,3,5,9,10,11,12,14,15,16,17,18,19,20,21,22,23,24,25,26,27,29,30,31,33,34,38,39,41 VCC3 VCC3

USBCLK/14M_25M_48M_OSC pin is CLK input pin when EXT CLKGEN mode.
It is output CLK source when INT CLKGEN mode.

U19D
SB800 Part 4 of 5

PCI_PME#/GEVENT4#
RI#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/GEVENT23#
GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
NB_PWRGD
RSMRST#
ACPI / WAKE UP EVENTS

29 SUSB# SUSB#
29 SUSC# SUSC#
29 DNBSWON# DNBSWON#
16 SB_PWRGD_IN SB_PWRGD_IN
9 SUS_STAT# SUS_STAT#
SB_TEST0
SB_TEST1
SB_TEST2
29 SIO_A20GATE SIO_A20GATE
29 SIO_RCIN# SIO_RCIN#
T70 LANLINK_STATE#
29 SIO_EXT_SMI# SIO_EXT_SMI#
29 SIO_EXT_SCI# SIO_EXT_SCI#
T71 SYS_RST#
B-48 30 PCIE_WAKE# PCIE_WAKE#
T73 IR_RX1
5 CPU_THERMTRIP# R57 *0/short_4 SB_THERMTRIP#
16 NB_PWRGD_IN
29 ICH_RSMRST# B-53 R610 *0_4 R611 22K C703 4.7U/6.3V_6 3V_S5

USB 1.1 USB MISC

USB_FSD1P/GPIO186
USB_FSD1N
USB_FSD0P/GPIO185
USB_FSD0N

USB 2.0

USB_HSD13P
USB_HSD13N
USB_HSD12P
USB_HSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N

USB_CARDP 22
USB_CARDN 22
USB_FDS12P 25
USB_FSD12N 25
USBP10+ 25
USBP10- 25
USBP9+ 25
USBP9- 25
USBP8+ 25
USBP8- 25
USBP7+ 24
USBP7- 24
USBP6+ 24
USBP6- 24
USBP5+ 25
USBP5- 25
USBP4+ 25
USBP4- 25
USBP3+ 30
USBP3- 30
USBP2+ 30
USBP2- 30
USBP1+ 30
USBP1- 30
USBP0+ 30
USBP0- 30

MULTI-TOUCH
Dongle
USB
CAMERA
BLUETOOTH
TV MINI
CARD
WLAN MINI
CARD
Side
USB
Side
USB
USB
board
USB
board
USB
board
USB
board

GPIO

41 SPKR SPKR
2,17,18,19,20,24 PCLK_SMB PCLK_SMB
2,17,18,19,20,24 PDAT_SMB PDAT_SMB
26 SB_SMBCLK1 SB_SMBCLK1
26 SB_SMBDATA1 SB_SMBDATA1
21,27,29 dGPU_PRSNT#
T25 CRD_CLKREQ#
T11
2 EXT_SB_OSC
SB_GPIO_PCIE_RST#
T31 MXM_PWR_EN
T33 SB_GPIO59

CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LLB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT7#
GBE_LED0/GPIO183
GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STAT0/GEVENT11#
CLK_REQG#/GPIO65/OSCIN

USB OC

T72 OC7#
T3 OC6#
T5
T4 OC4#
SB_JTAG_TDO
SB_JTAG_TCK
SB_JTAG_TDI
SB_JTAG_RST#

BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/TRST#/GEVENT12#

HD audio interface is +3VS5 voltage

16 ACZ_SDOUT
R56 *10K/F_4 ACZ_BCLK
ACZ_SDOUT
R422 *10K/F_4 ACZ_SDIN0
R144 *10K/F_4 ACZ_SDIN1
R272 *10K/F_4 ACZ_SDIN2
R59 *10K/F_4 ACZ_SDIN3
ACZ_SYNC
ACZ_RST#

AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#
HD AUDIO

3V_S5 B-8
R276 10K/F_4 GBE_COL
R63 10K/F_4 GBE_CRS
R58 10K/F_4 GBE_MDIO
R65 10K/F_4 GBE_RXERR
R64 10K/F_4 GBE_PHY_INTR

GBE_COL
GBE_CRS
GBE_MDCK
GBE_MDIO
GBE_RXCLK
GBE_RXD3
GBE_RXD2
GBE_RXD1
GBE_RXD0
GBE_RXCTL/RXDV
GBE_RXERR
GBE_TXCLK
GBE_TXD3
GBE_TXD2
GBE_TXD1
GBE_TXD0
GBE_TXCTL/TXEN
GBE_PHY_PD
GBE_PHY_RST#
GBE_PHY_INTR
GBE LAN

T2 ADP_PRES0
T6

PS2_DAT/SDA4/GPIO187
PS2_CLK/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
FC_RST#/GPO160
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192
EMBEDDED CTRL

SCL2/GPIO193 SB_SCLK2
SDA2/GPIO194 SB_SDATA2
SCL3_LV/GPIO195 SB_GPIO195
SDA3_LV/GPIO196 SB_GPIO196
EC_PWM0/EC_TIMER0/GPIO197
EC_PWM1/EC_TIMER1/GPIO198
EC_PWM2/EC_TIMER2/GPIO199 GPIO199 16
EC_PWM3/EC_TIMER3/GPIO200 GPIO200 16

KSI_0/GPIO201
KSI_1/GPIO202
KSI_2/GPIO203
KSI_3/GPIO204
KSI_4/GPIO205
KSI_5/GPIO206
KSI_6/GPIO207
KSI_7/GPIO208
KSO_0/GPIO209
KSO_1/GPIO210
KSO_2/GPIO211
KSO_3/GPIO212
KSO_4/GPIO213
KSO_5/GPIO214
KSO_6/GPIO215
KSO_7/GPIO216
KSO_8/GPIO217
KSO_9/GPIO218
KSO_10/GPIO219
KSO_11/GPIO220
KSO_12/GPIO221
KSO_13/GPIO222
KSO_14/GPIO223
KSO_15/GPIO224
KSO_16/GPIO225
KSO_17/GPIO226
EMBEDDED CTRL

SB_GPIO195 R266 10K/F_4
SB_GPIO196 R267 10K/F_4

SB820M_A12

A10 R257 22_4 CLK_48M_USB 2,22
G19 USB_RCOMP_SB R44 11.8K/F_6
USB_RCOMP

Quanta Computer Inc.
PROJECT : ZN8

Size	Document Number	Rev
	SB820-ACPI/GPIO/USB 2/4	1A

Date: Monday, March 22, 2010 Sheet 13 of 40

SATA PORT 0,1,2,3
can support AHCI
mode

SATA1

SATA ODD

U19B

SB800
Part 2 of 5

SATA_TX0+ / SATA_TX0- → AH9 / AJ9 → SATA_TX0P / SATA_TX0N
SATA_RX0- / SATA_RX0+ → AJ8 / AH8 → SATA_RX0N / SATA_RX0P
SATA_TX1+ / SATA_TX1- → AH10 / AJ10 → SATA_TX1P / SATA_TX1N
SATA_RX1- / SATA_RX1+ → AG10 / AF10 → SATA_RX1N / SATA_RX1P
AG12 / AF12 → SATA_TX2P / SATA_TX2N
AJ12 / AH12 → SATA_RX2N / SATA_RX2P
AH14 / AJ14 → SATA_TX3P / SATA_TX3N
AG14 / AF14 → SATA_RX3N / SATA_RX3P
AG17 / AF17 → SATA_TX4P / SATA_TX4N
AJ17 / AH17 → SATA_RX4N / SATA_RX4P
AJ18 / AH18 → SATA_TX5P / SATA_TX5N
AH19 / AJ19 → SATA_RX5N / SATA_RX5P

SERIAL ATA

Signal Name	Explanation
SATA_CALRP	SB800 A11: 800-? 1% resistor to GND. P/N:CS18062FB00(806 Ohm) SB800 A12: TBD-? 1% resistor to GND. (1K ohm)
SATA_CALRN	SB800 A11: 931-? 1% resistor to VDDAN_11_SATA. SB800 A12: TBD-? 1% resistor to VDDAN_11_SATA.

+1.1V_AVDD_SATA
R66 806/F_4 SATA_CALRP → AB14 SATA_CALRP
R68 931/F_4 SATA_CALRN → AA14 SATA_CALRN

PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF SB820

23 SATA_ACT# → AD11 SATA_ACT#/GPIO67
VCC3 R77 10K/F_4

C106 22P/50V_4 — SATA_X1 → AD16 SATA_X1
Y5 25MHZ, R81 1M/J_4
C105 22P/50V_4 — SATA_X2 → AC16 SATA_X2

B-54: SB_SO, SB_SI, SB_SCK, SB_SCE# → J5, E2, K4, K9 SPI_DI/GPIO164, SPI_DO/GPIO163, SPI_CLK/GPIO162, SPI_CS1#/GPIO165
T8 → G2 ROM_RST#/GPIO161

SPI ROM

FLASH

FC_CLK → AH28 → T110
FC_FBCLKOUT → AG28 → T93
FC_FBCLKIN → AF26 → T112
FC_OE#/GPIOD145 → AF28 → T100
FC_AVD#/GPIOD146 → AG29 → T113
FC_WE#/GPIOD148 → AG26 → T105
FC_CE1#/GPIOD149 → AF27 → T108
FC_CE2#/GPIOD150 → AE29 → T109
FC_INT1/GPIOD144 → AF29 → T92
FC_INT2/GPIOD147 → AH27 → T103
FC_ADQ0/GPIOD128 → AJ27 → T95
FC_ADQ1/GPIOD129 → AJ26 → T96
FC_ADQ2/GPIOD130 → AH25 → T104
FC_ADQ3/GPIOD131 → AH24 → T107
FC_ADQ4/GPIOD132 → AG23 → T94
FC_ADQ5/GPIOD133 → AH23 → T99
FC_ADQ6/GPIOD134 → AJ22 → T97
FC_ADQ7/GPIOD135 → AG21 → T98
FC_ADQ8/GPIOD136 → AF21 → T102
FC_ADQ9/GPIOD137 → AH22 → T101
FC_ADQ10/GPIOD138 → AJ23 → T111
FC_ADQ11/GPIOD139 → AF23 BOARD_ID0
FC_ADQ12/GPIOD140 → AJ24 BOARD_ID1
FC_ADQ13/GPIOD141 → AJ25 BOARD_ID2
FC_ADQ14/GPIOD142 → AG25 BOARD_ID3
FC_ADQ15/GPIOD143 → AH26 BOARD_ID4

FANOUT0/GPIO52 → W5
FANOUT1/GPIO53 → W6
FANOUT2/GPIO54 → Y9
FANIN0/GPIO56 → W7 WWAN_DET# → T22
FANIN1/GPIO57 → V9 CPPE_NC1# → T15
FANIN2/GPIO58 → W8 CRD_REQ1# → T21

HW MONITOR

TEMPIN0/GPIO171 → B6 TEMPIN0
TEMPIN1/GPIO172 → A6 TEMPIN1
TEMPIN2/GPIO173 → A5 MB_THRMDA_SB
TEMPIN3/TALERT#/GPIO174 → B5 THERM_ALERT# → THERM_ALERT# 5,29
TEMP_COMM → C7 TEMP_COMM R38 *0/short_4
VIN0/GPIO175 → A3 SB_GPIO175
VIN1/GPIO176 → B4 SB_GPIO176
VIN2/GPIO177 → A4 SIDE_PORT_ID0
VIN3/GPIO178 → C5 SIDE_PORT_ID1
VIN4/GPIO179 → A7 R612 *0_4 SB_BIOS_WP#
VIN5/GPIO180 → B7 GPIO180
VIN6/GBE_STAT3/GPIO181 → B8 CLR_BIOS_DATA
VIN7/GBE_LED3/GPIO182 → A8 CLR_PASSWD

NC1 → G27
NC2 → Y2

SB820M_A12

IF THERE IS NO IDE, TEST POINTS FOR DEBUG BUS IS MANDATORY

TEMPIN0 R252 10K/F_4
TEMPIN1 R259 10K/F_4
MB_THRMDA_SB R260 10K/F_4
SB_GPIO175 R262 10K/F_4
SB_GPIO176 R254 10K/F_4
SIDE_PORT_ID0 R261 10K/F_4
SIDE_PORT_ID1 R253 10K/F_4
GPIO180 R258 10K/F_4

VCC3
R323 *10K/F_4 BOARD_ID0 R332 10K/F_4
R322 *10K/F_4 BOARD_ID1 R331 10K/F_4
R321 *10K/F_4 BOARD_ID2 R330 10K/F_4
R320 *10K/F_4 BOARD_ID3 R329 10K/F_4
R327 *10K/F_4 BOARD_ID4 R328 *10K/F_4

	ID4	ID3	ID2	ID1	ID0
0				UMA	14"
1				Discrete	15"

8Mbit , SPI

B-54
3V_S5
R613 *10K_4
R614 *1K/F_4
R615 *10K_4
SB_SCE#
SB_SCK R616 *47R_4
SB_SI R617 *47R_4
SB_SO R618 *15R_4
SB_BIOS_WP#
U31 CE# SCK SI SO WP# VDD HOLD# VSS *MX25L1605A
U32 CE# SCK SI SO WP# VDD HOLD# VSS *MX25L1605A
C704 *0.1U/25V/4

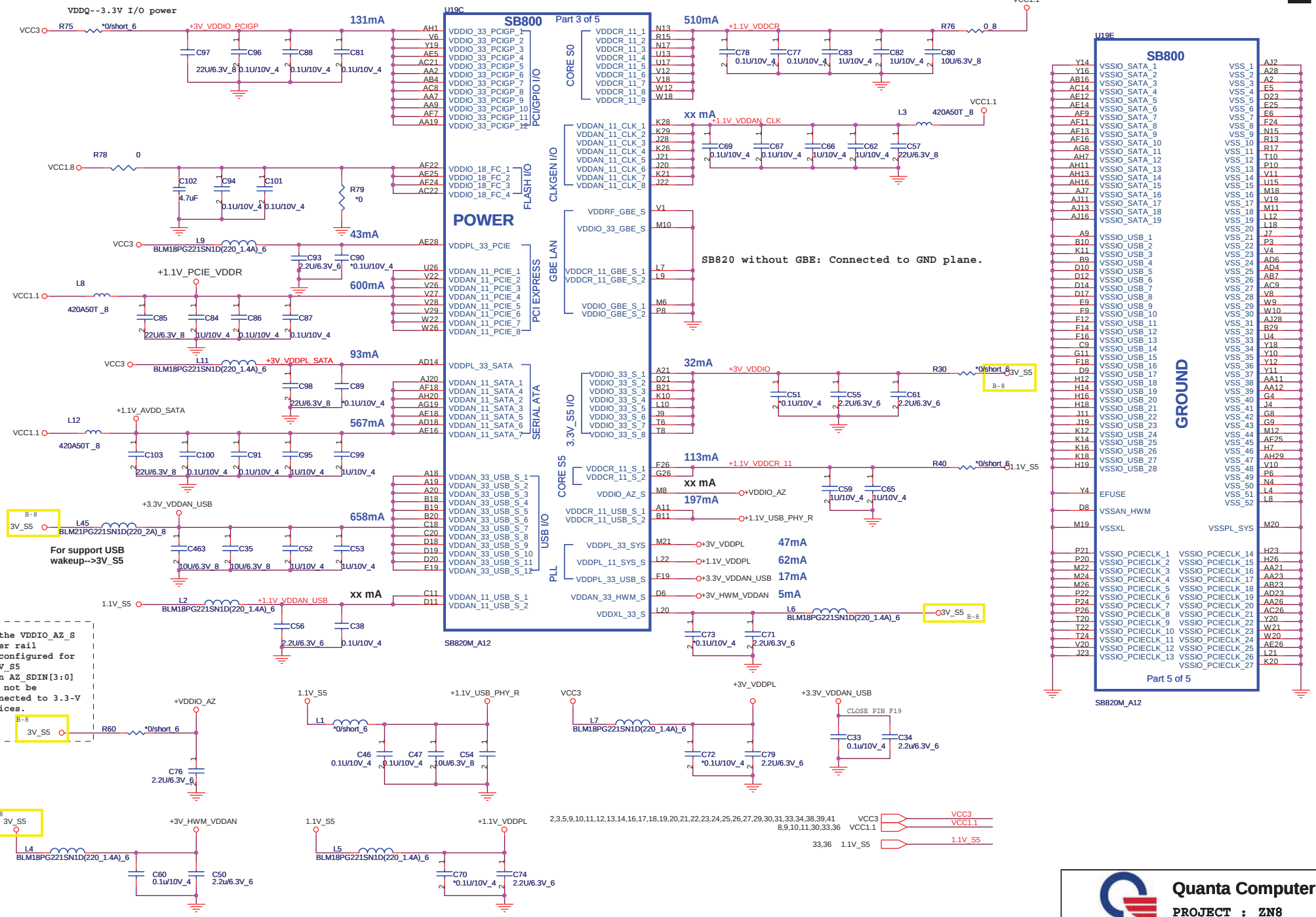
VCC3
R340 10K/F_4
R339 10K/F_4
JP2
CLR_BIOS_DATA
CLR_PASSWD
CONN RCPT 4x2

Quanta Computer Inc.
PROJECT : ZN8

Size	Document Number	Rev
	SB820-SATA/IDE/HWM/SPI 3/4	1A

Date: Monday, March 22, 2010 Sheet 14 of 40

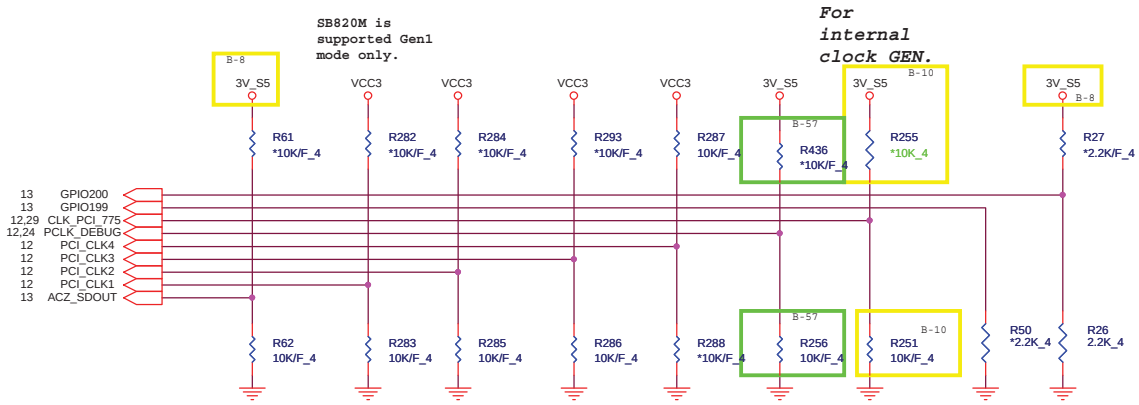
PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE



Quanta Computer Inc.	
PROJECT : ZN8	
Size	Document Number: SB820-PWR/DECOUPLING 4/4 — Rev: 1A
Date: Monday, March 22, 2010	Sheet 15 of 40

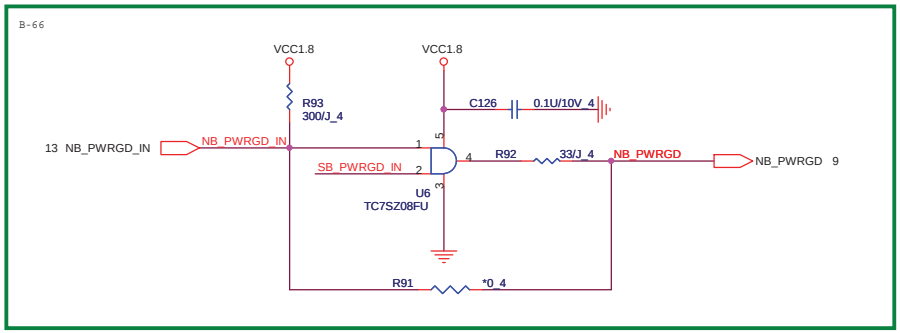
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

REQUIRED STRAPS



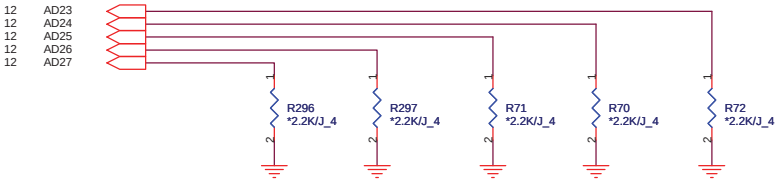
	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	INT. CLKGEN ENABLED DEFAULT	H, H=Reserved H, L=SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1 DEFAULT	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE	EC DISABLED DEFAULT	EXT. CLKGEN ENABLE	L,H=LPC ROM DEFAULT L, L=FWH ROM

internal have pull Hi 10K



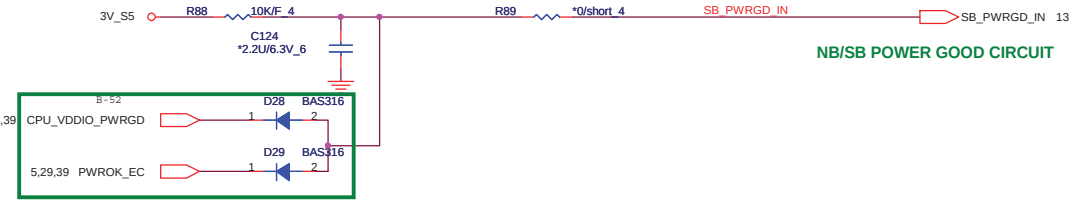
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	DISABLE I2C ROM DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	ENABLE I2C ROM use REQ3# as SDA use GNT3# as SCL	ENABLE PCI MEM BOOT

NB_PWRGD_IN:
RS880/RX881 = 1.8V;
Do NOT share it with SB_PWRGD when use Internal Clk Gen (Need SB PLL initialize firstly)



NB/SB POWER GOOD CIRCUIT

Quanta Computer Inc.

PROJECT : ZN8

Size	Document Number	Rev
	SB820-STRAPS/PWRGD	1A

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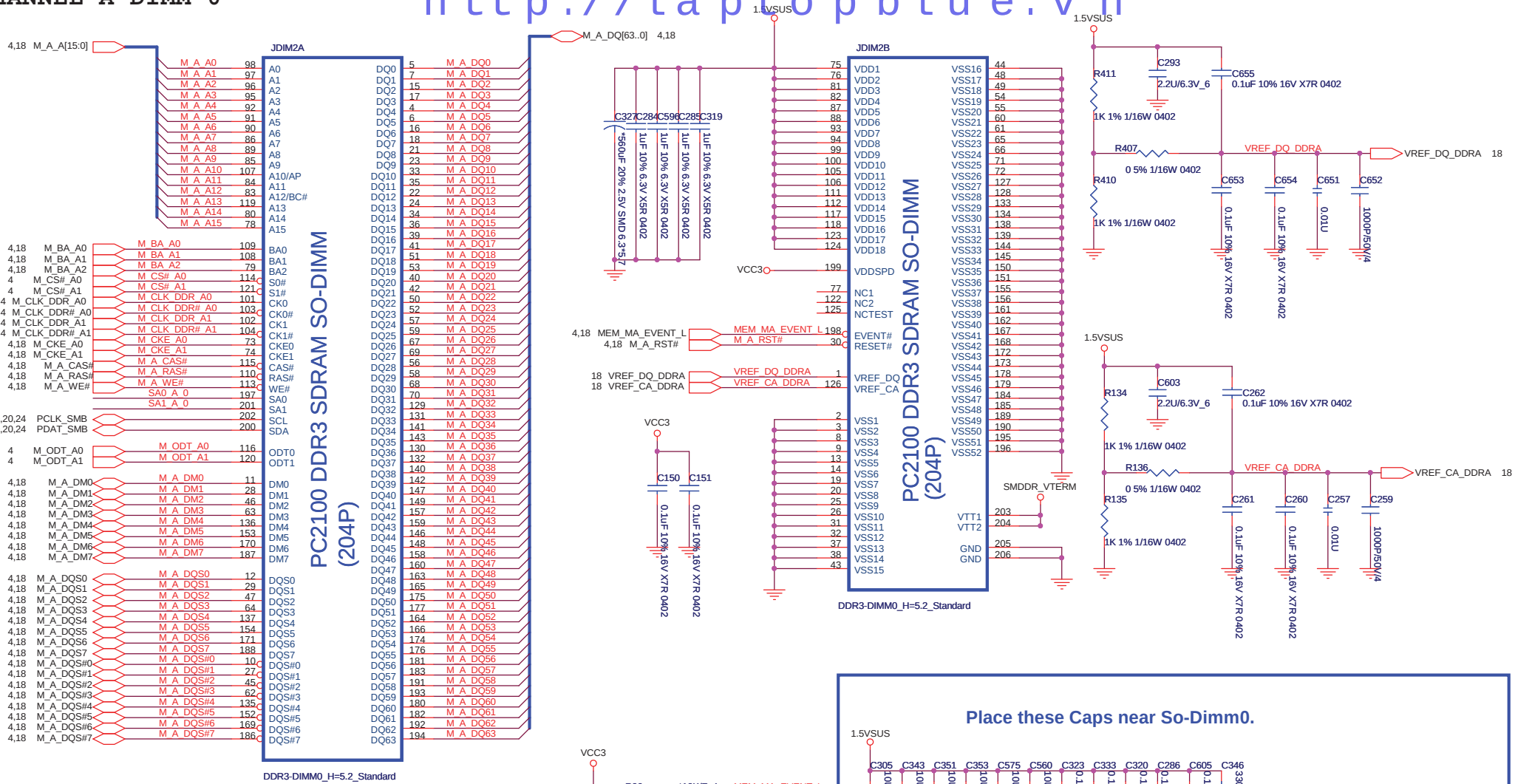
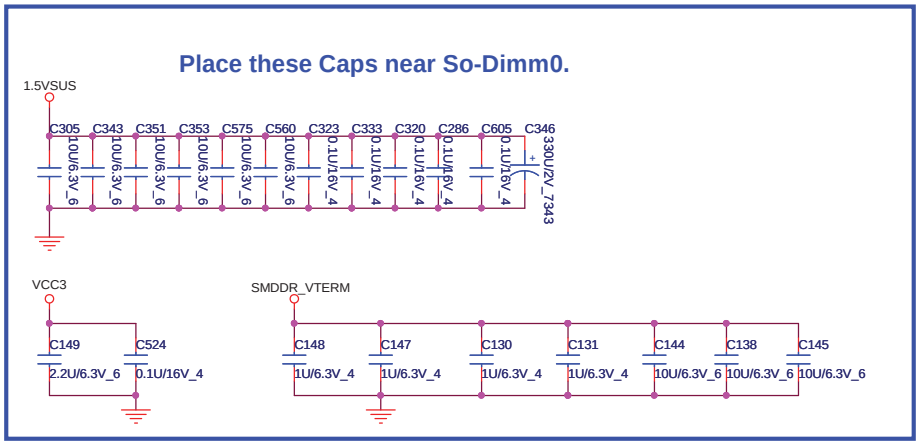
CHANNEL A DIMM 0

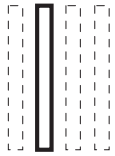


Place these Caps near So-Dimm0.



FOX H:9.2 white

PCB Placement



SPD SA0	0
SPD SA1	0

R98 0 5% 1/16W 0402 SA1_A_0
R99 0 5% 1/16W 0402 SA0_A_0

AM3

Quanta Computer Inc.			
PROJECT : ZN8			
Size	Document Number: DDR3 CHA DIMM 0		Rev 1A
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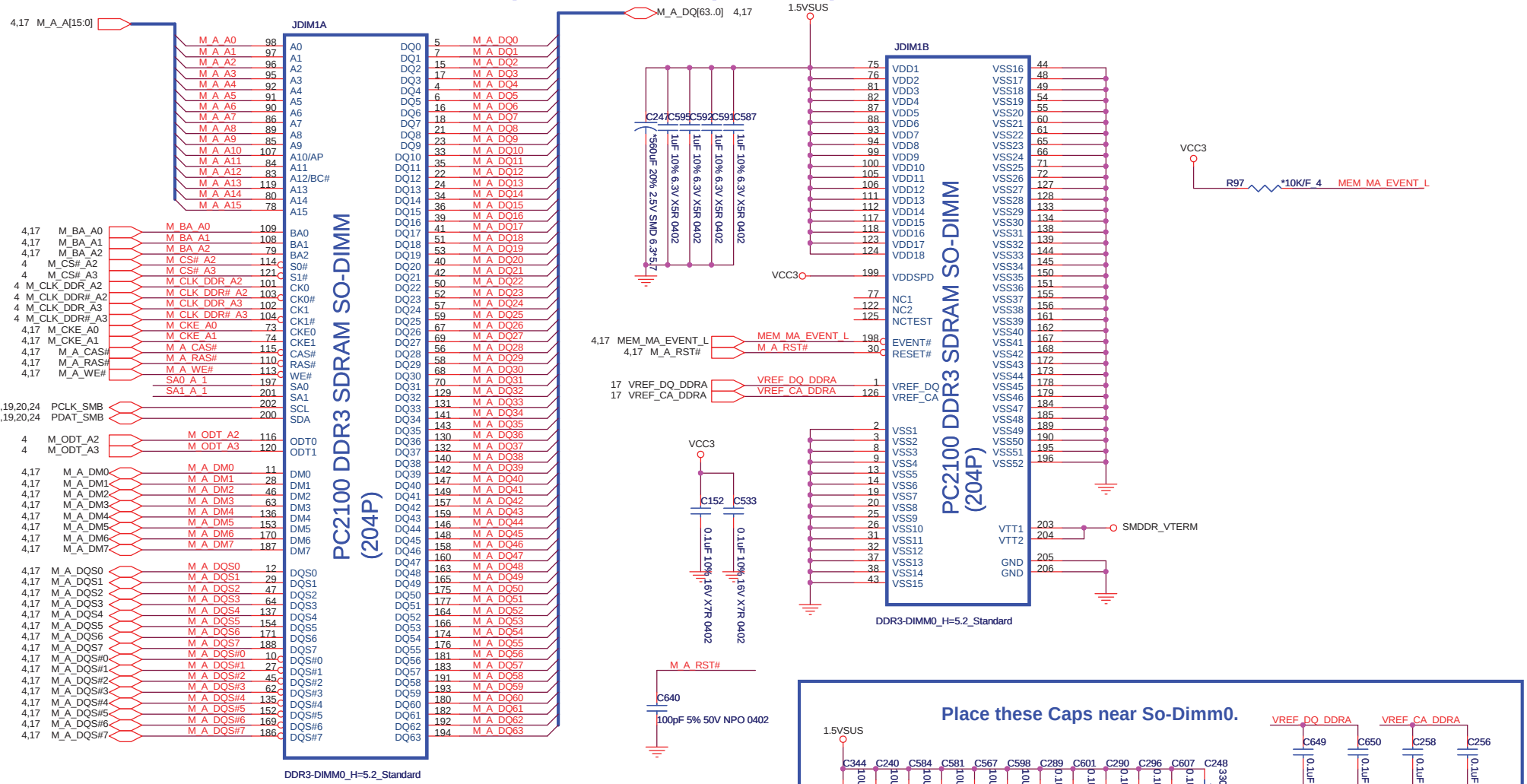
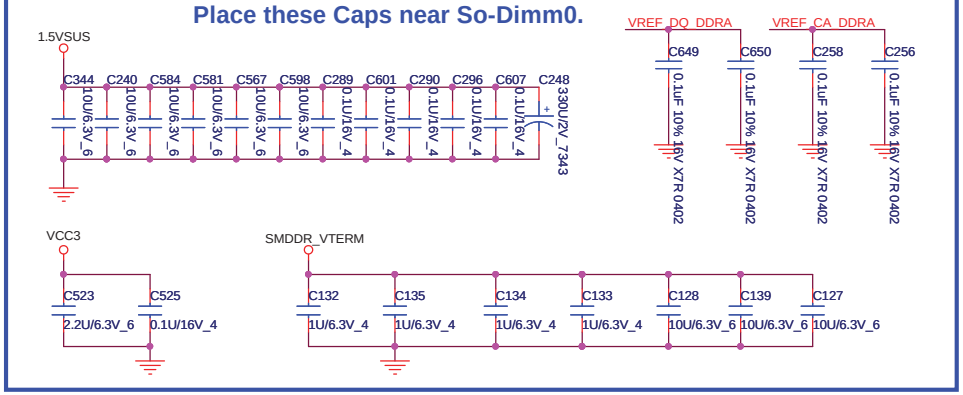
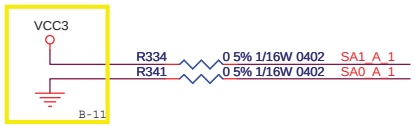
CHANNEL A DIMM 1



Place these Caps near So-Dimm0.



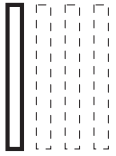
SPD SA0	1
SPD SA1	0



AM3

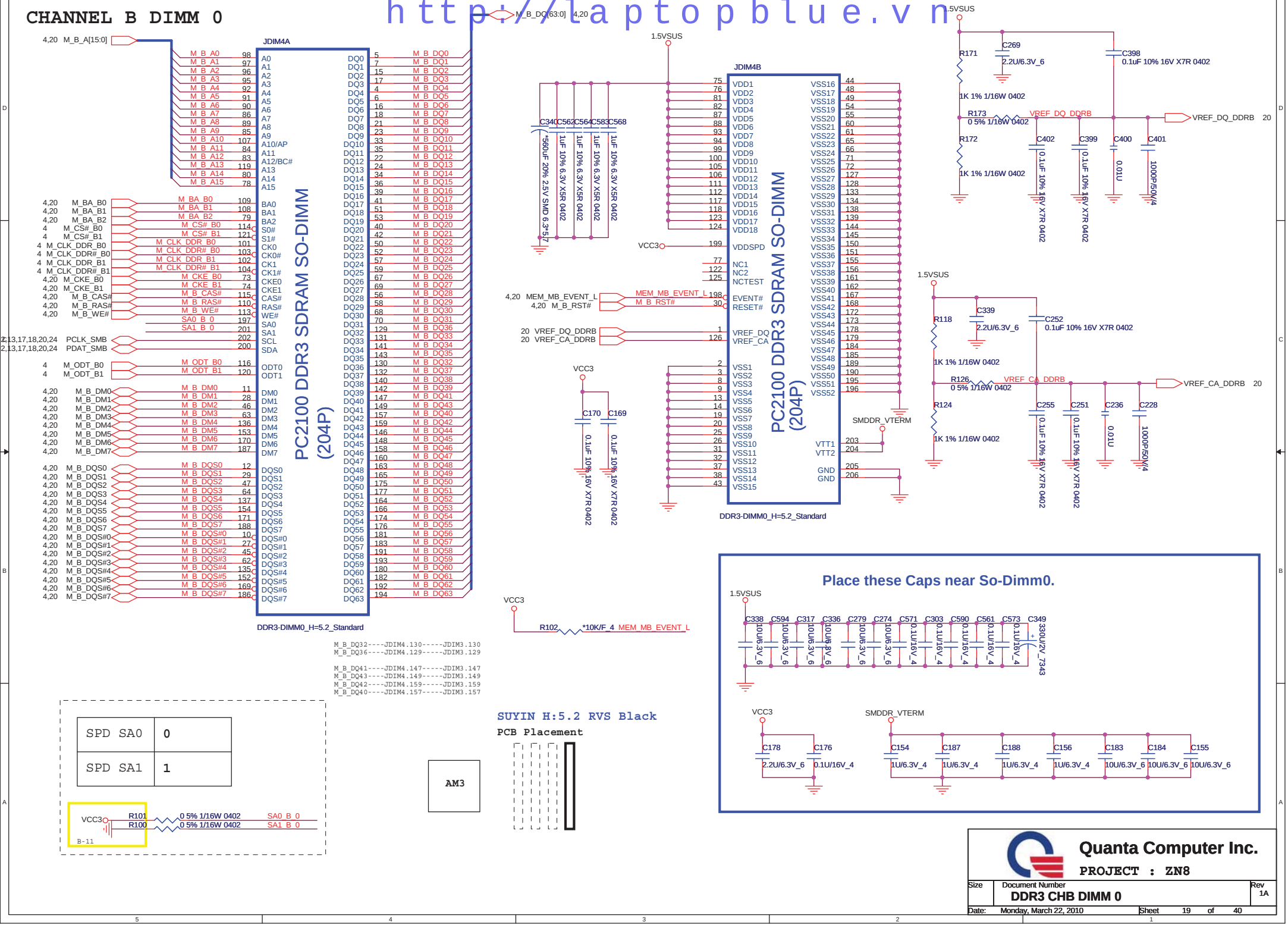
FOX H:5.2 white

PCB Placement



Quanta Computer Inc.			
PROJECT : ZN8			
Size	Document Number: DDR3 CHA DIMM1		Rev 1A
Date: Monday, March 22, 2010		Sheet 18 of 40	

CHANNEL B DIMM 0

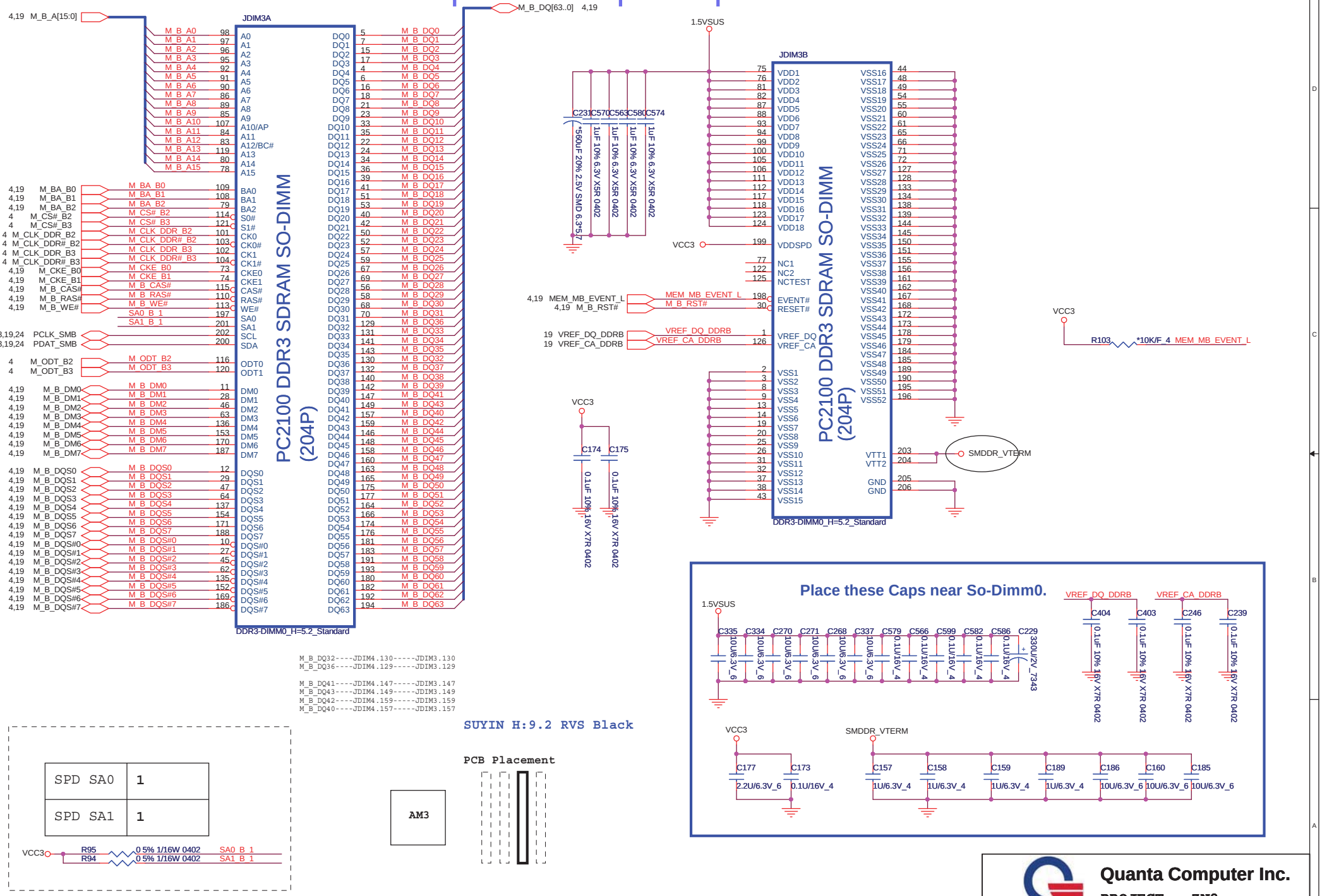


M_B_DQ32----JDIM4.130-----JDIM3.130
M_B_DQ36----JDIM4.129-----JDIM3.129

M_B_DQ41----JDIM4.147-----JDIM3.147
M_B_DQ43----JDIM4.149-----JDIM3.149
M_B_DQ42----JDIM4.159-----JDIM3.159
M_B_DQ40----JDIM4.157-----JDIM3.157

Quanta Computer Inc.		
PROJECT : ZN8		
Size	Document Number: DDR3 CHB DIMM 0	Rev: 1A
Date: Monday, March 22, 2010	Sheet 19 of 40	

CHANNEL B DIMM 1



Quanta Computer Inc.
PROJECT : ZN8

Size	Document Number	Rev
	DDR3 CHB DIMM1	1A

Date: Monday, March 22, 2010 Sheet 20 of 40

MXM Module

6/25 Change CN22 pin define and footprint at C test.

dGPU_PRSNT#	Sku
Low	MXM
High	WO/ MXM

MXM3.0	n-Vidia	AMD
LVDS	LVDS	LVDS/Int. DP
DP_D	N/A	X
DP_A	HDMI	HDMI
DP_C	Ext. DP/DVI	Ext. DP/DVI
DP_B	N/A	N/A

Thermo SMBus

MXM VIN Power switch

MXM 3V/5V Power switch

To EC

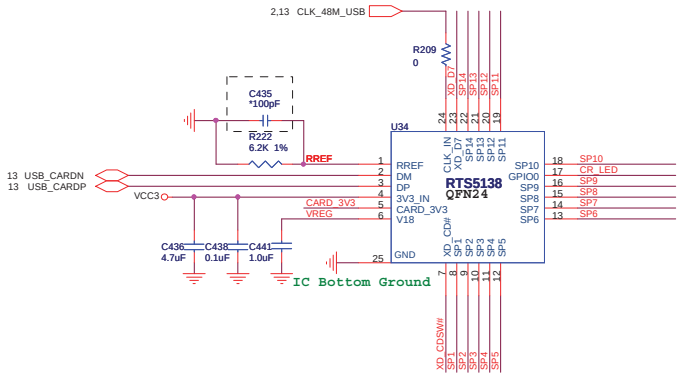
To low power status mode

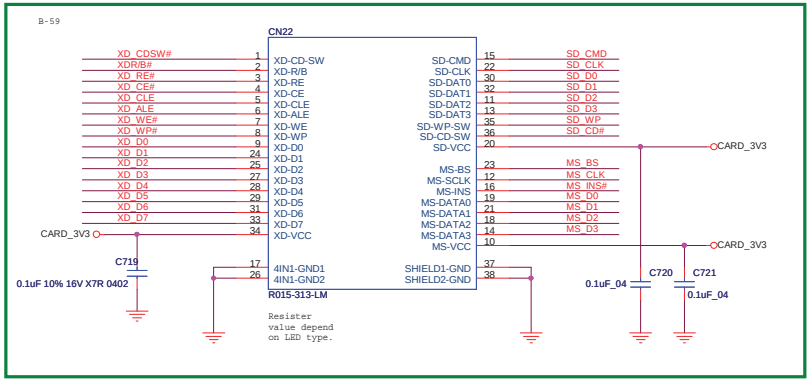
LVDS+DP CONN for MXM

MXM DP CONN for Scalar Board

For CRT Debug

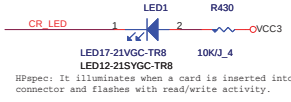
Quanta Computer Inc.
PROJECT : ZN8
MXM 3.0
Rev 1A
Monday, March 22, 2010
Sheet 21 of 40

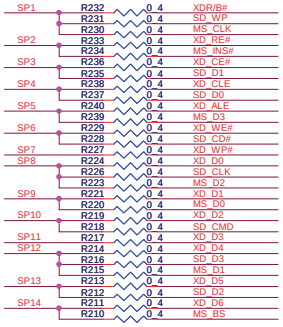


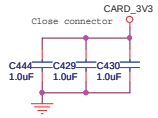


Share Pin

Share Pin	XD	MS	SD
SP1	XDR/B#	MS_CLK	SD_WP
SP2	XD_RE#	MS_INS#	
SP3	XD_CE#		SD_D1
SP4	XD_CLE	MS_D7	SD_D0
SP5	XD_ALE	MS_D3	SD_D7
SP6	XD_WE#		SD_CD#
SP7	XD_WP	MS_D6	SD_D6
SP8	XD_D0	MS_D2	SD_CLK
SP9	XD_D1	MS_D0	SD_D5
SP10	XD_D2		SD_CMD
SP11	XD_D3	MS_D4	SD_D4
SP12	XD_D4	MS_D1	SD_D3
SP13	XD_D5	MS_D5	SD_D2
SP14	XD_D6	MS_BS	







Quanta Computer Inc.

PROJECT : ZN8

Size	Document Number	Rev
	RTS5138	1A

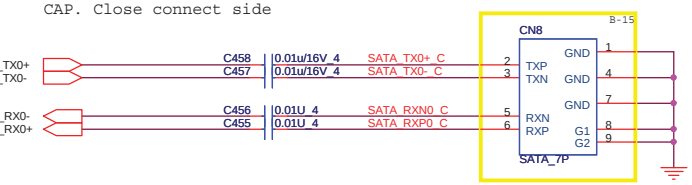
Date: Monday, March 22, 2010 Sheet 22 of 40

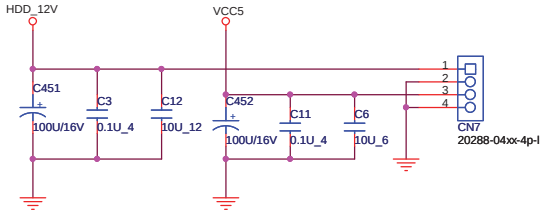
1st 2.5"/3/5" SATA HDD

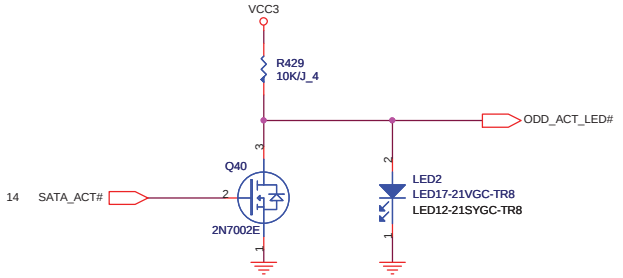
From PCH SATA

CAP. Close connect side

SATA HDD CONNECTOR





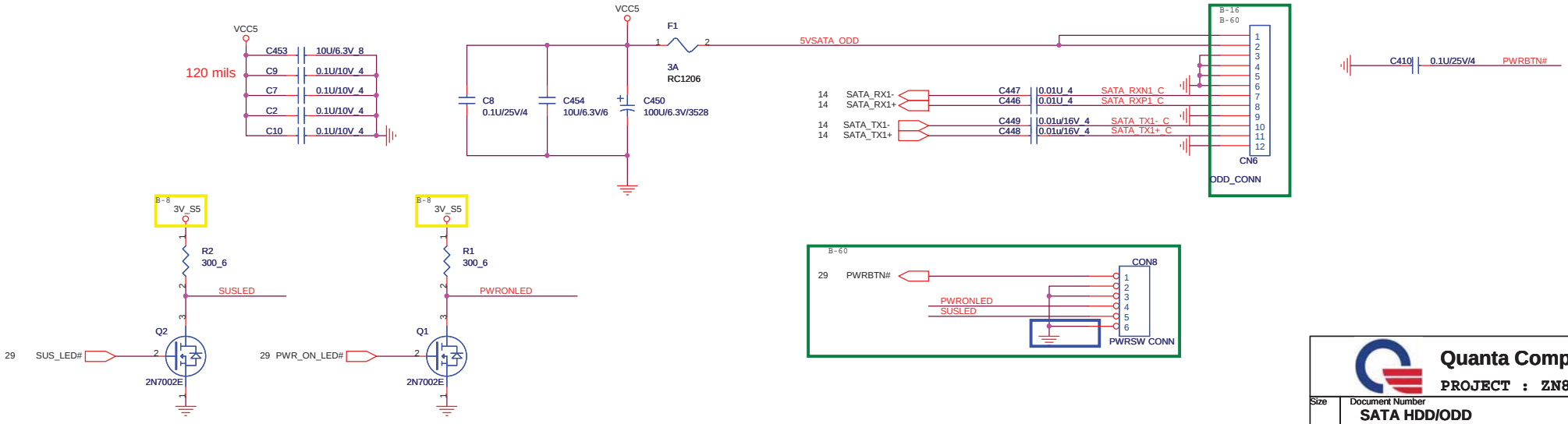


SATA CD-ROM

To SATA-HDD conn

SATA ODD CONNECTOR

USB connector same as ZN6



Quanta Computer Inc.

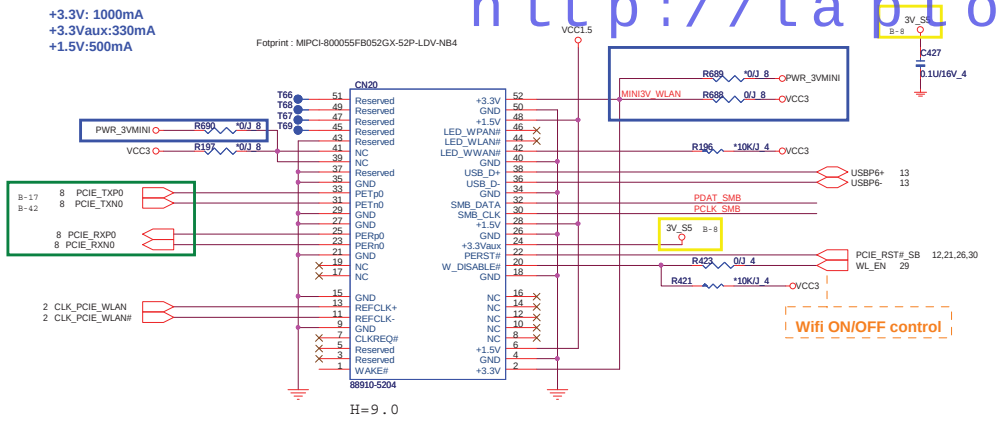
PROJECT : ZN8

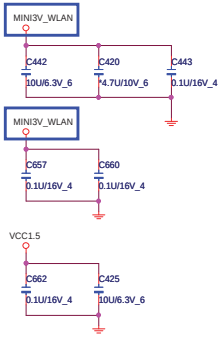
Size	Document Number	Rev
	SATA HDD/ODD	1A

Date: Monday, March 22, 2010 Sheet 23 of 40

Wireless + BT

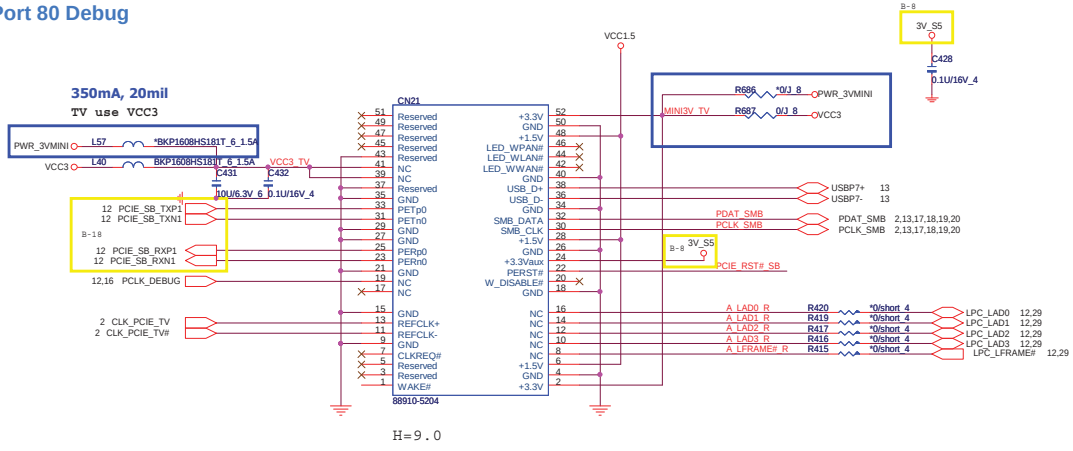
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

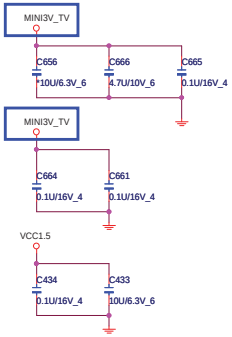


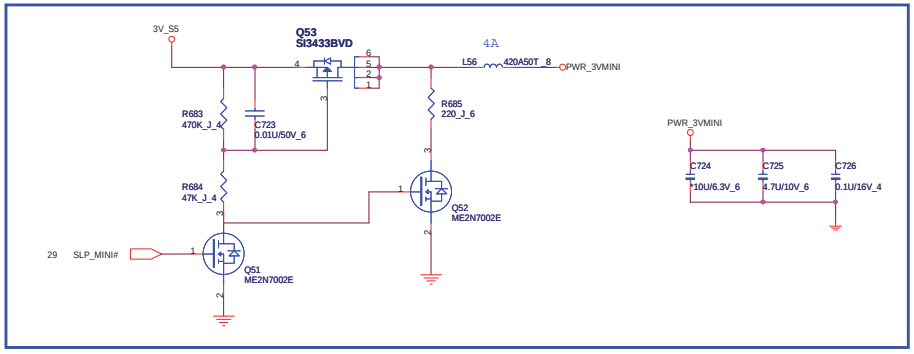


TV and Port 80 Debug

350mA, 20mil
TV use VCC3

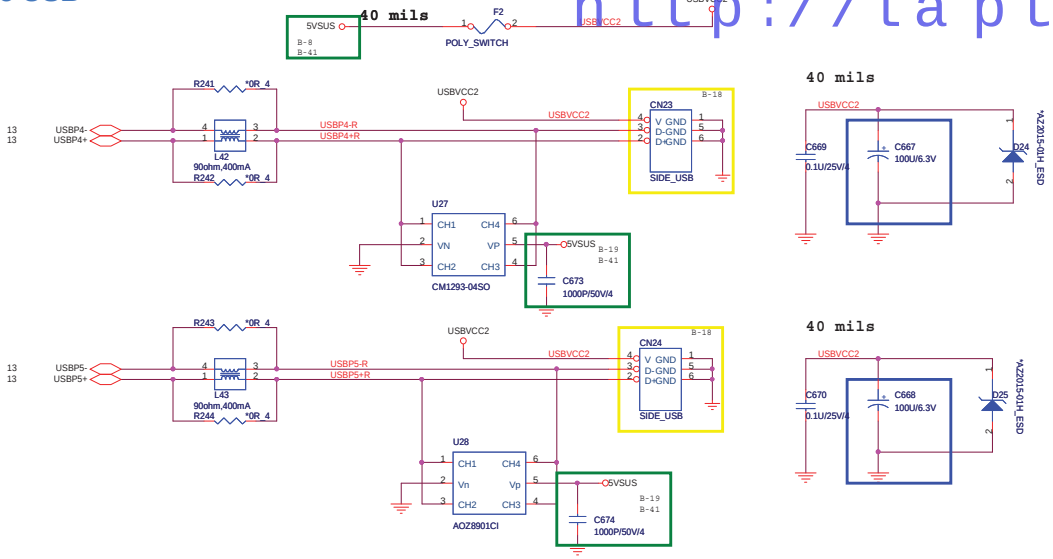


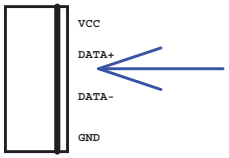




Quanta Computer Inc.			
PROJECT : ZN8			
Size	Document Number		Rev
	MINI PCIE (WLAN/TV)		1A
Date: Monday, March 22, 2010		Sheet 24 of 40	

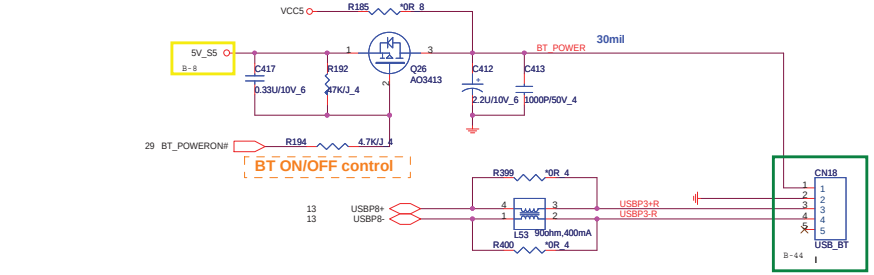
Side USB



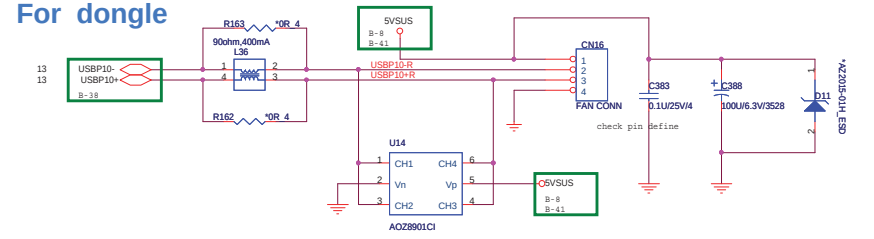


USB connector same as ZN6

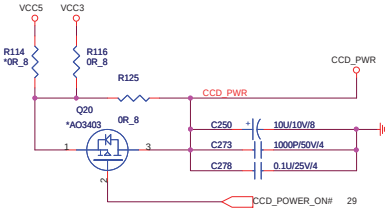
BLUETOOTH CONNECTOR



For dongle

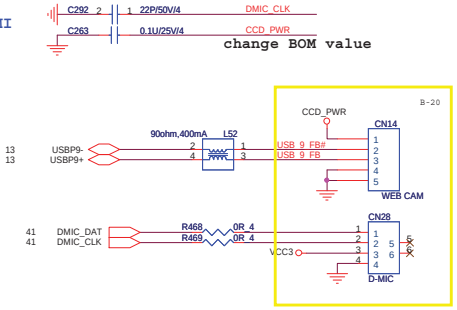


WEB CAM MODULE



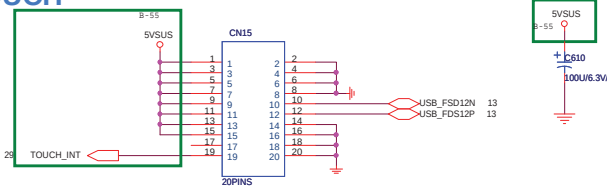
TO WEB CAM MODULE

FOR EMI



MULTI-TOUCH

HP spec:USB header for touch controller must be able to support 3.0 A.



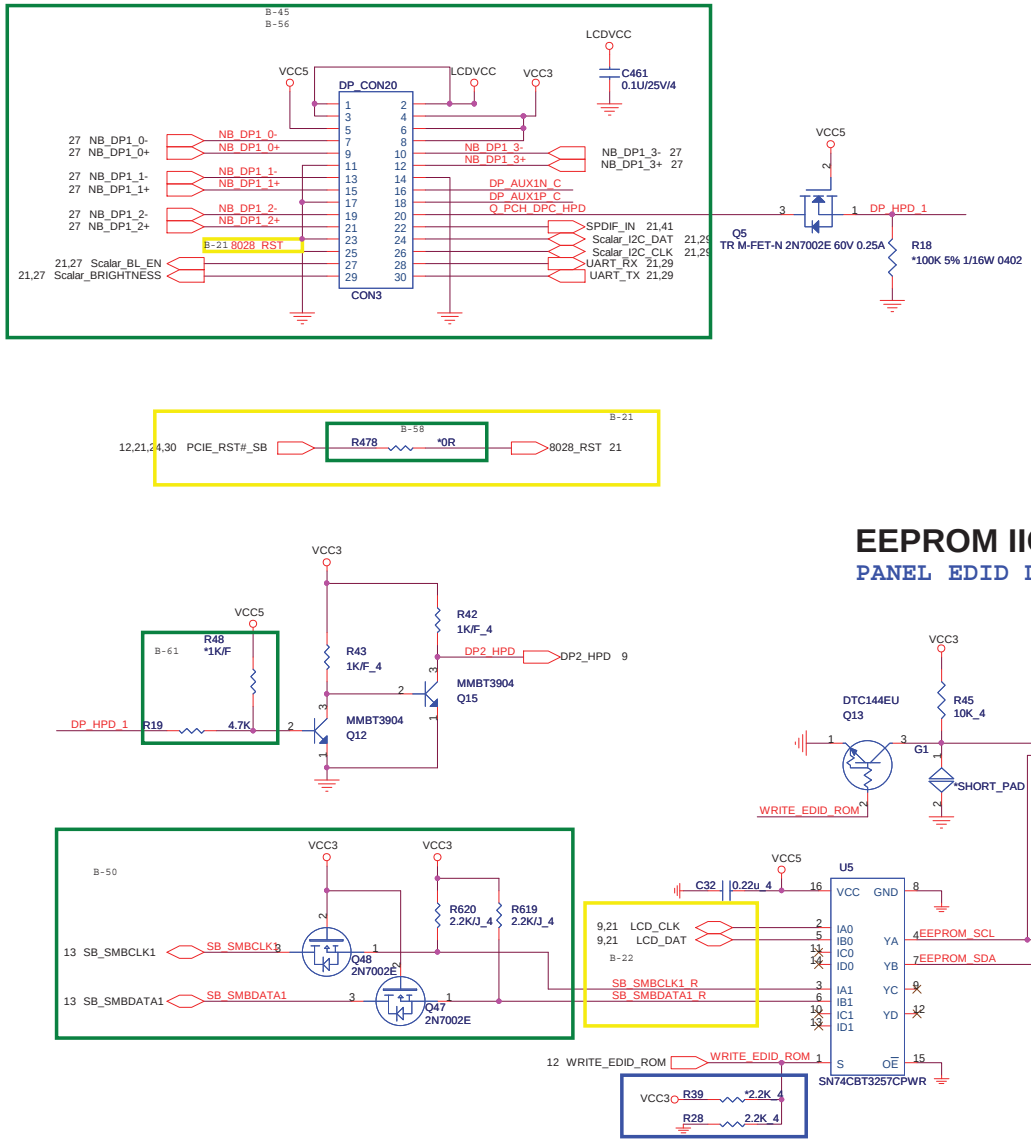
Quanta Computer Inc.

PROJECT : ZN8

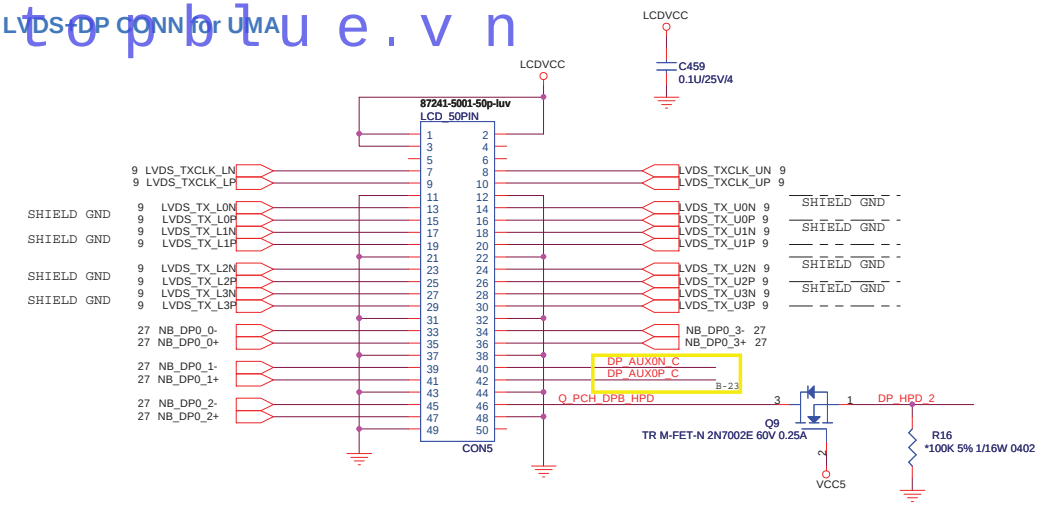
Size	Document Number	Rev
	USB/CCD/BT/MT	1A

Date: Monday, March 22, 2010 Sheet 25 of 40

UMA DP CONN for scalar Board

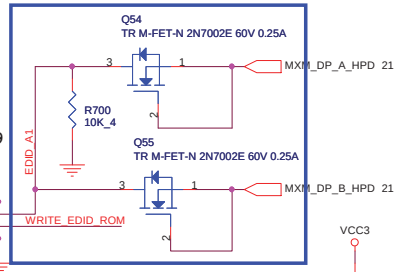


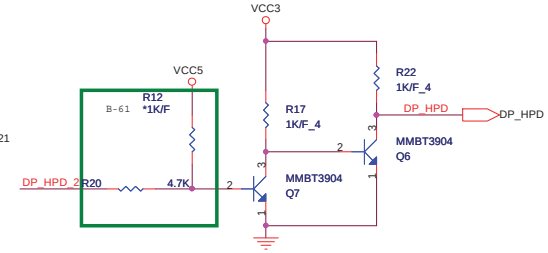
LVDS+DP CONN for UMA

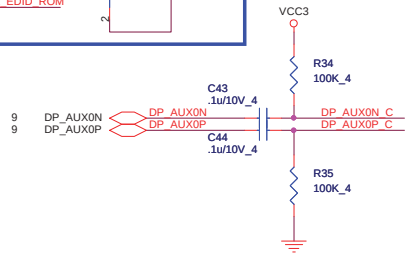


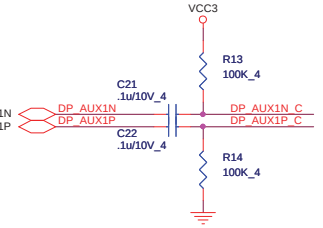
EEPROM IIC Selection

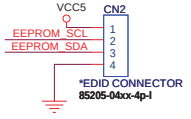
PANEL EDID DATA











Quanta Computer Inc.

PROJECT : ZN8

Size	Document Number	Rev
	Panel (DP/LVDS)	1A

Date: Monday, March 22, 2010 Sheet 26 of 40

PWM_CONTROL

H:ICH10 to DP
L:For MXM lane to DP

H:RS880 to DP
L:For MXM lane to DP

PANEL_ON	PANEL_ON_EC	LCDVCC
0	0	Power OFF
0	1	Power ON
1	0	Power ON
1	1	Power ON

Option 2
a.5V panel --- remove Q41,C675,R438,R441,D26
b.12V panel --- remove Q41,R442,D26
Option 4
remove R441,R442

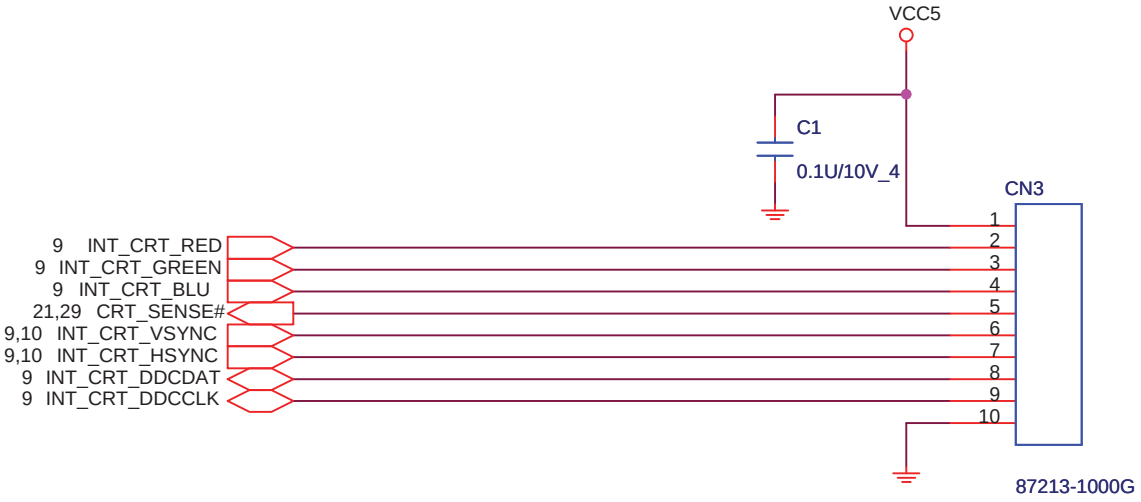
5V Converter BD
If 5V_12V_LCDEN signal NC, LCDVCC will output 5V for panel power
12V Converter BD
If 5V_12V_LCDEN signal connect to GND, LCDVCC will output 12V for panel power

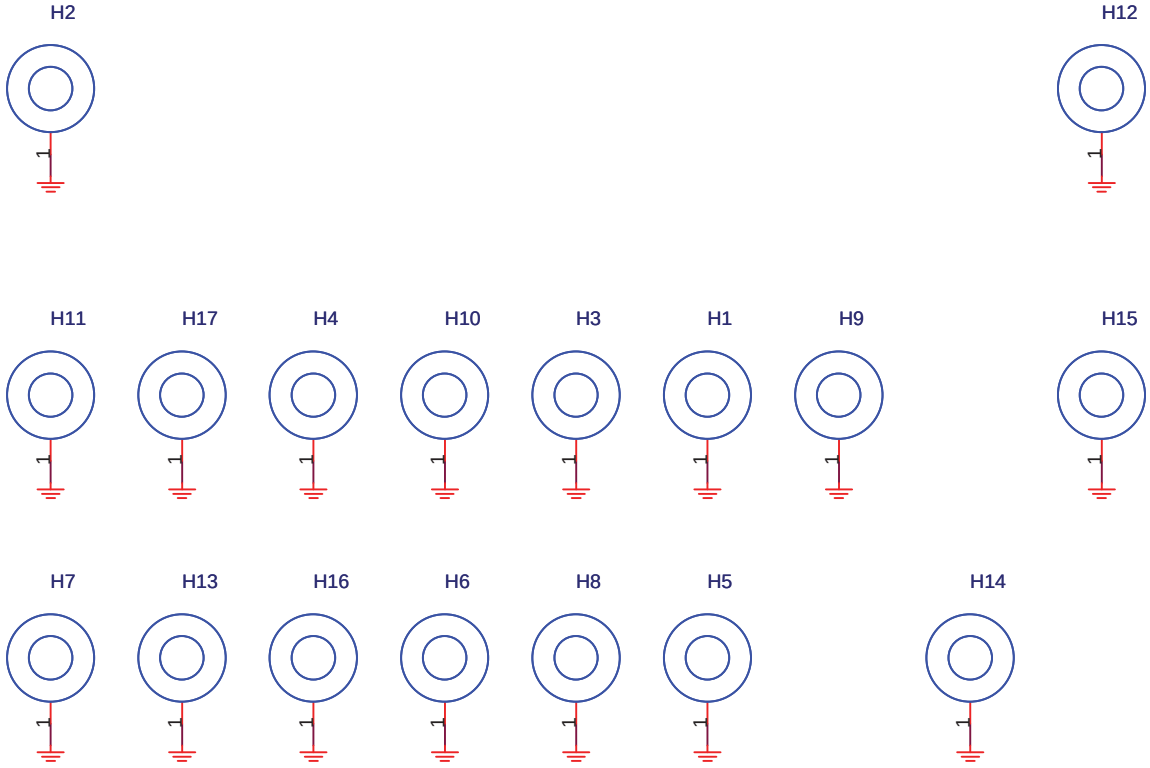
PANEL VCC CONTROL

12V/5V

Quanta Computer Inc.	PROJECT : ZN8
Size	Document Number: Panel (Control) — Rev: 1A
Date: Monday, March 22, 2010	Sheet 27 of 40

CRT for Debug





Quanta Computer Inc.		
PROJECT : ZN8		
Size	Document Number: CRT	Rev: 1A
Date: Monday, March 22, 2010	Sheet 28 of 40	

EC

Layout Note:
Place all capacitors close to IT8512.

Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.

(For ELL Power)

IT8512NX

LPC
GPIO
SM BUS
PS/2
CIR
PWM
UART port
EXTERNAL SERIAL FLASH
SPI Device
KBMX
WAKE UP
A/D D/A
CLOCK

For PS2

Input only

HWPG

8Mbit , SPI

MX25L1605A

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

Layout Note:
Place R471,R498,R534 within 500 mils from SPI Flash.Place R567 within 500mils from R534; R520 within 500mils from R498 and R570 within 500mils from R471.

Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

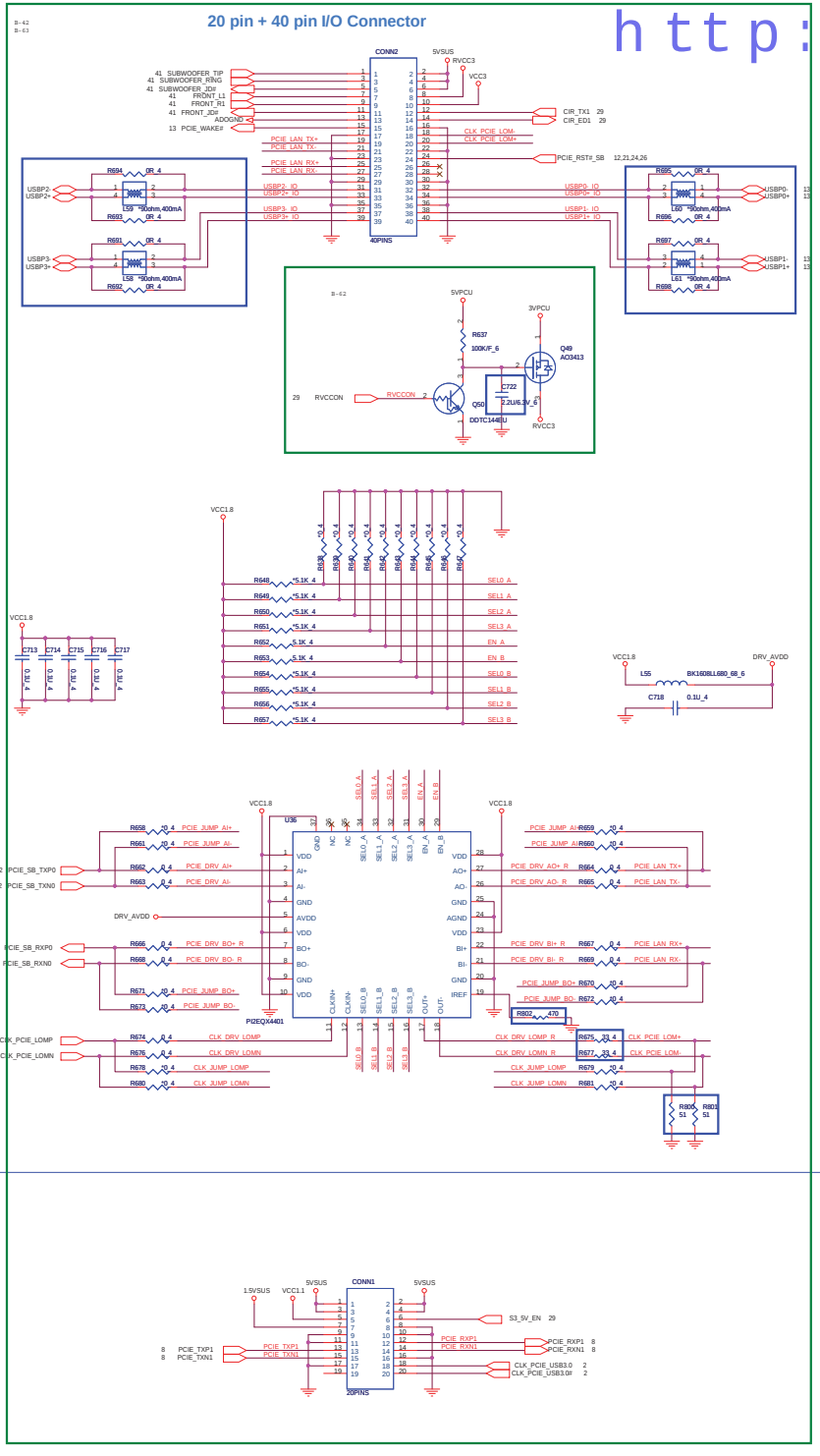
For Debug use

CON1 88502-2401-24P-L

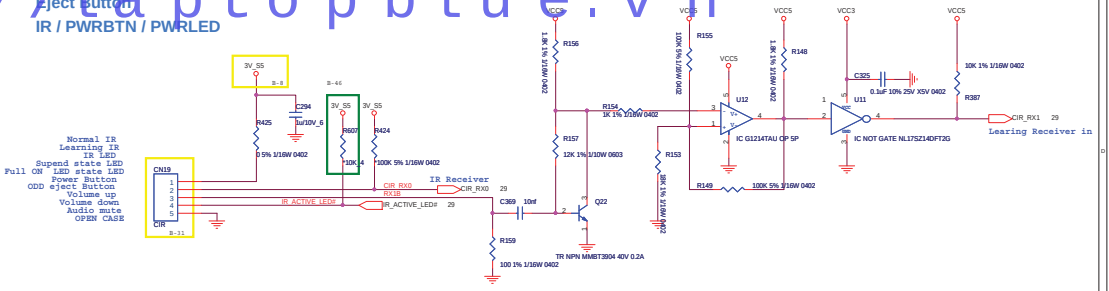
0402 size

Quanta Computer Inc.	
PROJECT : ZN8	
Size	Document Number: EC ITE 8512N/FLASH — Rev: 1A
Date: Monday, March 22, 2010	Sheet 29 of 40

20 pin + 40 pin I/O Connector

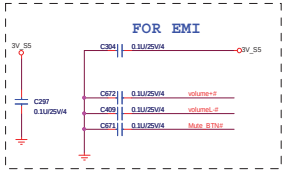


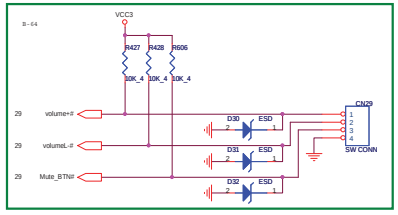
Eject Button
IR / PWRBTN / PWRLED

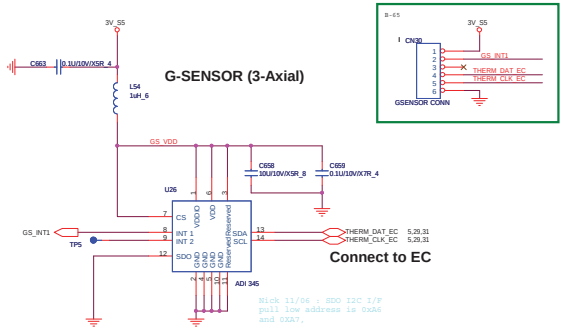


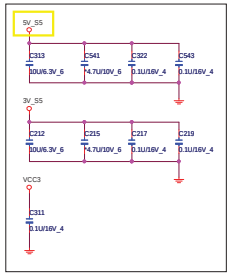
The aqua-white (470 +/- 5 nm) color is used to indicate the system is powered on and in the S0 state. The amber (590 +/- 5 nm) color is used to indicate the system is in one of the standby states (S3, S4, S5).

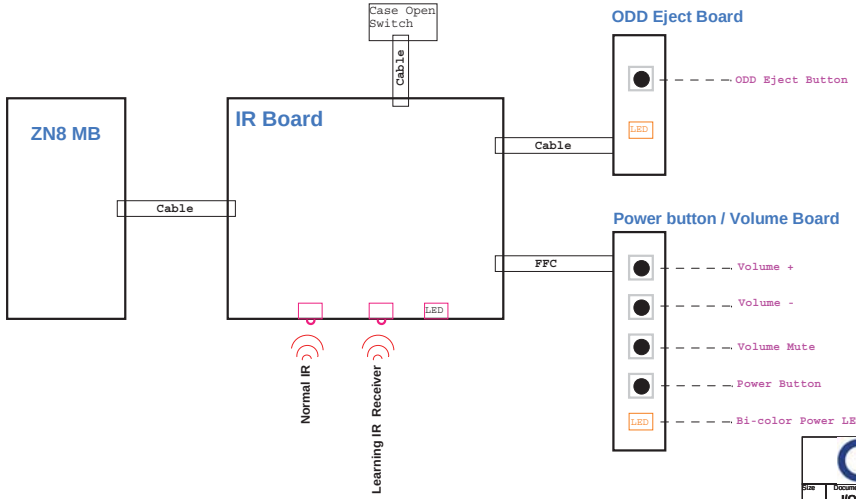
PWRBTN# must pull up to PCU power well





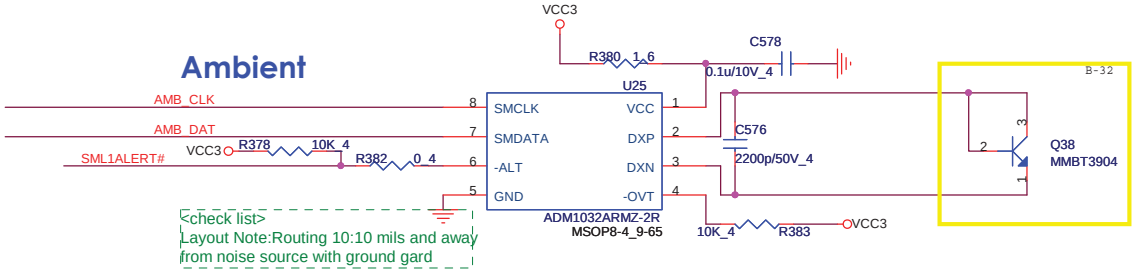




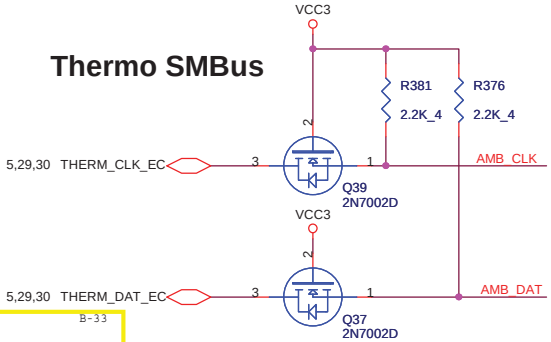


Quanta Computer Inc.			
PROJECT : ZN8			
Size	Document Number		Rev
	I/O Board Connector		1A
Date: Tuesday, March 23, 2010		Sheet 30 of 40	

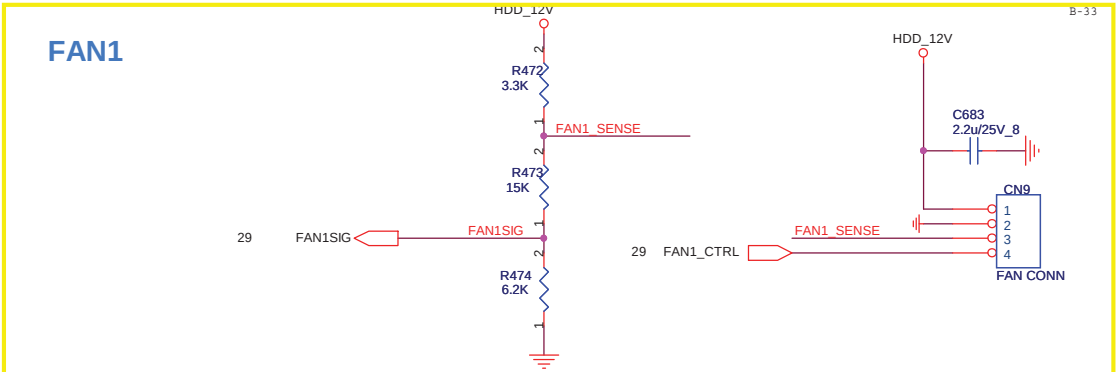
Ambient



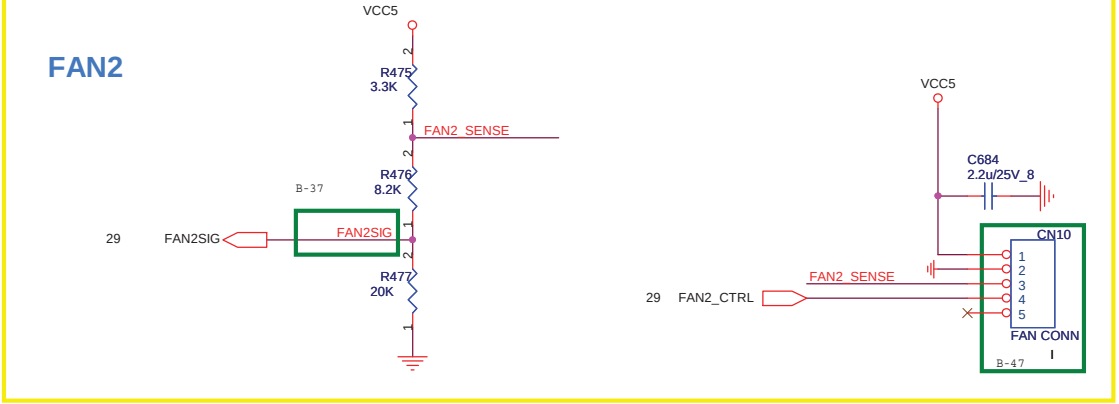
Thermo SMBus



FAN1



FAN2



Quanta Computer Inc.		
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Size	Document Number: FAN/Thermal Protection	Rev: 1A
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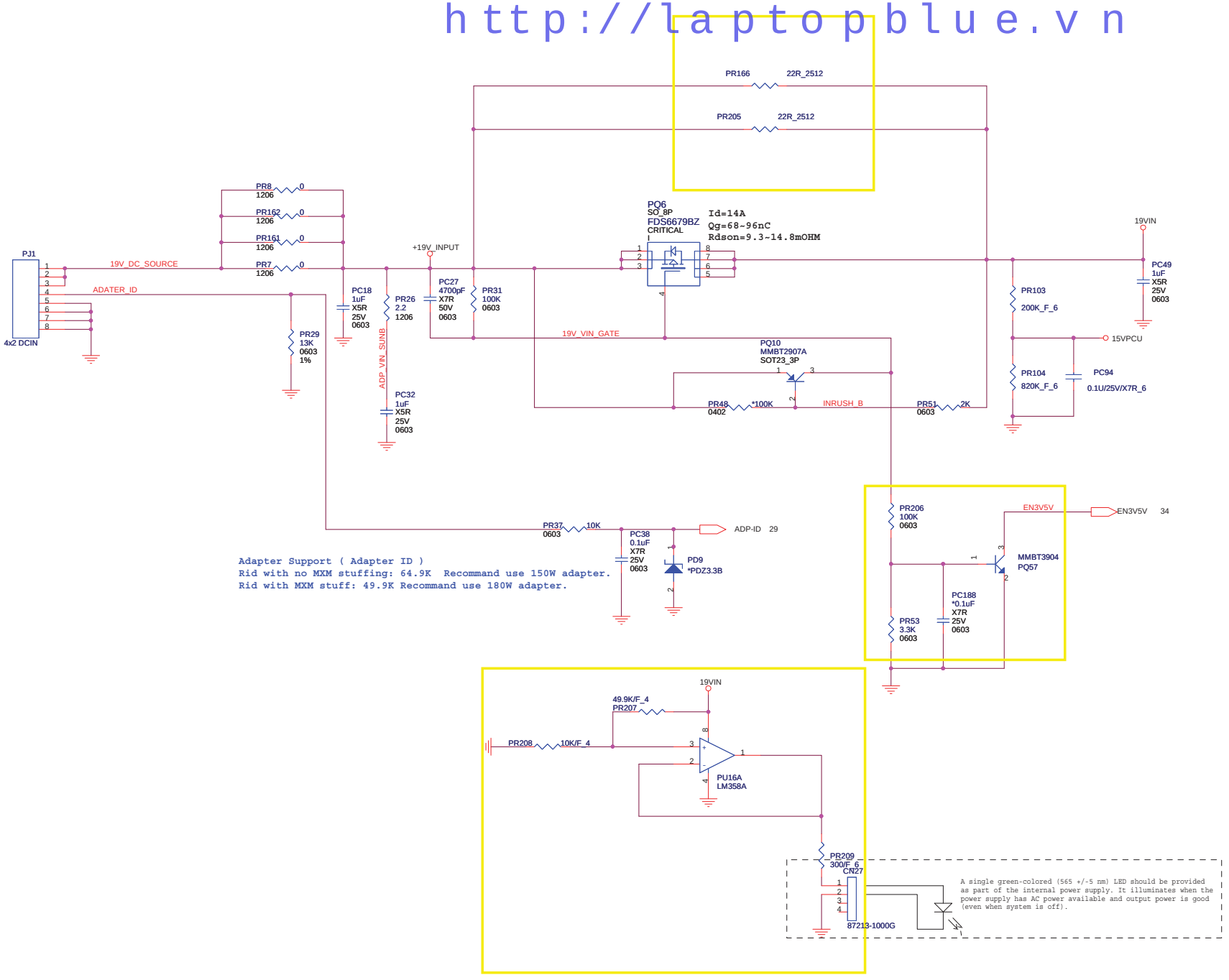

Quanta Computer Inc.

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Size	Document Number	Rev
	ACIN	1A
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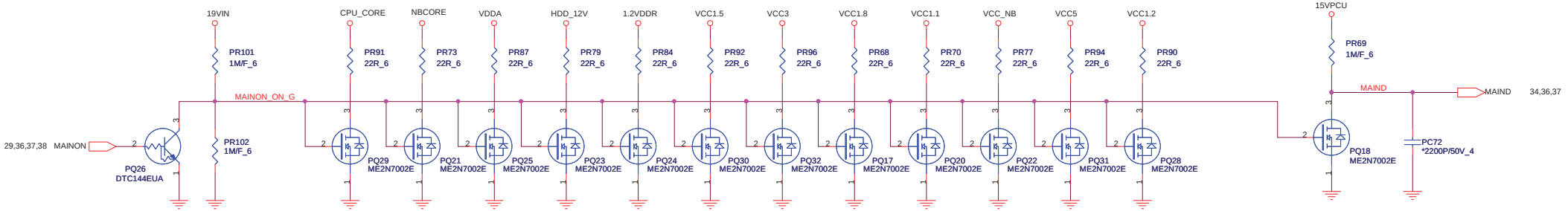

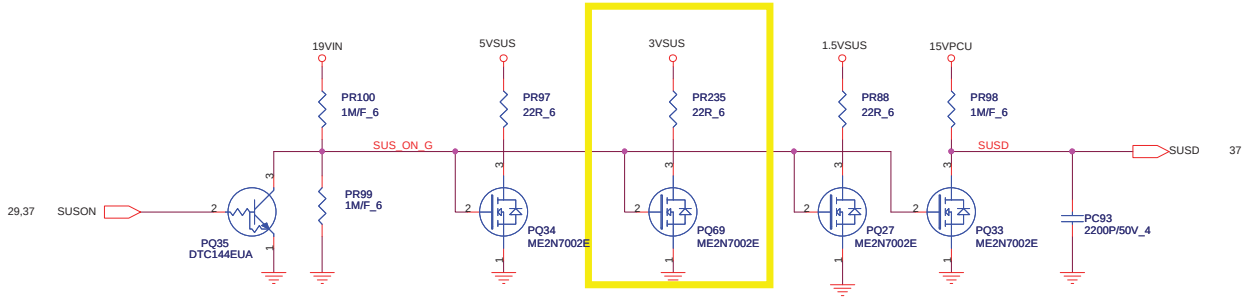

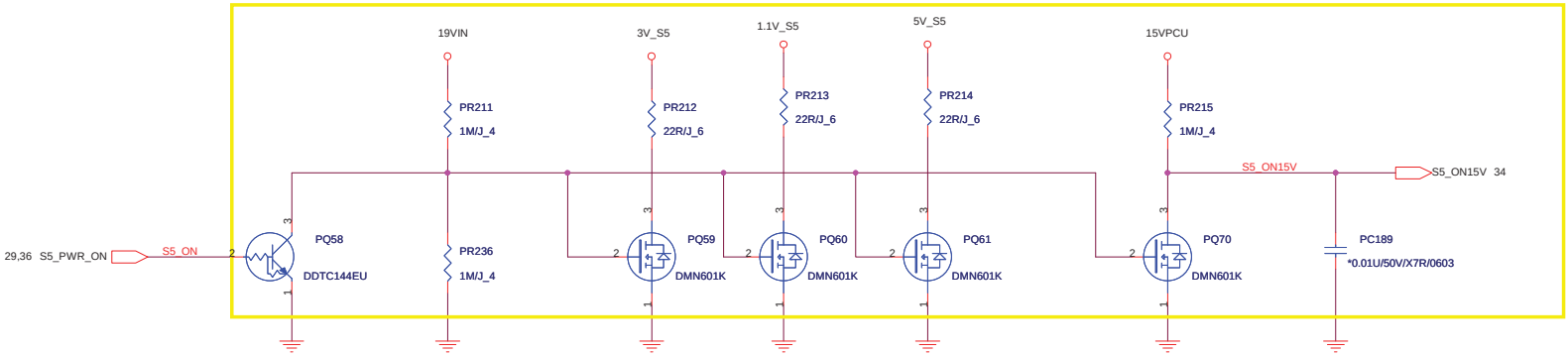

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Size	Document Number	Rev
	DISCHG & MOS SW	1A

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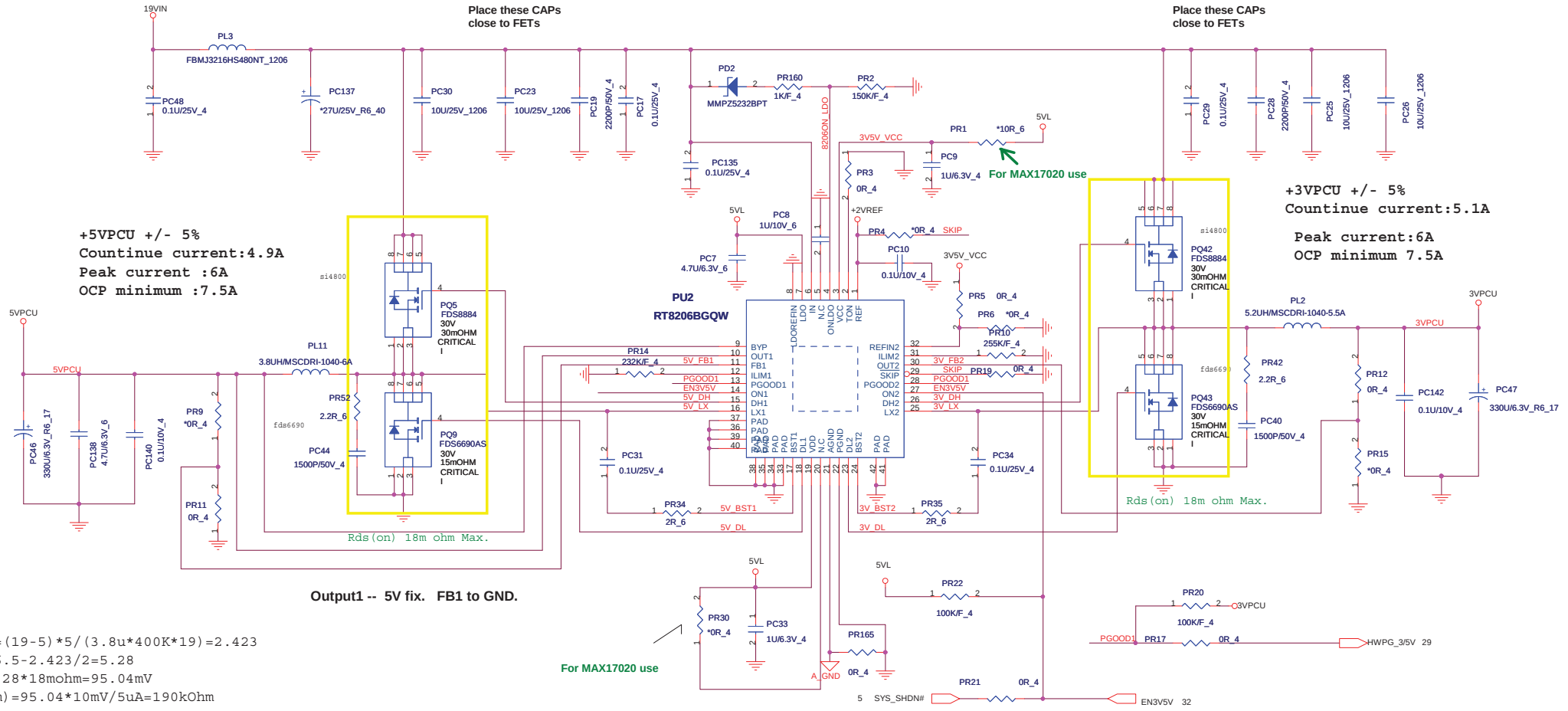
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW



Design common circuit for ,
RT8206B or Max17020 or TPS51427

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Size	Document Number	Rev
	+5V/+3V (RT8206B)	1A
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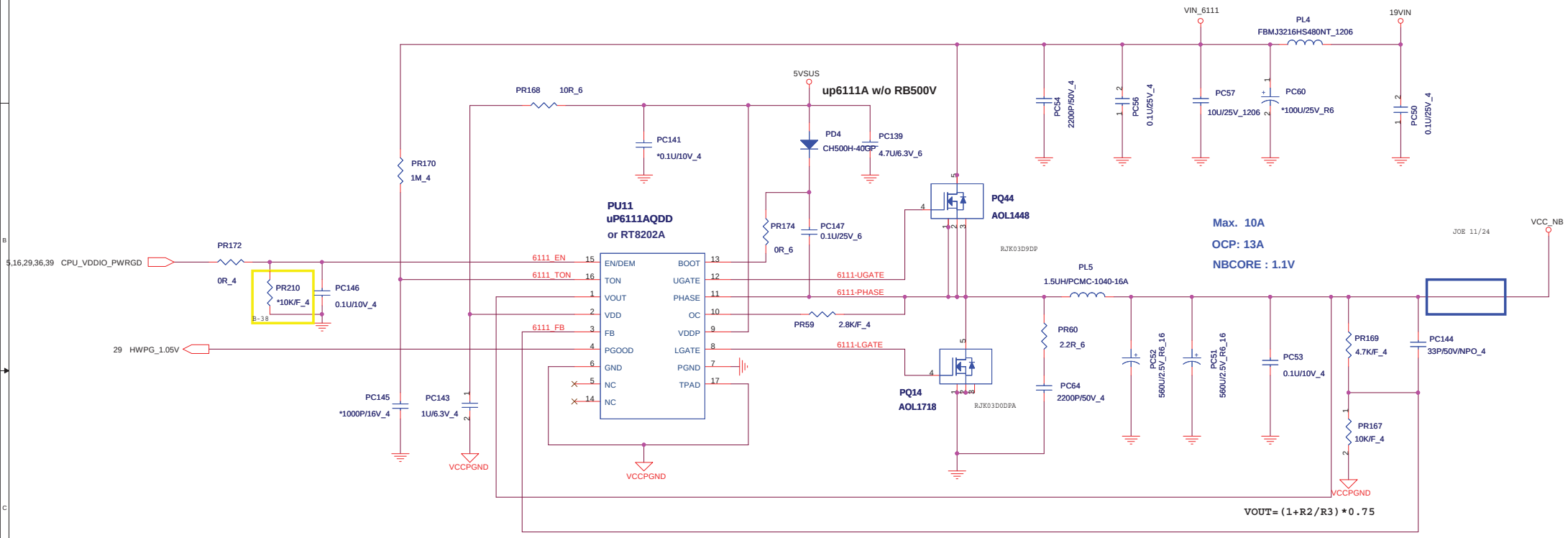
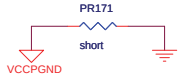


TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)



AO4712 Rds=4.3m Ohm Max./4.5V

Rds * OCP = RILIM * 20uA

13A OCP --- R_OC = 2.8K

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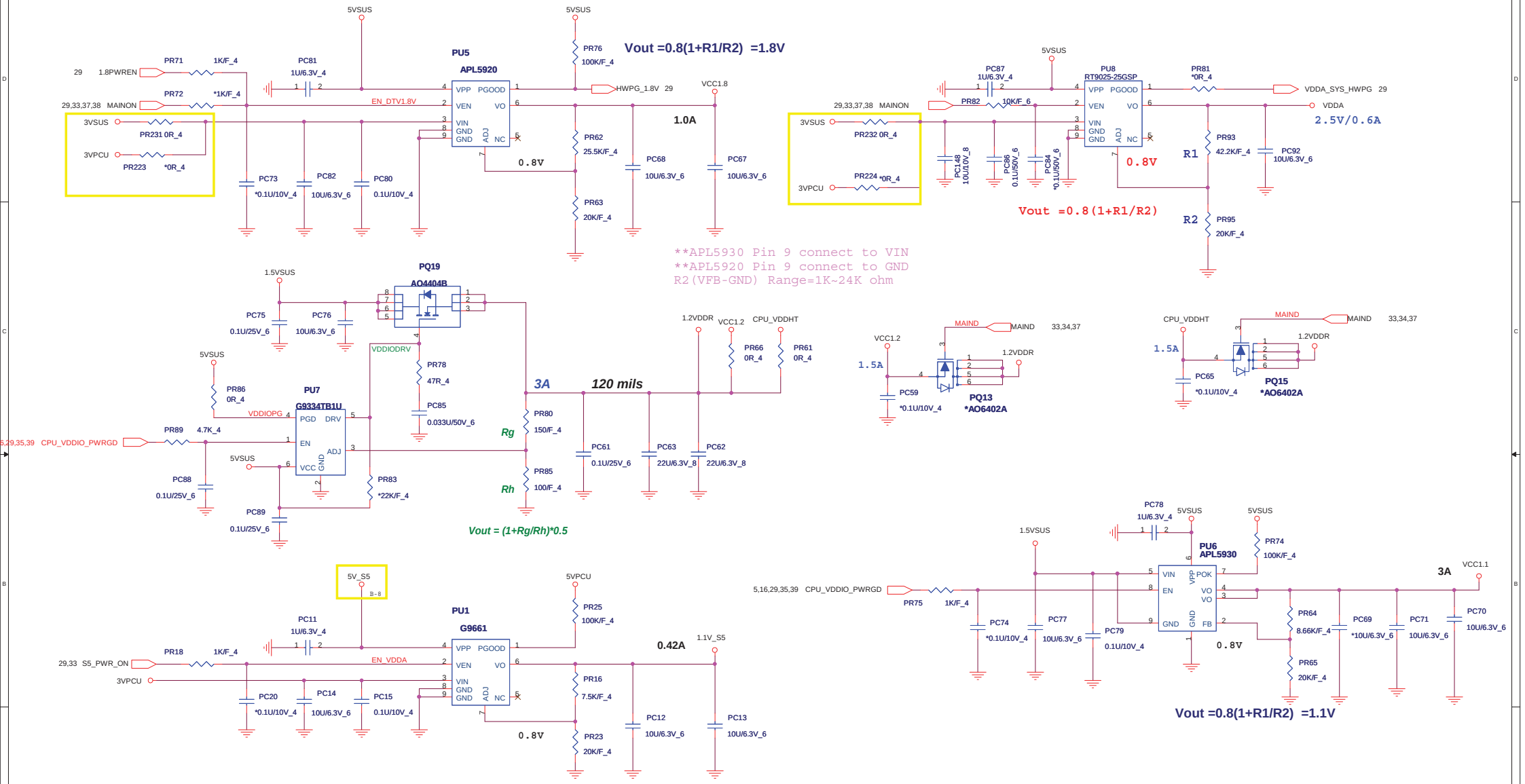
VCC1.1V, 1.2VDDR, VCC1.8V,VDDA,1.1V_S5



Quanta Computer Inc.			
PROJECT : ZN8			
Size	Document Number		Rev
	VCC1.1,VDD1.8,2.5V(LDO)		1A
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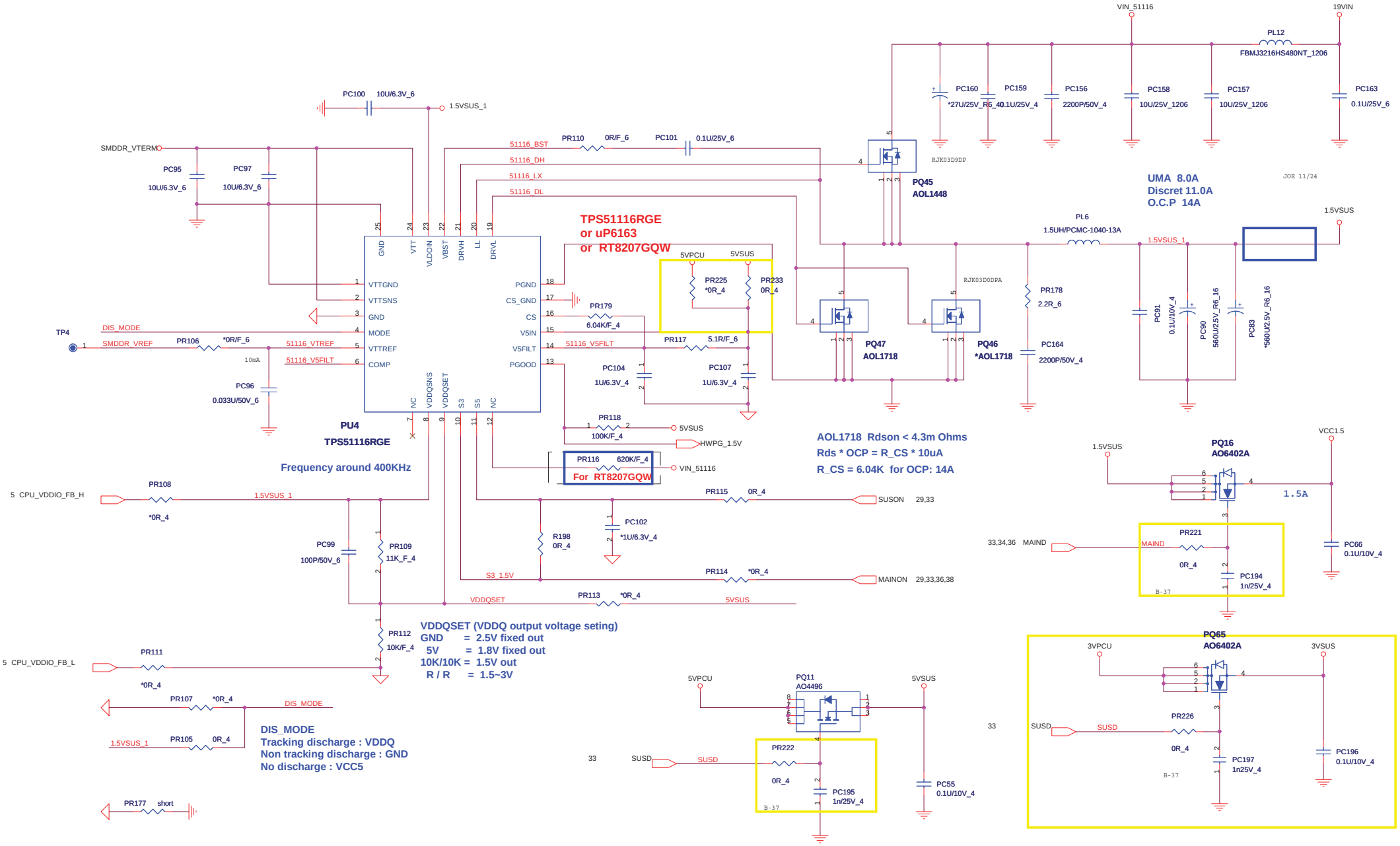
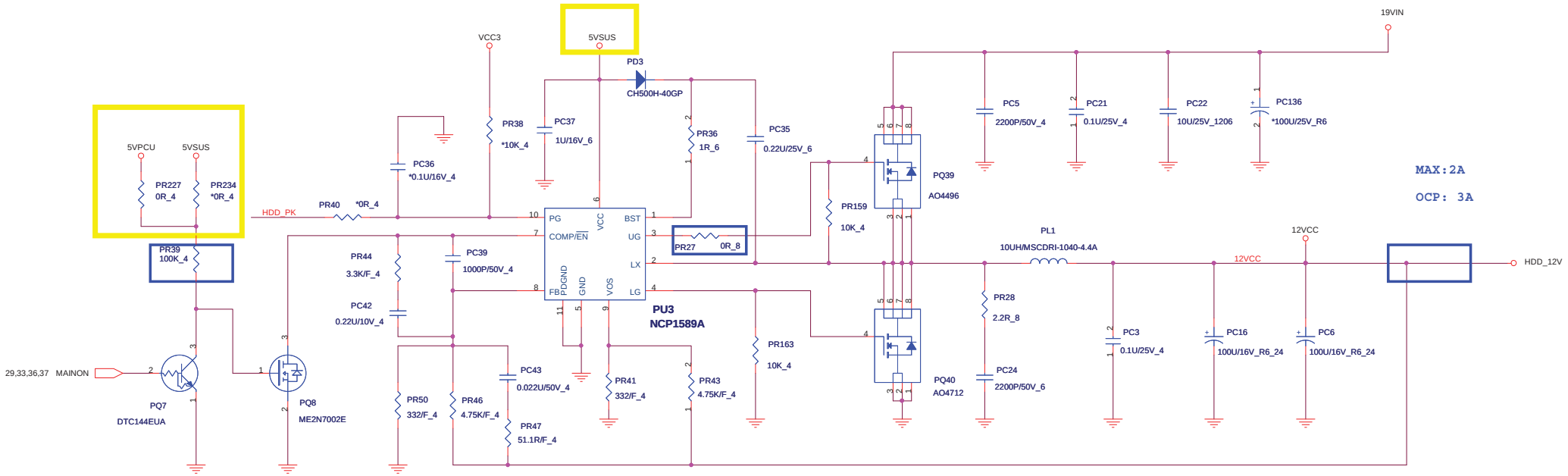
DDRIII-- 1.5VSUS



Quanta Computer Inc.	
PROJECT : ZN8	
Size	Document Number: DDR(TPS51116) — Rev: 1A
Date: Tuesday, March 23, 2010	Sheet 37 of 43



Quanta Computer Inc.		
PROJECT : ZN8		
Size	Document Number: HDD12V	Rev: 1A
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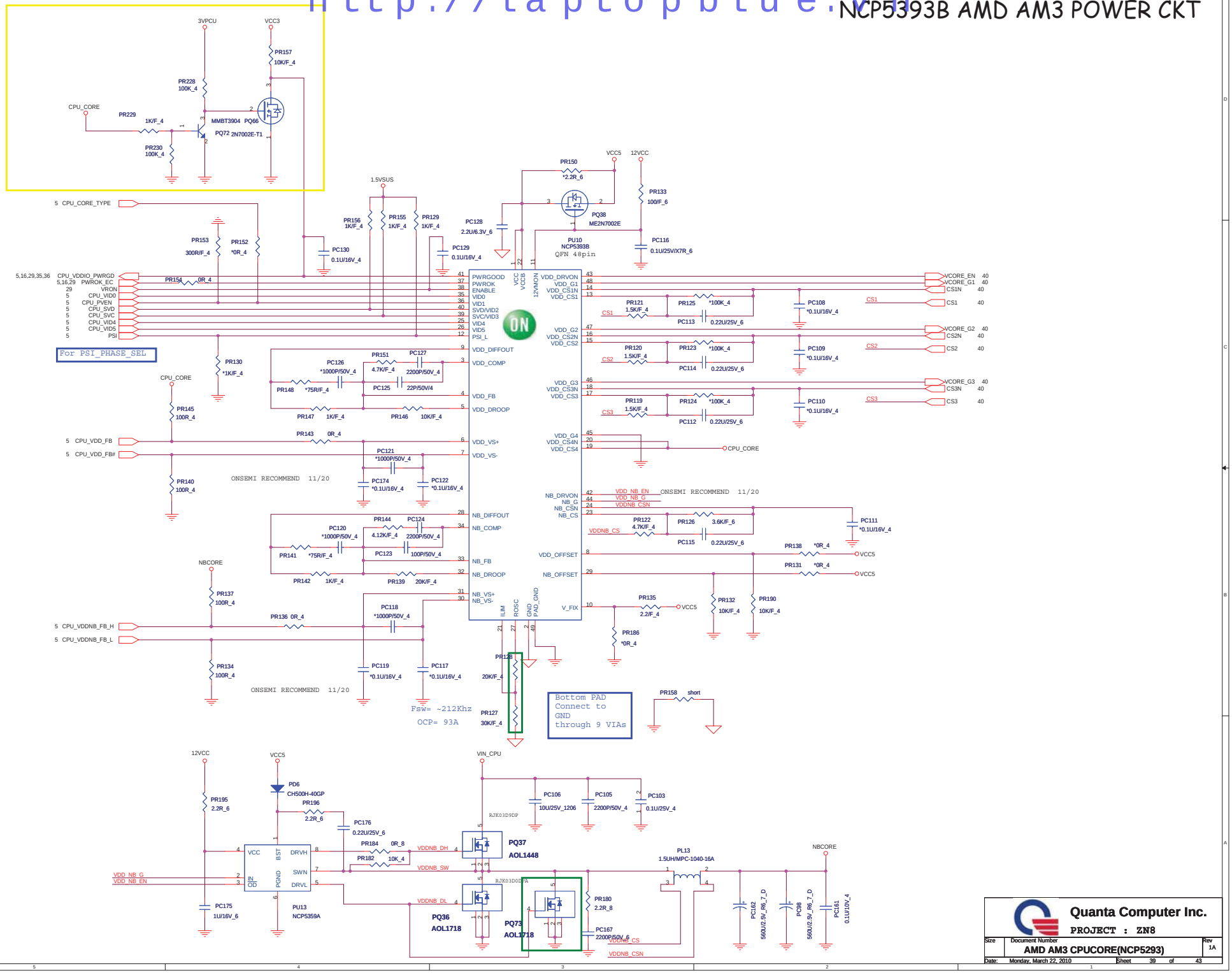
NCP5393B AMD AM3 POWER CKT



Quanta Computer Inc.

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Size	Document Number	Rev
	AMD AM3 CPUCORE(NCP5293)	1A
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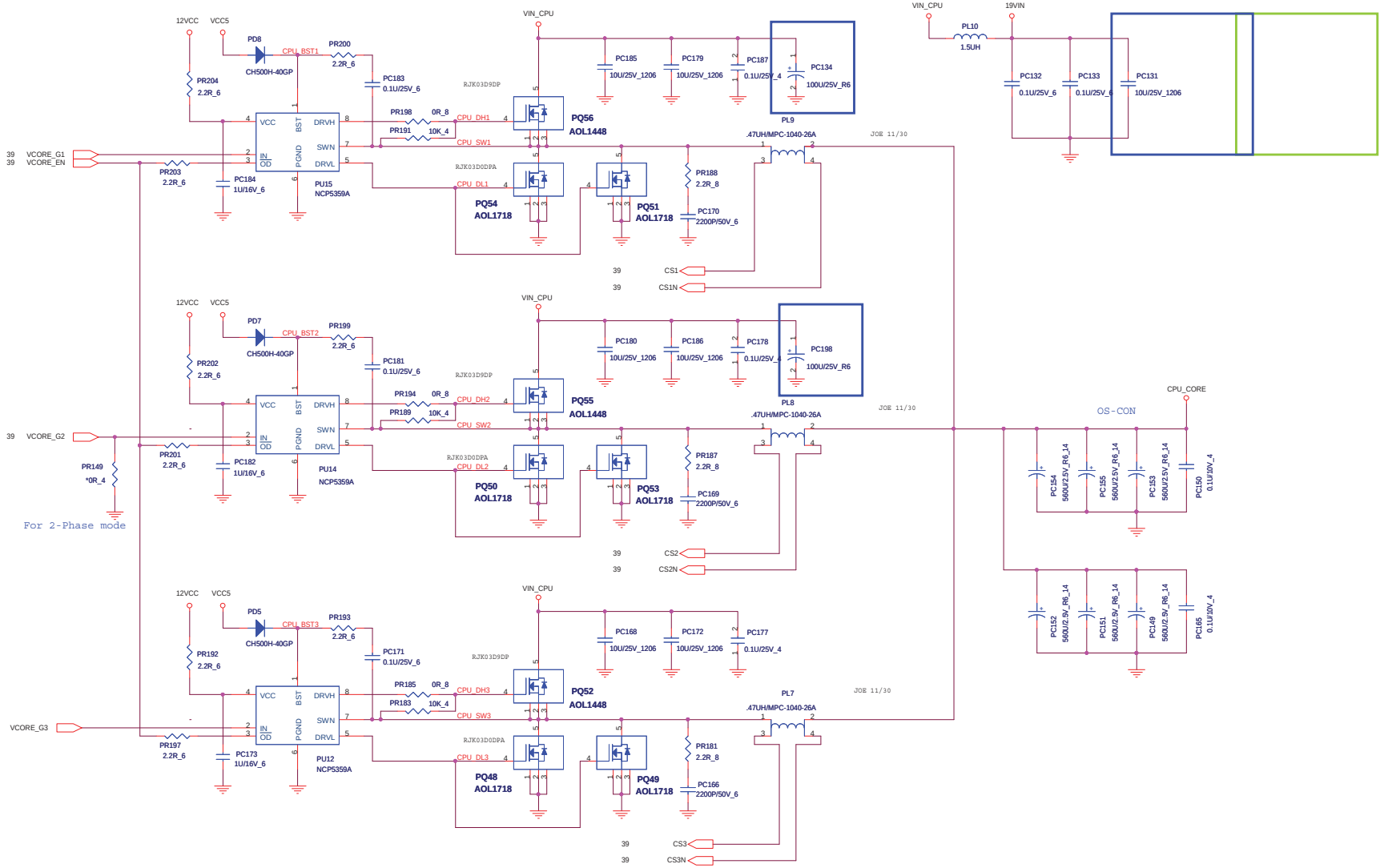

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PROJECT : ZN8		
Size	Document Number: CPU DRIVER	Rev: 1A
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CODEC

92HD89D3

IC AUDIO CODEC 92HD89D3

Analog / Digital

Near sense pin

12/8 AC90/AC93 change to 0ohms by IDT demanded

2/3 AC17/AC19 from 1u to 10u solved the THD issue.

2/3 AC20/AC21 from 1u to 100u solved the THD issue.

AC19/AC21 place near AU7 Pin9

2/3 AC14/AC16/AC18 from 1u to 10u solved the THD issue.

2/3 AC22/AC23 from 1u to 100u solved the THD issue.

AC92/AC23 place near AU7 Pin1,3

12/8. AR59 need move close to the MIC by IDT demanded

12/8 resistors change to null by IDT demanded

VOUT = 1.25 (1+R1/R2)
R1 R2
4.8375V 28.7K 10K

2nd source : G923-330T1U
AL000923003

12/8. AU3 current too small, when use we need to find other by IDT demanded

AC17 should near AU2

AC12 should near AU1

Place near AU4

11/30. change net name HPL and HPR to HPL1 and HPR1

LINE IN/Mic Reserved Jack

Normal Close

HeadPhone/Mic Combo Jack

Normal Close

11/25 add filter by IDT demanded

2/3 change 22ohm to 16ohm for meet 2Vrms output.

11/25 value change from 100P to 0.01u by IDT demanded

MUTE

Check

EC 29 EC_AMP_MUTE# → AD2 RB500V-40 → AR15 47K_F4 → AMP_MUTE# 42

PCH CODEC_RST PCH_AZ_CODEC_RST# AD1 RB500V-40

BUZZER

VCC5 AR36 47 5% 1/16W 0402 AR20 0.1% 1/10W 0603 BZ1

BZ 3.6V 90DB 8.5*8.5MM DNGJ4B20001

13 SPKR AR21 2.7K 1% 1/16W 0402 MMBT3904 40V 0.2A AQ1 AC22 0.1uF 10% 10V X5R 0402

AC97 ALC SCHEMATIC (AFTER PLUG IN)

AC97 ALC SCHEMATIC (BEFORE PLUG IN)

Quanta Computer Inc.
PROJECT : ZN8
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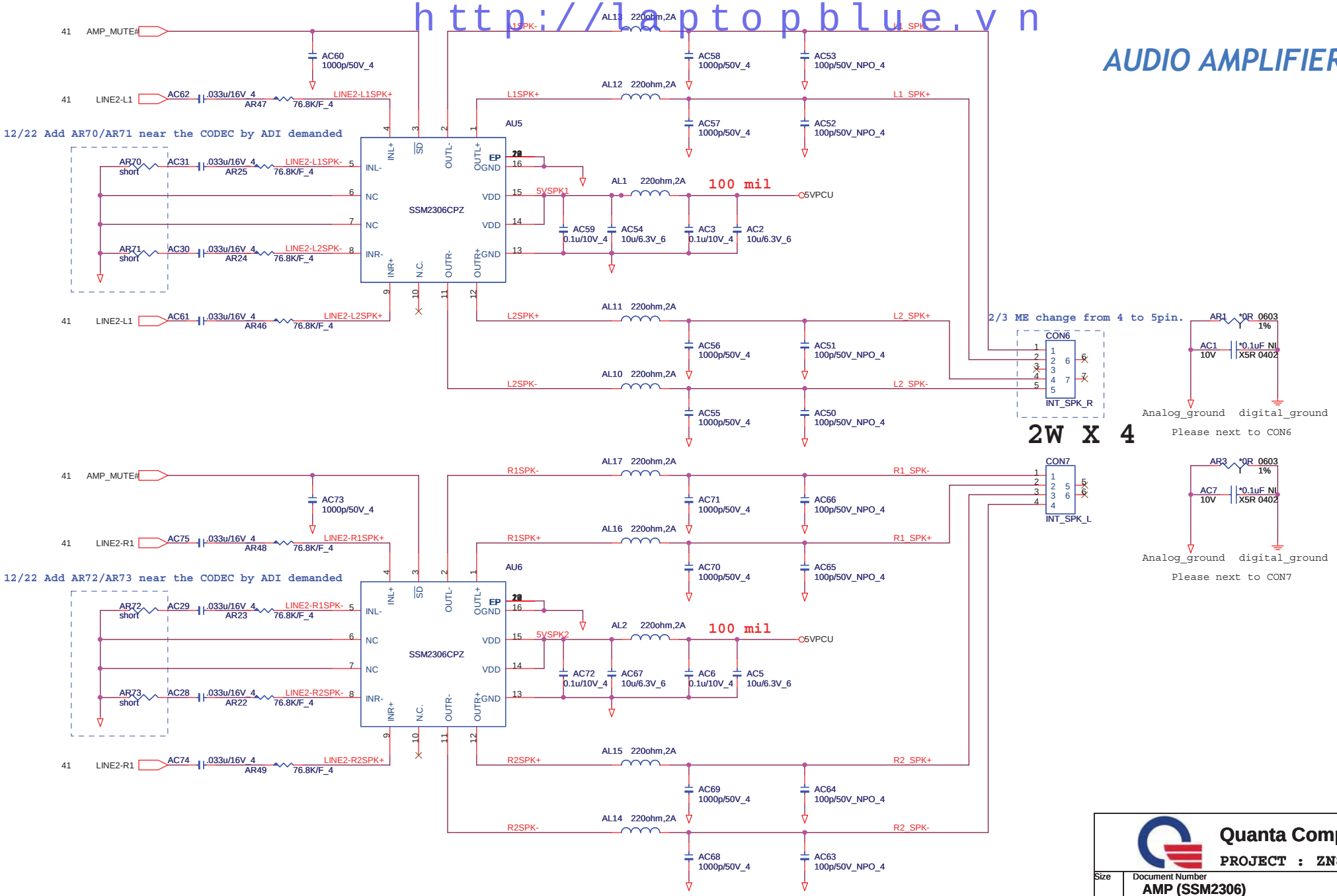
AUDIO AMPLIFIER



Quanta Computer Inc.		
PROJECT : ZN8		
Size	Document Number: AMP (SSM2306)	Rev: 1A
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B-1 : CLK source change to CLK GEN from SB
B-2 : Change resistor footprint type
B-3 : Remove resistor for CLK GEN source
B-4 : Linking for EDID read
B-5 : For LAN and USB3.0 PCIE signal
B-6 : For EDID writing control
B-7 : Change CLK source from SB to CLK GEN
B-8 : Separate system 5% power from 3VPCU
B-9 : Mount R80 and D5 for MDN control
B-10 : Change SB strap setting
B-11 : Correct DIMM setting
B-12 : Linking for EDID read
B-13 : Correct 19V power rail net name
B-14 : Correct PCIE_RST% SB connection
B-15 : Change CRT connector type
B-16 : Change GSE connector type
B-17 : Change mini PCIE controller form NB to SB
B-18 : Change mini PCIE controller form NB to SB
B-19 : Add capacitor for noise filtration
B-20 : Separate DMIC and camera connector
B-21 : Correct scalar board reset signal
B-22 : Modify panel EDID read / write function
B-23 : Modify display port AUX channel connection
B-24 : Add panel power 12V/5V switch function
B-25 : Correct 19V power rail net name
B-26 : Panel power 12V/5V power selection
B-27 : Link KP amp I2C to EC for GAIN control
B-28 : PWM driving for FAN control
B-29 : CPU_CORE PWRD assertion for EC
B-30 : Adjust I/O port pin define
B-31 : Change CIR connector type
B-32 : Correct DIMM thermal detect function
B-33 : Modify FAN circuit for 12V FAN
B-34 : CLK_SRSRCP_P# / CLK_SRSRCN_P# link to CLK GEN SRSRC_CLK_R / SRSRC_CLK#_R
B-35 : Change R173,R175 to 150 ohm from 4.7K
B-36 : De-pop R111,R159
B-37 : Fix FAN net name issue
B-38 : Fix DDR dongle issue
B-39 : Change MUX SB from port B to port C
B-40 : Add R-C delay
B-41:Change USB power to VSUS
B-42: Change PCIEx1 Lane to fix Lan issue
B-43: Modified Panel power circuit
B-44: Change CN19(MT) from 4pin to 5pin
B-45: Change CON2, CON3 pin definition
B-46: Reserve PU Res. for IR con pin4.
B-47: Change FAN2(CN13) from 4pin to 5pin
B-48: Connector PCIE_WAKE to IO_RD for WOL
B-49: Remove CN11 Logo light# circuit
B-50: Change DL SMBUS from main to resume
B-51: De-pop R144,R149
B-52: Change D4 to D28,D29
B-53: Add DDR RSMRST# RC delay circuit
B-54: Reserve SB_SPI for debug
B-55: Change MT touch power to 5VSUS
B-56: Change scalar EC conn. power.
B-57: Disable SB EC strap
B-58: De-pop R479 to fix scalar RD reset issue
B-59: Change carder connector type(CN12)
B-60: Isolate power btn from CN4 to CON8
B-61: Change R19,R20 to 4.7k and de-pop R12,R48 for RDD issue
B-62: Add EVCC1 power control circuit
B-63: Add re-driver IC for PCIE LAN and USB3.0
B-64: Add CN39 for vol+/vol-/mute function
B-65: Add CN38 for D-SENSOR
B-66: Add NB_PWRGD control circuit for spike issue

PAGE 32

1.del DCIN1 · PR176 · PR175 · PR173 · PR24 · PQ4 · PQ2 · PR32 · PR24 · PR49 · PD1 · PC41 · PR33 · PR164 · CR1 · PR13 · PQ41 · PQ3 · PR55 · PR56 · PC45 · PR54 · PR45 · PR57 · PC4 · PC2

2 - ADD PR206/100kohm · PC188/0.1uF · PQ57/MMBT3904 · PR207/49.9kohm · PR37/10kohm · PU16A/LM358 · PR166/22ohm · PD9/PDZ3.3B · PR209/300ohm

3 - change PR29 FROM 64.9k ohm TO 13kohm

PAGE 35

1 - change PR172 FROM 1k ohm TO 0 ohm

2 - ADD PR7/10kohm · PC51/560uF/2.5V

PAGE 36

1 - change PU8 VEN FROM CPU_VDDIO_PWRGD TO MAINON

PAGE 37

1 - change VCC1.5V TO VCC1.5

2 - add pq65, pr226,pc197,pc196 for 3vsus

PAGE 39

1 - change PU10 PWRGOOD FROM CPU_CORE TO VCC3

2 - add mosfet in VDDNB

3 - add pr229,pr230,pr228,pr157,pq67,p166 for pwrgood

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