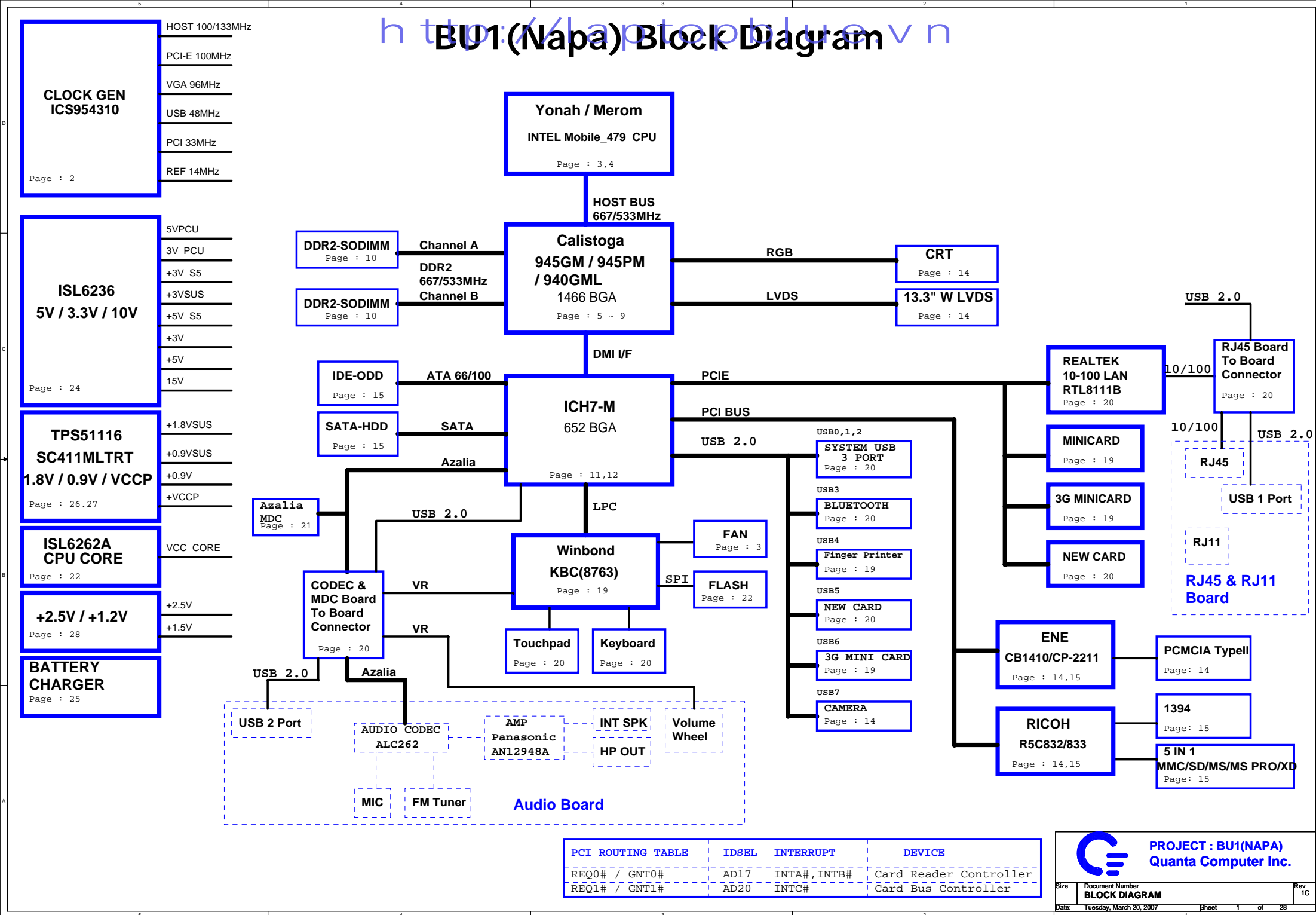
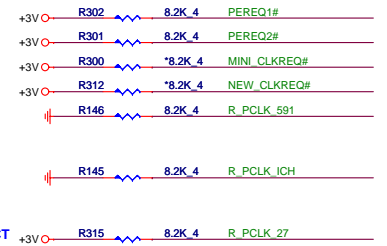
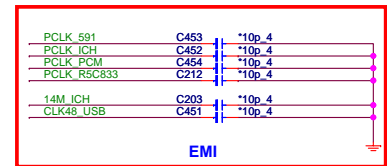
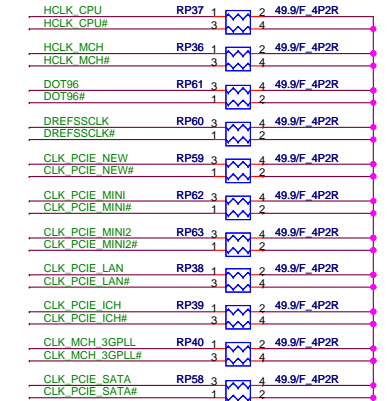


BU1(Napa) Block Diagram



<http://laptopblue.vn>



```
SELLCD_27# SELECT
0: 27MSS 1: LCD
CLK
```

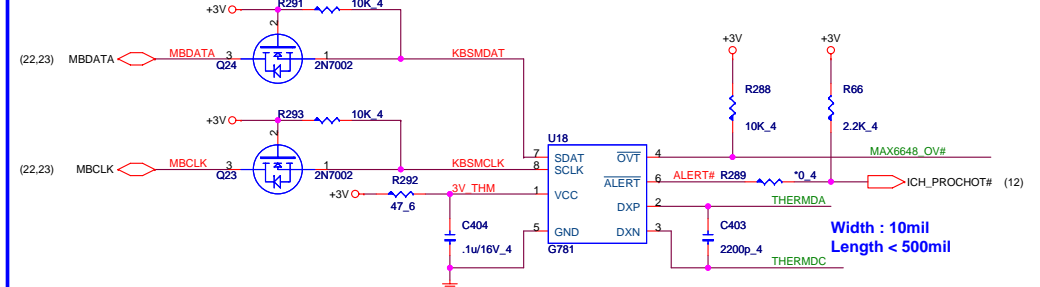
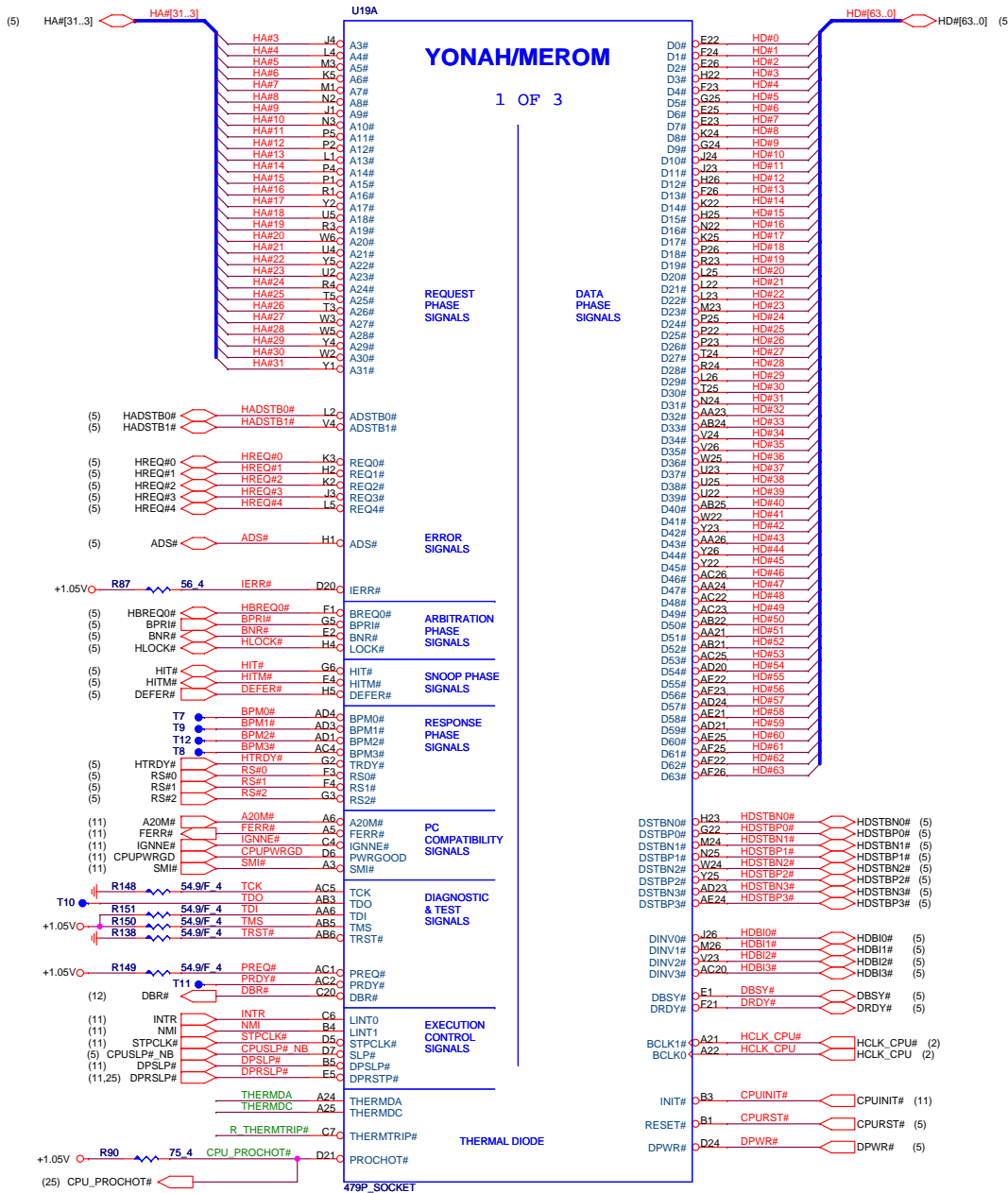
SMBUS Address : D2 (Read) , D3 (Write)



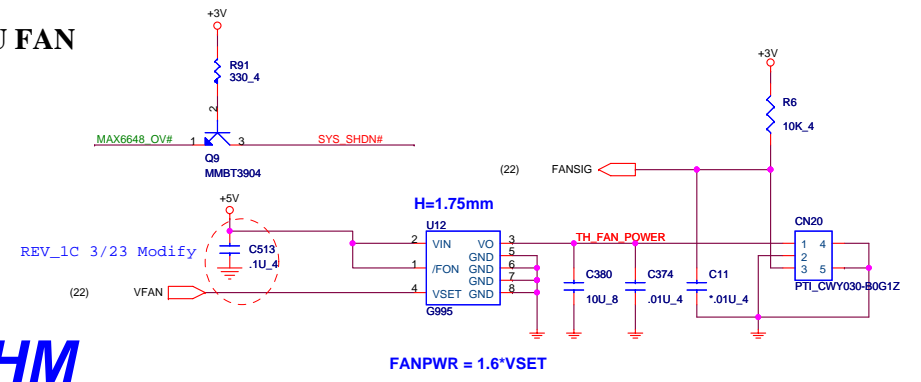
	FSC	FSB	FSA	CPU	PCIE	PC
0	0	0		266	100	33
0	0	1		133	100	33
0	1	0		200	100	33
0	1	1		166	100	33
1	0	0		333	100	33
1	0	1		100	100	33
1	1	0		400	100	33
1	1	1		200	100	33



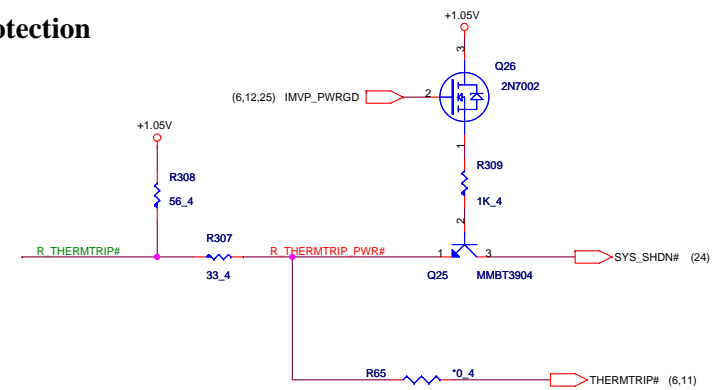
PROJECT : BU1(NAPA)
Quanta Computer Inc.



CPU FAN



125 Degree Protection



PROJECT : BU1(NAPA)
Quanta Computer Inc.

COMP0 - COMP3
Width : 200mil
Length < 500mil

GTLREF
Width : 5mil
Length < 500mil

YONAH/
MEROM

2 OF 3
POWER,
RESERVED
SIGNALS

YONAH/MEROM

3 OF 3
GROUND

U19B

U19C

479P_SOCKET

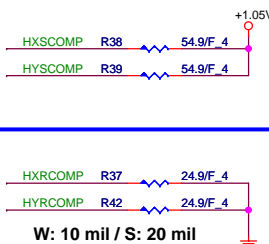
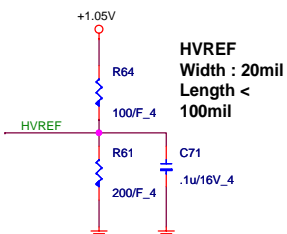
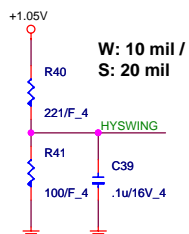
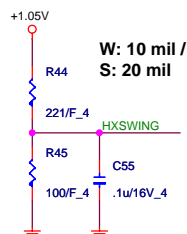
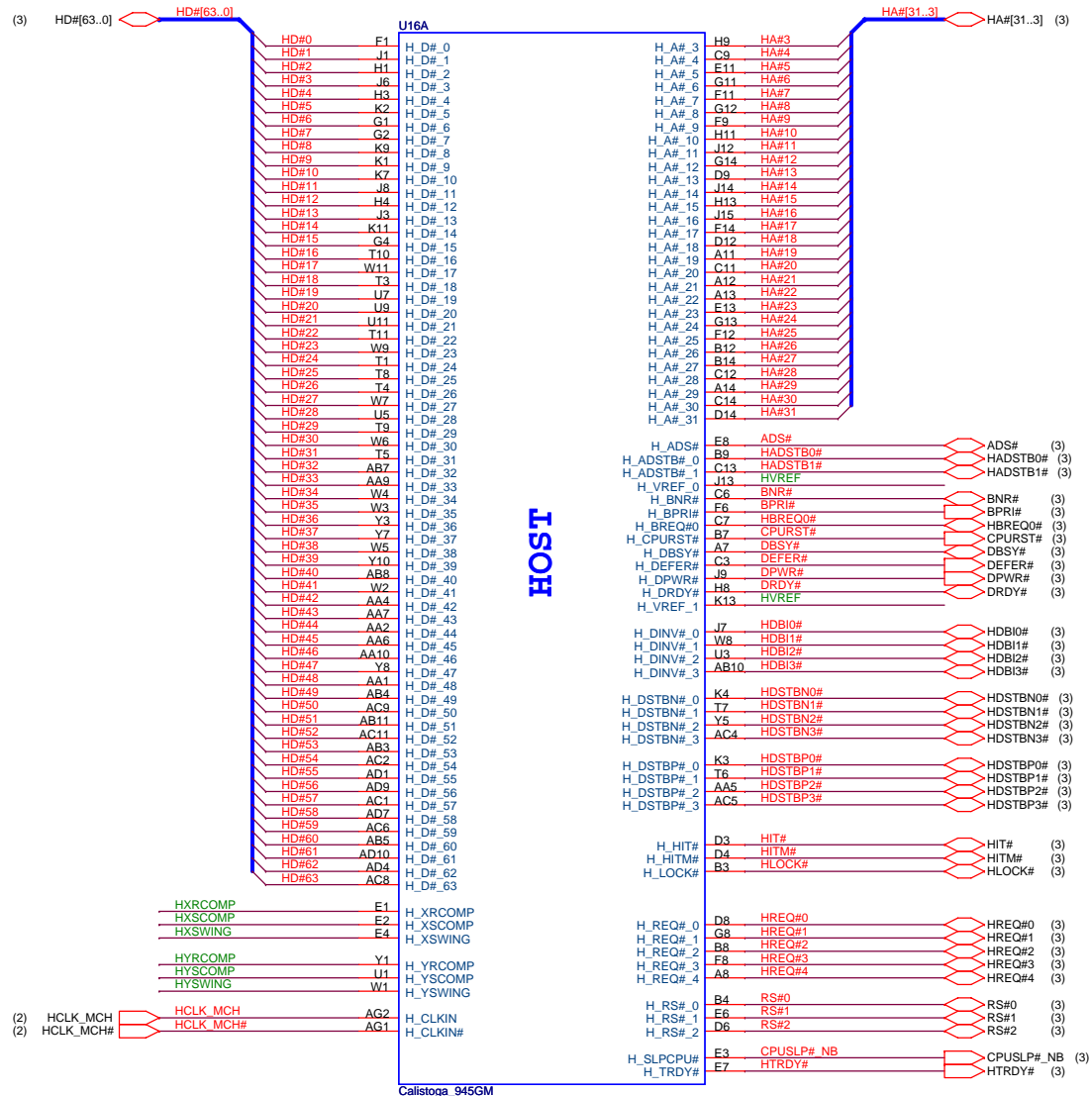
479P_SOCKET

CPU

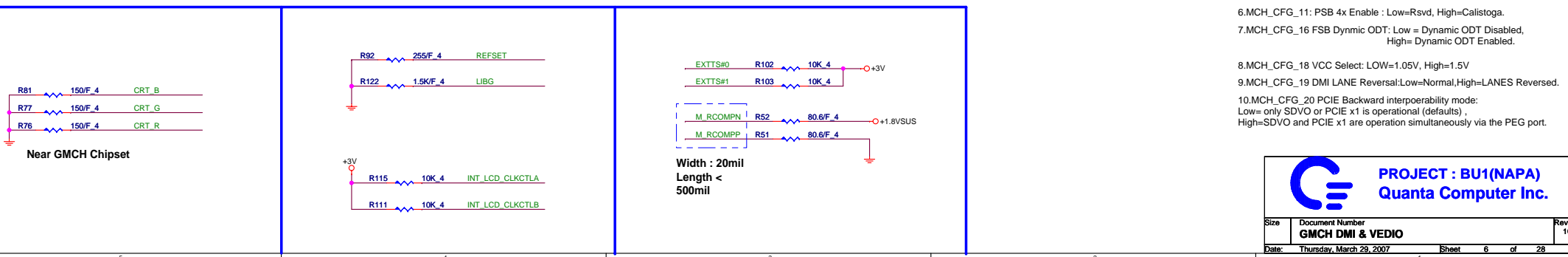
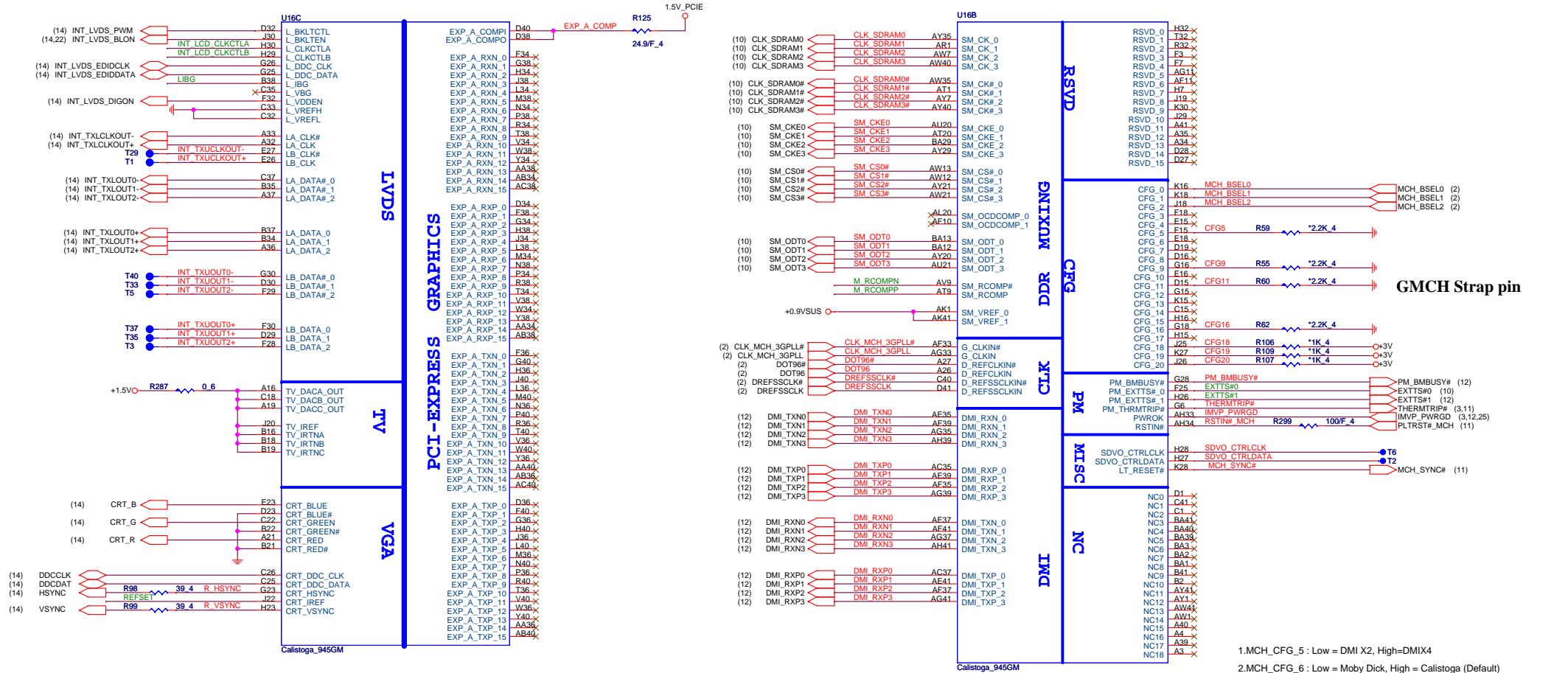


PROJECT : BU1(NAPA)
Quanta Computer Inc.

Size	Document Number	Rev
	CPU (POWER/GND)	1C
Date:	Thursday, March 29, 2007	Sheet 4 of 28



PROJECT : BU1(NAPA)
Quanta Computer Inc.

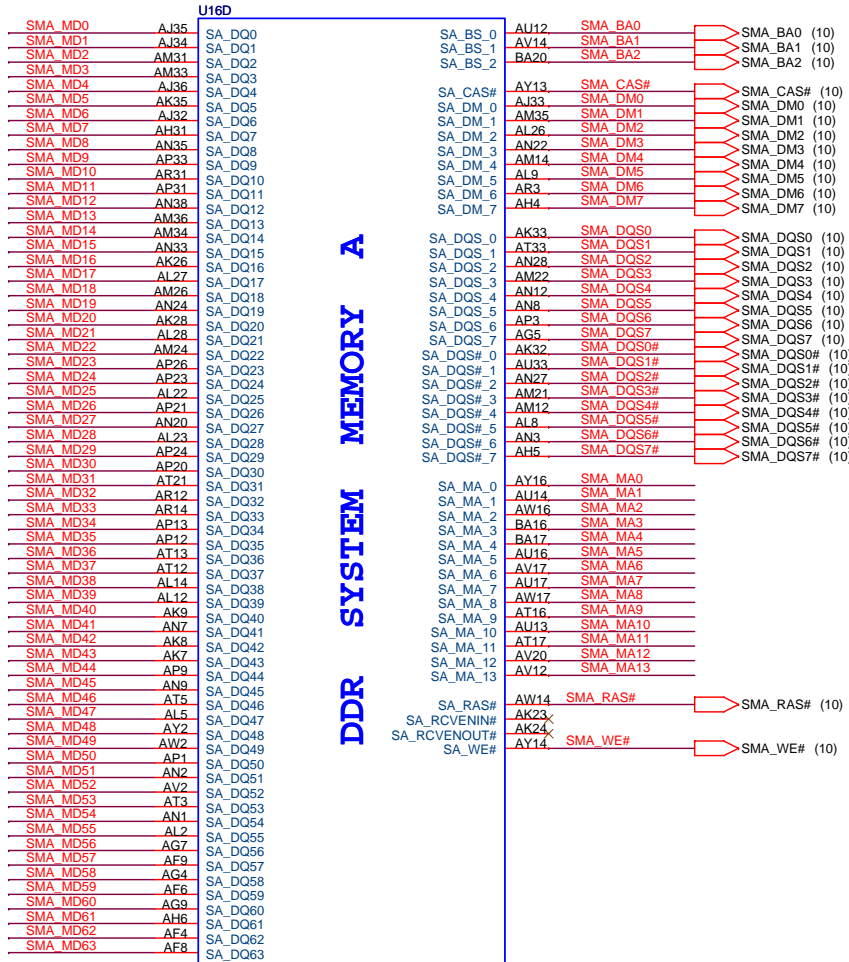


- 1.MCH_CFG_5 : Low = DMI X2, High=DMIX4
- 2.MCH_CFG_6 : Low = Mosby Dick, High = Calistoga (Default)
- 3.MCH_CFG_7 : Low = Rsvd, High = Mobile CPU
- 4.MCH_CFG_9 PCI Express Graphics Lane: Low =Reverse lane ,High=Normal
- 5.MCH_CFG_10 Host PLL VCC Select: Low=Reserved, High=Mobility
- 6.MCH_CFG_11: PSB 4x Enable : Low=Rsvd, High=Calistoga.
- 7.MCH_CFG_16 FSB Dymnic ODT: Low = Dynamic ODT Disabled,
High= Dynamic ODT Enabled.
- 8.MCH_CFG_18 VCC Select: LOW=1.05V, High=1.5V
- 9.MCH_CFG_19 DMI Lane Reversal:Low=Normal,High=LANES Reversed.
- 10.MCH_CFG_20 PCIe Backward interoperability mode:
Low= only SDVO or PCIE x1 is operational (defaults) ,
High=SDVO and PCIE x1 are operation simultaneously via the PEG port.



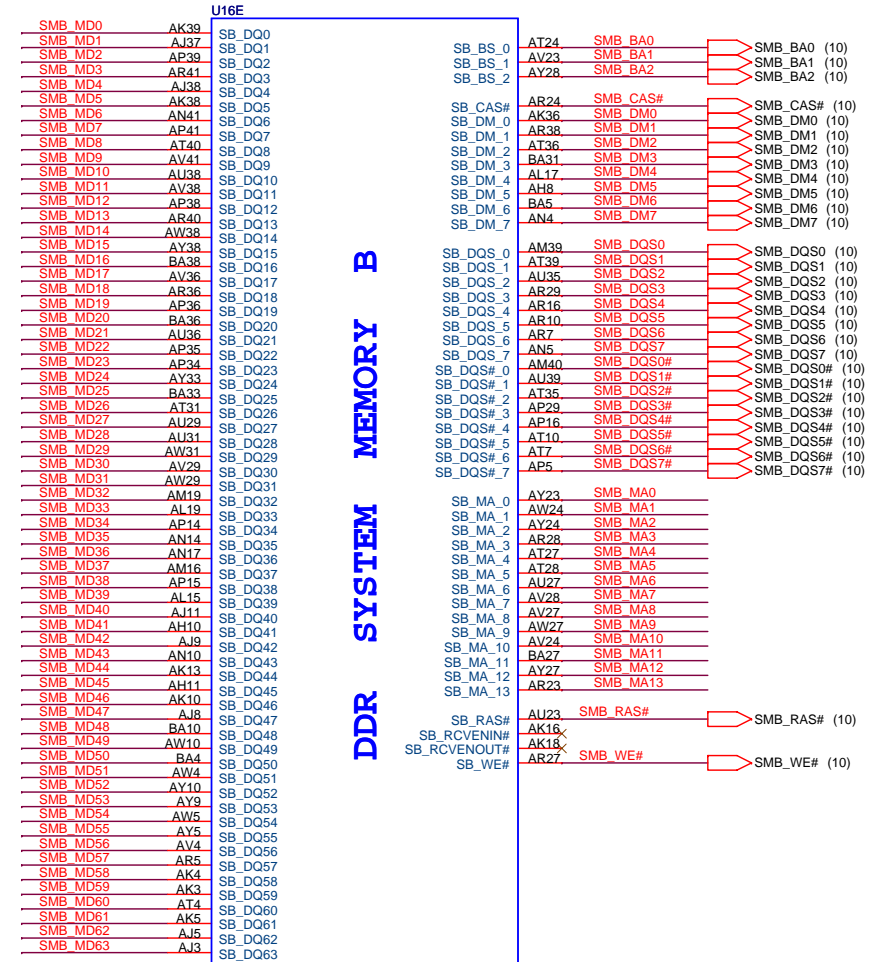
PROJECT : BU1(NAPA)
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH DMI & VEDIO	1
Date:	Thursday, March 29, 2007	Sheet 6 of 28



SMA_MD[63..0] SMA_MD[63..0] (10)

SMA_MA[13..0] SMA_MA[13..0] (10)



SMB_MD[63..0] SMB_MD[63..0] (10)

SMB_MA[13..0] SMB_MA[13..0] (10)

CLG



PROJECT : BU1(NAPA)
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH (MEMORY)	1C
Date:	Thursday, March 29, 2007	Sheet 7 of 28

CLG



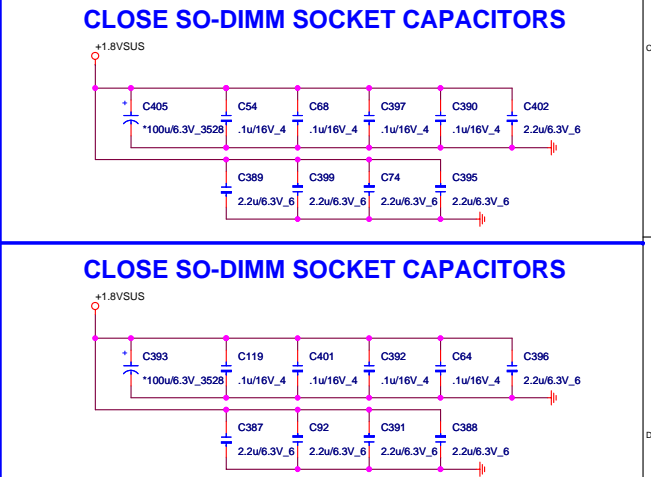
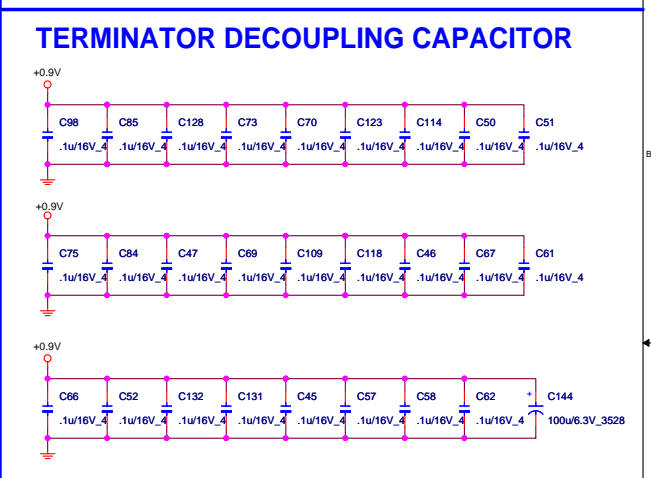
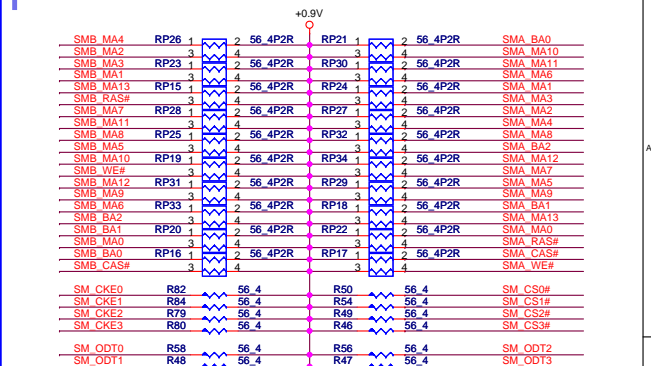
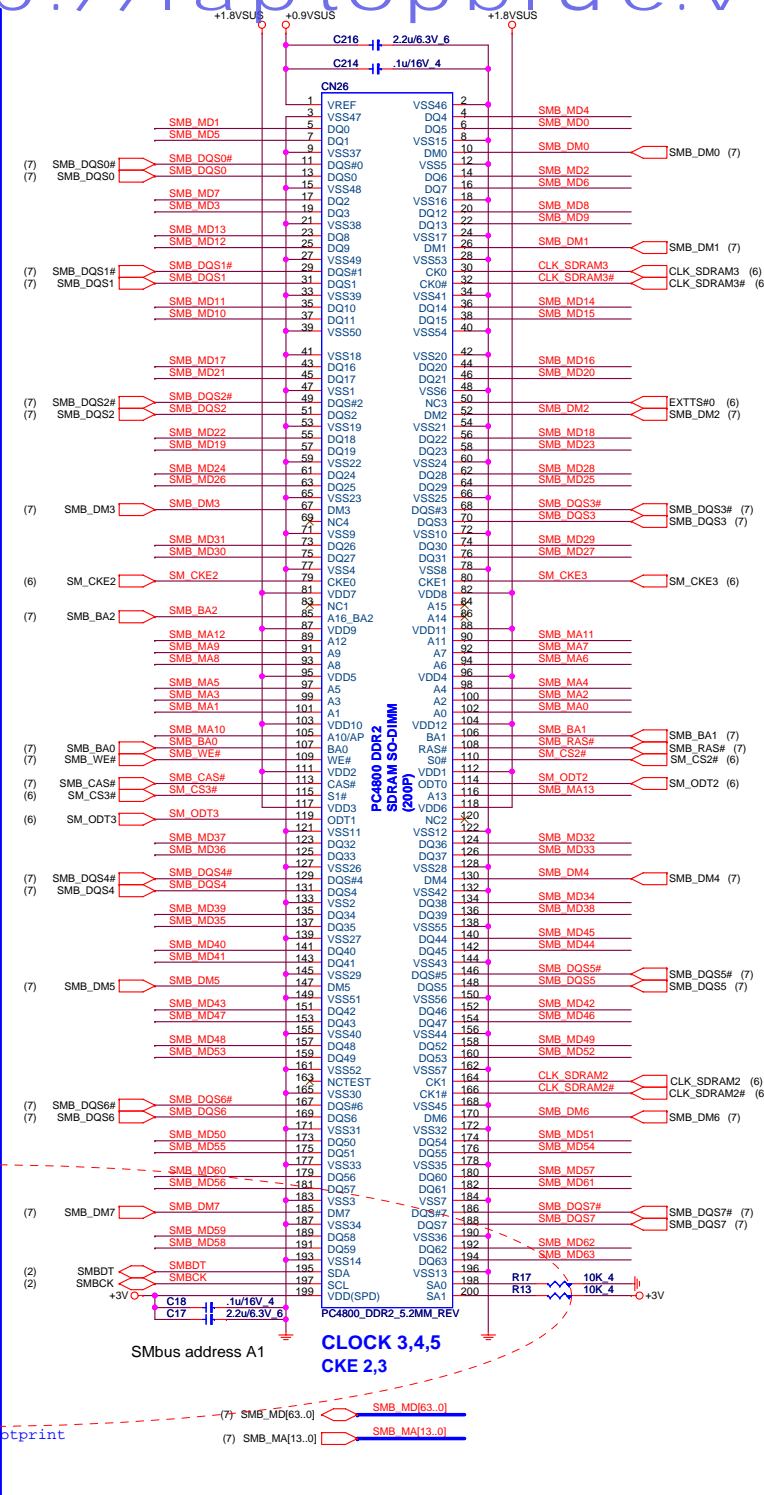
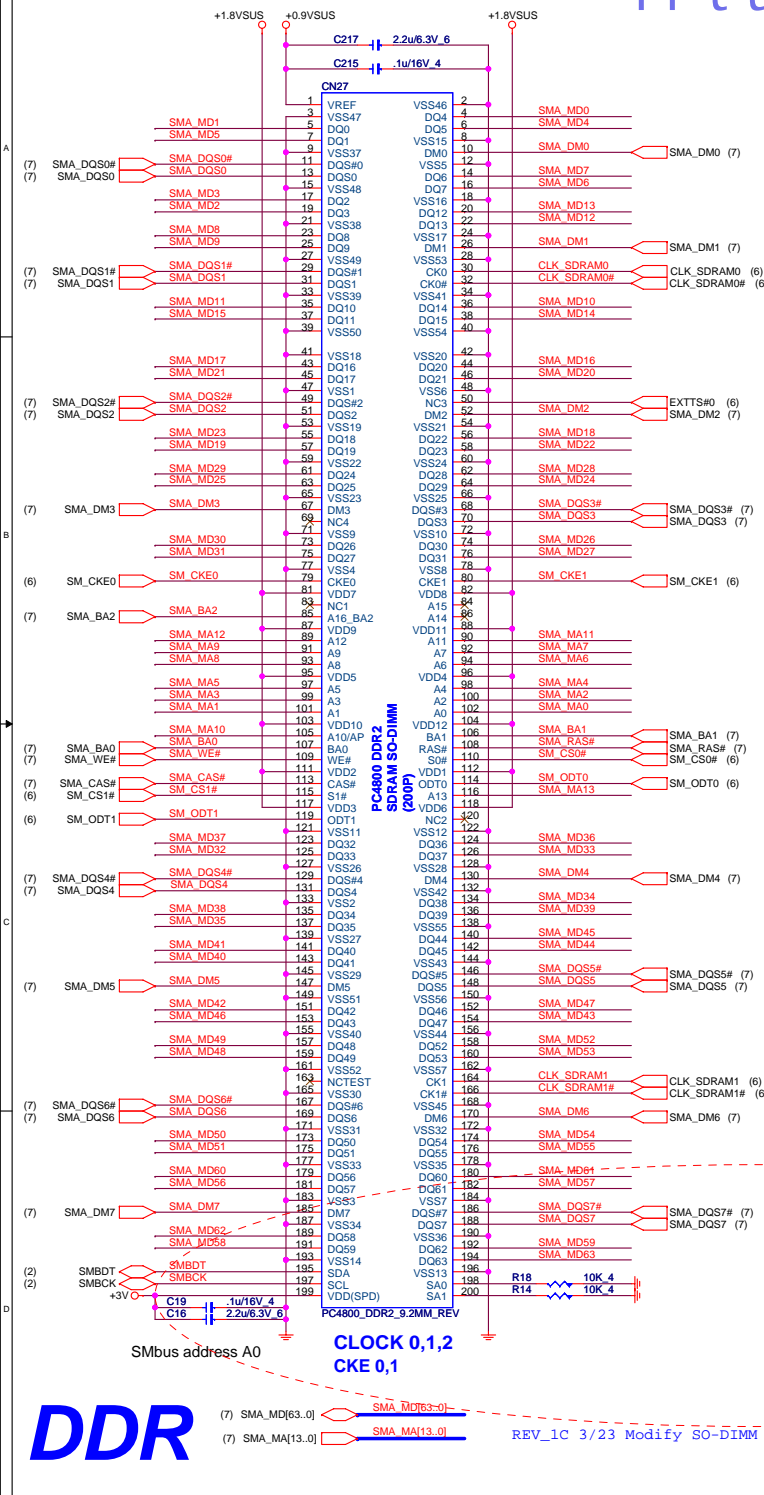
Size	Document Number GMCH (POWER/NCTF)	Rev 1C
Date:	Tuesday, March 20, 2007	Sheet 8 of 28

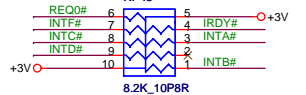
CLG

Size	Document Number	Rev
	GMCH (POWER/GND)	1C
Date:	Tuesday, March 20, 2007	Sheet 9 of 28

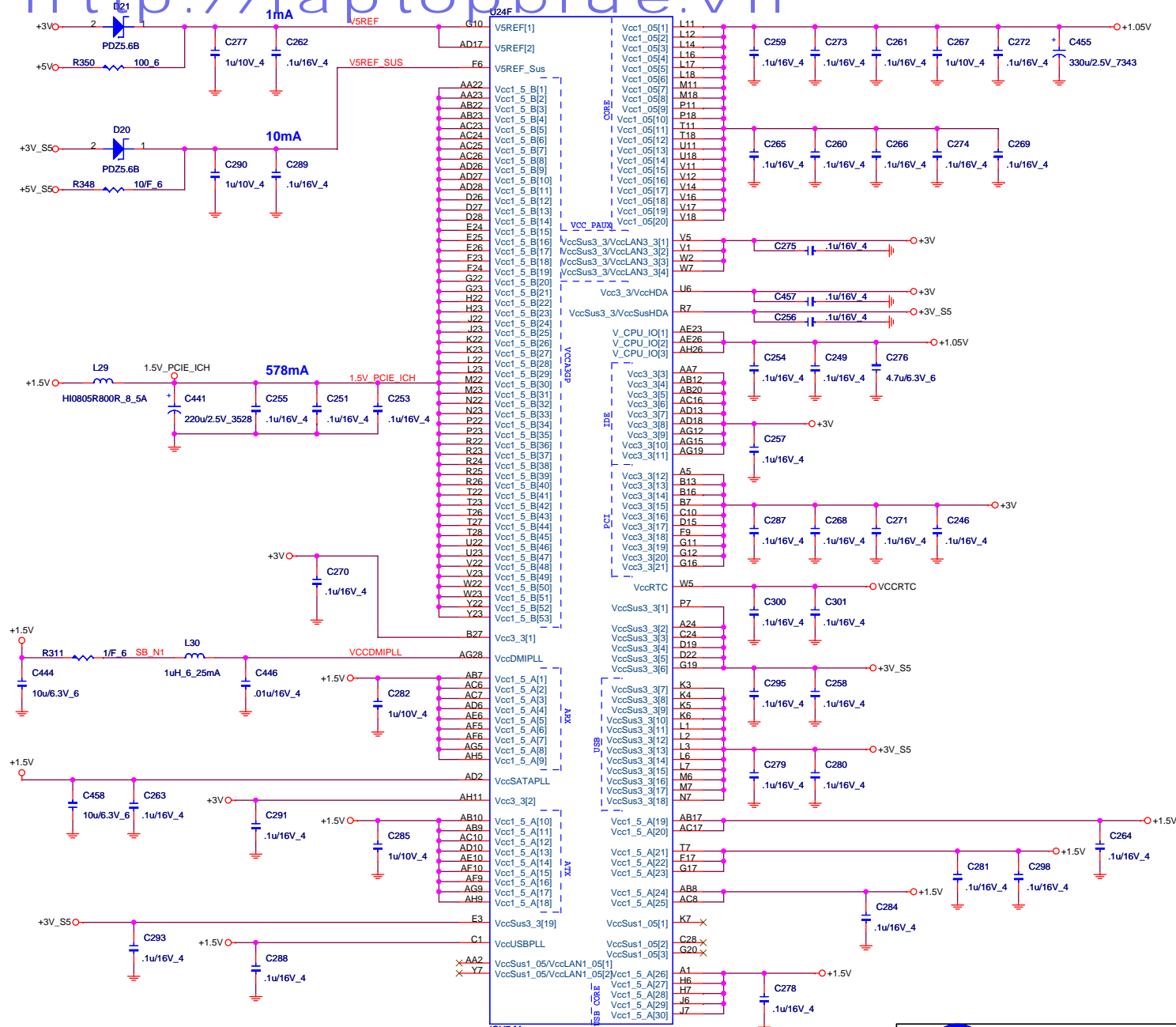
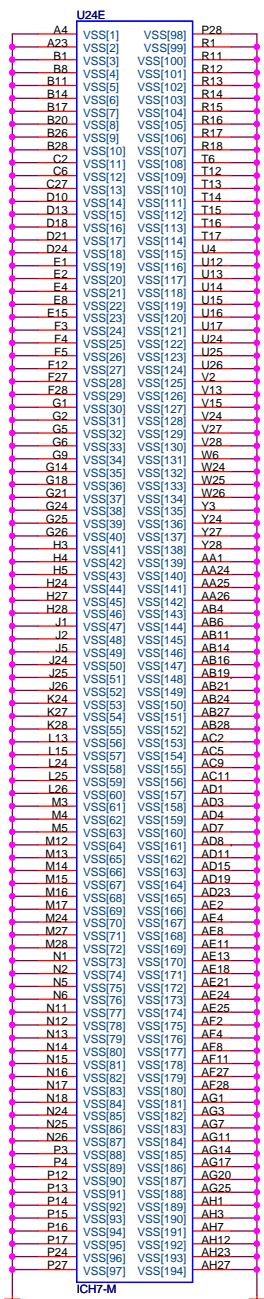
DDR2 SO-DIMM SOCKET

DDR2 TERMINATOR





h t t p : / / l a p t o p b l u e . v n



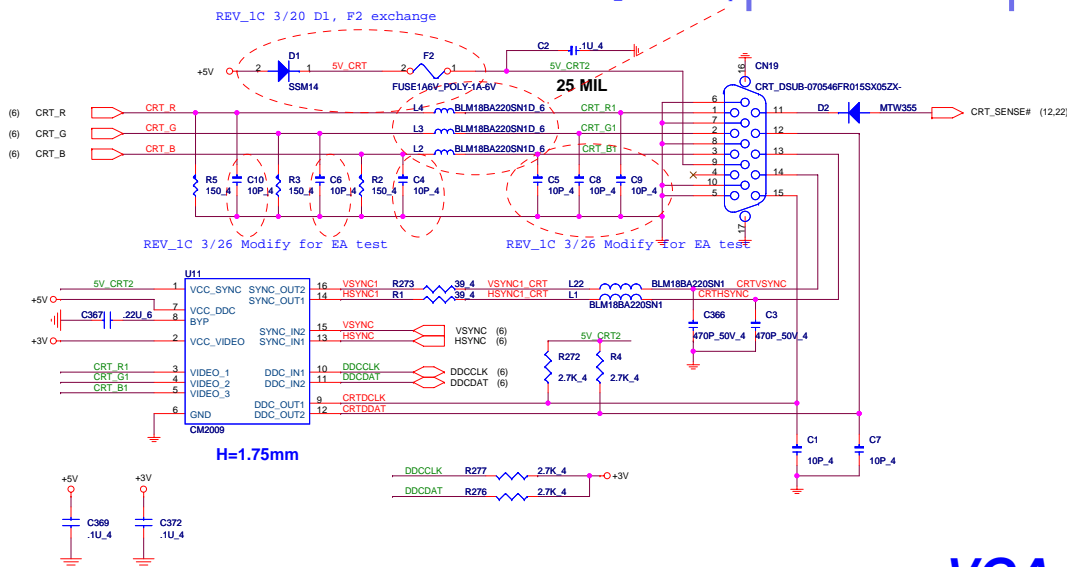
CLG



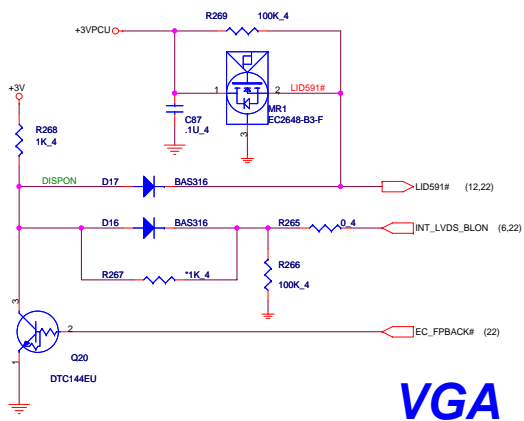
PROJECT : BU1(NAPA)
Quanta Computer Inc.

Size	Document Number ICH7 (POWER)	Rev 1C
Date:	Tuesday, March 20, 2007	Sheet 13 of 28

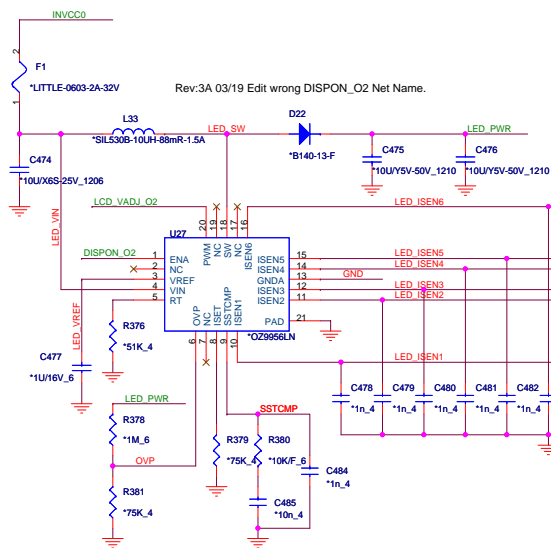
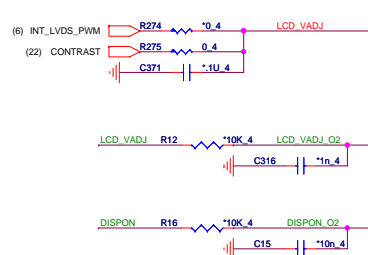
CRT PORT



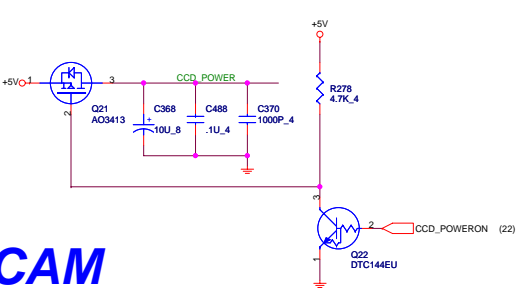
LID SWITCH



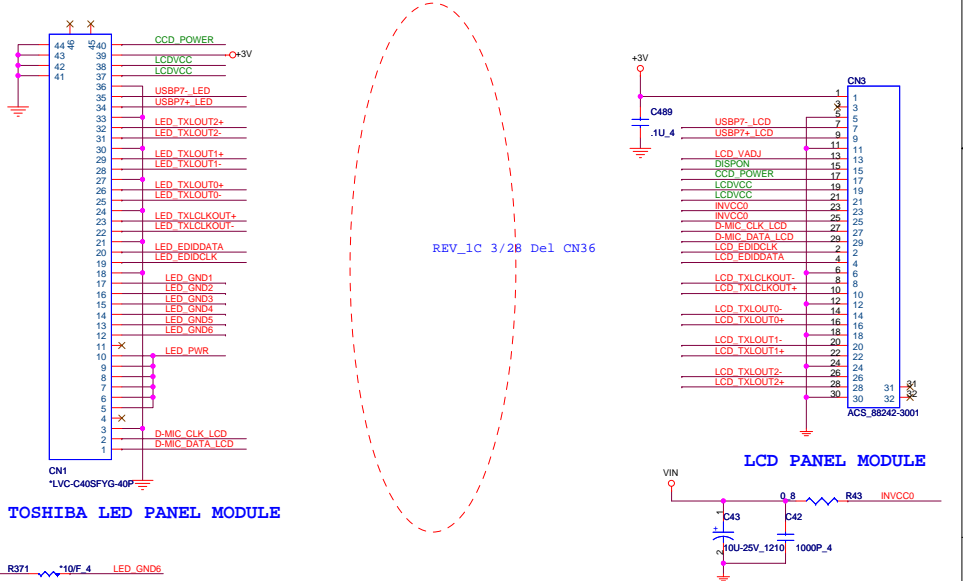
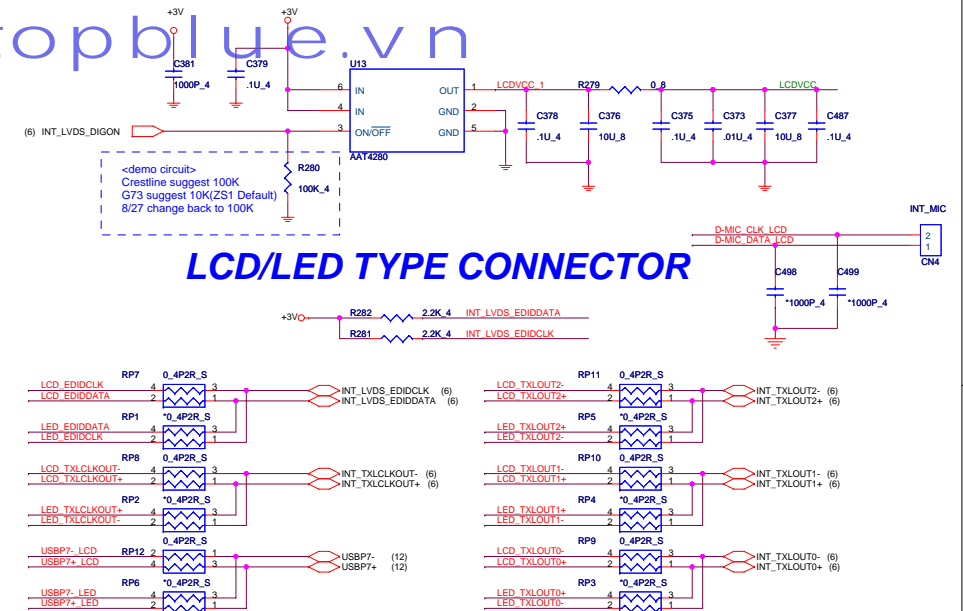
VGA



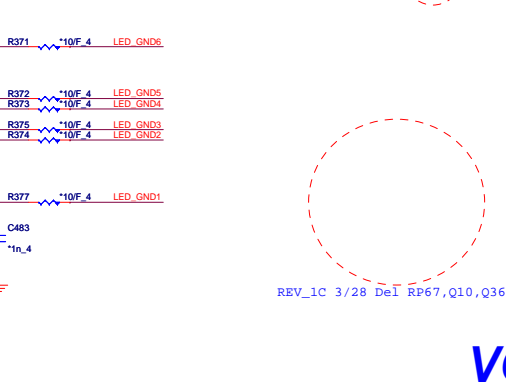
CAMERA MODULE Power



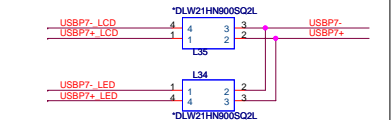
CAM

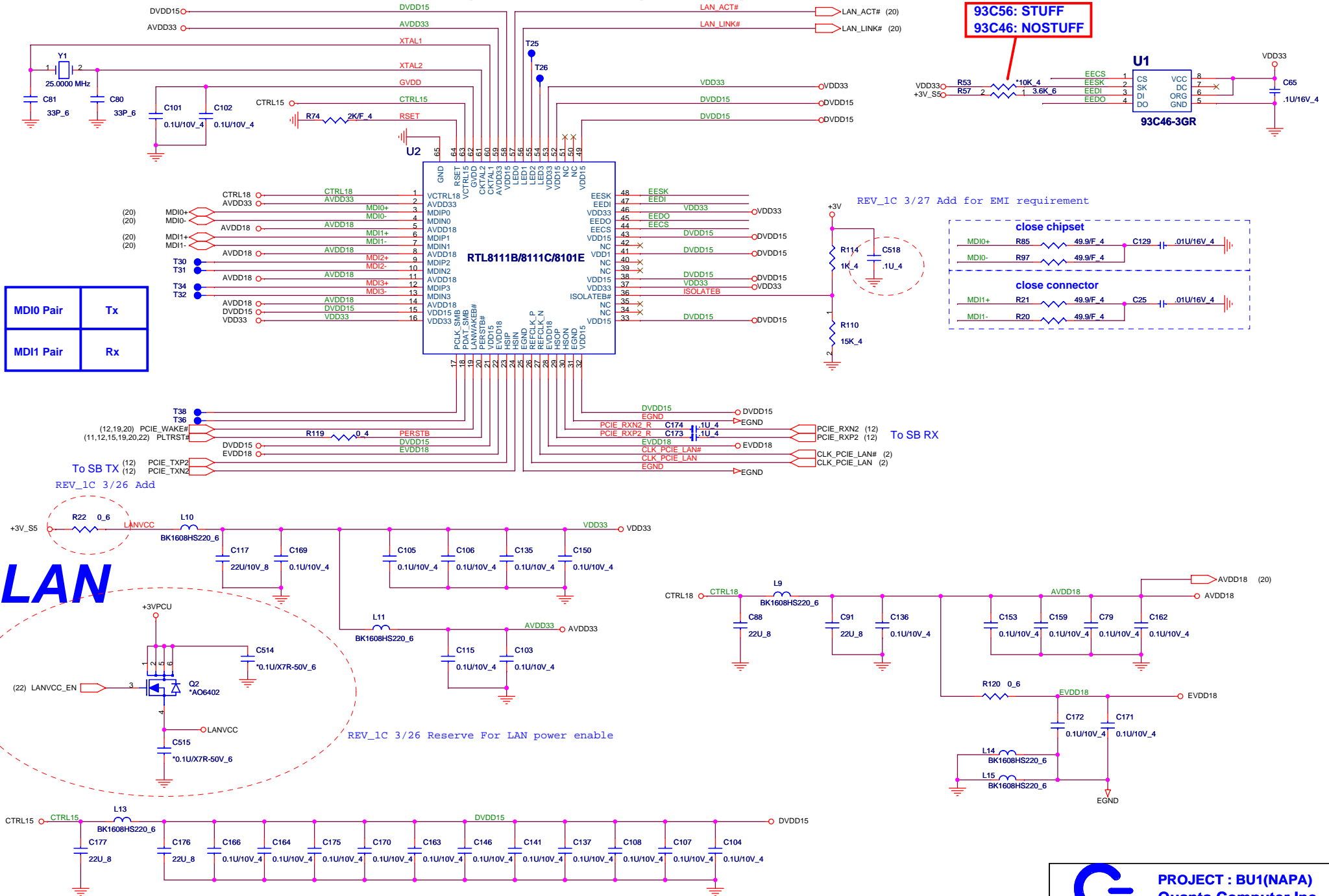


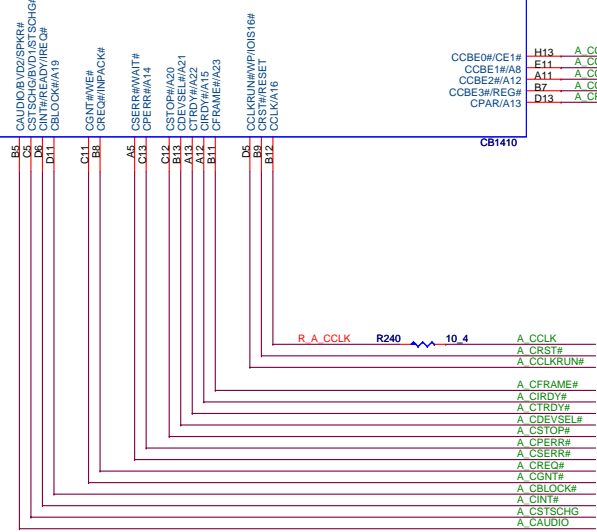
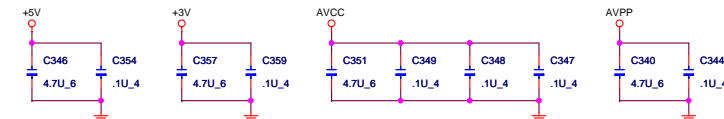
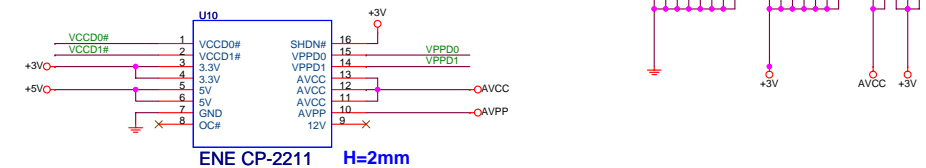
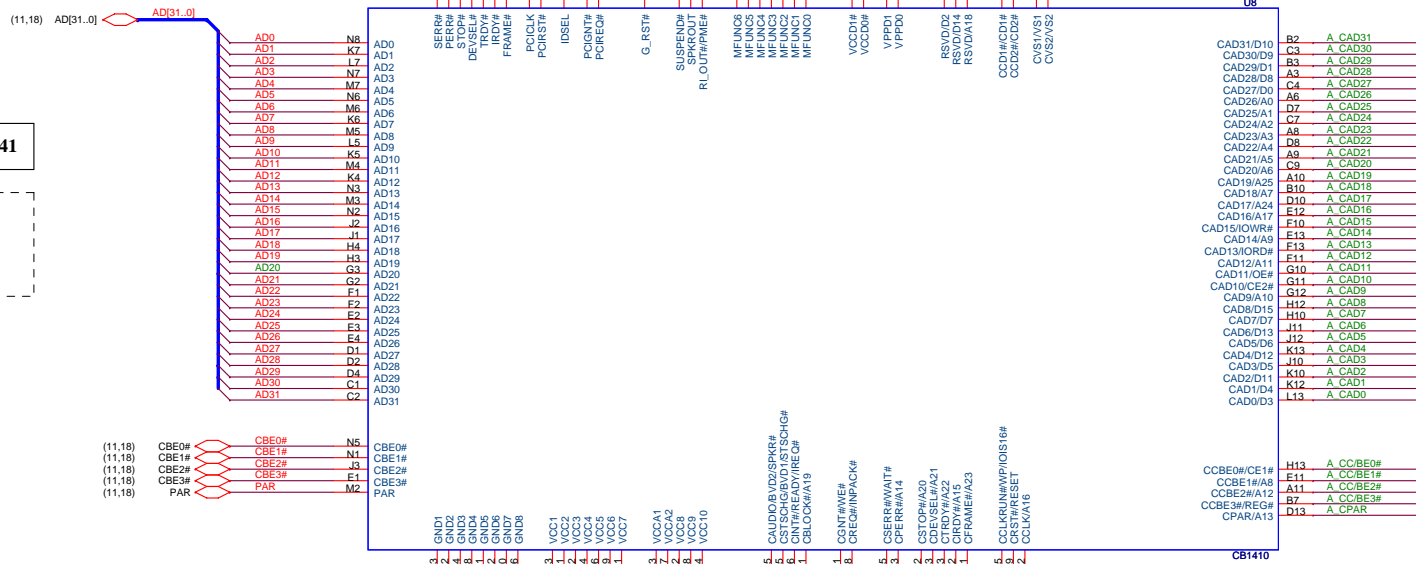
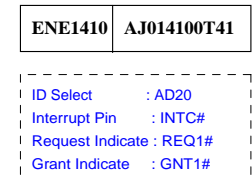
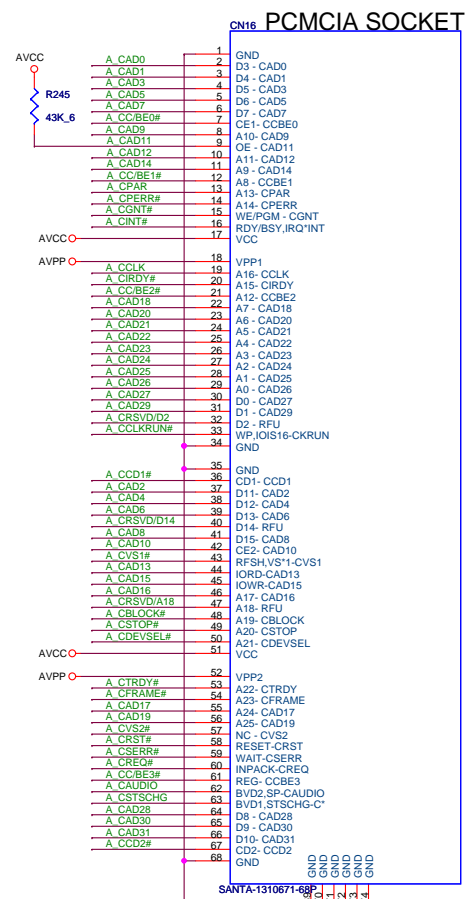
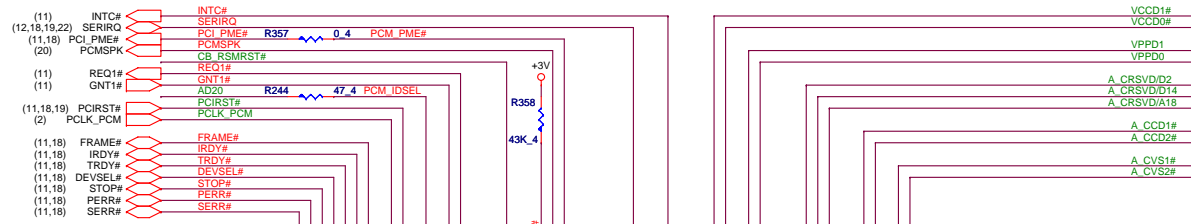
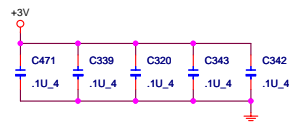
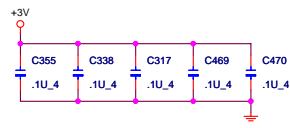
TOSHIBA LED PANEL MODULE



VGA

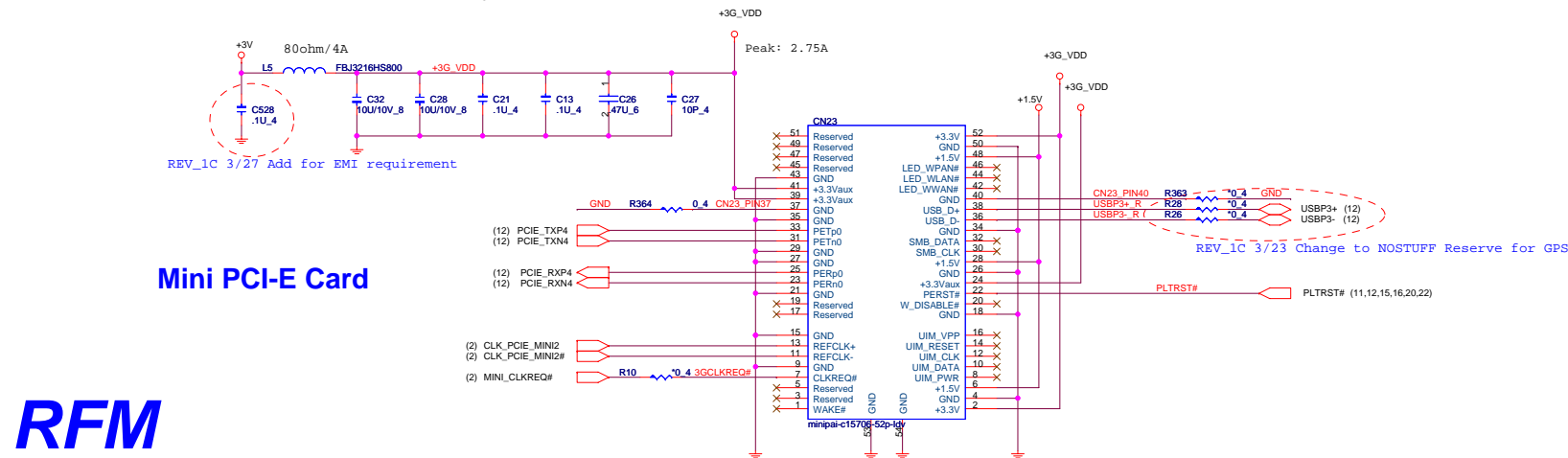
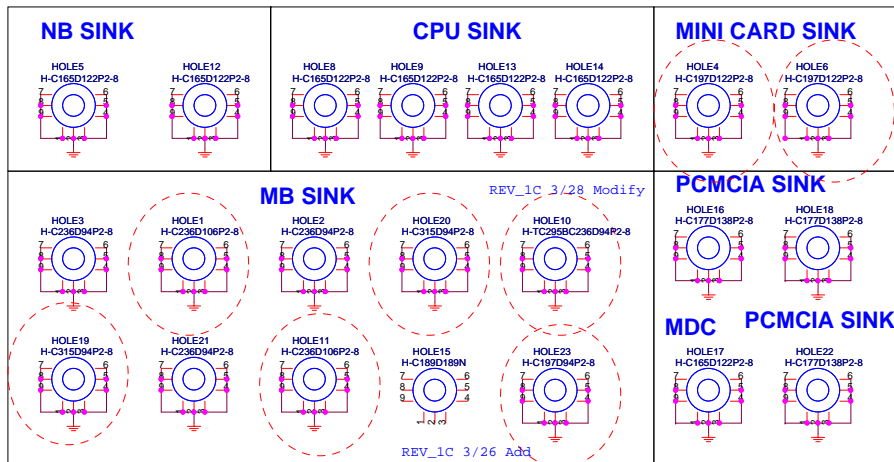






PROJECT : BU1(NAPA)
Quanta Computer Inc.

REV_1C 3/23 Change to +3V_S5 for wake from WLAN

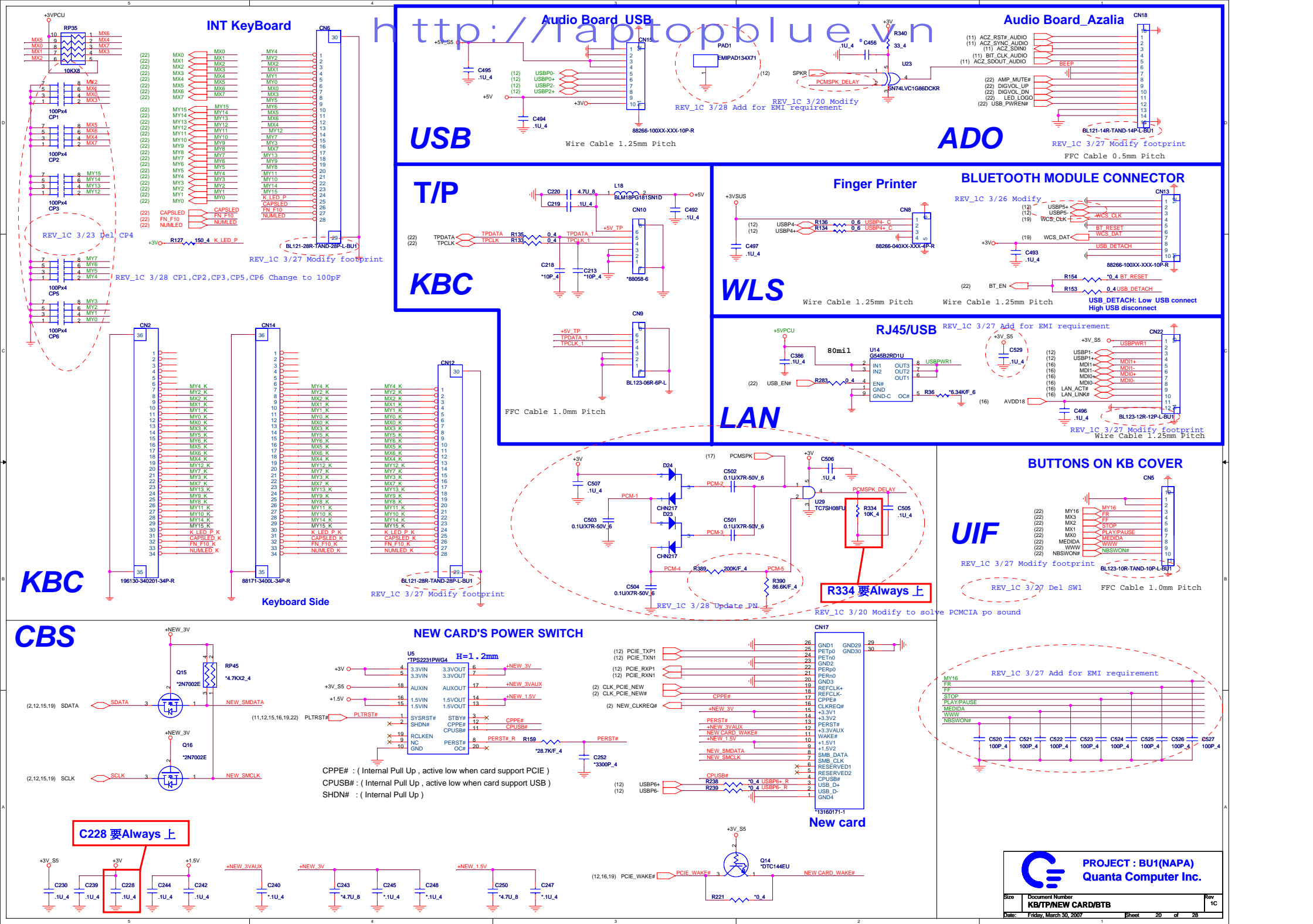
**RFM**

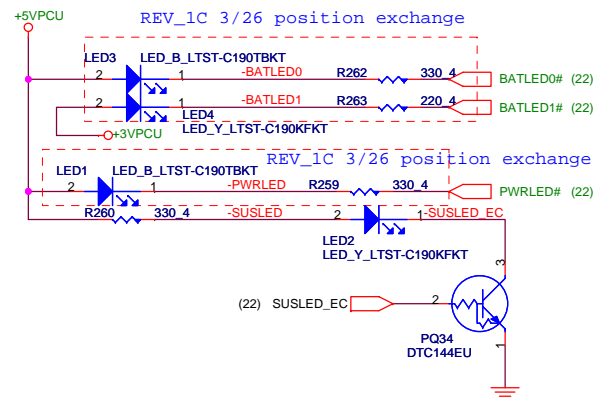
OTH



PROJECT : BU1(NAPA)
Quanta Computer Inc.

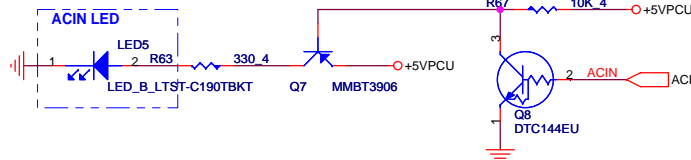
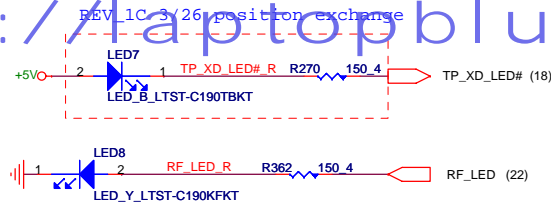
Size	Document Number MINI CARD/HOLE	Rev 1C
Date:	Friday, March 30, 2007	Sheet 19 of 28



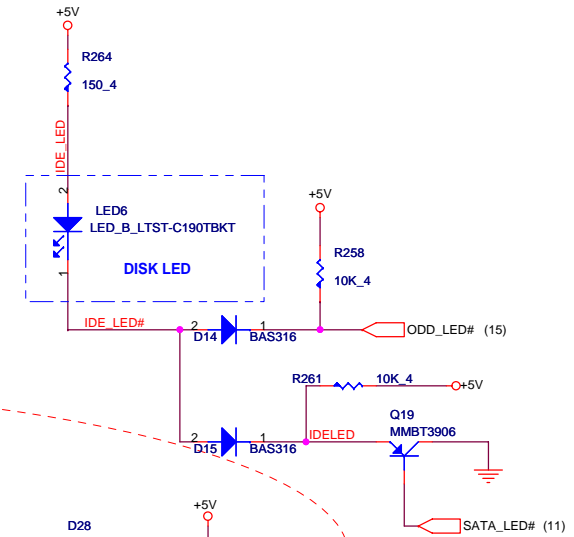


BATTERY
Full Charge --> Blue
Charging --> Orange

POWER
Power On --> Blue
S3 --> Orange



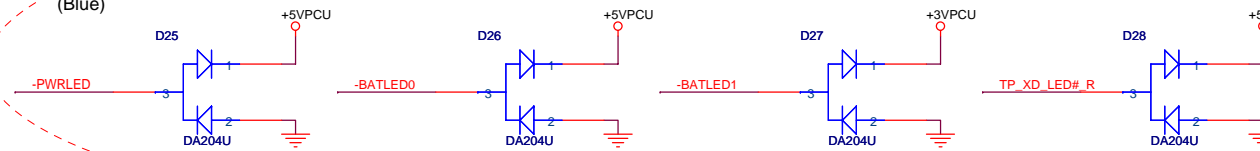
ODD / HDD
Blue



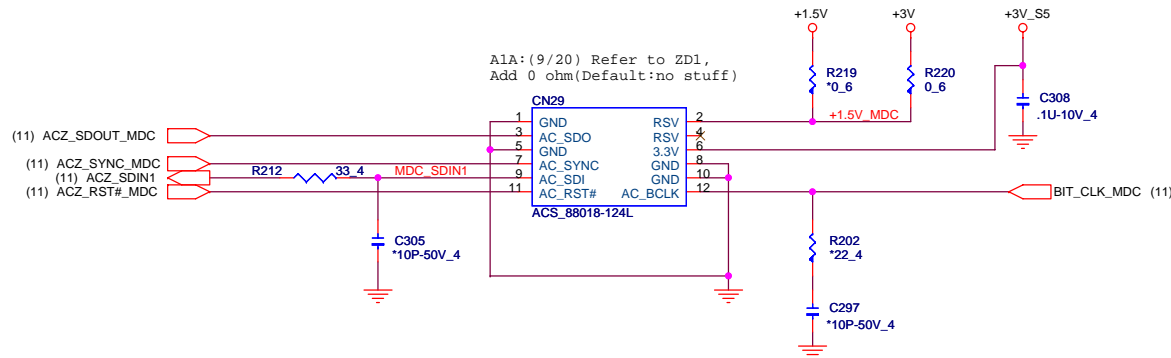
W_LAN&BT / 3G (Amber) (Blue)
DC-IN / Power / Battery / HDD(ODD) / Bridge Media access (Blue) (Blue) (Blue) (Blue) (Amber) (Amber)

UIF

REV_1C 3/23 Add for ESD protection



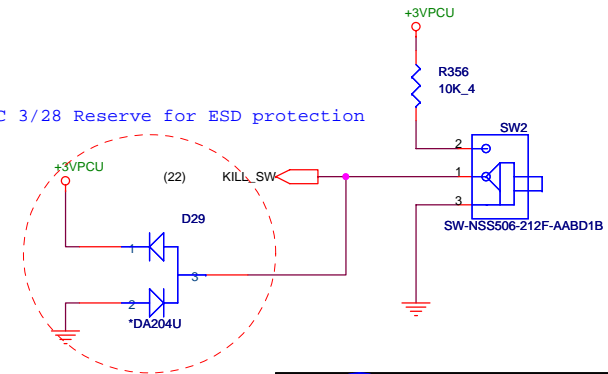
MDC (MODULE)



MDM

W-LAN SWITCH

REV_1C 3/28 Reserve for ESD protection



UIF

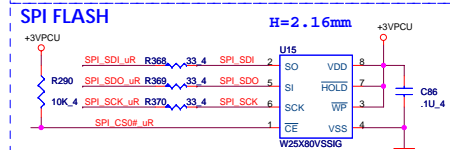


BADDR1-0	I/O Address	
	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

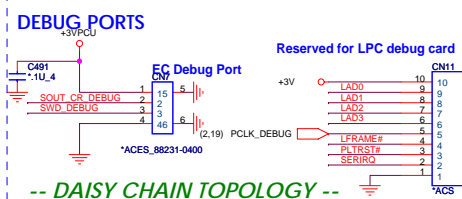
BADDR0 BADDR0 R126 10K

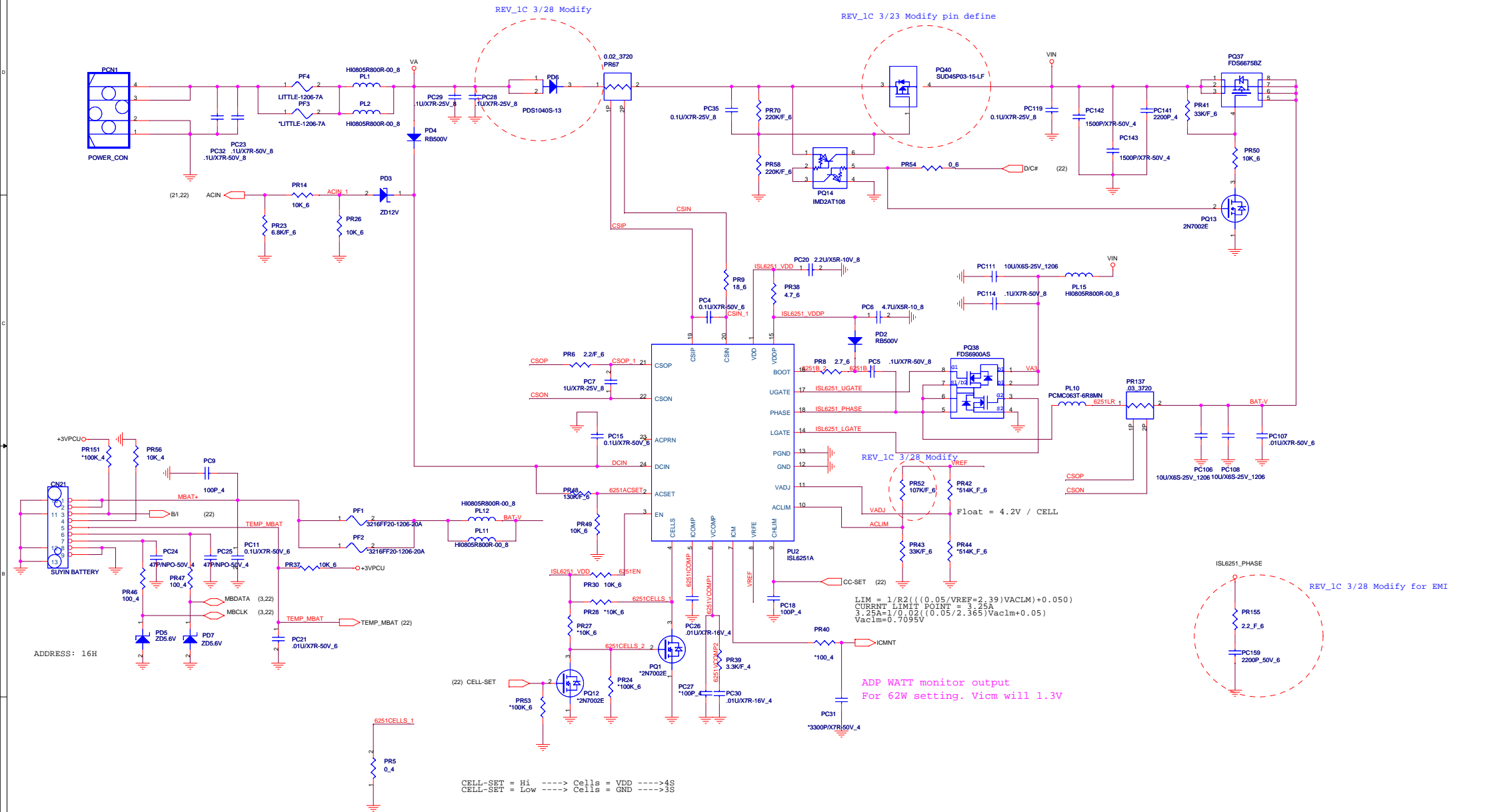
BADDR1 SOUT_CR_DEBUG R123 *10K

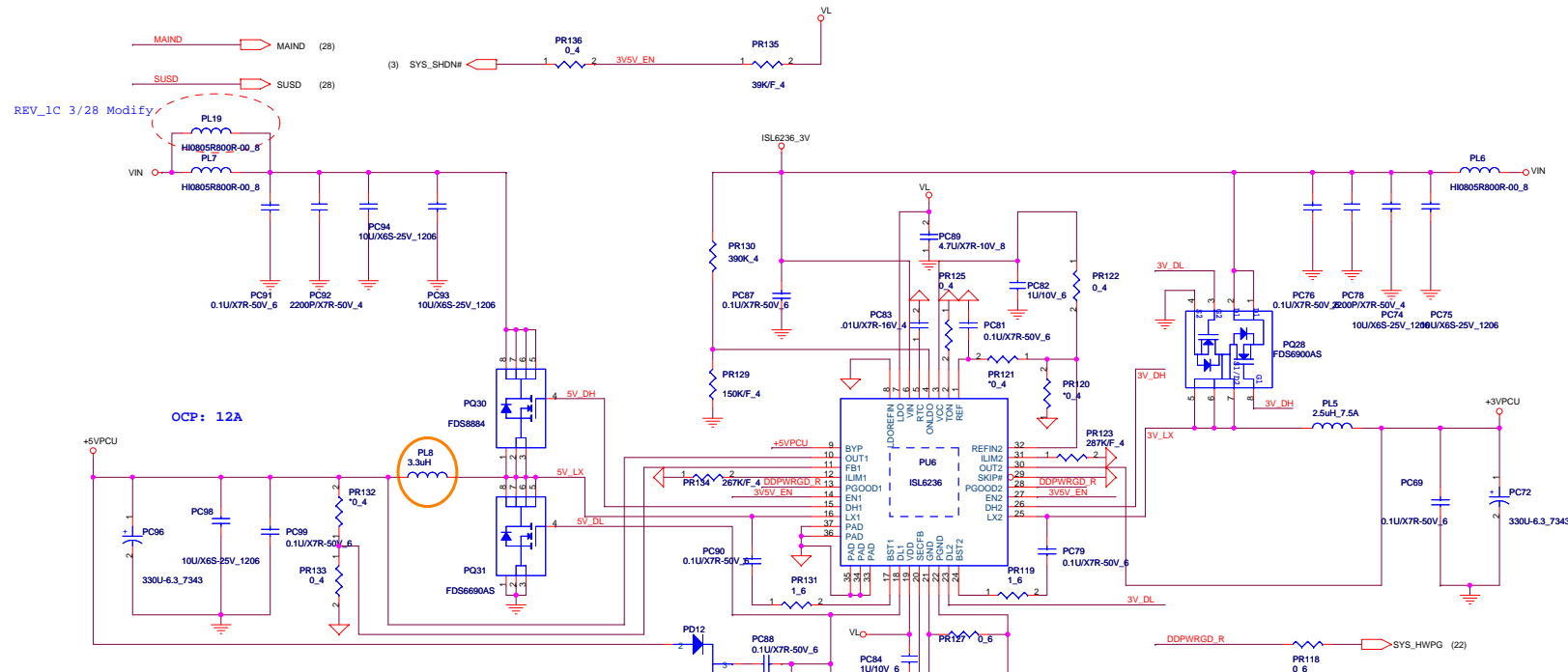
1/13 Confirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware



FWH







OCP: 12A

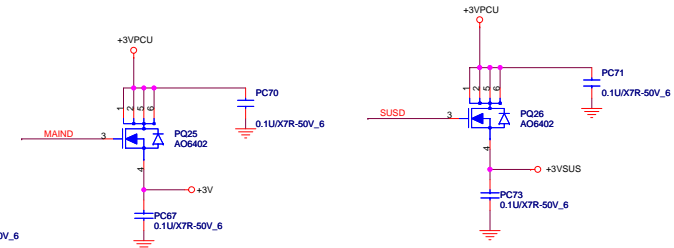
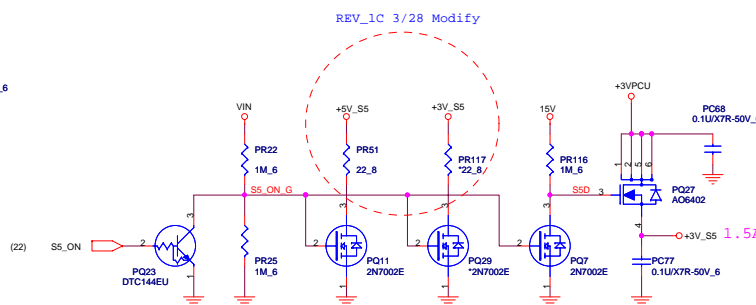
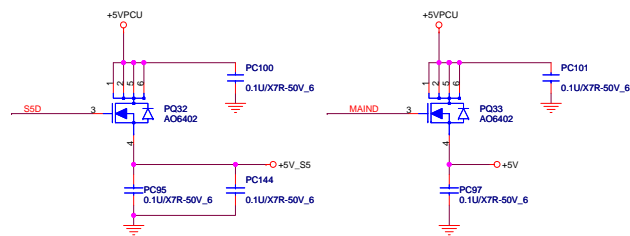
OCP:12A

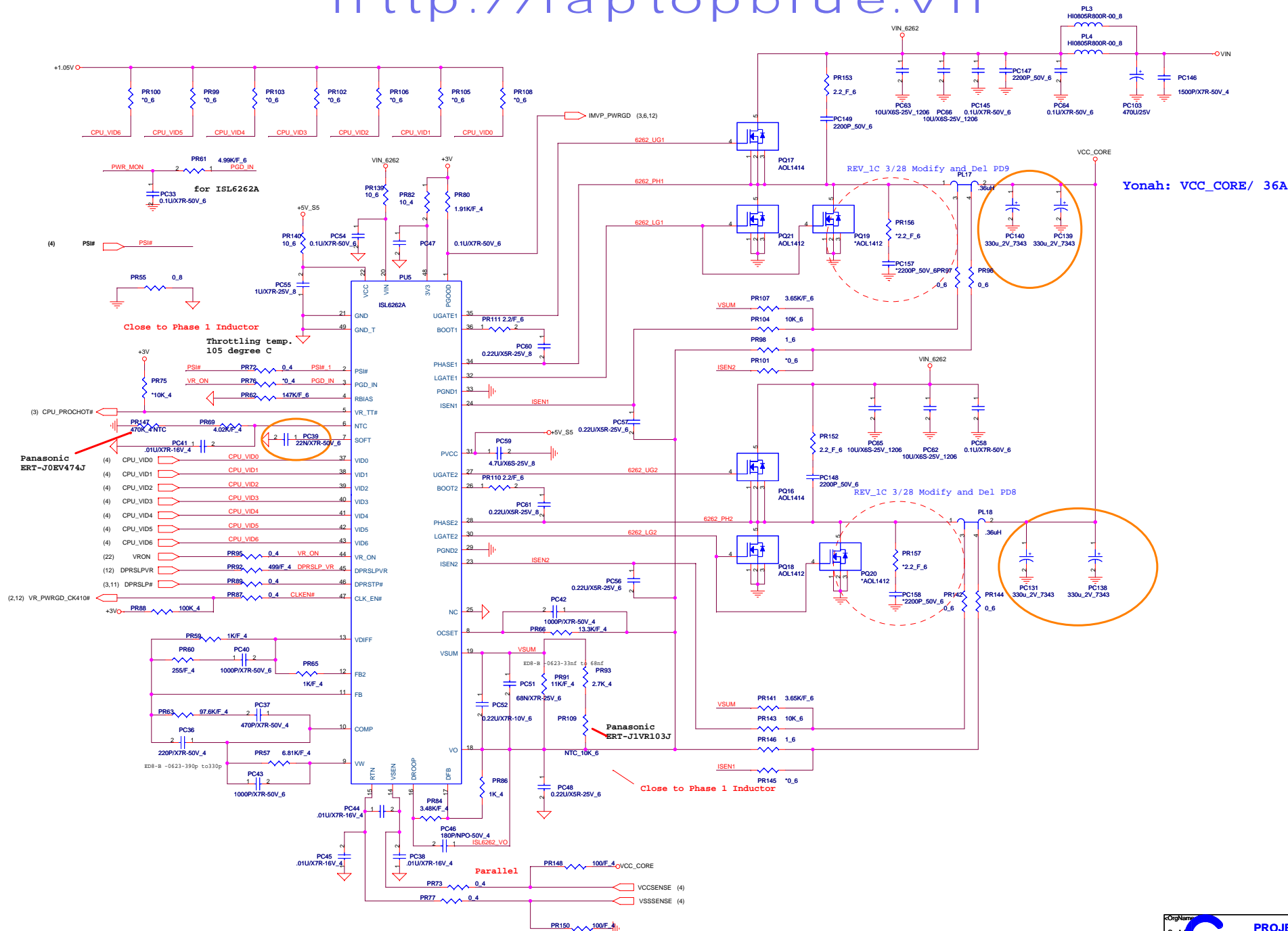
$L(\text{ripple current}) = (19-5) * 5 / (1.5u * 0.4M * 19) \sim 6A$
 $I_{ocp} = 12 - (6/2) = 9A$
 $V_{th} = 9A * 15m\Omega = 135mV$
 $R(I_{lim}) = (135mV * 10) / 5uA \sim 270K$

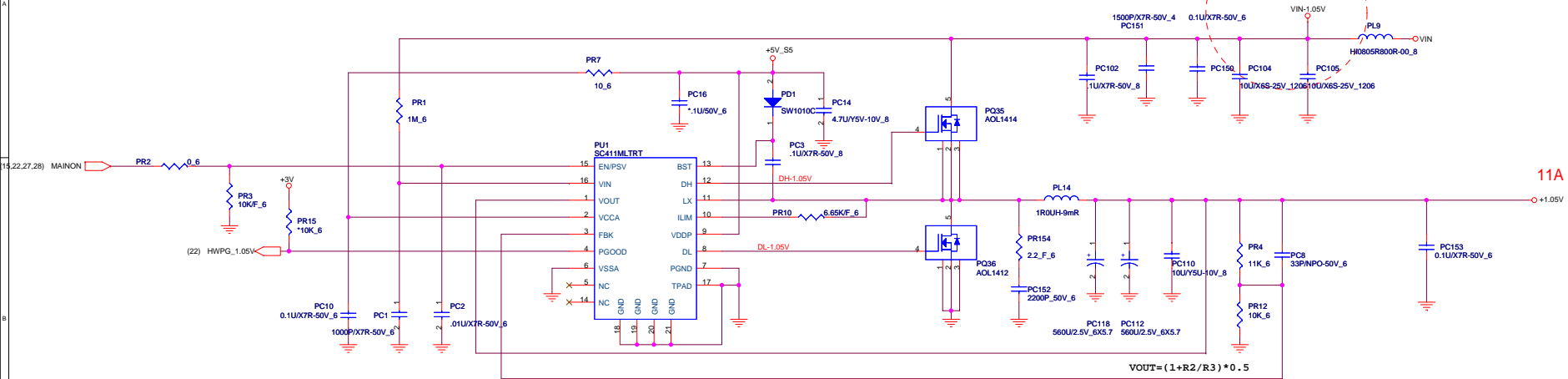
OCP:6.25A

$L(\text{ripple current}) = (19-3.3) * 3.3 / (2.5u * 0.5M * 19) \sim 2.18A$
 $I_{ocp} = 6.25 - (2.18/2) = 5.16A$
 $V_{th} = 5.16A * 28m\Omega = 145mV$
 $R(I_{lim}) = (145mV * 10) / 5uA \sim 294K$

OCP : 6.25A



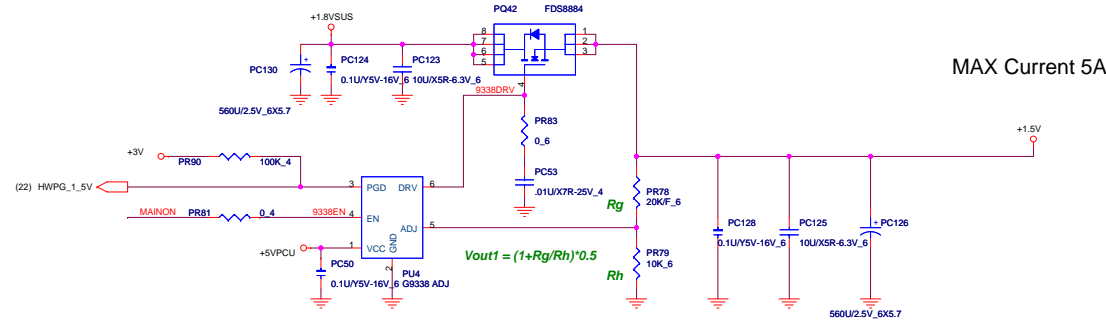




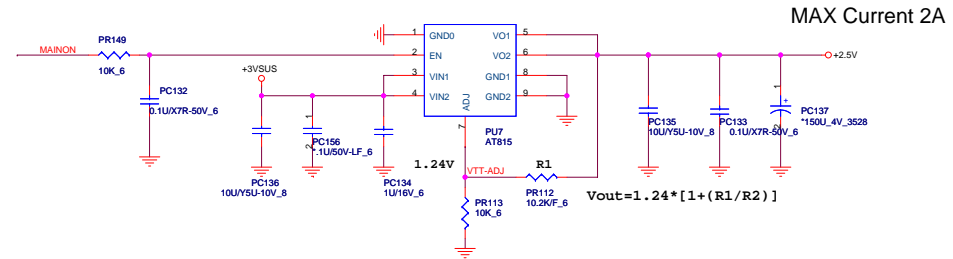
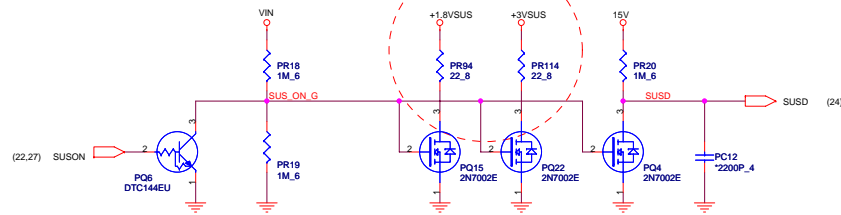
PROJECT : BU1(NAPA)
Quanta Computer Inc.



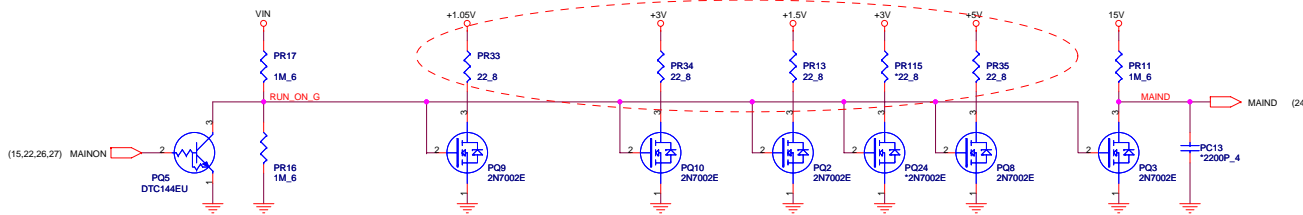
Size	Document Number DDR2 1.8V(TP1116)	Rev 1C
Date:	Thursday, March 29, 2007	Sheet 27 of 28



REV_1C 3/28 Modify



REV_1C 3/28 Modify



PROJECT : BU1(NAPA)
Quanta Computer Inc.

PROJECT MODEL :	BU1	APPROVED BY:	Vic Lin #15598	DATE:	2007/01/04	DOC NO. 204
PART NUMBER:	31BU1MB0010	DRAWING BY:	Jack Lin #17535	REVISION:	1A	SHEET: 1 of 3

[illegible]