



LA-7491P
DA60000N810

http://laptopblue.vn

Compal Confidential

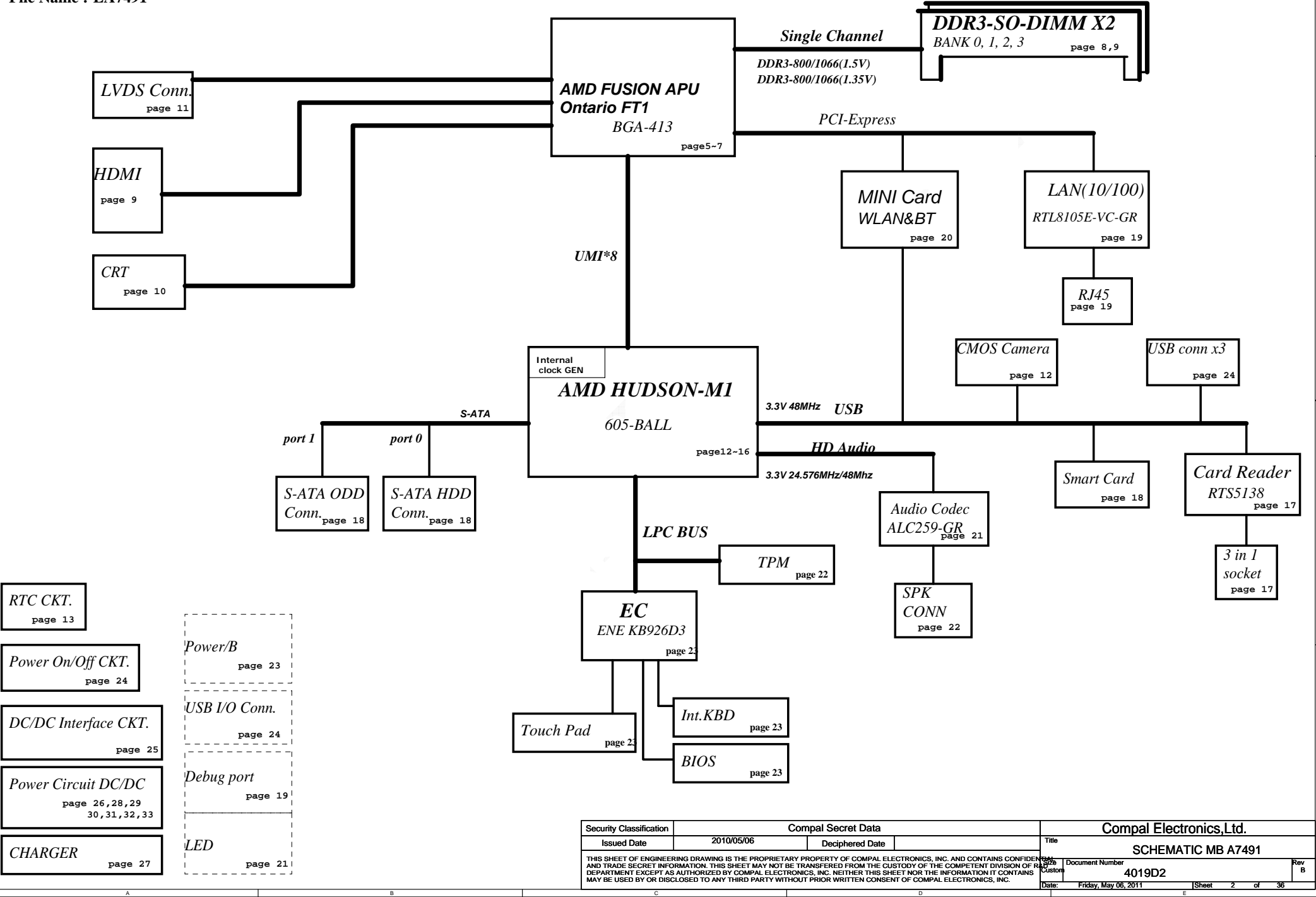
Brazos PCW20 LA7491 Schematics Document

AMD APU Ontario-FT1+ FCH Hudson-M1

2011-03-29

REV:1.0

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DDR3 Voltage Rails

power plane State	+B +3VL +5VL +RTCVCC	+5VALW +3VALW +1.1VALW	+1.5V	+5VS +3VS +1.5VS +CPU_CORE +NB_CORE +1.8VS +0.75VS +1.1VS +1.0VS
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

@	Reserve
CONN@	ME CONNECTOR
8105E@	100M LAN function
8111E@	GLAN function
REAL@	ALC259-GR
VIA@	V1802T
ROM@	not support flash ROM
FROM@	Support flash ROM

FCH SM Bus0 address

Device	HEX	Address
SDDIM I	A0	1010 0000
SDDIM II	A2	1010 0010

FCH SM Bus1 address

Device	HEX	Address
WLAN		

EC SM Bus1 address

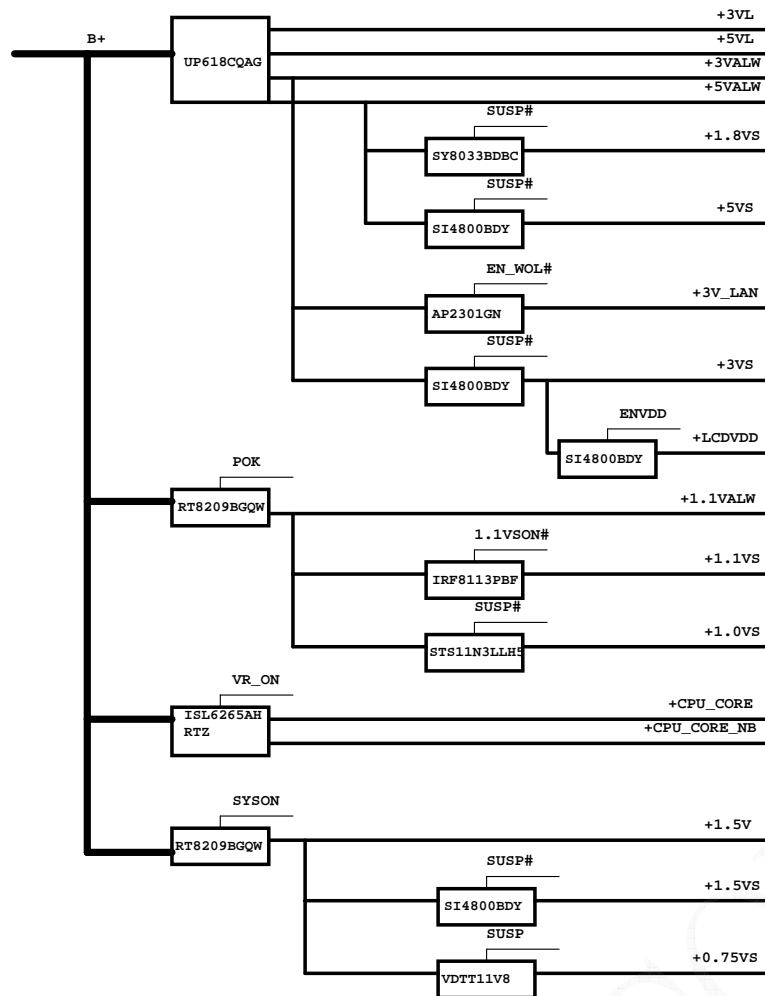
Device	HEX	Address
Smart Battery	16H	0001 011X b

EC SM Bus2 address

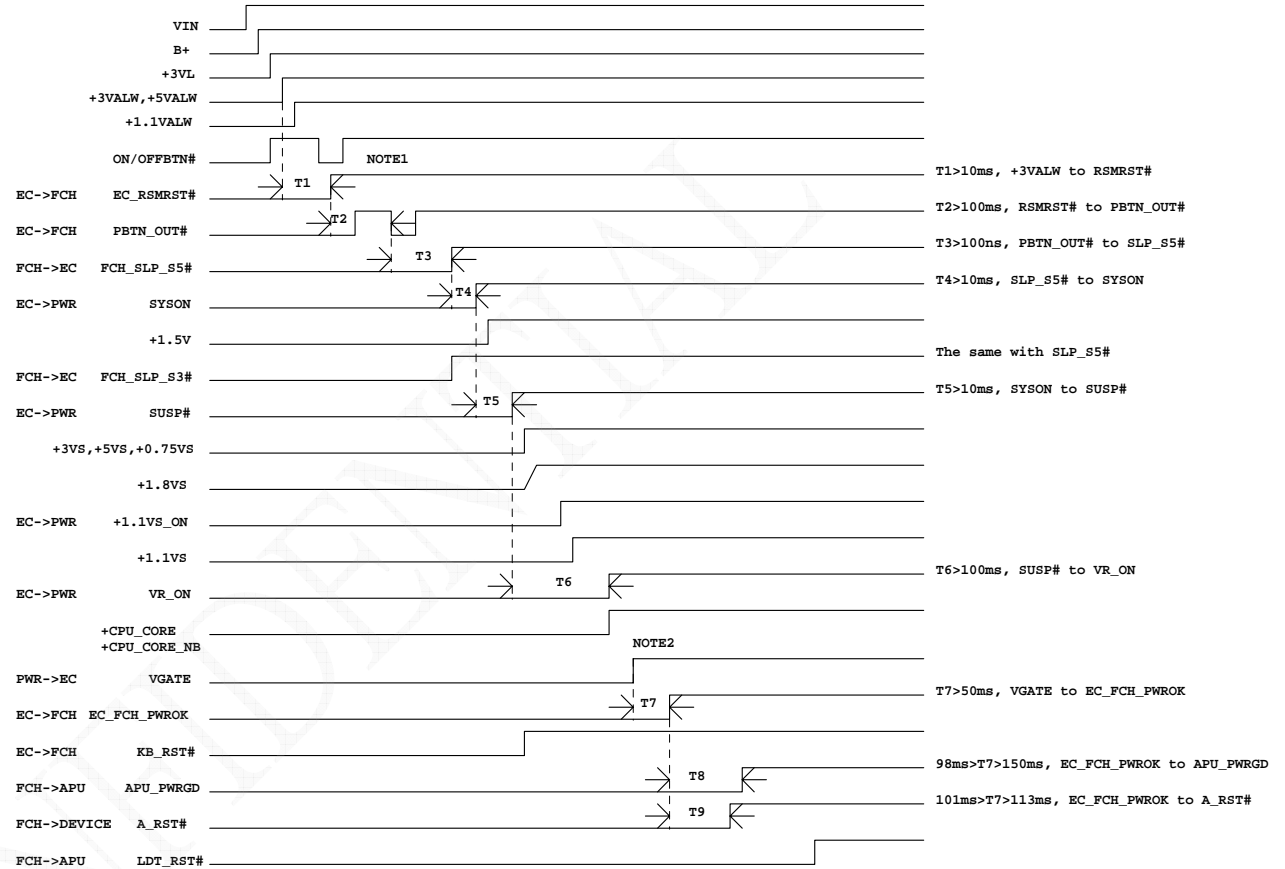
Device	HEX	Address
APU internal thermal sensor		1001 100X b

	SOURCE	POWER PLAN	HDMI	LVDS	CRT	FCH	CPU CORE	SDDIM I/II	WLAN	BATT	APU
TDP1_AUXP TDP1_AUXN	APU	+3VS	V								
LTDP0_AUXP LTDP1_AUXN	APU	+3VS		V +5VS							
DAC_SCL DAC_SDA	APU	+3VS			V +5VS						
SIC SID	APU	+3VS				V +3VALW					
SVC SVD	APU	+1.8VS					V				
SMB_FCH_CK0 SMB_FCH_DA0	FCH	+3VS						V			
SMB_FCH_CK1 SMB_FCH_DA1	FCH	+3VALW							V		
SMB_EC_CK1 SMB_EC_DA1	EC	+5VALW								V	
SMB_EC_CK2 SMB_EC_DA2	EC	+3VS									V

POWER MAP

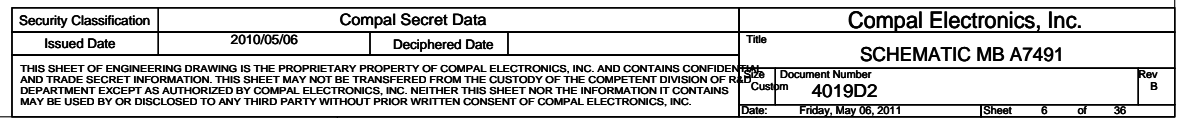


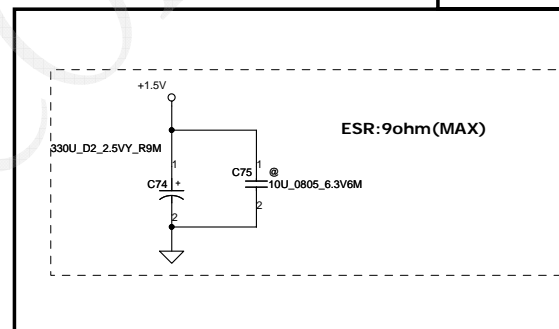
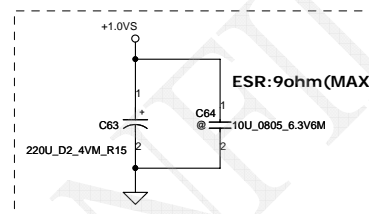
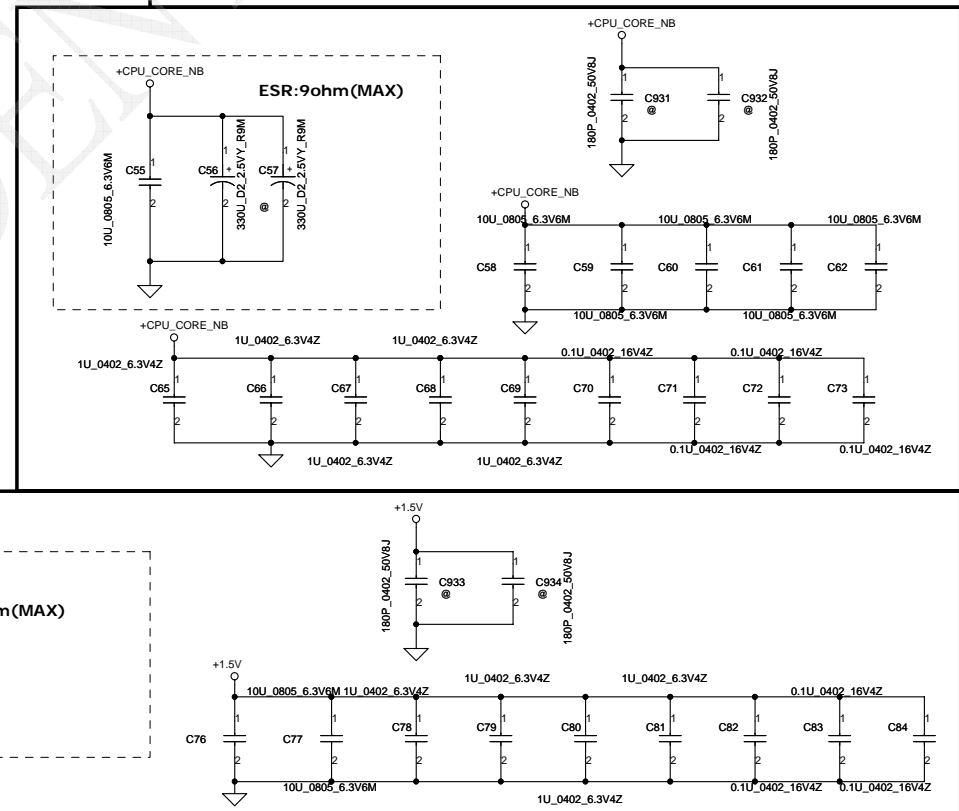
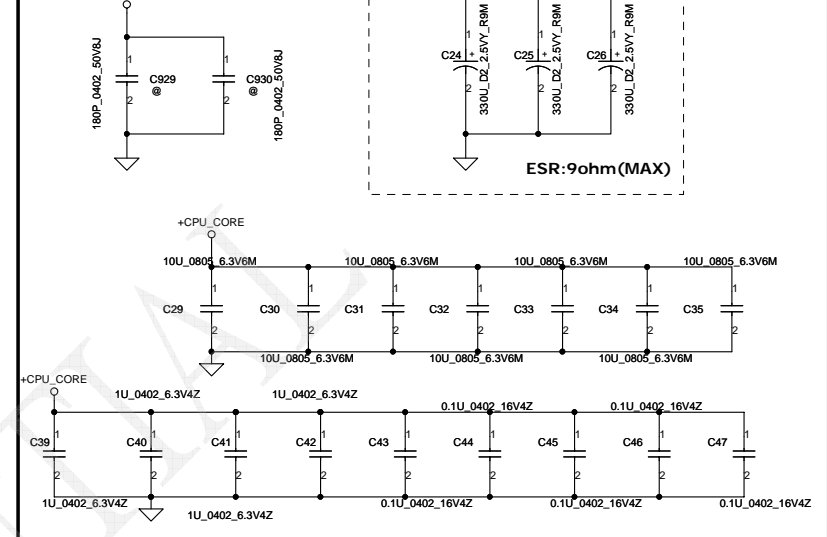
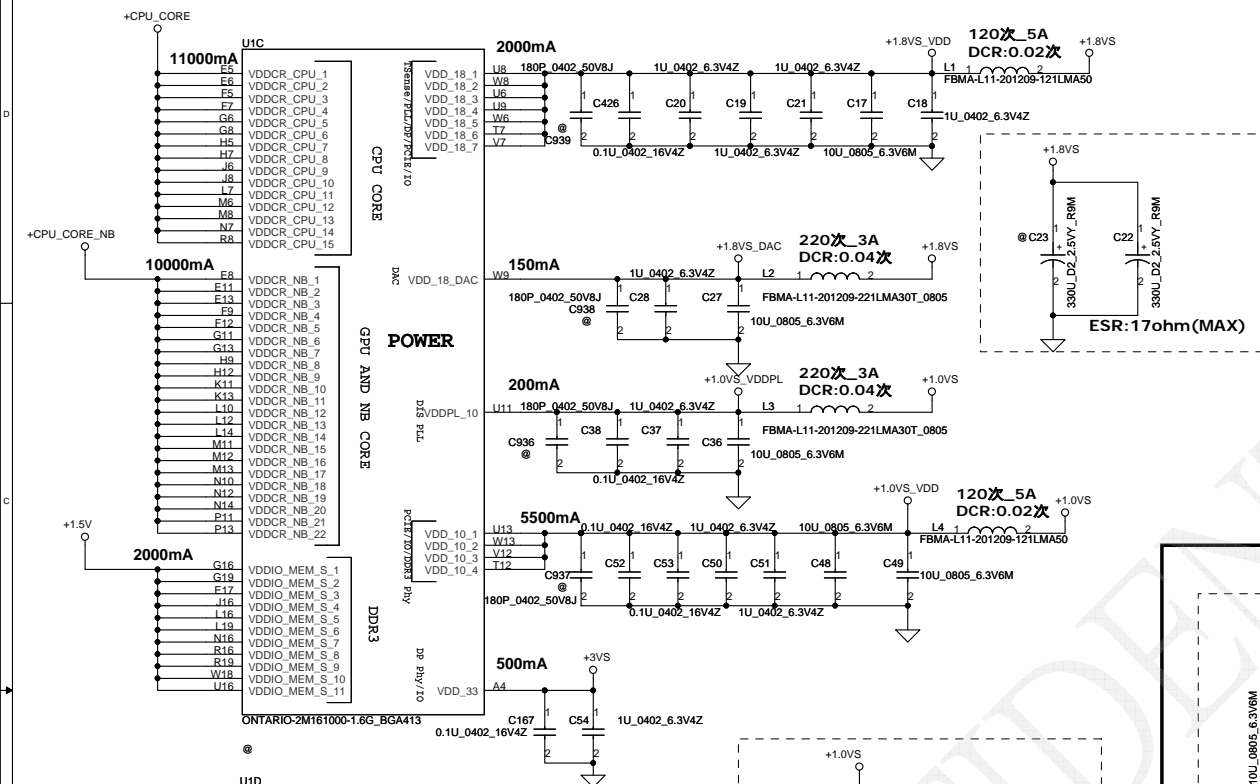
POWER SEQUENCE



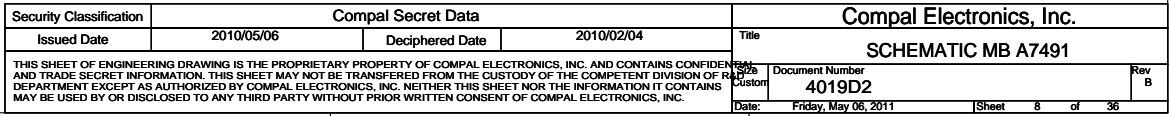
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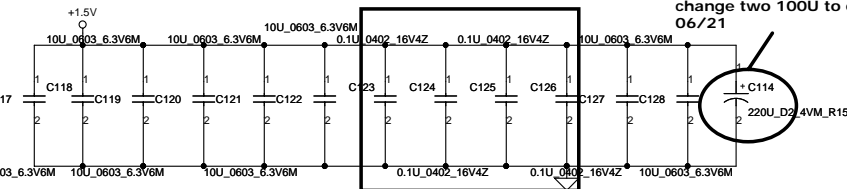


<6.8> DDR_DQS#[0..7]
 <6.8> DDR_D[0..63]
 <6.8> DDR_DM[0..7]
 <6.8> DDR_DQS[0..7]
 <6.8> DDR_MA[0..15]

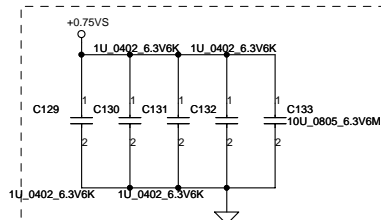
Layout Note:
Place near JP3

Layout Note: Place these 4 Caps near Command
and Control signals of DIMMA

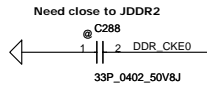
change two 100U to one 220U
06/21



Layout Note:
Place near JP3.203 & JP3.204

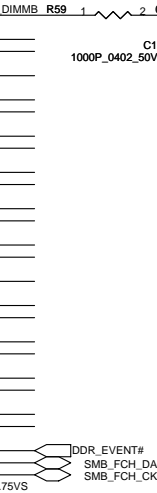
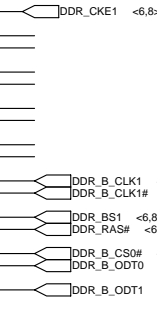
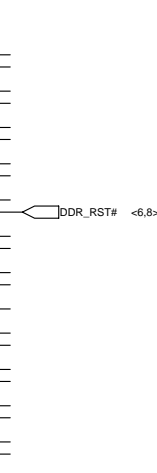
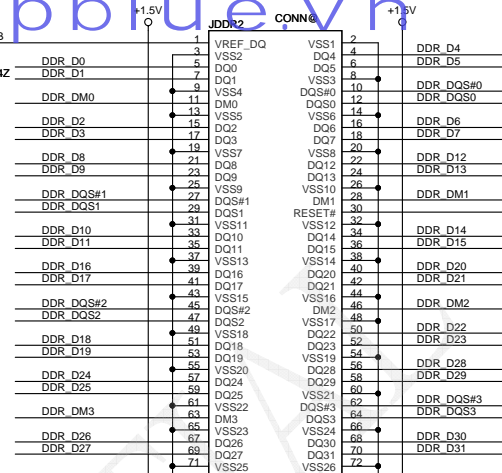
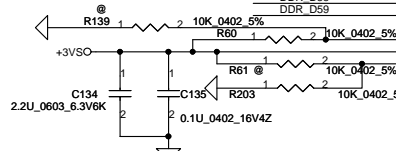


	SA0	SA1
Compal common design	0	1
ADM CRB	1	0



<6.8> DDR_CKE0
 <6.8> DDR_BS2

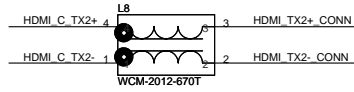
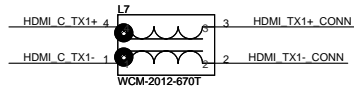
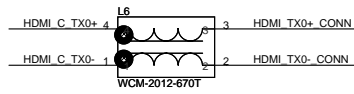
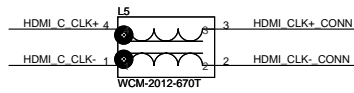
<6.8> DDR_B_CLK0
 <6.8> DDR_B_CLK0#
 <6.8> DDR_BS0
 <6.8> DDR_WE#
 <6.8> DDR_CAS#
 <6.8> DDR_B_CS#



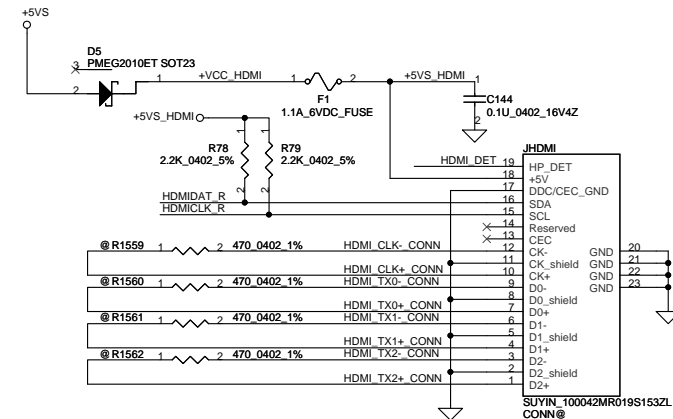
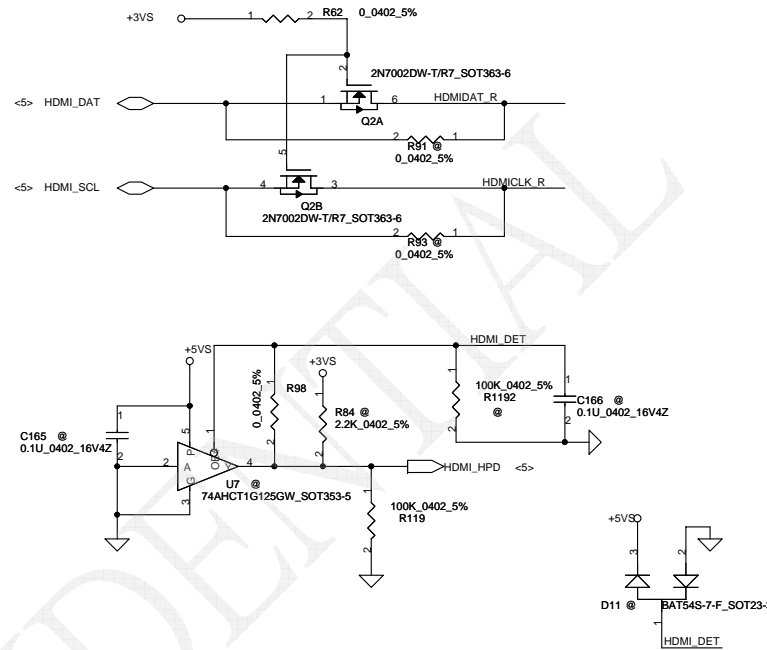
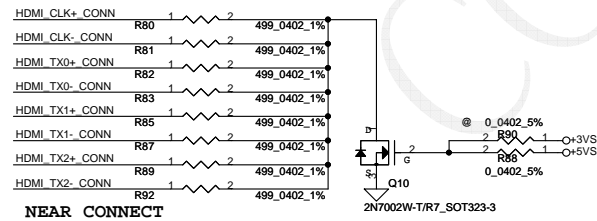
DDR3 SO-DIMM B
REV Type

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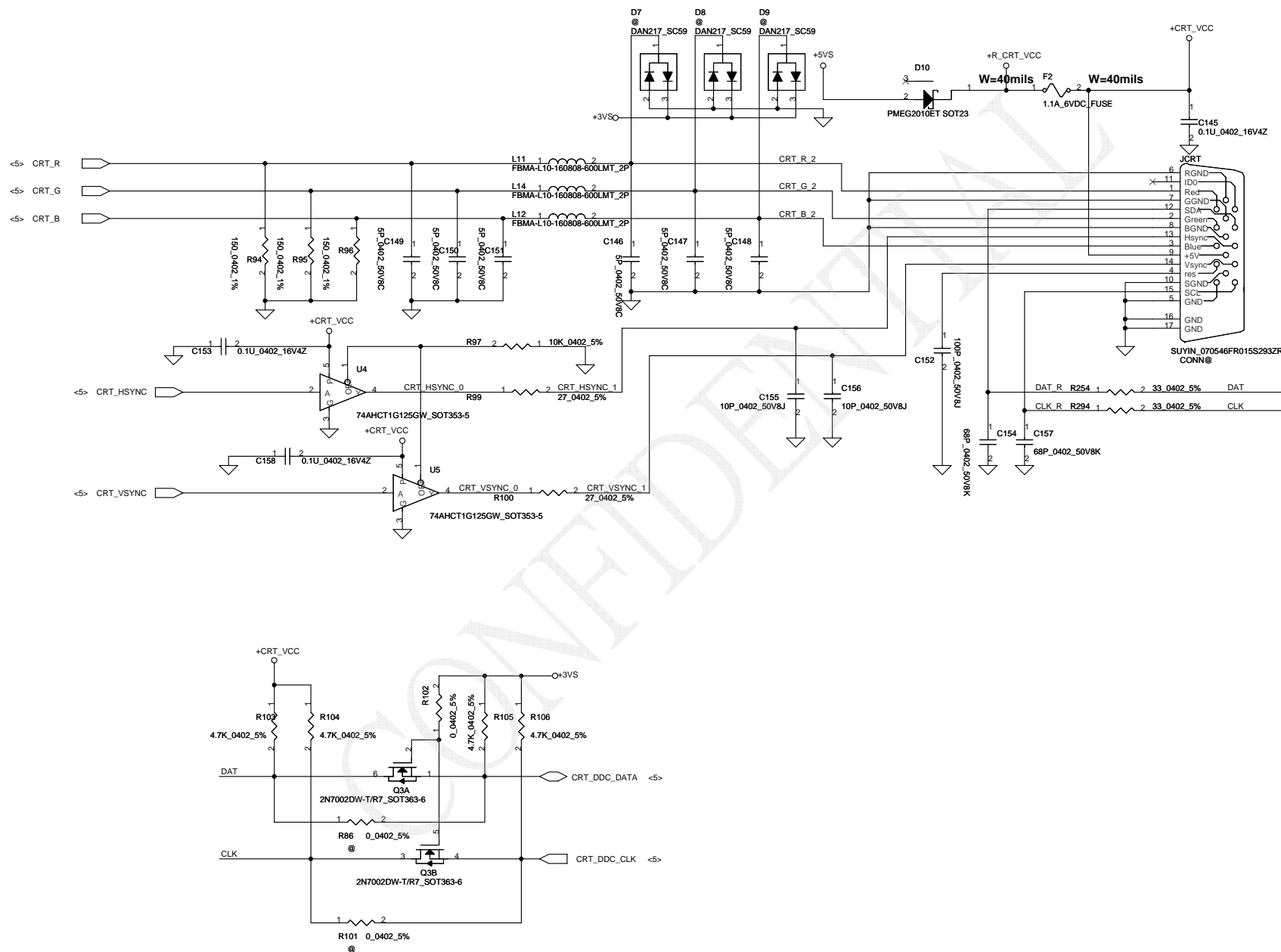
<5> HDMI_CLK-	HDMI_CLK-	C136	1	2	0.1U_0402_16V7K	HDMI_C_CLK-
<5> HDMI_CLK+	HDMI_CLK+	C137	1	2	0.1U_0402_16V7K	HDMI_C_CLK+
<5> HDMI_TX2+	HDMI_TX2+	C138	1	2	0.1U_0402_16V7K	HDMI_C_TX2+
<5> HDMI_TX2-	HDMI_TX2-	C139	1	2	0.1U_0402_16V7K	HDMI_C_TX2-
<5> HDMI_TX1+	HDMI_TX1+	C140	1	2	0.1U_0402_16V7K	HDMI_C_TX1+
<5> HDMI_TX1-	HDMI_TX1-	C141	1	2	0.1U_0402_16V7K	HDMI_C_TX1-
<5> HDMI_TX0+	HDMI_TX0+	C142	1	2	0.1U_0402_16V7K	HDMI_C_TX0+
<5> HDMI_TX0-	HDMI_TX0-	C143	1	2	0.1U_0402_16V7K	HDMI_C_TX0-



HDMI_C_CLK+	@	R65	1	2	0.0402_5%	HDMI_CLK+ CONN
HDMI_C_CLK-	@	R66	1	2	0.0402_5%	HDMI_CLK- CONN
HDMI_C_TX0+	@	R67	1	2	0.0402_5%	HDMI_TX0+ CONN
HDMI_C_TX0-	@	R68	1	2	0.0402_5%	HDMI_TX0- CONN
HDMI_C_TX1+	@	R71	1	2	0.0402_5%	HDMI_TX1+ CONN
HDMI_C_TX1-	@	R72	1	2	0.0402_5%	HDMI_TX1- CONN
HDMI_C_TX2+	@	R73	1	2	0.0402_5%	HDMI_TX2+ CONN
HDMI_C_TX2-	@	R75	1	2	0.0402_5%	HDMI_TX2- CONN

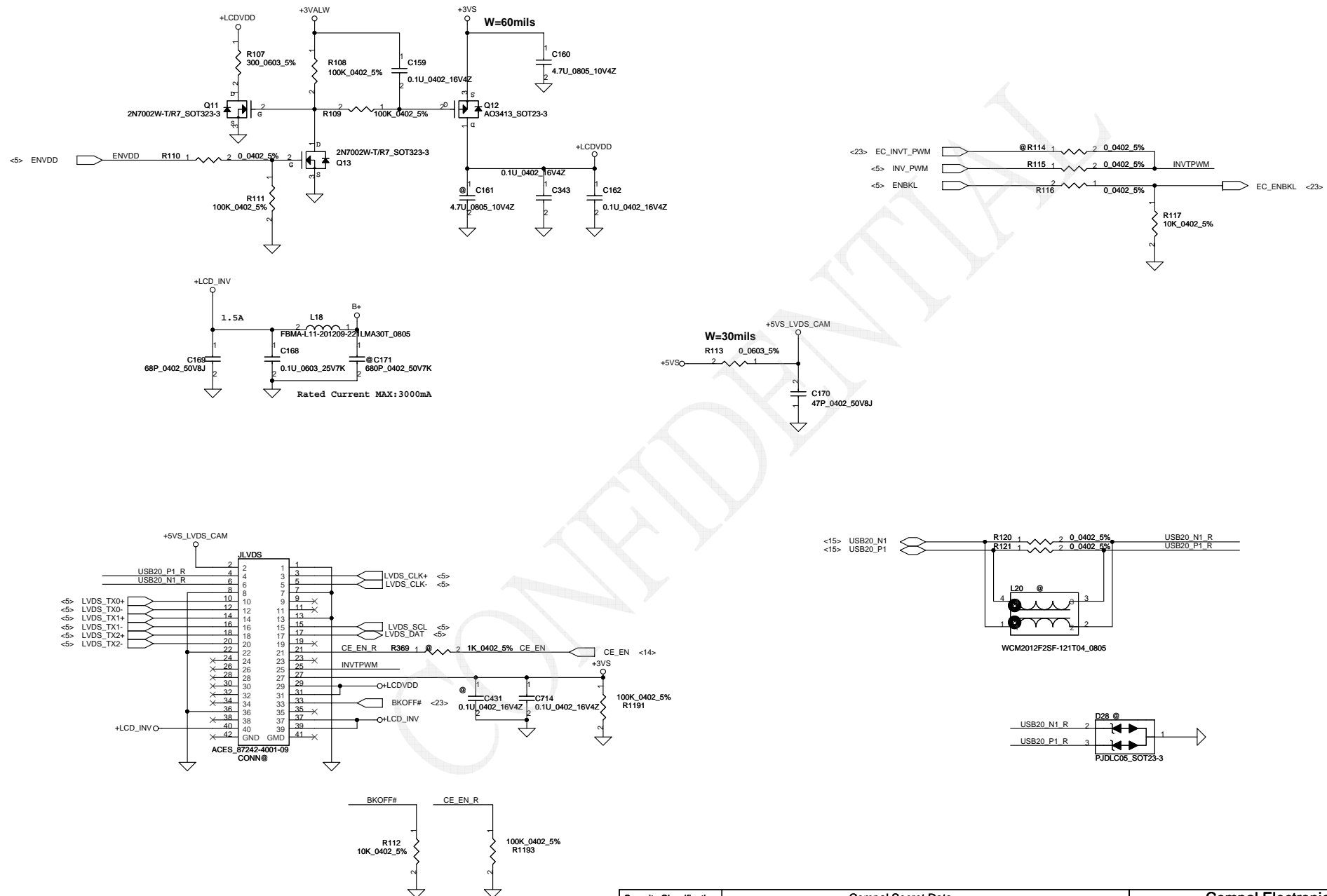


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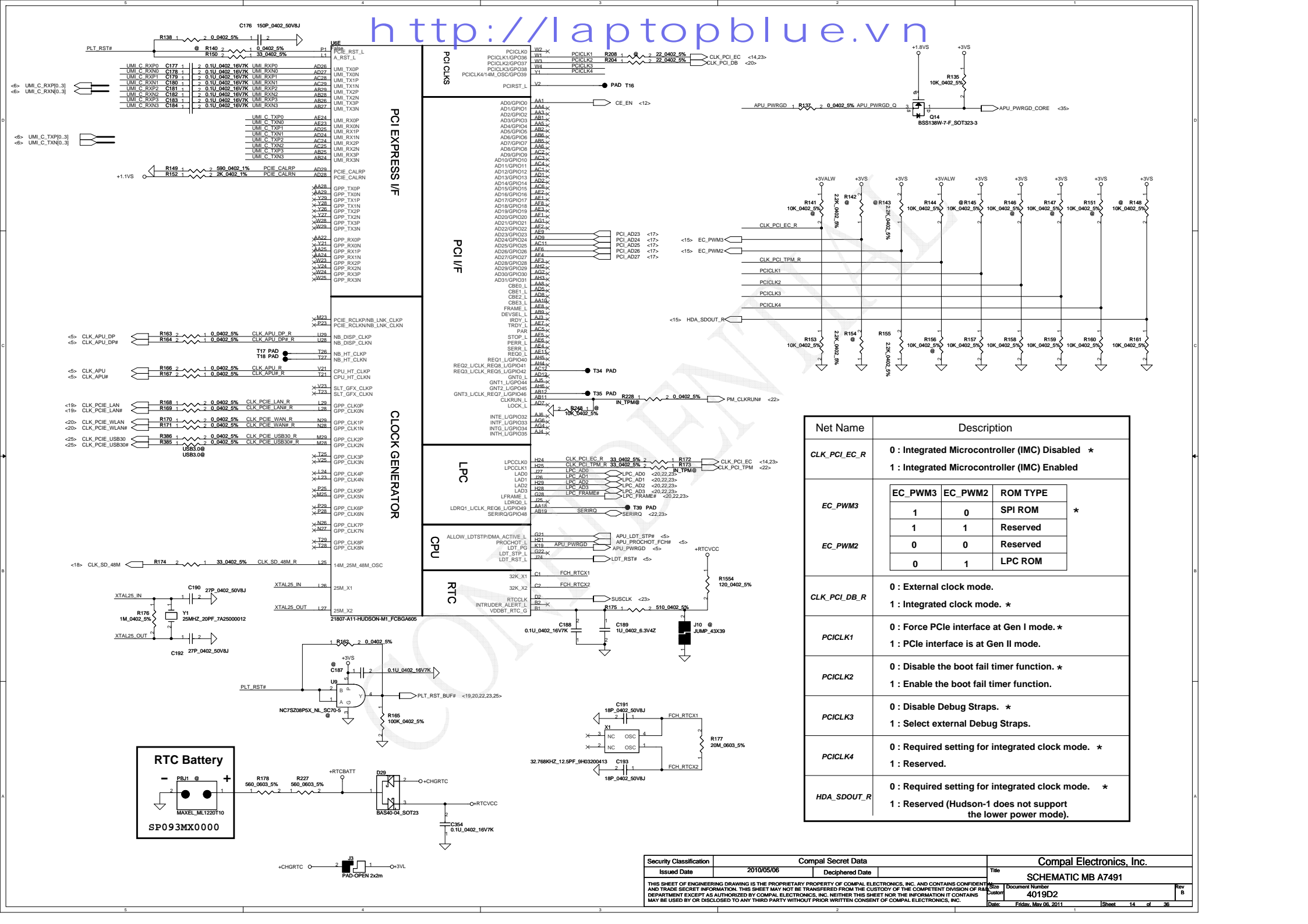


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LCD POWER CIRCUIT



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The schematic diagram illustrates the MB A7491 motherboard layout, featuring various components and their connections. The diagram is organized into several functional blocks:

- PCI Express I/F:** Shows connections for PCI Express lanes, including UMI, TXN, RXN, and TXP.
- PCI I/F:** Details the PCI interface components, including PCI, TXN, RXN, and TXP.
- Clock Generator:** Includes the USB3.0 and USB3.0+ components, along with the USB3.0+ and USB3.0- signals.
- LPC:** Shows the LPC interface components, including LPC, TXN, RXN, and TXP.
- CPU:** Details the CPU interface components, including CPU, TXN, RXN, and TXP.
- RTC:** Shows the RTC interface components, including RTC, TXN, RXN, and TXP.

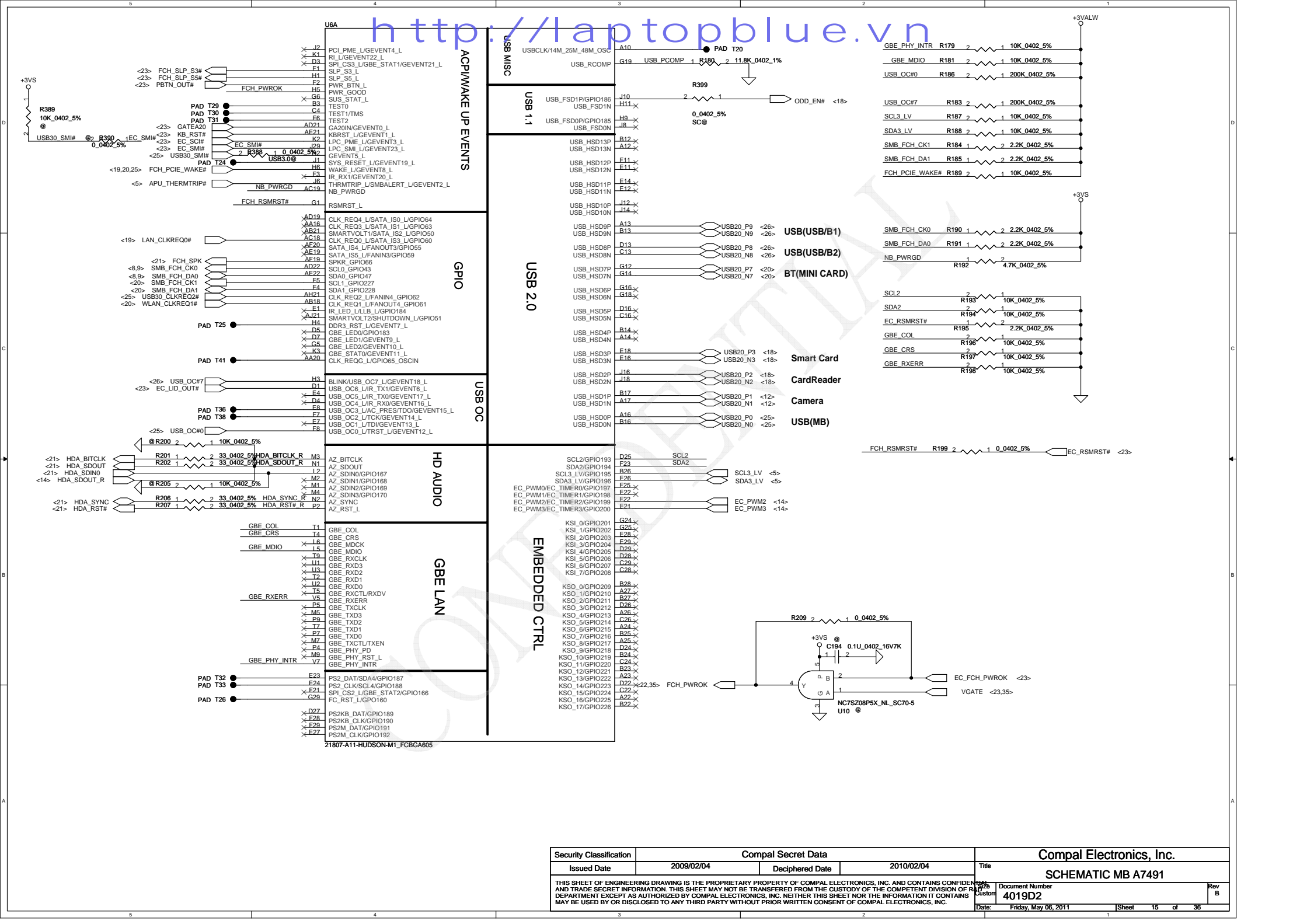
The diagram also includes a table for Net Name and Description, and a table for Security Classification.

Net Name	Description
CLK_PCI_EC_R	0 : Integrated Microcontroller (IMC) Disabled * 1 : Integrated Microcontroller (IMC) Enabled
EC_PWM3	EC_PWM3 EC_PWM2 ROM TYPE
EC_PWM2	0 : Disable the boot fail timer function. * 1 : Enable the boot fail timer function.
CLK_PCI_DB_R	0 : External clock mode. 1 : Integrated clock mode. *
PCICLK1	0 : Force PCIe interface at Gen I mode. * 1 : PCIe interface is at Gen II mode.
PCICLK2	0 : Disable the boot fail timer function. * 1 : Enable the boot fail timer function.
PCICLK3	0 : Disable Debug Straps. * 1 : Select external Debug Straps.
PCICLK4	0 : Required setting for integrated clock mode. * 1 : Reserved.
HDA_SDOUT_R	0 : Required setting for integrated clock mode. * 1 : Reserved (Hudson-1 does not support the lower power mode).

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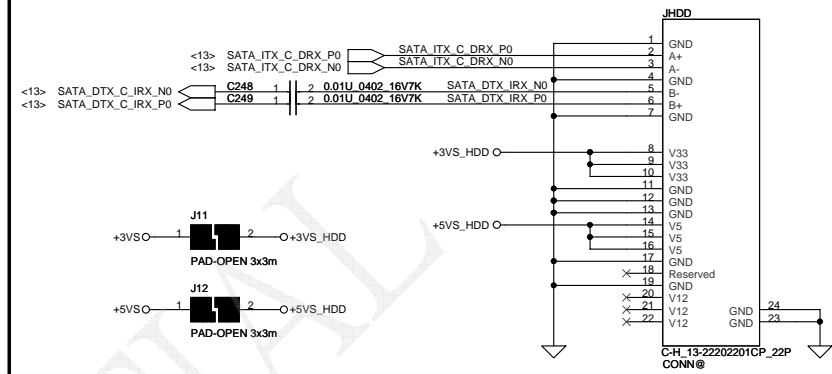
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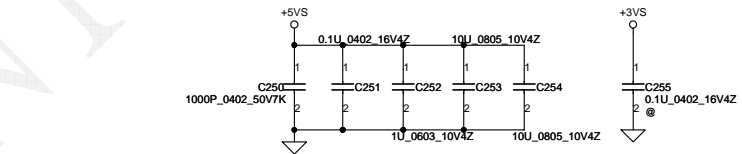


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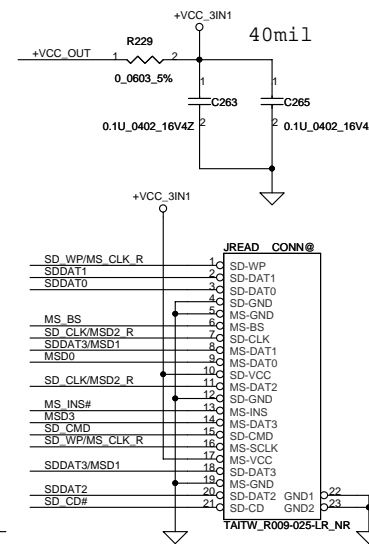
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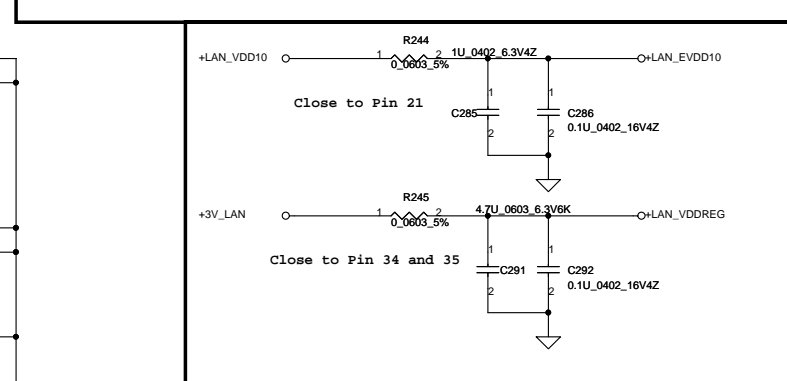
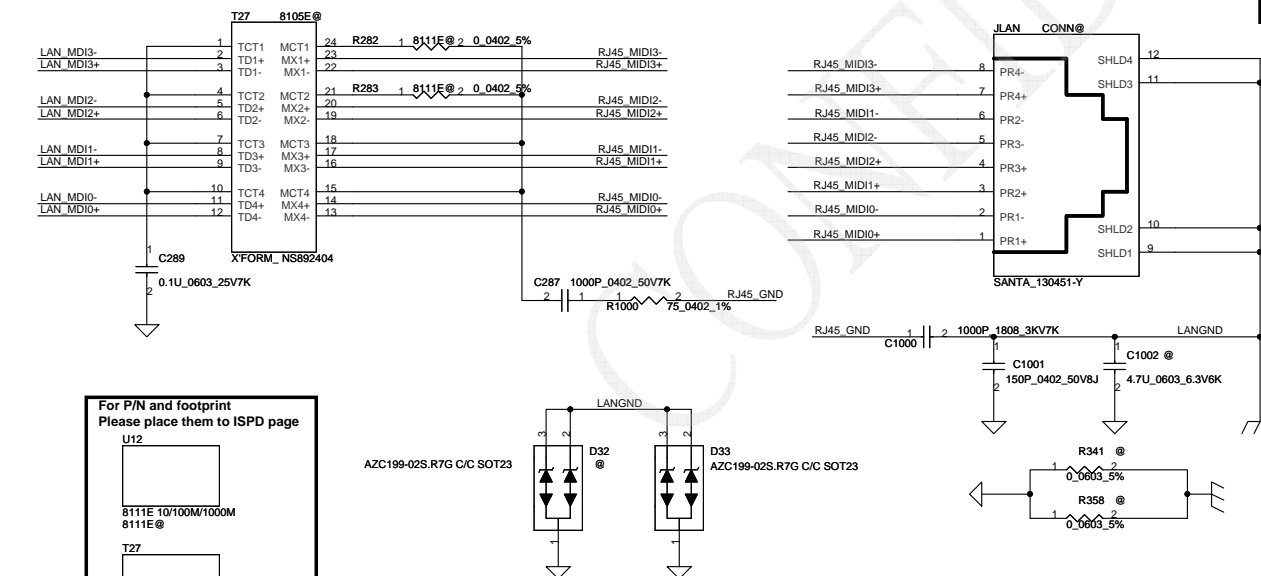
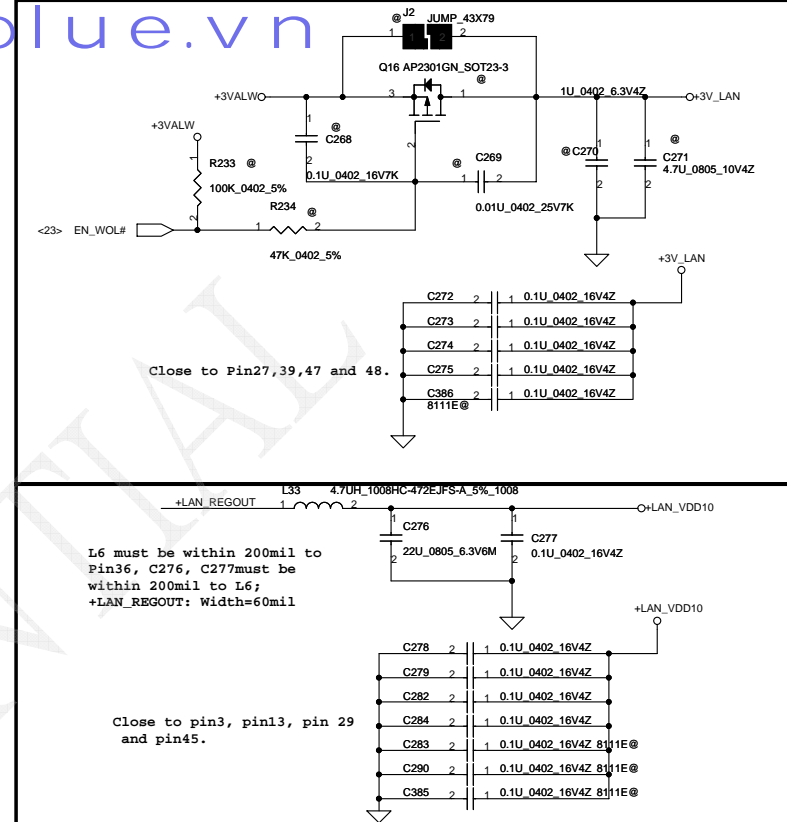
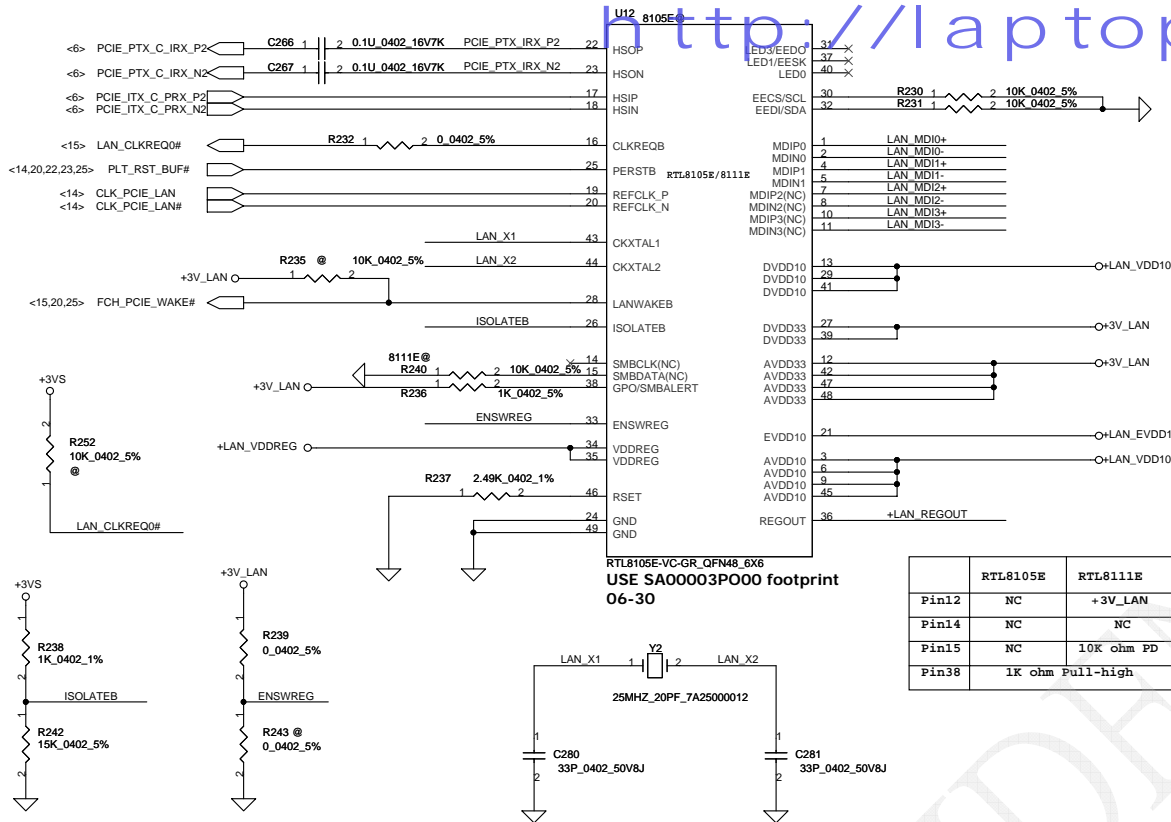
C-H_13-22202201CP_222
CONN@



MDIO	SD Card	MMC Card	MS Card
PIN Name	PIN Name	PIN Name	PIN Name
SP1	SP1		SP1
SP2			
SP3			
SP4			
SP5			
SP6			
SP7			
SP8			
SP9			
SP10			
SP11			
SP12			
SP13			
SP14			
SP15			
SP16			
SP17			
SP18			
SP19			



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For P/N and footprint
Please place them to ISPD page

U12

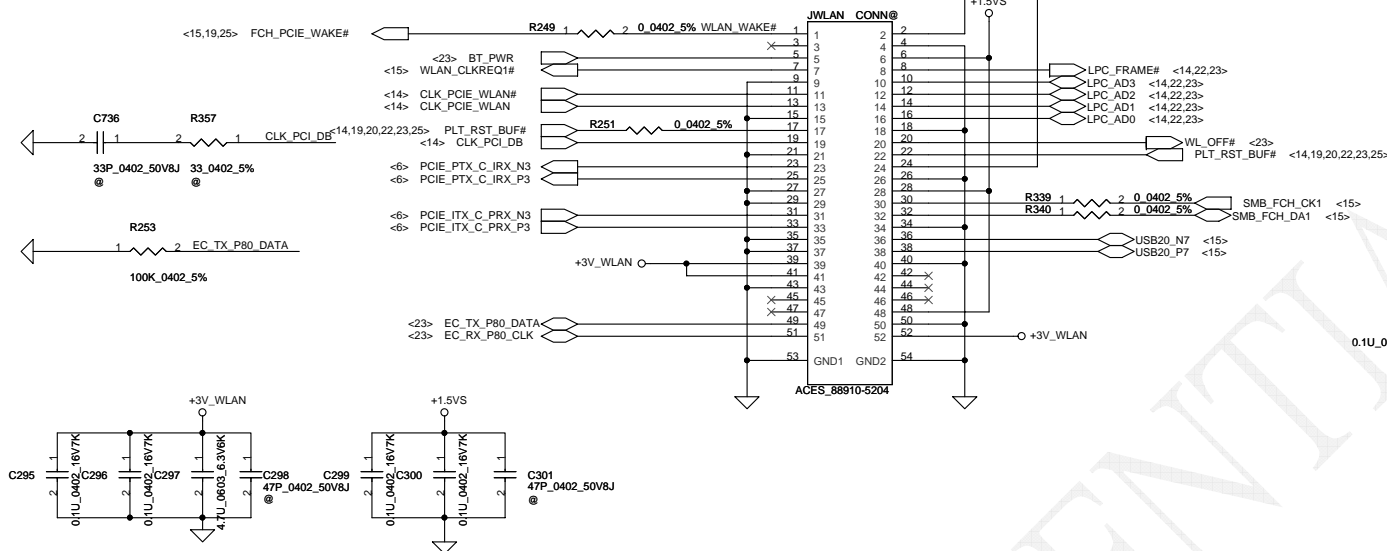
8111E 10/100M/1000M
8111E@

T27

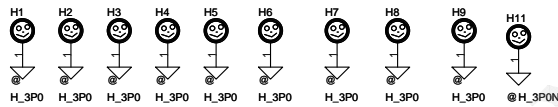
10/100M/1000M transformer
8111E@

WLAN&BT

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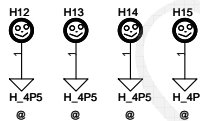
Screw Hole



NPTH



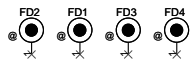
CPU



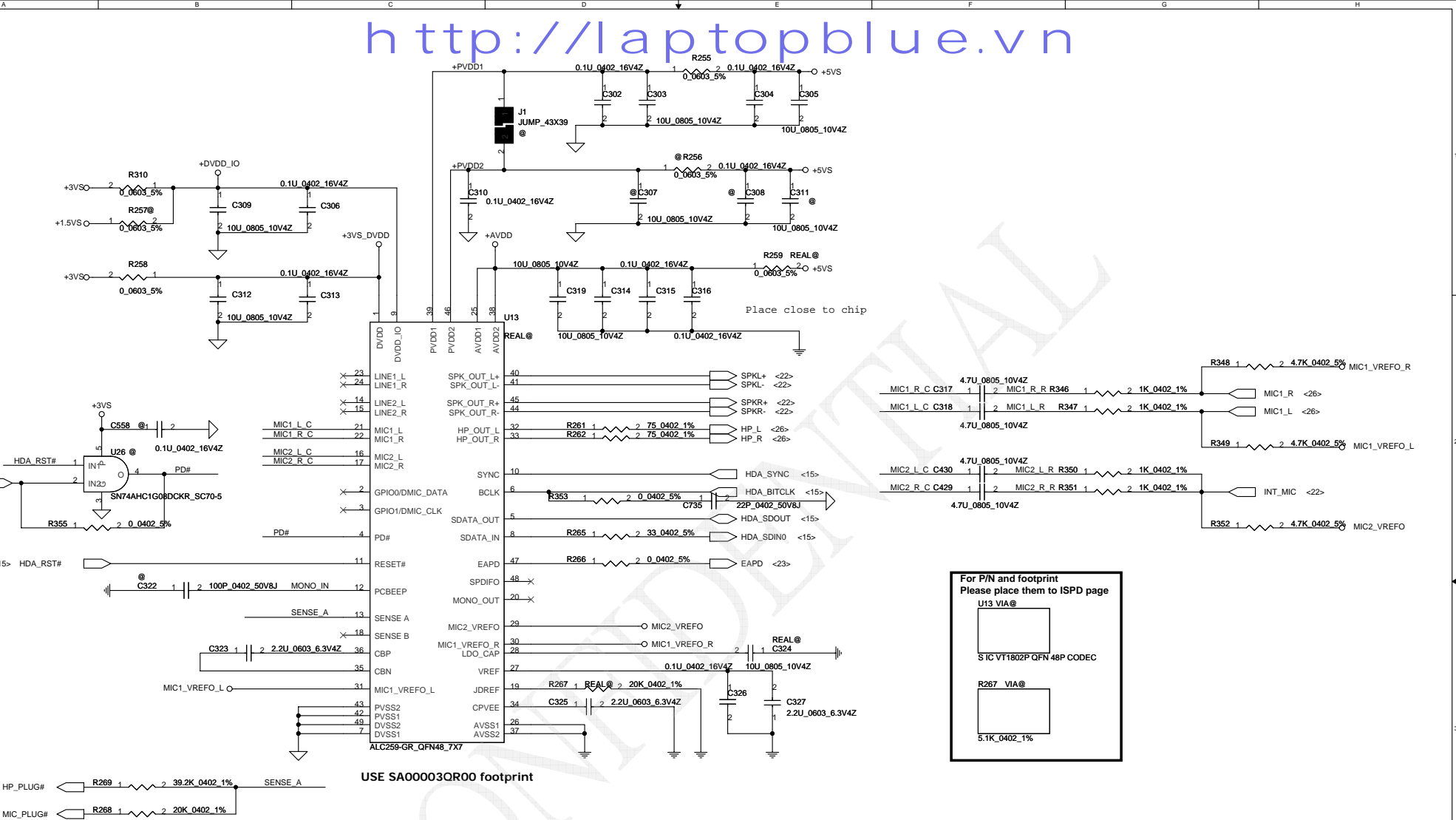
JWLAN



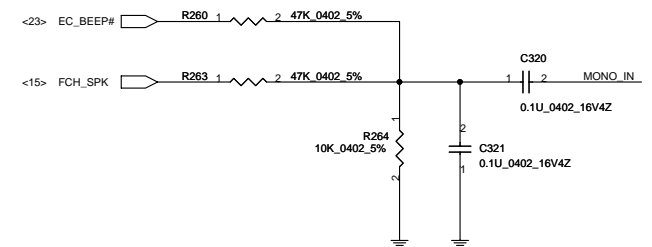
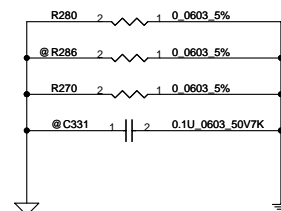
PCB Fedical Mark PAD



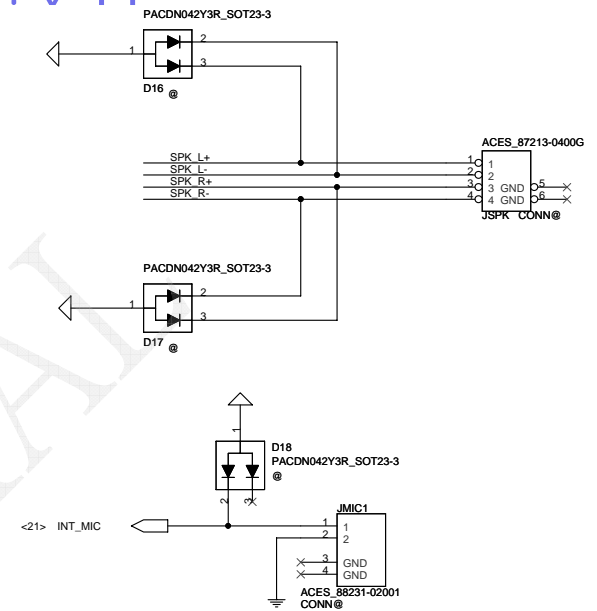
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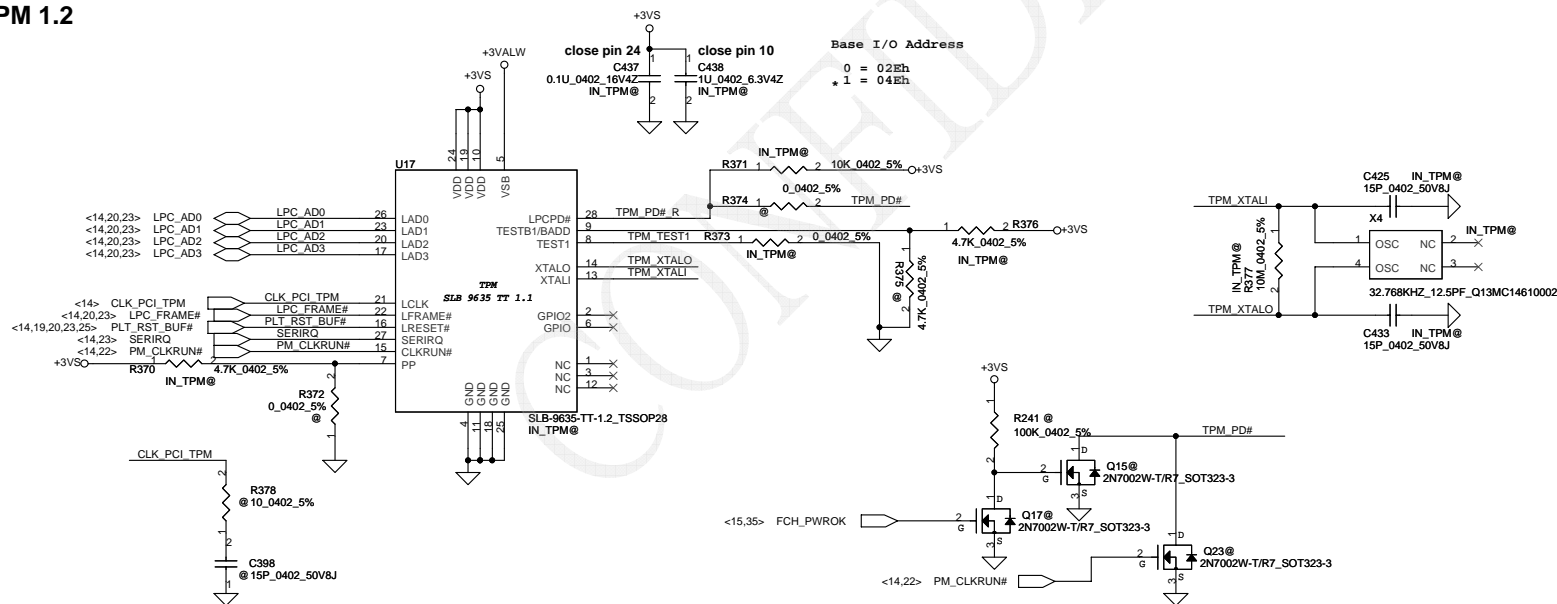
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32,33)	Headphone out
	20K	PORT-I (PIN 21,22)	EXT.MIC
	10K		
	5.1K		
SENSE B	39.2K		
	20K		
	10K		
	5.1K		



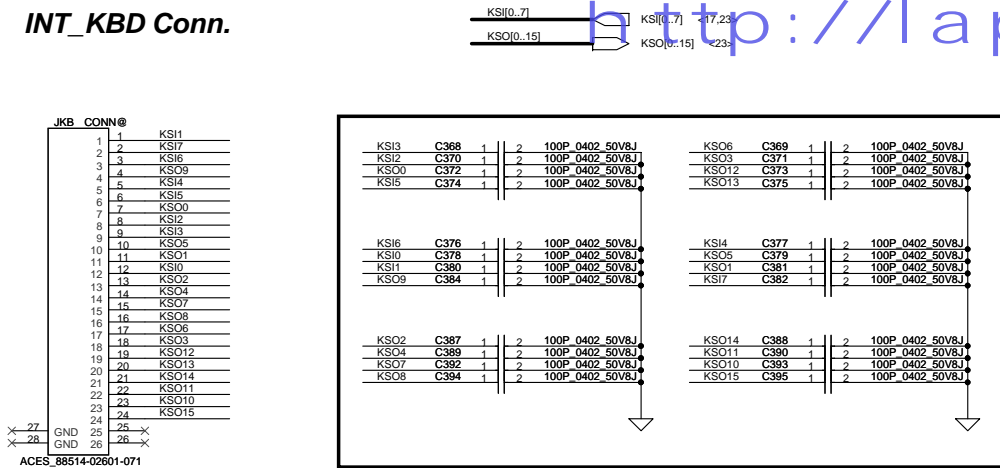
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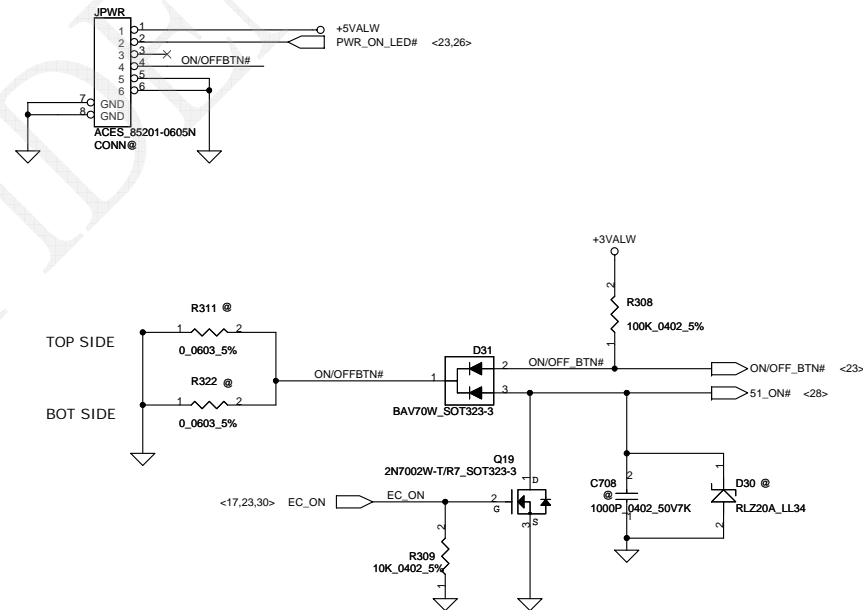
TPM 1.2



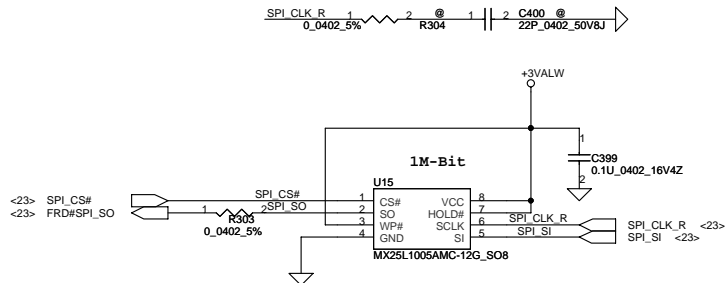
INT_KBD Conn.



Power BTN Board Conn

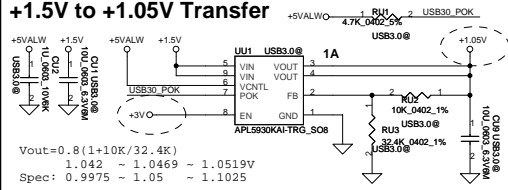


EC ROM

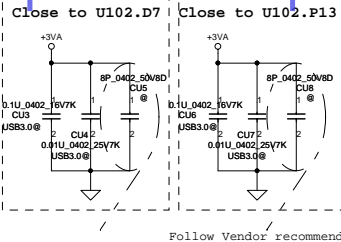
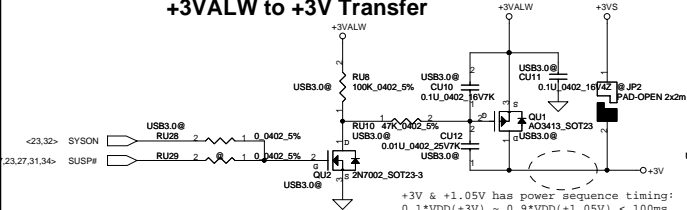


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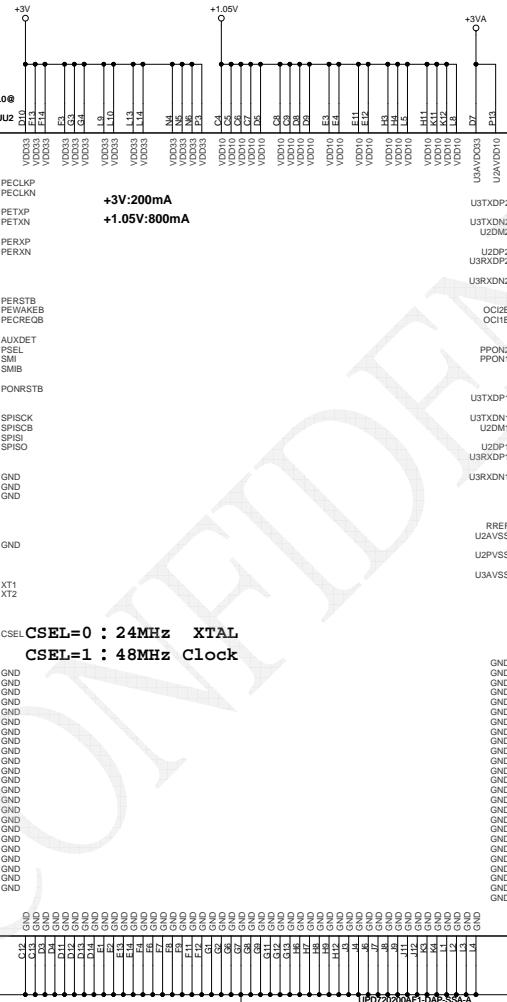
+1.5V to +1.05V Transfer



+3VALW to +3V Transfer

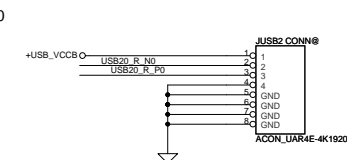
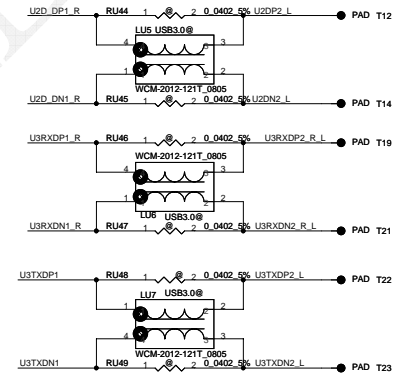
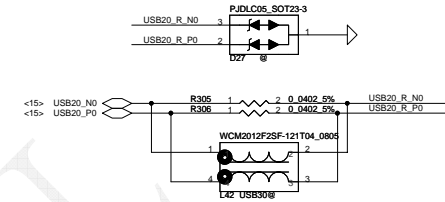
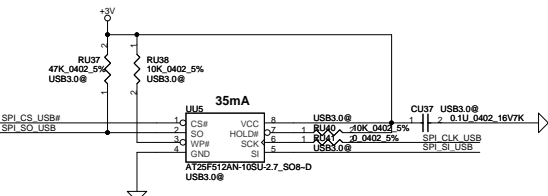


+3V:200mA
 +1.05V:800mA



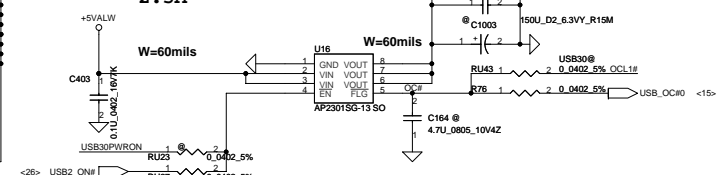
CSEL=0: 24MHz XTAL
 CSEL=1: 48MHz Clock

Place as close as possible to U2.N14 and U2.M14



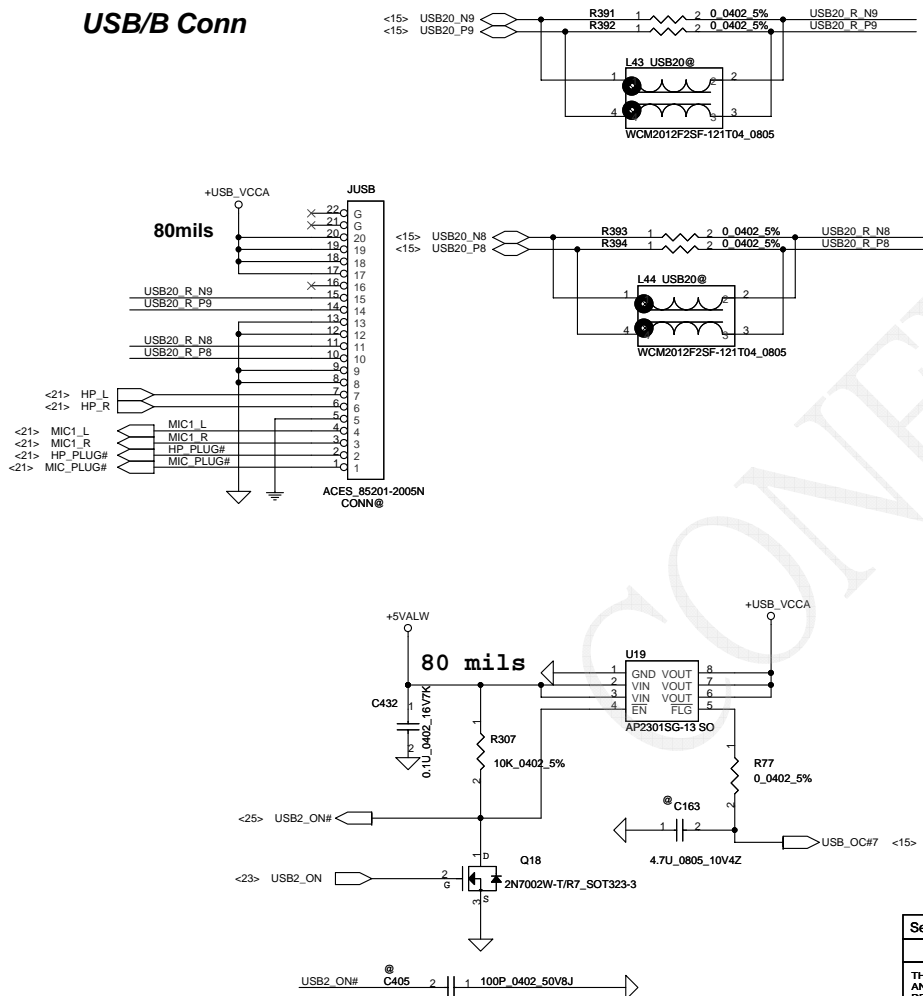
2.5A

W=60mils



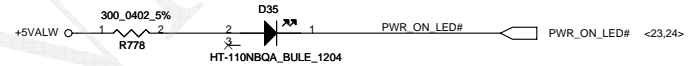
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Issued Date		Deciphered Date		SCHEMATIC MB A7491	
2010/05/27		2011/03/04		4019D2	
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USB/B Conn



LEDs

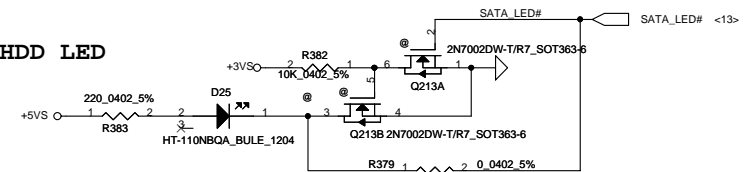
Power on LED



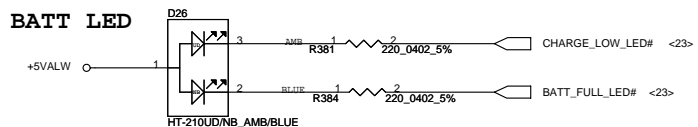
WL&BT LED



HDD LED



BATT LED



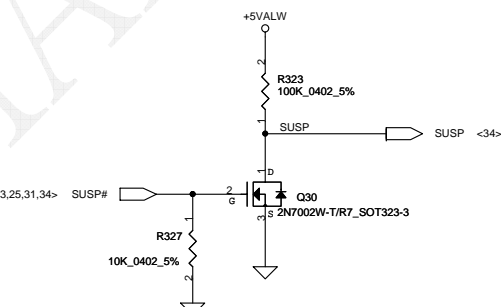
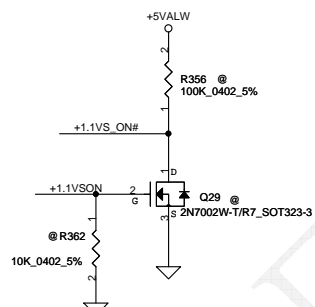
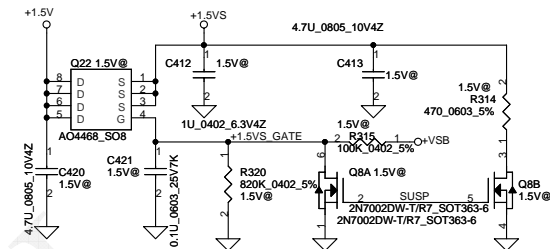
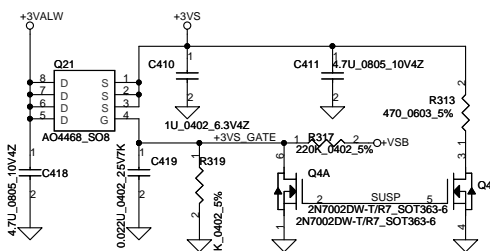
CAP LOCK LED



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http://aptopblue.vn

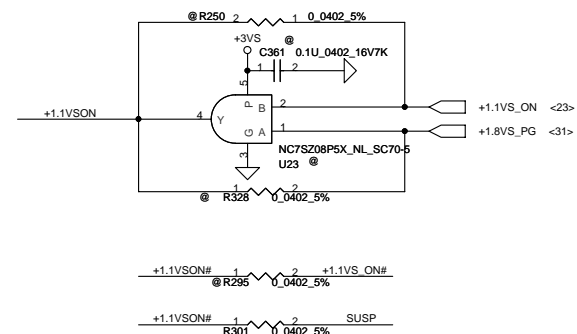
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2N7002W-T/R7_SOT323-3

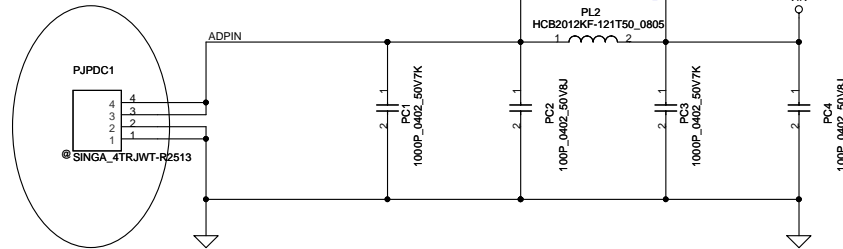
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2N7002W-T/R7_SOT323-3

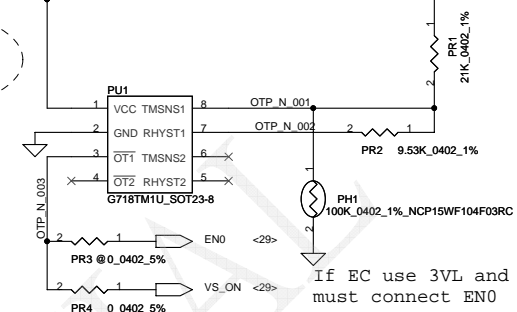
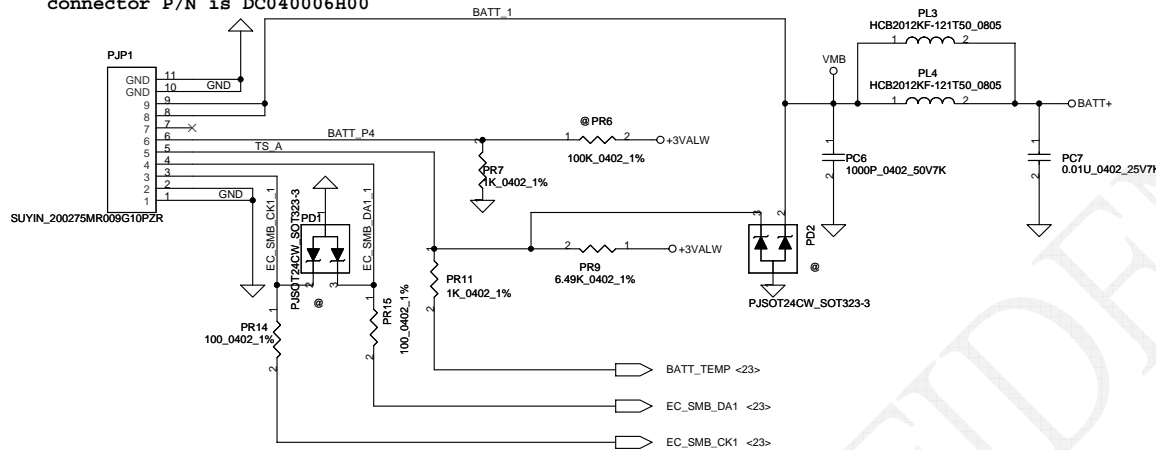


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PH1 under CPU bottom side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C



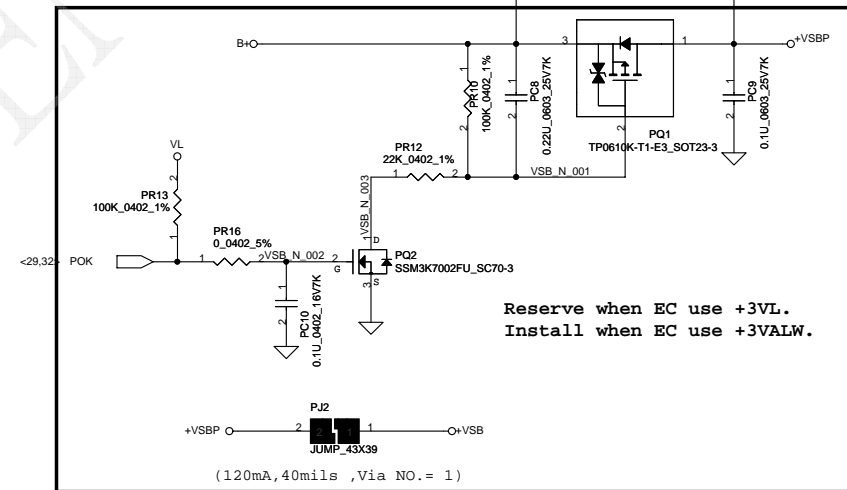
need confirm: ME give us battery
connector P/N is DC040006H00



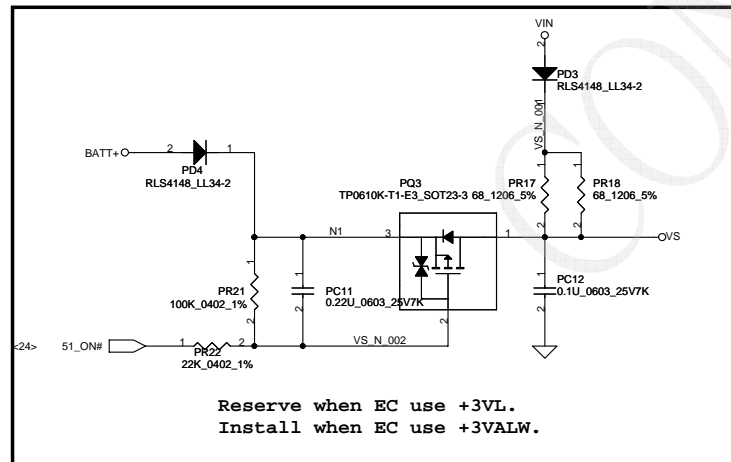
If EC use 3VL and can not detect VGATE,
must connect ENO

Install when EC use +3VL
and SUSP was Pull high to +3VL.

Reserve when EC use +3VALW.

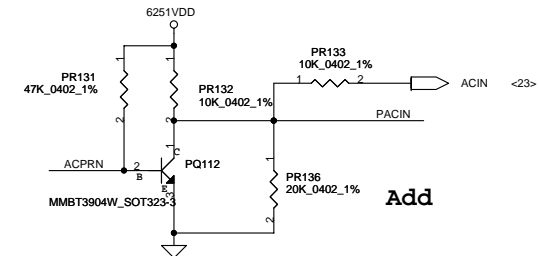


Reserve when EC use +3VL.
Install when EC use +3VALW.



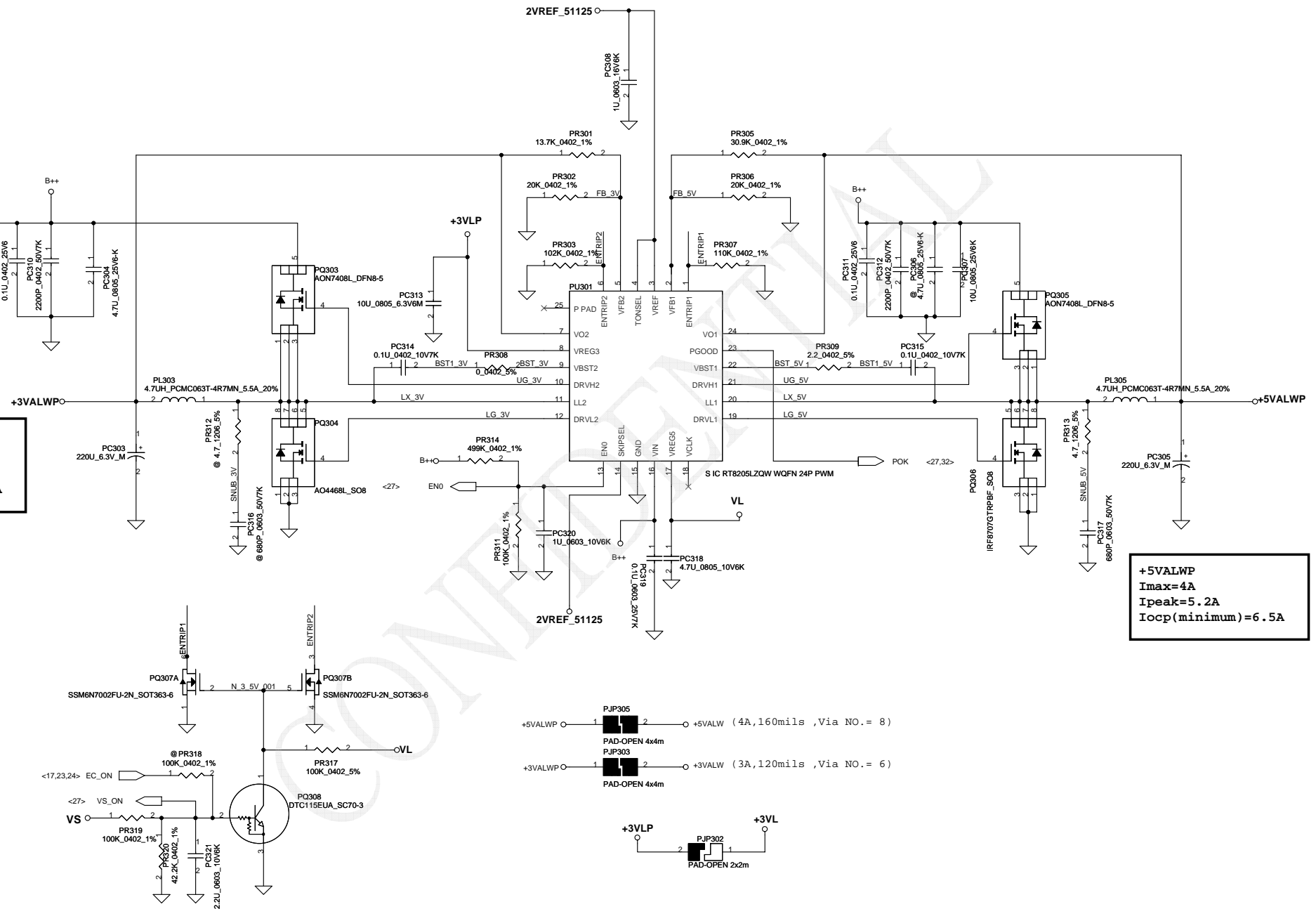
Reserve when EC use +3VL.
Install when EC use +3VALW.

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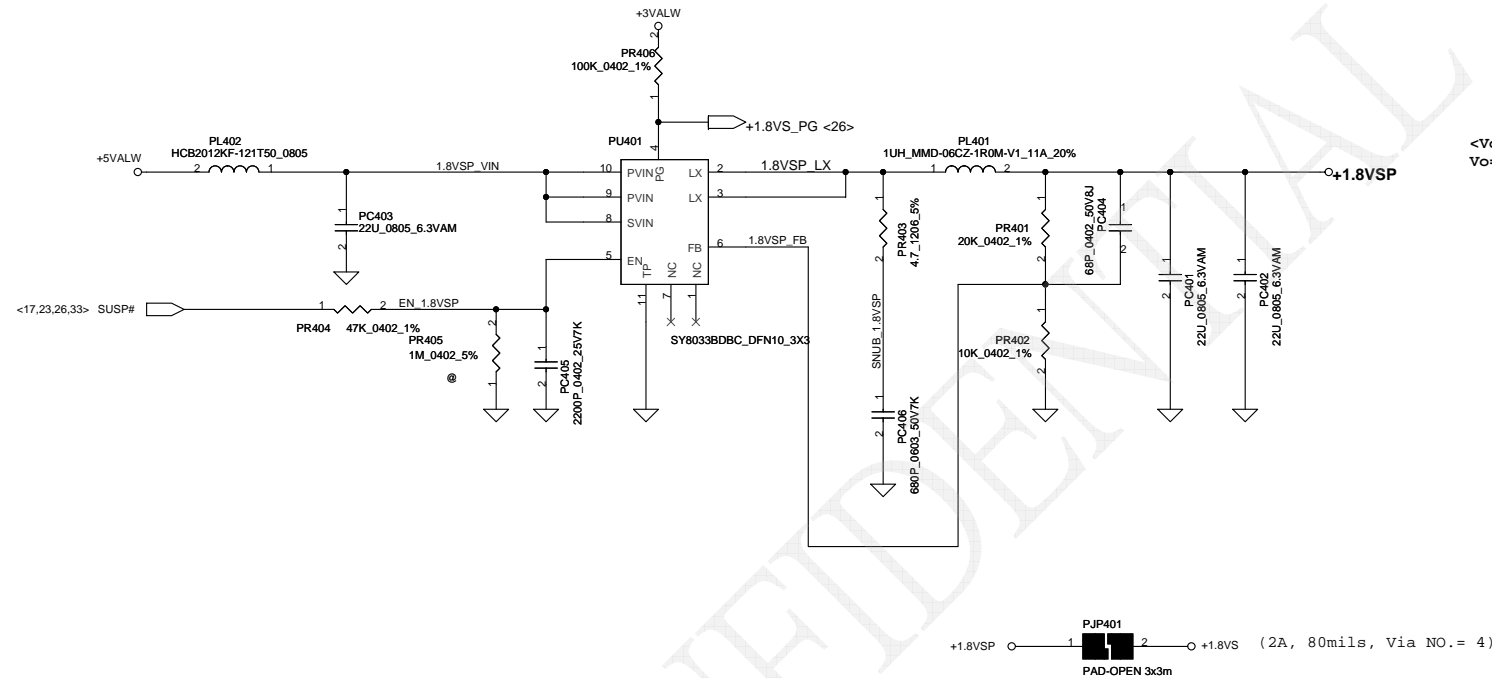


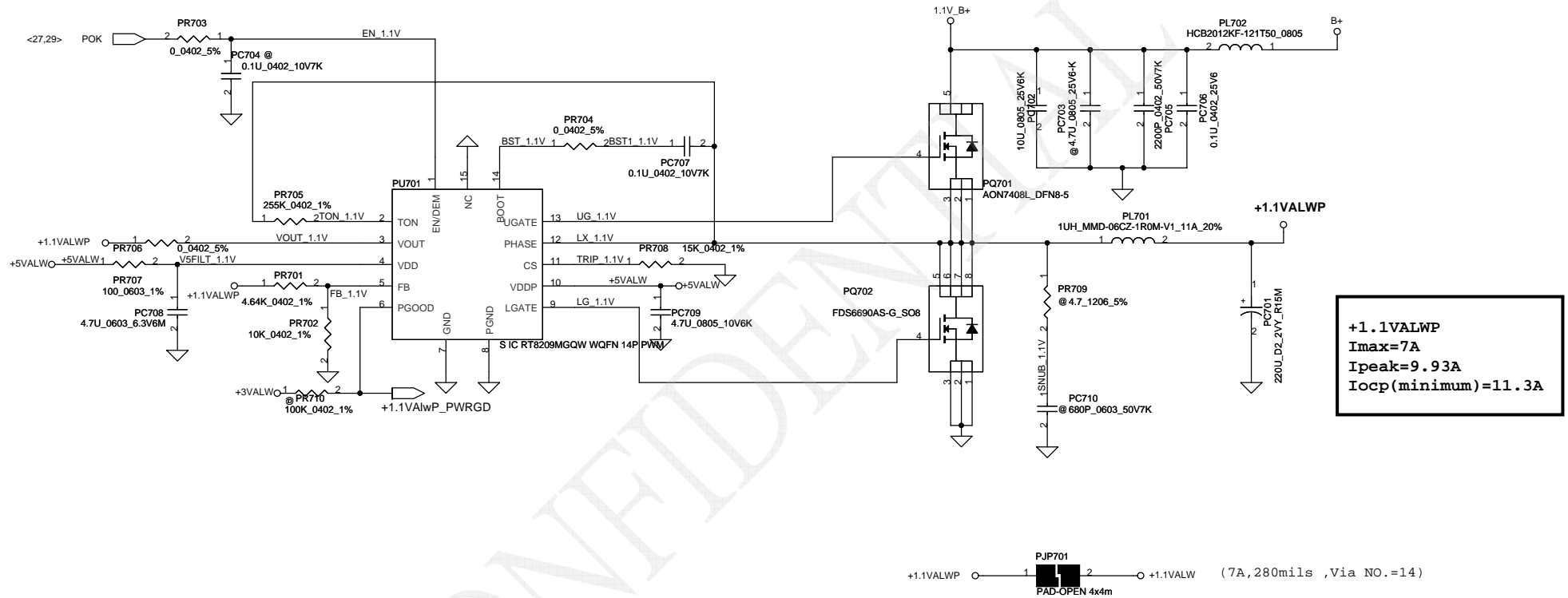
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```
EC:+3VL, reserve PR319, install PR318, PR320 100K
EC:+3VALW, reserve PR318, install PR319, PR320 40.2K
```

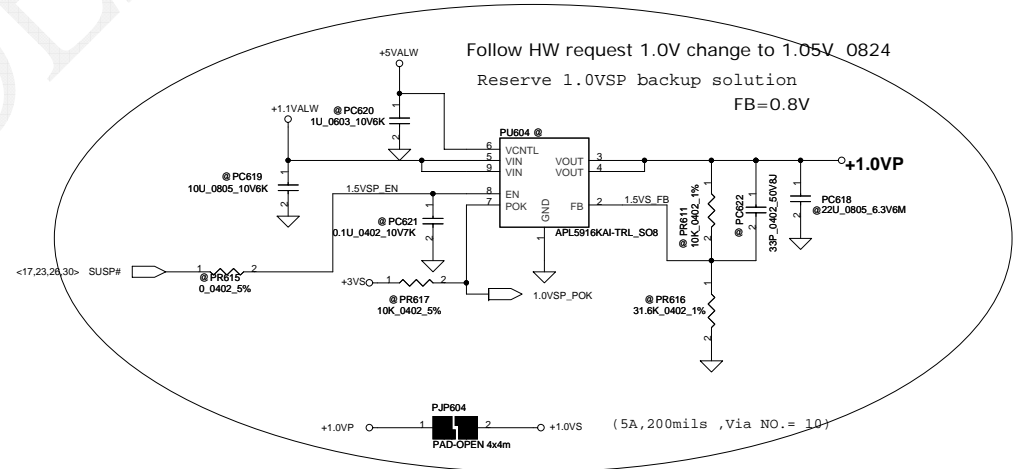
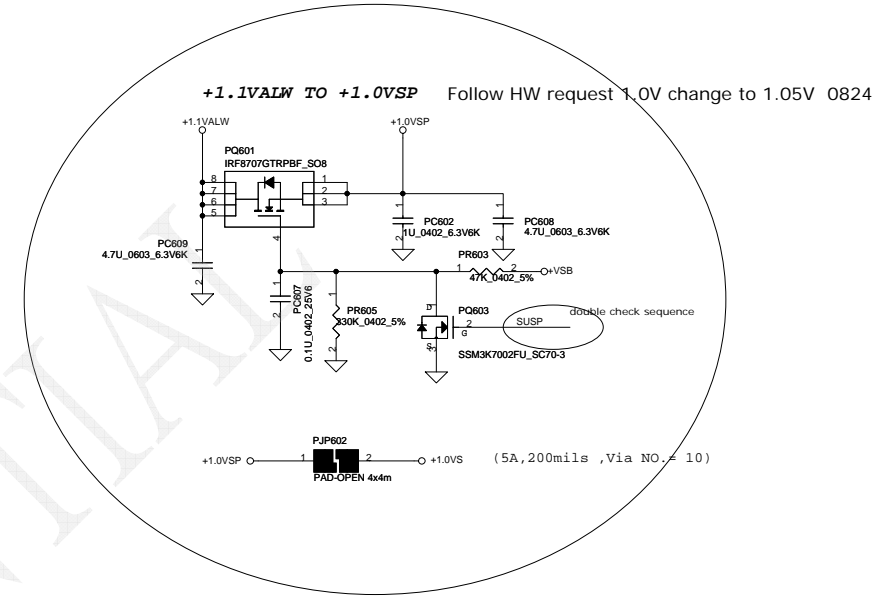
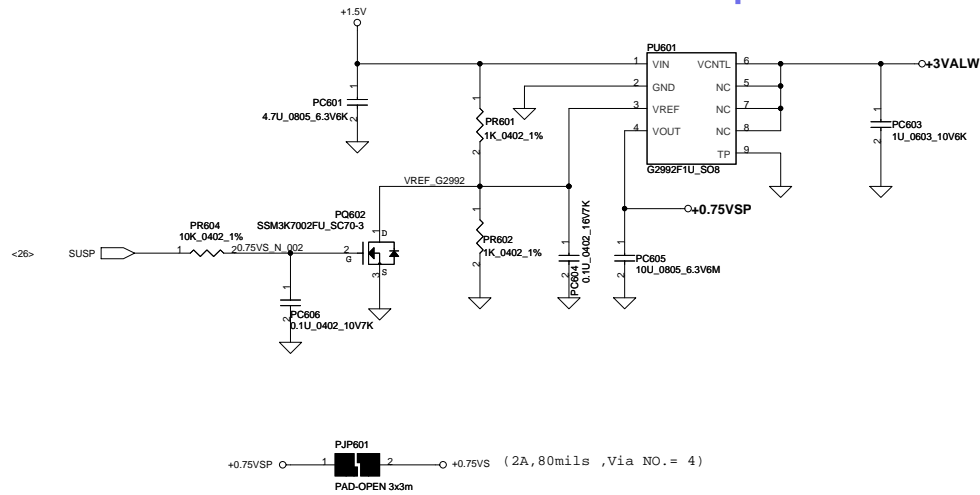


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Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Reason for change	Description	phase	modify	Rev.
1	31	Follow EMI request to add PR54, PR59, PC511 for EMI issue.	add PR54, PR59, PC511	PVT	add PR54, PR59, PC511	
2	34	Follow ME request change PQ205 for height issue	Change PQ205 from AO4726L AON6788	PVT	Change PQ205 from AO4726L AON6788	
3	28	For common desgin	Delete PC107	Pre-MP	Remove PC107	
4	28	For common desgin	PR110 from 47K change to 200K	Pre-MP	PR110 from 47K change to 200K	
5	28	For common desgin	PR112 from 10K change to 47K	Pre-MP	PR110 from 10K change to 47K	
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