

JSKAA

Irving 10/10G

LA4161P REV 1.0 Schematic

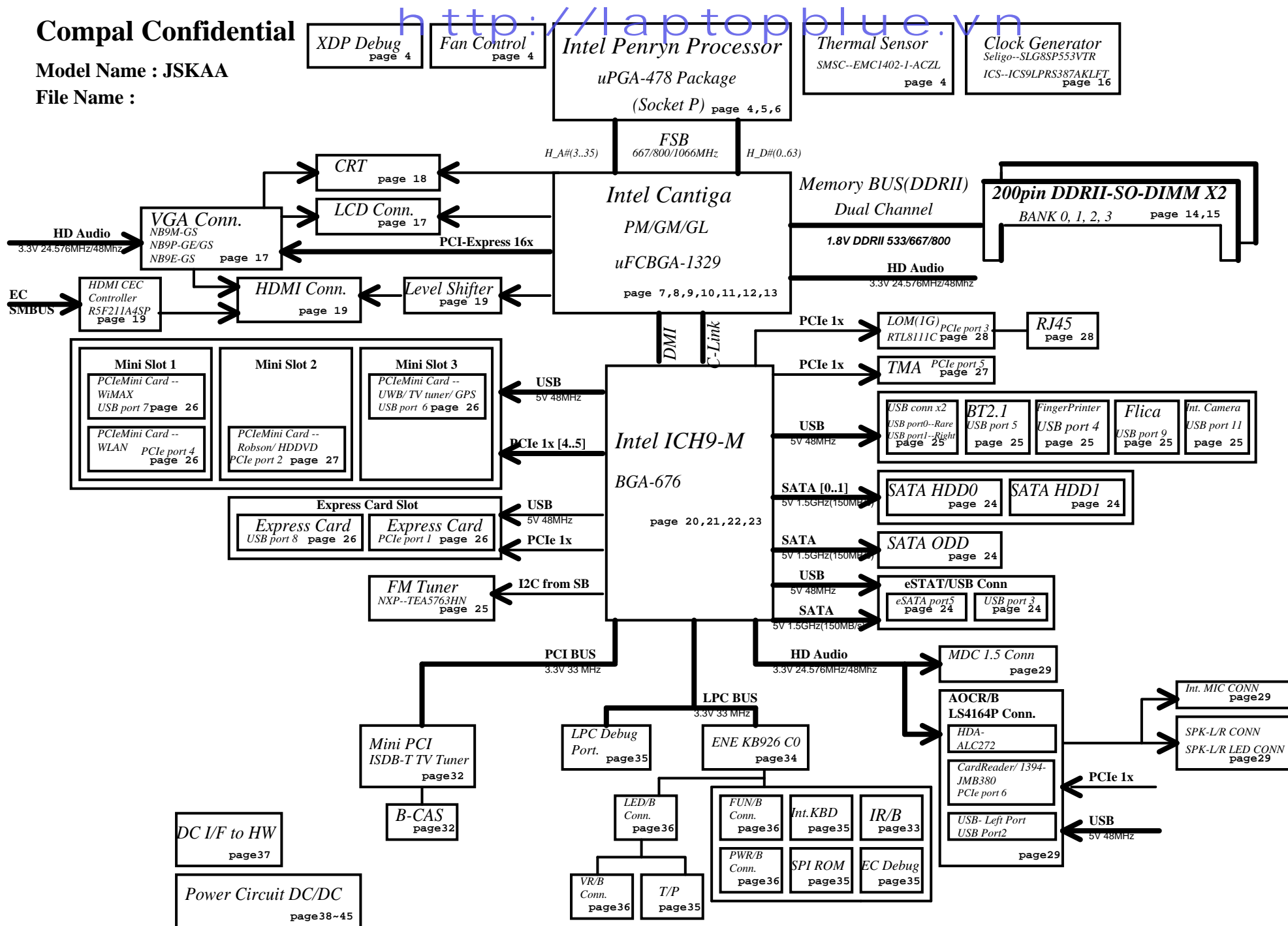
Intel Penryn/ Cantiga (GL45/GM45/PM45)/ ICH9M
2008-10-01 Rev. 1.0

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Compal Confidential

Model Name : JSKAA

File Name :



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Voltage Rails

| Power Plane | Description | S1 | S3 | S5 | G3 |
|-------------|---|----|-----|-----|-----|
| VIN | Adapter power supply (19V) | ON | ON | ON | OFF |
| B+ | AC or battery power rail for power circuit. | ON | ON | ON | ON |
| +CPU_CORE | Core voltage for CPU | ON | OFF | OFF | OFF |
| +0.9V | 0.9V switched power rail for DDR terminator | ON | OFF | OFF | OFF |
| +1.05VS | 1.05V switched power rail | ON | OFF | OFF | OFF |
| +1.5VS | 1.5V switched power rail | ON | OFF | OFF | OFF |
| +1.8V | 1.8V power rail for DDR | ON | ON | OFF | OFF |
| | | | | | |
| +3VALW | 3.3V always on power rail | ON | ON | ON | OFF |
| +3VL | 3.3V always on power rail | ON | ON | ON | ON |
| +3V_SB | 3.3V power rail for LAN | ON | ON | OFF | OFF |
| +3V_LAN | 3.3V power rail for LAN | ON | ON | OFF | OFF |
| +3V_WLAN | 3.3V power rail for LAN | ON | ON | OFF | OFF |
| +3VS | 3.3V switched power rail | ON | OFF | OFF | OFF |
| +5VALW | 5V always on power rail | ON | ON | ON | OFF |
| +5VL | 5V always on power rail | ON | ON | ON | ON |
| +5V_SB | 5V power rail for SB | ON | ON | OFF | OFF |
| +5VS | 5V switched power rail | ON | OFF | OFF | OFF |
| +VSB | VSB always on power rail | ON | ON | ON | OFF |
| +RTCVCC | RTC power | ON | ON | ON | ON |

External PCI Devices

| Device | IDSEL# | REQ#/GNT# | Interrupts |
|--------------|-------------------------------|-----------------------------|---------------------------------|
| PCI TV Tuner | AD18 (Master) AD19 (Slave) | 1/1 (Master) 2/2 (Slave) | PIRQG (Master) PIRQH (Slave) |

EC SM Bus1 address

| Power | Device | Address | Power | Device | Address |
|-------|--------------------|-------------|-------|---------------------|-------------|
| +5VL | EC K8926 C0 | | +3VS | EC K8926 C0 | |
| +5VL | Smart Battery | 0001 01X b | +3VS | CPU THM Sen. SMC | |
| +5VL | HDMI-CEC | 0011 010x b | +3VS | EMC1402-1-ACZL-TR | 1001 100x b |
| +5VL | FUN/B (CAP Sensor) | | +3VS | VGA THM Sen. nVidia | 1001 1110 b |
| | | | | | |
| | | | | | |

ICH9M SM Bus address

| Power | Device | Address |
|--------|-----------------------------|--------------|
| +3V_SB | ICH9M | |
| | Clock Generator (SLG8SP56V) | 1101 001Xb |
| +3VS | DDR DIMM0 | 1001 000Xb |
| +3VS | DDR DIMM1 | 1001 010Xb |
| +3VS | Express | |
| +3VS | FM Module | Vertical I2C |

| STATE | SIGNAL | SLP_S1# | SLP_S3# | SLP_S4# | SLP_S5# |
|----------------------|--------|---------|---------|---------|---------|
| Full ON | | HIGH | HIGH | HIGH | HIGH |
| S1(Power On Suspend) | | LOW | HIGH | HIGH | HIGH |
| S3 (Suspend to RAM) | | LOW | LOW | HIGH | HIGH |
| S4 (Suspend to Disk) | | LOW | LOW | LOW | HIGH |
| S5 (Soft OFF) | | LOW | LOW | LOW | LOW |
| G3 | | LOW | LOW | LOW | LOW |

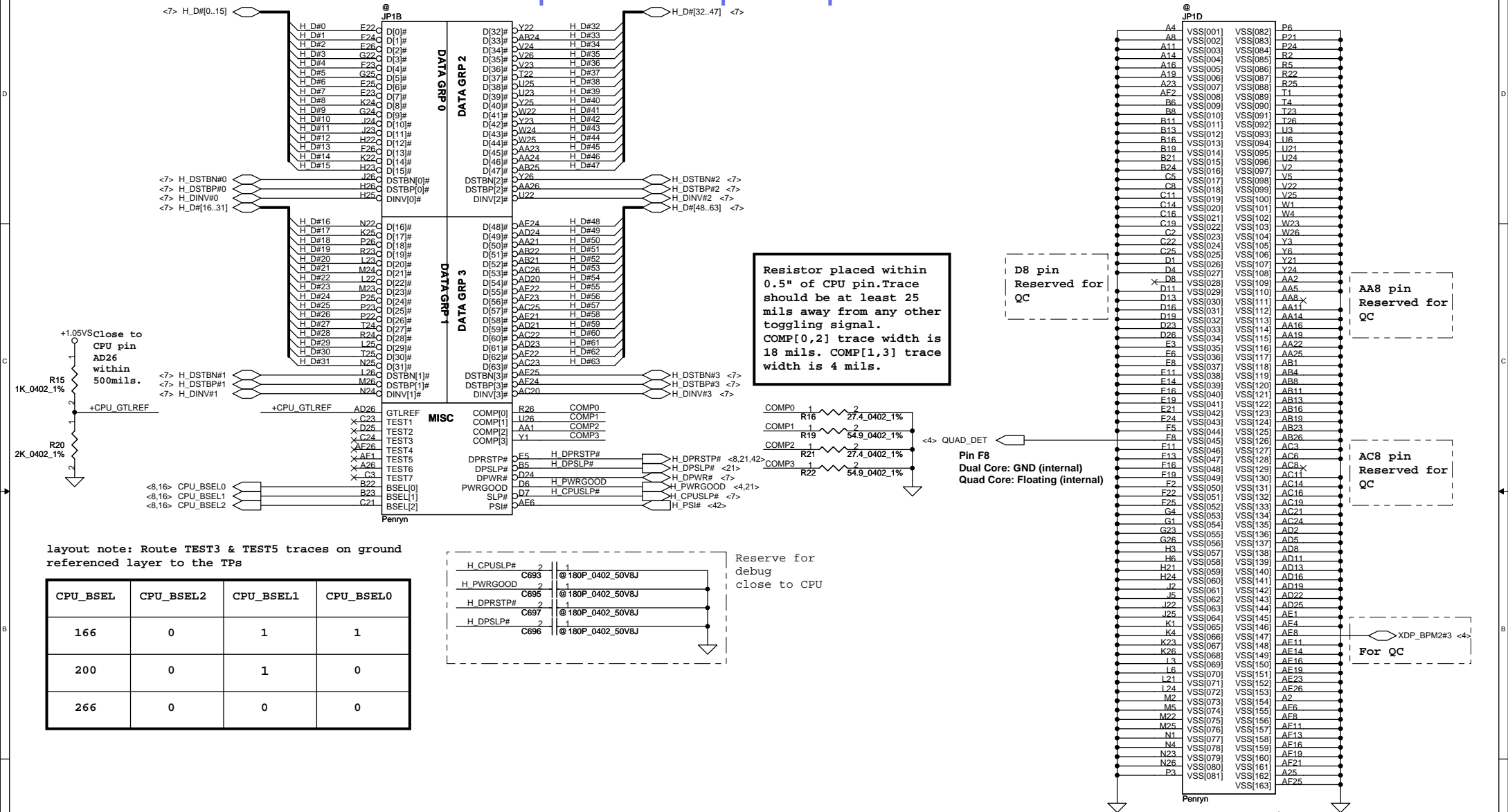
Reserve for AD channel define.

| | | | | |
|----------|--------------|-------------|-------------|-------------|
| Vcc | 3.3V +/- 5% | | | |
| Ra/Rc/Re | 100K +/- 5% | | | |
| Board ID | Rb / Rd / Rf | VAD_BID min | VAD_BID typ | VAD_BID max |
| 0 | 0 | 0 V | 0 V | 0 V |
| 1 | 8.2K +/- 5% | 0.216 V | 0.250 V | 0.289 V |
| 2 | 18K +/- 5% | 0.436 V | 0.503 V | 0.538 V |
| 3 | 33K +/- 5% | 0.712 V | 0.819 V | 0.875 V |
| 4 | 56K +/- 5% | 1.036 V | 1.185 V | 1.264 V |
| 5 | 100K +/- 5% | 1.453 V | 1.650 V | 1.759 V |
| 6 | 200K +/- 5% | 1.935 V | 2.200 V | 2.341 V |
| 7 | NC | 2.500 V | 3.300 V | 3.300 V |

BTO Option Table

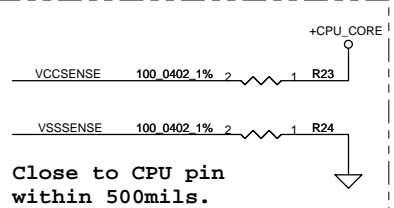
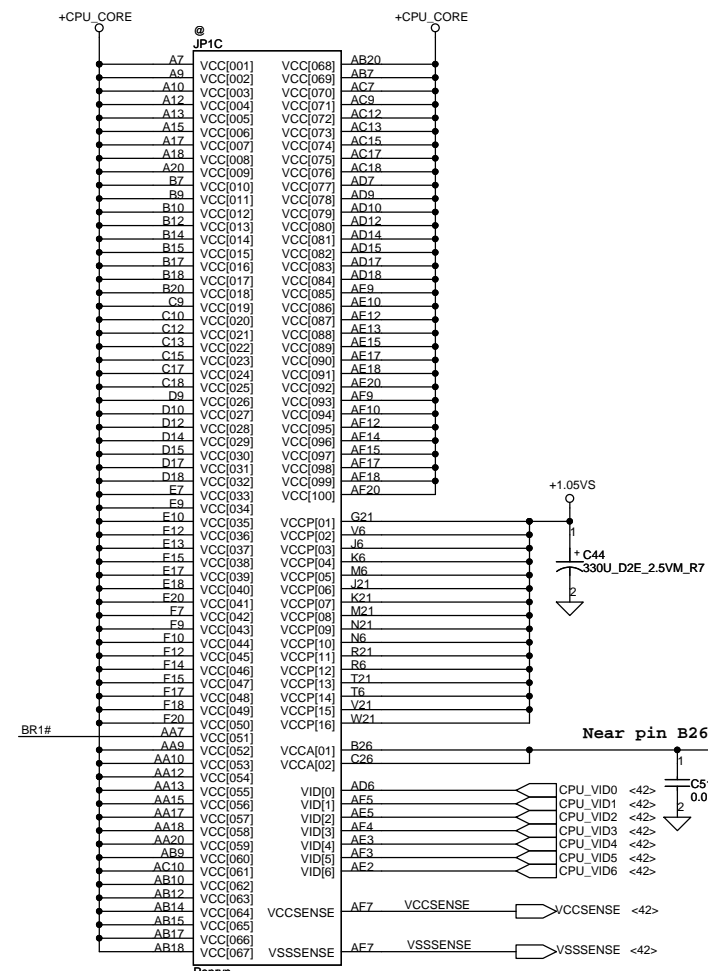
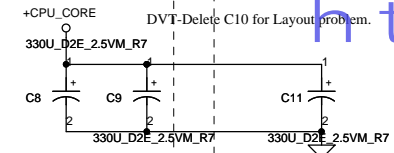
| BTO Item | BOM Structure |
|----------|---------------|
| | |
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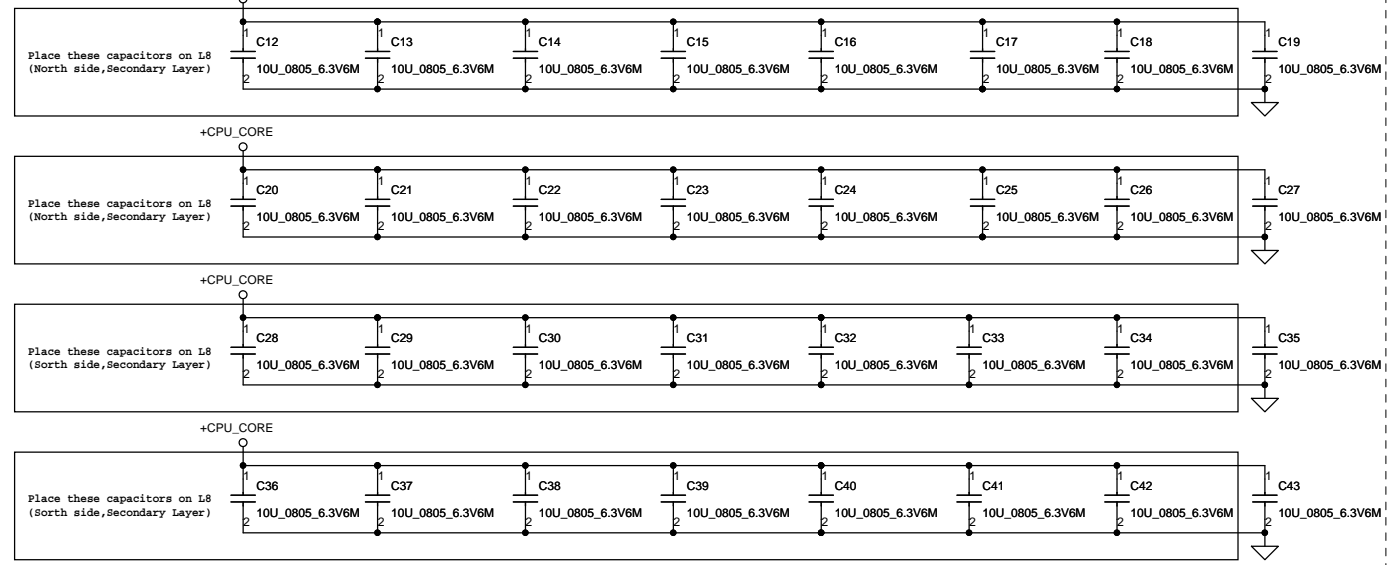
Near CPU CORE regulator

ESR <= 1.5m ohm
Capacitor > 1980uF

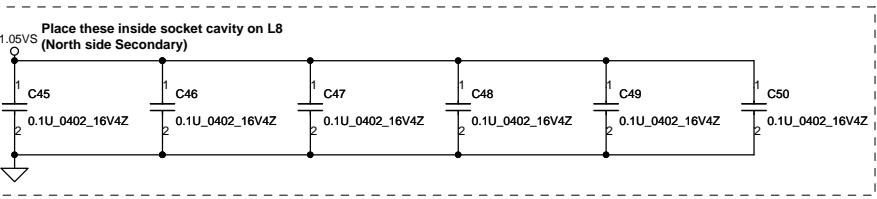


Length match within 25 mils.
The trace width/space/other is
20/7/25.

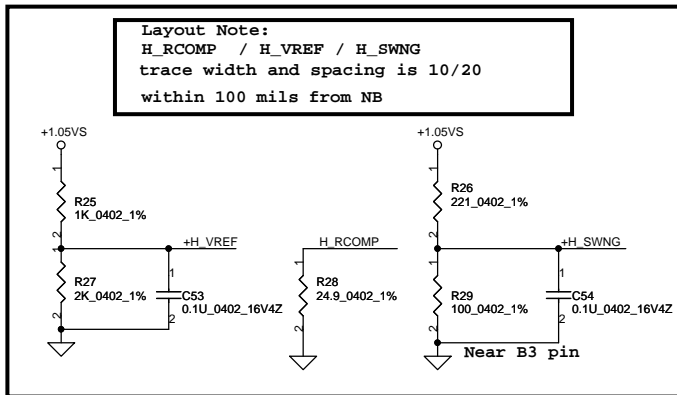
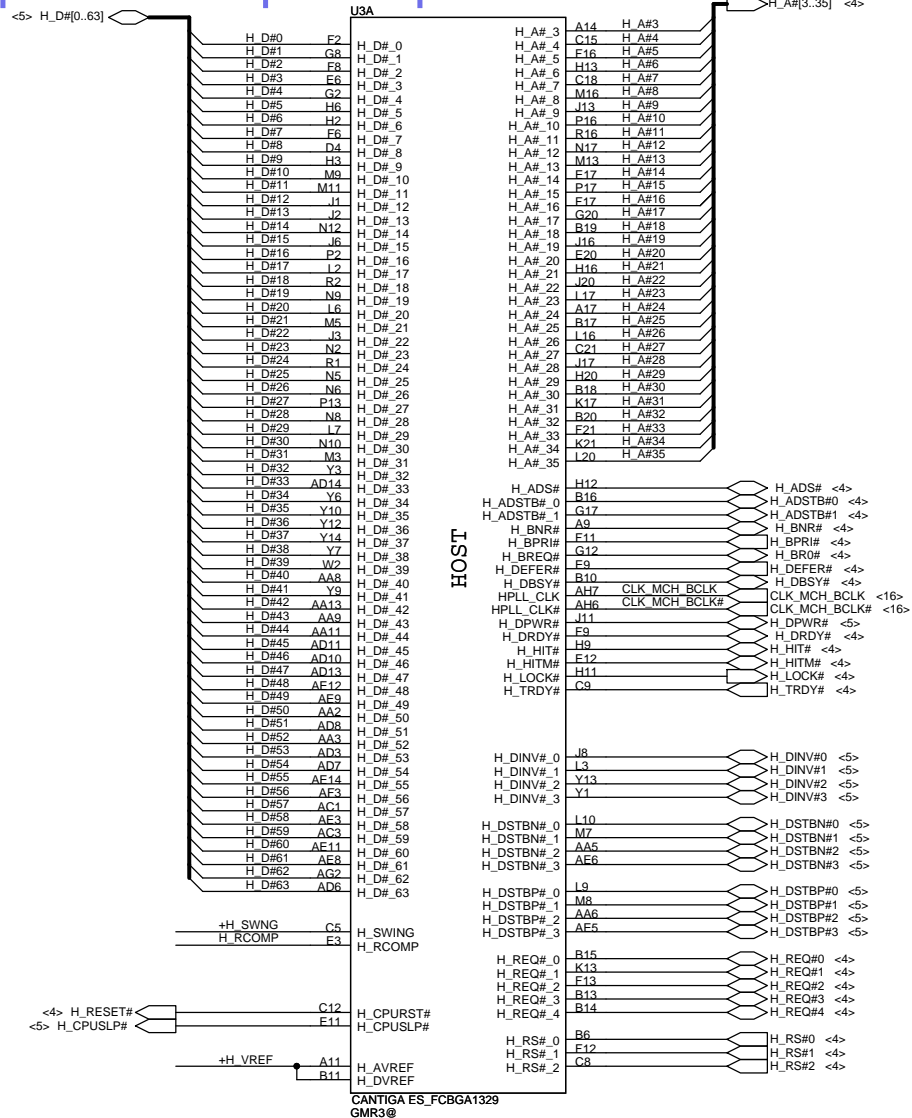
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Mid Frequence Decoupling

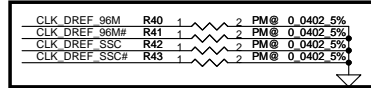
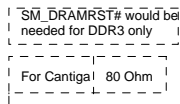
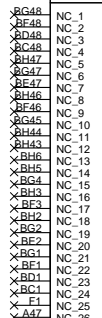
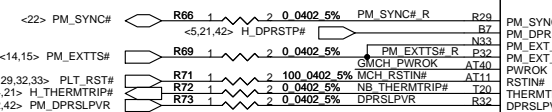


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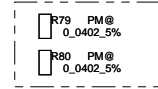
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| | U3B |
|-------|--------|
| X M36 | RSVD1 |
| X A36 | RSVD2 |
| X B33 | RSVD3 |
| X T33 | RSVD4 |
| X AH9 | RSVD5 |
| AH10 | RSVD6 |
| AH12 | RSVD7 |
| AH13 | RSVD8 |
| X K12 | RSVD9 |
| X A34 | RSVD10 |
| X A34 | RSVD11 |
| AH35 | RSVD12 |
| AH35 | RSVD13 |
| X T24 | RSVD14 |
| X B31 | RSVD15 |
| X B2 | RSVD16 |
| X M1 | RSVD17 |
| AY21 | RSVD20 |
| BG23 | RSVD22 |
| BF23 | RSVD23 |
| BH18 | RSVD24 |
| BF18 | RSVD25 |

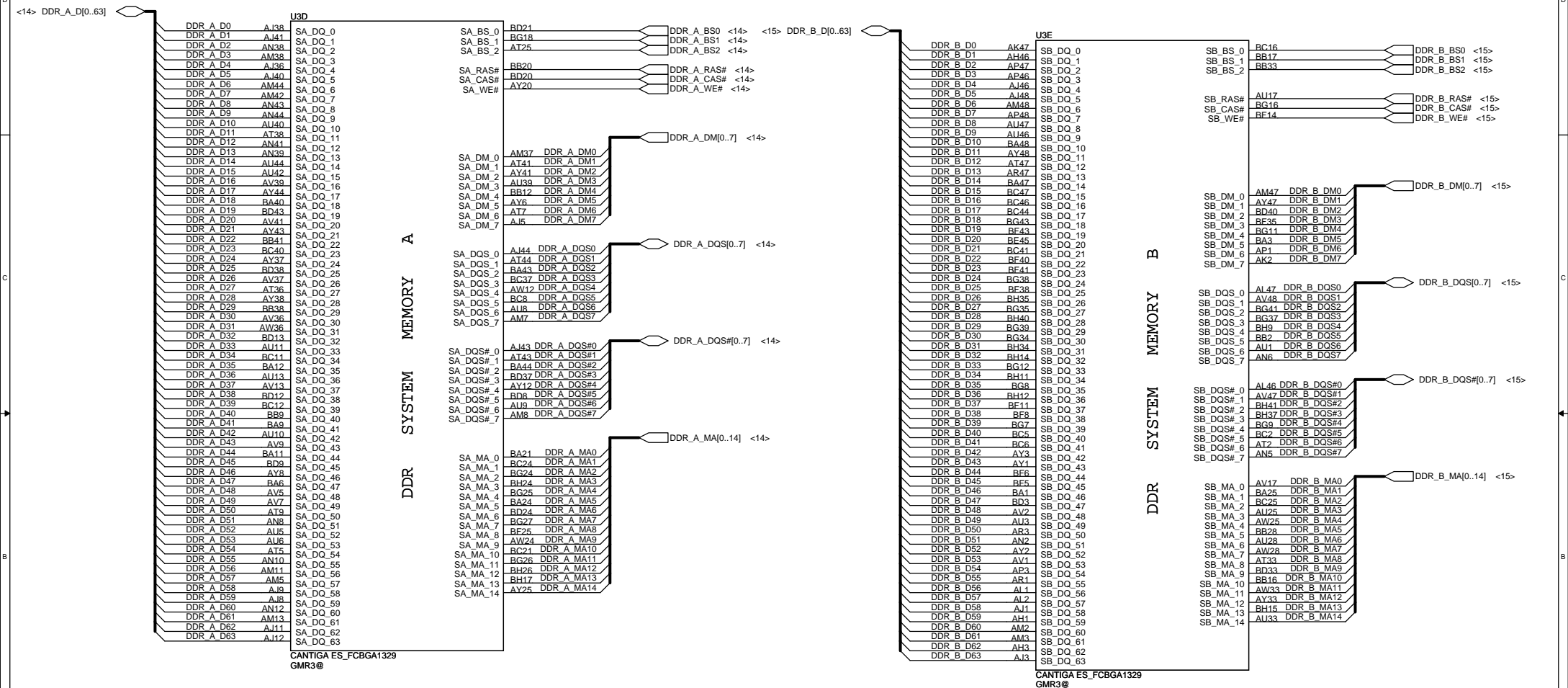


Strap Pin Table

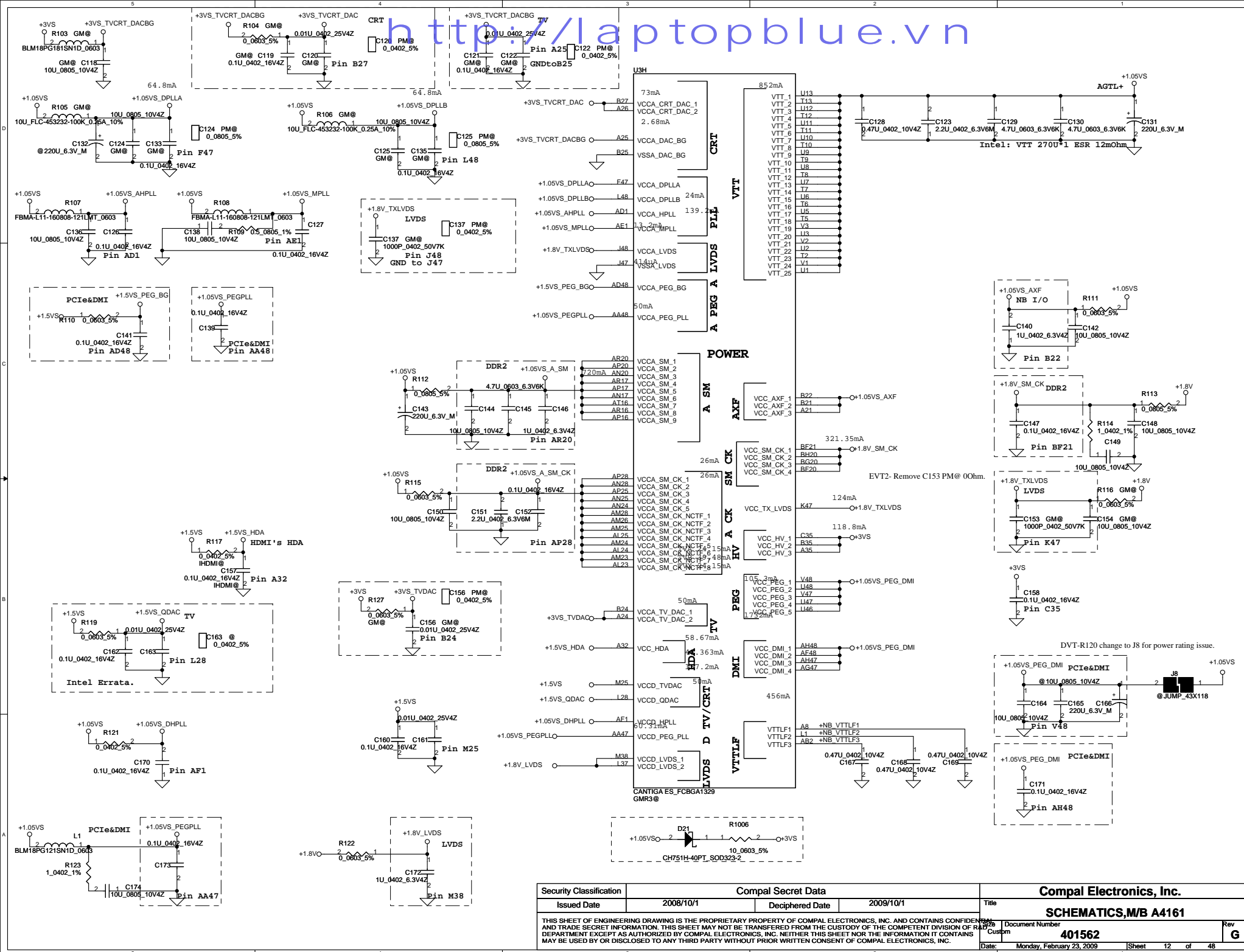
Figure 1 is a schematic diagram of a power supply circuit. It shows two input lines, SDVO_SCLK and SDVO_SDATA, each with a 2.2K 0402 5% resistor (R79 and R80) connected to a 3V3 supply. The circuit also includes resistors R135 and R134, and labels GM@ and PM@.

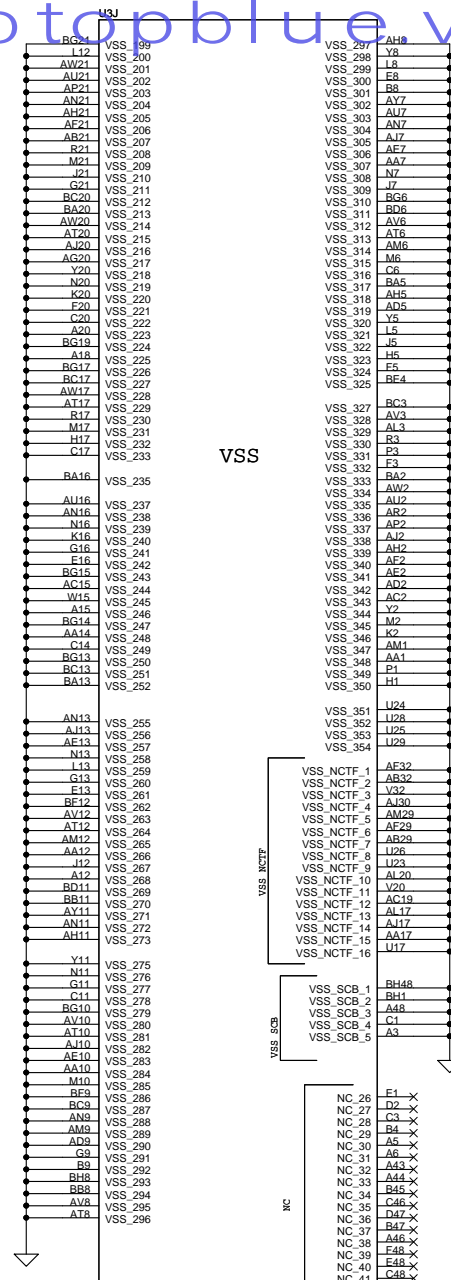
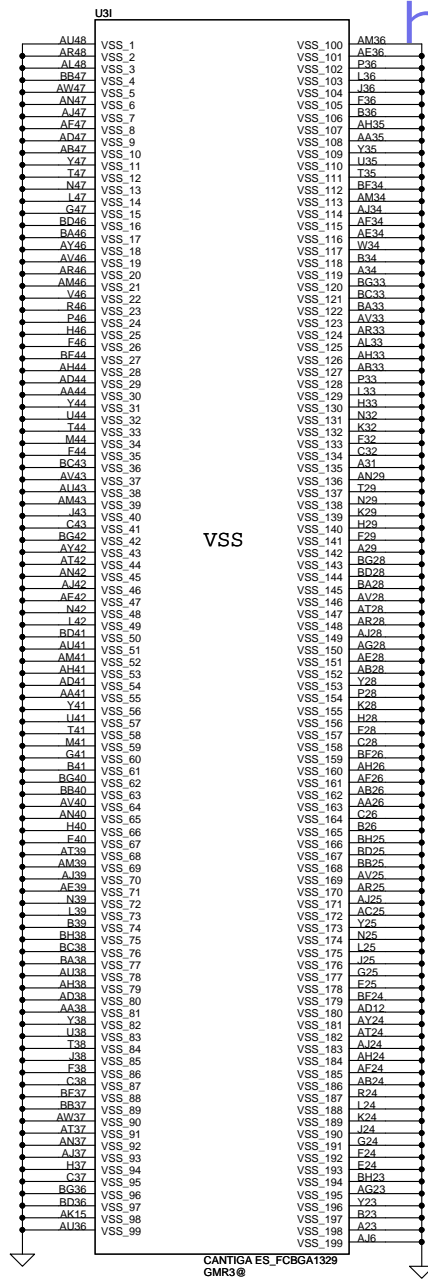


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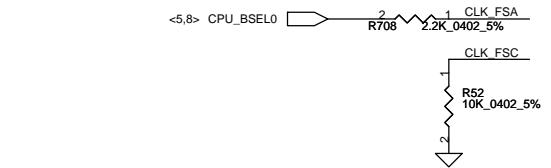
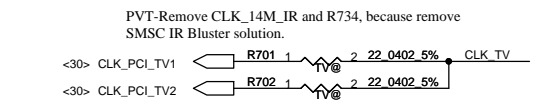
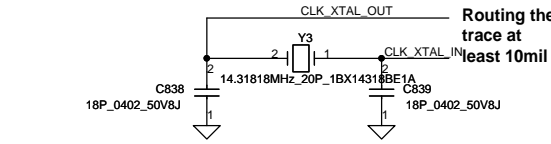
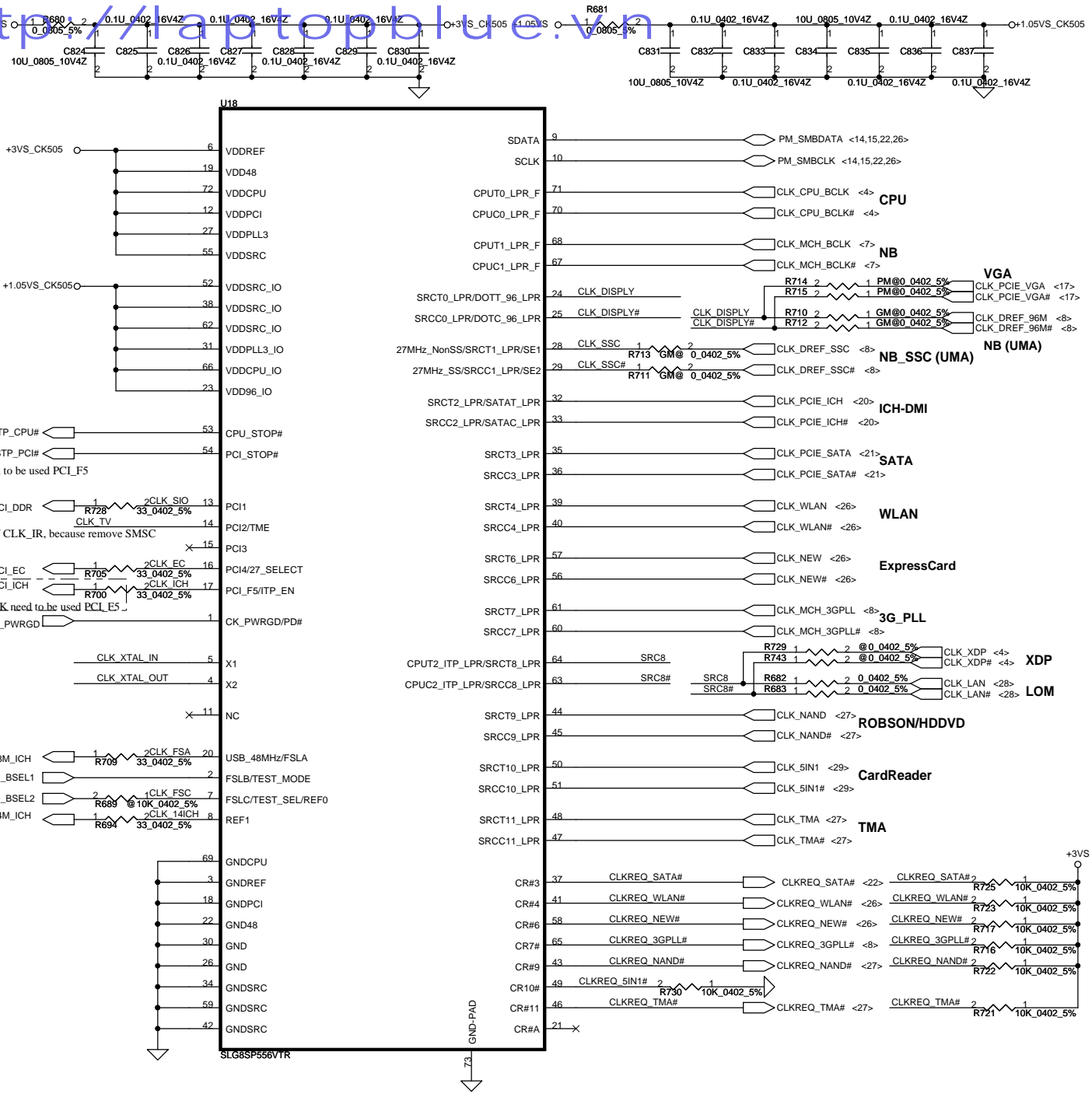




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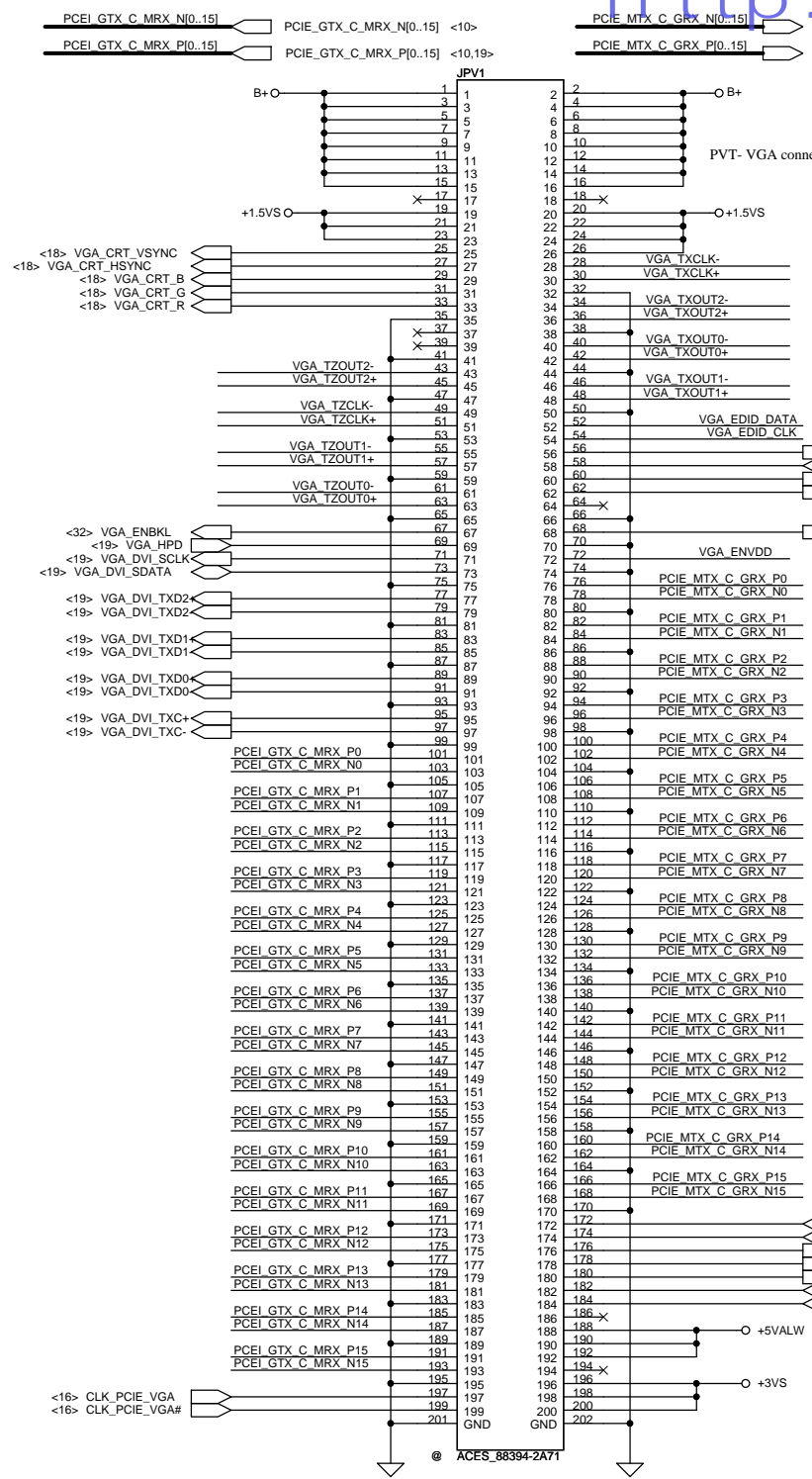
| FSC | FSB | FSA | CPU | SRC | PCI | REF | DOT_96 | USB |
|---------|---------|---------|----------|-----|------|--------|--------|------|
| CLKSEL2 | CLKSEL1 | CLKSEL0 | MHz | MHz | MHz | MHz | MHz | MHz |
| 0 | 0 | 0 | 266 | 100 | 33.3 | 14.318 | 96.0 | 48.0 |
| 0 | 0 | 1 | 133 | 100 | 33.3 | 14.318 | 96.0 | 48.0 |
| 0 | 1 | 0 | 200 | 100 | 33.3 | 14.318 | 96.0 | 48.0 |
| 0 | 1 | 1 | 166 | 100 | 33.3 | 14.318 | 96.0 | 48.0 |
| 1 | 0 | 0 | 333 | 100 | 33.3 | 14.318 | 96.0 | 48.0 |
| 1 | 0 | 1 | 100 | 100 | 33.3 | 14.318 | 96.0 | 48.0 |
| 1 | 1 | 0 | 400 | 100 | 33.3 | 14.318 | 96.0 | 48.0 |
| 1 | 1 | 1 | Reserved | | | | | |



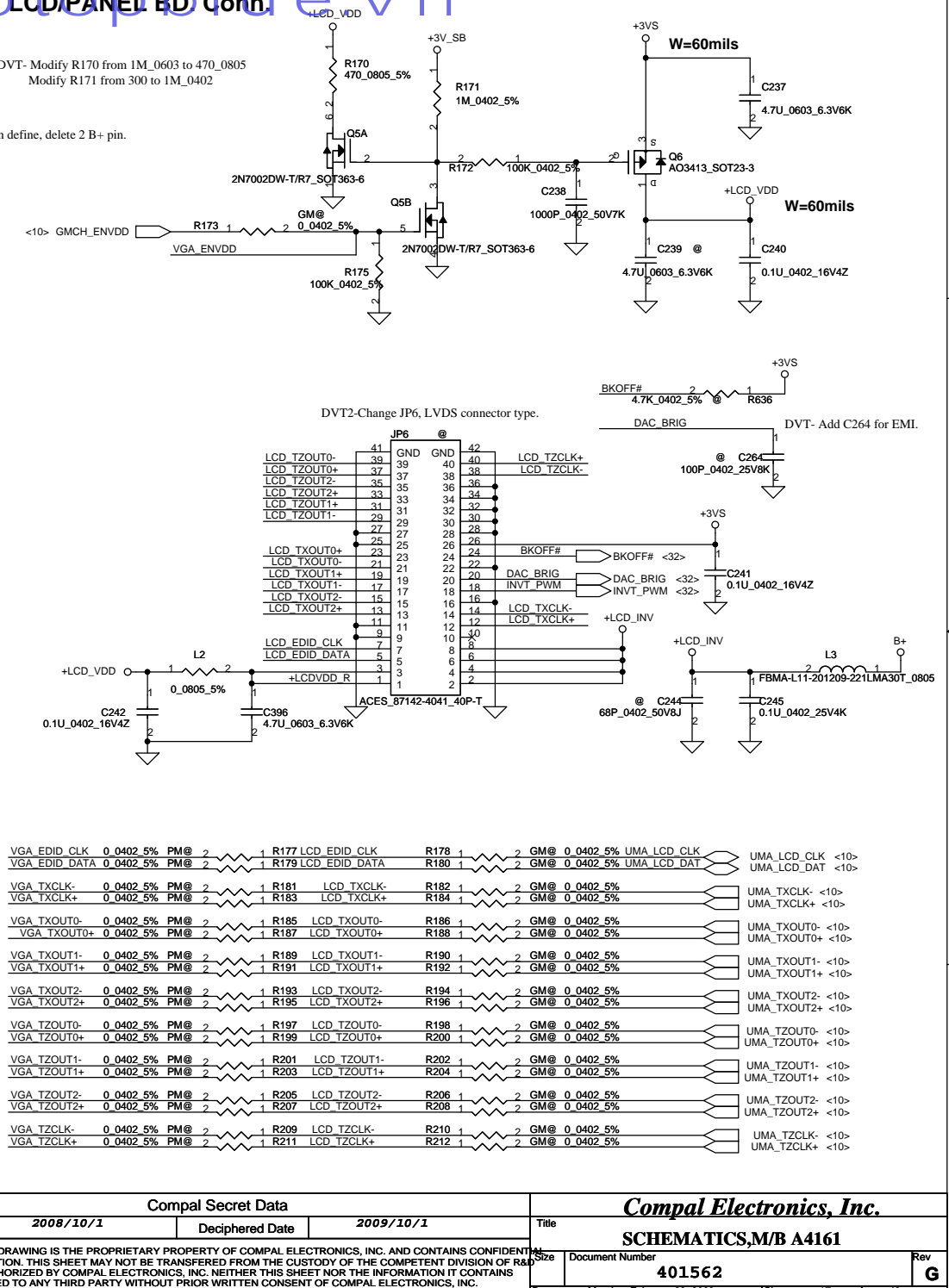
| | |
|--|--|
| CLK_ICH | 0 = SRC8/SRC8# 1 = ITP/ITP# |
| CLK_EC | 0 = Enable DOT96 & SRC1(UMA) 1 = Enable SRC0 & 27MHz(DIS) |
| PVT-modify R719/R724 signal from CLK_SIO to CLK ICH. | |
| | |

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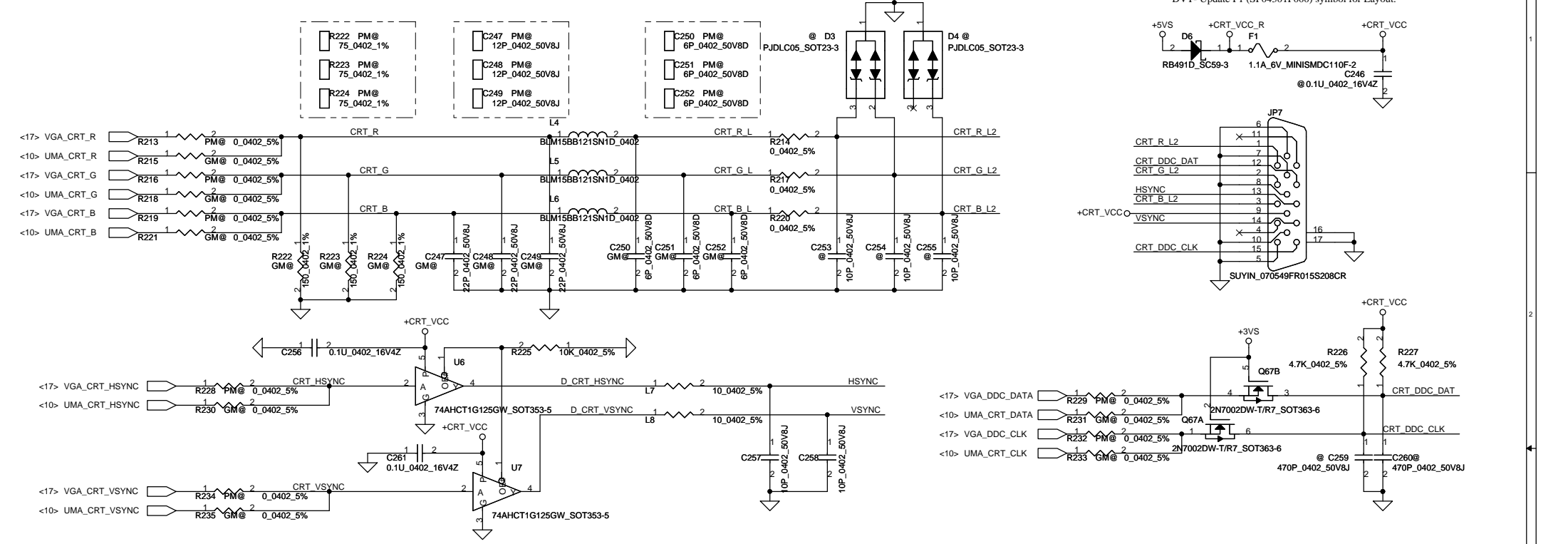
VGA BOARD Conn.



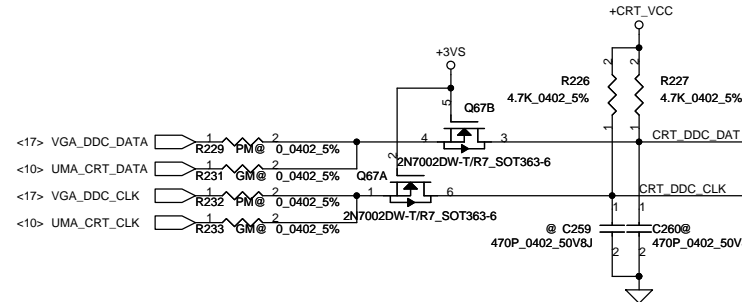
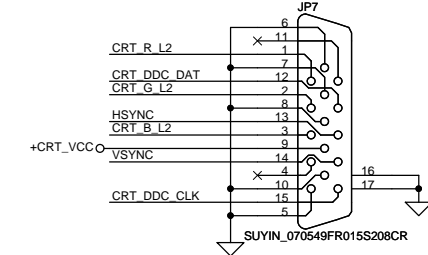
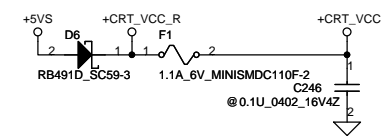
LCD/PANEL ED Conn.



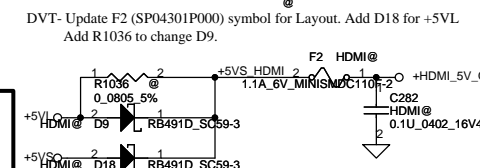
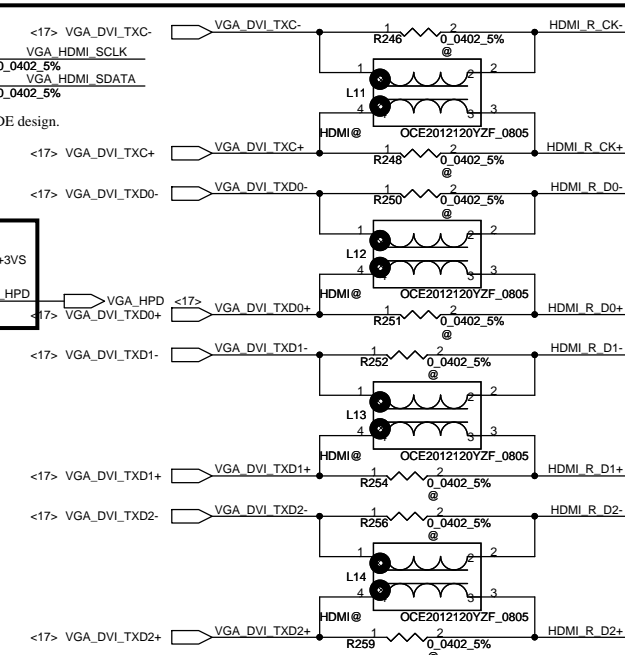
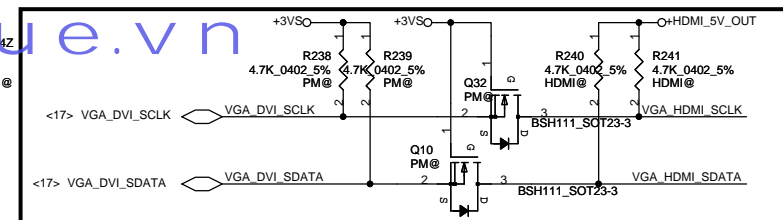
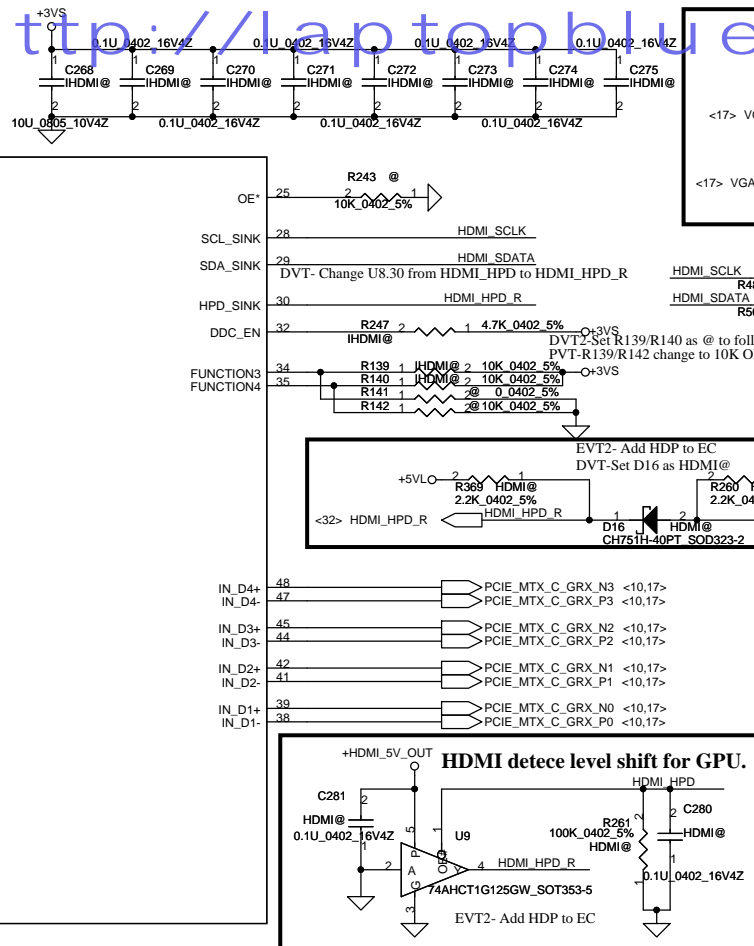
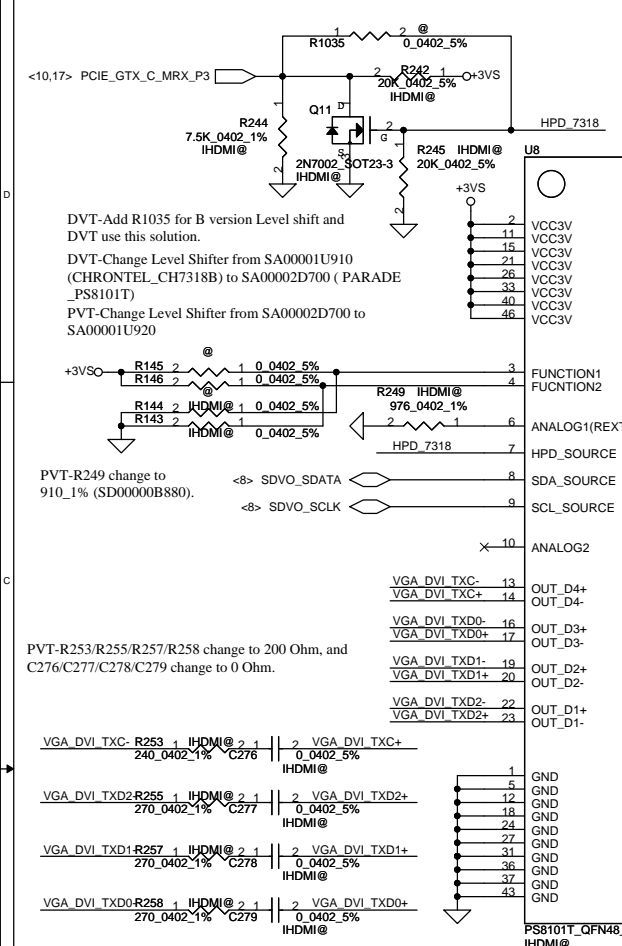
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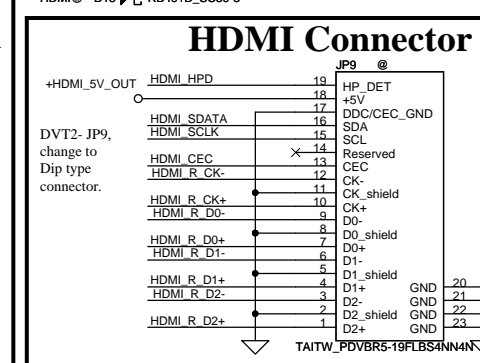
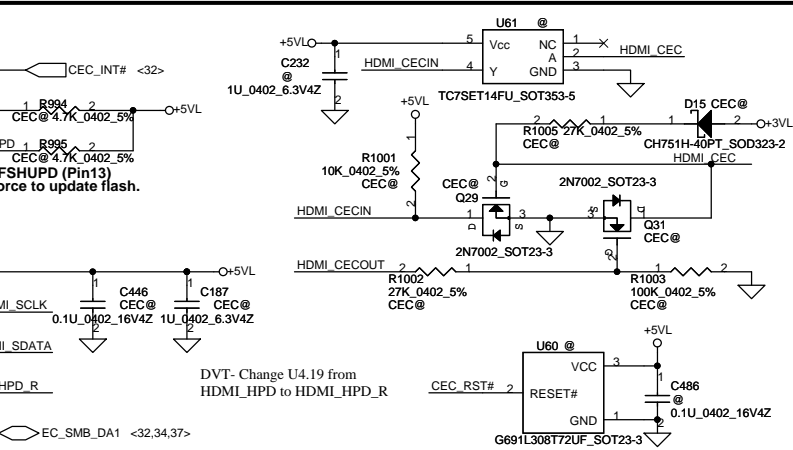
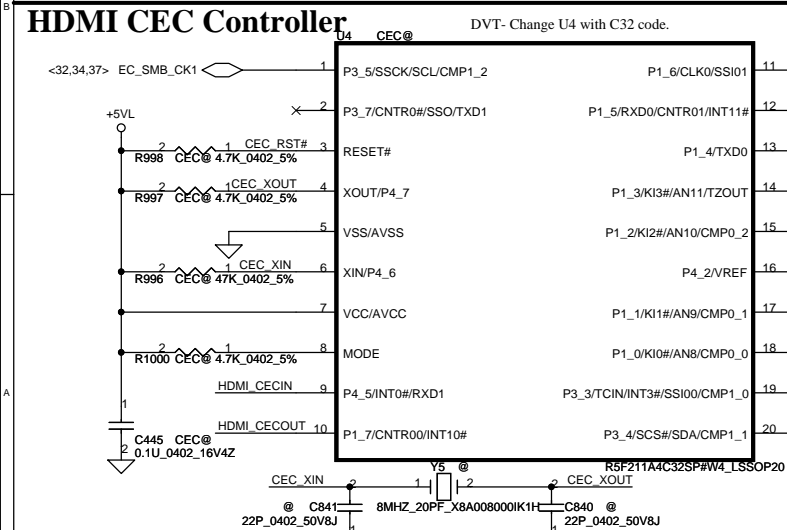
DVT- Update F1 (SP04301P000) symbol for Layout.



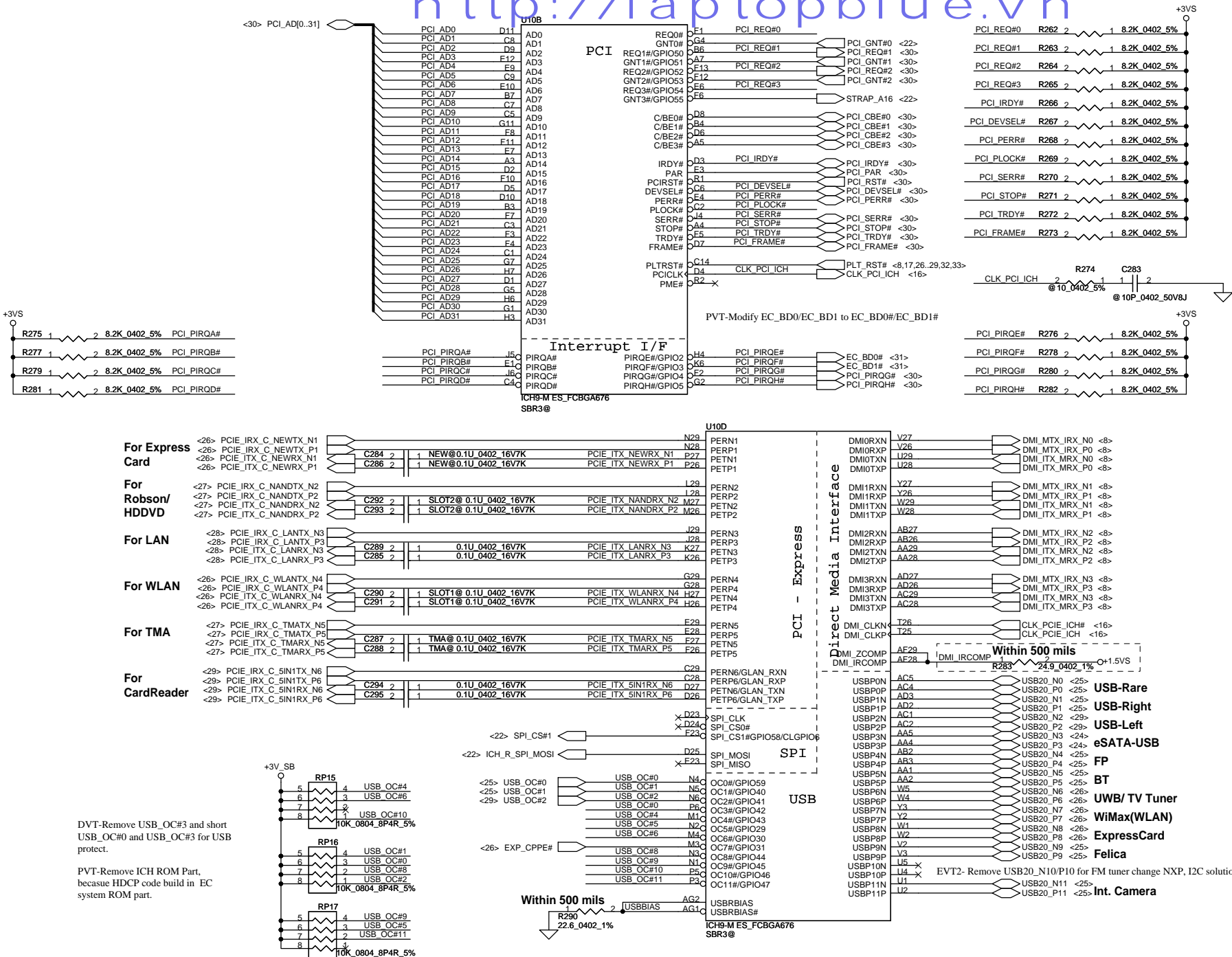
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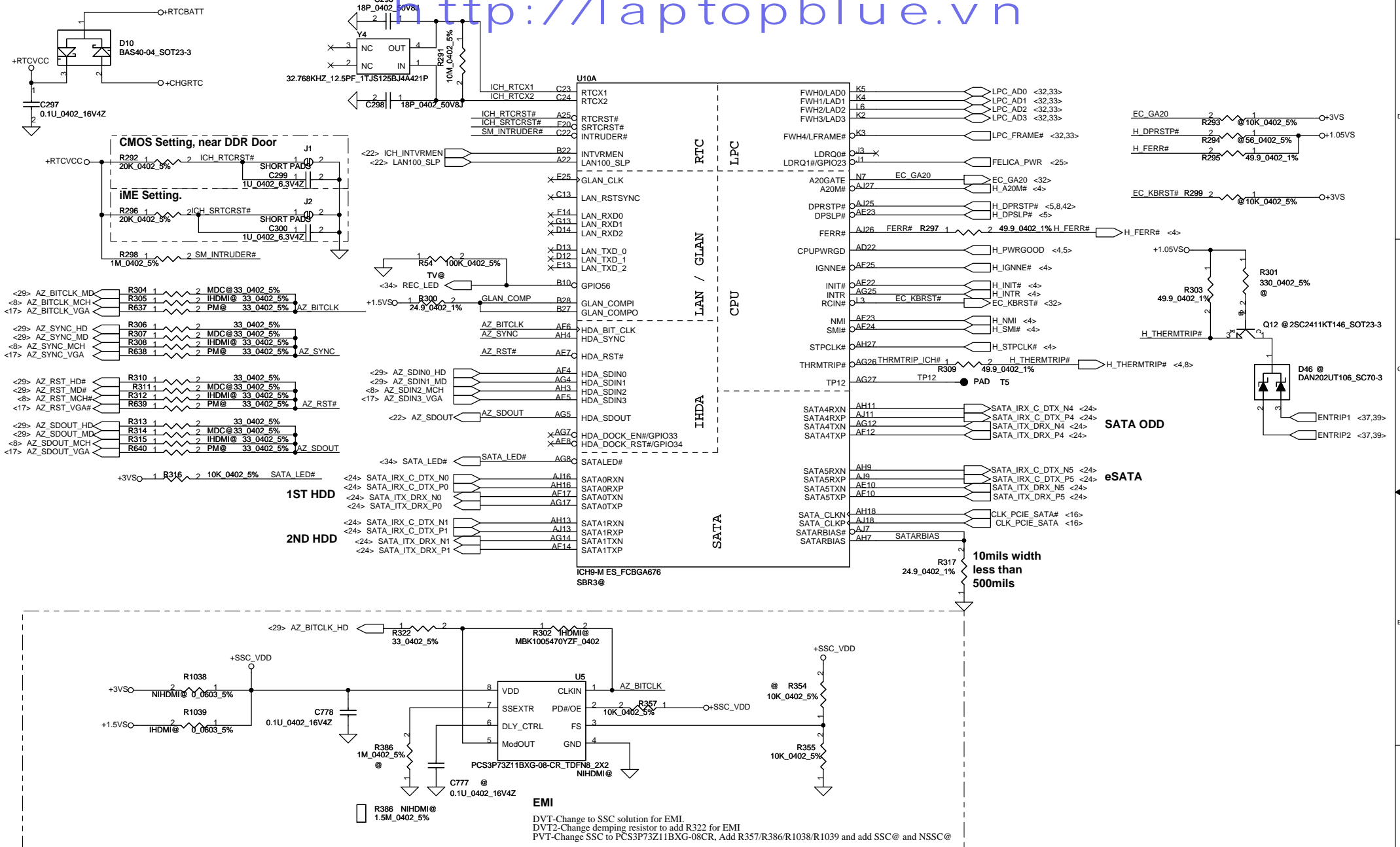
B HDMI CEC Controller



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| | | | | Date: | Monday, February 23, 2009 |
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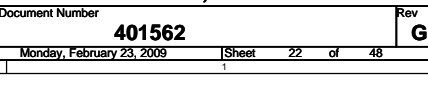
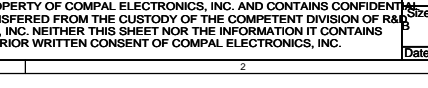
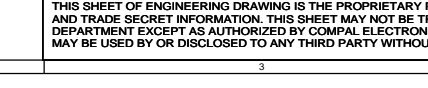
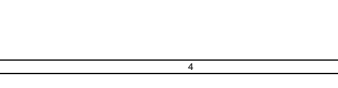
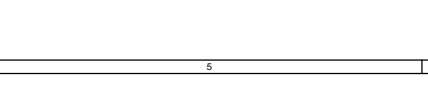
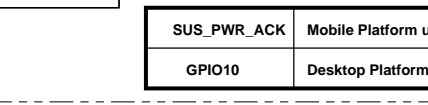
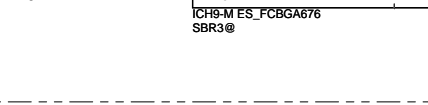
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Default: De-POP PU/PD Resistors, BIOS set GPIO

Default: De-POP PU/PD Resistors, BIOS set GPIO



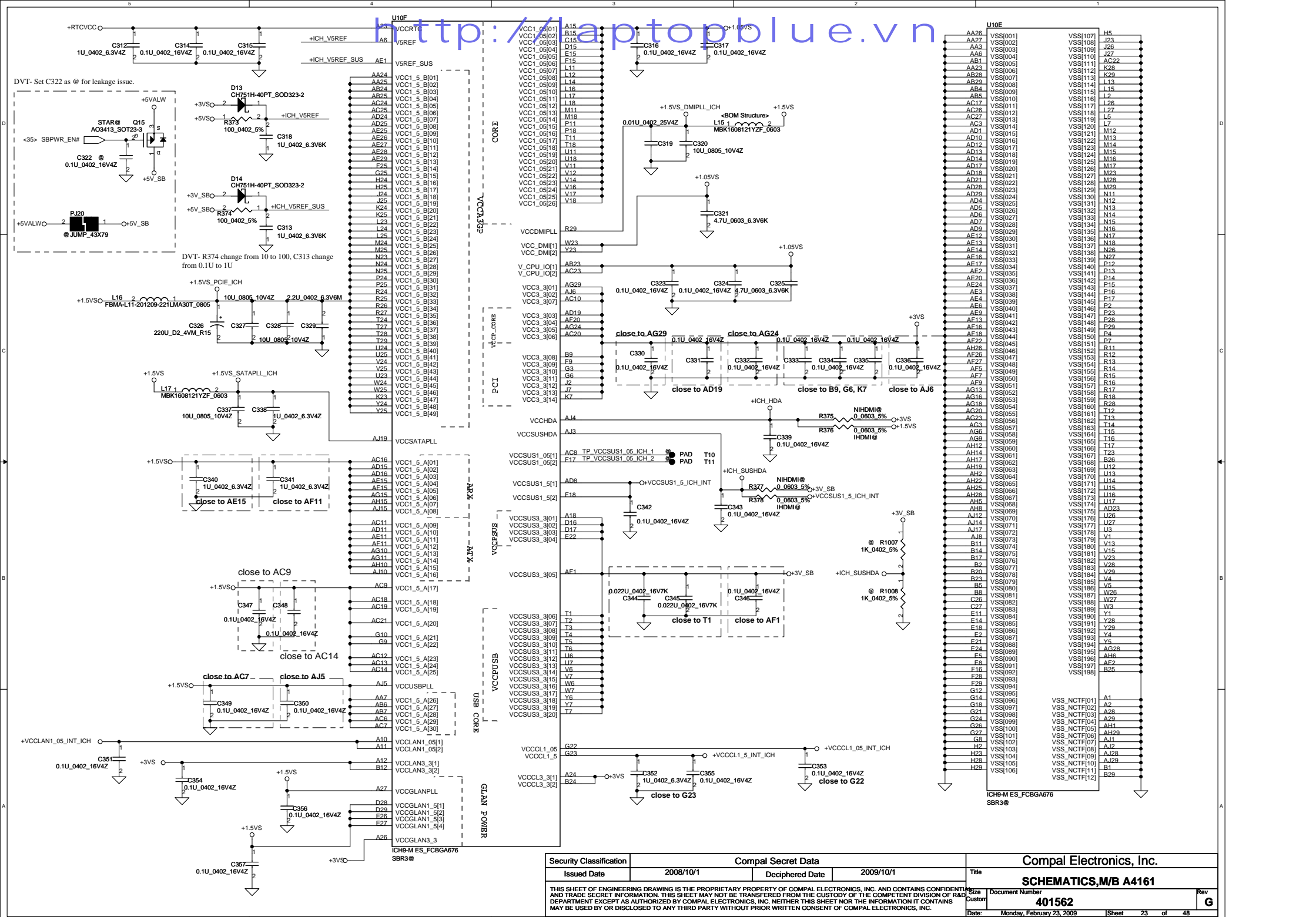
| XOR Chain Entrance Strap | | |
|--------------------------|-----------|----------------------------|
| ICH_TP3 | HDA_SDOUT | Description |
| 0 | 0 | RSVD |
| 0 | 1 | Enter XOR Chain |
| 1 | 0 | Normal Operation (Default) |
| 1 | 1 | Set PCIE port config bit 1 |

| Flash Descriptor Security Override Strap | |
|--|--|
| GPIO33 | Low= Descriptor Security override High= Default* (Internal pull-up) |

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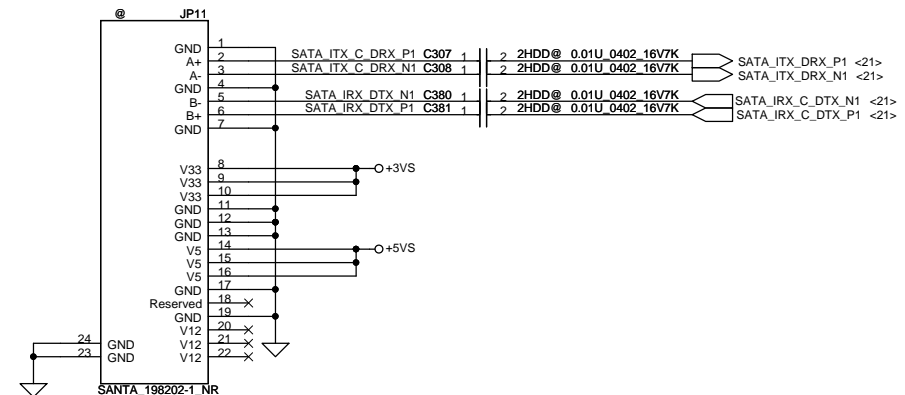
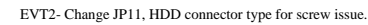
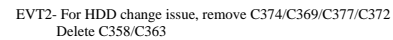
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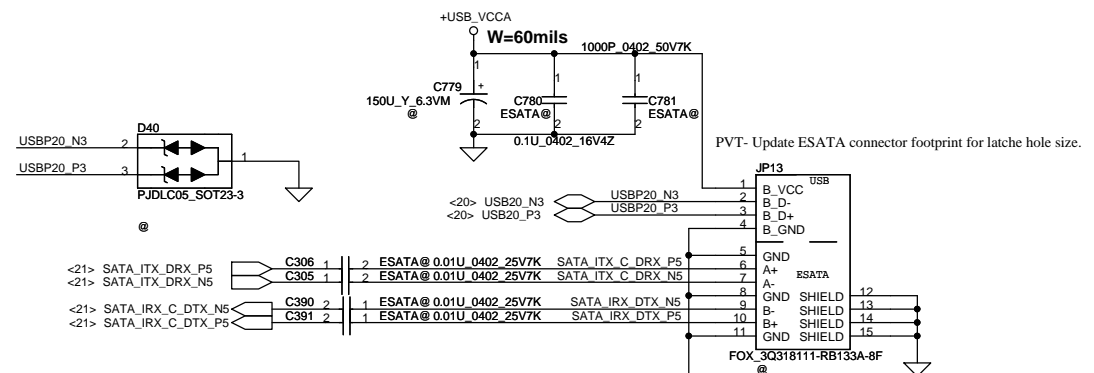


2nd SATA HDD Conn.

2nd SATA HDD Conn.

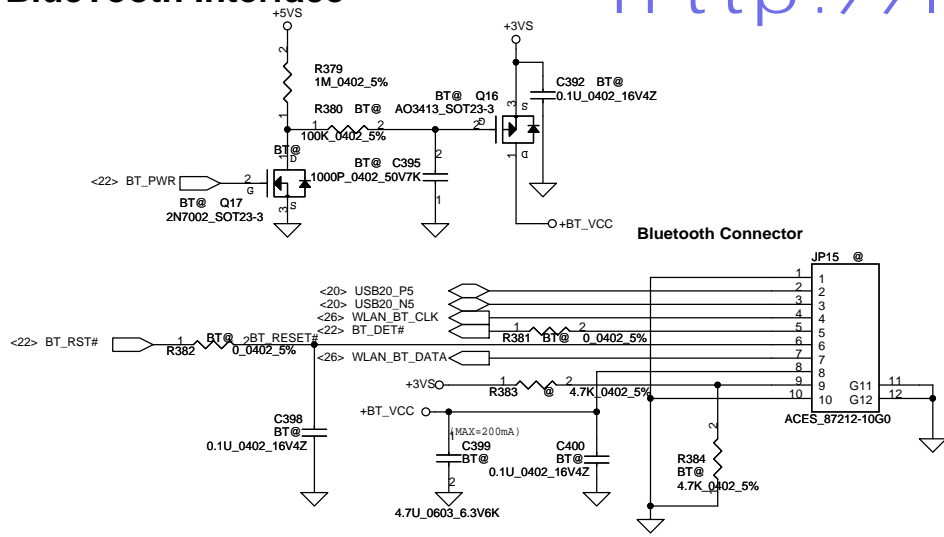


SATA ODD Conn

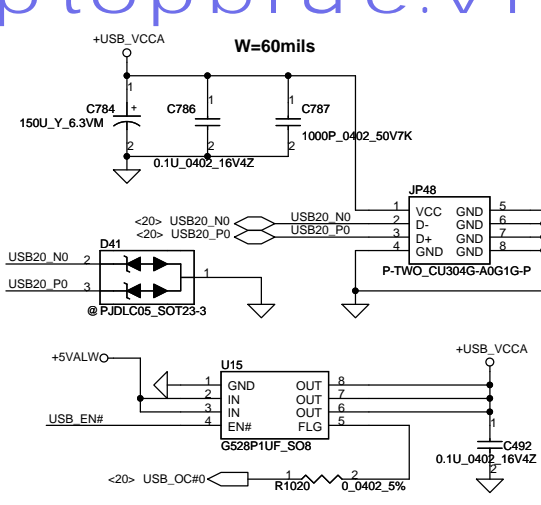


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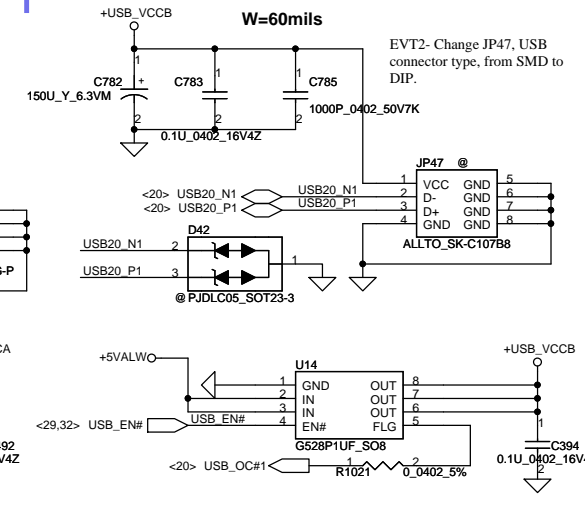
BlueTooth Interface



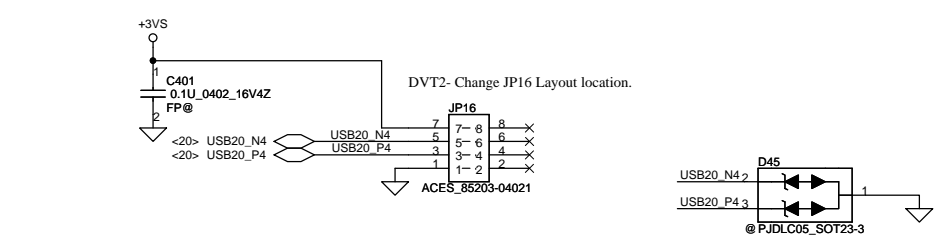
USB CONN.1 -- Rear



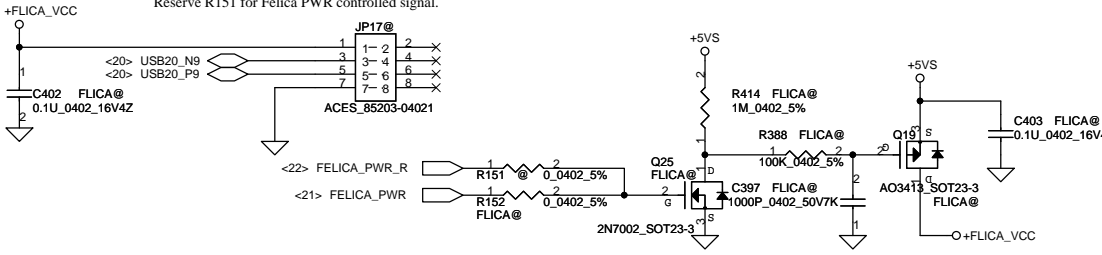
USB CONN.2 -- Right



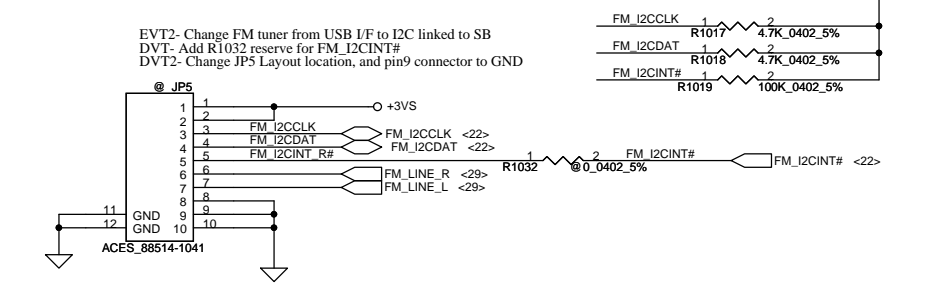
Finger printer



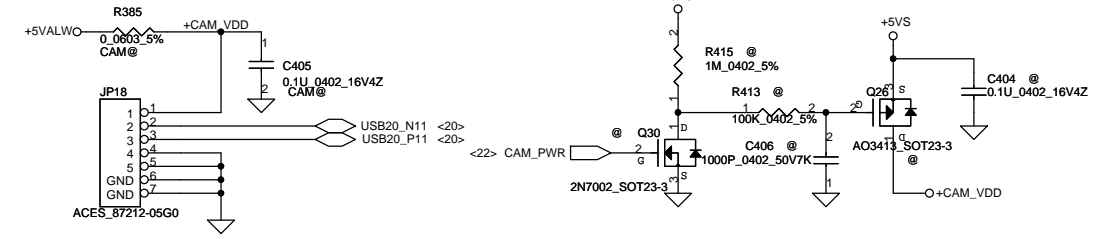
Felica



FM Module

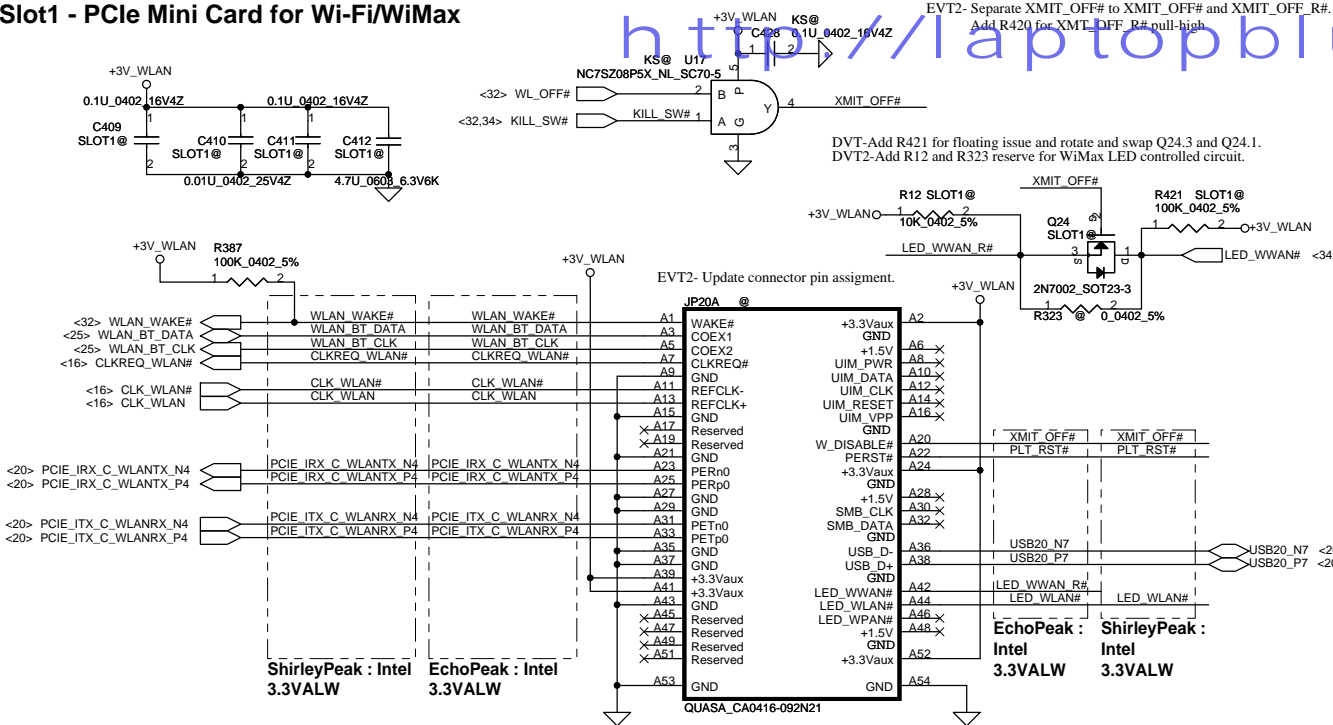


Int. Camera

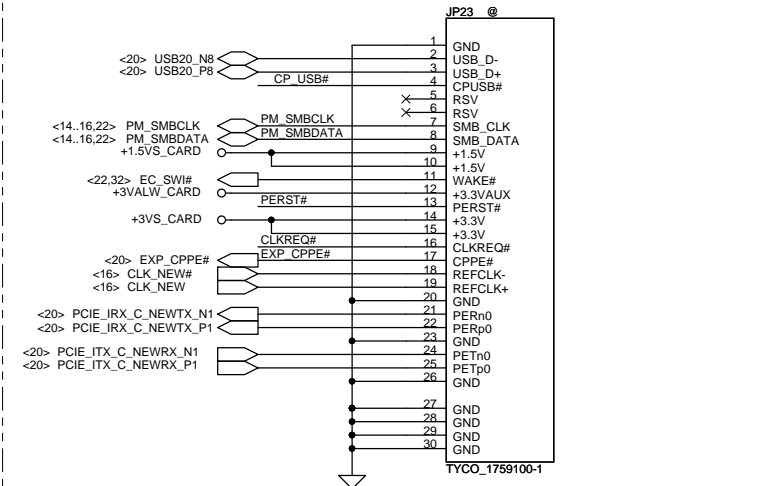
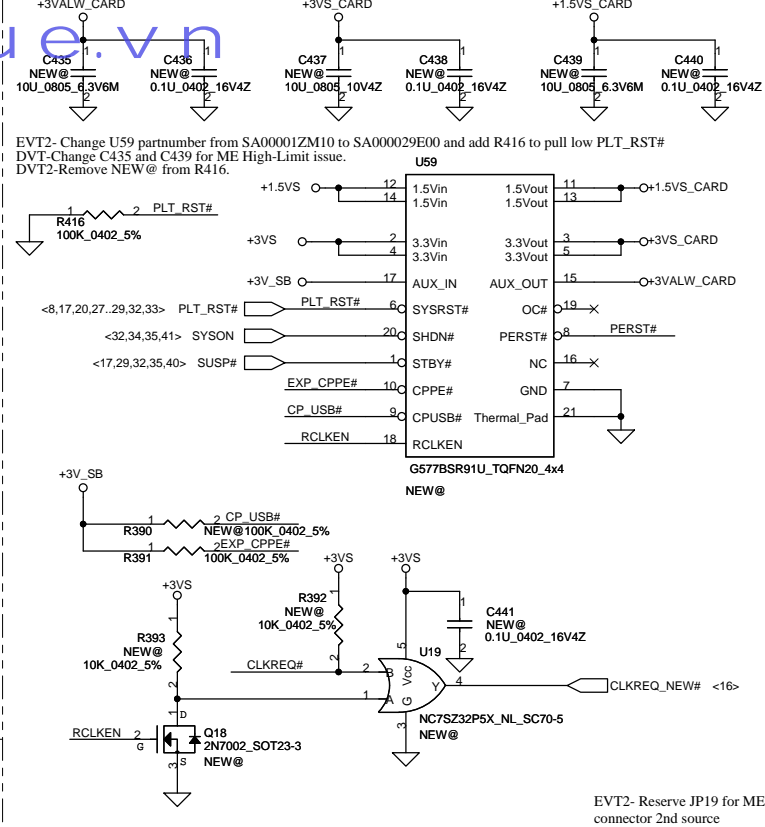
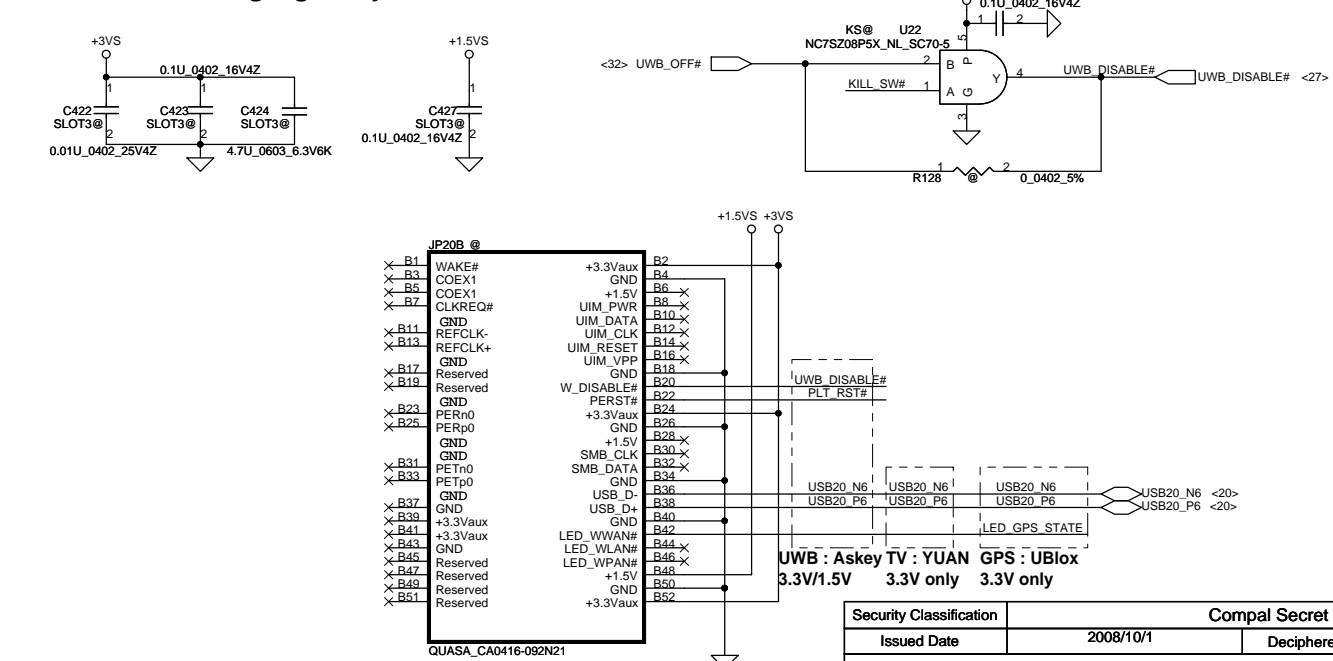


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Slot1 - PCIe Mini Card for Wi-Fi/WiMax

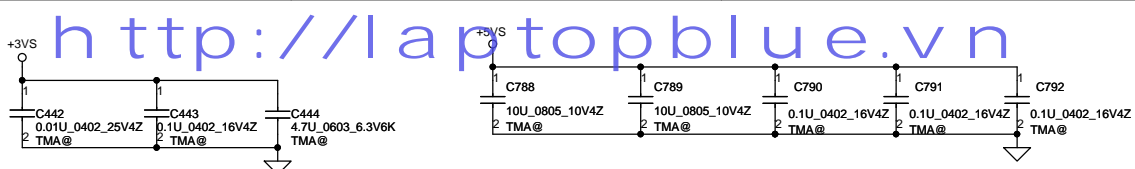


Slot3 - PCIe Mini Card for UWB/
DVB-T analog/digital Hybrid TV Tuner

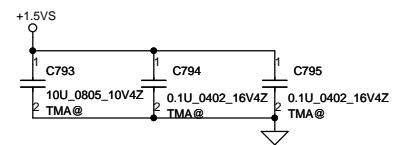
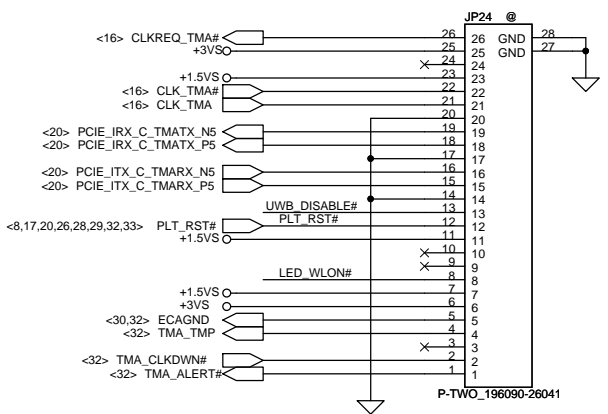


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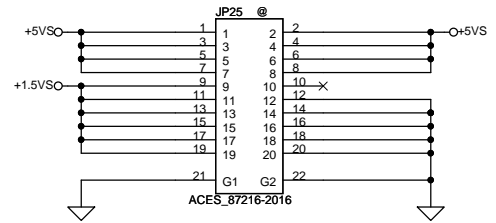
PCle Mini Card for TMA



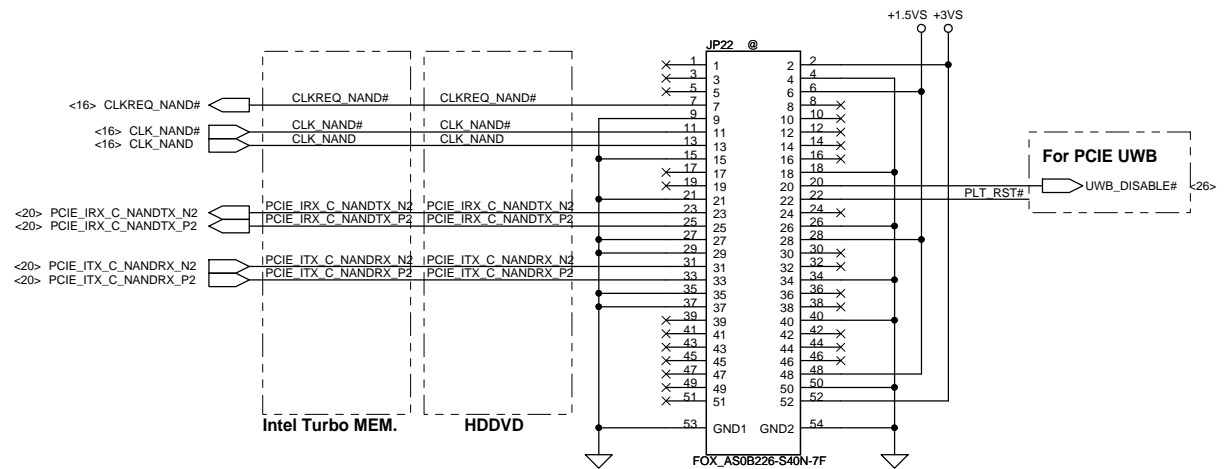
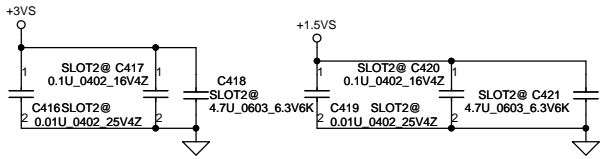
EVT2- Change JP24, TMA connector from 34pin to 24pin type.
DVT- Change JP24, TMA connector from 24pin to 26pin type. To add TMA_TMP and ECAGND.
PVT- Change JP24 pin24 as NC because near power pin to prevent assembly issue.



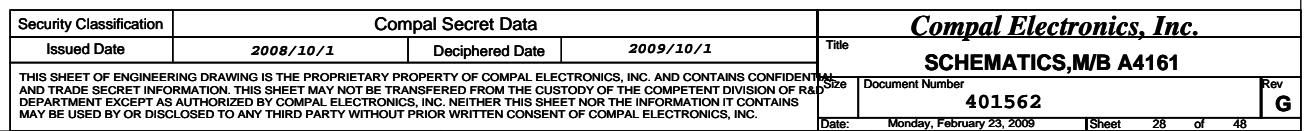
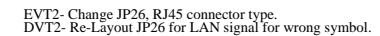
EVT2- Change JP25, TMA power connector type, from right-angle to Horizontal.



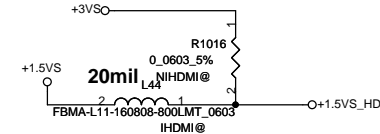
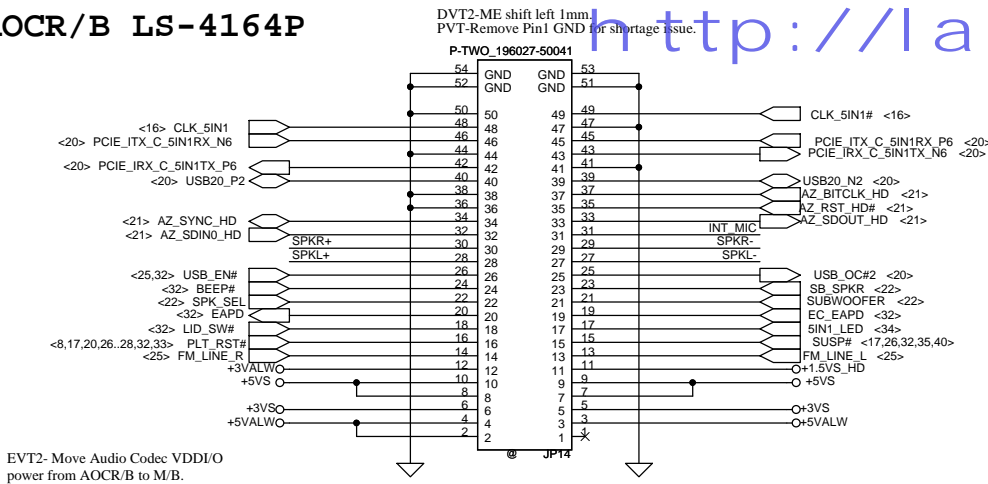
Slot2 - PCIe Mini Card for Robson/ HDDVD



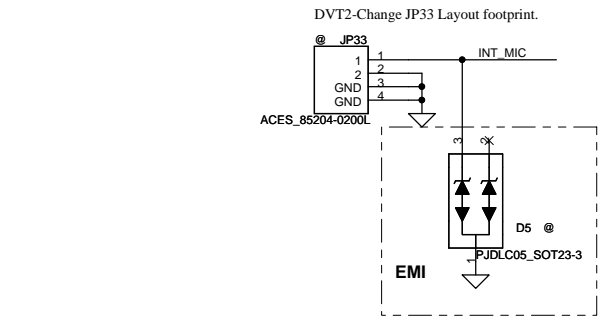
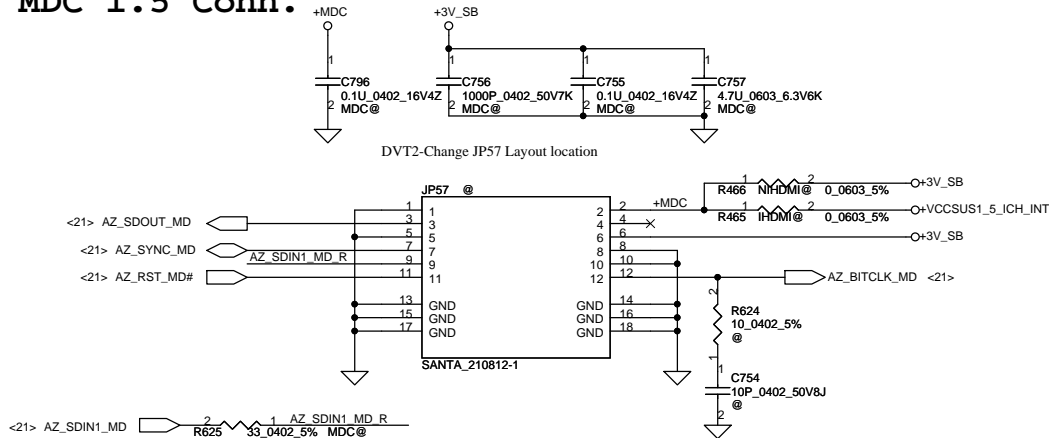
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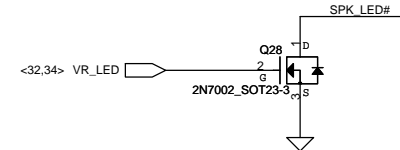
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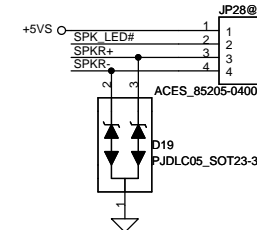
MDC 1.5 Conn.



Right Main Speaker & SPKR-LED/B Connector

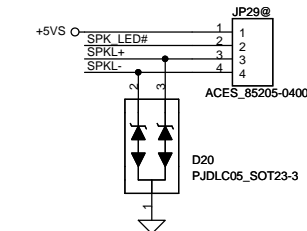


EVT2- JP28, JP29 chage footprint to meet ME.
Remove SPK ALC269 circuit.

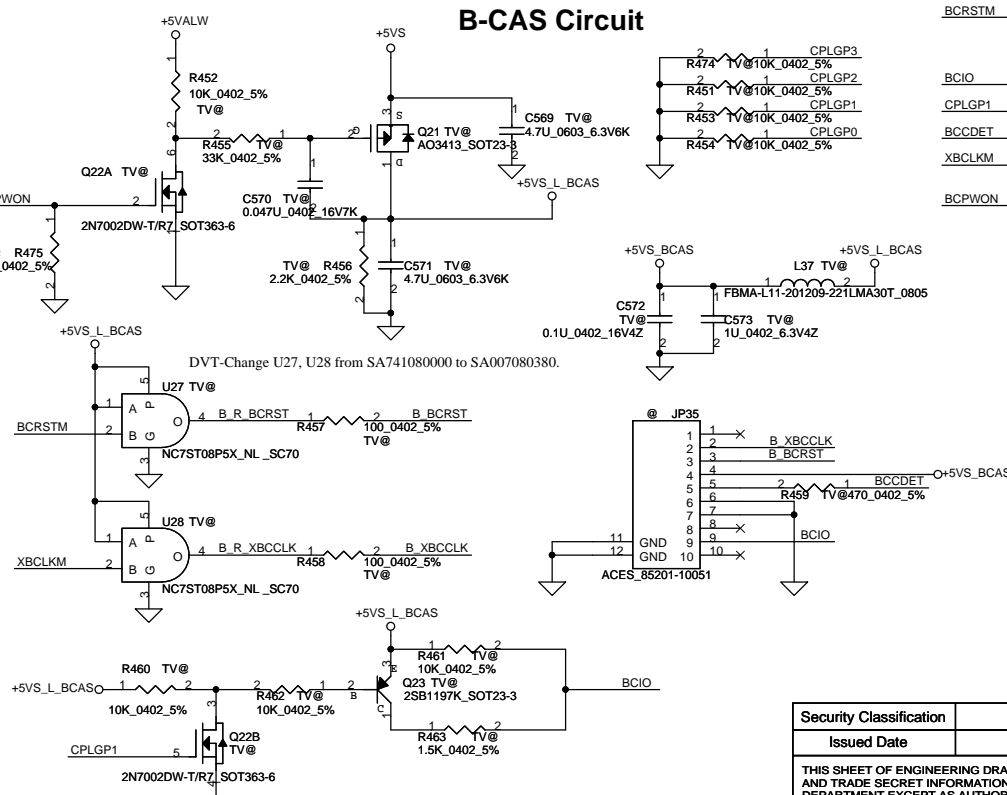
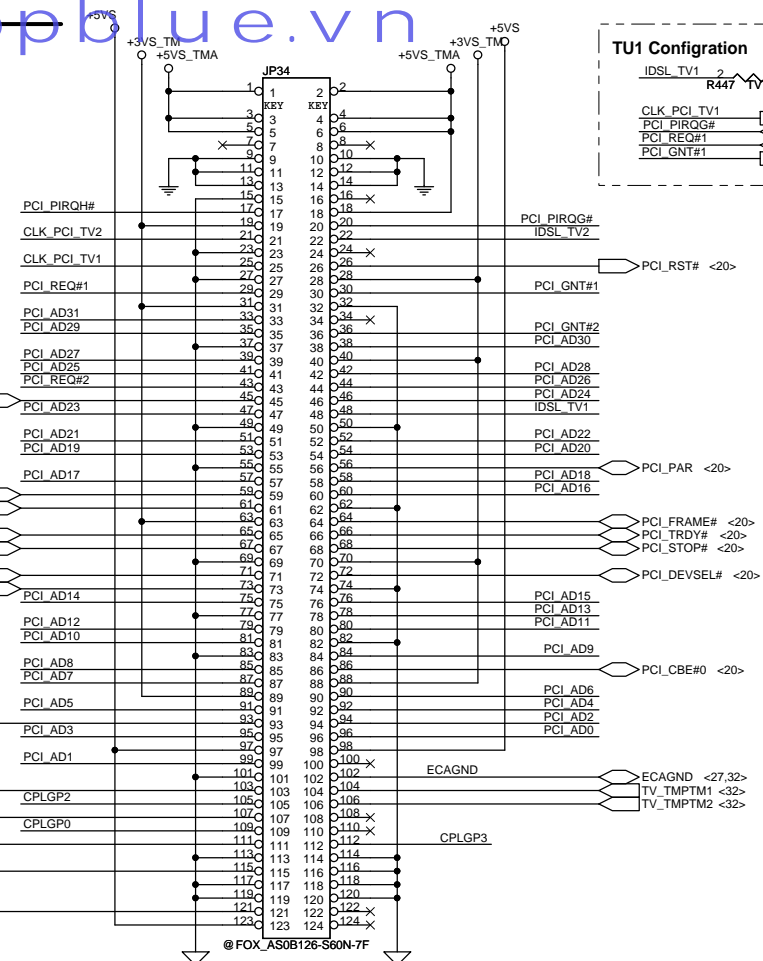
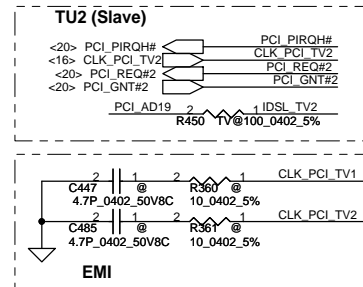
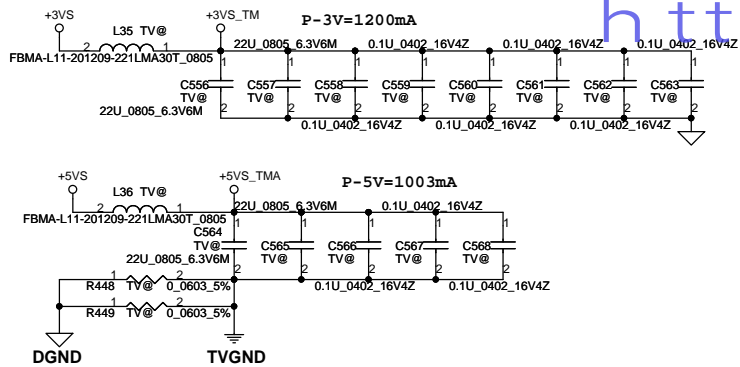


Left Main Speaker & SPKR-LED/B Connector

EVT2- JP28, JP29 chage footprint to meet ME.
Remove SPK ALC269 circuit.

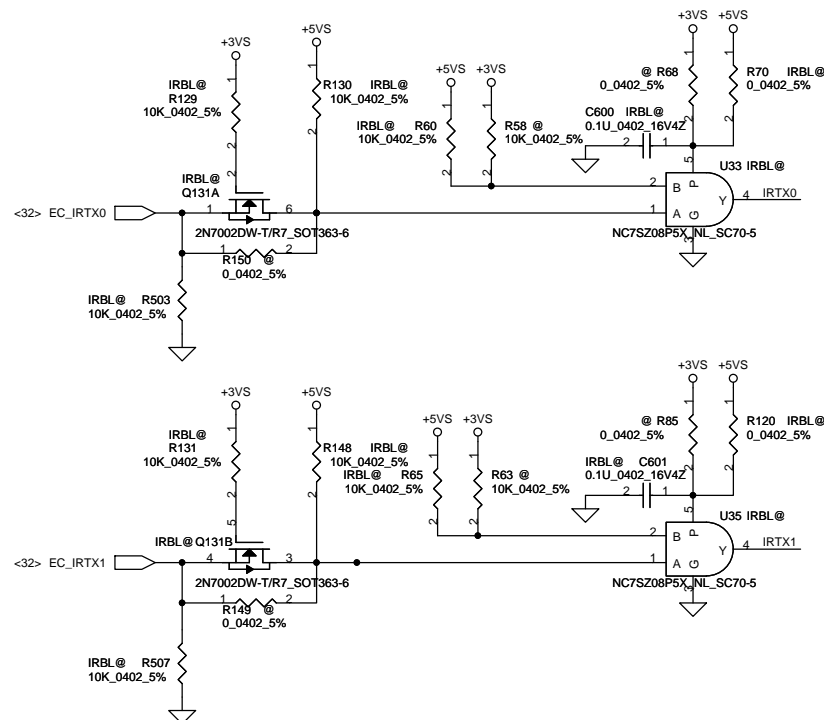


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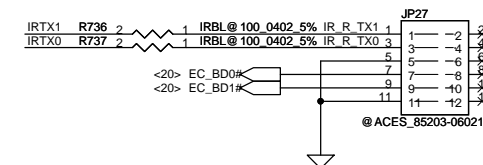


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EVT2- LEARNIR change to LEARNIR#
PVT-Delete SMC IR Bluster solution
Delete R738,R739, R748,R749



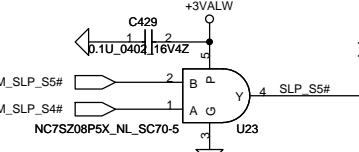
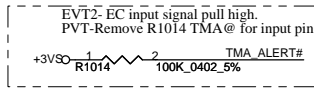
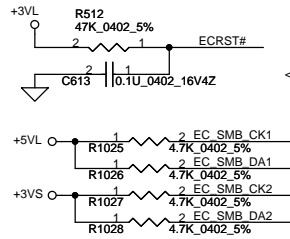
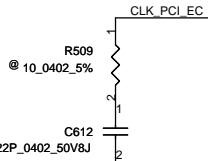
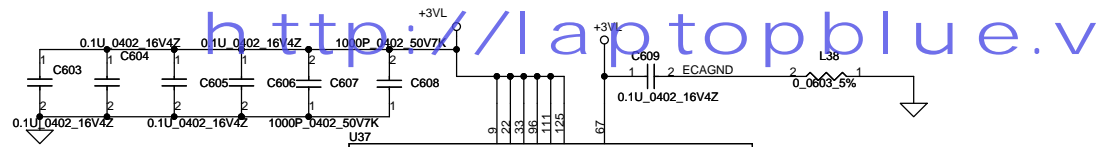
DVT- Delete R508 and R510, duplicate with R276 and R278.
R736 and R737, change from 100 to 33.



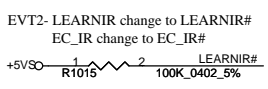
PVT-Modify EC_BD0/EC_BD1 to EC_BD0#/EC_BD1#
Modify BD0/BD1 to BD0#/BD1#

DVT2- Reserve Q3/Q8/Q136/R1013/R1037 for IR Blaster test

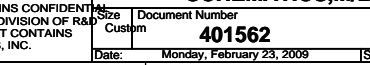
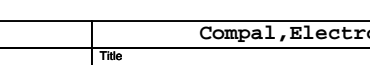
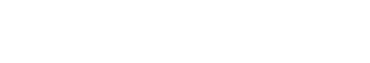
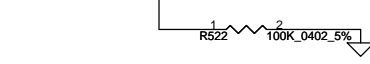
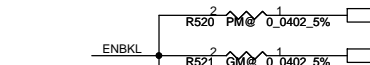
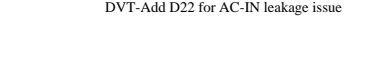
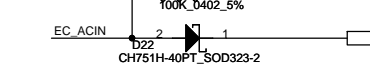
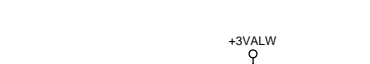
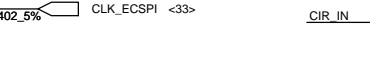
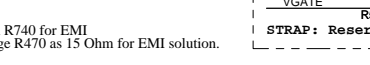
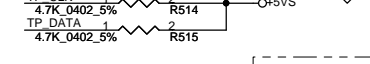
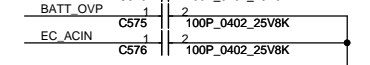
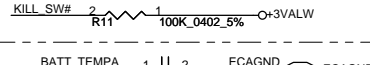
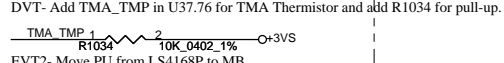
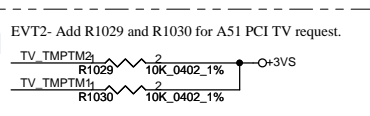
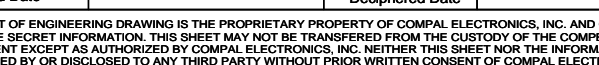
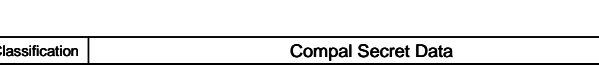
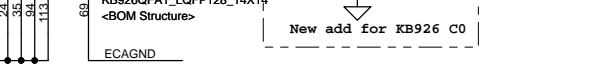
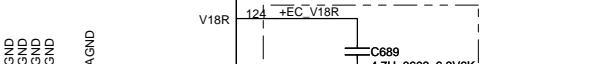
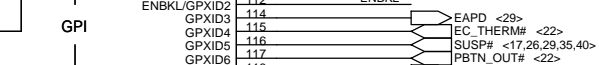
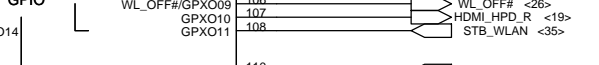
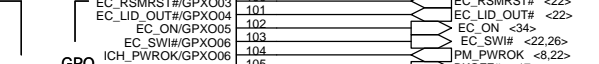
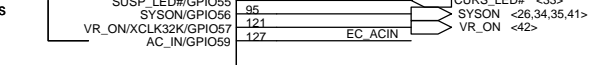
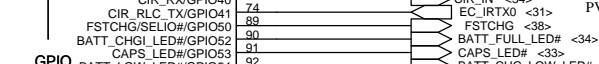
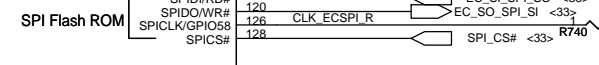
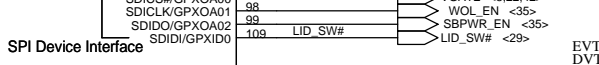
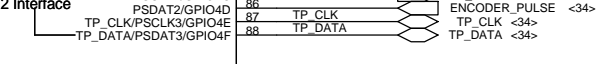
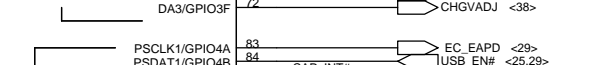
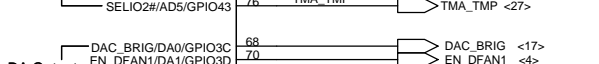
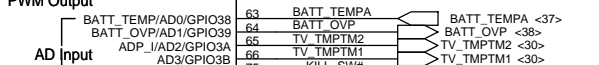
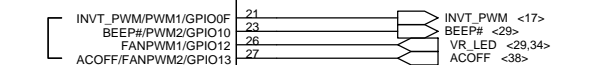
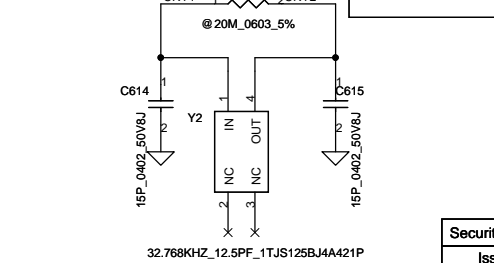
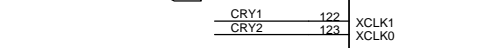
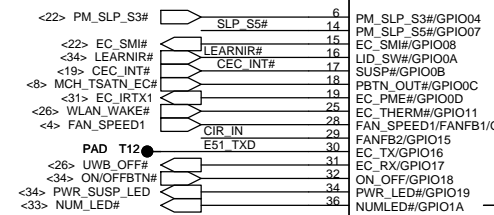
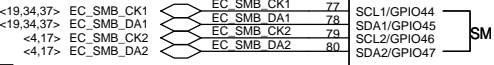
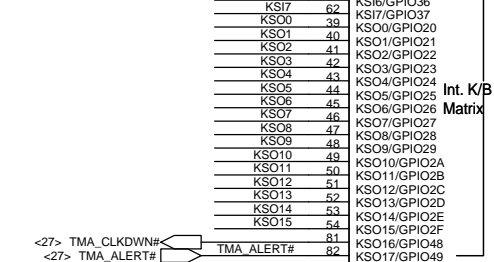
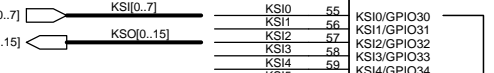
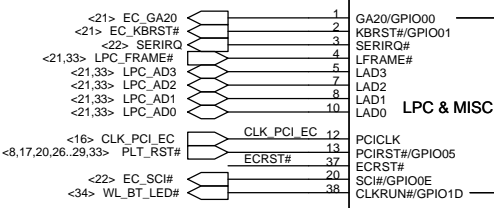
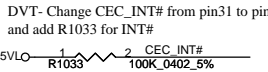
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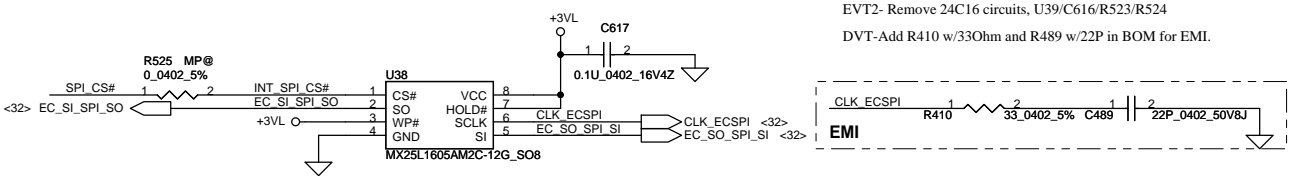
PVT-Remove IR_WAKE#/EC_IR# and R745/R744 for delete SMC solution.
DVT- Change MCH_TSATN_EC# from pin76 to pin18



EVT2- EC input signal pull high.
CEC_INT# add by A51.
DVT- Change CEC_INT# from pin31 to pin17

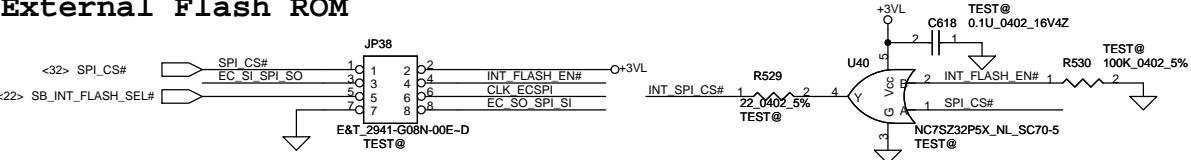


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EVT2- Remove 24C16 circuits, U39/C616/R523/R524
DVT-Add R410 w/330Ohm and R489 w/22P in BOM for EMI.

External Flash ROM



SI/O Debug

TP CONN.

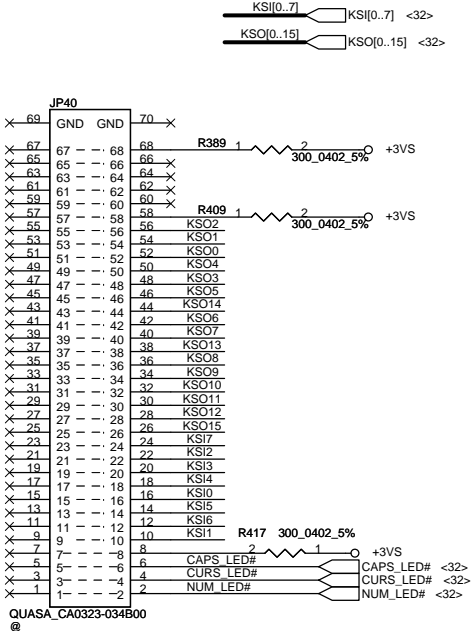
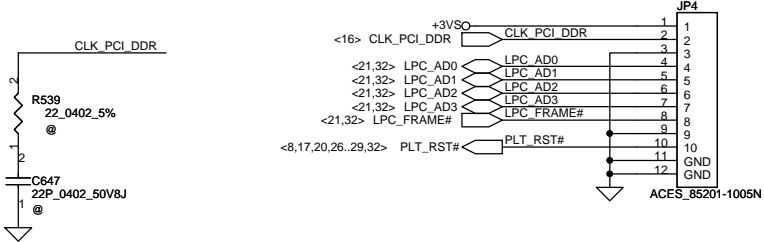
DVT2- Remove JP39, TP/B connector, and C621, because combined in LED/B connector

KEYBOARD CONN.

DVT- Change Keyboard capacitors to mount components for EMI.

LPC Debug Port

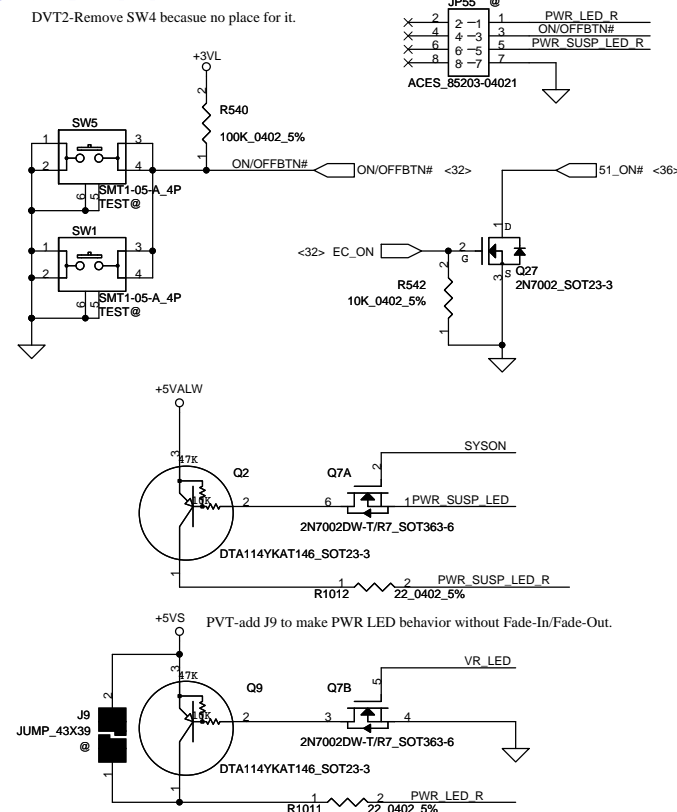
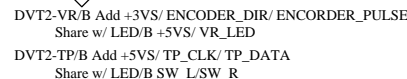
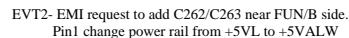
EVT2- Delete EC debug port to reduce space for Layout.
Change Debug PAD to 10pin connector.



| | | |
|-----------|------|-----------------|
| KSO2 | C619 | 100P_0402_25V8K |
| KSO1 | C620 | 100P_0402_25V8K |
| KSO0 | C621 | 100P_0402_25V8K |
| KSO4 | C622 | 100P_0402_25V8K |
| KSO3 | C623 | 100P_0402_25V8K |
| KSO5 | C624 | 100P_0402_25V8K |
| KSO14 | C625 | 100P_0402_25V8K |
| KSO16 | C626 | 100P_0402_25V8K |
| KSO6 | C627 | 100P_0402_25V8K |
| KSO7 | C628 | 100P_0402_25V8K |
| KSO13 | C629 | 100P_0402_25V8K |
| KSO8 | C630 | 100P_0402_25V8K |
| KSO9 | C631 | 100P_0402_25V8K |
| KSO10 | C632 | 100P_0402_25V8K |
| KSO11 | C633 | 100P_0402_25V8K |
| KSO12 | C634 | 100P_0402_25V8K |
| KSO15 | C635 | 100P_0402_25V8K |
| KSI7 | C636 | 100P_0402_25V8K |
| KSI2 | C637 | 100P_0402_25V8K |
| KSI3 | C638 | 100P_0402_25V8K |
| KSI4 | C639 | 100P_0402_25V8K |
| KSI0 | C640 | 100P_0402_25V8K |
| KSI5 | C641 | 100P_0402_25V8K |
| KSI6 | C642 | 100P_0402_25V8K |
| KSI1 | C643 | 100P_0402_25V8K |
| CAPS_LED# | C644 | 100P_0402_25V8K |
| CURS_LED# | C645 | 100P_0402_25V8K |
| NUM_LED# | C646 | 100P_0402_25V8K |

LED/B LS4168P Connector

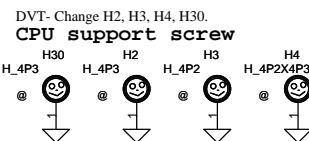
DVT2-Change JP55 Layout location



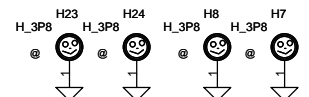
EVT2- Add R12/D7/Q3 for test checking.
DVT- Remove DC-IN test circuits, delete R12, D7 and Q3

DVT2- Remove JP51, VR/B connector, because combined in LED/B connector.

Screw Hole

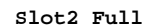


VGA support screw

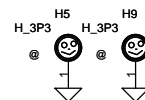


FAN module screw

DVT- New add in EVT2 for FAN Module.

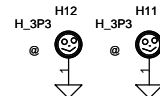


EVT2- Separate Slot2&Slot3 screw hole.
DVT- Change screw size from 1.15 to 1.2
DVT2- Change H9 and H10 from 1.2 to 3.3



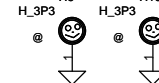
Slot1 Full/ Slot3 Full
support screw

DVT- Change screw size from 3.25 to 3.3



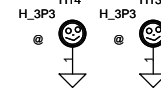
Slot3 Helf support screw

EVT2- Add H5/H6 for Slot3 half-module for movement issue.
DVT- Change screw size from 1.15 to 1.2
DVT2- Change H5 and H6 from 1.2 to 3.3



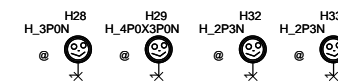
MDC/FM Module support

DVT- Change screw size from 1.15 to 1.2
DVT2- Change H13 and H14 from 1.2 to 3.3



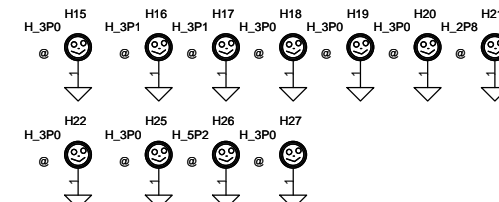
NPDH holes

EVT2- Add H32 and H33 for 2nd HDD bracket hole



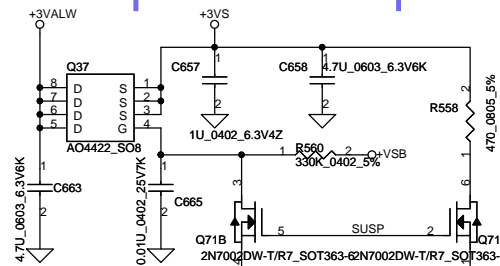
Other screw hole

EVT2- Change H21 to H 2P8

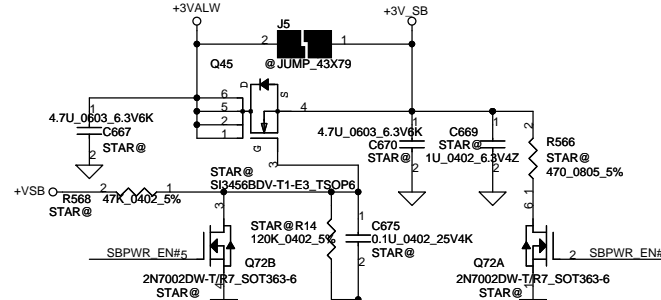


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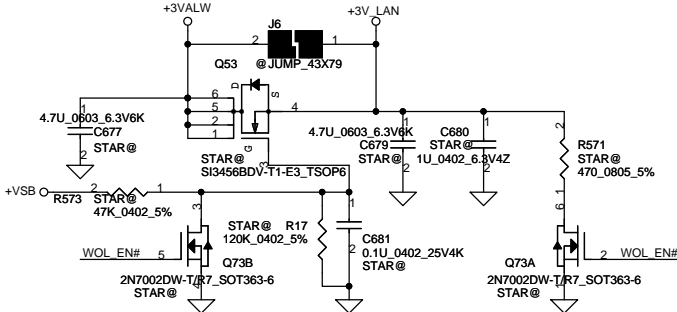
+3VALW TO +3VS



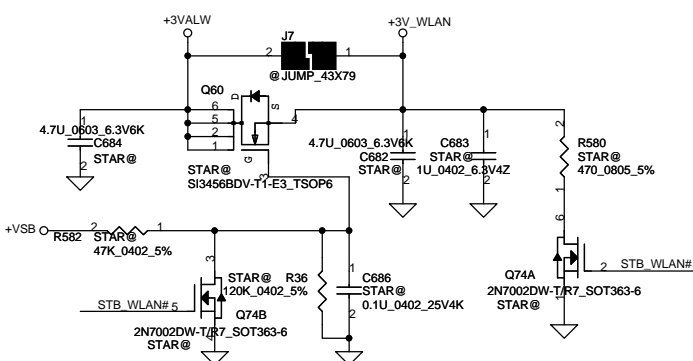
+3VALW TO +3V_SB



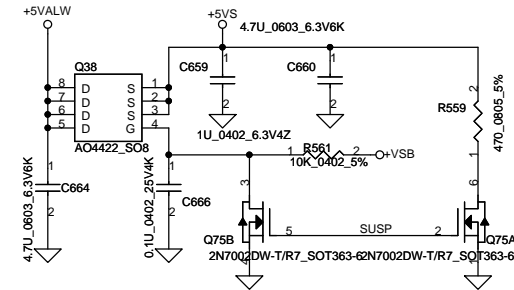
+3VALW TO +3V_LAN



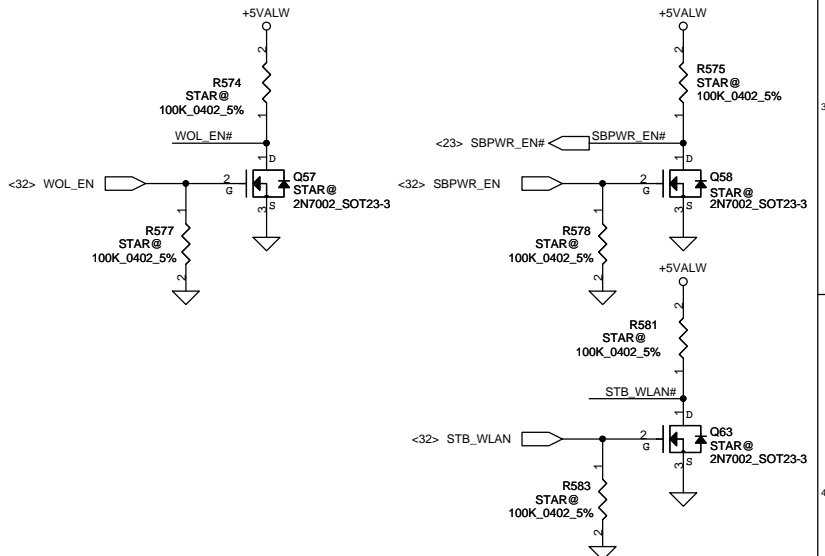
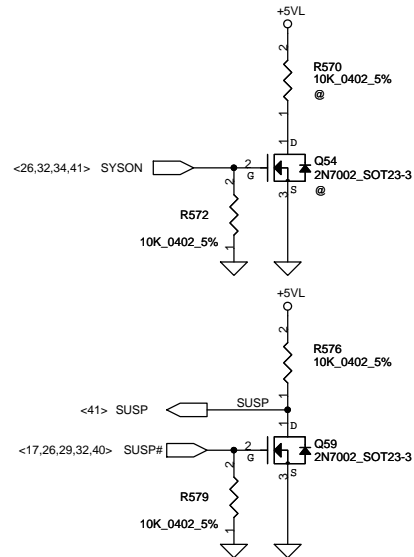
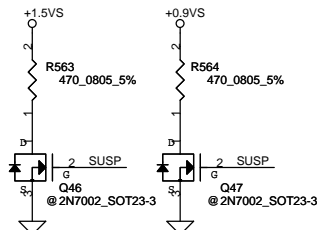
+3VALW TO +3V_WLAN



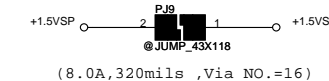
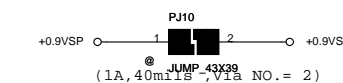
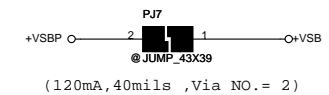
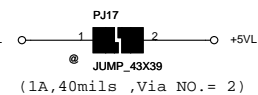
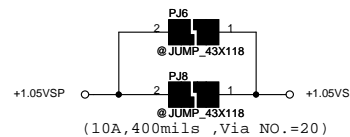
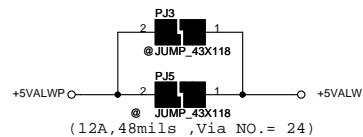
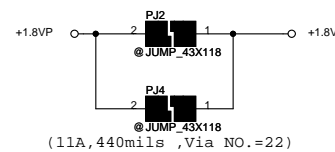
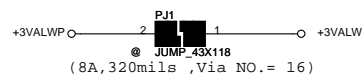
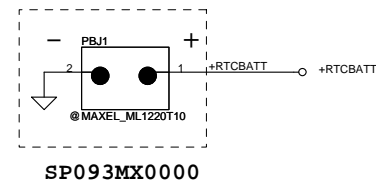
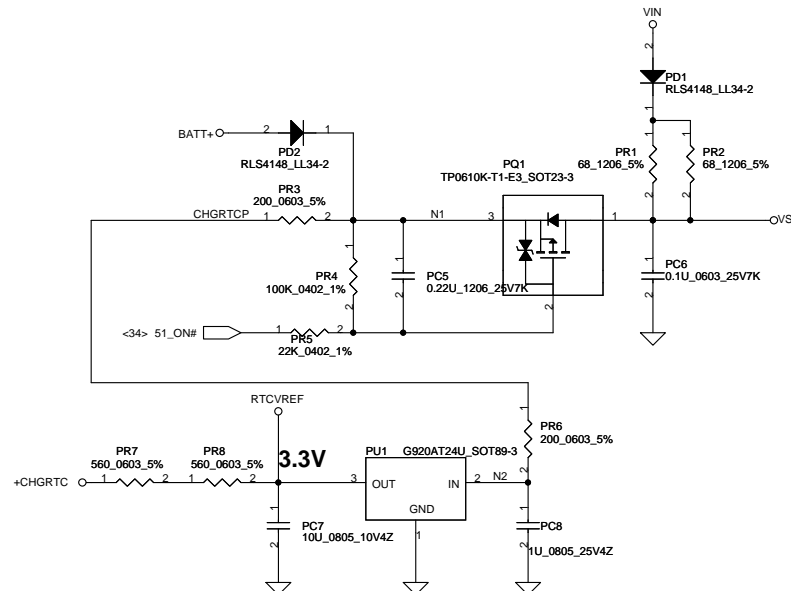
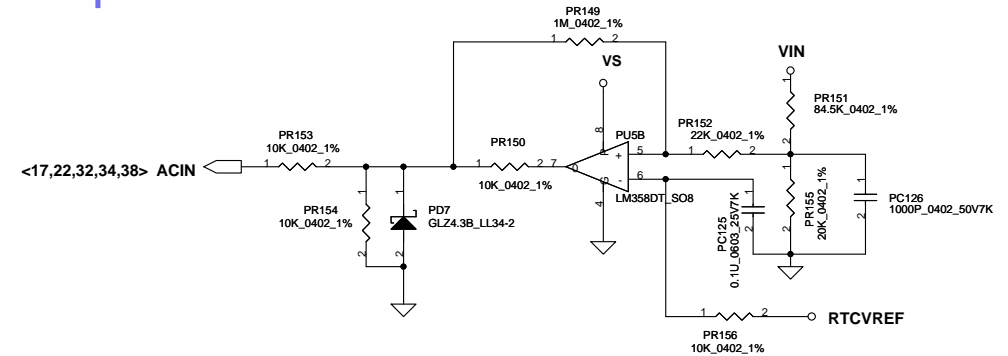
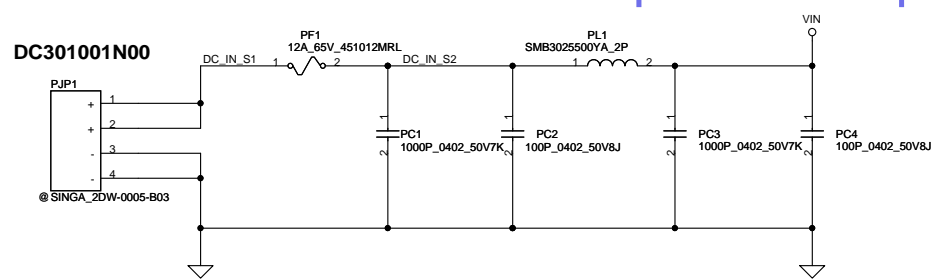
+5VALW TO +5VS



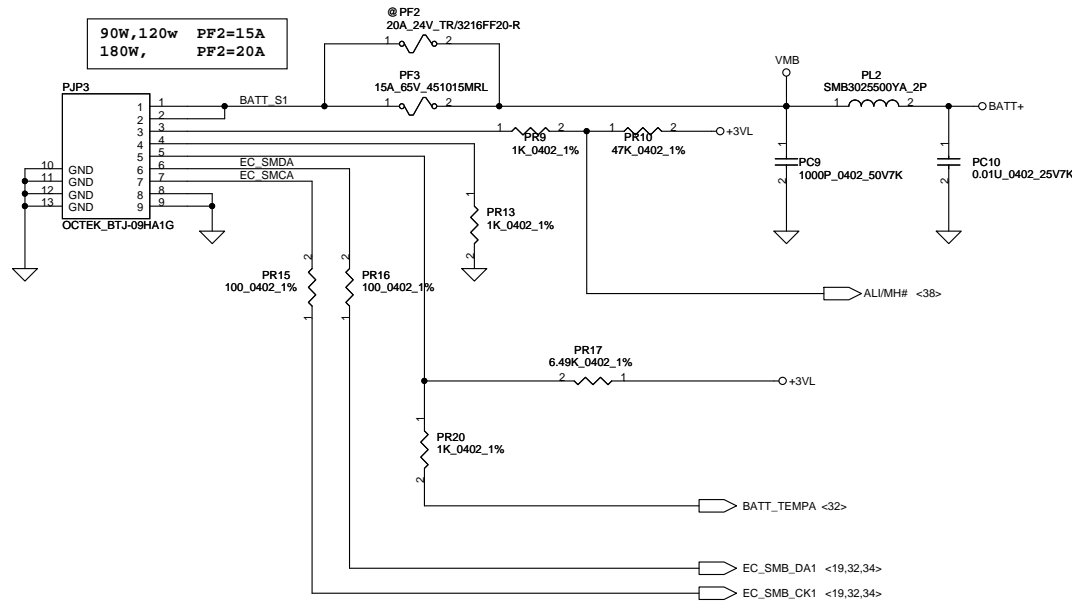
DVT2- Change +0.9V to +0.9VS



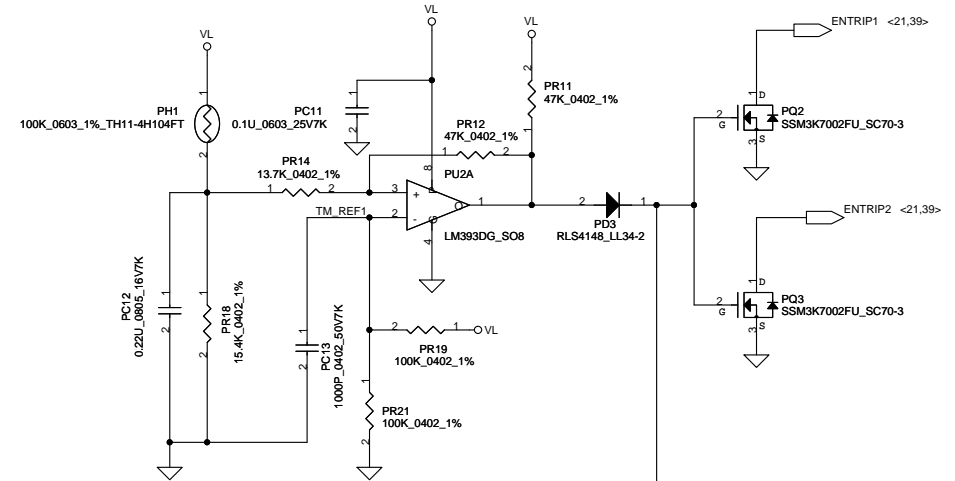
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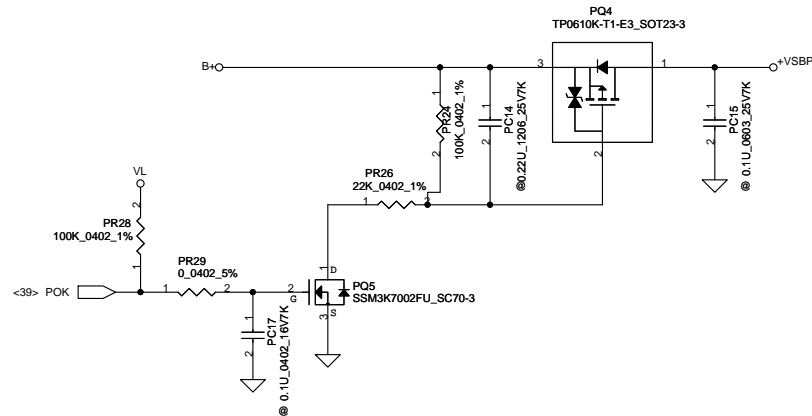
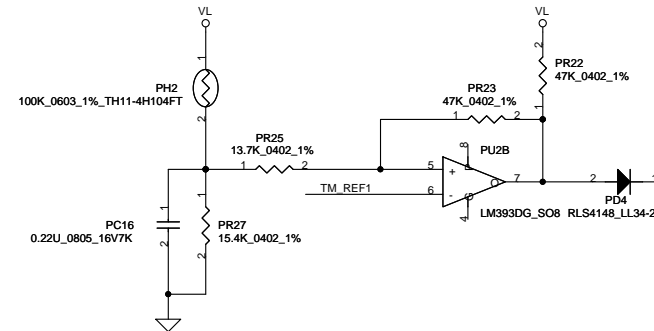
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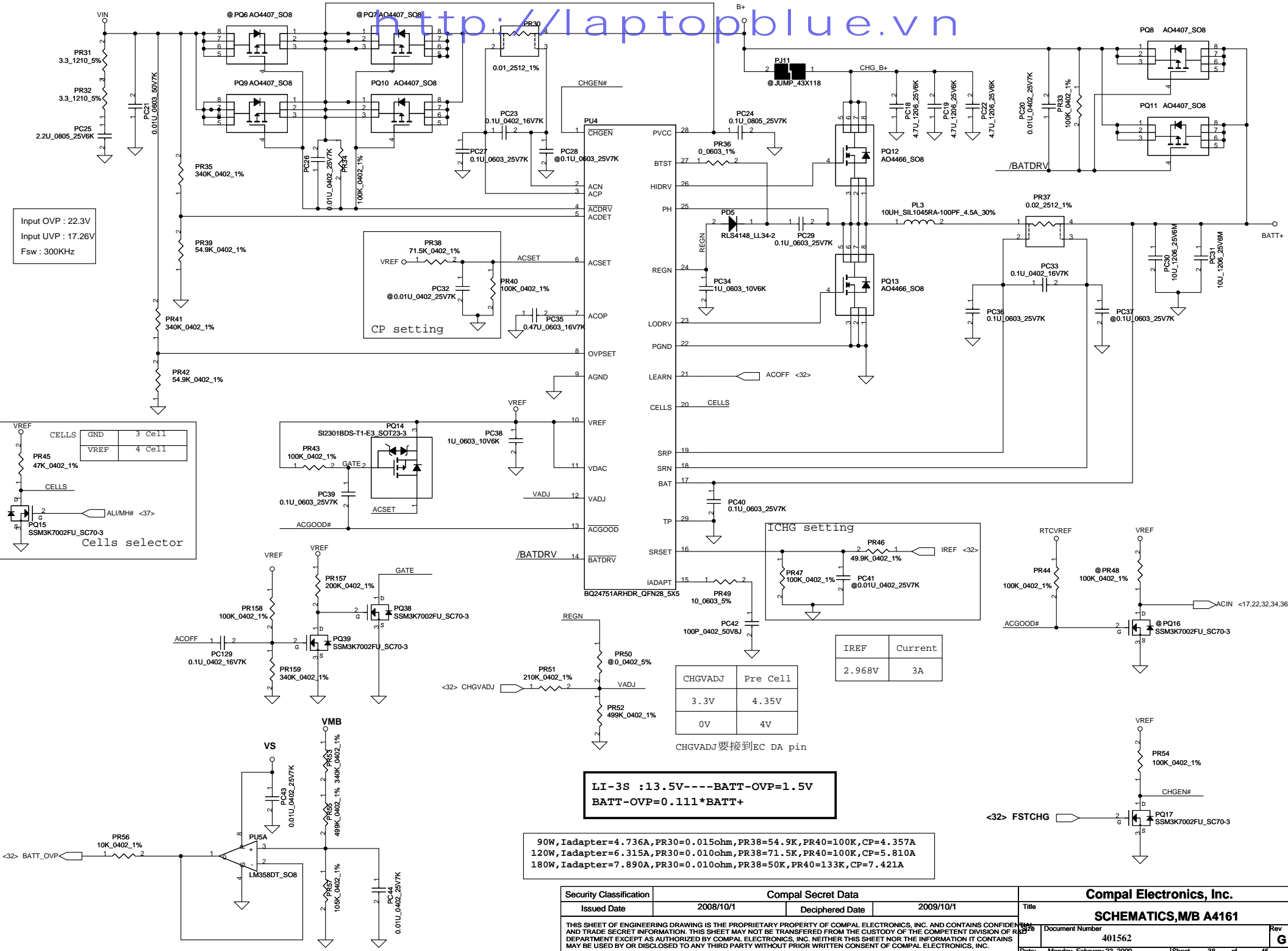


PH1 under CPU bottom side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 92 degree C
Recovery at 56 degree C





Input OVP : 22.3V
Input UVP : 17.26V
Fsw : 300KHz

Cells selector

| VREF | CELLS |
|------|--------|
| GND | 3 Cell |
| VREF | 4 Cell |

PR45 47K_0402_1%
PC15 SSM3K7002FU_SC70-3
ALIMH# <37>

CP setting

PR38 71.5K_0402_1%
PC32 0.01U_0402_25V7K
PR40 100K_0402_1%
PC35 0.47U_0603_16V7K

ICHG setting

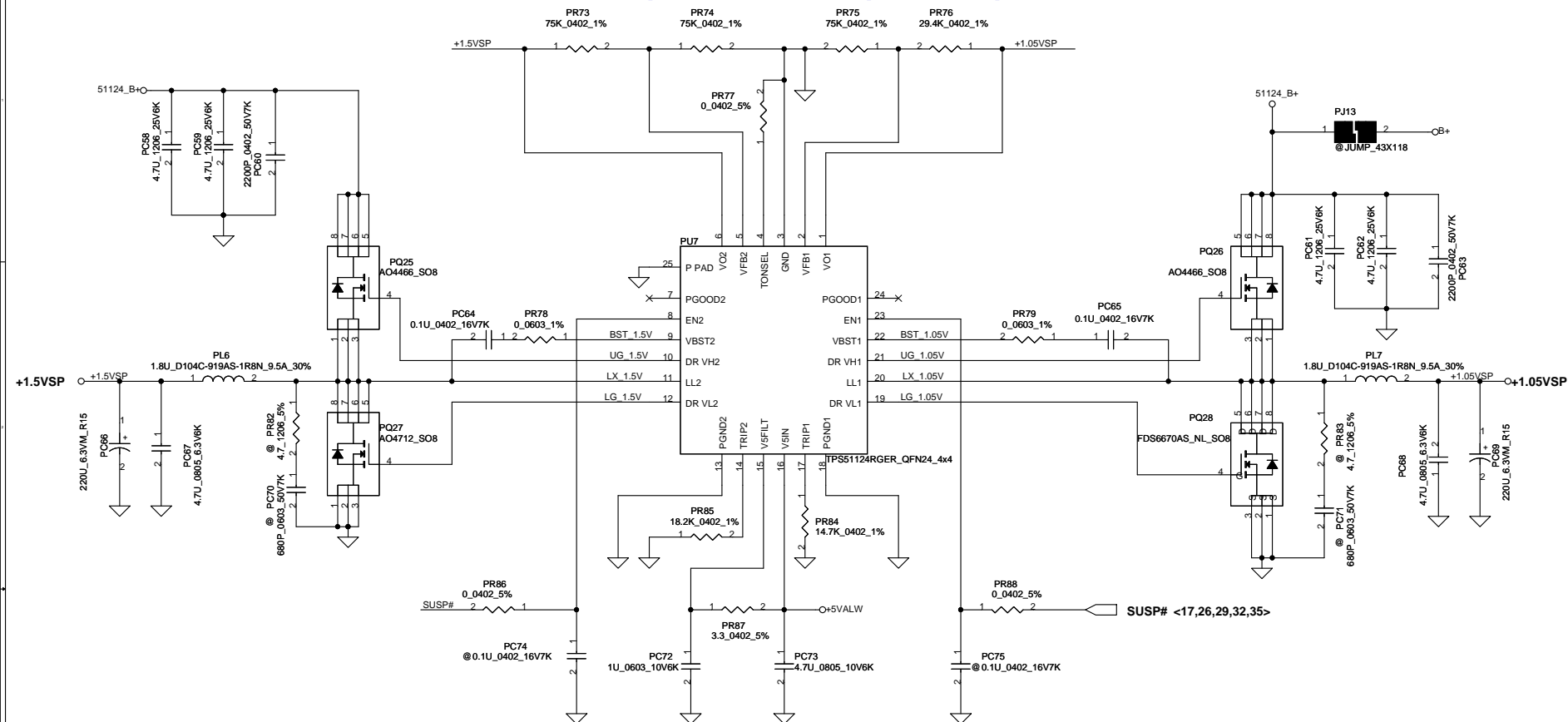
PR46 49.9K_0402_1%
PC41 0.01U_0402_25V7K

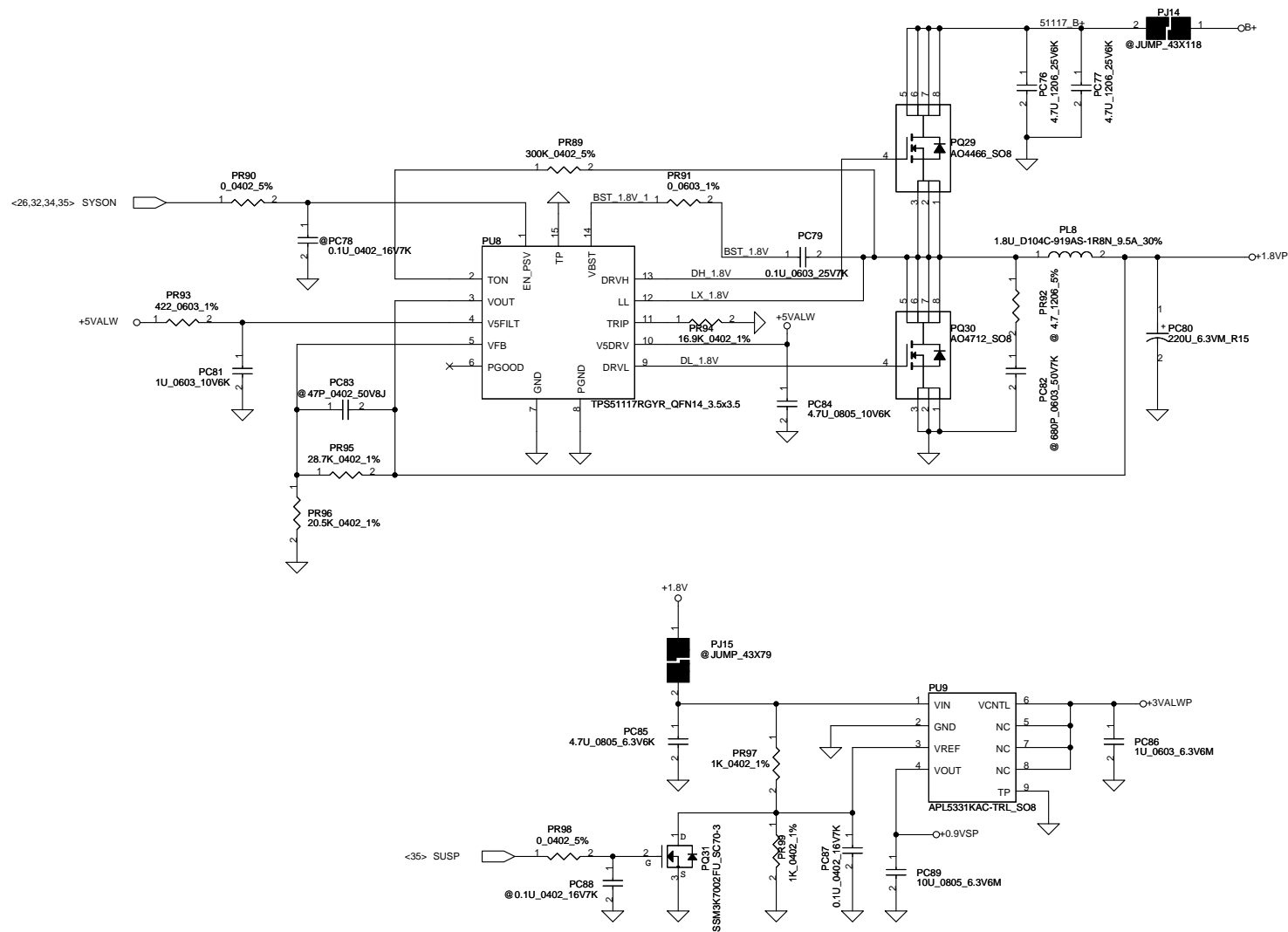
| CHGVADJ | Pre Cell |
|---------|----------|
| 3.3V | 4.35V |
| 0V | 4V |

| IREF | Current |
|--------|---------|
| 2.968V | 3A |

**LI-3S : 13.5V---BATT-OVP=1.5V
BATT-OVP=0.111*BATT+**

90W, Iadapter=4.736A, PR30=0.015ohm, PR38=54.9K, PR40=100K, CP=4.357A
120W, Iadapter=6.315A, PR30=0.010ohm, PR38=71.5K, PR40=100K, CP=5.810A
180W, Iadapter=7.890A, PR30=0.010ohm, PR38=50K, PR40=133K, CP=7.421A





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| NO | DATE | PAGE | MODIFICATION LIST | PURPOSE |
|----|----------|------|--|--|
| 1 | 11/01'07 | | Release | |
| 2 | 12/25'07 | P.36 | Add AC-IN schematic | Add AC-IN detect function |
| | | P.38 | move PR44 | Add AC-IN pull-higher resistor |
| | | P.39 | PR66,PR67,PC127,PC128 | Add 3VALWP and 5VALWP snubber |
| 3 | 2/13'08 | P.38 | change PR51, PR52 | Change CHGVADJ voltage |
| | | P.42 | Change PR113,PR127,PR117,PC101,PR129,PC110 | Add CPU boost and snubber for EMI request |
| | | | Change PQ33,PQ34,PQ36,PQ37 | Change low side Mosfet |
| 4 | 3/5'08 | P.38 | Add PQ38,PQ39,PR159,PC129,PR157,PR158 | Add wrong adapter protection function |
| 5 | 3/23'08 | P.39 | Add PR160 | Add TPS51125/RT8205A p2p |
| | | P.37 | Change +3VALW->+3VL on Battery port | Change battery temperature action |
| 6 | 4/28'08 | P.36 | Delete PD6,change PR150 and PR153 | For ACIN detect to meet wrong adapter function |
| | | P.39 | Change +3VL->B+ in PU6 pin13 | Add 2nd source RT8205A P2P |
| | | P.39 | Add PR67,PC127,PR66,PC128 | GPS noise |
| | | P.40 | Add PR82,PR83,PC70,PC71 | GPS noise |
| | | P.41 | Add PR92,PC82 | GPS noise |
| 6 | 6/219'08 | P.38 | Change PR45 from 100K_0402_1% to 47K_0402_1%(SD034470280) | For ACIN detect to meet wrong adapter function |

| | | | | | |
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45@ Part

PJP1 45@
DC-JACK

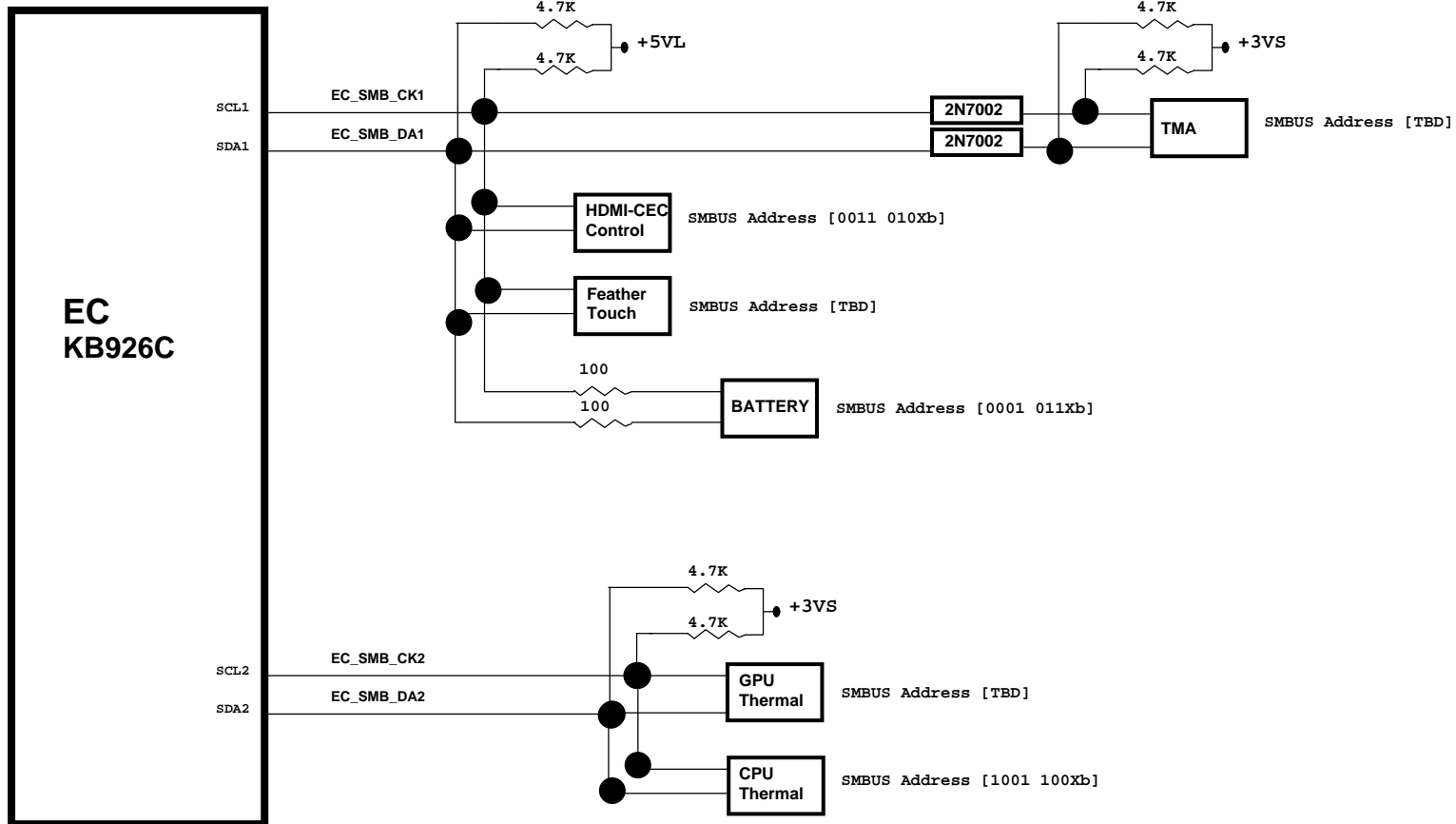
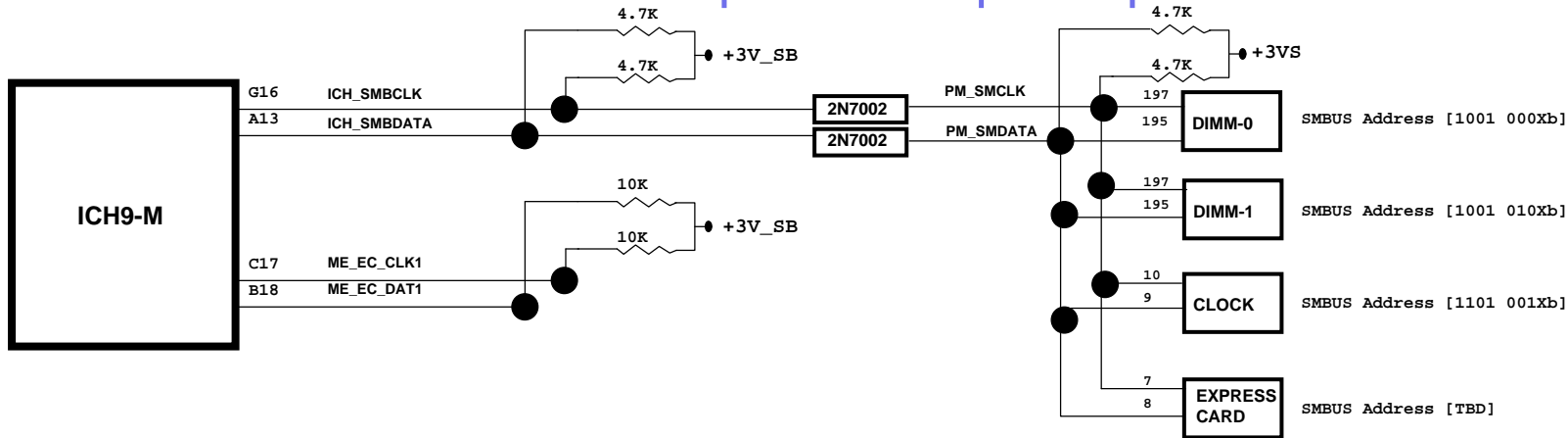
PCB

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LA-4161P DAZ BOM--DAZ04G00101

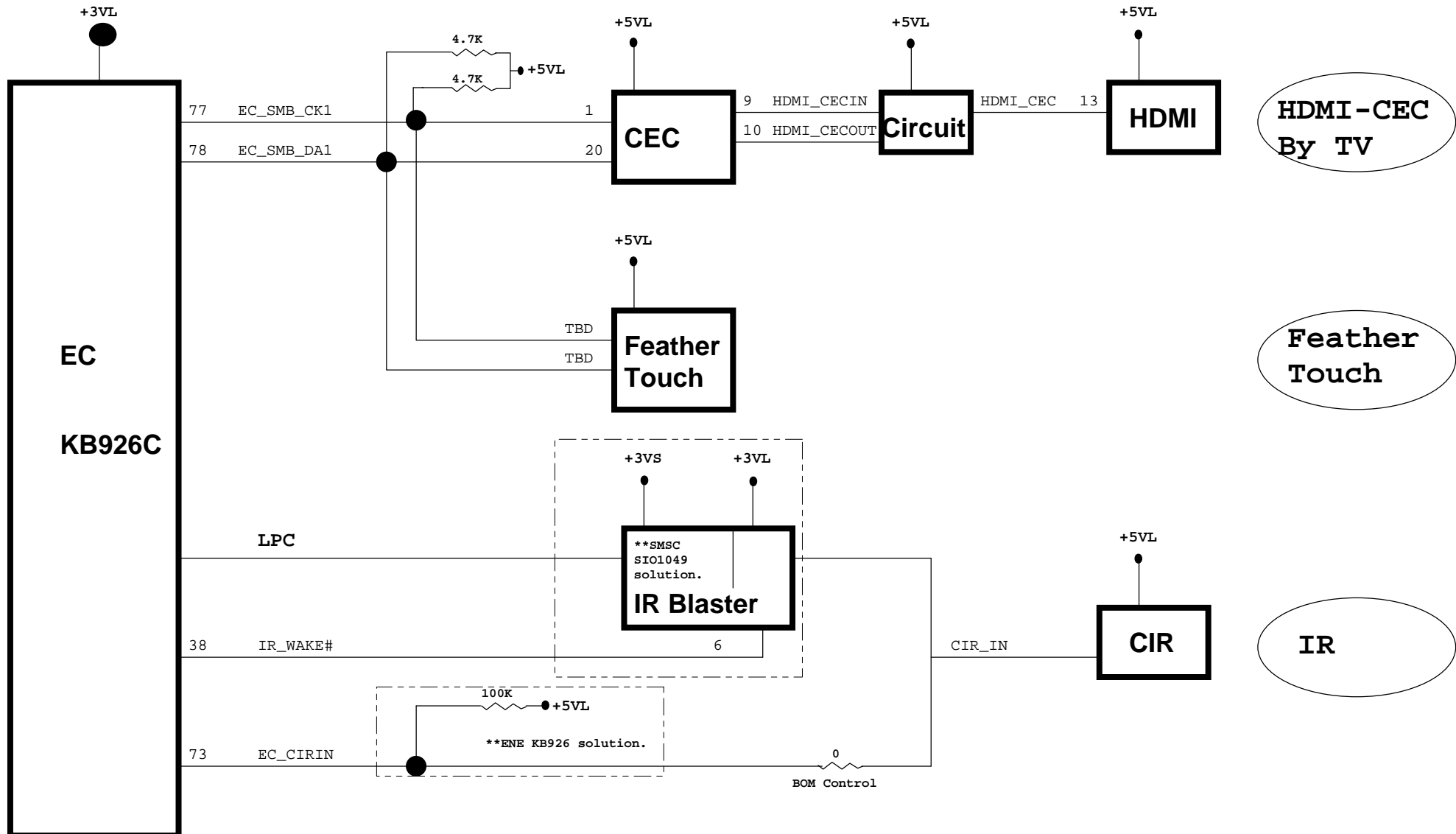
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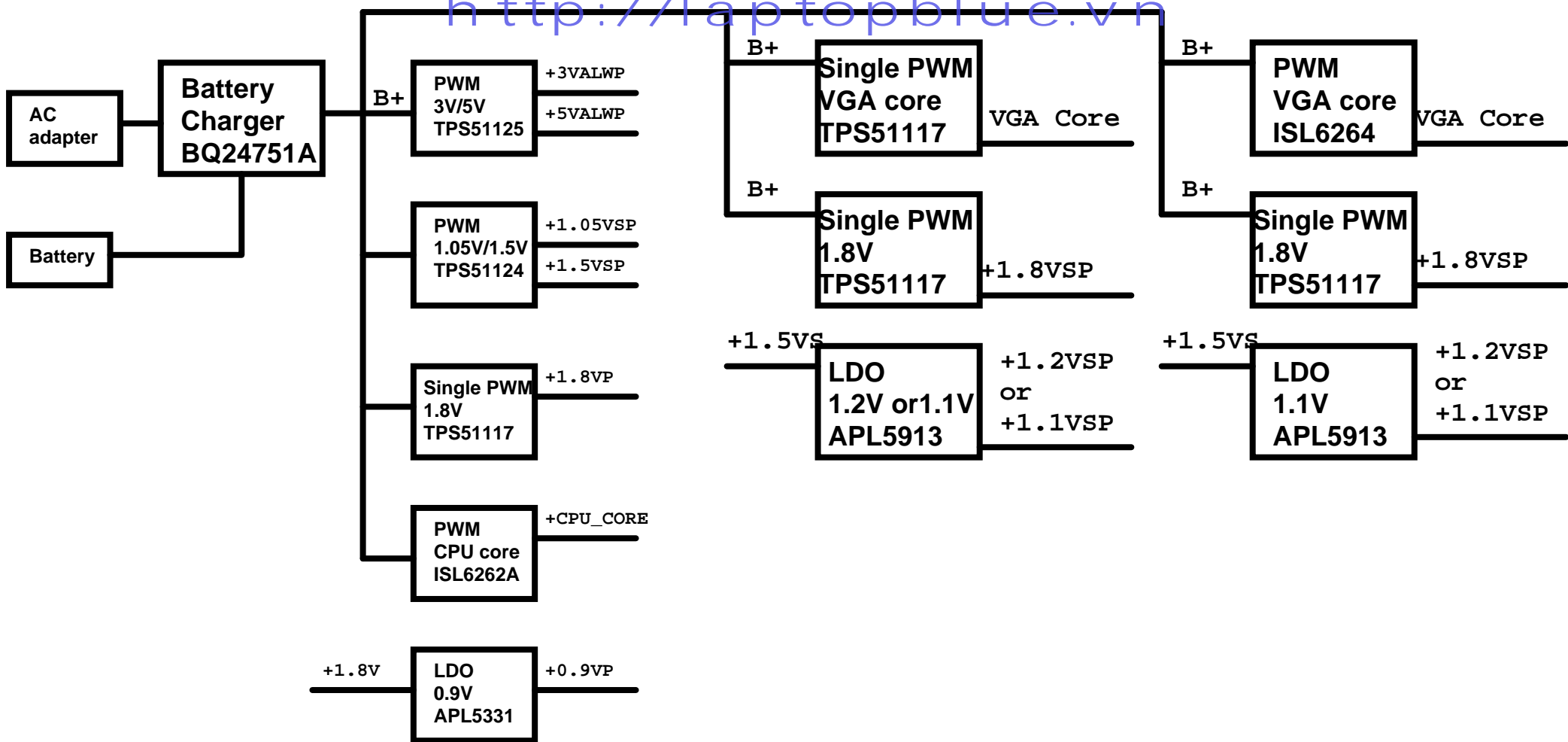
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NB-R3
- U3 GMLR3@
NB-R3

[illegible]



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