

EAT20 (Sakhir 10GC)

LA-2492 Schematics Document

Intel Dothan / AlvisoPM / DDR-1 / ICH6-M / Select Bay

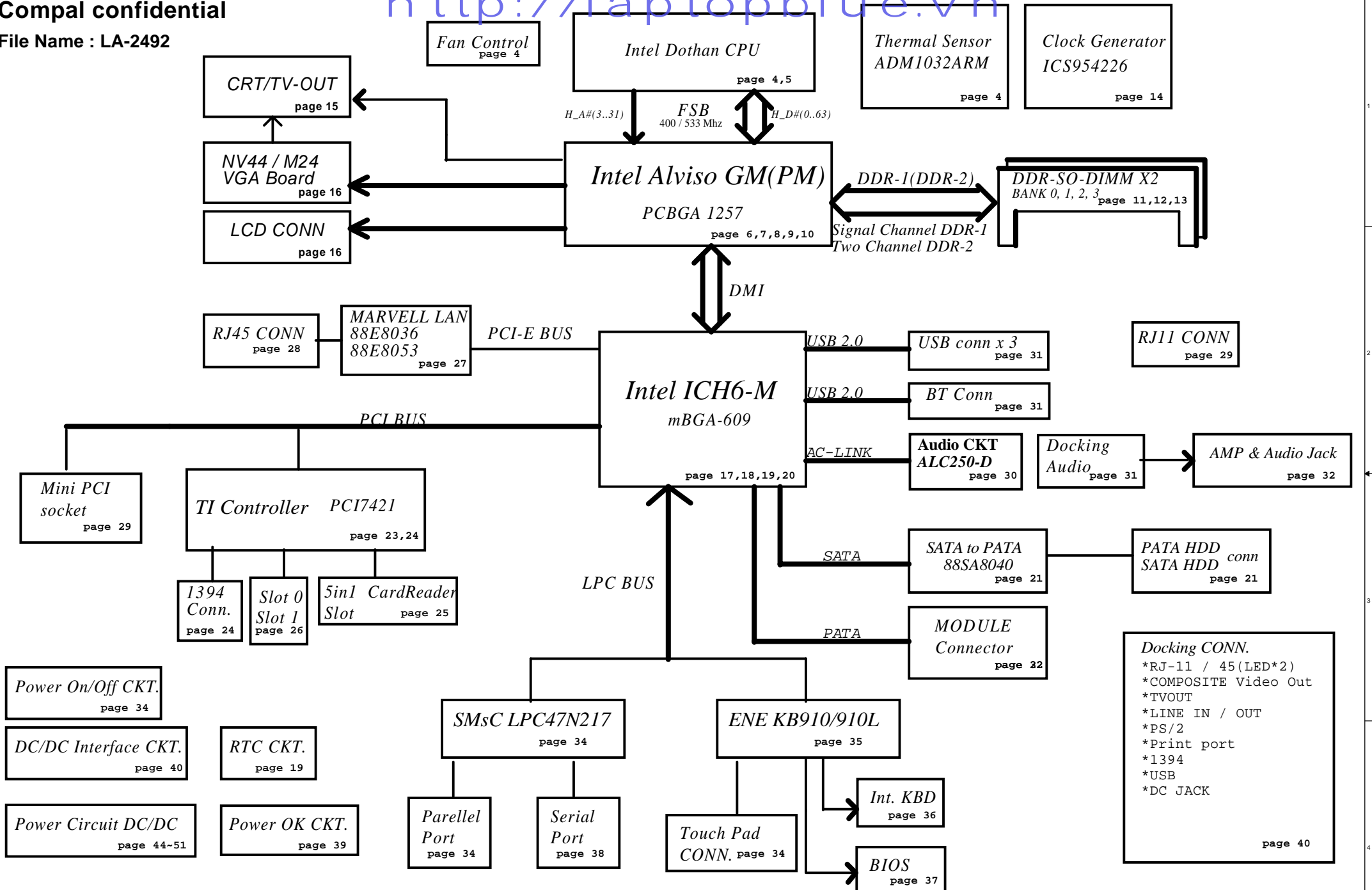
(nVIDIA NV43M & NV44M/ ATi M22 & M24)

2004 / 12 / 22

Rev:1.0

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+DDRVTT	1.25V switched power rail for DDR terminator	ON	OFF	OFF
+1.5VALW	1.5V always on power rail	ON	ON	ON*
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+DDRVCC	2.5V power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+5VCD	5V switched power rail for Direct CD	ON	OFF	OFF
+5VMOD	5V switched power rail for Module Bay	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD20	2	PIRQA/PIRQB
1394	AD20	2	PIRQA/PIRQB
SD	AD20	2	PIRQA/PIRQB
Mini-PCI	AD18	1	PIRQG/PIRQH

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 110X b
EEPROM(24C16/02)	1010 000X b	2nd Battery	1001 011X b
(24C04)	1011 000Xb	Docking	1010 000X b

ICH6M SM Bus address

Device	Address
Clock Generator (ICS 952623)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 001Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	NC
2	0.2
3	1.0
4	
5	
6	
7	

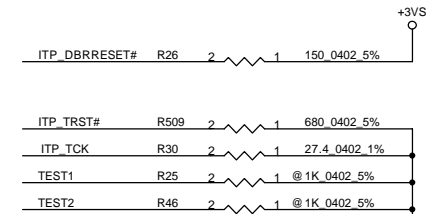
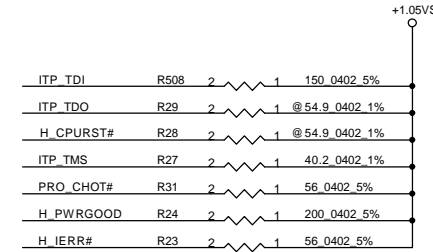
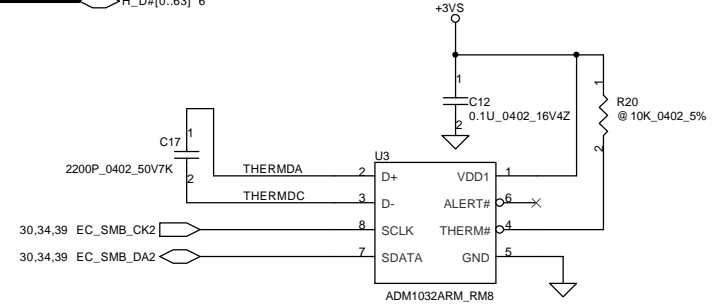
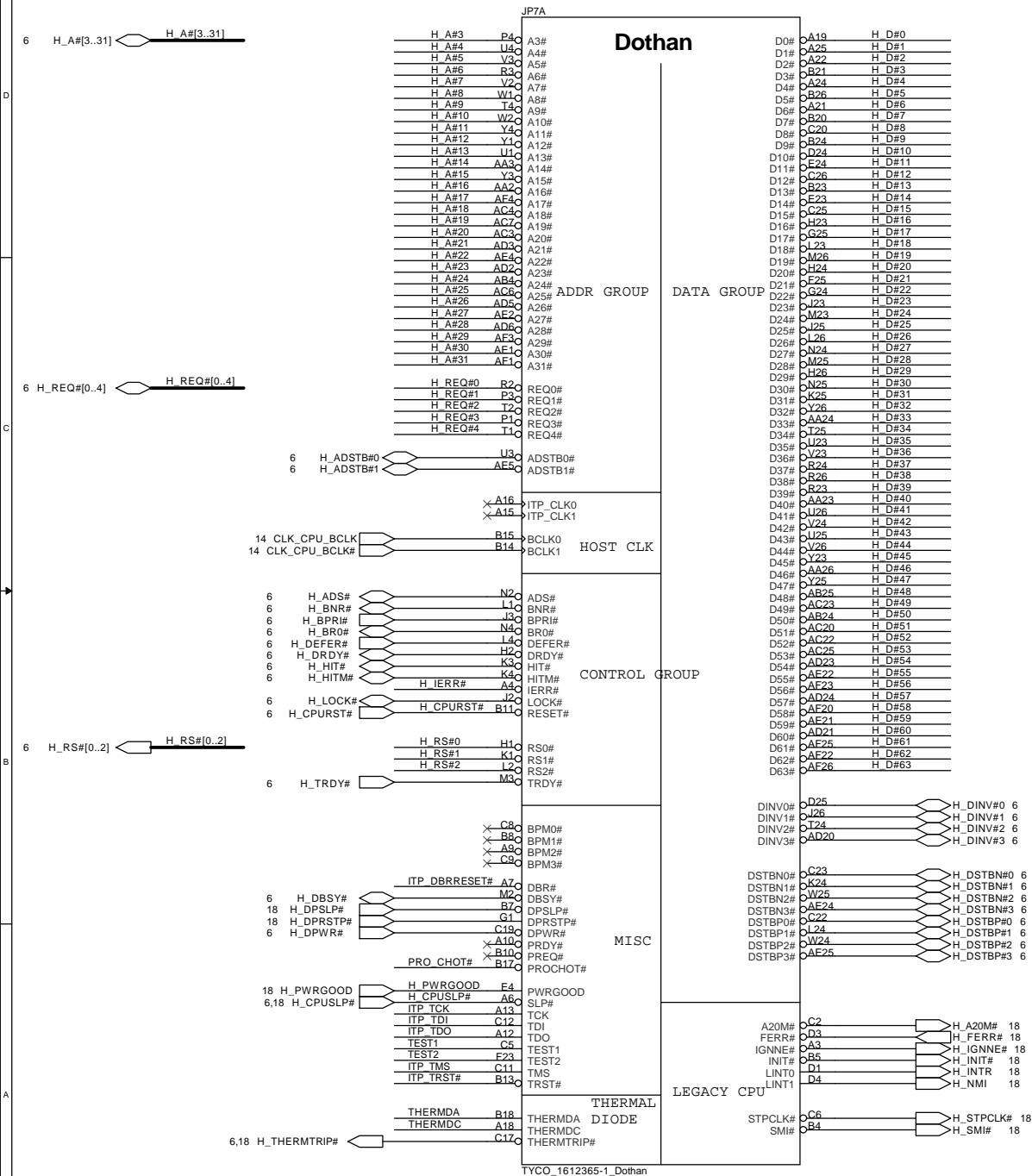
SKU ID Table

SKU_ID_CHECK_0	SKU_ID_CHECK_1	7	6	5
		1-Button	3-Buttons	7-Buttons
0	10	1		0
1	10C	3	12	2
2	10G	5		4
3	10GC	7	13	6
4	10J	11		10
5				
6				

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H_D#[0..63] 6

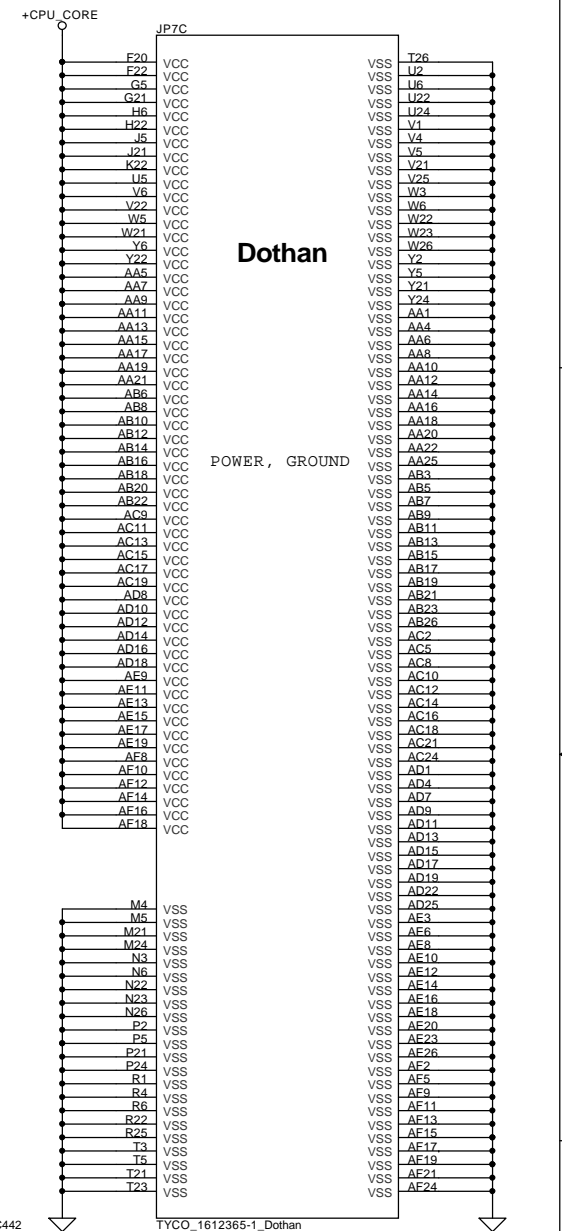
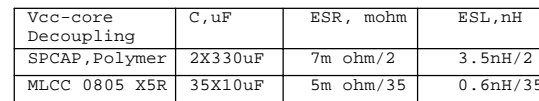
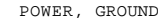


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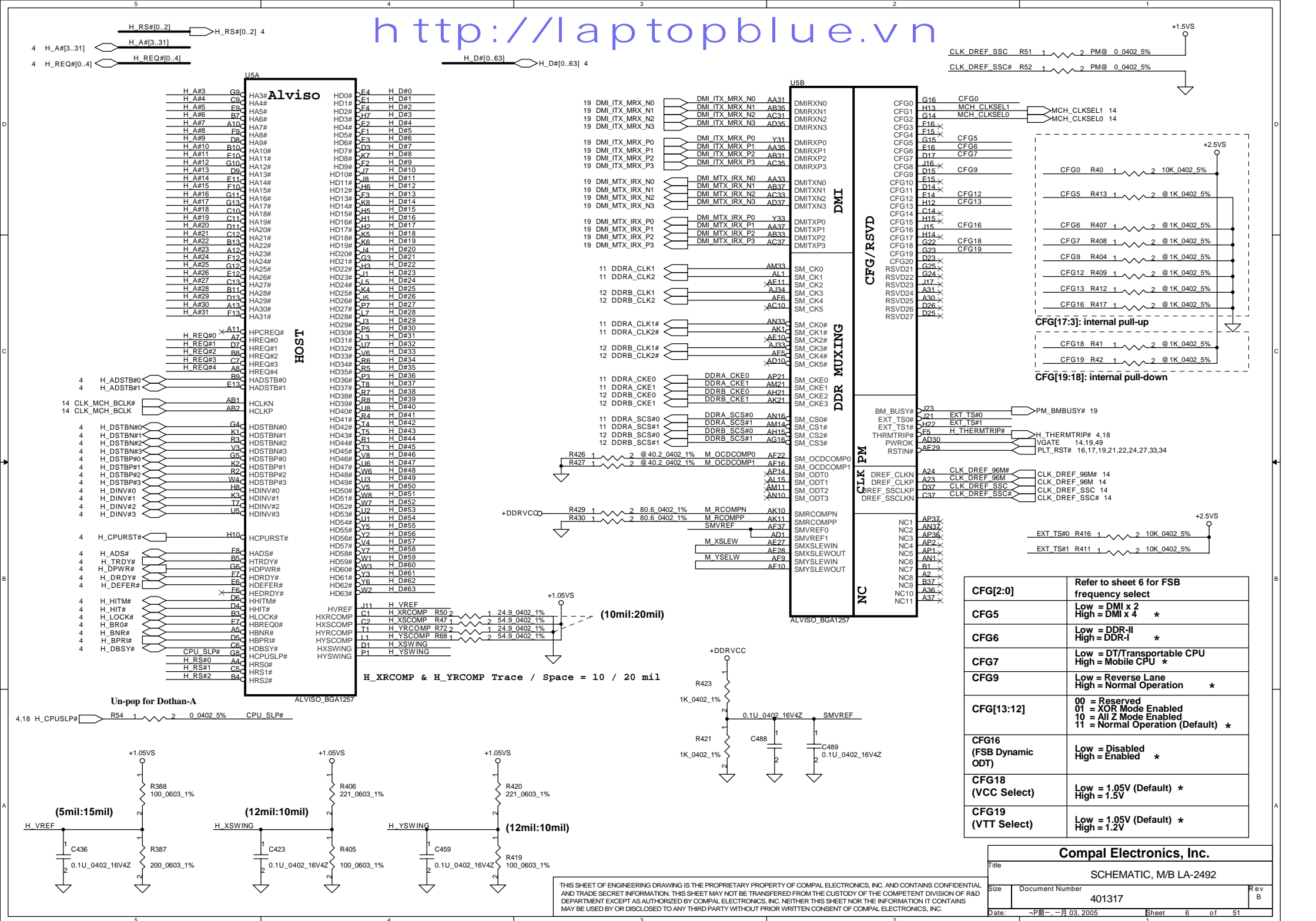
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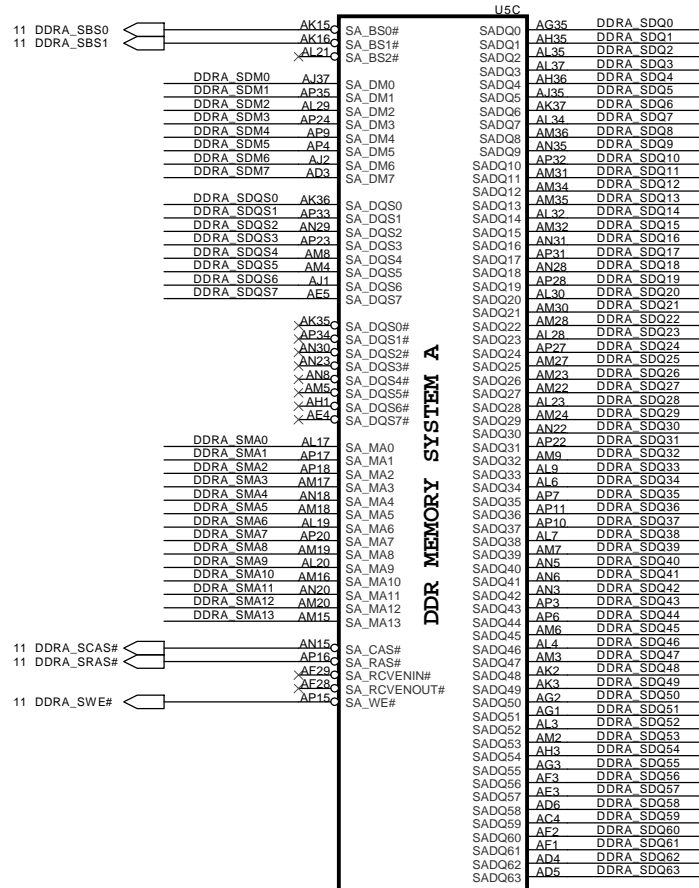


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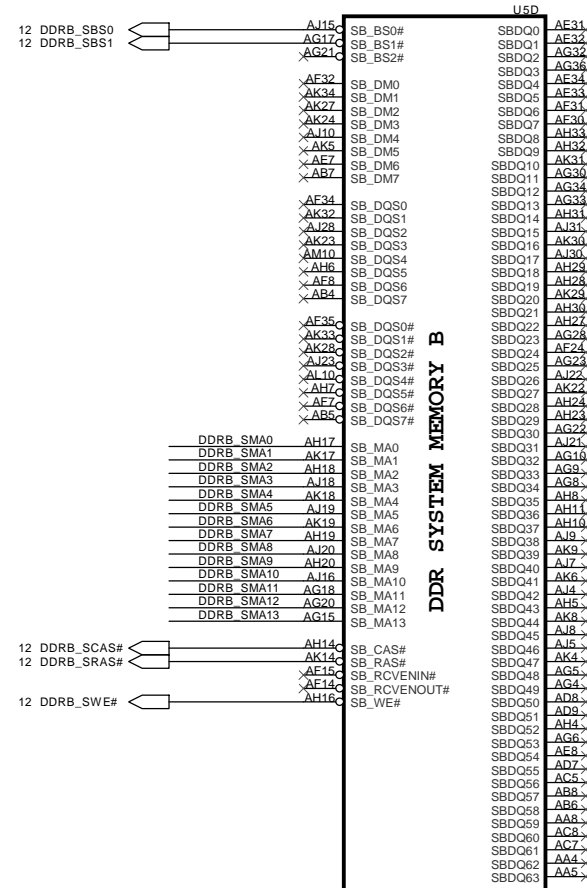


11 DDRA_SDQ[0..63] ← DDRA_SDQ[0..63]
11 DDRA_SDM[0..7] ← DDRA_SDM[0..7]
11 DDRA_SDQS[0..7] ← DDRA_SDQS[0..7]
11 DDRA_SMA[0..13] ← DDRA_SMA[0..13]

12 DDRB_SMA[0..13] ← DDRB_SMA[0..13]



ALVISO_BGA1257

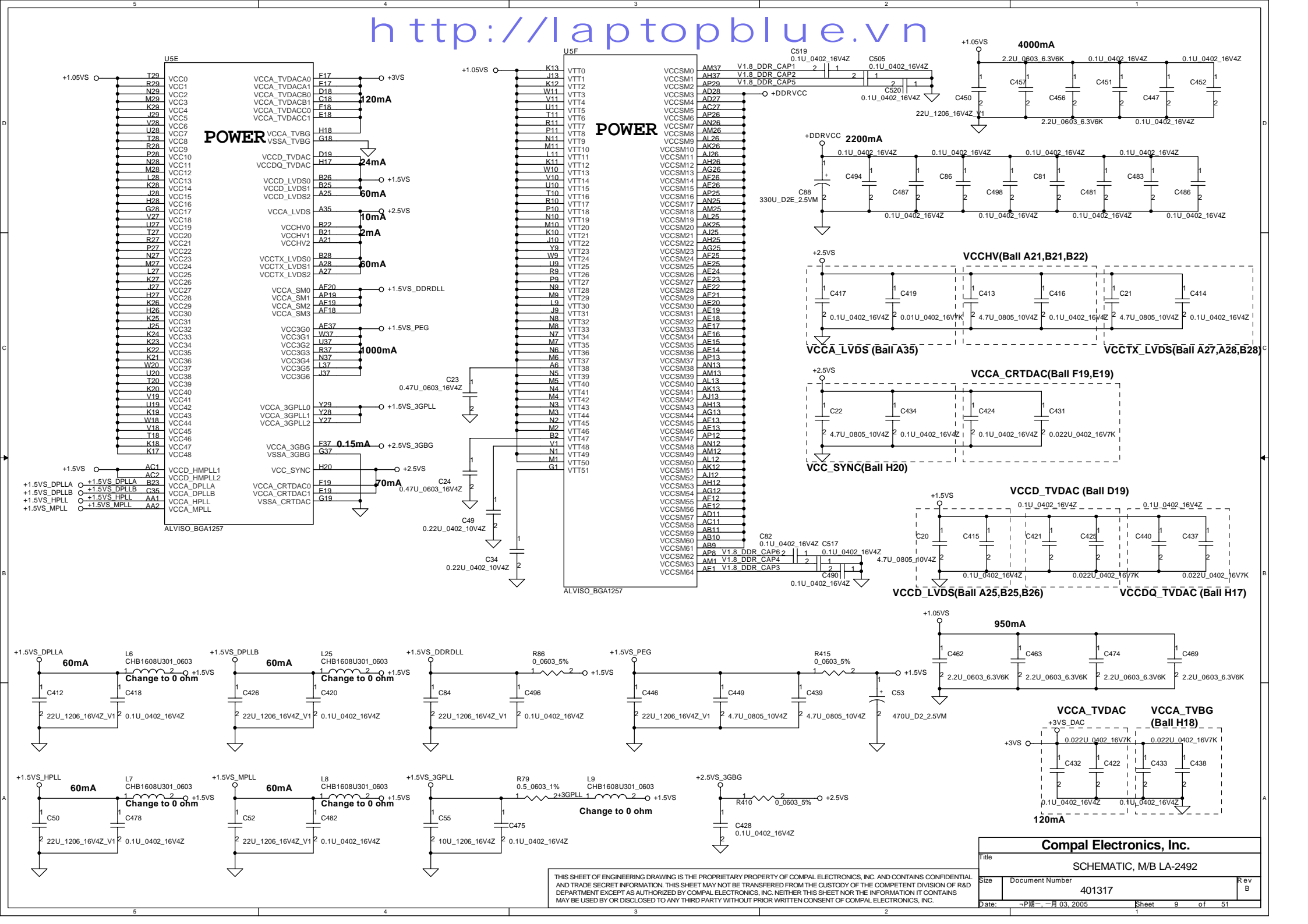


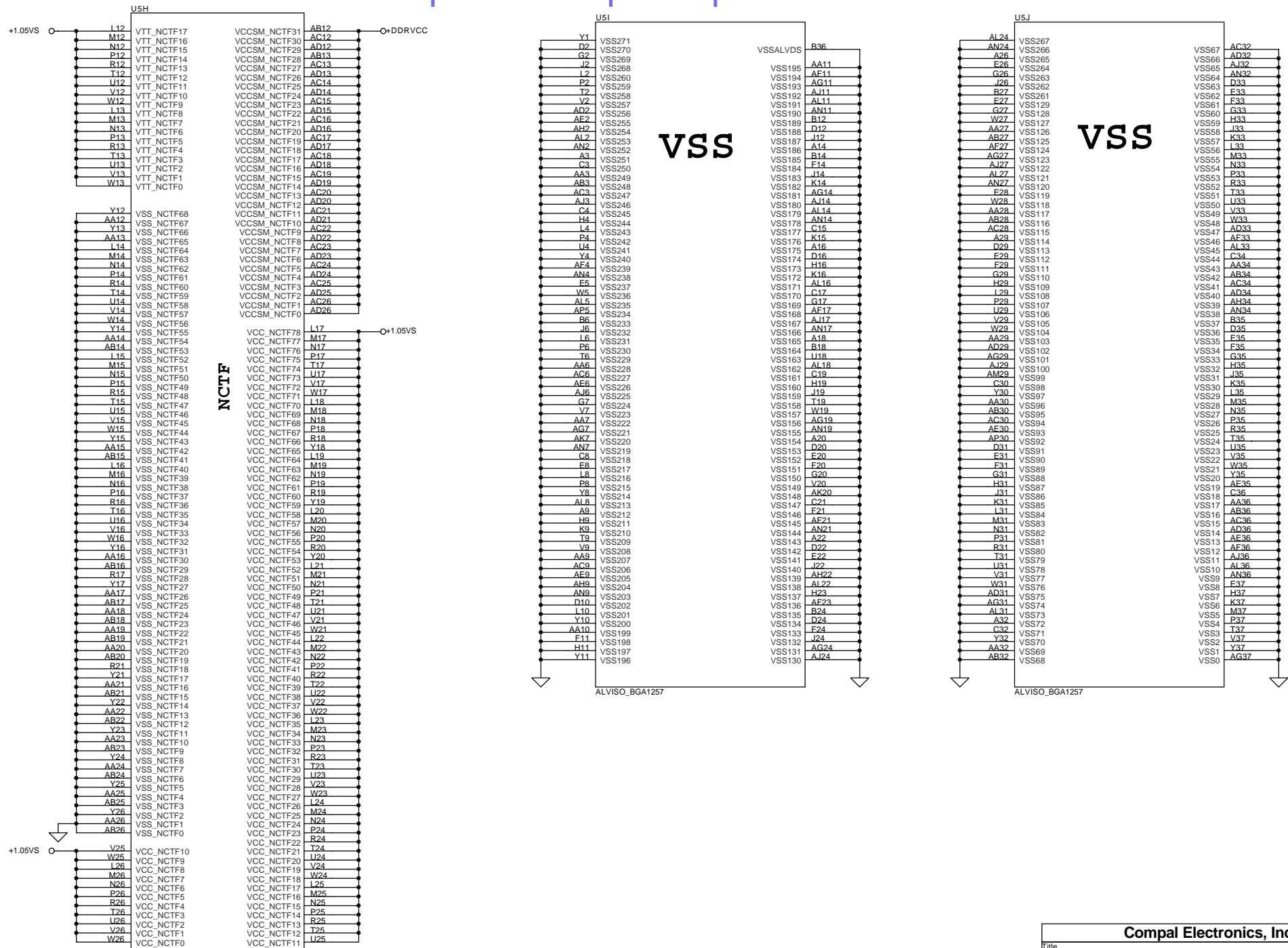
ALVISO_BGA1257

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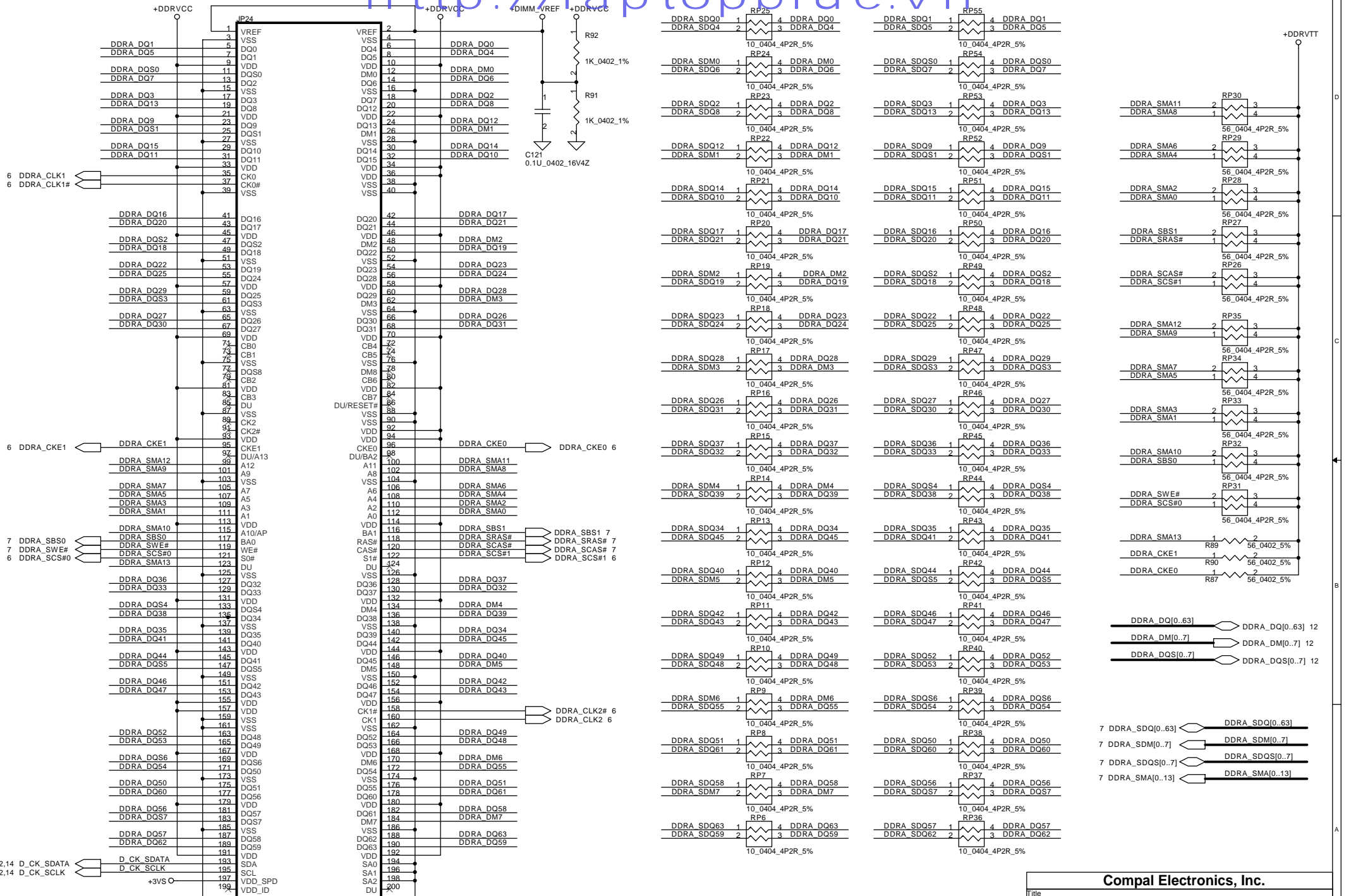
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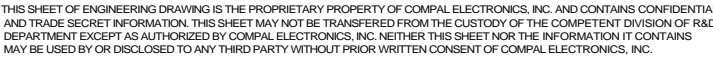
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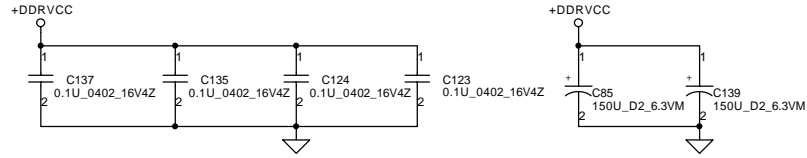
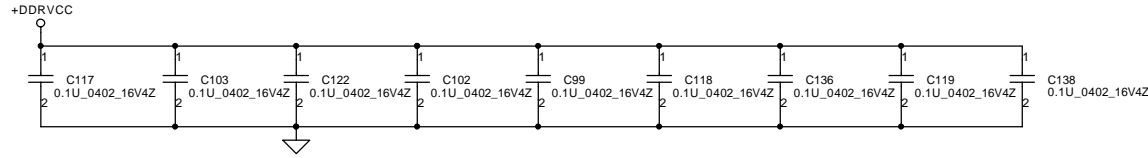


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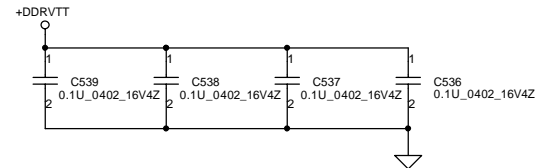
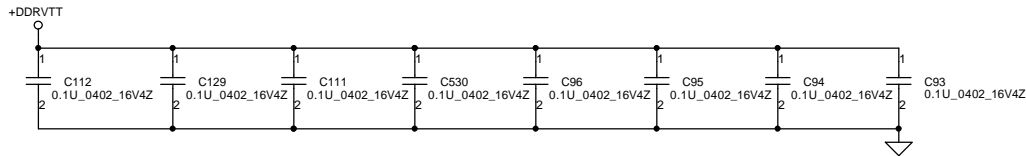
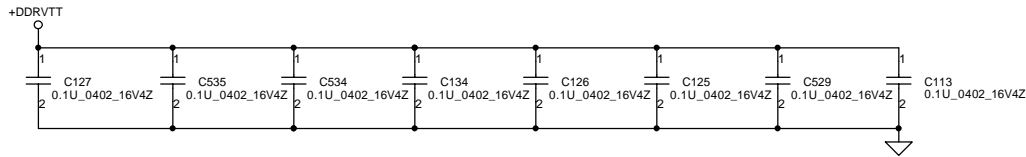
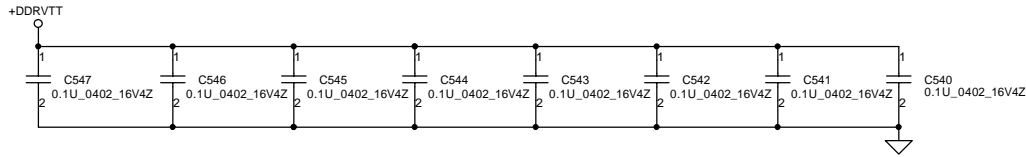
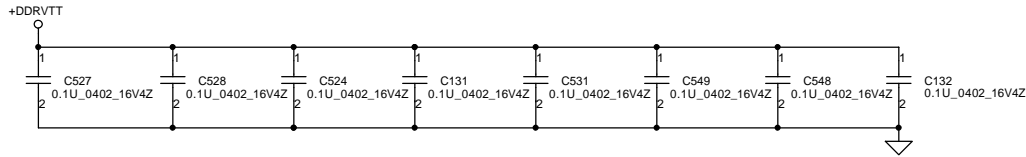
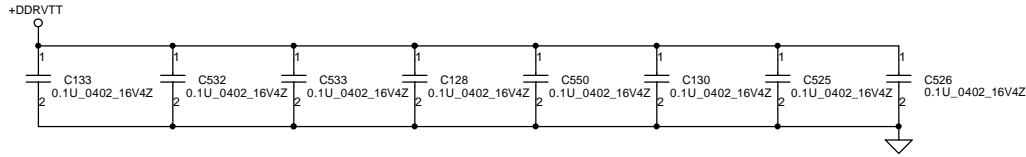
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Layout note :
Distribute as close as possible to DDR-SODIMM.



Layout note :
Place one cap close to every 2 pull up resistors termination to +1.25V



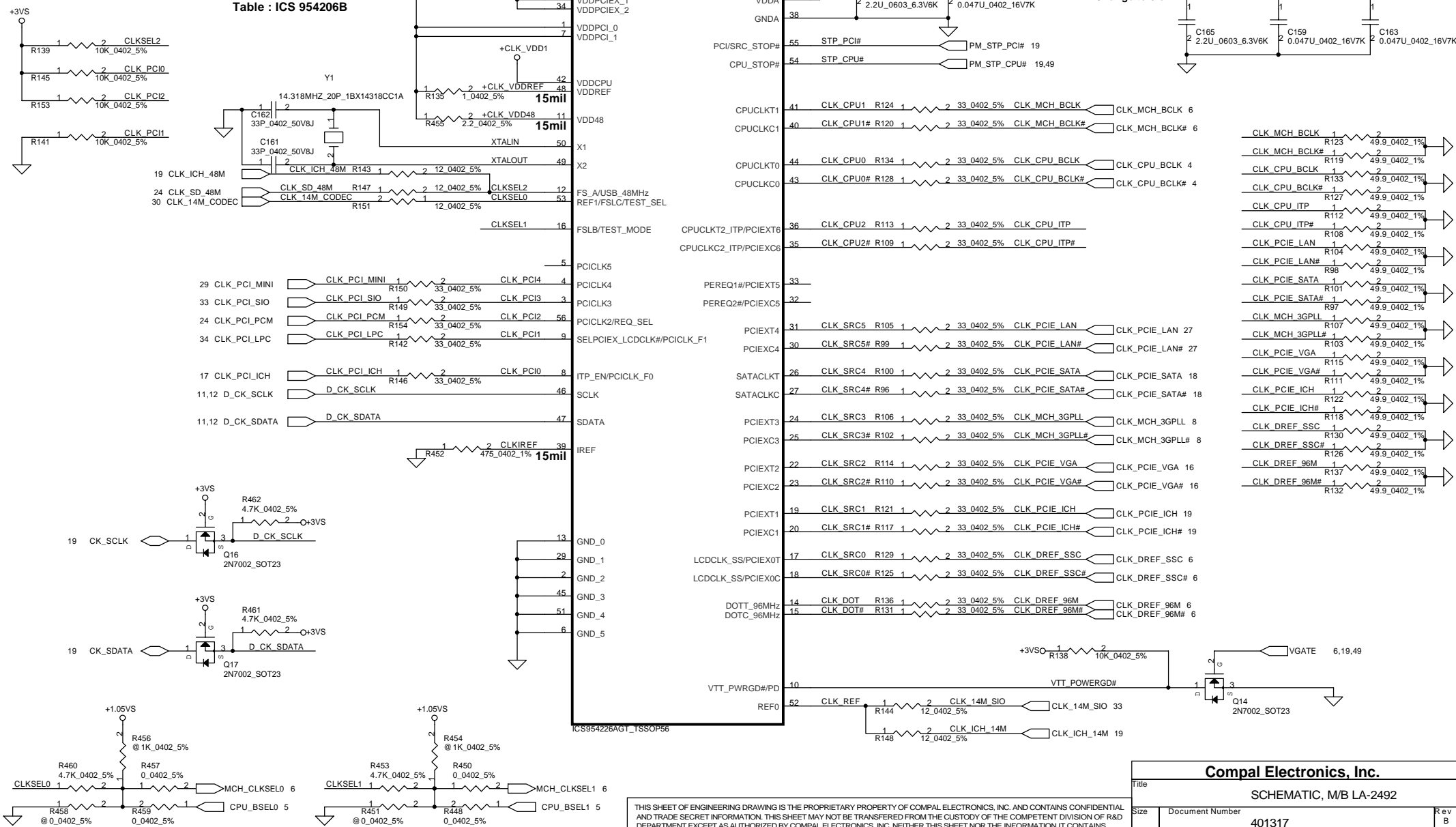
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FSC CLKSEL0	FSB CLKSEL1	FSA CLKSEL2	CPU MHz	SRC MHz	PCI MHz
1	0	1	100	100	33.3
0	0	1	133	100	33.3
0	1	1	166	100	33.3
0	1	0	200	100	33.3

Table : ICS 954206B

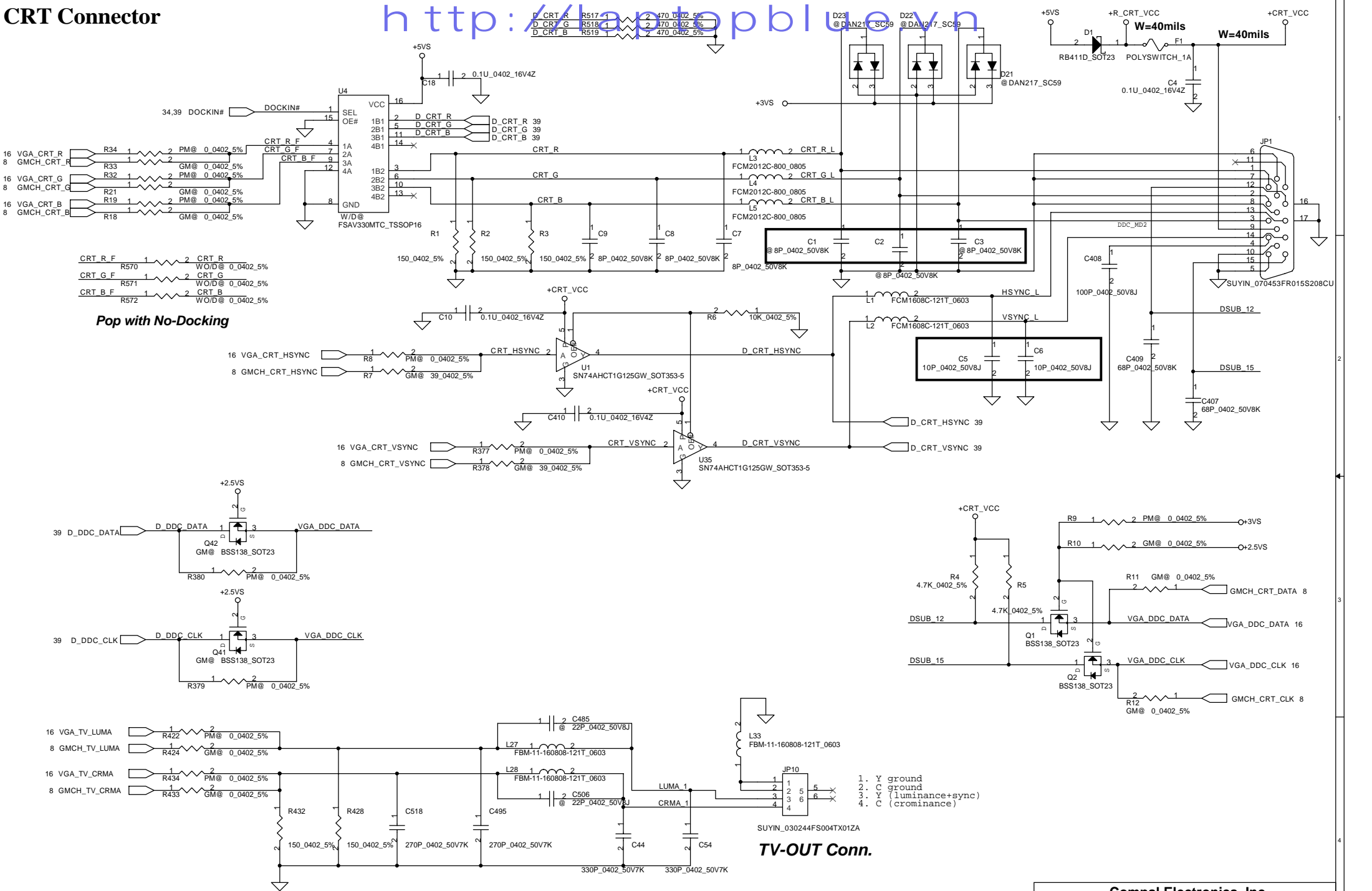


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CRT Connector

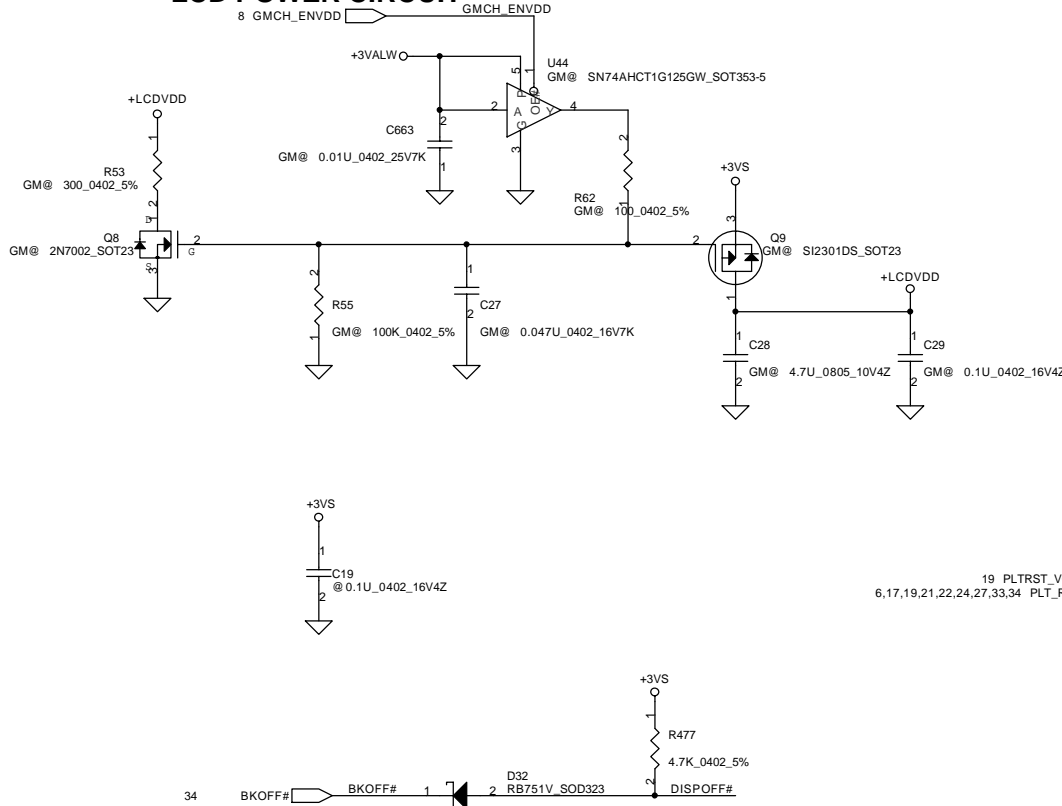
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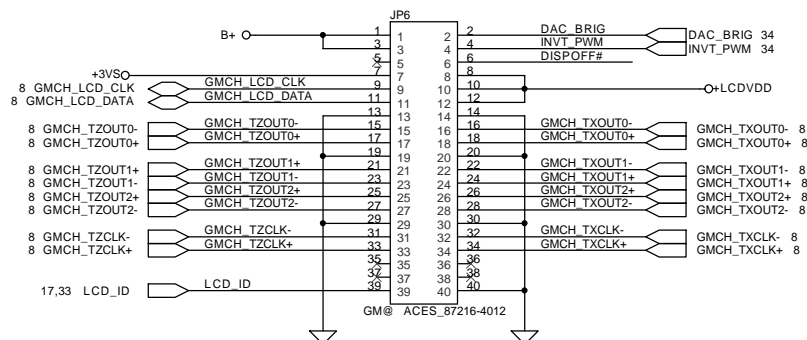
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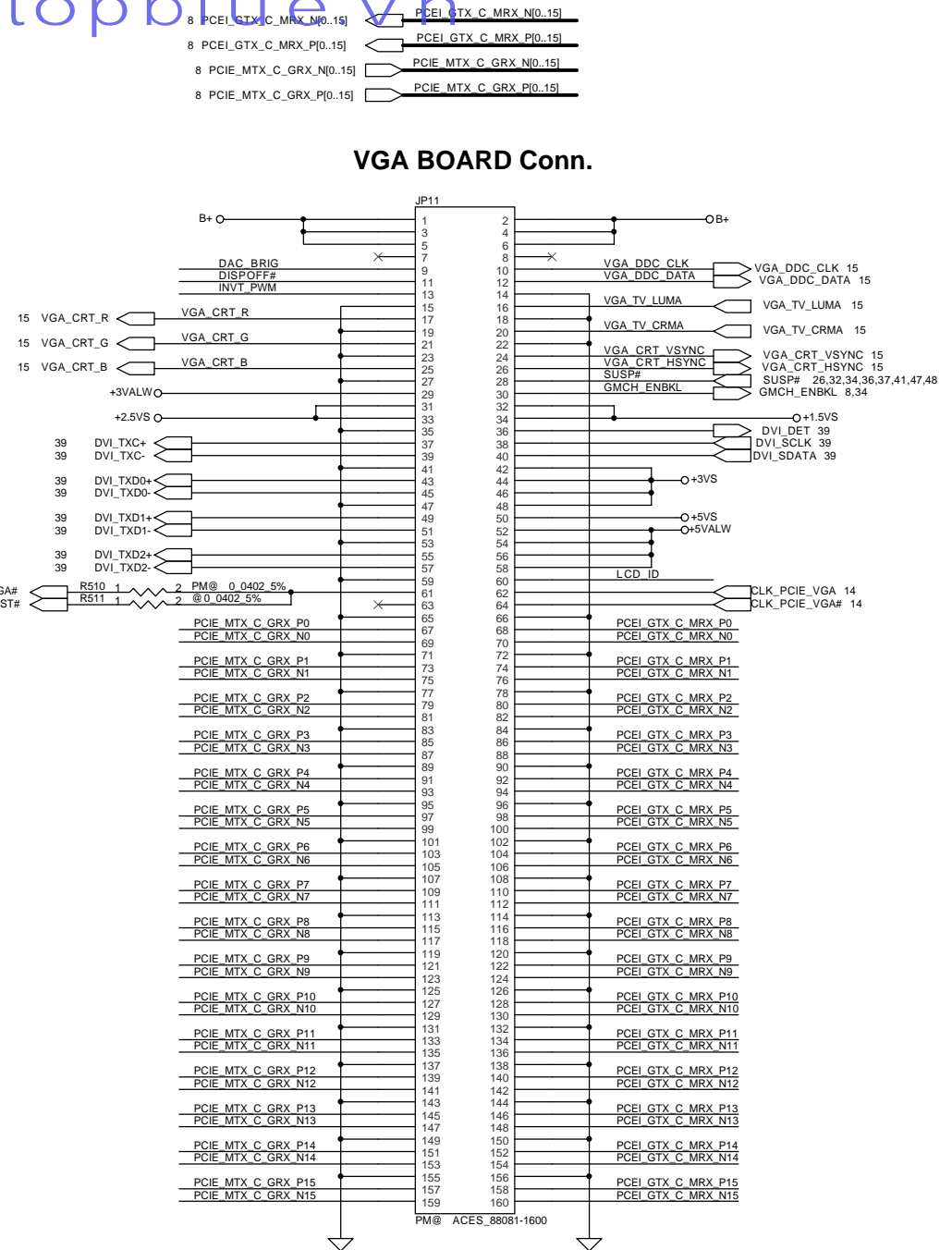
LCD POWER CIRCUIT



LCD/PANEL BD. Conn.



VGA BOARD Conn.



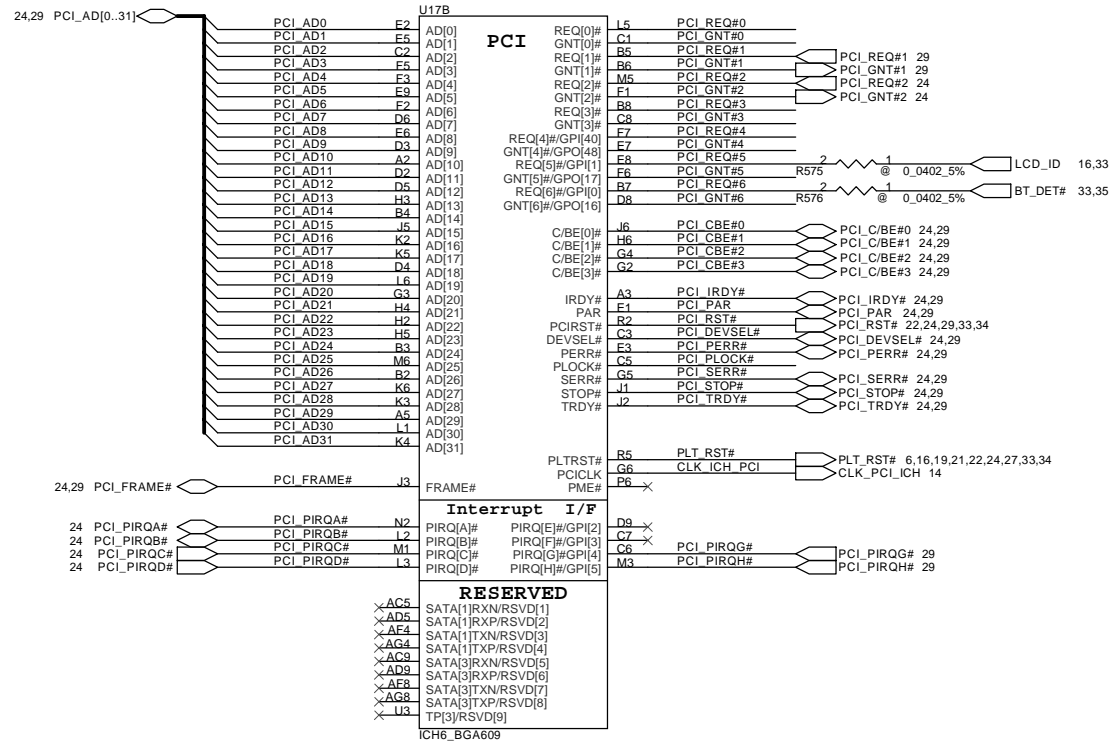
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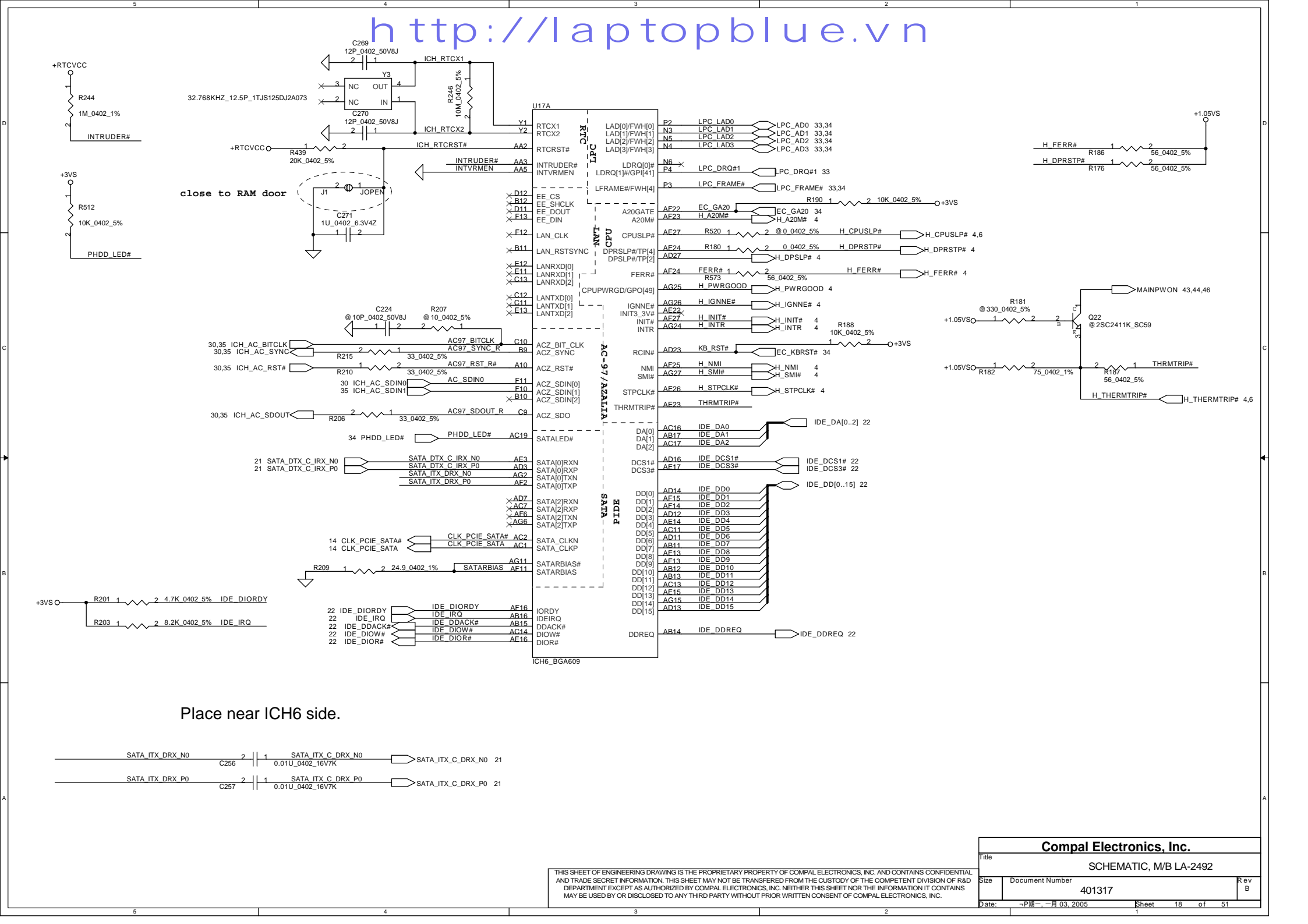


http://laptopblue.vn

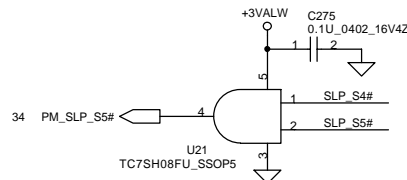
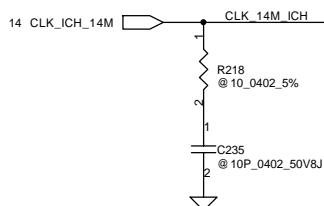
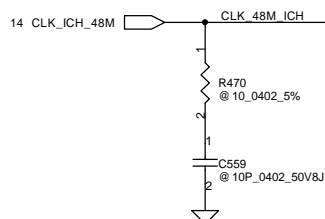
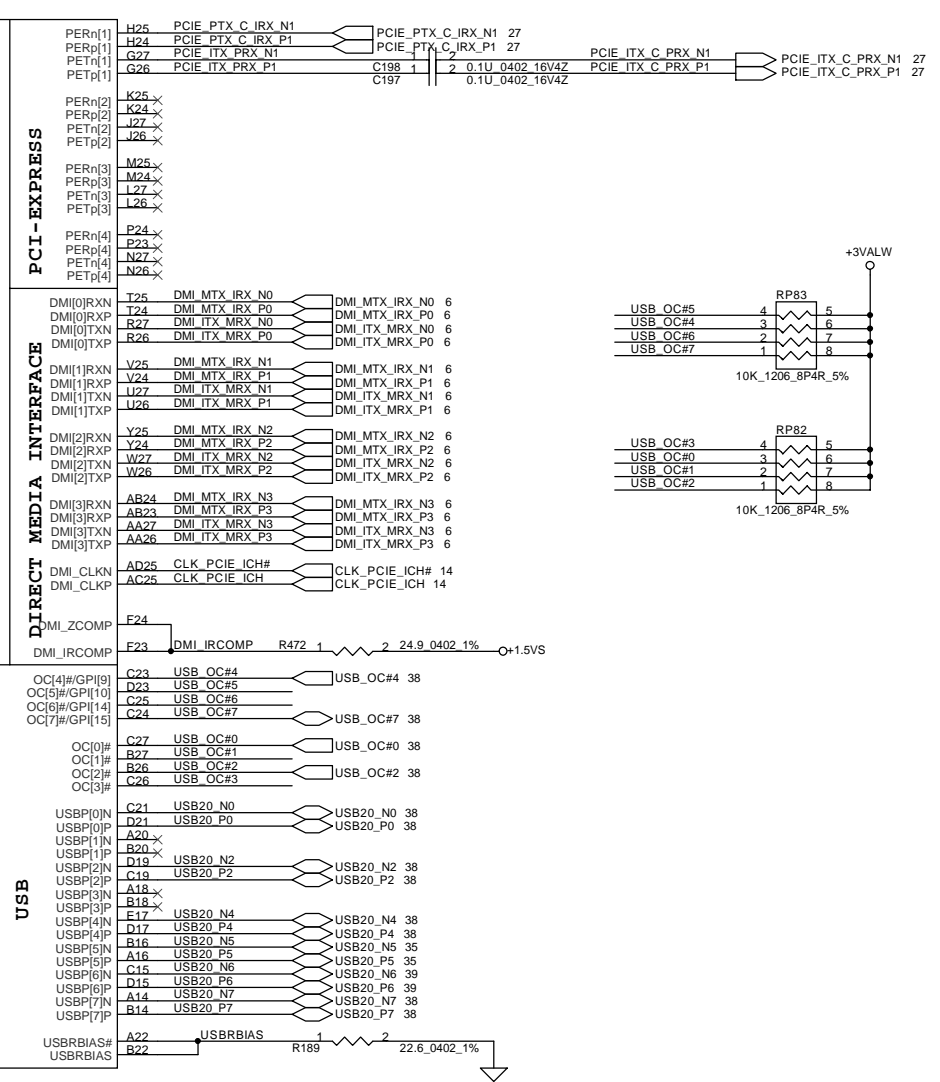
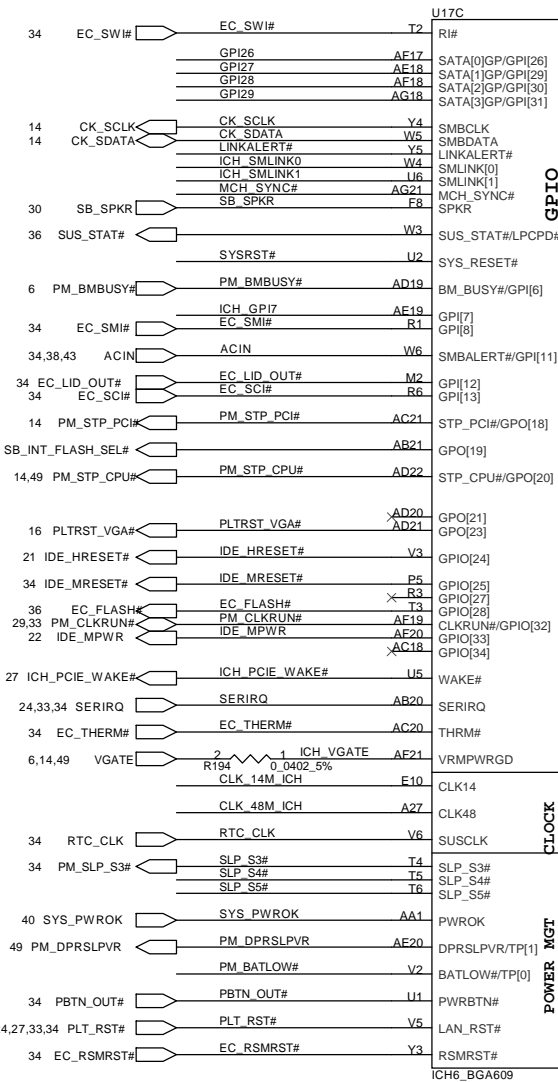
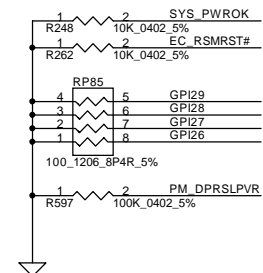
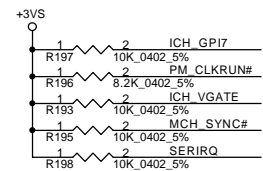
Place near ICH6 side.

SATA ITX_DRX_N0
SATA ITX_DRX_P0

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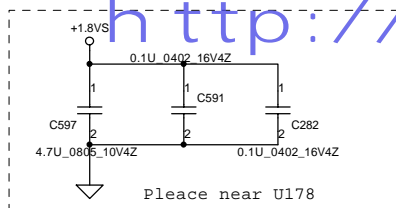


+3V3WLV
 1 R259 10K 0402 5% ICH_SMLINK0
 1 R257 10K 0402 5% ICH_SMLINK1
 1 R464 2.2K 0402 5% CK_SCLK
 1 R465 2.2K 0402 5% CK_SDATA
 1 R260 10K 0402 5% LINKALERT#
 1 R255 @10K 0402 5% EC_LID_OUT#
 1 R256 10K 0402 5% EC_SWI#
 1 R249 8.2K 0402 5% PM_BATLOW#
 1 R258 1K 0402 5% ICH_PCIE_WAKE#
 1 R261 10K 0402 5% SYSRST#



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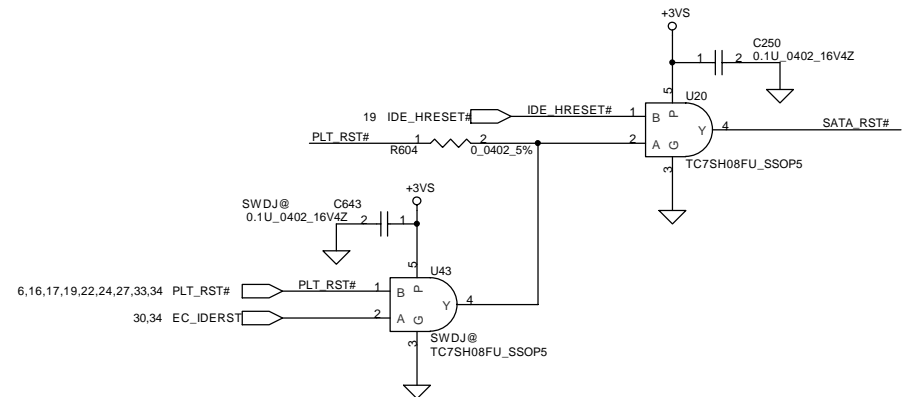
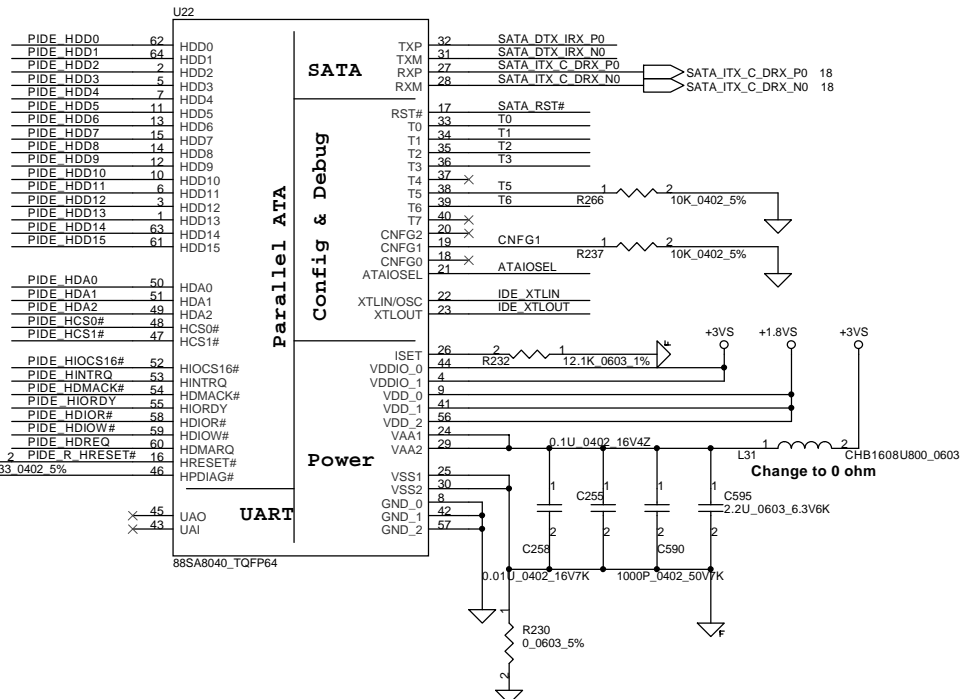
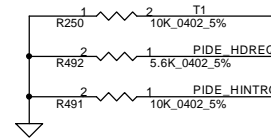


http://laptopblue.vn

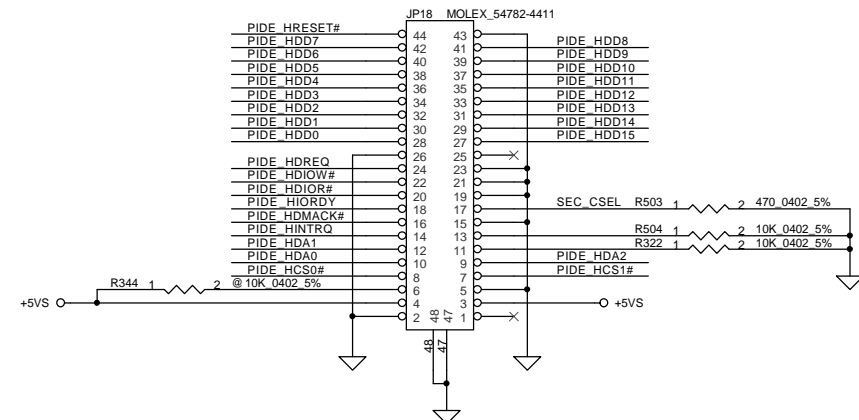
SATA Module

Sets maximum transfer rate and UDMA mode

	CNFG2 INT PD	CNFG1	CNFG0 INT PD	NOTE
*	0	0	0	Device Mode 100MB/s
	0	0	1	Device Mode 133MB/s
	0	1	0	Device Mode 150MB/s
	1	0	0	Host Mode 100MB/s
	1	0	1	Host Mode 133MB/s
	1	1	0	Host Mode 150MB/s
	0	1	1	Reserved
	1	1	1	Reserved

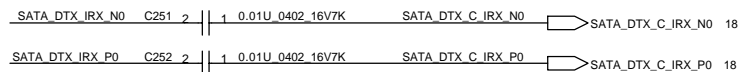


P-ATA HDD Conn.



```
25MHz reference clock T[4:3] = 01
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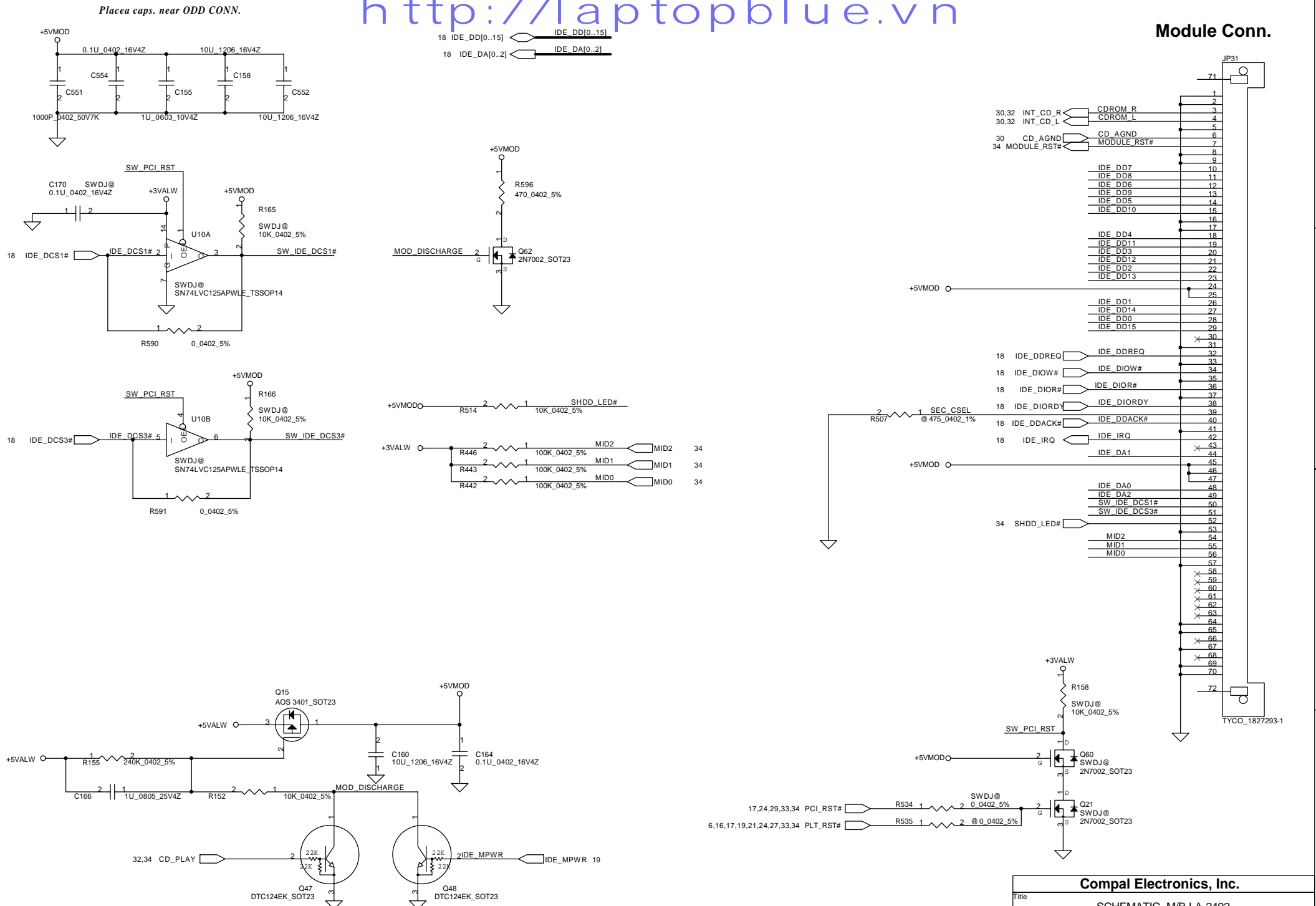
Place near connector side.



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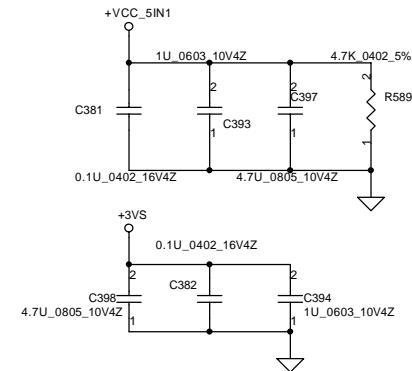
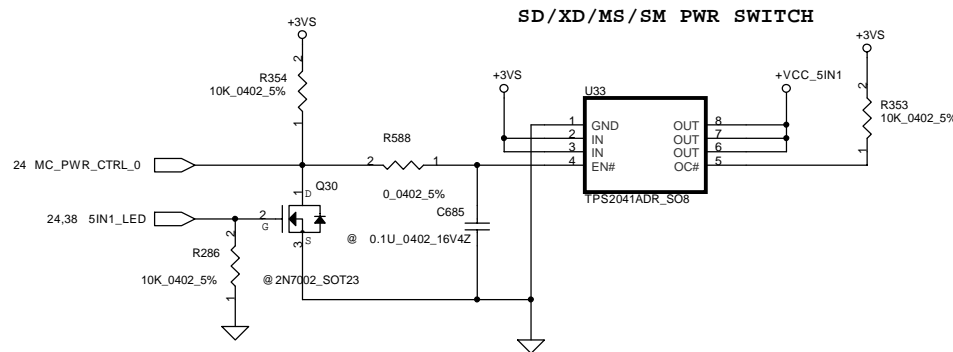
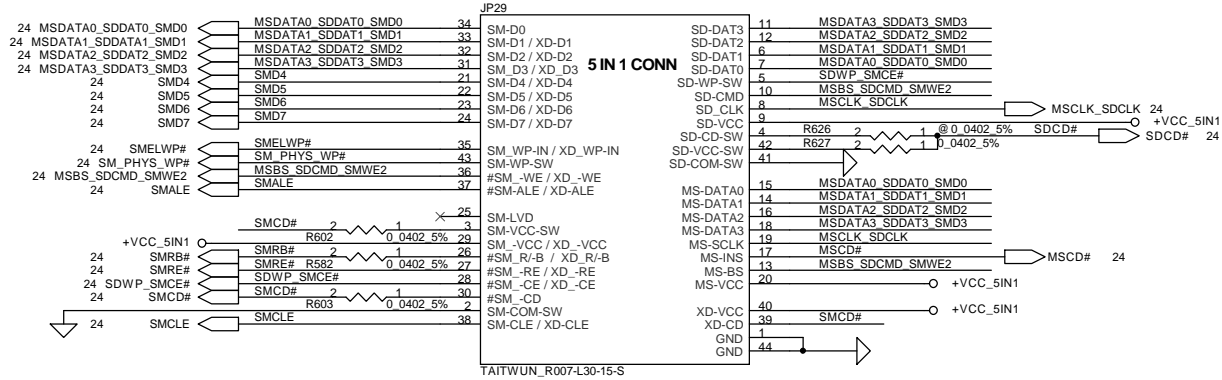
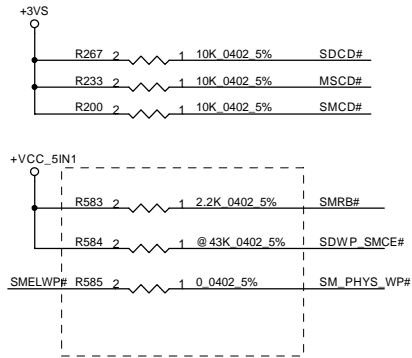
Module Conn.



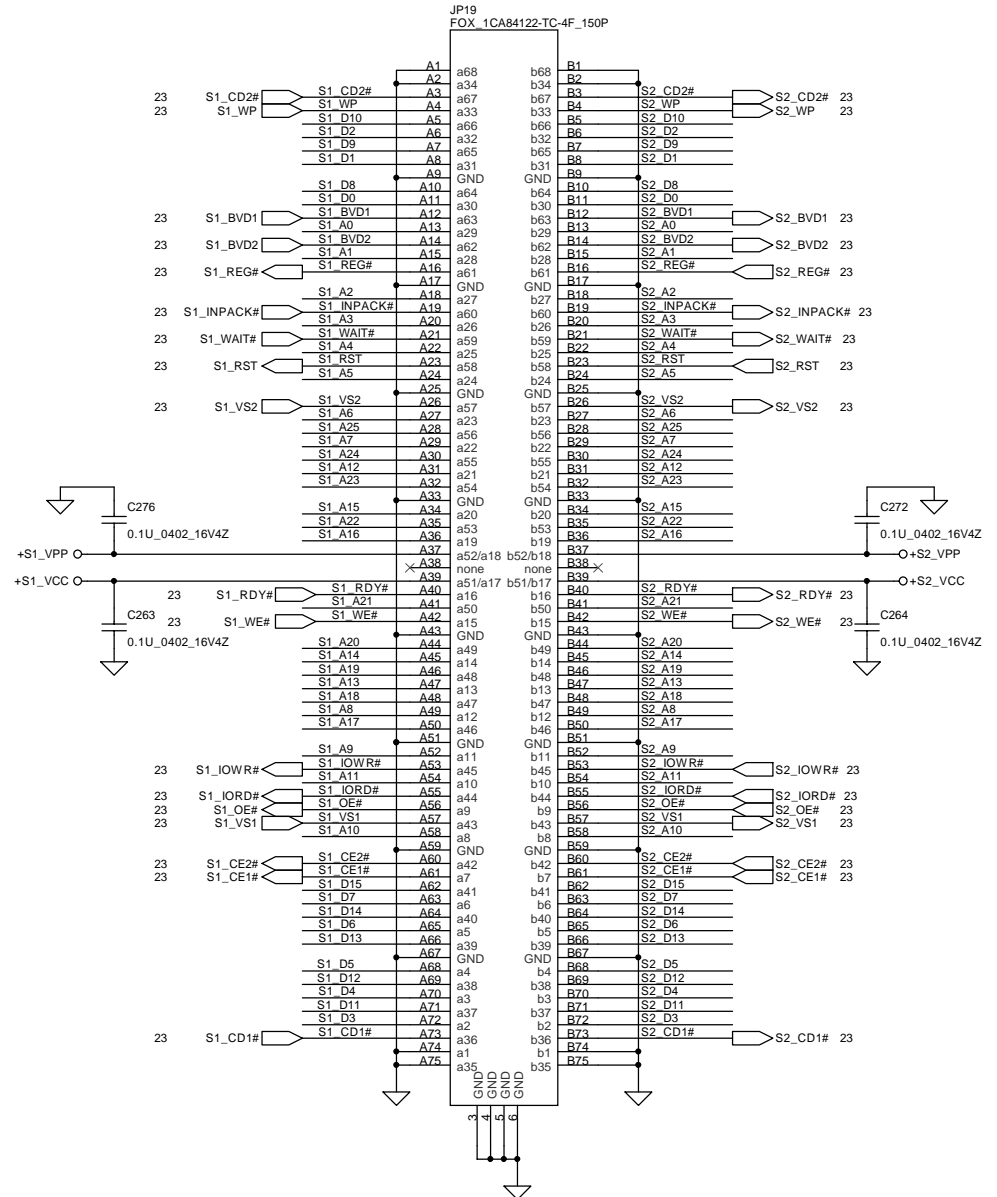
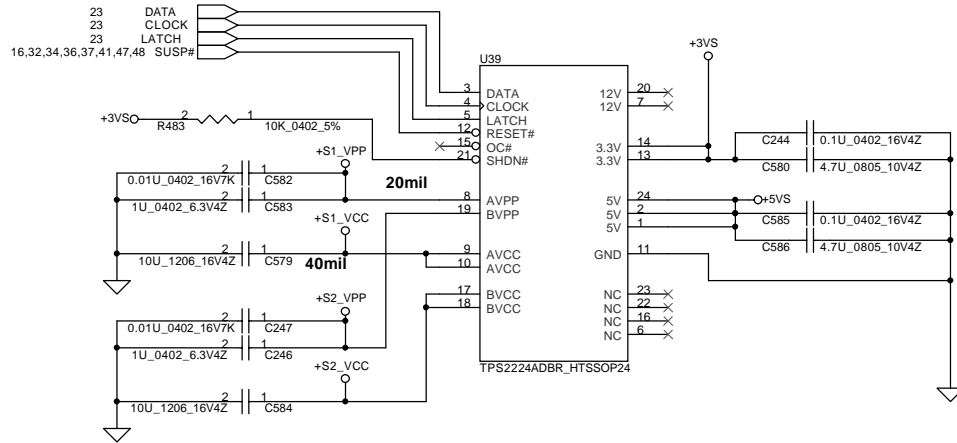
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5 in 1 CardReader Conn.



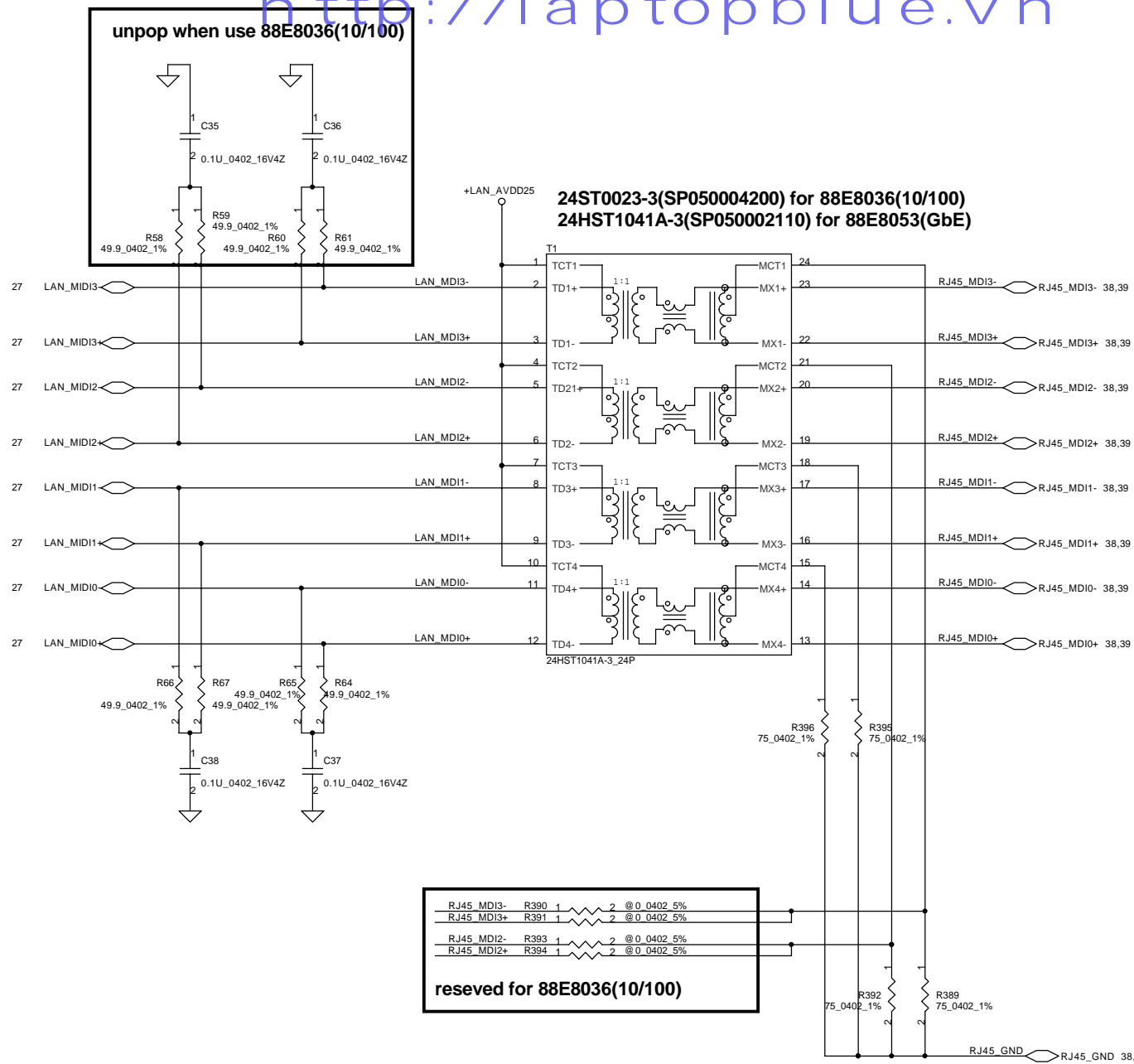
Power Switch for PCMCIA



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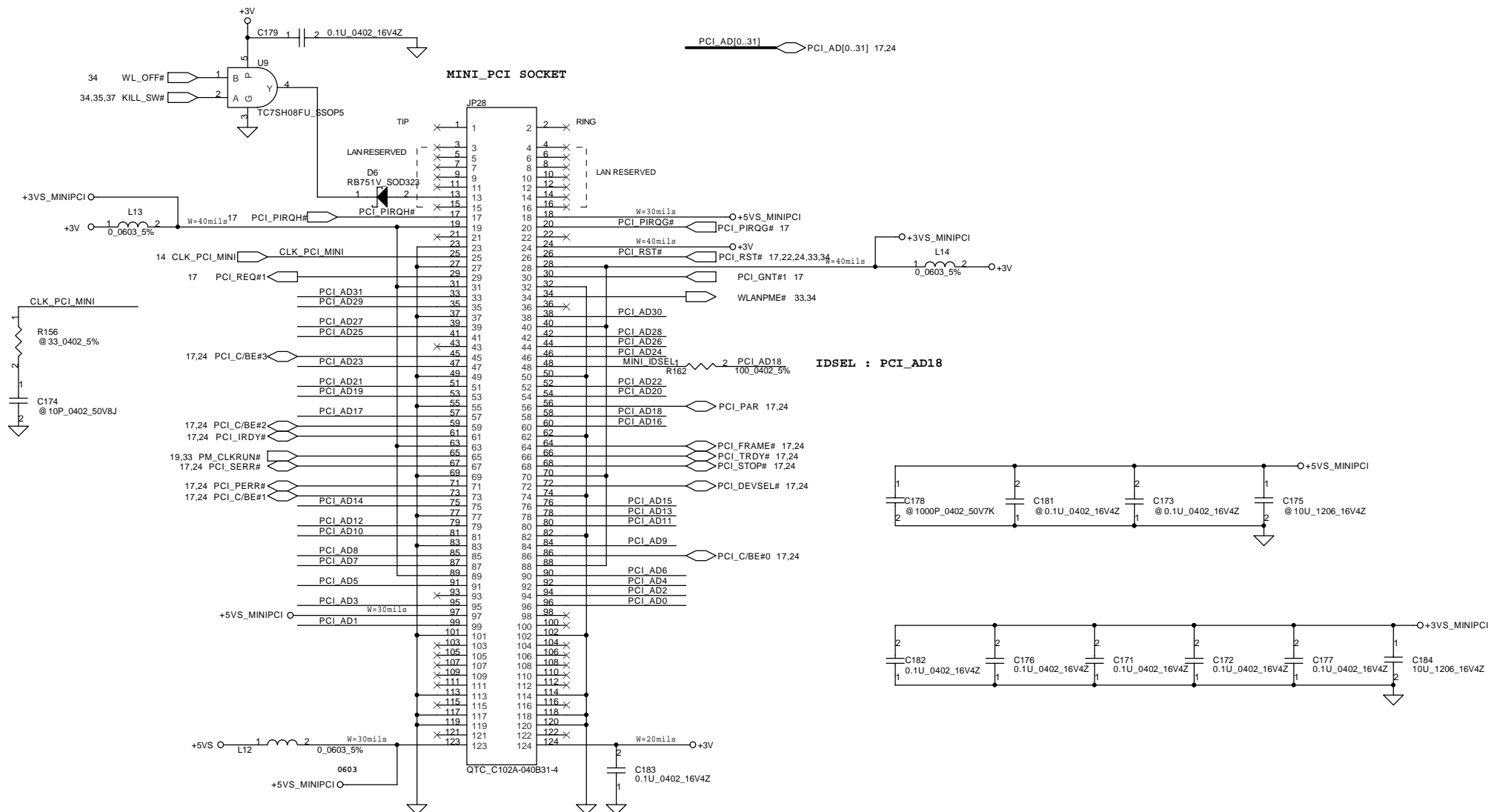
Compal Electronics, Inc.

Title SCHEMATIC, M/B LA-2492

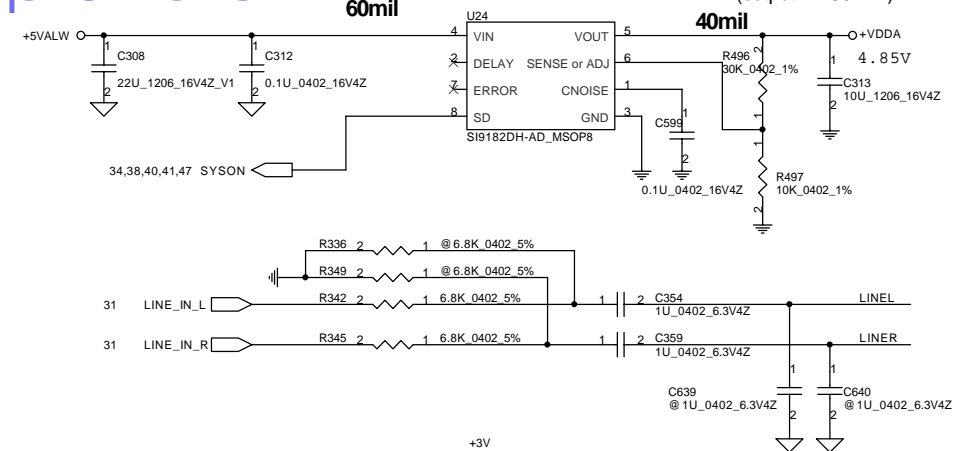
Size Document Number 401317 Rev B

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(output = 250 mA)



Change to 0 ohm

4,34,39 EC_SMB_CLK2

Q58 @ 2N7002_SOT23

R538 @ 1K_0402_5%

R537 @ 4.7K_0402_5%

SMB_CLK

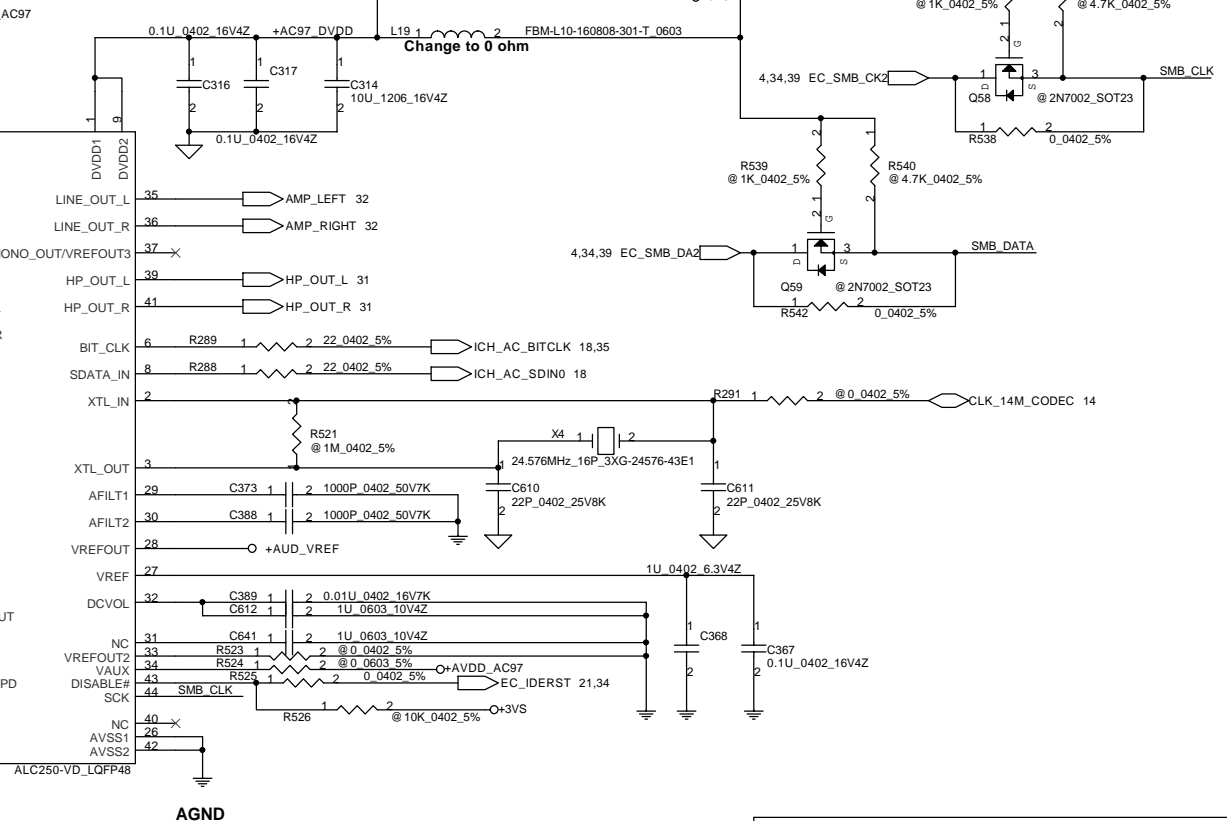
4,34,39 EC_SMB_DA2

Q59 @ 2N7002_SOT23

R540 @ 4.7K_0402_5%

R542 @ 0_0402_5%

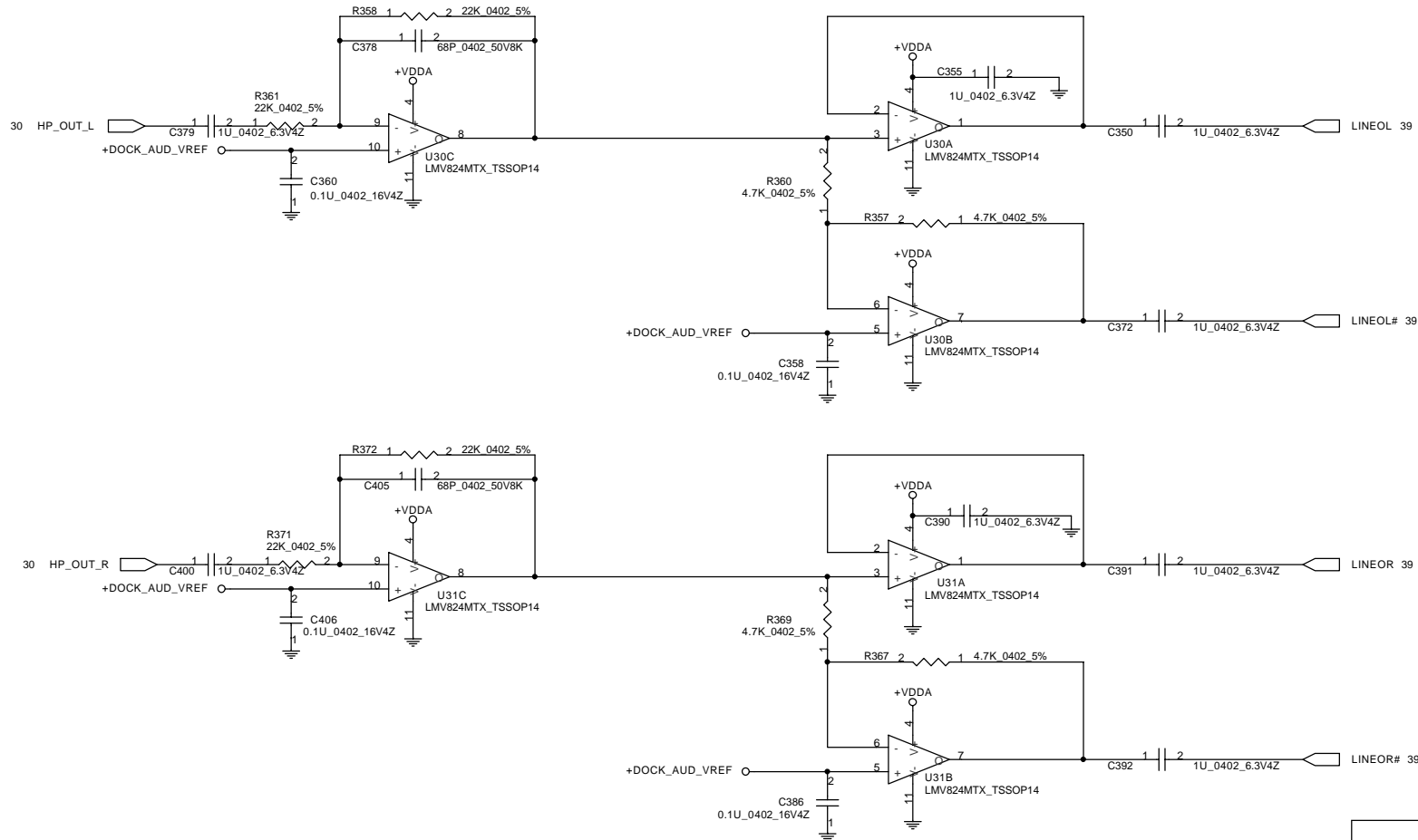
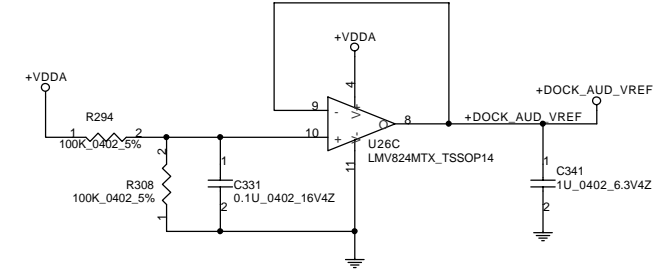
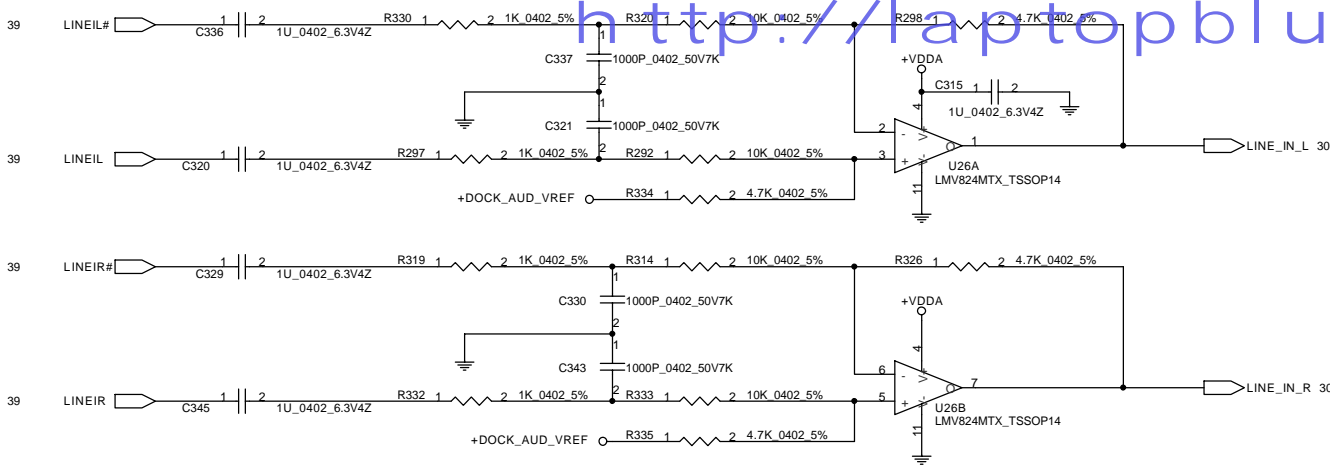
SMB_DATA



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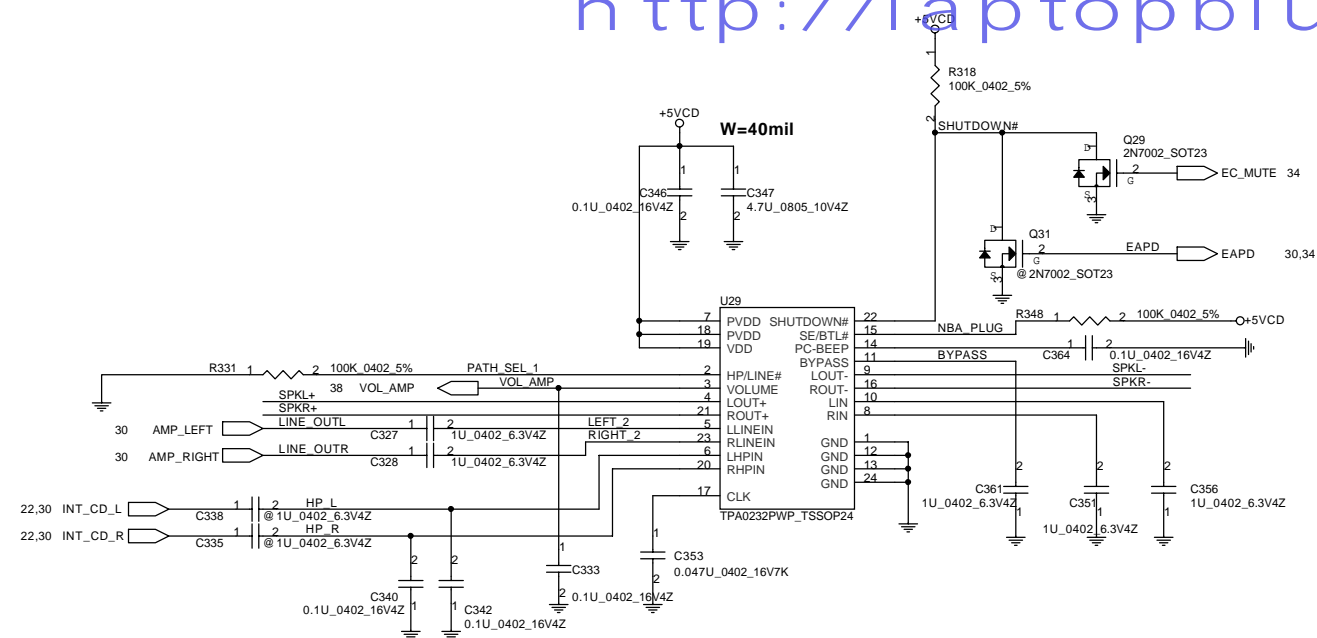
Date: 星期一, 一月 03, 2005 Sheet 30 of 51



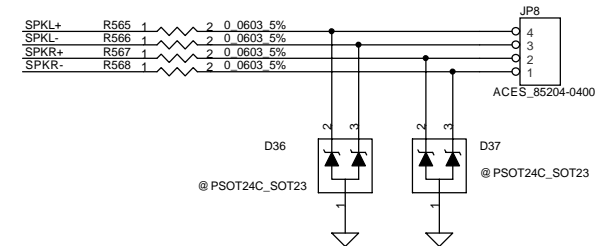
Compal Electronics, Inc.

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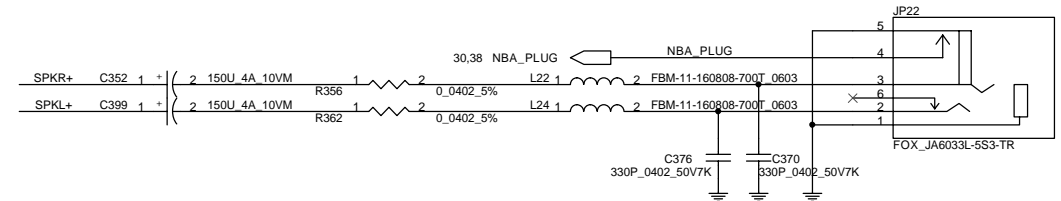
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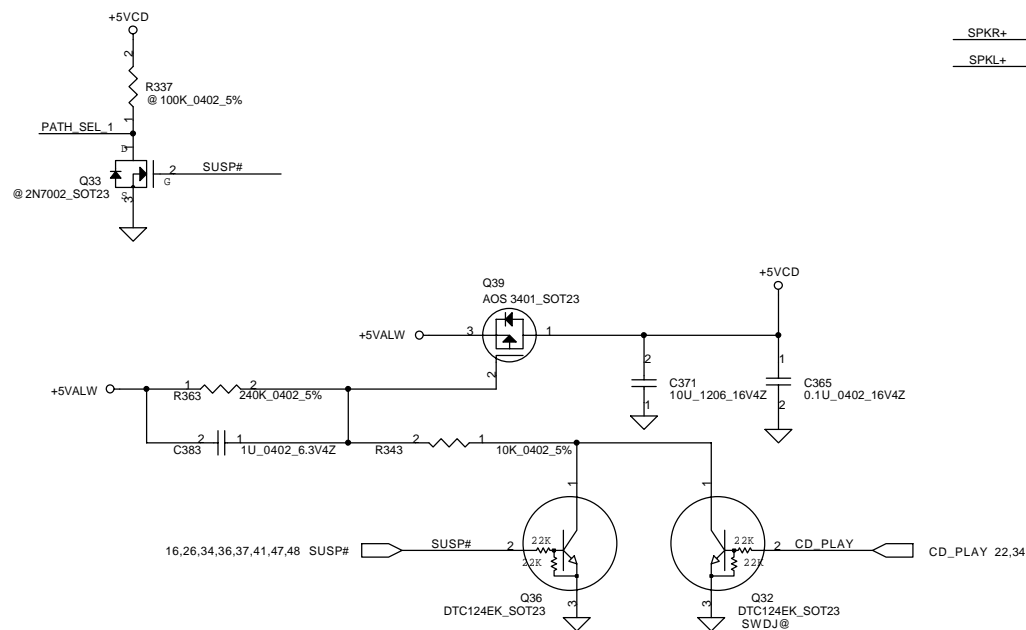
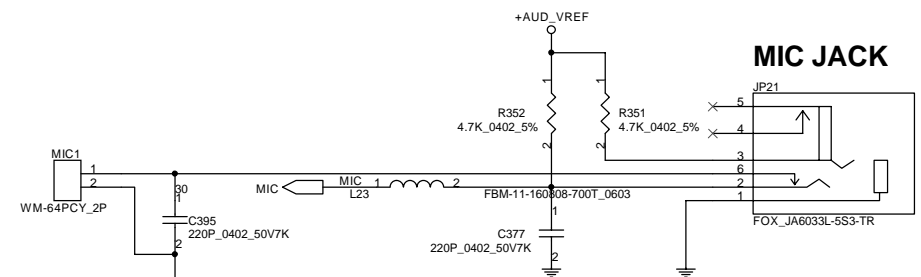
Speaker Conn.



HeadPhone JACK



MIC JACK



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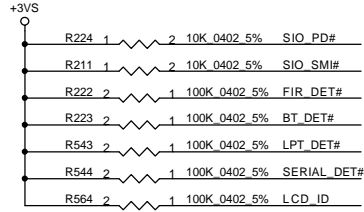
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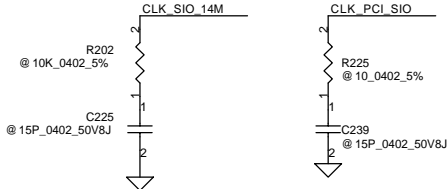
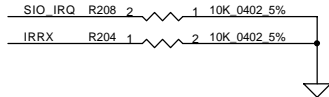
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SUPER I/O SMsC LPC47N217

http://laptopblue.vn



LCD ID : High -- EDID
Low -- Panel ID



17,22,24,29,34 PCI_RST#
6,16,17,19,21,22,24,27,34 PLT_RST#

18,34 LPC_FRAME#
18 LPC_DRQ#1

19,29 PM_CLKRUN#
14 CLK_PCI_SIO
19,24,34 SERIRQ
29,34 SIO_PME#

14 CLK_14M_SIO
16,17 LCD_ID

37 FIR_DET#
17,35 BT_DET#
38 SERIAL_DET#

SIO_GPIO11#
SIO_SMI#
SIO_IRQ

VSS
VSS
VSS
VSS

VTR
VCC
VCC
VCC
VCC

LPC47N217_STQFP64

LPT Module
L: R POP LPT Enable
H: R De-POP LPT Disable

LPT_DET# R551 1 2 1K 0402_5%

LPTSLECT R610 1 2 33 0402_5% LPT@ LPTSLECT EMI
LPTPE R611 1 2 33 0402_5% LPT@ LPTPE EMI
LPTBUSY R612 1 2 33 0402_5% LPT@ LPTBUSY EMI
LPTACK# R613 1 2 33 0402_5% LPT@ LPTACK# EMI

AFD#/3M# R614 1 2 33 0402_5% LPT@ AFD#/3M# EMI
LPTERR# R615 1 2 33 0402_5% LPT@ LPTERR# EMI
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LPTSLECTIN# R617 1 2 33 0402_5% LPT@ LPTSLECTIN# EMI

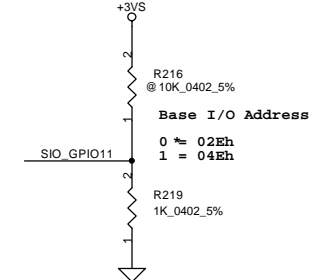
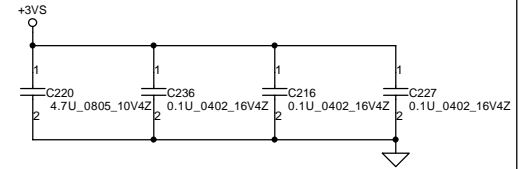
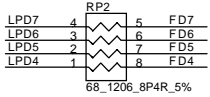
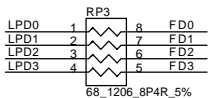
FD0 R618 1 2 33 0402_5% LPT@ FD0 EMI
FD1 R619 1 2 33 0402_5% LPT@ FD1 EMI
FD2 R620 1 2 33 0402_5% LPT@ FD2 EMI
FD3 R621 1 2 33 0402_5% LPT@ FD3 EMI

FD7 R622 1 2 33 0402_5% LPT@ FD7 EMI
FD6 R623 1 2 33 0402_5% LPT@ FD6 EMI
FD5 R624 1 2 33 0402_5% LPT@ FD5 EMI
FD4 R625 1 2 33 0402_5% LPT@ FD4 EMI

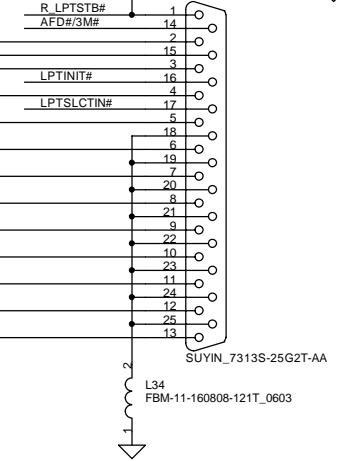
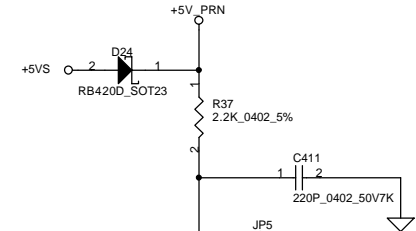
EMI Request for LPT ISSUE

Close to Docking

LPTSTB# R43 1 2 33 0402_5% R_LPTSTB# 39
LPTAFD# R36 1 2 33 0402_5% AFD#/3M# 39
INIT# R22 1 2 33 0402_5% LPTINIT# 39
SLCTIN# R35 1 2 33 0402_5% LPTSLECTIN# 39



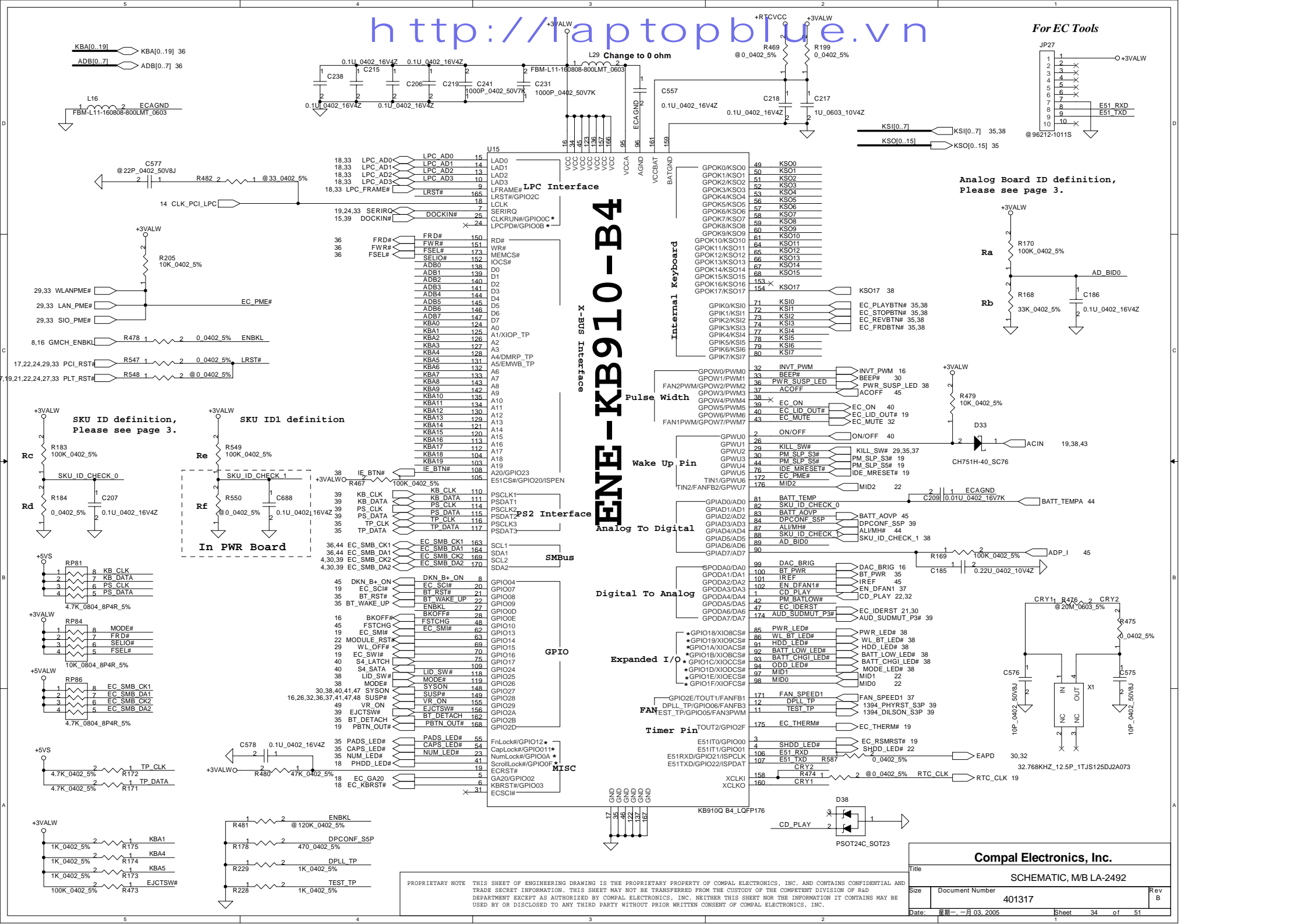
Parallel Port



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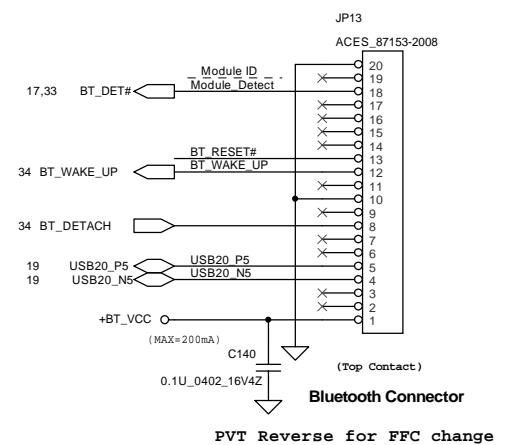
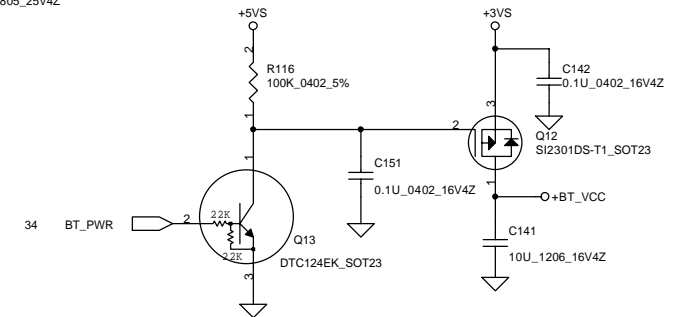
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Analog Board ID definition, Please see page 3.

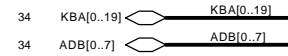
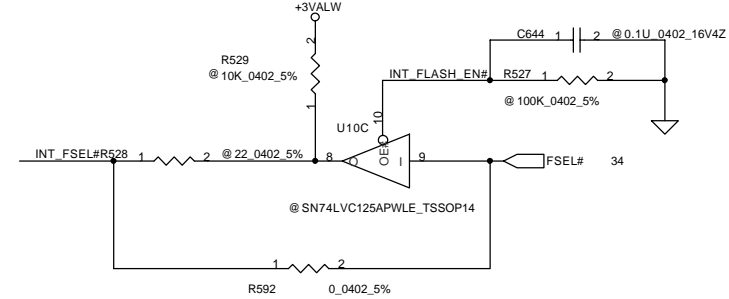
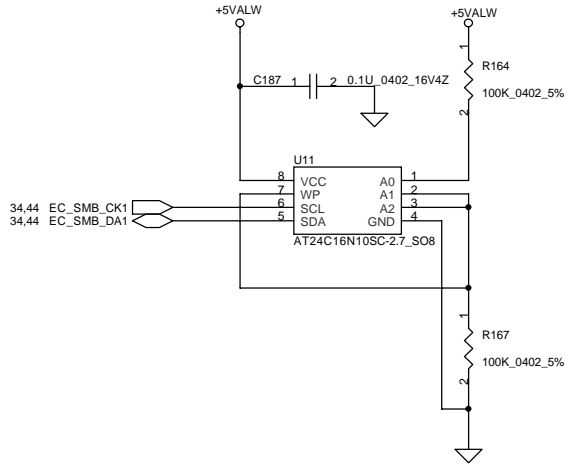
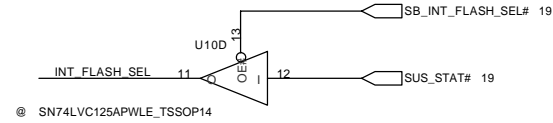
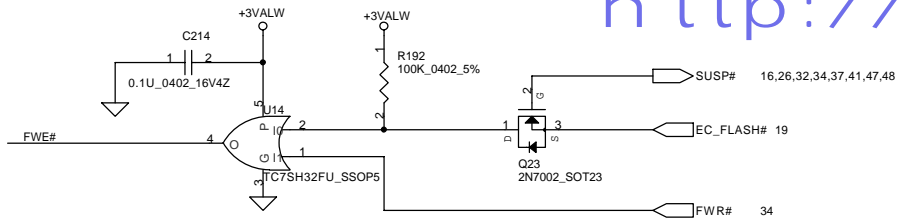
SKU ID definition, Please see page 3.

In PWR Board

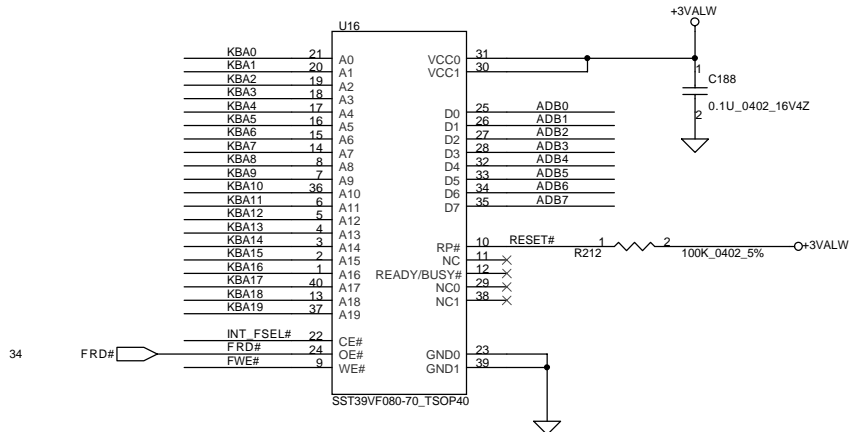


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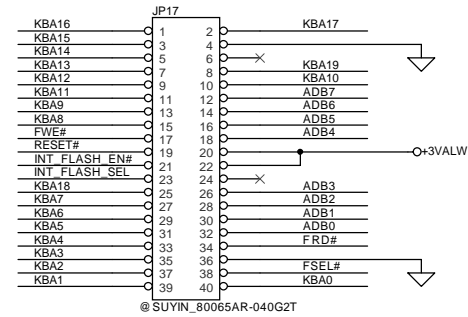
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1MB Flash ROM



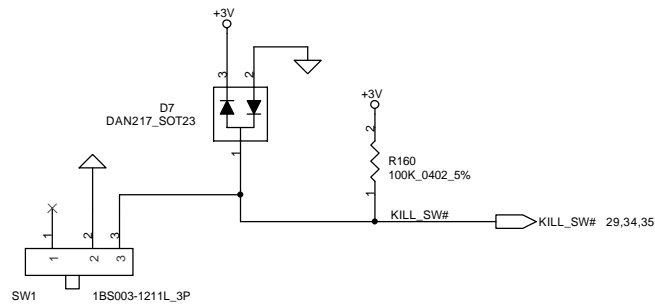
1MB ROM Socket



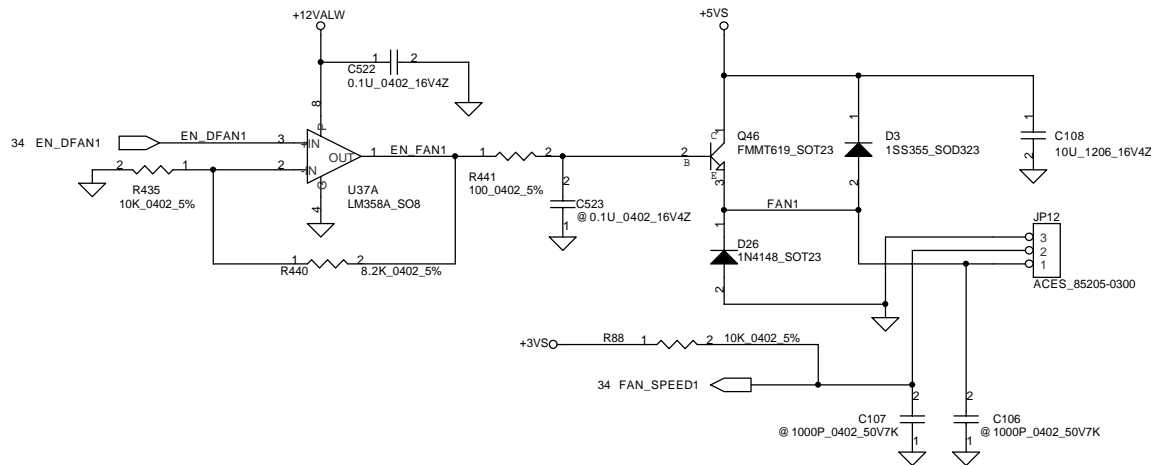
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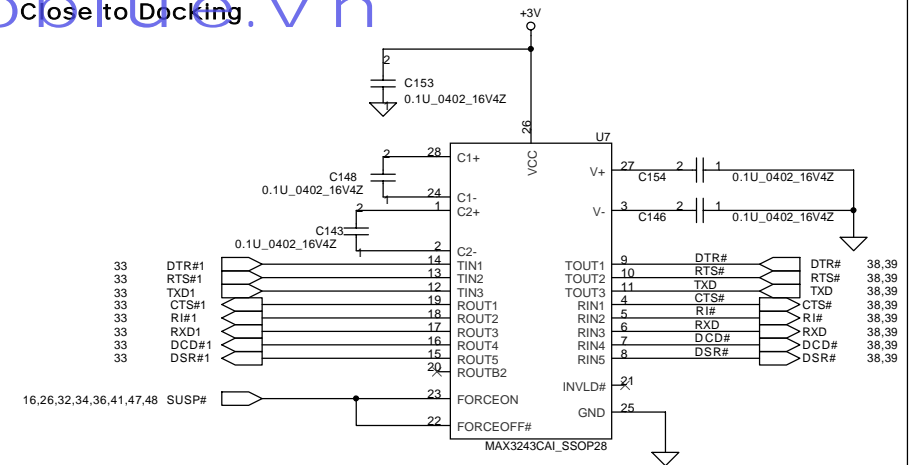
Kill SWITCH



FAN Conn



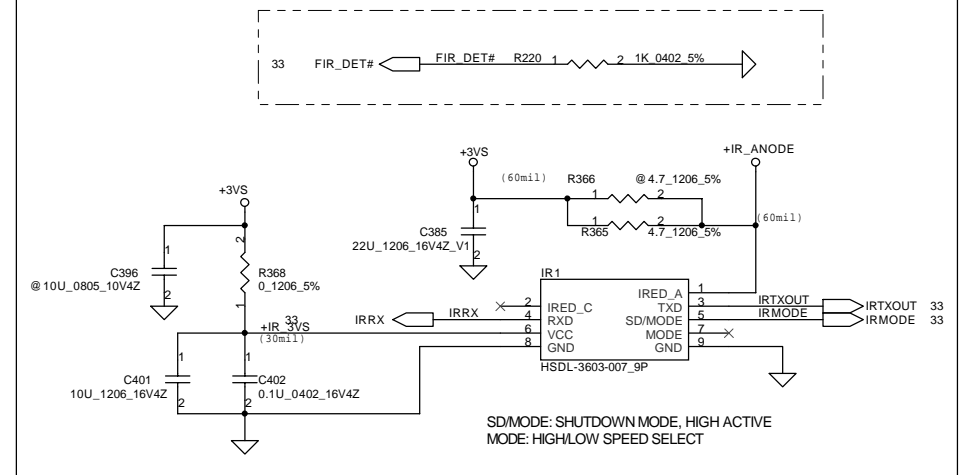
Close to Docking



No Docking and Serial Port -----> Del

FIR Module

L: R POP; FIR Enable
H: R De-POP; FIR Disable

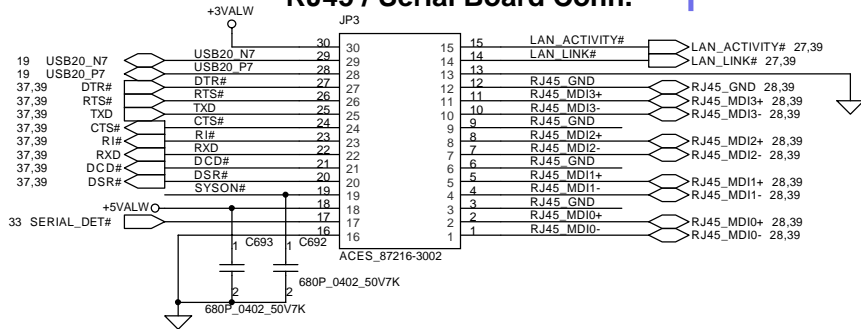


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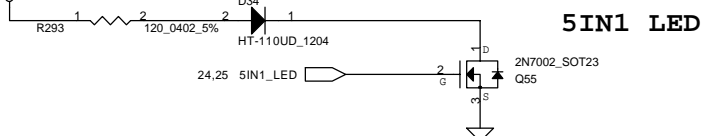
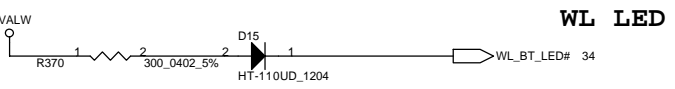
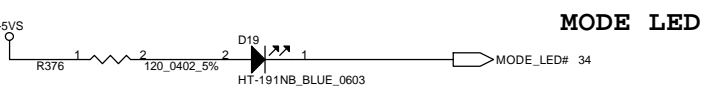
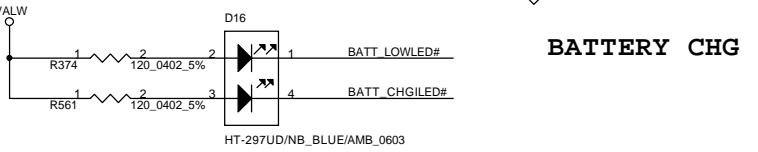
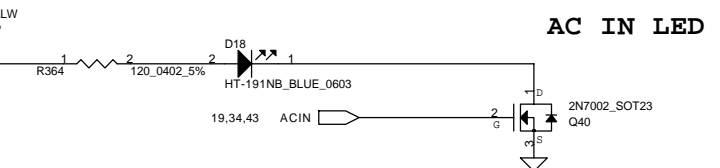
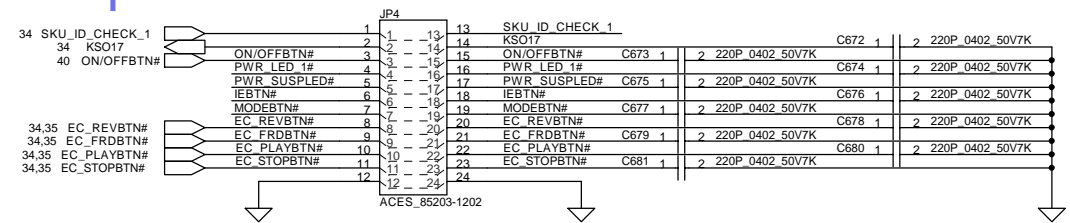
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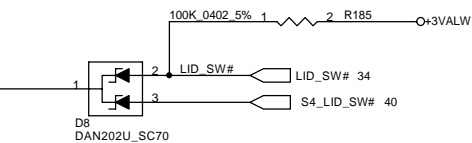
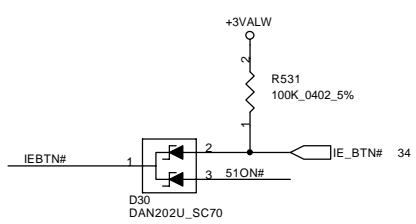
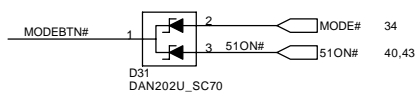
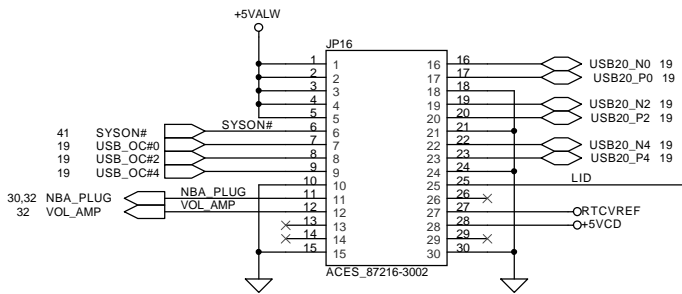
RJ45 / Serial Board Conn.



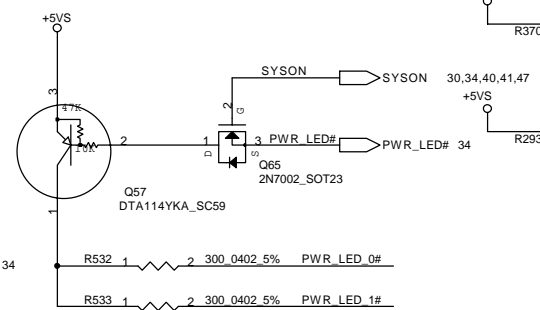
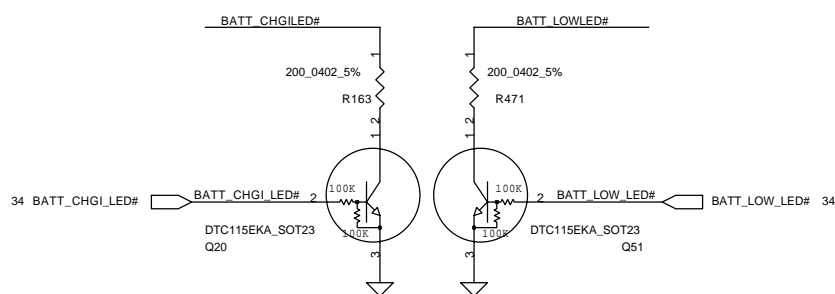
Power/LED Board Conn.



USB Board Conn.



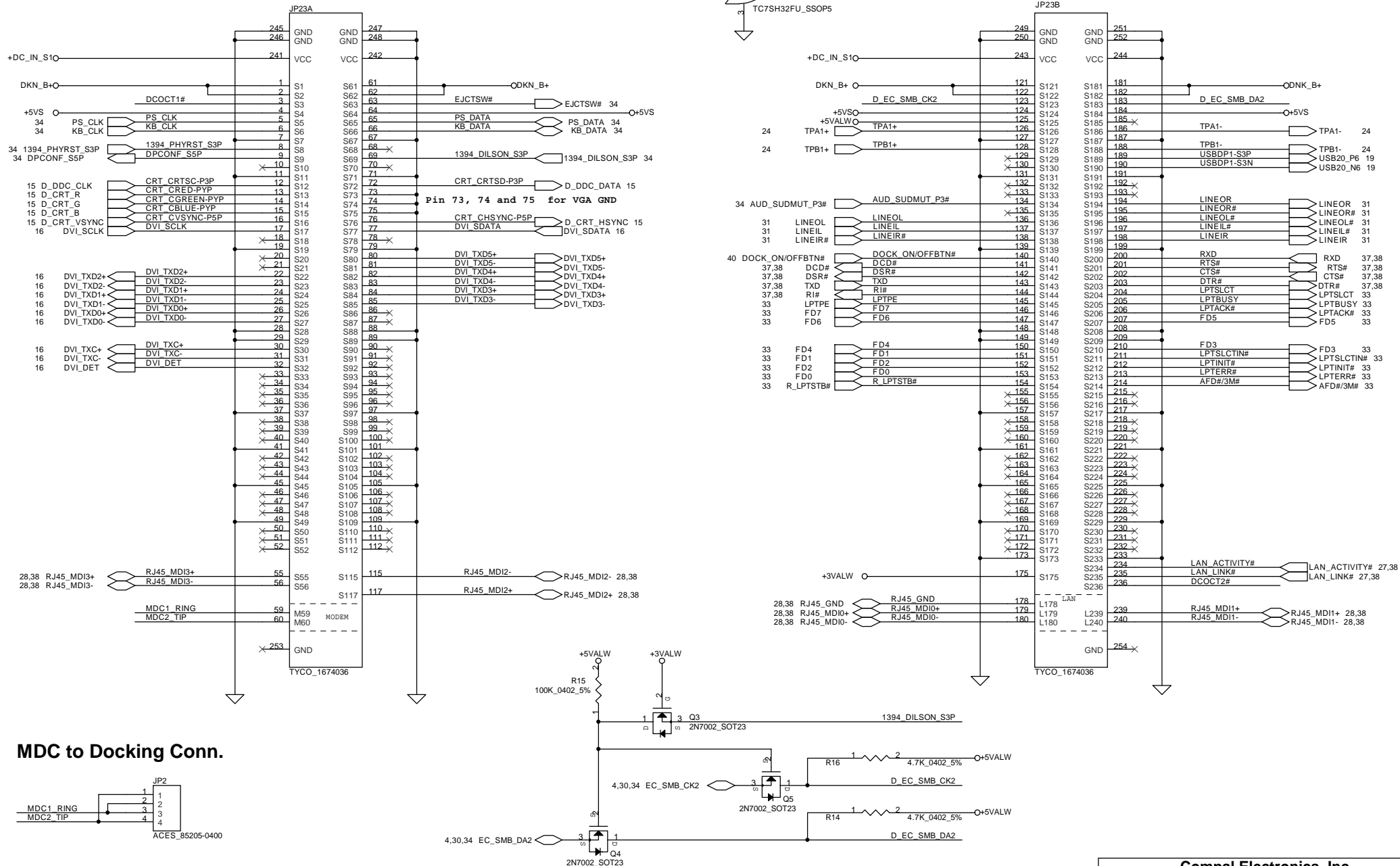
BATTERY CHG/LOW LED



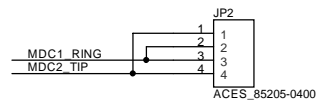
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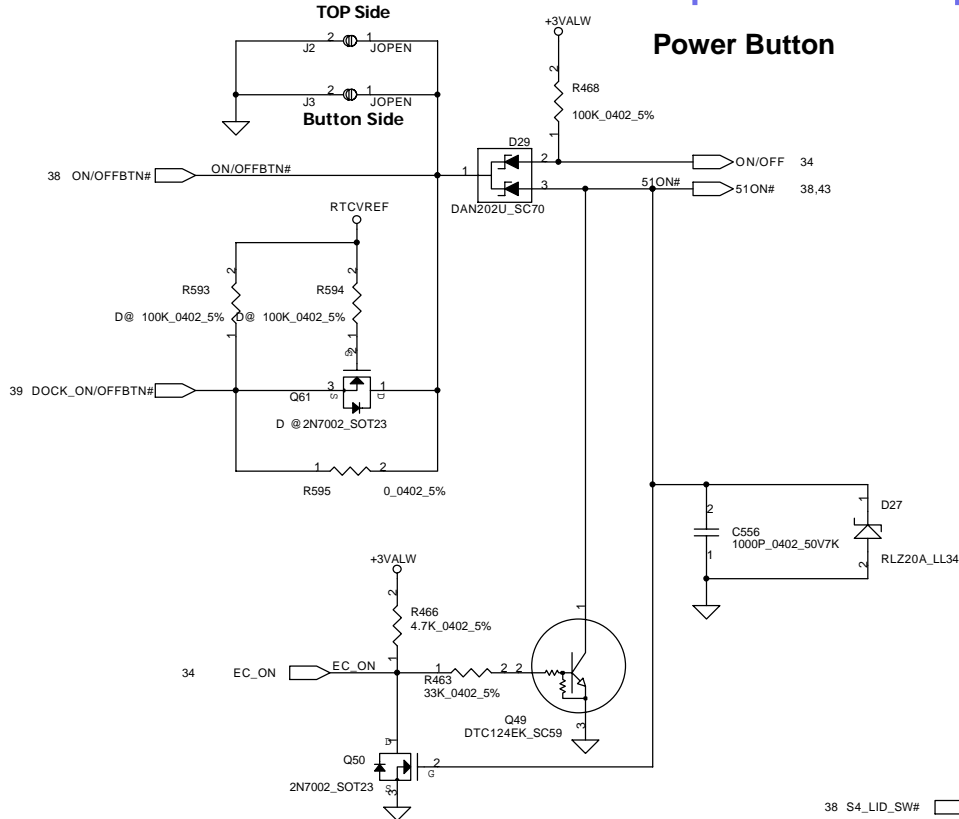


MDC to Docking Conn.

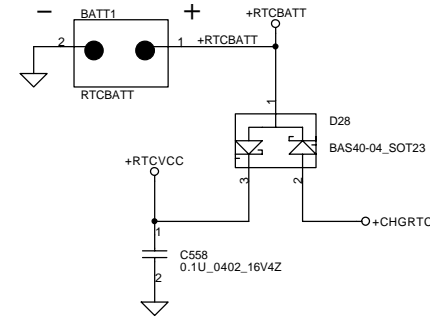


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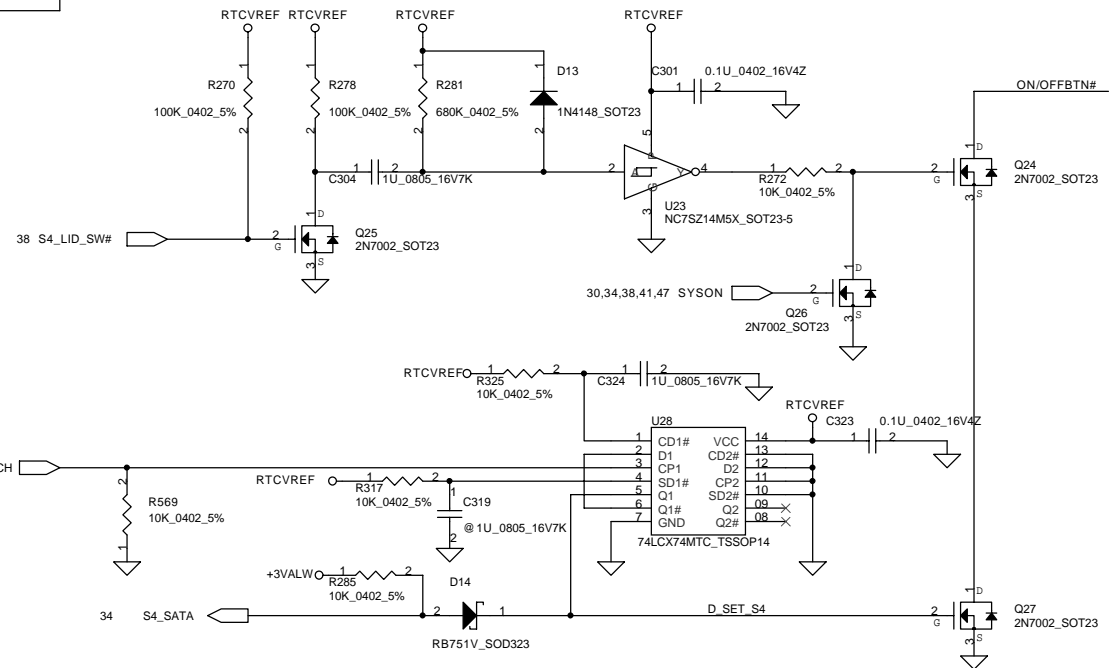
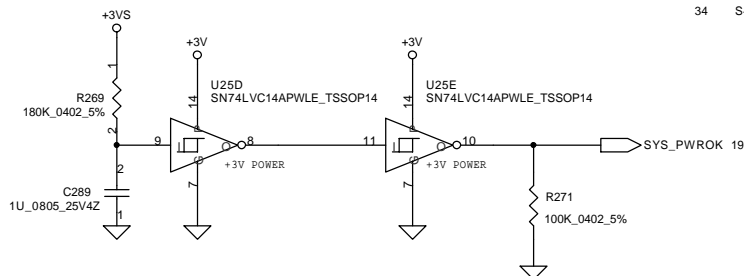
Power Button



RTC Battery



Power ON Circuit



Compal Electronics, Inc.

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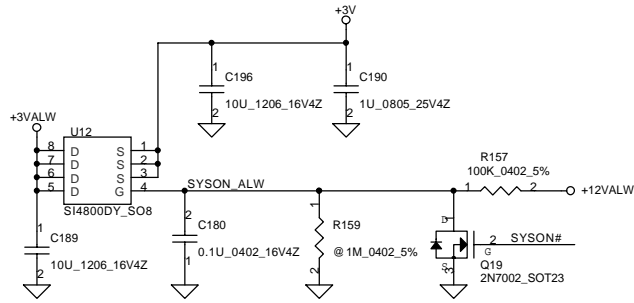
401317

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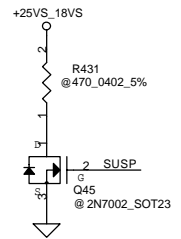
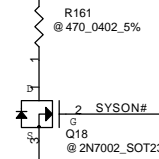
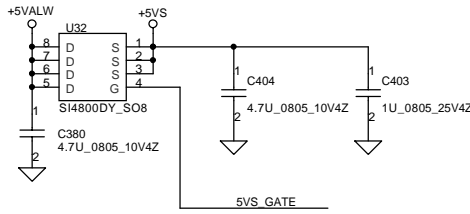
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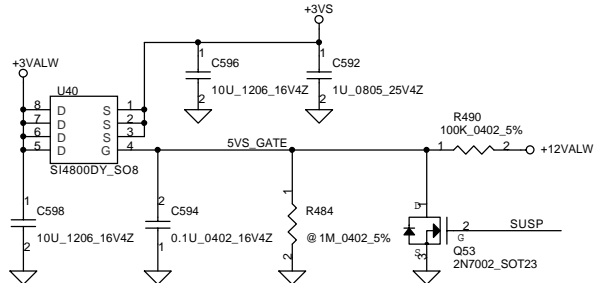
+3VALW TO +3V



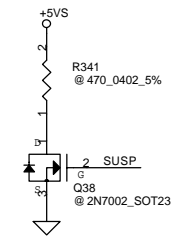
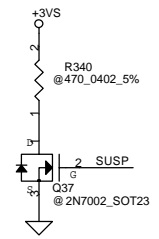
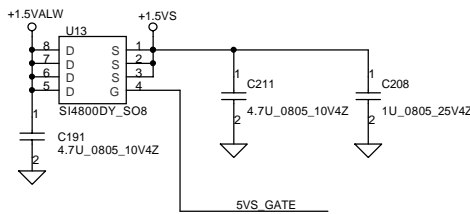
+5VALW TO +5VS



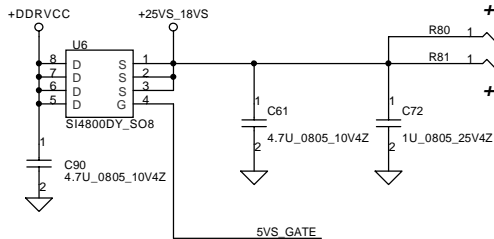
+3VALW TO +3VS



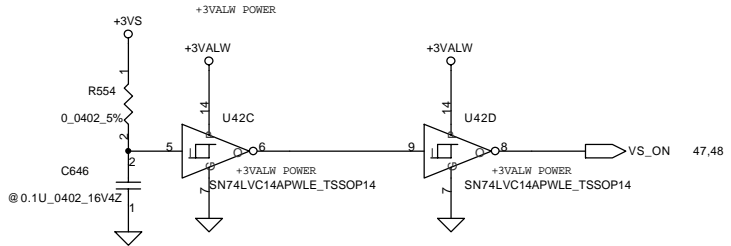
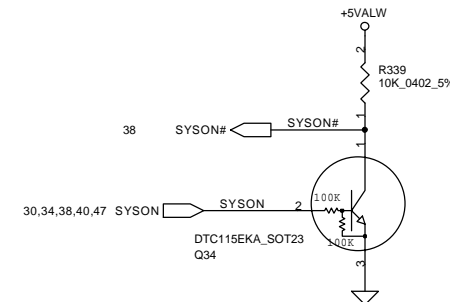
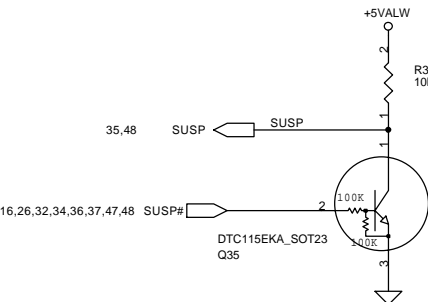
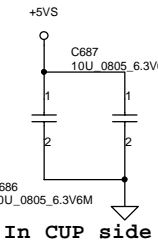
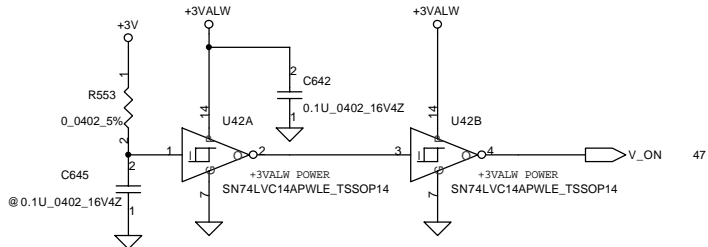
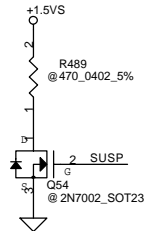
+1.5VALW TO +1.5VS



+2.5V TO +2.5VS (DDR1)

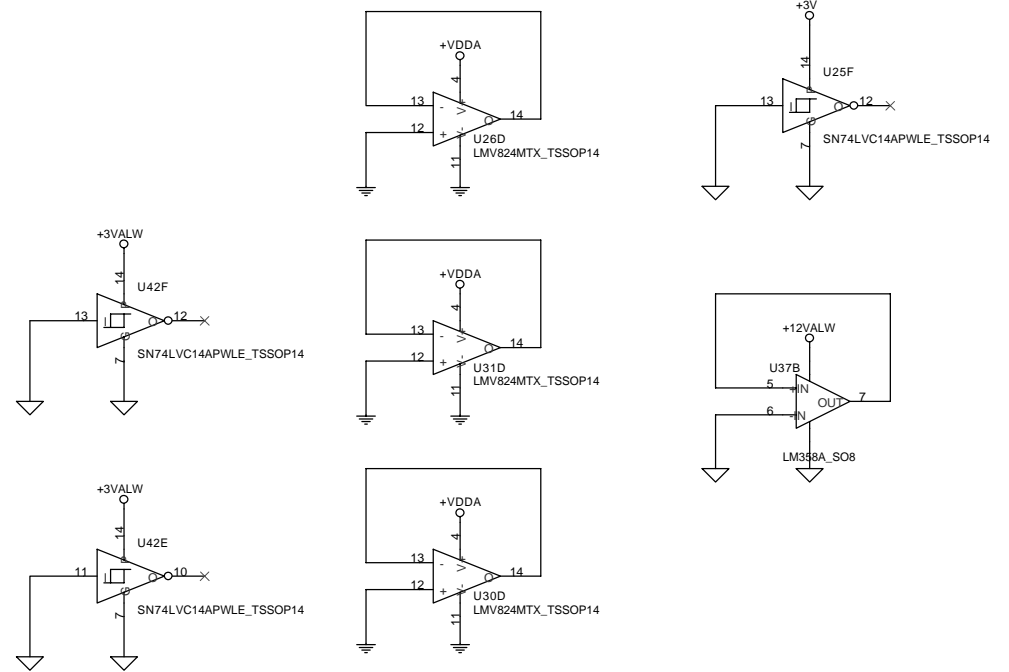
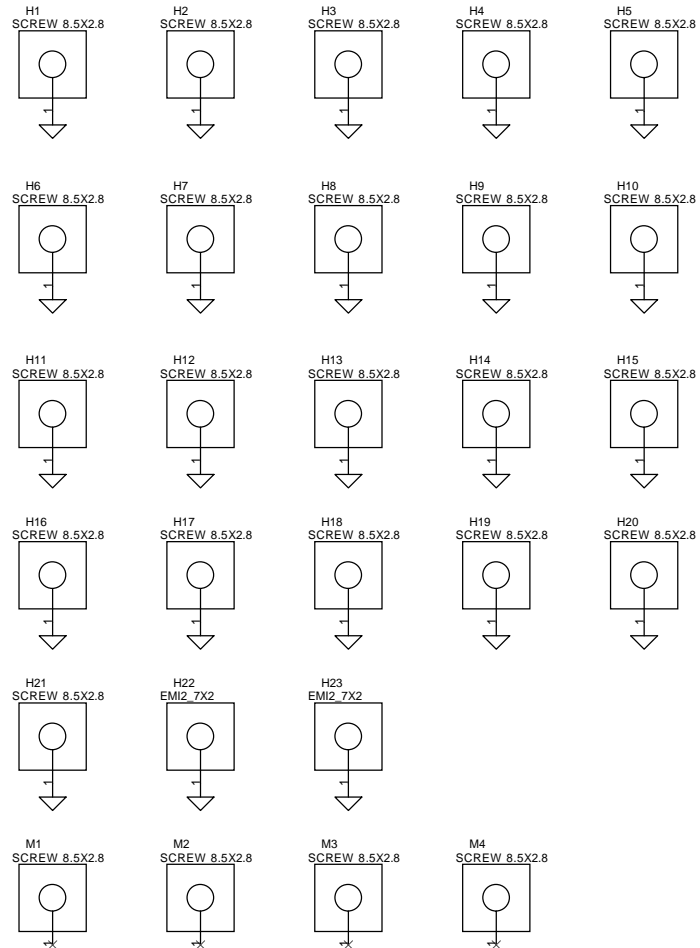
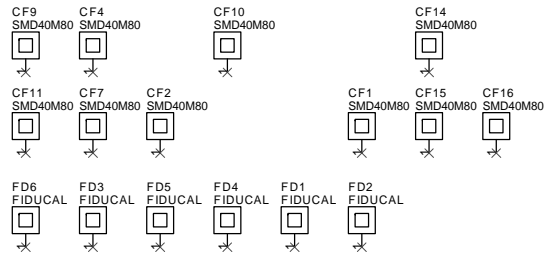


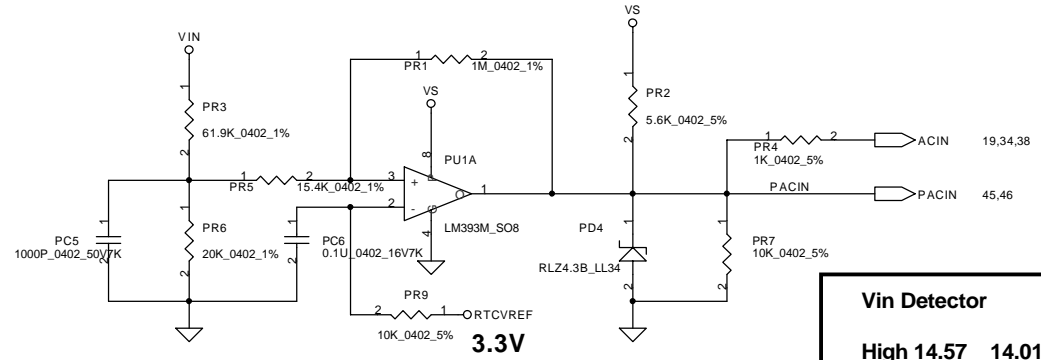
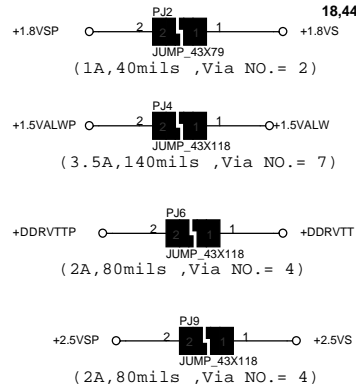
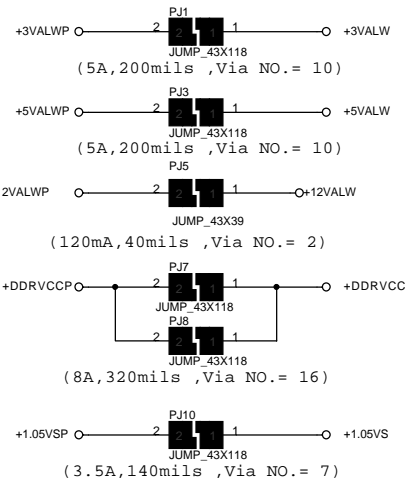
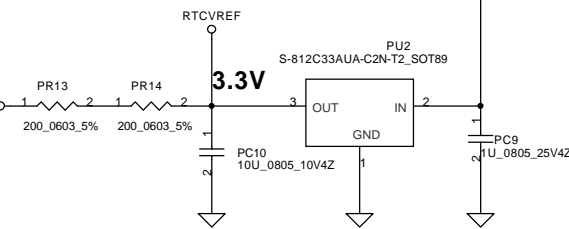
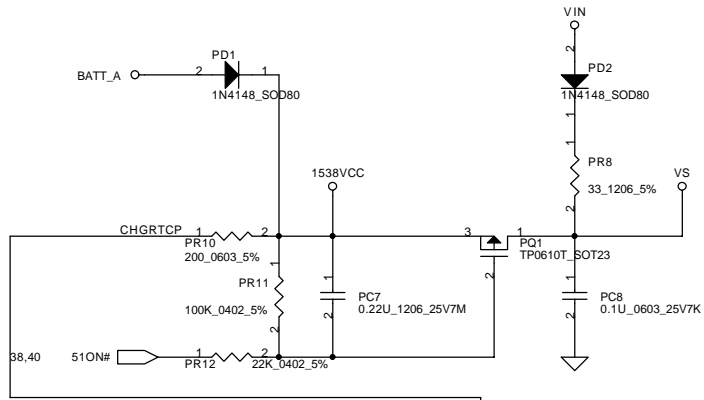
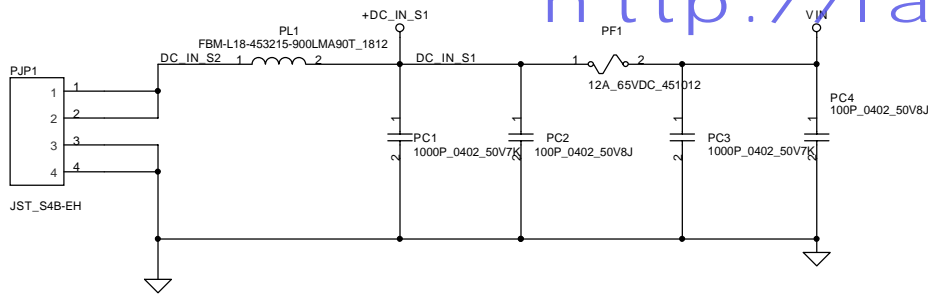
+1.8V TO +1.8VS (DDR2)



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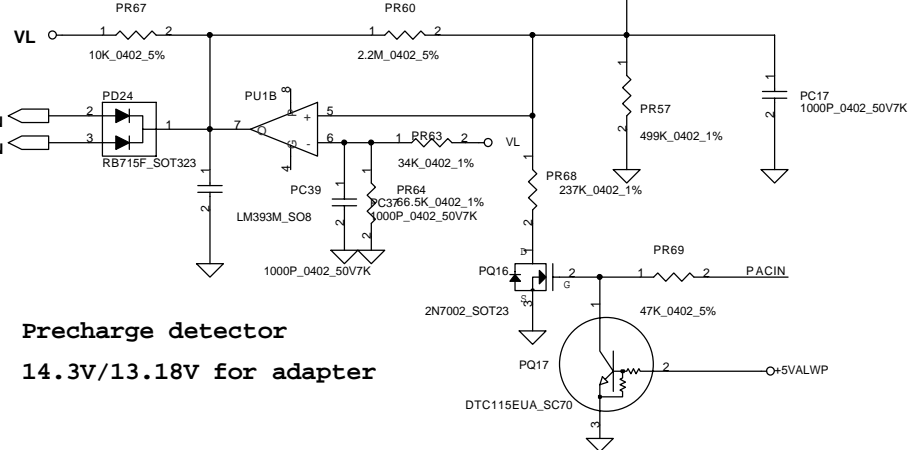
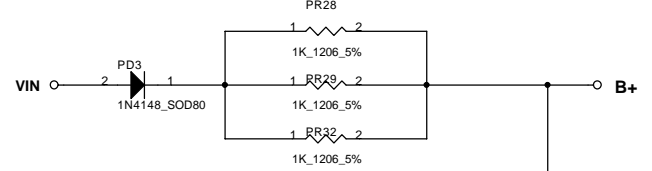
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Vin Detector

High 14.57 14.01 13.46
Low 14.06 13.51 12.98

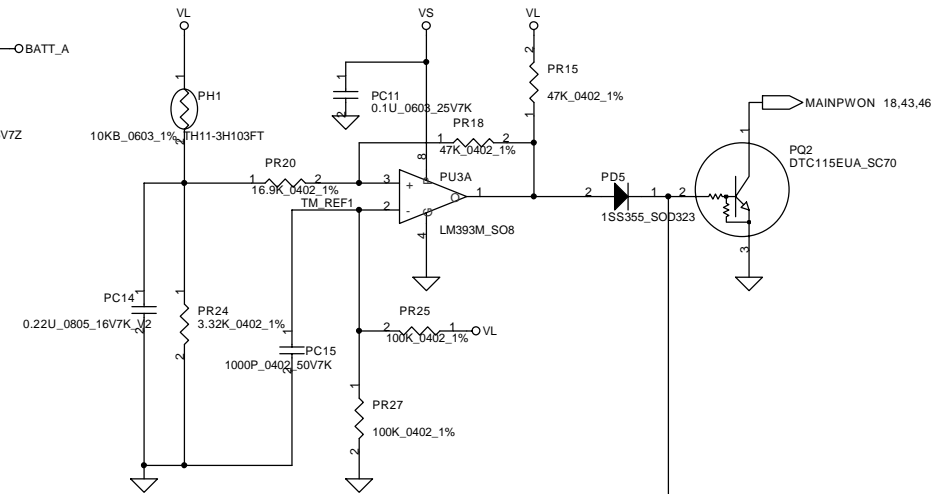


Precharge detector

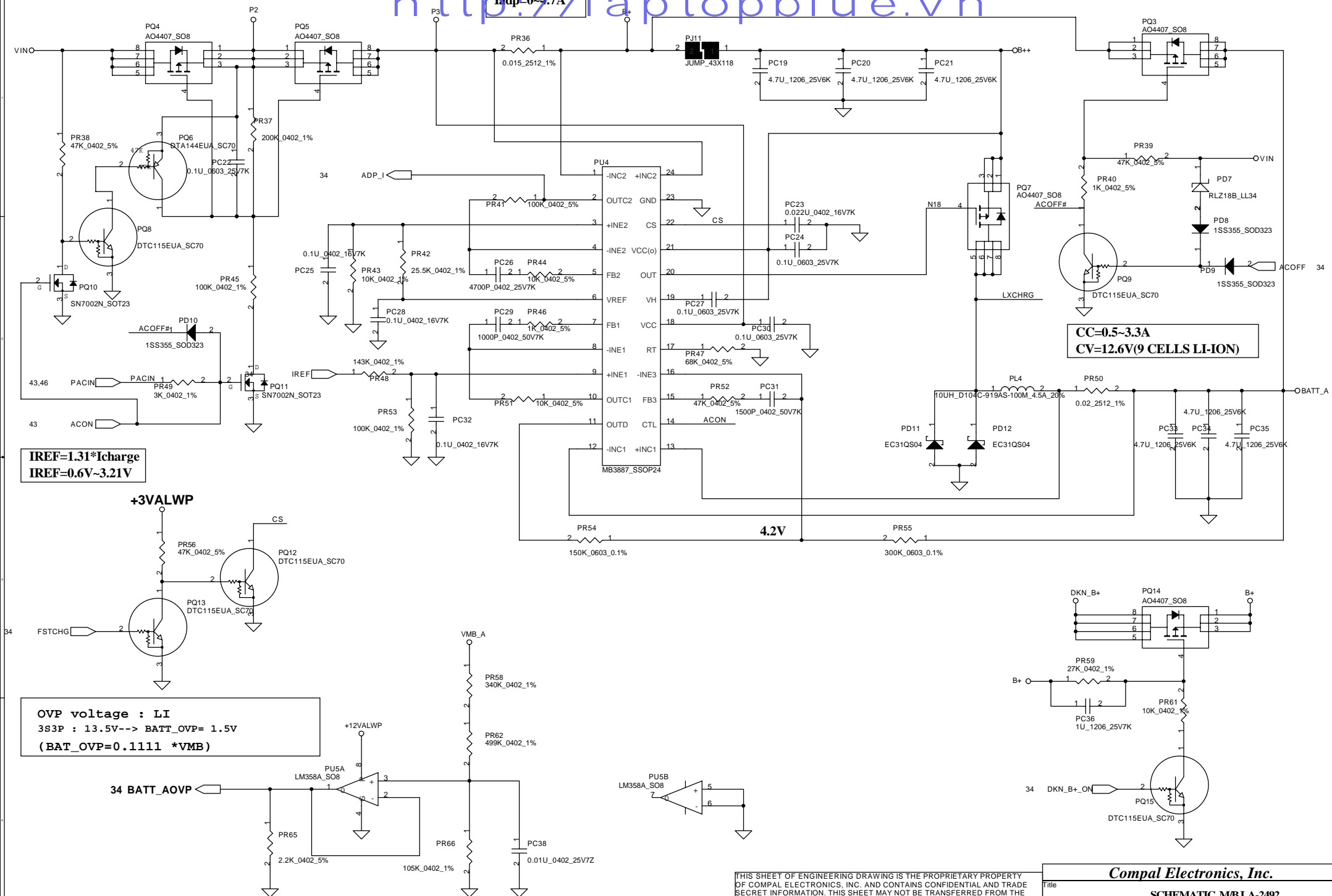
14.3V/13.18V for adapter

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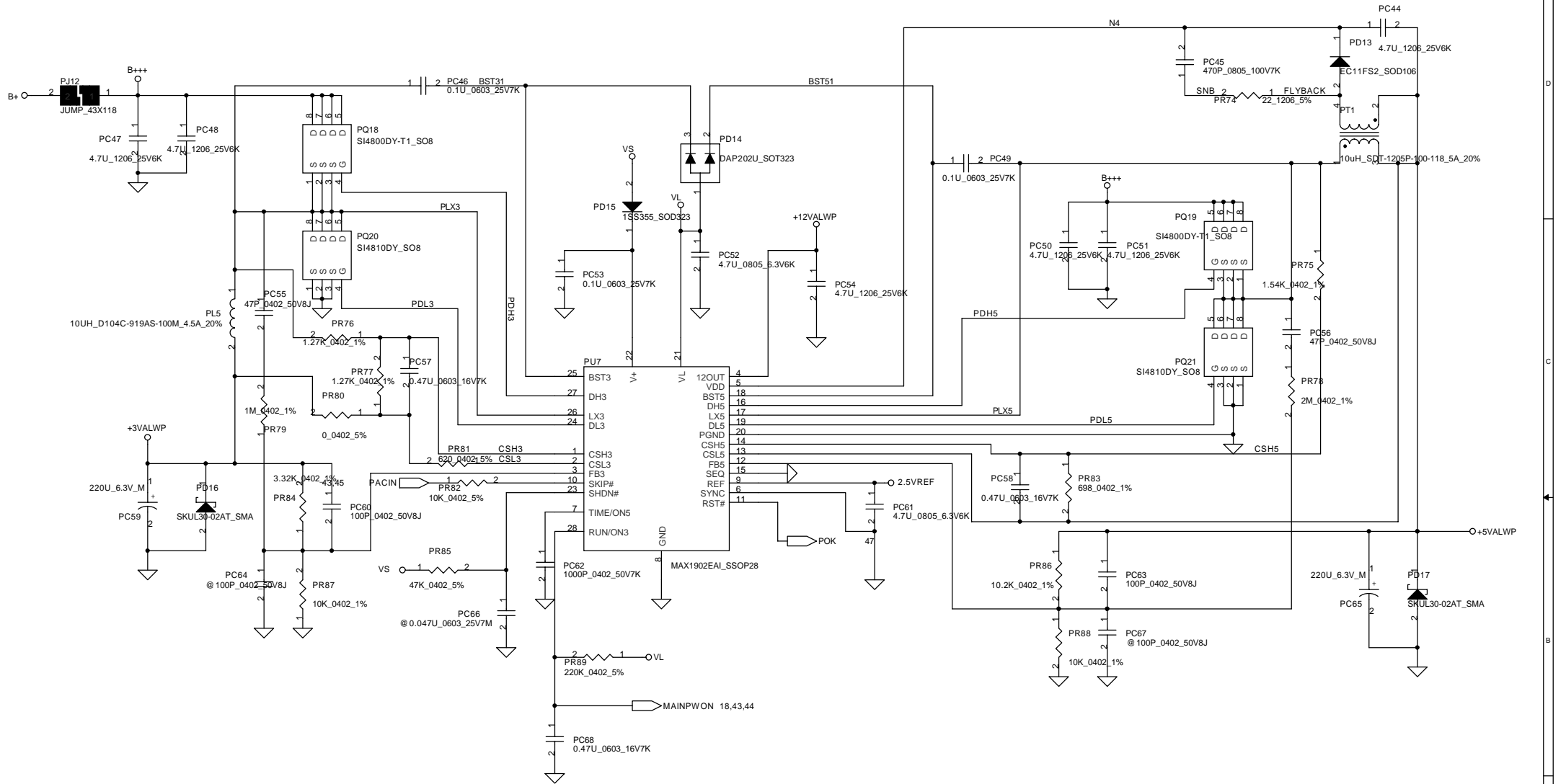


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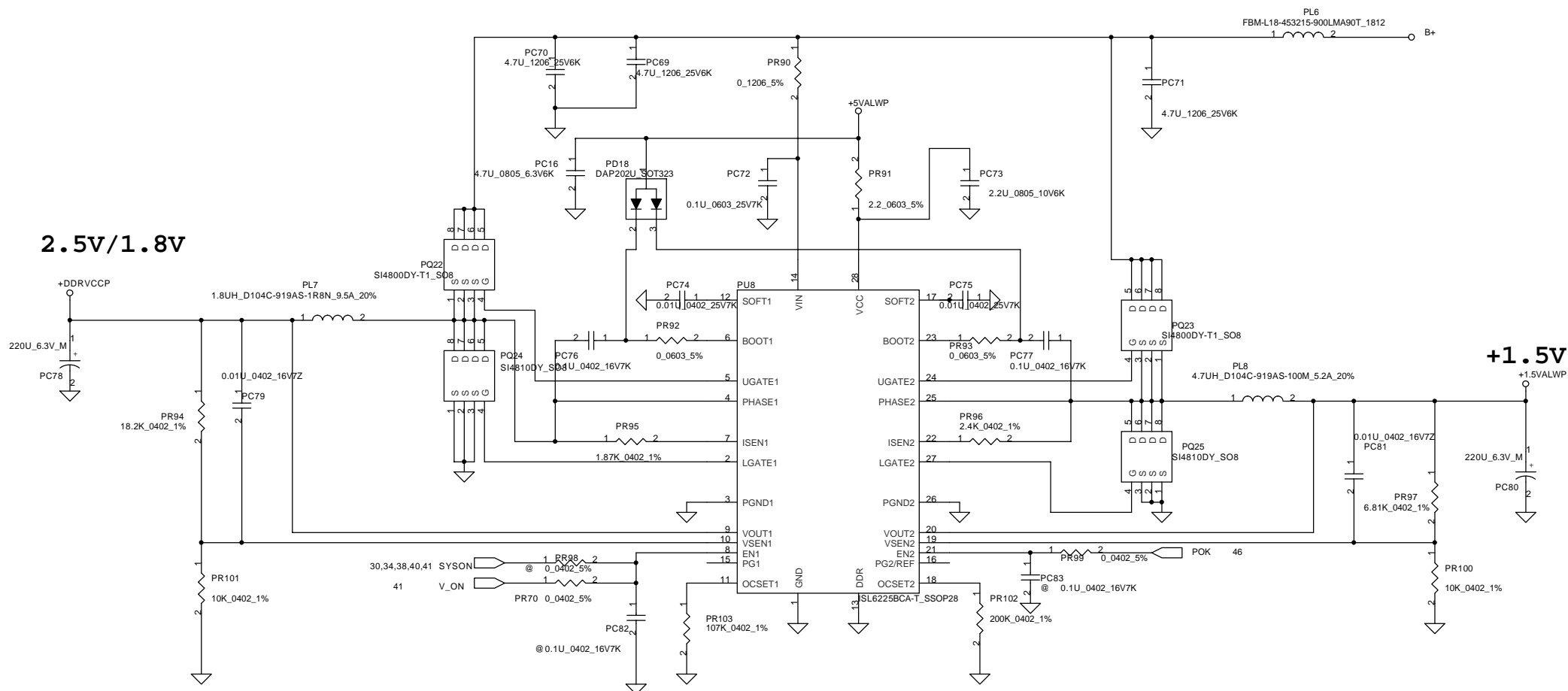
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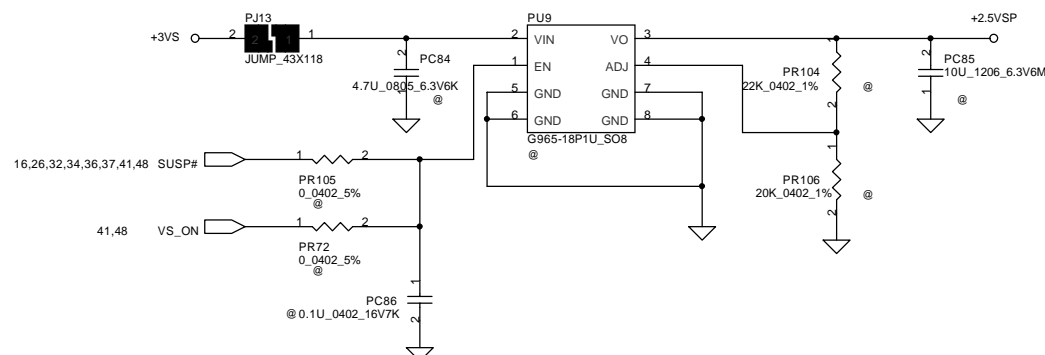


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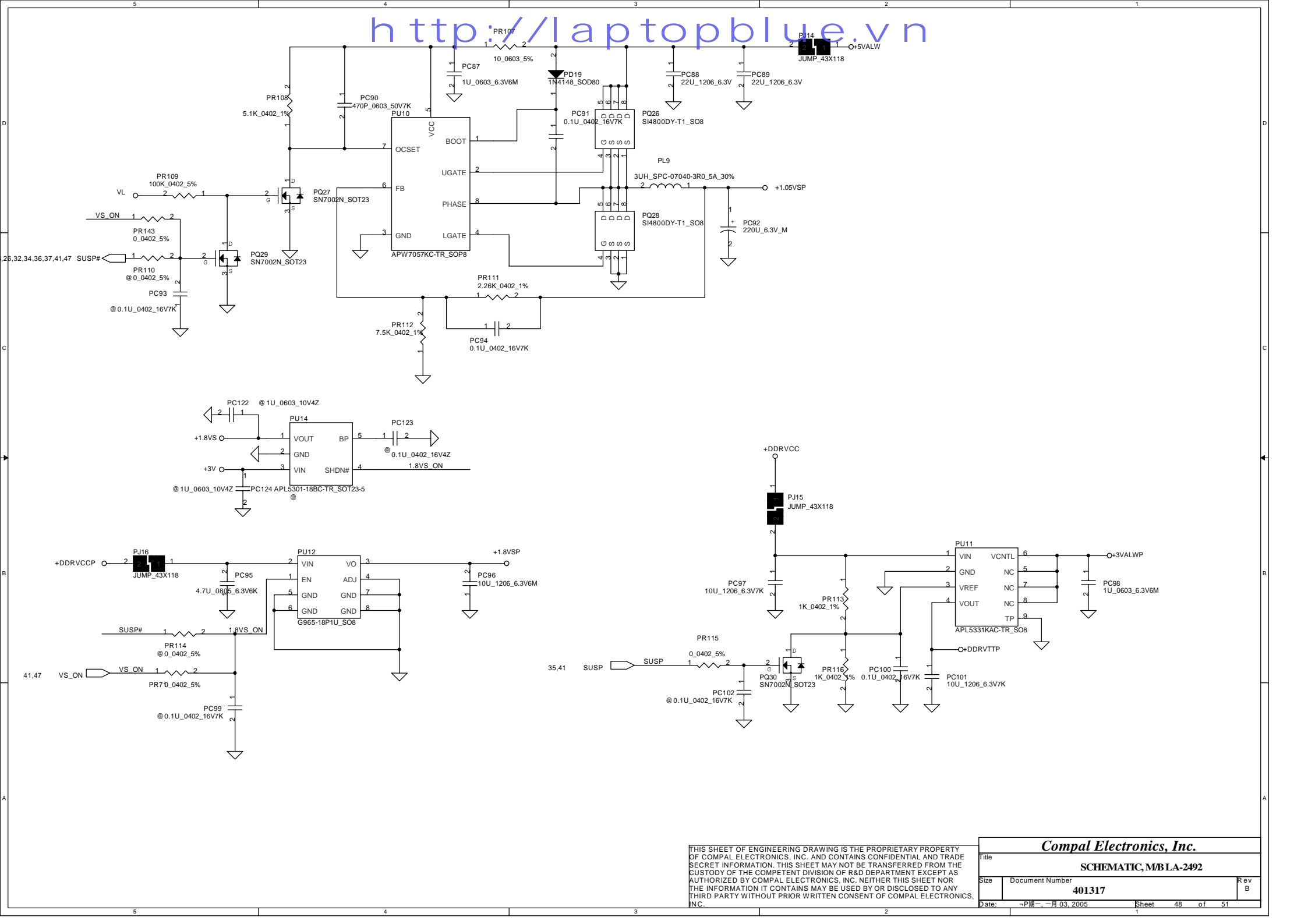
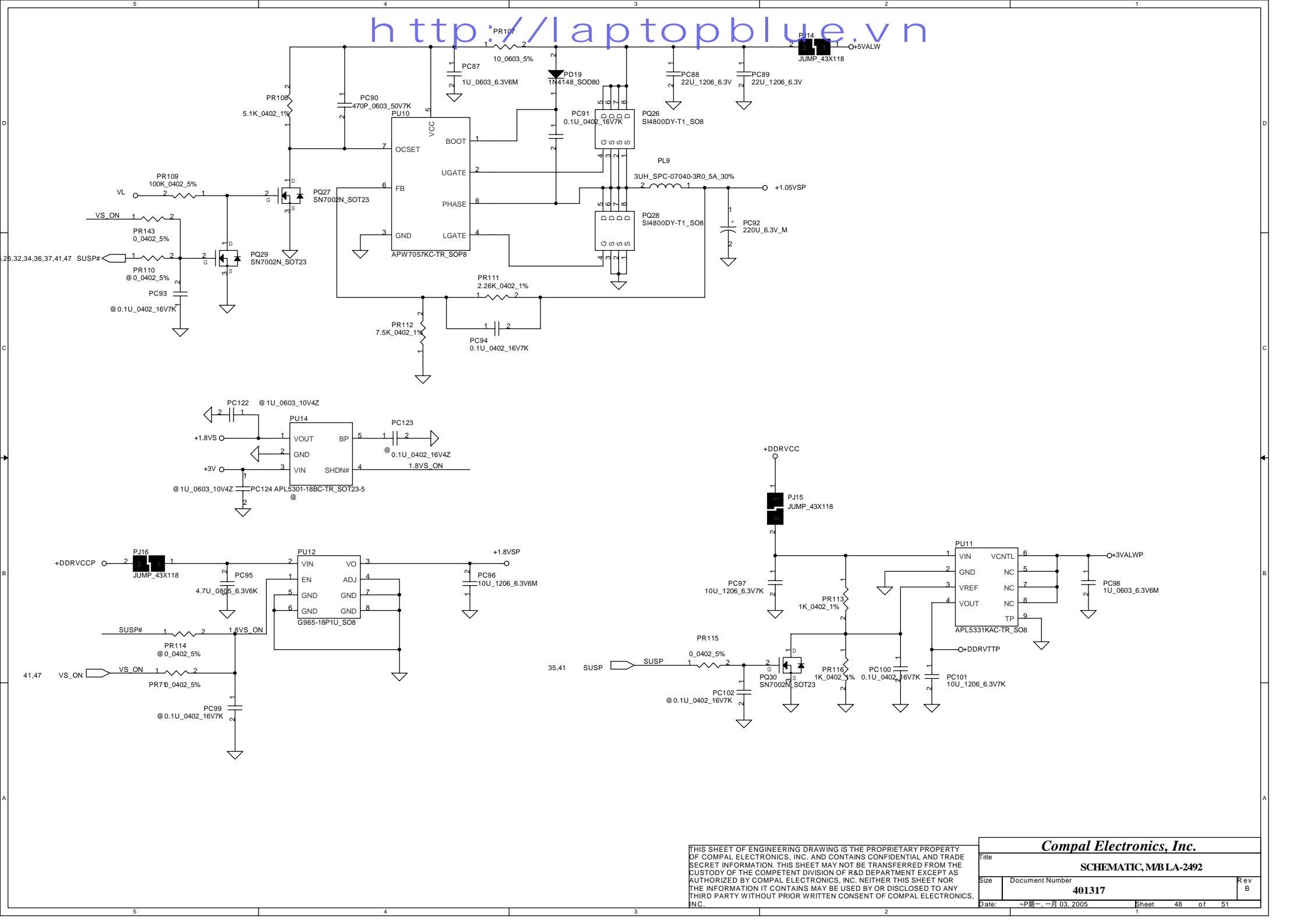
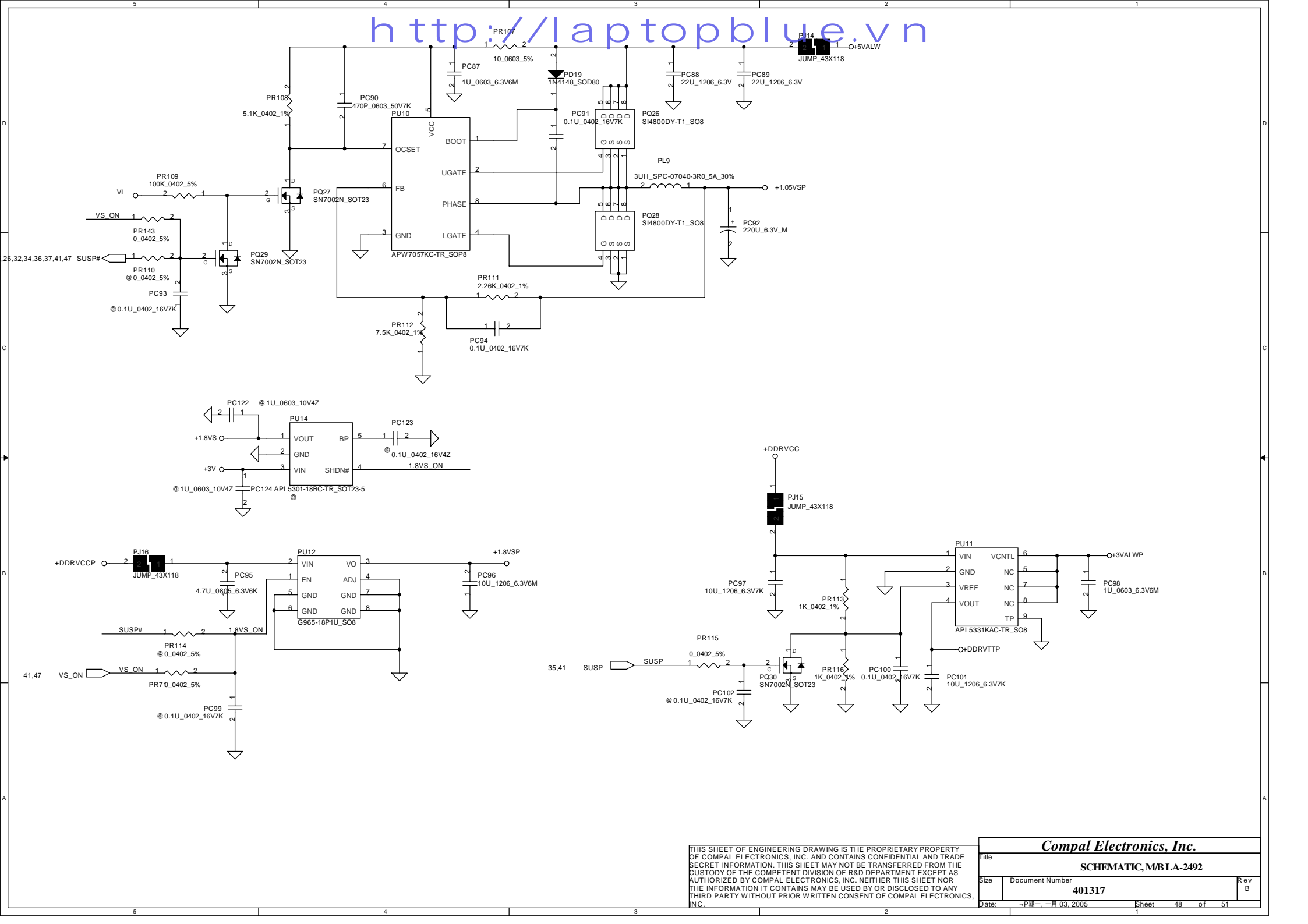
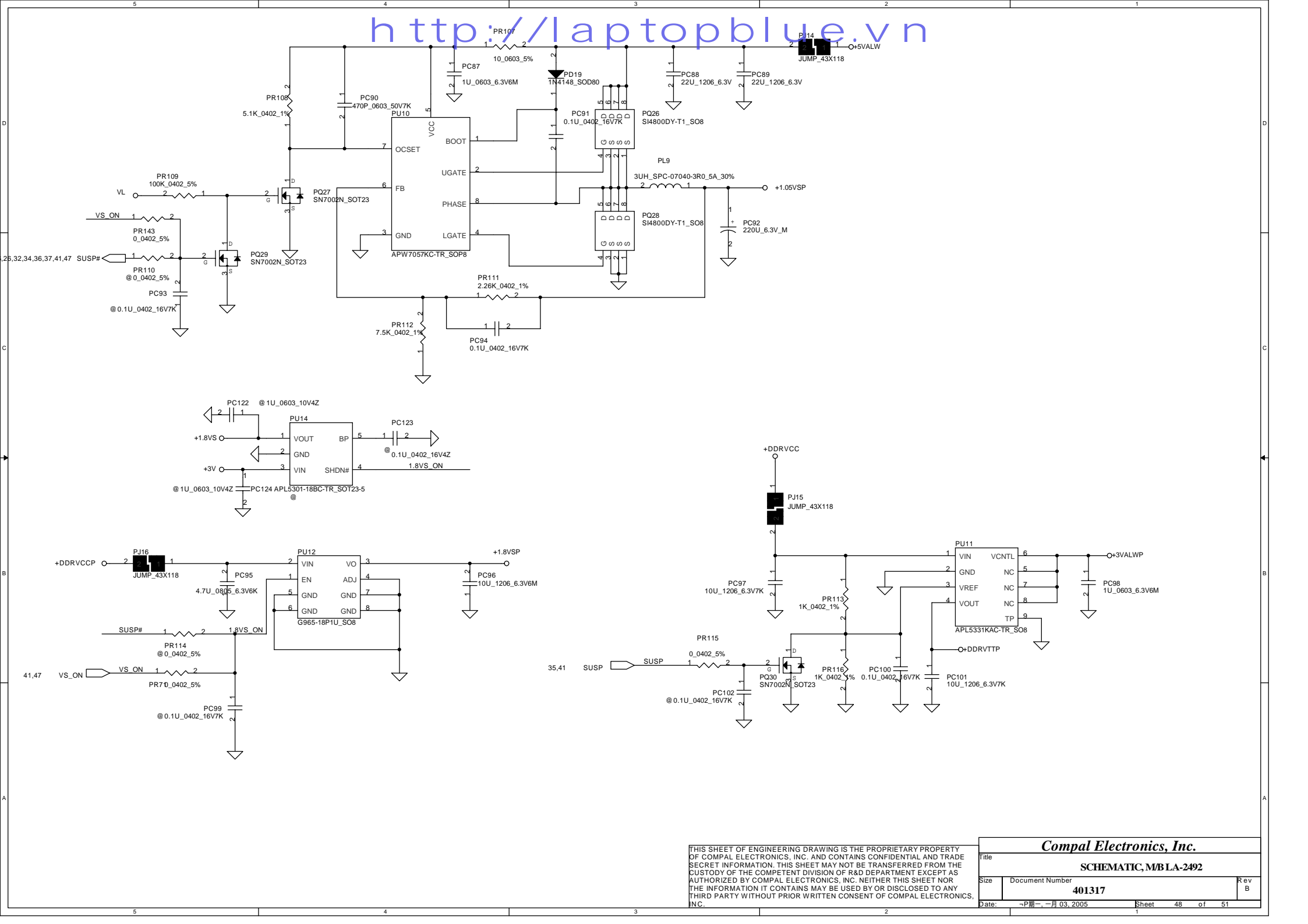
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	PR94	UNPOP
DDRI	18.2K_0402_1% (2.5V)	PU9,PC84,PR105,PR104,PR106,PC85
DDRII	10K_0402_1% (1.8V)	PU12,PC95,PR114,PC96



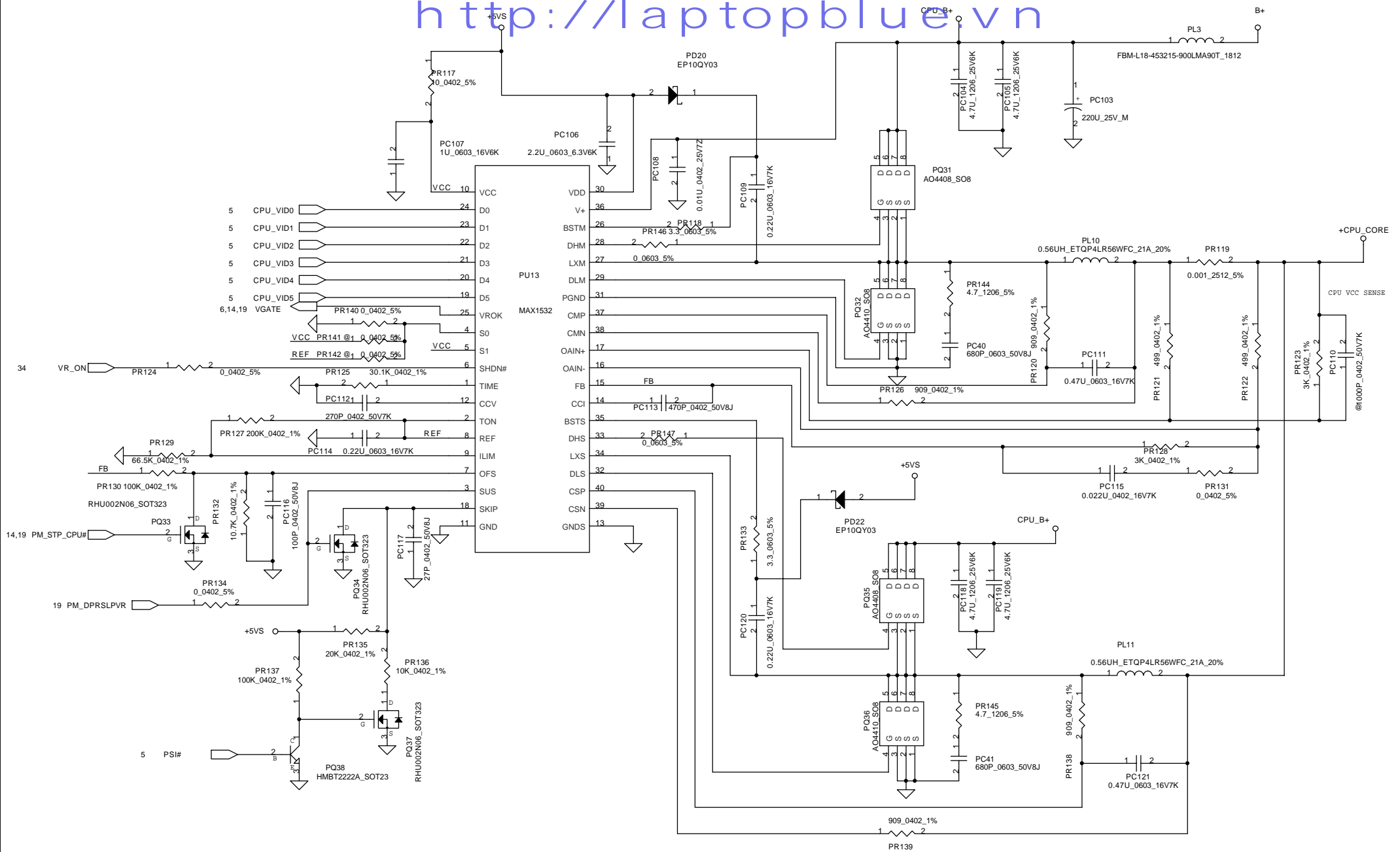
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EAT10 PIR List

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***** Rev:0.2 PIR List 2004/10/26 Writer by Sam Tsai *****

P04:Add @ in R28	Intel Recommend
P06:Add @ in C441, C427 D12J29 C460 Change Value from 220U to 330U	Power Team testing OK
P12:+3VS change from JP25.196 to JP25.194	Intel Recommend
P15:New add R570, R571 & R572 New add L33 Del D2 & D25	RGB without Docking EMI EMI
P16:Change U44 from 7404 to 74125	LCDVDD Soft-Start
P18:New add R573 R439 Change Value from 180K to 20K C271 Change Value from 0.1U to 1U	Intel Recommend Intel Recommend Intel Recommend
P20:R214 Change Value from 1K to 10ohm	Intel Recommend
P22:New add @R , @R& Q	SWDJ testing
P24:New add R586 New add @R581	TI Recommend
P25:New add R582, R583, @R584, R585, R588, R589 & @C685	TI Recommend
P27:R73 Change Value from 4.99K to 4.7K	Marvll Recommend
P31:R361 & R371 Change Value from 47K to 22K P33:New add R543, R544 P32:Modify C399 Net to SPKL+	Design Change Design Change Design Change
P33:New add L34 add@ in C647 ~ C662	EMI
P34:New add R587	Design Change
P35:New add JP32 & C671 New add C682 ~ C684 JP13 reverse	Design Change EMI Design Change
P36:New add	SWDJ testing
P37:SW1 change to 1BS003-1211L_3P	Design Change
P38:Q52.3 change from +3VALW to +3V Q57.3 change from +5VALW to +5VS Lid Switch IC Power change from JP16.26 +3VALW to JP16.27 New add C672 ~ C681	Design Change RTCVREF EMI
P39:New add R574	Design Change
P40:Del D11	Design Change

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List) for Power Circuit

A vertical bar is divided into four segments labeled A, B, C, and D from bottom to top. An arrow points to the boundary between segments B and C.

	1
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