

Compal confidential

Hamburg 10ADG

NALAE LA-6052P Schematics Document

Mobile AMD S1G4/ RS880M / SB820M

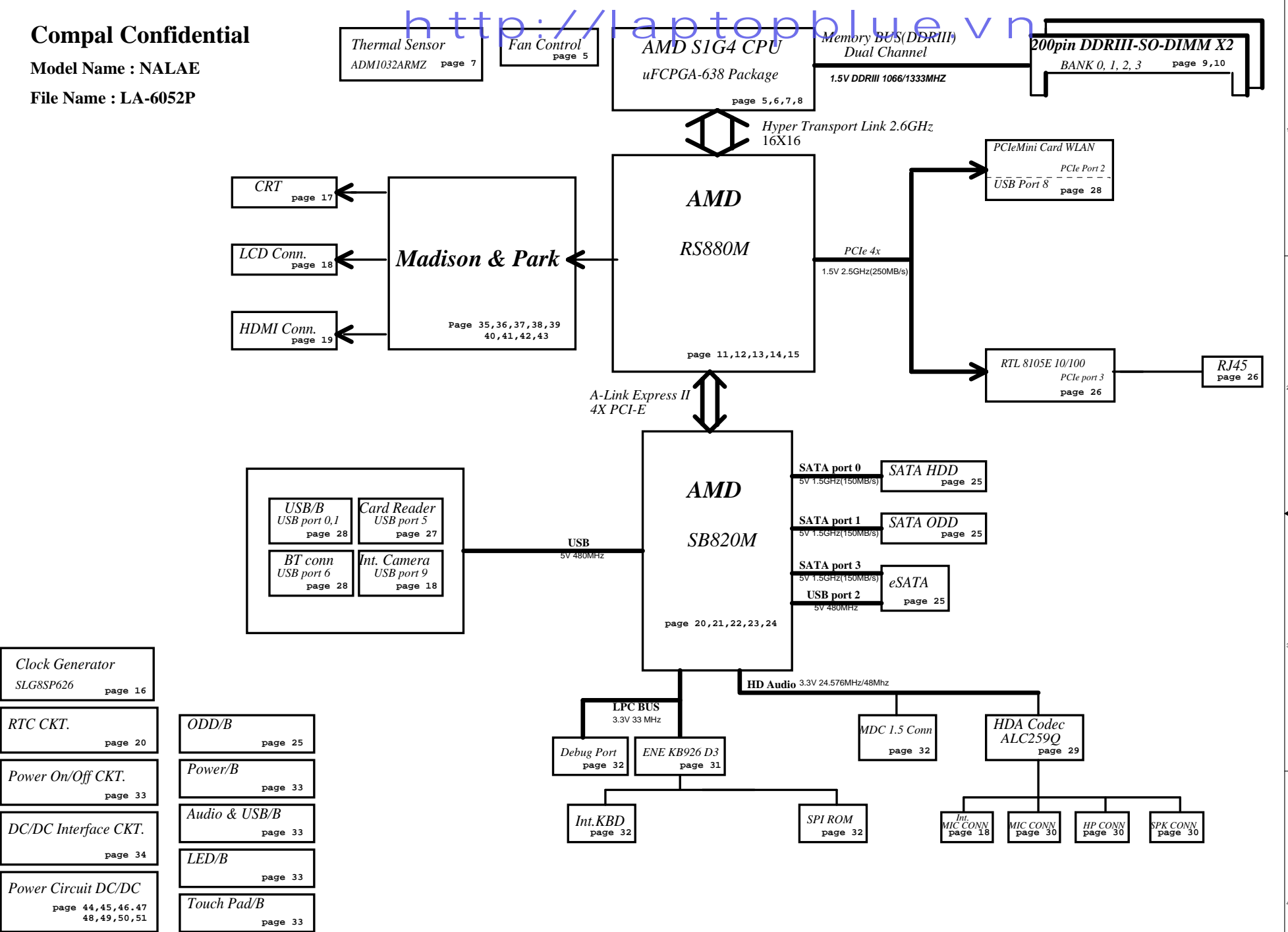
2009-11-27 Rev. 0.2

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2008-09-25	Deciphered Date	2009-09-25	Title	SCHEMATIC, MB A6052
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	401851
				Date:	Wednesday, January 20, 2010
				Sheet	1 of 53

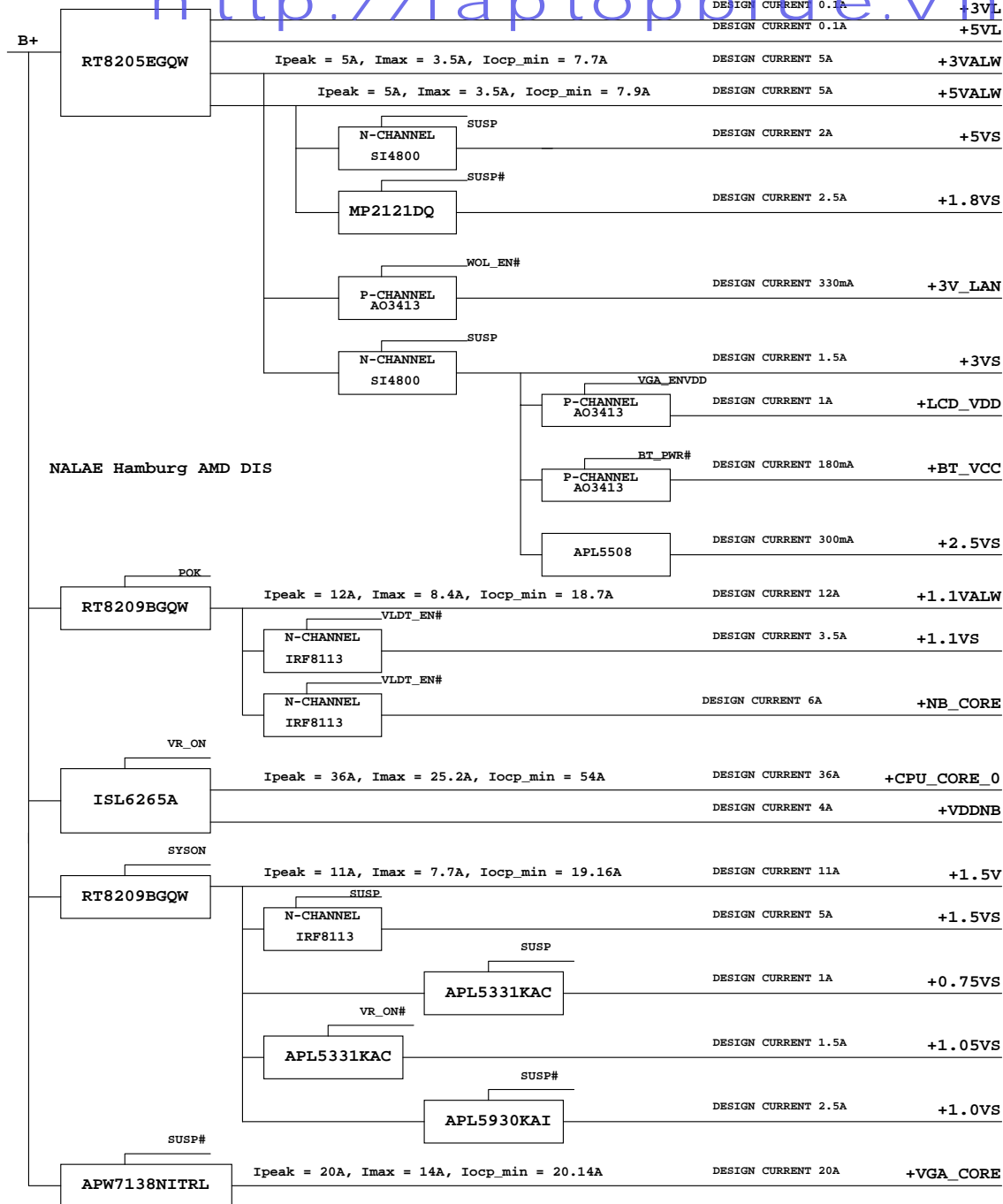
Compal Confidential

Model Name : NALAE

File Name : LA-6052P



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008-09-25	Deciphered Date	2009-09-25	Title	SCHEMATIC, MB A6052
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	401851
				Date	Wednesday, January 20, 2010
				Sheet	2 of 53
				Rev	A



Voltage Rails

O : ON
X : OFF

power plane	State	B+ +3VL +5VL +RTCVC	+5VALW +3VALW +1.1VALW	+1.5V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +1.05VS +0.75VS +VGA_CORE +VDDNB +CPU_CORE +NB_CORE
S0		O	O	O	O
S1		O	O	O	O
S3		O	O	O	X
S5 S4/AC		O	O	X	X
S5 S4/ Battery only		O	X	X	X
S5 S4/AC & Battery don't exist		X	X	X	X

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 X
DDR SO-DIMM 1	A2	1 0 1 0 0 0 1 X
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

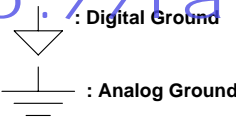
EC SM Bus1 address

Device	HEX	Address
Smart Battery	16H	0001 011X b
HDMI-CEC	34H	0011 010X b
EC KB926D4		

EC SM Bus2 address

Device	HEX	Address
ADH1032-1 CPU	98H	1001 100X b
ADH1032-2 VGA	9AH	1001 101X b
EC KB926D3		

Symbol Note :



@ : just reserve , no build

Platform	CPU	NB	VGA	SB	Comment
Danube	S1G4	RS880M	NA	SB820M	

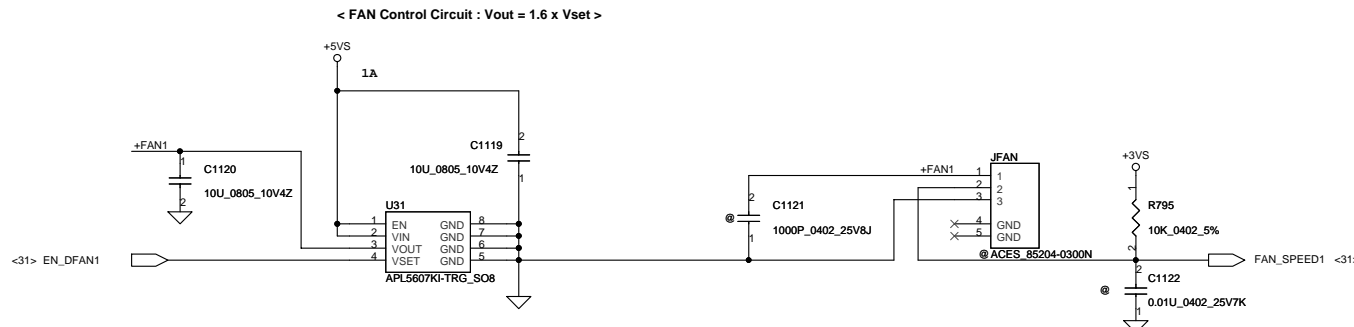
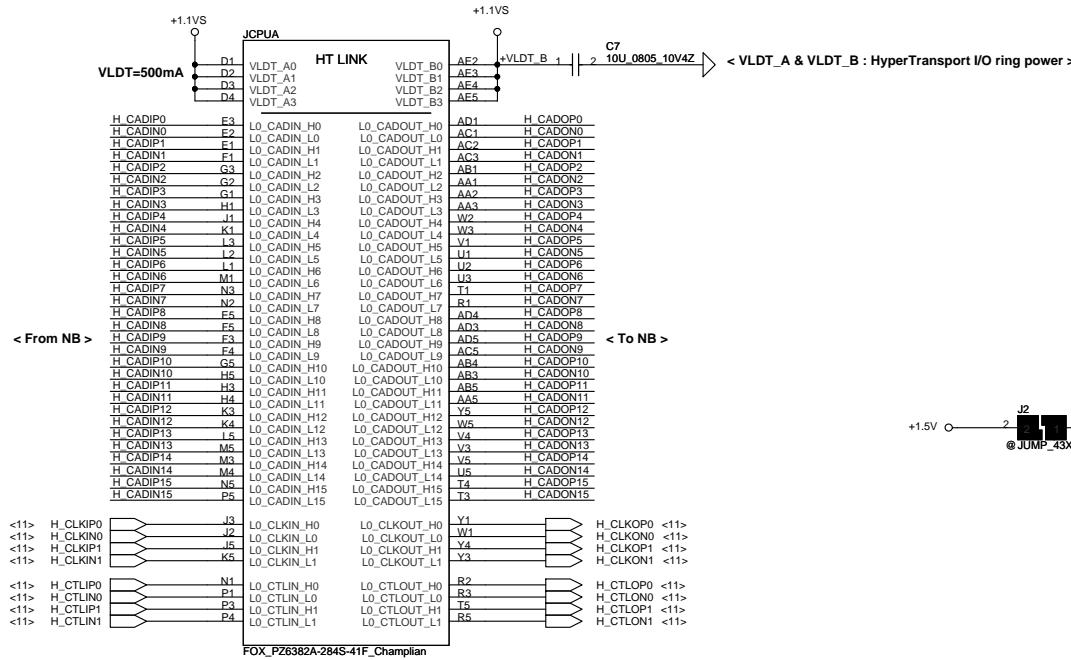
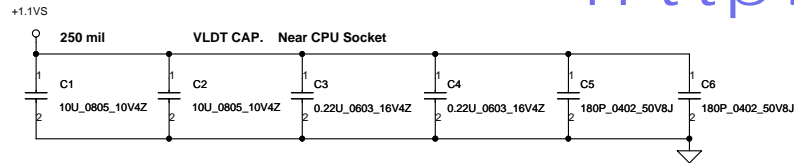
GPU	CPU	NB	VGA	SB	Comment
Manhattan	S1G4	RS880M	MADISON	SB820M	MANHA@+MADISON@ or PARK@+
M9X	S1G4	RS880M	M96	SB820M	M9X@+M92@ +4PCS or 8PCS

BTO (Build-To-Order) Option Table

Function	BLUE TOOTH	HDMI				
Description	(B)	(Y)				
Explain						
BTO	BT@	H@				

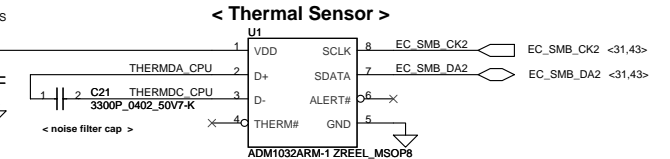
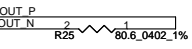
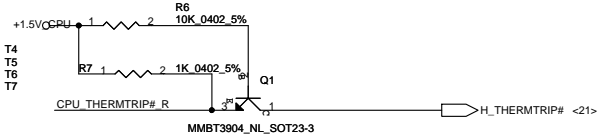
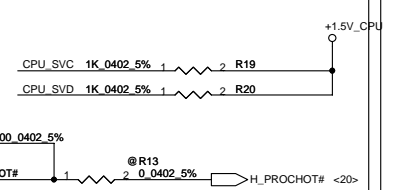
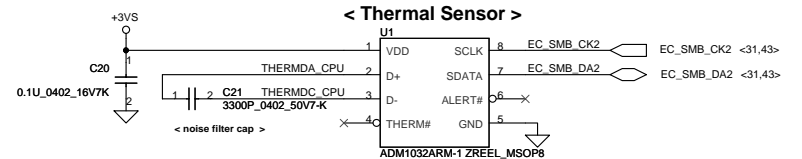
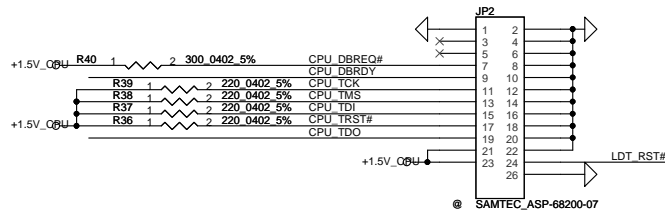
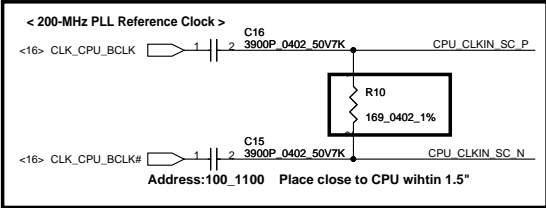
SMBUS Control Table

	SOURCE	BATT	CPU THERMAL SENSOR	SODIMM I / II	CLK GEN	WLAN	LCD DDC ROM	HDMI DDC ROM
EC_SMB_CK1 EC_SMB_DA1	KB926	V						
EC_SMB_CK2 EC_SMB_DA2	KB926		V					
I2C_CLK I2C_DATA	RS880M						V	
DDC_CLK0 DDC_DATA0	RS880M							V
SCL0 SDA0	SB820			V	V			
SCL1 SDA1	SB820					V		



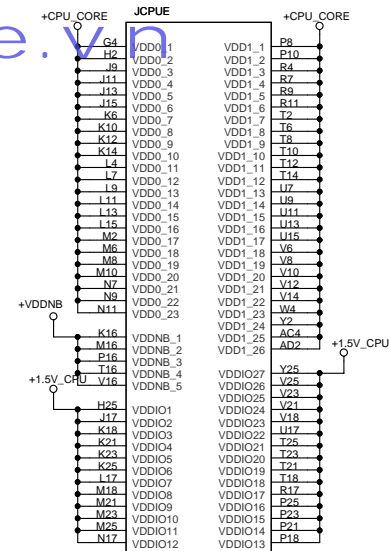
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2008-09-25	Deciphered Date	2009-09-25	Title	SCHEMATIC, MB A6052
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	401851
				Date	Wednesday, January 20, 2010
				Sheet	5 of 53

Security Classification	Compal Secret Data			Compal Electronics, Inc. SCHEMATIC, MB A6052		
Issued Date	2008-09-25	Deciphered Date	2009-09-25	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RESEARCH AND DEVELOPMENT DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number 401851	Rev A	
				Date:	Wednesday, January 20, 2010	Sheet 6 of 53

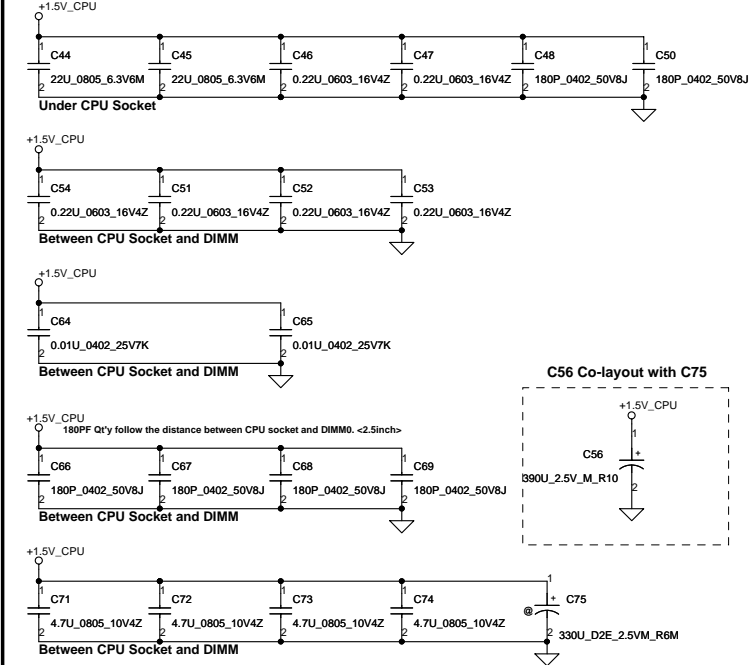


Security Classification		Compal Secret Data		Compal Electronics, Inc. SCHEMATIC, MB A6052	
Issued Date	2008-09-25	Deciphered Date	2009-09-25	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev A
				401851	
Date:				Wednesday, January 20, 2010	Sheet 7 of 53

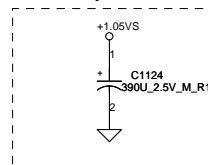
Diagram illustrating a network connection from a laptop to a JCUPE server. The laptop is labeled "laptop" and the server is labeled "JCUPE". The connection is labeled "http://laptopblue.vpn". The diagram shows the physical connection (cable) and the logical connection (VPN tunnel).



JCPUF



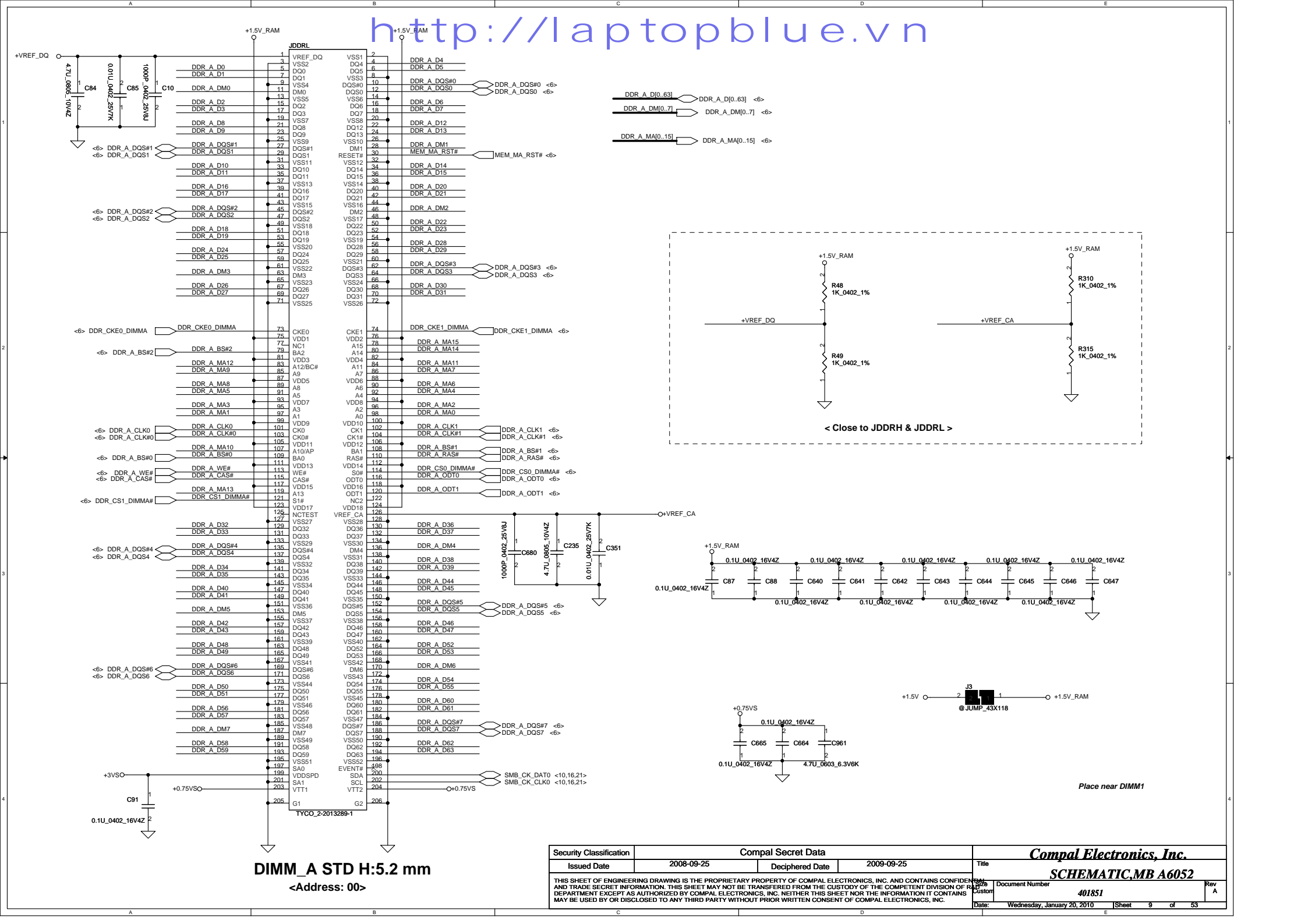
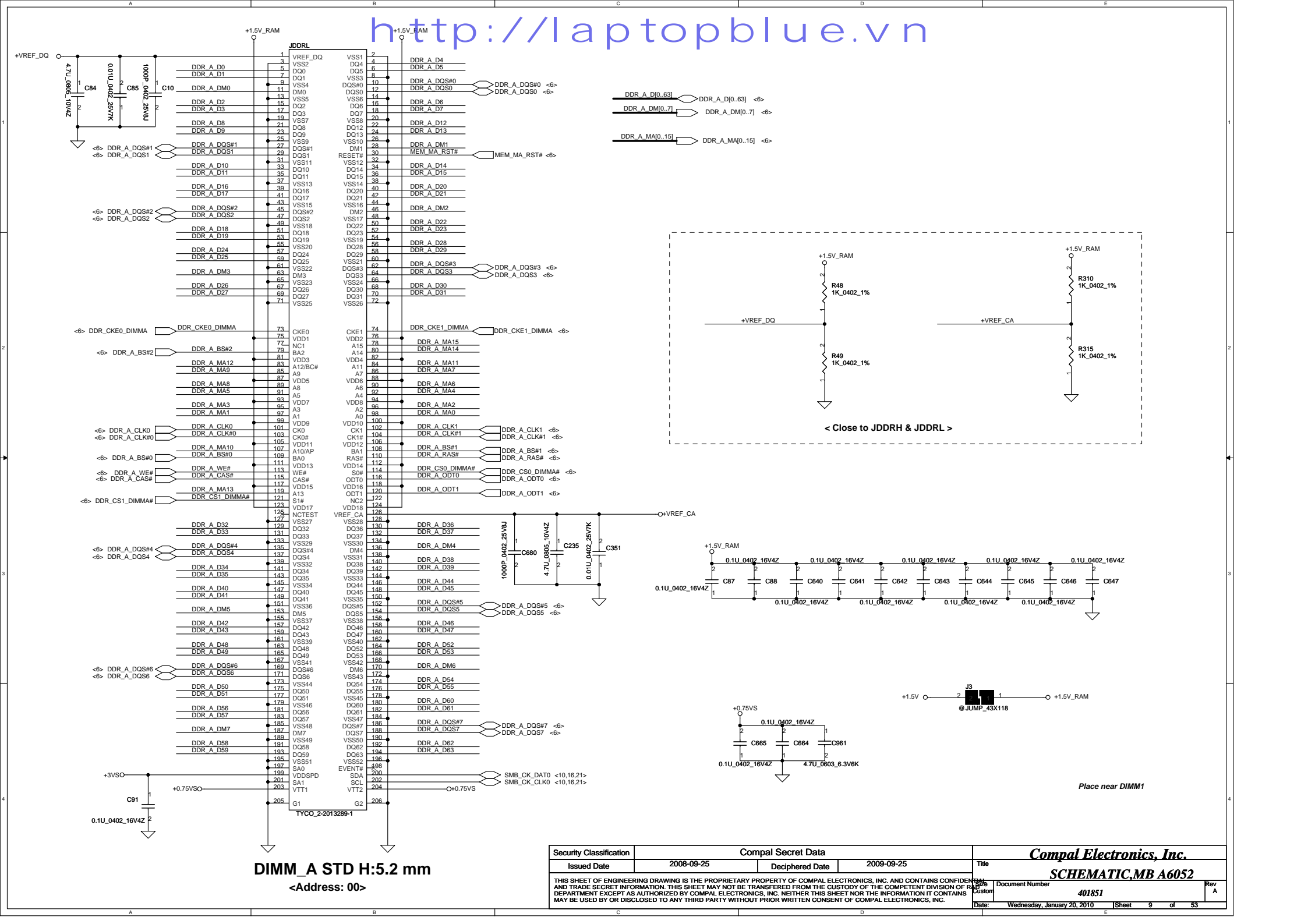
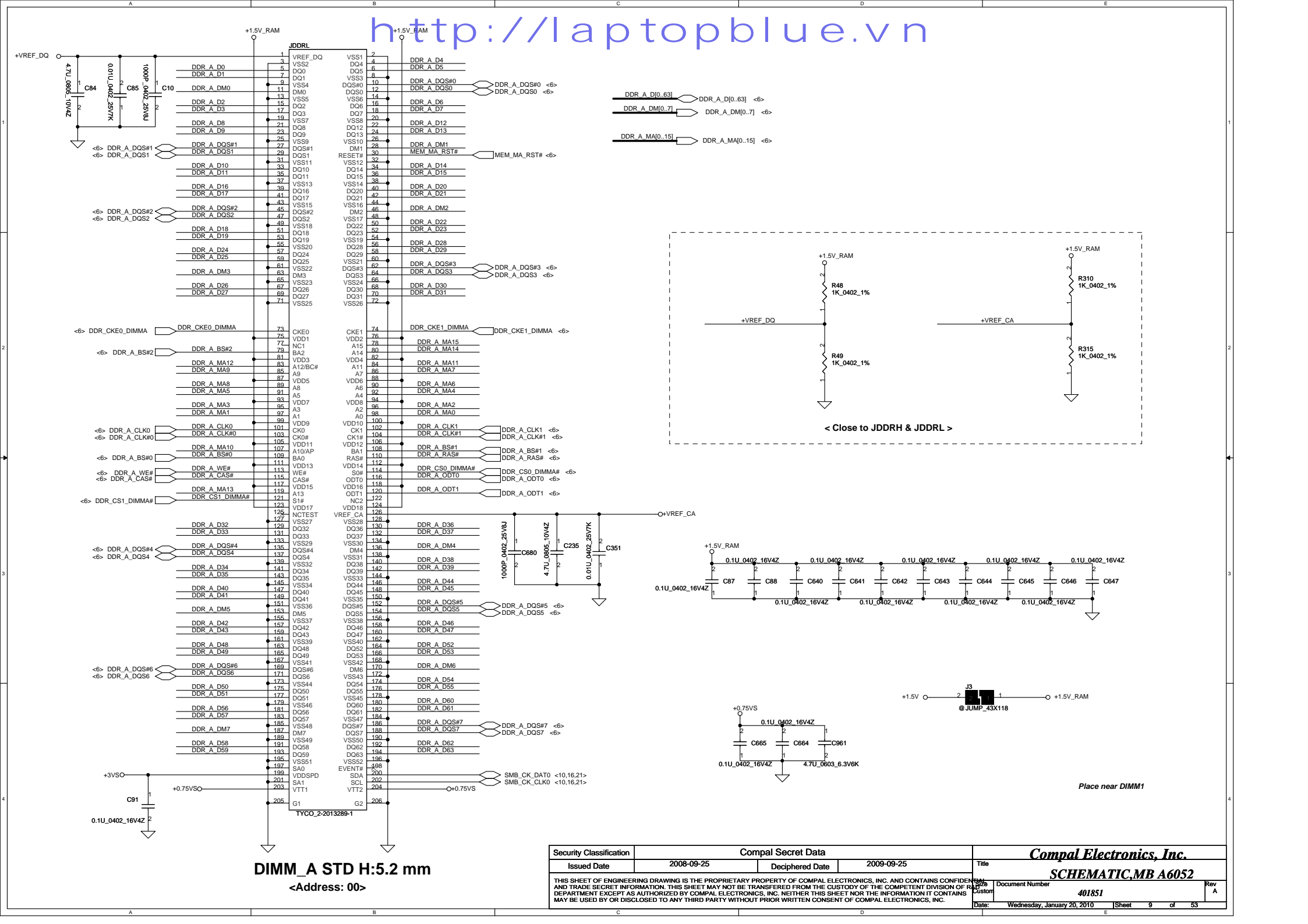
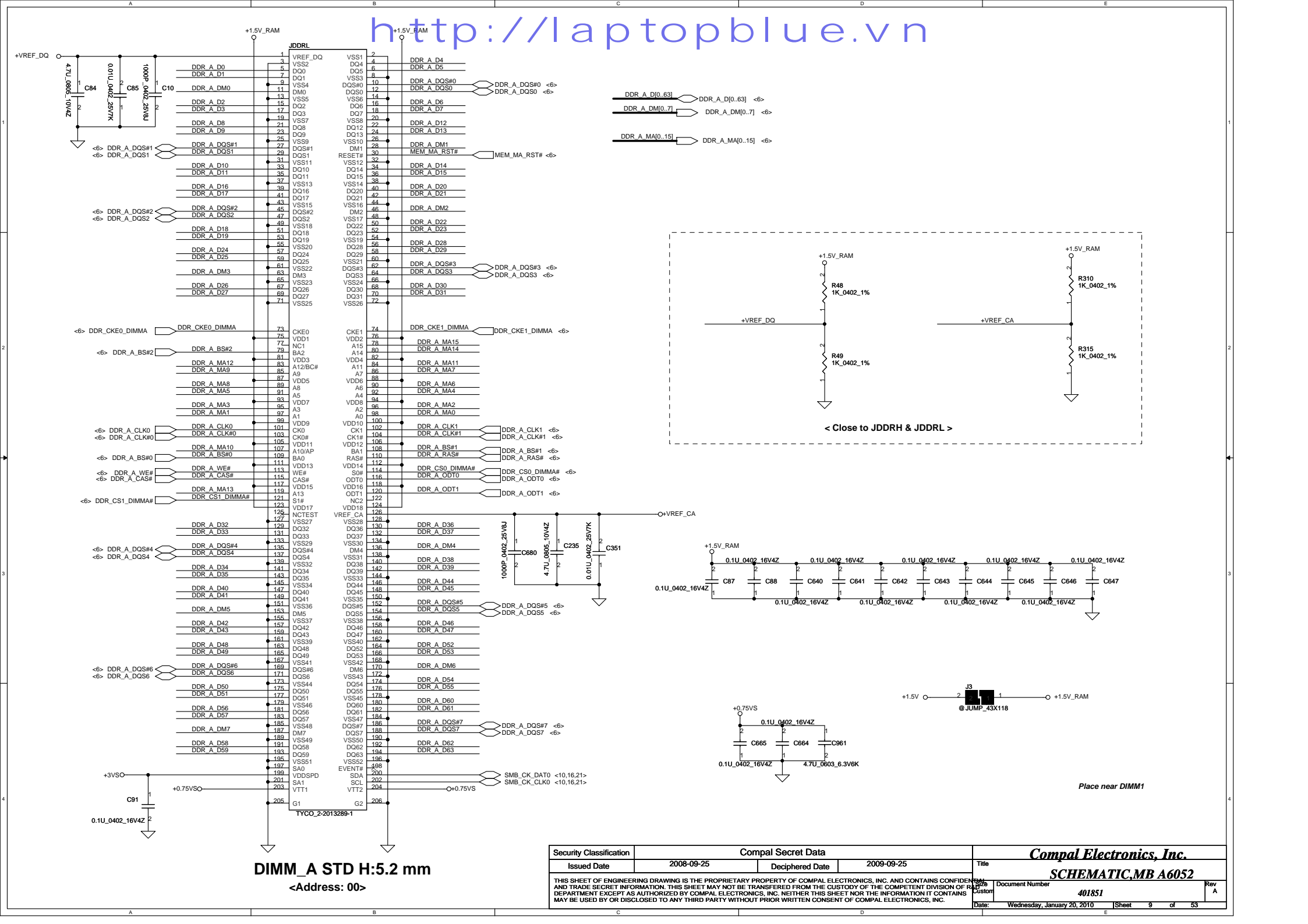
C1124 Co-layout with C1125



JCPU1			
A44	VSS31	VS566	J6
AA11	VSS2	VS567	J8
AA13	VSS3	VS568	J10
AA15	VSS4	VS569	J12
AA17	VSS5	VS570	J14
AA19	VSS6	VS571	J16
AB2	VSS7	VS572	J18
AB7	VSS8	VS573	K2
AB9	VSS9	VS574	K9
AB23	VSS10	VS575	K11
AB25	VSS11	VS576	K13
AC11	VSS12	VS577	K15
AC13	VSS13	VS578	K17
AC15	VSS14	VS579	K19
AC17	VSS15	VS580	L8
AD19	VSS16	VS581	L10
AD21	VSS17	VS582	L12
AD6	VSS18	VS583	L14
AD8	VSS19	VS584	L16
AD25	VSS20	VS585	L18
AE11	VSS21	VS586	M2
AE13	VSS22	VS587	M7
AE15	VSS23	VS588	AC6
AE17	VSS24	VS589	M17
AE19	VSS25	VS590	N4
AE21	VSS26	VS591	N8
AE23	VSS27	VS592	N10
B4	VSS28	VS593	N16
B6	VSS29	VS594	N18
B8	VSS30	VS595	P2
B11	VSS31	VS596	P7
B13	VSS32	VS597	P9
B15	VSS33	VS598	P11
B17	VSS34	VS599	P17
B19	VSS35	VS100	R2
B21	VSS36	VS101	R10
B23	VSS37	VS102	R16
B25	VSS38	VS103	R18
D6	VSS39	VS104	T7
D8	VSS40	VS105	T9
D9	VSS41	VS106	T11
D11	VSS42	VS107	T13
D13	VSS43	VS108	T15
D15	VSS44	VS109	T17
D17	VSS45	VS110	T19
D19	VSS46	VS111	U8
D21	VSS47	VS112	U10
D23	VSS48	VS113	U12
D25	VSS49	VS114	U14
D26	VSS50	VS115	U16
F4	VSS51	VS116	U18
F11	VSS52	VS117	V2
F13	VSS53	VS118	V12
F15	VSS54	VS119	V17
F17	VSS55	VS120	V19
F19	VSS56	VS121	V21
F21	VSS57	VS122	V23
F23	VSS58	VS123	V13
F25	VSS59	VS124	V15
H9	VSS60	VS125	V6
H7	VSS61	VS126	W1
H21	VSS62	VS127	Y23
H23	VSS63	VS128	N6
H25	VSS64	VS129	
J4	VSS65		

FOX_PZ6382A-284S-41F_Champlian

Security Classification		Compal Secret Data		Compal Electronics, Inc. SCHEMATIC, MB A6052	
Issued Date	2008-09-25	Deciphered Date	2009-09-25	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Doc No	
				Custom	401851
				Date:	Wednesday, January 20, 2010
				Sheet	8 of 53



http://laptopblue.vn

http://laptopblue.vn

DIMM_A STD H:5.2 mm
<Address: 00>

Security Classification
 Issued Date: 2008-09-25
 Deciphered Date: 2009-09-25
 Title: **Compal Secret Data**

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.
SCHEMATIC_MB A6052
 Document Number: 401851
 Date: Wednesday, January 20, 2010
 Sheet 9 of 53

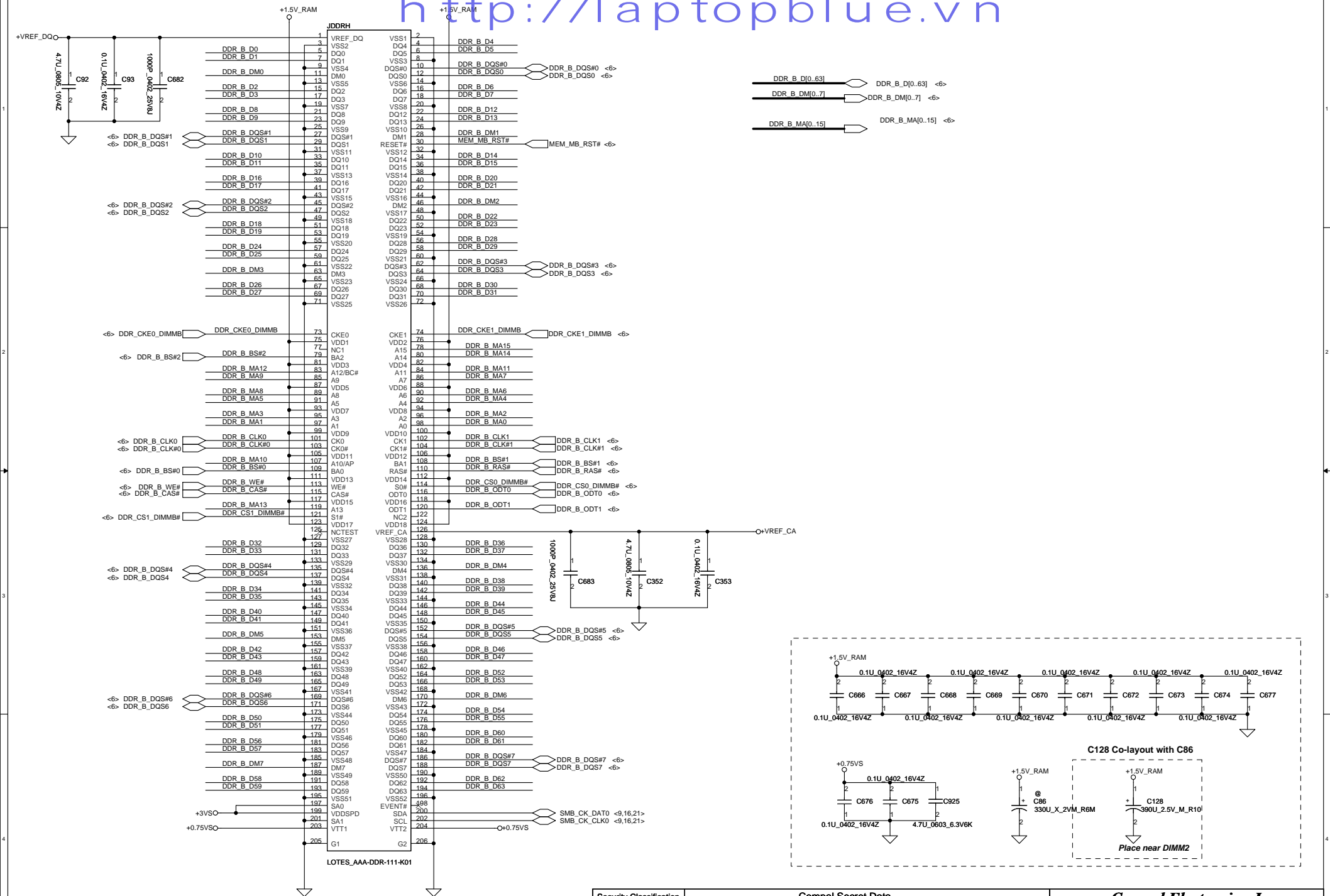
http://laptopblue.vn

DIMM_A STD H:5.2 mm
<Address: 00>

Security Classification
 Issued Date: 2008-09-25
 Deciphered Date: 2009-09-25
 Title: **Compal Secret Data**

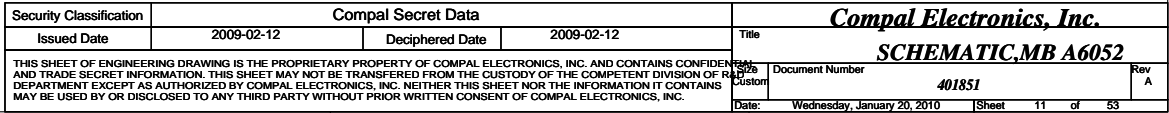
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

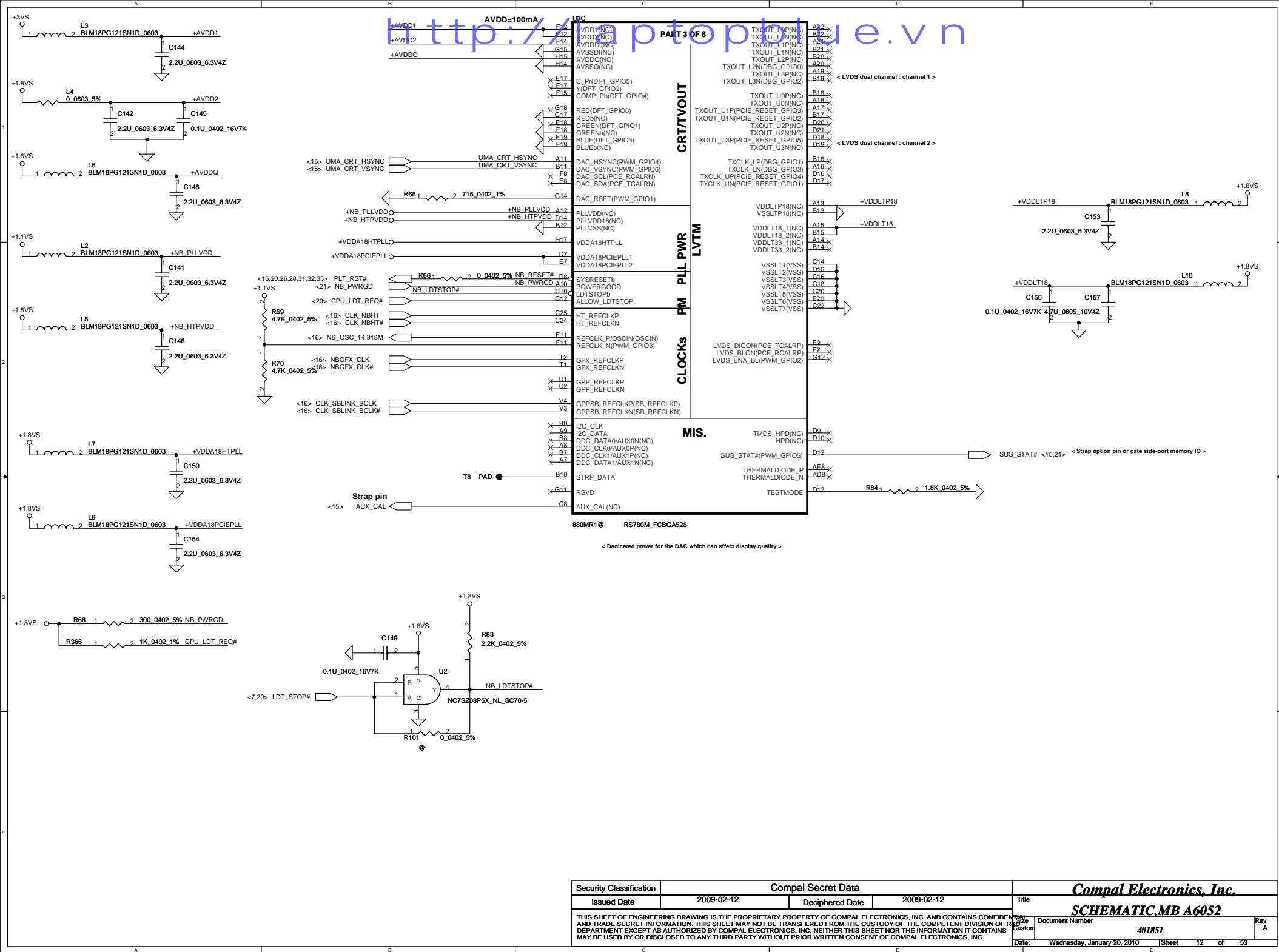
Compal Electronics, Inc.
SCHEMATIC_MB A6052
 Document Number: 401851
 Date: Wednesday, January 20, 2010
 Sheet 9 of 53



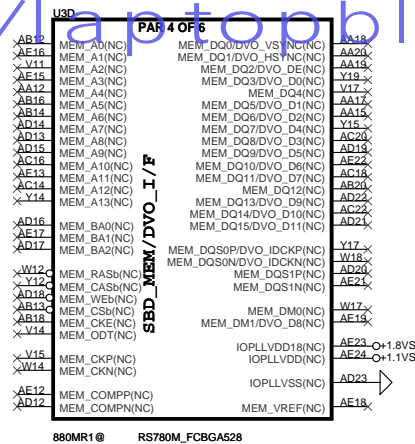
DIMM_B STD H:9.2 mm
<Address: 01>

Security Classification		Compal Secret Data		Title	
Issued Date	2008-09-25	Deciphered Date	2009-09-25	SCHEMATIC, MB A6052	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	401851
				Date:	Wednesday, January 20, 2010
				Sheet	10 of 53

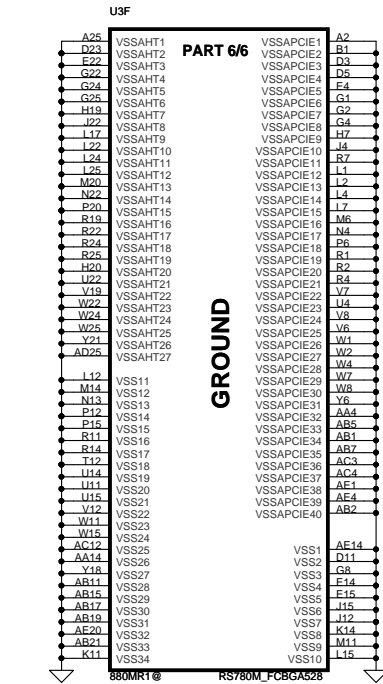




Security Classification		Compal Secret Data		Compal Electronics, Inc. SCHEMATIC, MB A6052	
Issued Date		2009-02-12		Title	
		Deciphered Date		2009-02-12	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number 401851	
				Rev A	
				Date: Wednesday, January 20, 2010	
				Sheet 12 of 53	

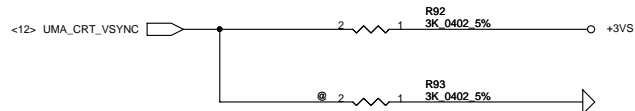


Security Classification		Compal Secret Data				Compal Electronics, Inc.							
Issued Date		2009-02-12		Deciphered Date		2009-02-12		Title		SCHEMATIC,MB A6052			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.										Rev		A	
										Document Number		401851	
										Date:		Wednesday, January 20, 2010	



Security Classification		Compal Secret Data		Compal Electronics, Inc. SCHEMATIC, MB A6052	
Issued Date	2009-02-12	Deciphered Date	2009-02-12	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev. A
				Customer	
				Date:	Wednesday, January 20, 2010
				Sheet	14 of 53

< RS880 VSYNC mux at CRT_VSYNC pull High to 3K >



< RS880 use register to control PCI-E configure >

< VSYNC : STRAP_DEBUG_BUS_GPIO_ENABLEb >

Enables the Test Debug Bus using GPIO.

1 : Disable (RX881, RS880)
0 : Enable (RX881, RS880)

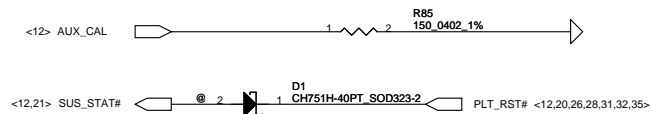
PIN: RS880--> VSYNC#

< DFT_GPIO[4:2] : STRAP_PCIE_GPP_CFG[2:0] >

These pin straps are used to configure PCI-E GPP mode.

000 : 00001
001 : 00010
010 : 01011
011 : 00100
100 : 01010
101 : 01100
111 : 01011

< RS880 SUS_STAT# >



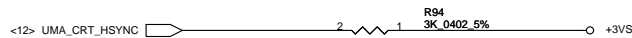
< SUS_SATA# : LOAD_EEPROM_STRAPS >

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS880:SUS_STAT#

< RS880 use HSYNC to enable SIDE PORT (internal pull high) >



< HSYNC : STRAP_DEBUG_BUS_PCIE_ENABLEb >

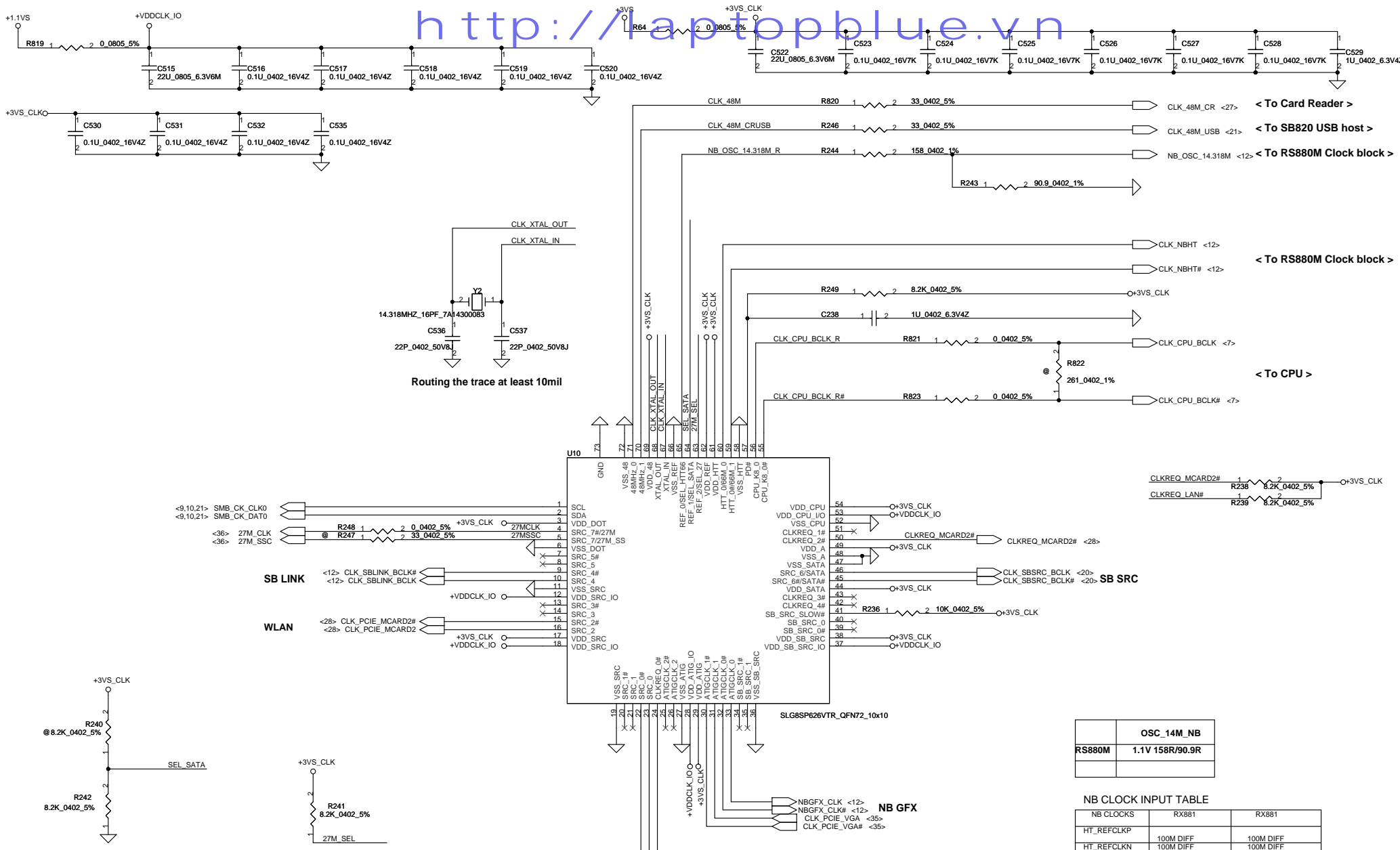
RX881: Enables the Test Debug Bus using PCIE bus

1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

RS880: Enables Side port memory (RS780 use HSYNC#)

1. Disable (RS880)
0 : Enable (RS880)

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2009-02-12	Deciphered Date	2009-02-12	Title	SCHEMATIC, MB A6052
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	401851
				Date	Wednesday, January 20, 2010
				Sheet	15 of 53



SEL_SATA	1	configure as SATA output
	0 *	configure as normal SRC(SRC.6) output * default

27M_SEL	1 *	configure as 27M and 27M_SS output
	0	configure as SRC.7 output * default

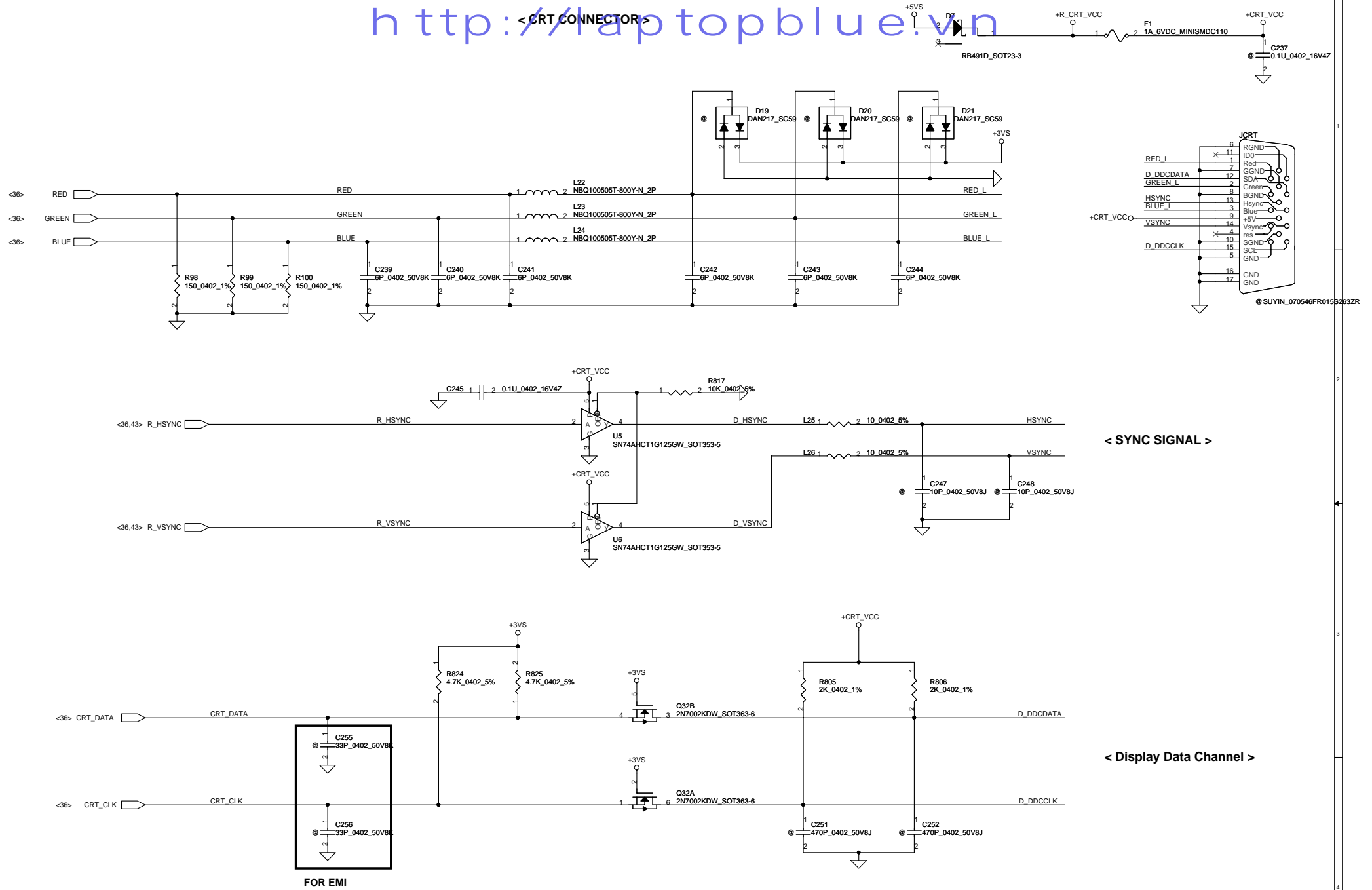
Use voltage divider resistor R243 & R244 to pull low

NB_OSC_14.318M	1	configure as single-ended 66MHz output
	0 *	configure as differential 100MHz output * default

	OSC_14M_NB
RS880M	1.1V 158R/90.9R

NB CLOCK INPUT TABLE

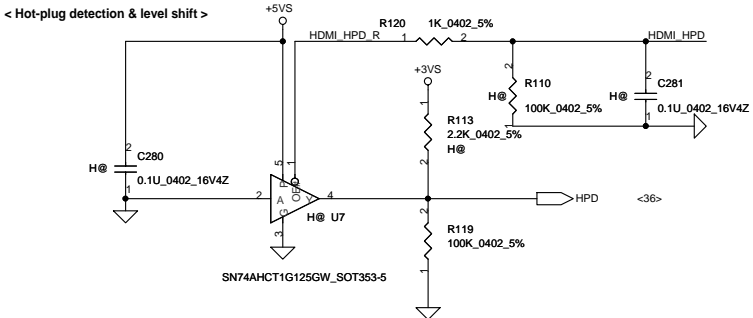
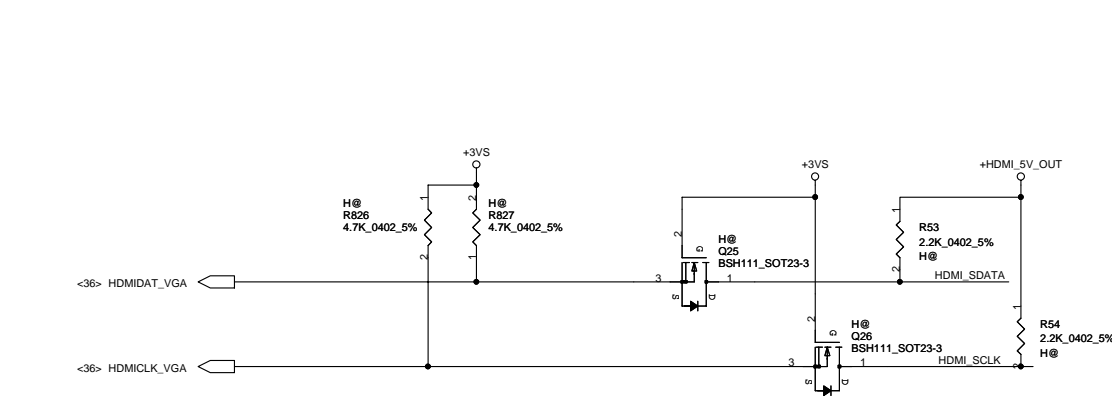
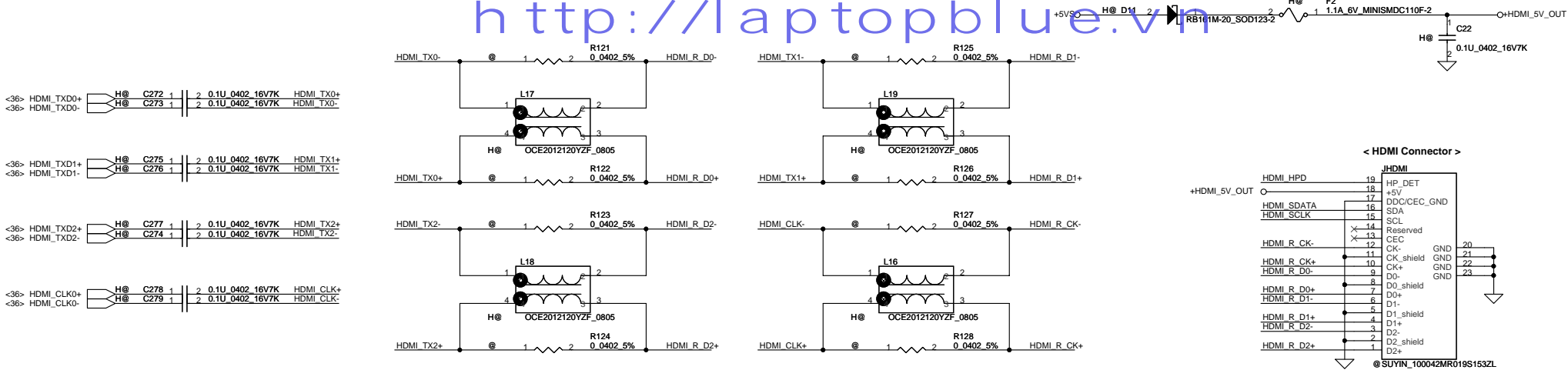
NB CLOCKS	RX881	RX881
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF



< SYNC SIGNAL >

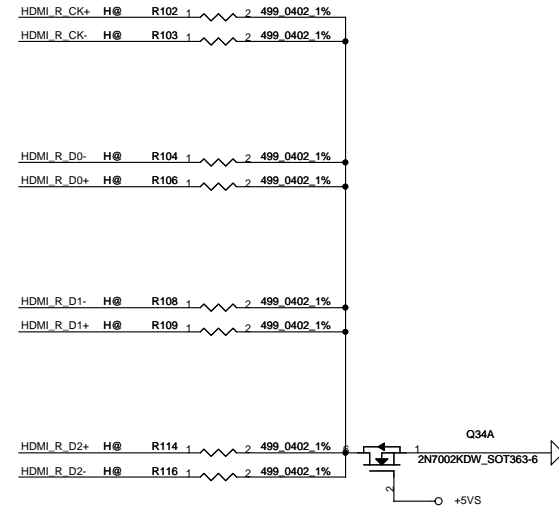
< Display Data Channel >

Security Classification		Compal Secret Data				Compal Electronics, Inc.							
Issued Date		2008-09-25		Deciphered Date		2009-09-25		Title					
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.								SCHEMATIC, MB A6052					
								Doc Number		401851		Rev A	
								Date:		Wednesday, January 20, 2010		Sheet 17 of 53	

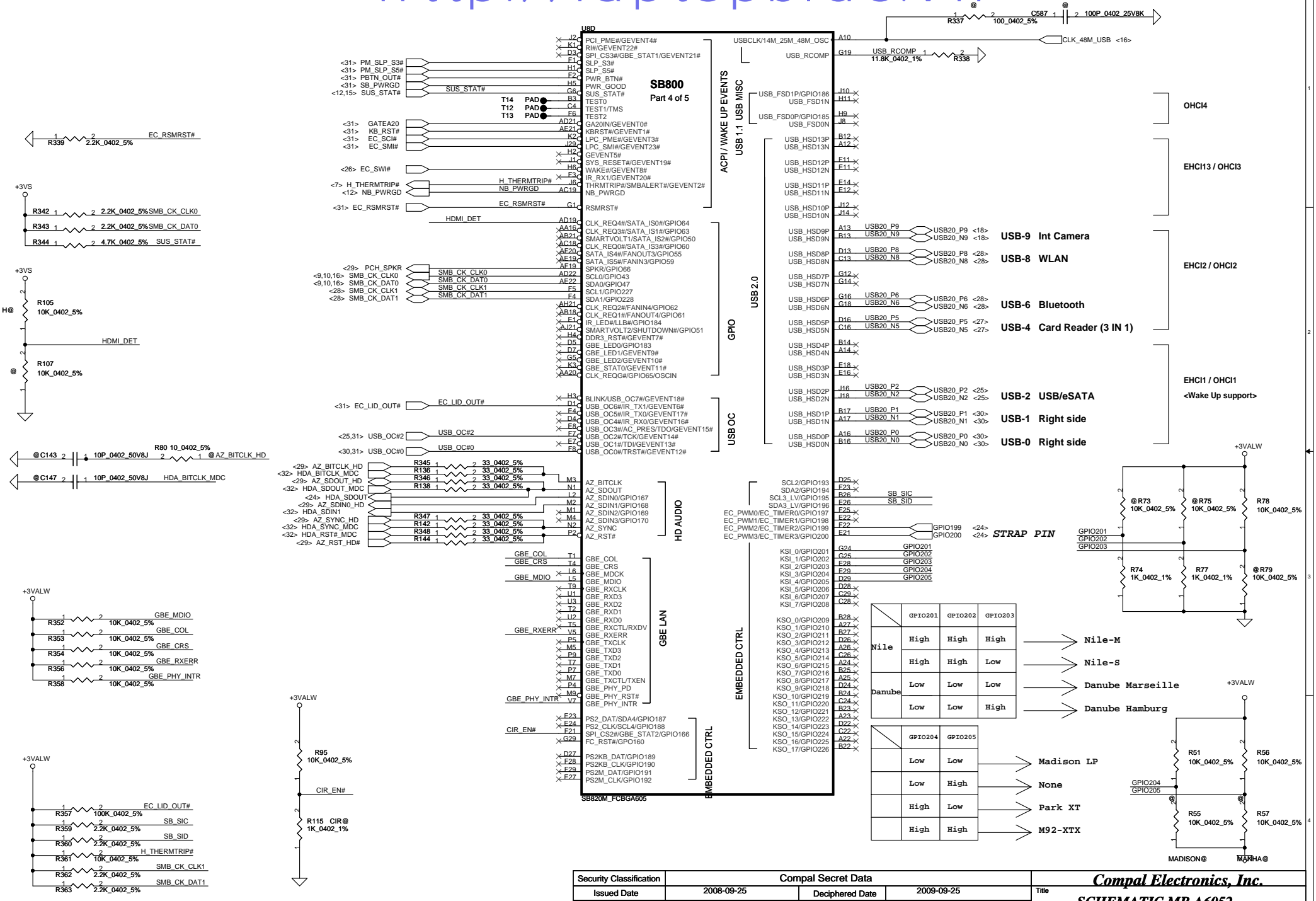


< Termination resistor >

< Close to Connector >



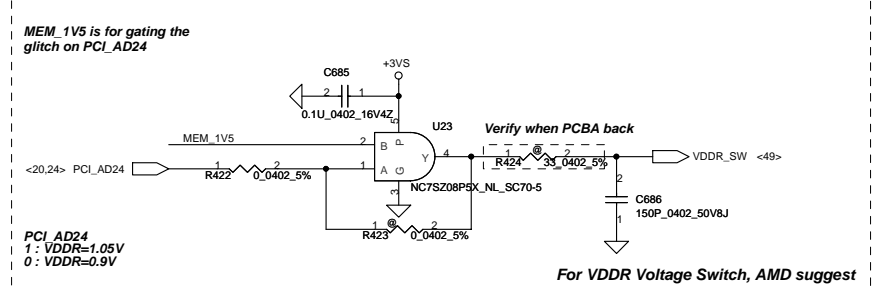
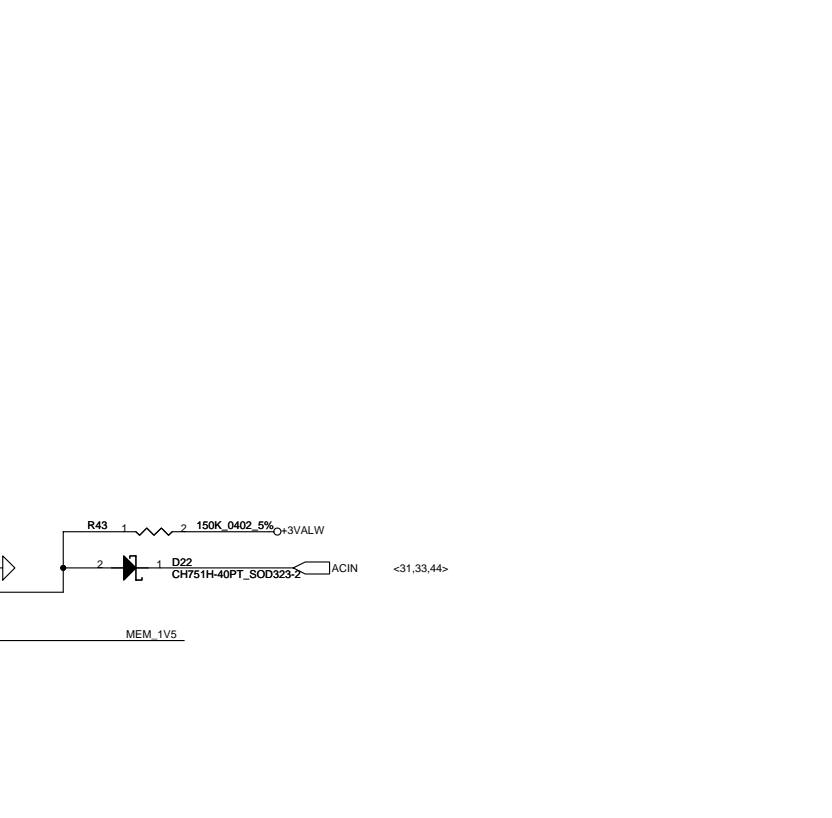
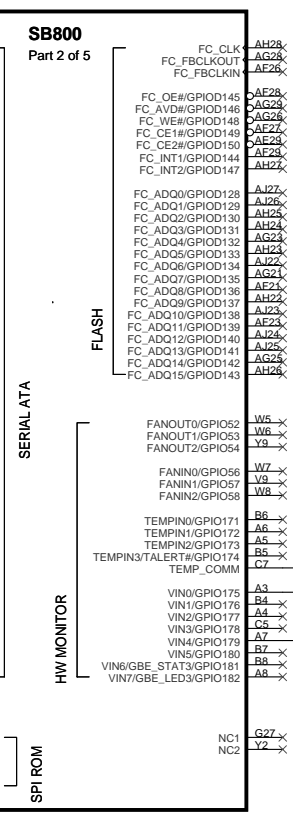
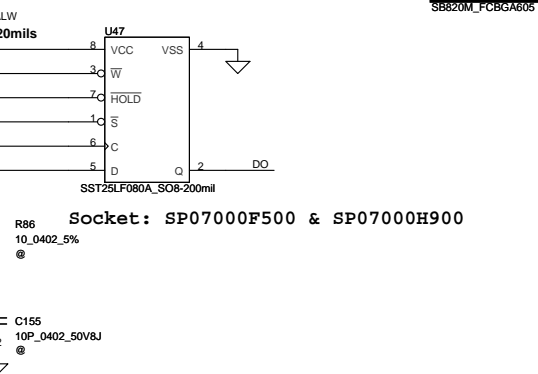
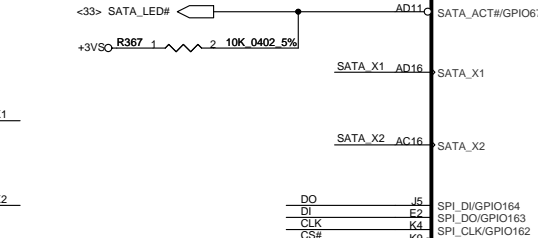
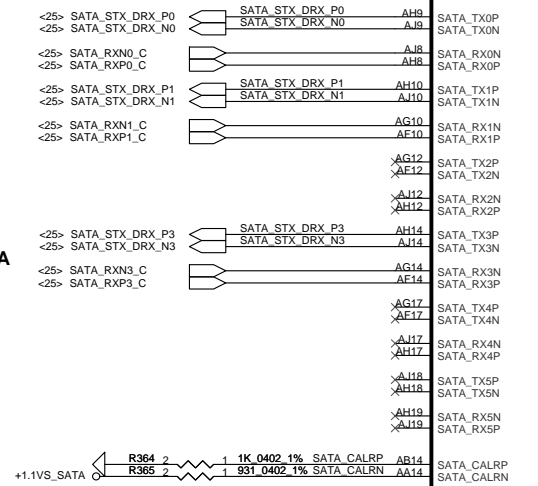
Security Classification	Compal Secret Data			Title	
Issued Date	2008-09-25	Deciphered Date	2009-09-25	SCHEMATIC,MB A6052	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	401851
				Date:	Wednesday, January 20, 2010
				Sheet	19 of 53



HDD

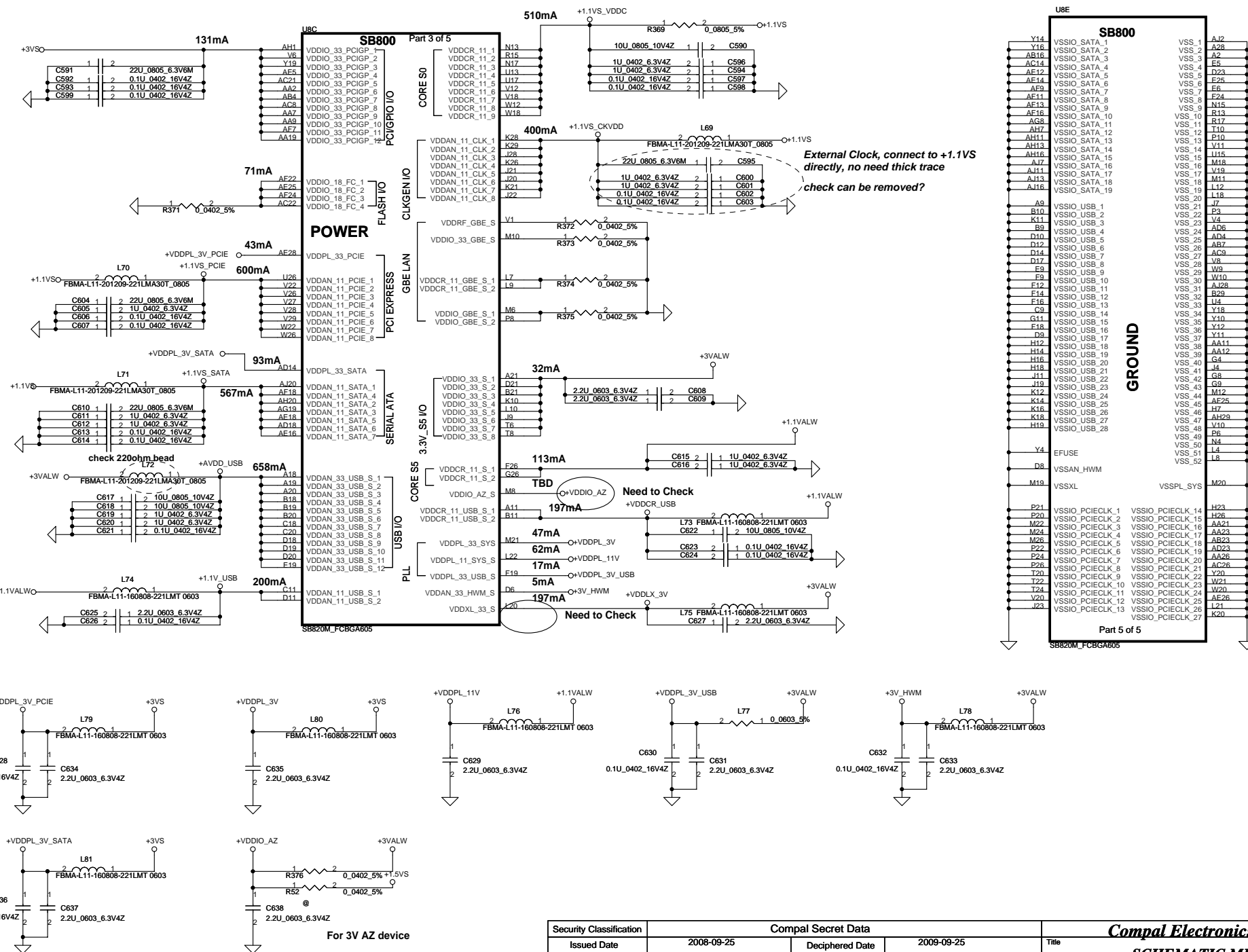
ODD

eSATA



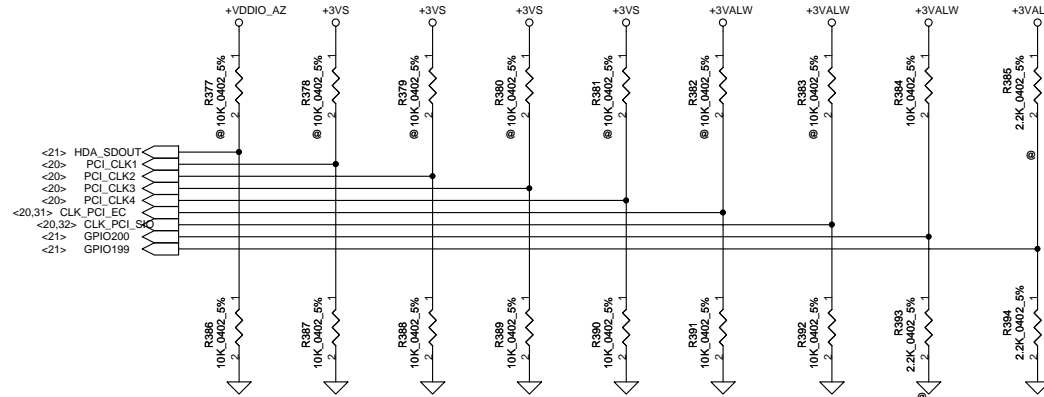
Security Classification		Compal Secret Data		Title	
Issued Date	2008-09-25	Deciphered Date	2009-09-25	Rev	401851
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	401851
				Date	Wednesday, January 20, 2010
				Sheet	22 of 53

Compal Electronics, Inc.
SCHEMATIC_MB A6052



Security Classification		Compal Secret Data		Compal Electronics, Inc. SCHEMATIC, MB A6052	
Issued Date	2008-09-25	Deciphered Date	2009-09-25	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Doc No	
				Customer	401851
				Date:	Wednesday, January 20, 2010
				Sheet	23 of 53

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LCP_CLK1		GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE GEN2	WATCHDOG TIMER ENABLE	USE DEBUG STRAP	Inter CLK Gen Mode Enable	EC ENABLE	CLOCKGEN ENABLE		H,H = Reserved	
PULL LOW	Performance MODE	FORCE PCIE GEN1	WATCHDOG TIMER DISABLE	IGNORE DEBUG STRAP	Inter CLK Gen Mode Disable	EC DISABLE	CLOCKGEN DISABLE		H,L = SPI ROM (Default)	
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT		L,H = LPC ROM	L,L = FWH ROM



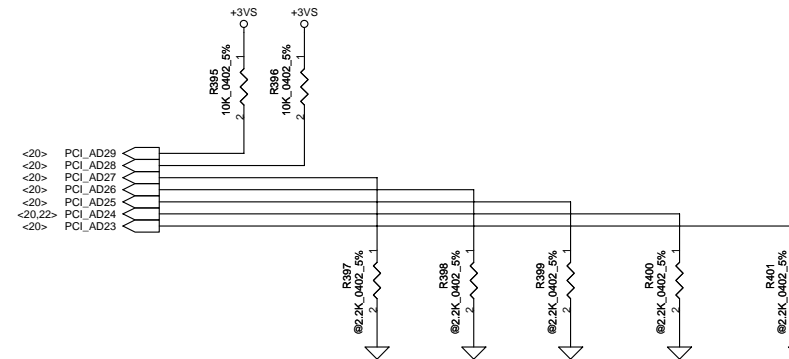
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

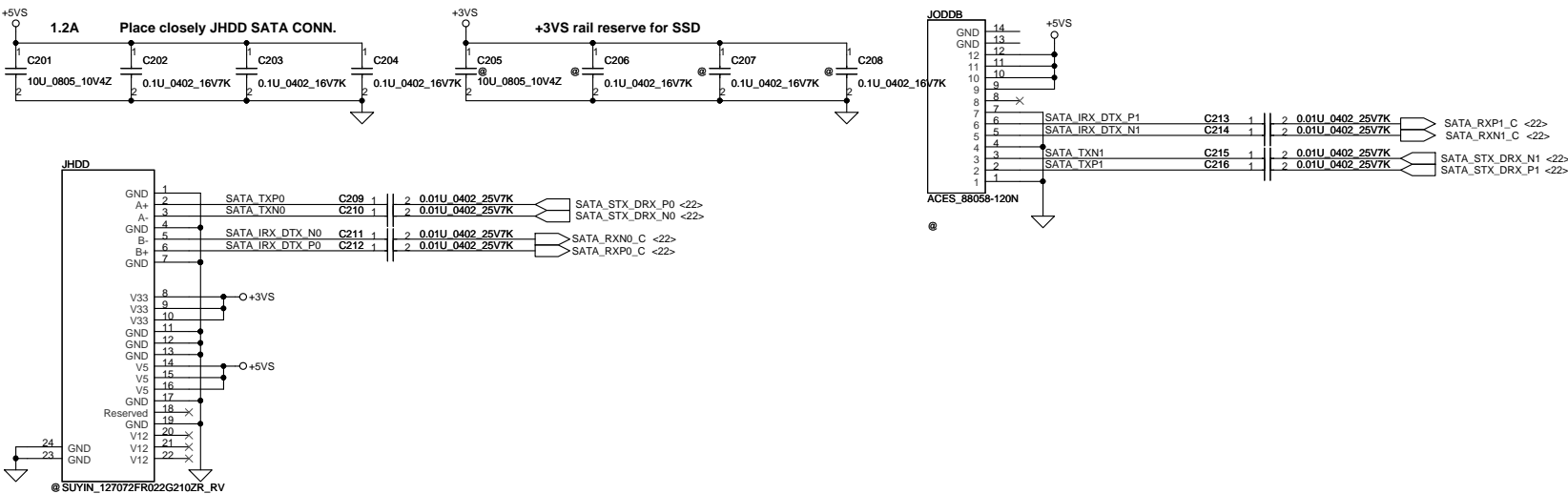
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL	DISABLE ILA AUTORUN	USE FC PLL	USE DEFAULT PCIE STRAPS	DISABLE PCI MEM BOOT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT

Check AD29,AD28 strap function

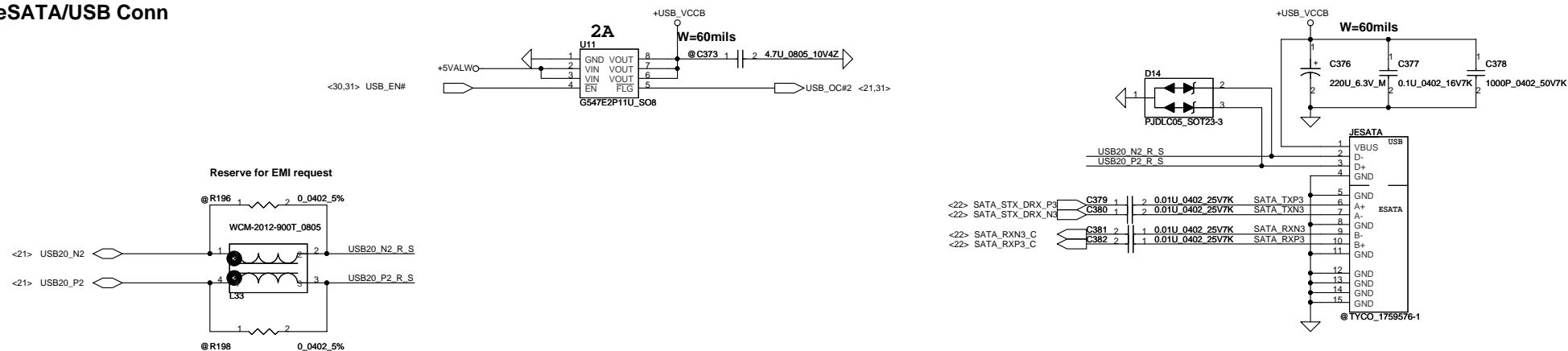
check default



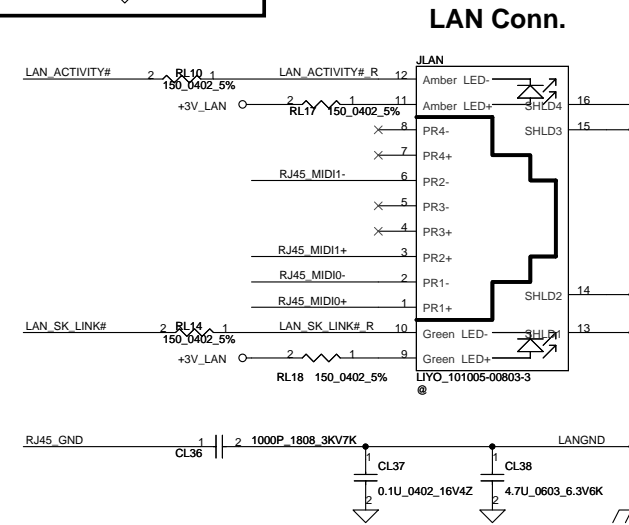
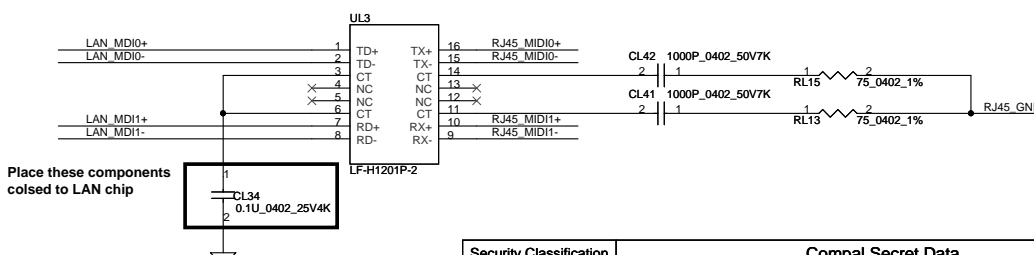
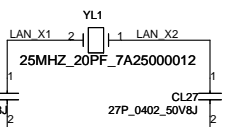
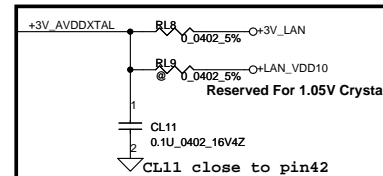
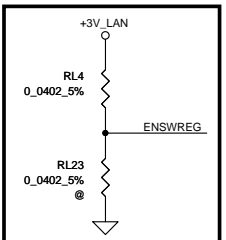
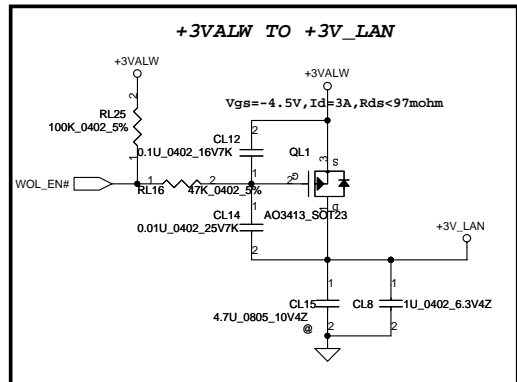
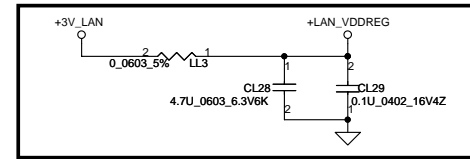
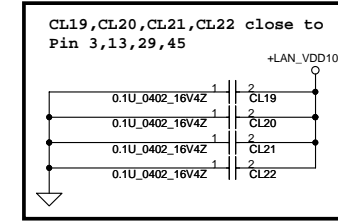
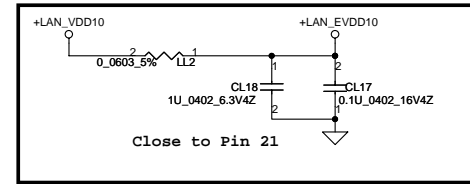
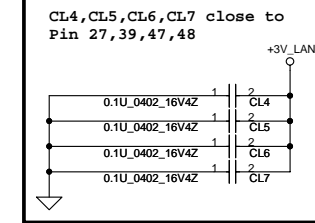
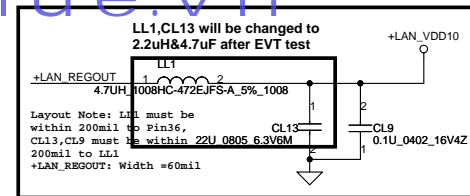
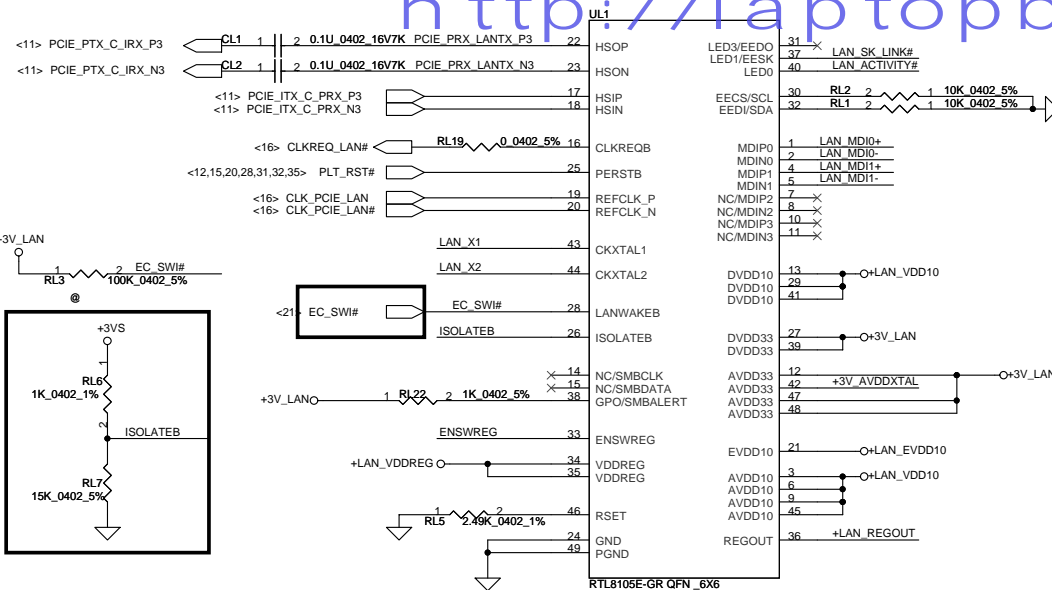
< SATA ODD Conn >



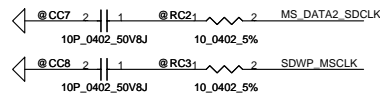
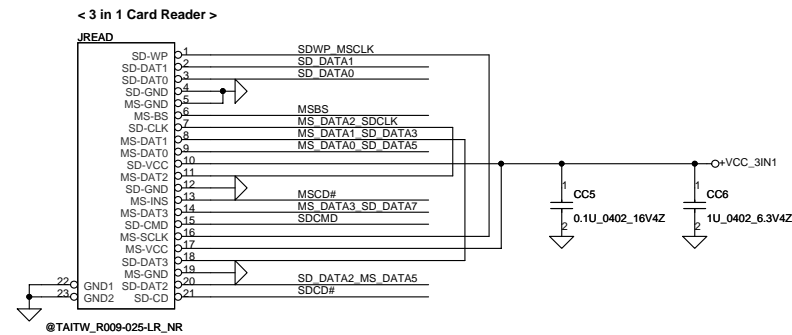
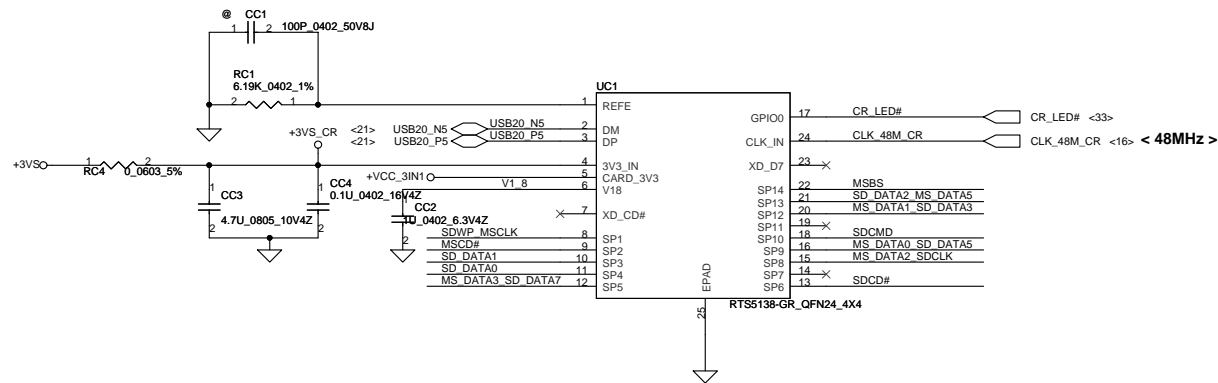
eSATA/USB Conn

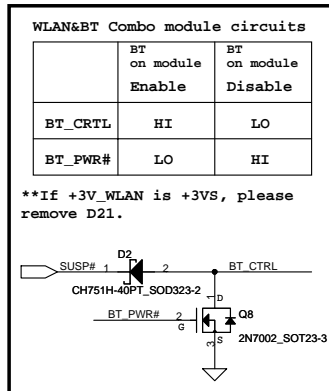
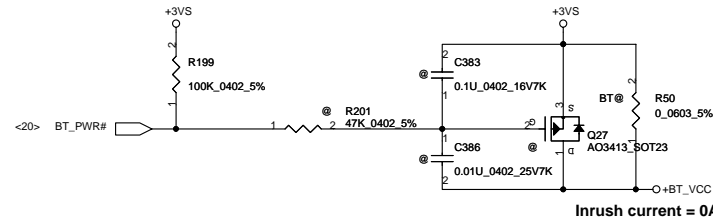


Security Classification	Compal Secret Data			<i>Compal Electronics, Inc.</i> SCHEMATIC, MB A6052		
Issued Date	2008-09-25	Deciphered Date	2009-09-25	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
				Custom	401851	A
				Date:	Wednesday, January 20, 2010	Sheet 25 of 53

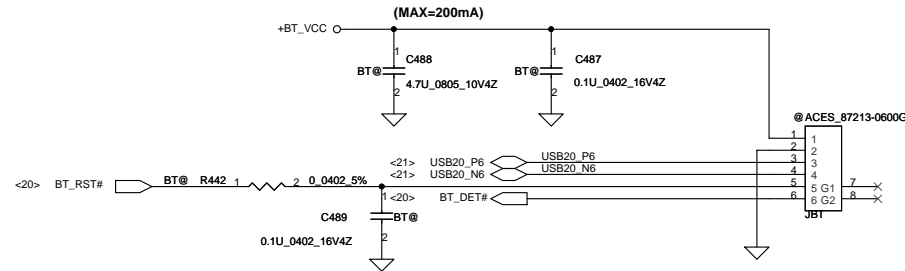


Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2009-02-12		Deciphered Date		2009-02-12		Title		SCHEMATIC, MB A6052	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.						Size	Document Number	401851	Rev	A	
						Date:	Wednesday, January 20, 2010	Sheet	26	of	53

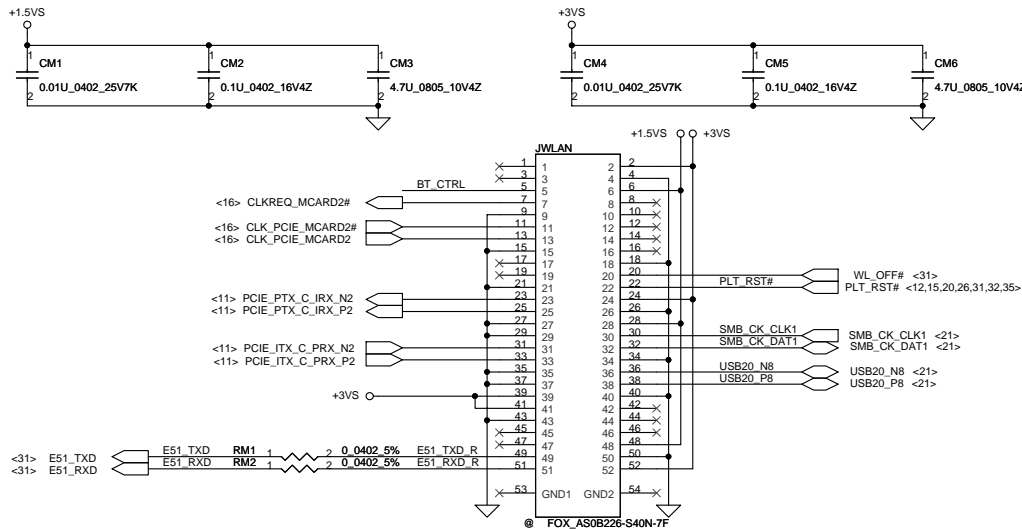




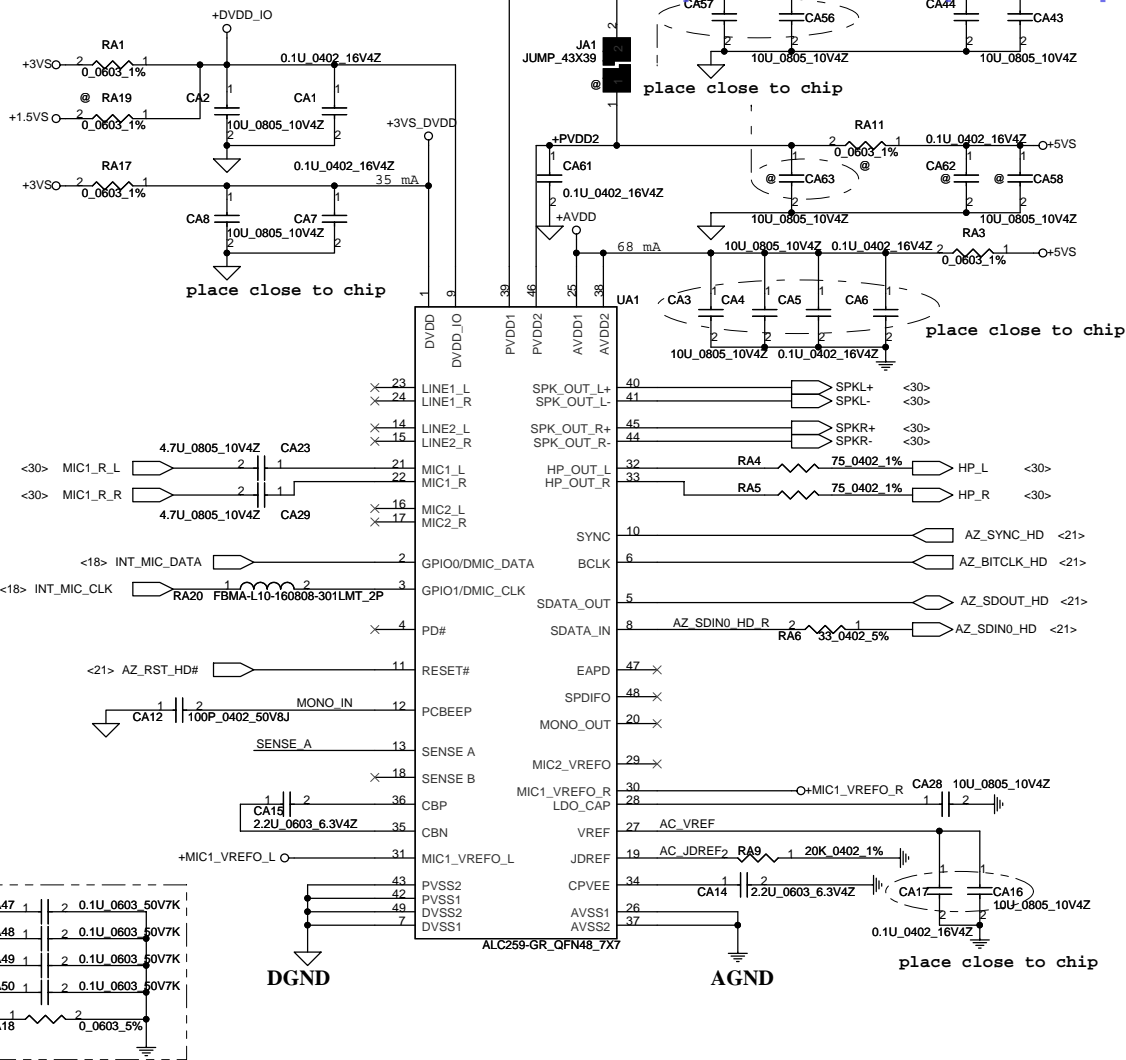
< Bluetooth Connector >



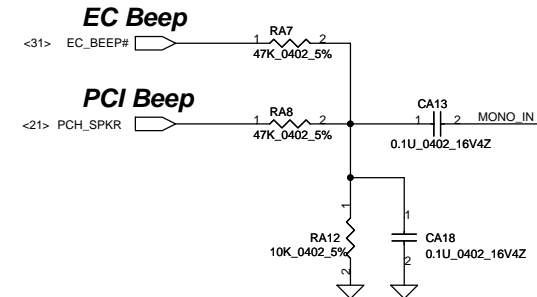
< PCIe Mini Card for WLAN >



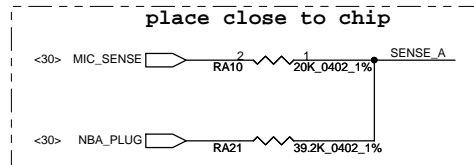
Codec



Beep sound



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

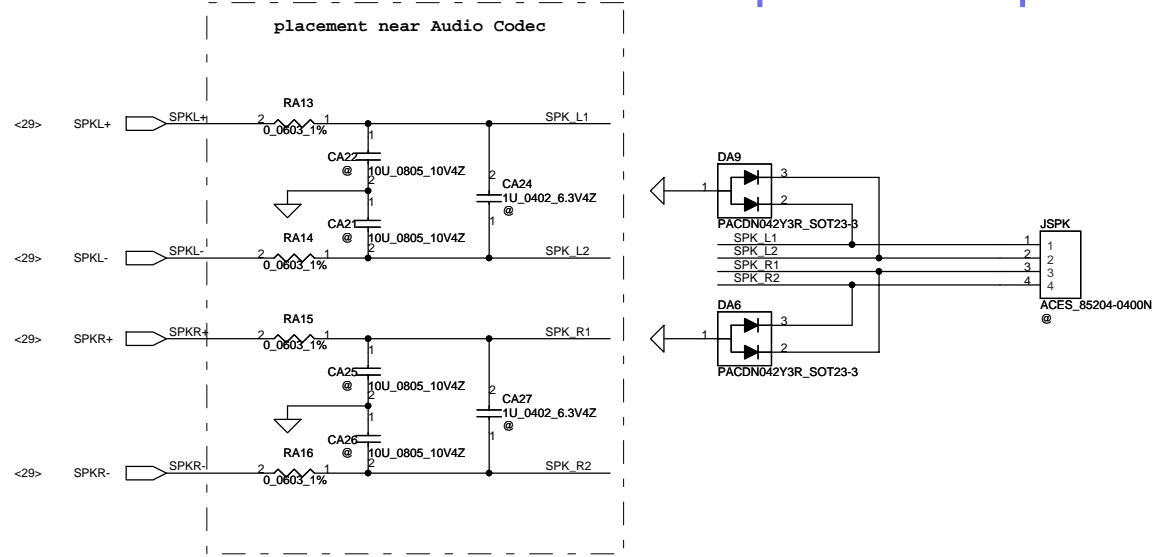


Security Classification				Compal Secret Data				Compal Electronics, Inc.	
Issued Date		2009-02-12		Deciphered Date		2009-02-12		Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Size		Document Number		Rev		A	
Date:		Wednesday, January 20, 2010		Sheet		29		of 53	

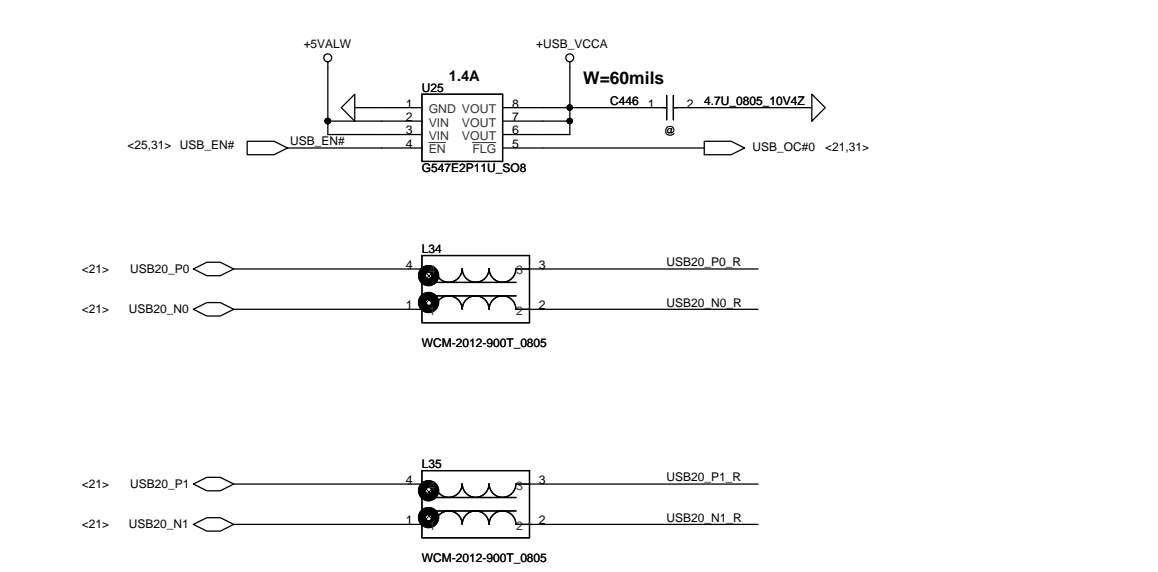
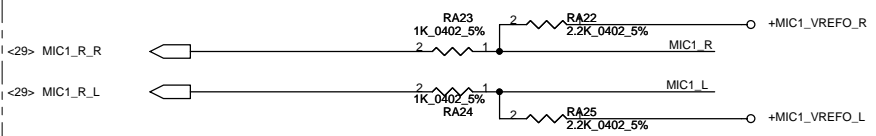
Speaker Connector

http://laptopblue.vn

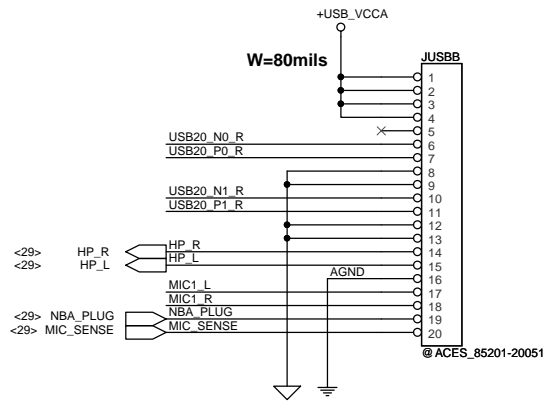
HeadPhone/LINE Out JACK



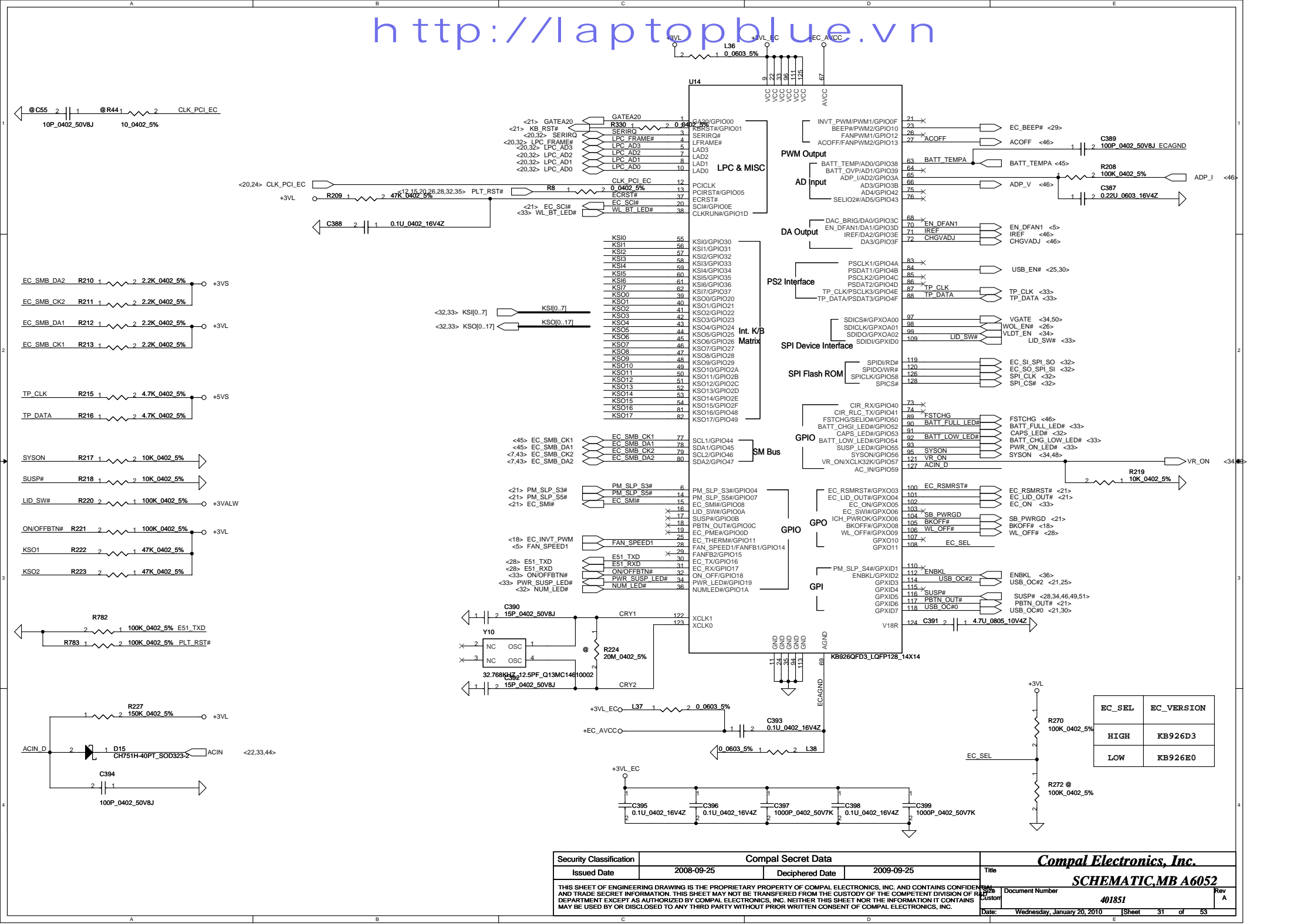
Ext.MIC/LINE IN JACK



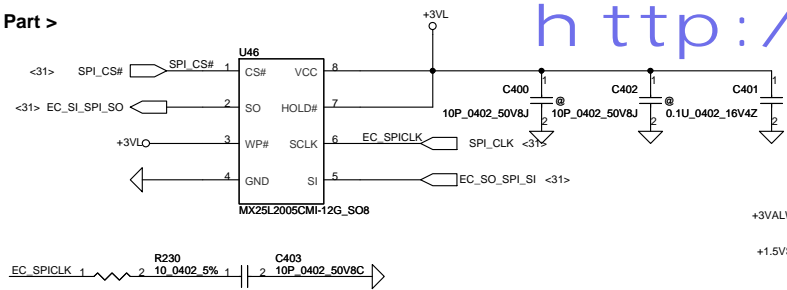
Audio & USB Sub-Board Conn.



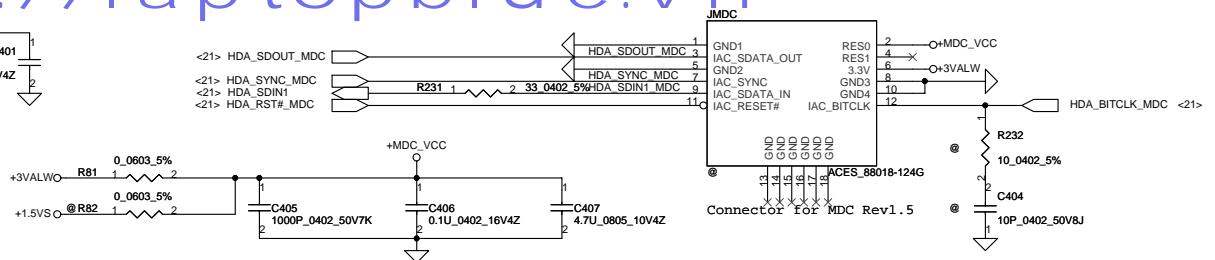
Security Classification	Compal Secret Data		Title	
Issued Date	2009-02-12	Deciphered Date	2009-02-12	Rev A
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number
				401851
Date: Wednesday, January 20, 2010				Sheet 30 of 53



< ROM Part >

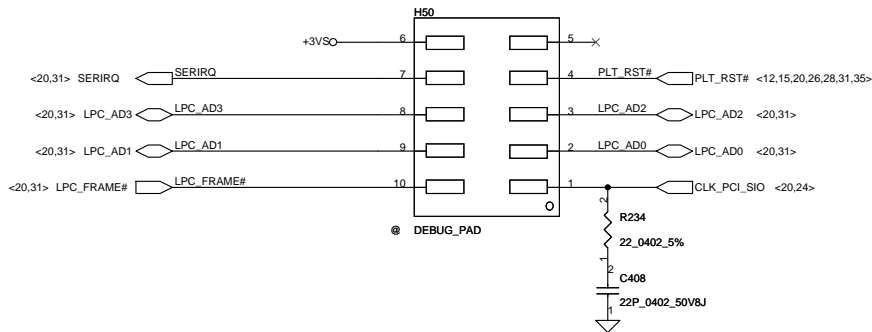


< MDC 1.5 Conn >



< LPC Debug Port >

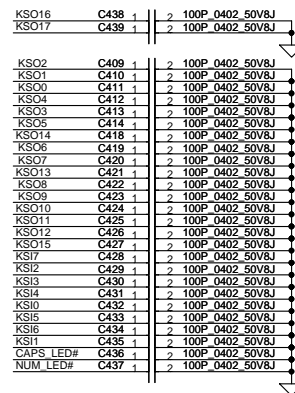
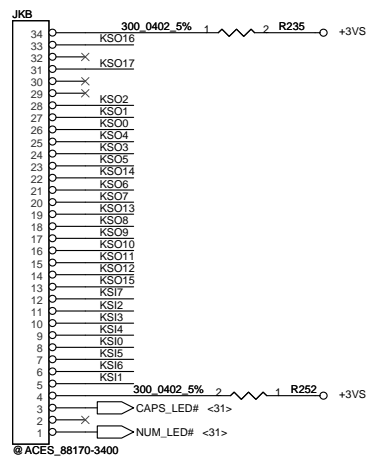
Please place the PAD under DDR DIMM.



< KEYBOARD Conn >

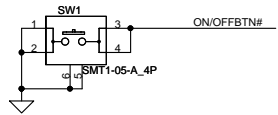


< For EMI >

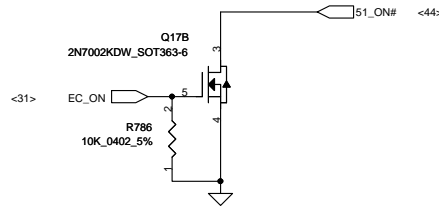


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008-09-25	Deciphered Date	2009-09-25	Title	SCHEMATIC, MB A6052
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Date	
				Customer	401851
				Date	Wednesday, January 20, 2010
				Sheet	32 of 53
				Rev	A

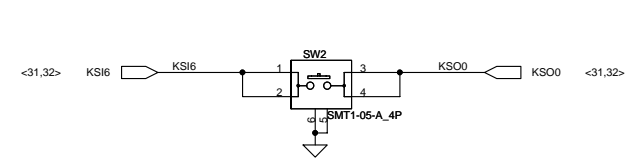
< Power Button for Debug >



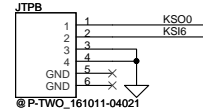
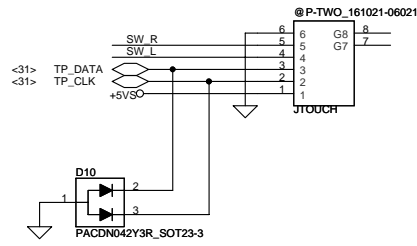
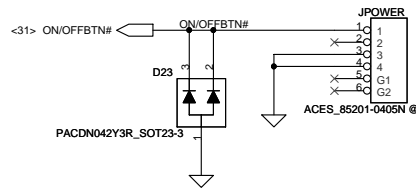
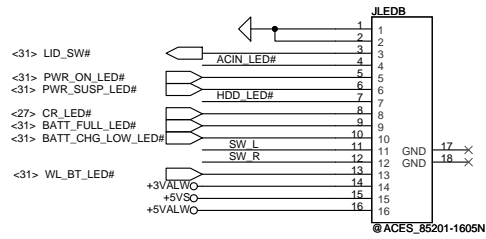
< Power Button Circuit >



< TP on & off BTN on M/B>

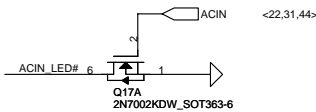


Sub-B Connector

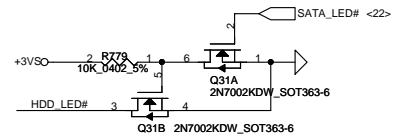


LED Circuit

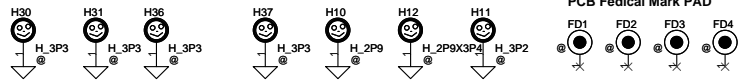
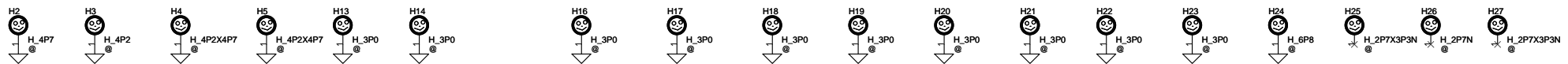
DC-IN LED



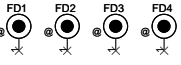
HDD LED



SCREW

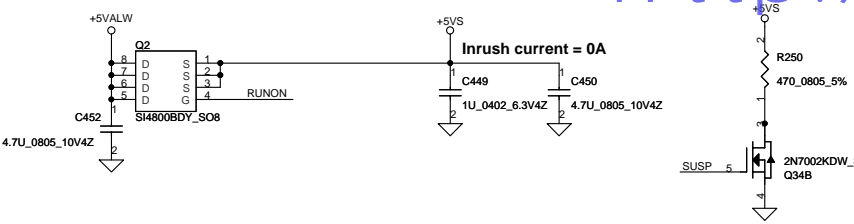


PCB Federal Mark PAD

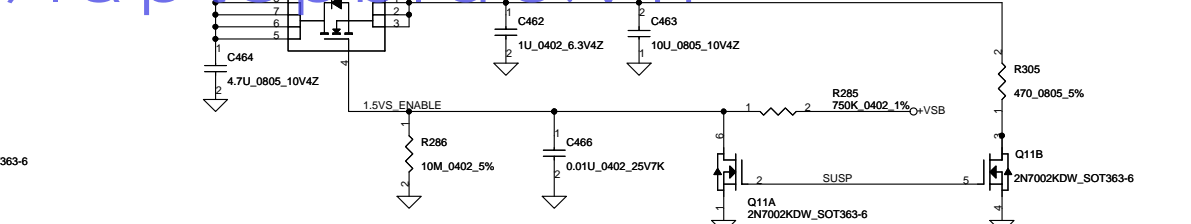


Security Classification	Compal Secret Data			Title	
Issued Date	2008-09-25	Deciphered Date	2009-09-25	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				401851	A
				Date: Wednesday, January 20, 2010	Sheet 33 of 53

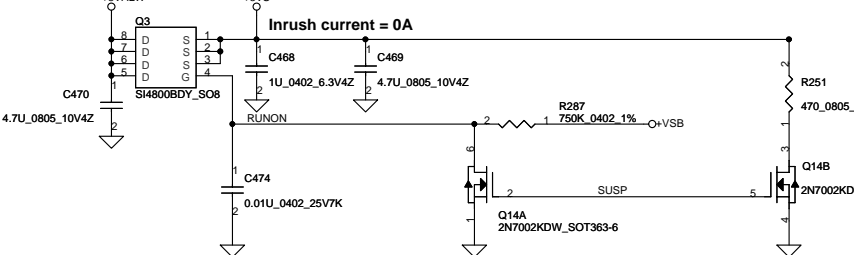
< +5VALW TO +5VS >



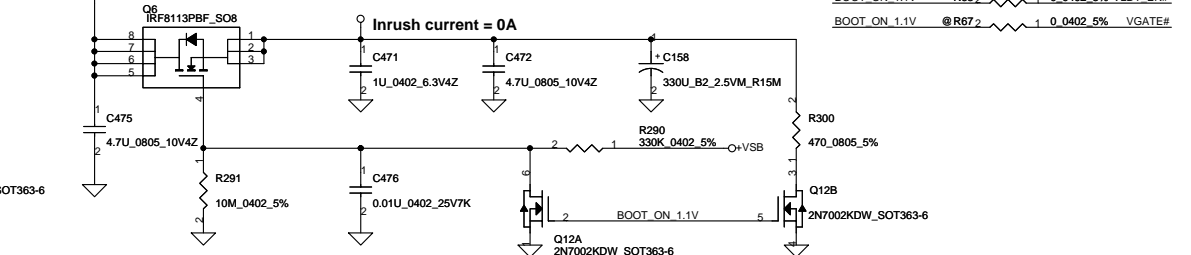
< +1.5V TO +1.5VS >



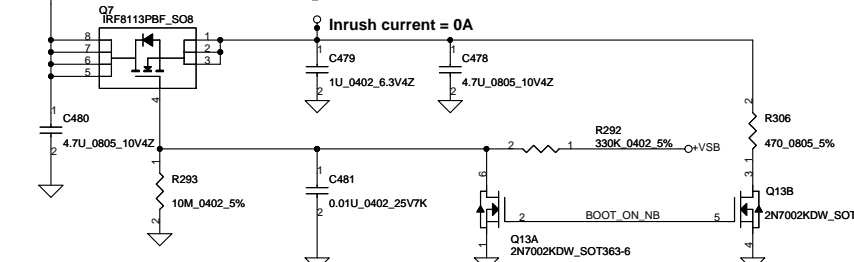
< +3VALW TO +3VS >



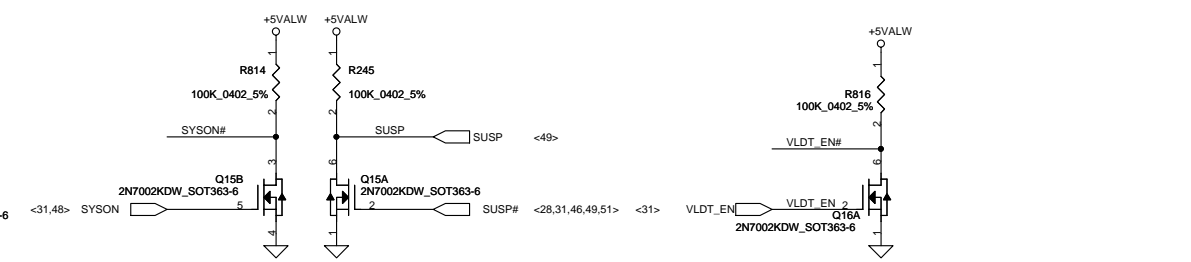
< +1.1VALW TO +1.1VS >



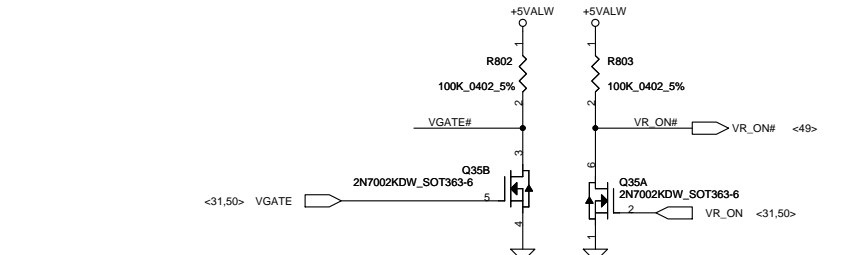
< +1.1VALW TO +NB_CORE >



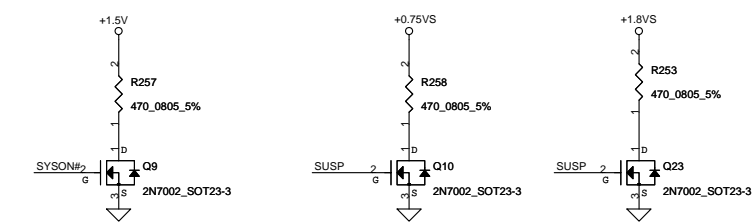
< Inversion of SYSON, SUSP#, VLDT_EN, EC_ON >





BOOT_ON_NB @R45 1 0.0402 5% SUSP
BOOT_ON_NB R46 1 0.0402 5% VLDT_EN#
BOOT_ON_NB @R47 1 0.0402 5% VGATE#





< Discharge circuit >

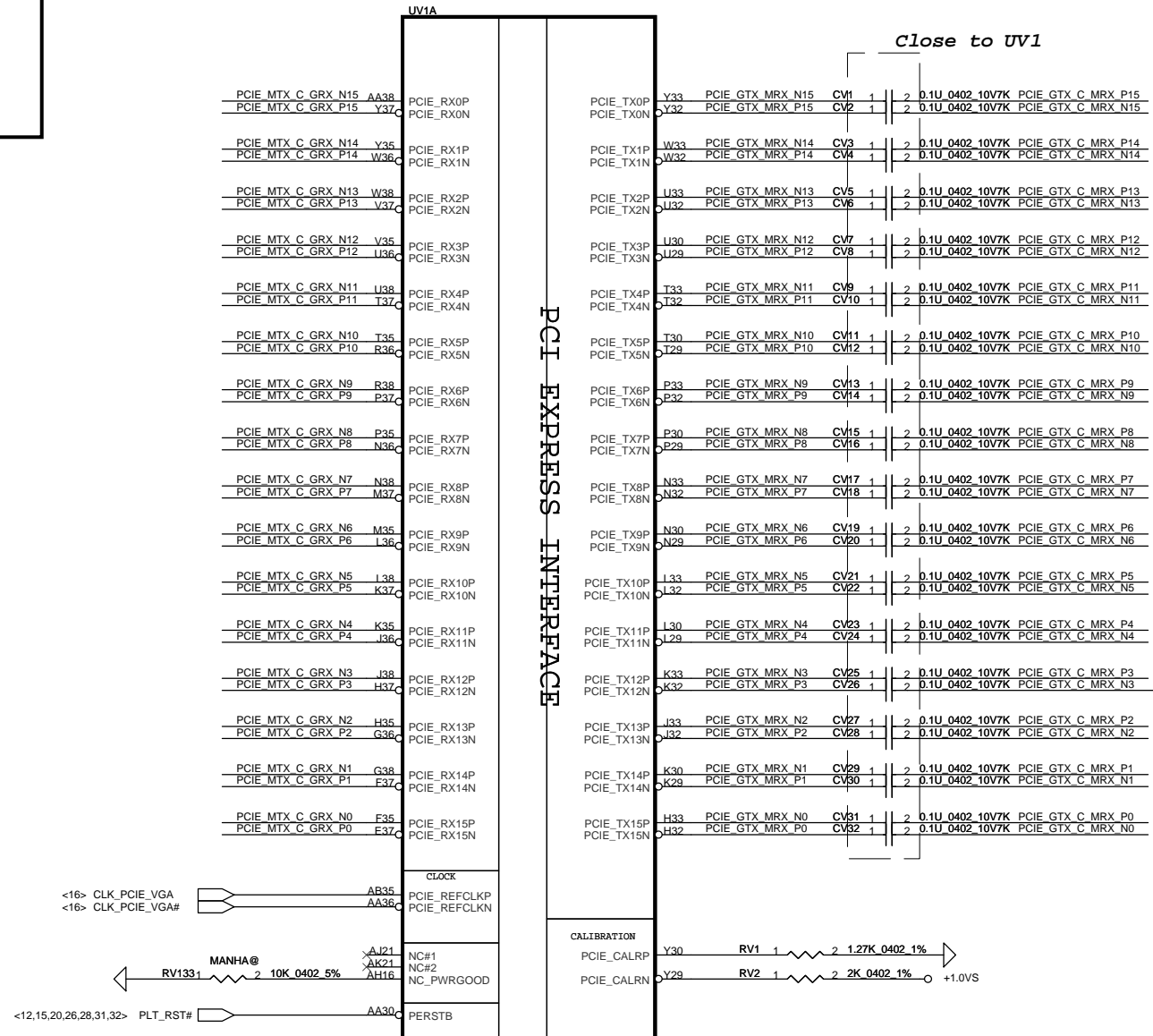


<11> PCIE_GTX_C_MRX_P[0..15]  PCIE GTX C_MRX_P[0..15]

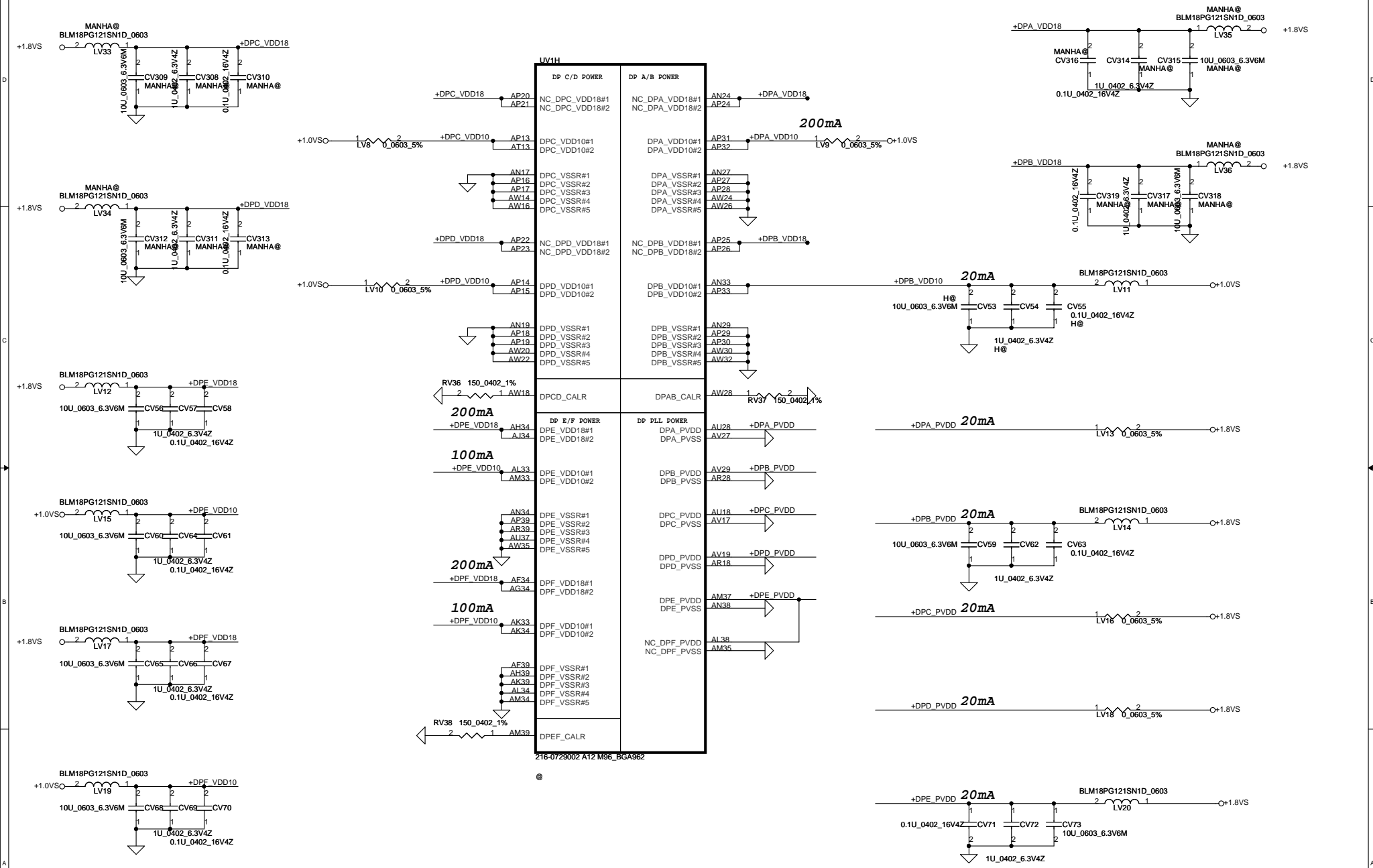
<11> PCIE_GTX_C_MRX_N[0..15]  PCIE GTX C_MRX_N[0..15]

<11> PCIE_MTX_C_GRX_P[0..15]  PCIE MTX C_GRX_P[0..15]

<11> PCIE_MTX_C_GRX_N[0..15]  PCIE MTX C_GRX_N[0..15]



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008-09-25	Deciphered Date	2009-09-25	Title	SCHEMATIC, MB A6052
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	401851
				Date	Wednesday, January 20, 2010
				Sheet	35 of 53



Security Classification			Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008-09-25	Deciphered Date	2009-09-25	Title	SCHEMATIC, MB A6052	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
				Custom	401851	A
				Date:	Wednesday, January 20, 2010	Sheet 37 of 53



Date: Wednesday, January 20, 2010 Sheet 38 of 53

UV4F

AB39 PCIE_VSS#1
F39 PCIE_VSS#2
F34 PCIE_VSS#3
F39 PCIE_VSS#4
G33 PCIE_VSS#5
G34 PCIE_VSS#6
H31 PCIE_VSS#7
H34 PCIE_VSS#8
H39 PCIE_VSS#9
J31 PCIE_VSS#10
J34 PCIE_VSS#11
K31 PCIE_VSS#12
K34 PCIE_VSS#13
K39 PCIE_VSS#14
L31 PCIE_VSS#15
L34 PCIE_VSS#16
M34 PCIE_VSS#17
M39 PCIE_VSS#18
N31 PCIE_VSS#19
N34 PCIE_VSS#20
P31 PCIE_VSS#21
P34 PCIE_VSS#22
P39 PCIE_VSS#23
R34 PCIE_VSS#24
T31 PCIE_VSS#25
T34 PCIE_VSS#26
T39 PCIE_VSS#27
U31 PCIE_VSS#28
U34 PCIE_VSS#29
V34 PCIE_VSS#30
V39 PCIE_VSS#31
W31 PCIE_VSS#32
W34 PCIE_VSS#33
Y34 PCIE_VSS#34
Y39 PCIE_VSS#35

GND

F15 GND#101
F17 GND#102
F19 GND#103
F21 GND#104
F23 GND#105
F25 GND#106
F27 GND#107
F29 GND#108
F31 GND#109
F33 GND#110
F7 GND#111
F9 GND#112
G2 GND#113
G6 GND#114
H6 GND#115
J2 GND#116
J27 GND#117
J6 GND#118
J8 GND#119
K14 GND#120
K7 GND#121
L11 GND#122
L17 GND#123
L2 GND#124
L22 GND#125
L24 GND#126
L6 GND#127
M17 GND#128
M22 GND#129
M24 GND#130
N16 GND#131
N18 GND#132
N2 GND#133
N21 GND#134
N23 GND#135
N26 GND#136
N6 GND#137
R15 GND#138
R17 GND#139
R2 GND#140
R20 GND#141
R22 GND#142
R24 GND#143
R27 GND#144
R6 GND#145
T11 GND#146
T13 GND#147
T16 GND#148
T18 GND#149
T21 GND#150
T23 GND#151
T26 GND#152
U15 GND#153
U17 GND#154
U2 GND#155
U20 GND#156
U22 GND#157
U24 GND#158
U27 GND#159
U6 GND#160
V11 GND#161
V16 GND#162
V18 GND#163
V21 GND#164
V23 GND#165
V26 GND#166
W2 GND#167
W6 GND#168
Y15 GND#169
Y17 GND#170
Y20 GND#171
Y22 GND#172
Y24 GND#173
Y27 GND#174
U13 GND#175
V13 GND#176

VSS_MECH#1
VSS_MECH#2
VSS_MECH#3

A39-X
A31-X
A33-X

A3 GND#1
A37 GND#2
AA16 GND#3
AA18 GND#4
AA2 GND#5
AA21 GND#6
AA23 GND#7
AA26 GND#8
AA28 GND#9
AA6 GND#10
AB12 GND#11
AB15 GND#12
AB17 GND#13
AB20 GND#14
AB22 GND#15
AB24 GND#16
AB27 GND#17
AC11 GND#18
AC13 GND#19
AC16 GND#20
AC18 GND#21
AC2 GND#22
AC21 GND#23
AC23 GND#24
AC26 GND#25
AC28 GND#26
AC6 GND#27
AD15 GND#28
AD17 GND#29
AD20 GND#30
AD22 GND#31
AD24 GND#32
AD27 GND#33
AD9 GND#34
AE2 GND#35
AE6 GND#36
AF10 GND#37
AF16 GND#38
AF18 GND#39
AF21 GND#40
AG17 GND#41
AG2 GND#42
AG20 GND#43
AG22 GND#44
AG6 GND#45
AG9 GND#46
AH21 GND#47
AH29 GND#48
AI10 GND#49
AI11 GND#50
AI2 GND#51
AJ28 GND#52
AJ6 GND#53
AK11 GND#54
AK31 GND#55
AK7 GND#56
AL11 GND#57
AL14 GND#58
AL17 GND#59
AL2 GND#60
AL20 GND#61
AL21 GND#62
AL23 GND#63
AL26 GND#64
AL32 GND#65
AL6 GND#66
AL8 GND#67
AM11 GND#68
AM31 GND#69
AM9 GND#70
AN11 GND#71
AN2 GND#72
AN30 GND#73
AN6 GND#74
AN8 GND#75
AP11 GND#76
AP7 GND#77
AP9 GND#78
AR5 GND#79
AW34 GND#80
B11 GND#81
B13 GND#82
B15 GND#83
B17 GND#84
B19 GND#85
B21 GND#86
B23 GND#87
B25 GND#88
B27 GND#89
B29 GND#90
B31 GND#91
B33 GND#92
B7 GND#93
B9 GND#94
C1 GND#95
C39 GND#96
E35 GND#97
E5 GND#98
F11 GND#99
F13 GND#100

216-0729002 A12 M86_BGA862

Security Classification		Compal Secret Data		Title	
Issued Date	2008-09-25	Deciphered Date	2009-09-25	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				401851	A
Date: Wednesday, January 20, 2010				Sheet	39 of 53

MDA[0..63] → MDA[0..63] <41>

MDB[0..63] → MDB[0..63] <42>

Park uses memory group B only

UV1C

MEMORY INTERFACE A

MDA0	C37	DQA_0	MAA_0	G24	MAA0
MDA1	C35	DQA_1	MAA_1	J23	MAA1
MDA2	A35	DQA_2	MAA_2	H24	MAA2
MDA3	E34	DQA_3	MAA_3	J24	MAA3
MDA4	C32	DQA_4	MAA_4	H26	MAA4
MDA5	D33	DQA_5	MAA_5	J26	MAA5
MDA6	F32	DQA_6	MAA_6	H21	MAA6
MDA7	E32	DQA_7	MAA_7	G21	MAA7
MDA8	D31	DQA_8	MAA_8	H19	MAA8
MDA9	F30	DQA_9	MAA_9	H20	MAA9
MDA10	C30	DQA_10	MAA_10	L13	MAA10
MDA11	A30	DQA_11	MAA_11	G16	MAA11
MDA12	F28	DQA_12	MAA_12	H16	MAA12
MDA13	C28	DQA_13	MAA_13/BA2	H17	A_BA2
MDA14	A28	DQA_14	MAA_14/BA0	H17	A_BA0
MDA15	E28	DQA_15	MAA_15/BA1	H17	A_BA1
MDA16	D27	DQA_16			
MDA17	F26	DQA_17			
MDA18	C26	DQA_18			
MDA19	A26	DQA_19			
MDA20	F24	DQA_20			
MDA21	C24	DQA_21			
MDA22	A24	DQA_22			
MDA23	F24	DQA_23			
MDA24	C22	DQA_24			
MDA25	F22	DQA_25			
MDA26	D22	DQA_26			
MDA27	F20	DQA_27			
MDA28	A20	DQA_28			
MDA29	F19	DQA_29			
MDA30	D19	DQA_30			
MDA31	E18	DQA_31			
MDA32	C18	DQA_32			
MDA33	A18	DQA_33			
MDA34	F18	DQA_34			
MDA35	D17	DQA_35			
MDA36	A16	DQA_36			
MDA37	F16	DQA_37			
MDA38	D15	DQA_38			
MDA39	E14	DQA_39			
MDA40	C14	DQA_40			
MDA41	A14	DQA_41			
MDA42	F12	DQA_42			
MDA43	A12	DQA_43			
MDA44	D11	DQA_44			
MDA45	F10	DQA_45			
MDA46	A10	DQA_46			
MDA47	C10	DQA_47			
MDA48	G13	DQA_48			
MDA49	H13	DQA_49			
MDA50	H13	DQA_50			
MDA51	H11	DQA_51			
MDA52	G10	DQA_52			
MDA53	G8	DQA_53			
MDA54	K9	DQA_54			
MDA55	K10	DQA_55			
MDA56	G9	DQA_56			
MDA57	C8	DQA_57			
MDA58	A8	DQA_58			
MDA59	E8	DQA_59			
MDA60	A6	DQA_60			
MDA61	C6	DQA_61			
MDA62	E6	DQA_62			
MDA63	A5	DQA_63			

216-0729002 A12 M96_BGA962

MAA[13..0] → MAA[13..0] <41>

A_BA[2..0] → A_BA[2..0] <41>

DQMA#[7..0] <41>

QSA[7..0] <41>

QSA#[7..0] <41>

ODTA0 ODTA1 <41>

ODTA0 ODTA1 <41>

CLKA0 CLKA0# <41>

CLKA0# CLKA0# <41>

CLKA1 CLKA1# <41>

CLKA1# CLKA1# <41>

RASA0# RASA1# <41>

RASA1# RASA1# <41>

CASA0# CASA1# <41>

CASA1# CASA1# <41>

CSA0#_0 CSA0#_0 <41>

CSA0#_0 CSA0#_0 <41>

CSA1#_0 CSA1#_0 <41>

CSA1#_0 CSA1#_0 <41>

CKEA0 CKEA1 <41>

CKEA1 CKEA1 <41>

WEA0# WEA1# <41>

WEA1# WEA1# <41>

RSVD#1 RSVD#6 <41>

RSVD#6 RSVD#6 <41>

RSVD#9 RSVD#11 <41>

RSVD#11 RSVD#11 <41>

MAA13 MAB13 <41>

MAA13 MAB13 <41>

MAA13 MAB13 <41>

MAA13 MAB13 <41>

MAA13 MAB13 <41>

MAA13 MAB13 <41>

MAA13 MAB13 <41>

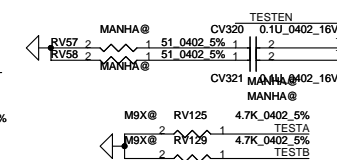
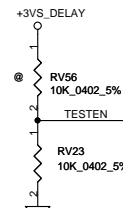
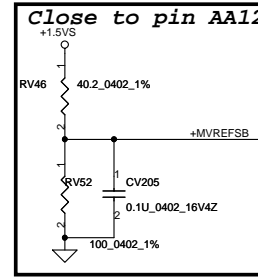
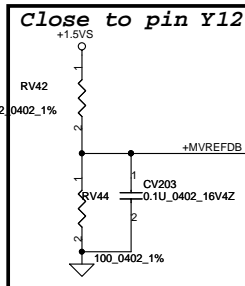
MAA13 MAB13 <41>

MAA13 MAB13 <41>

MAA13 MAB13 <41>

MAA13 MAB13 <41>

MAA13 MAB13 <41>



UV1D

MEMORY INTERFACE B

MDB0	C5	DOB_0	P8	MAB0	MAB[13..0]	MAB[13..0] <42>
MDB1	C3	DOB_1	T9	MAB1		
MDB2	E3	DOB_2	P9	MAB2		
MDB3	E1	DOB_3	N7	MAB3		
MDB4	F1	DOB_4	N8	MAB4		
MDB5	F3	DOB_5	N9	MAB5		
MDB6	F5	DOB_6	U9	MAB6		
MDB7	G4	DOB_7	U8	MAB7		
MDB8	H5	DOB_8	W9	MAB8		
MDB9	H6	DOB_9	AC8	MAB9		
MDB10	J4	DOB_10	AC9	MAB10		
MDB11	K6	DOB_11	AA7	MAB11		
MDB12	K5	DOB_12	AA7	MAB12		
MDB13	L4	DOB_13	AA7	MAB13		
MDB14	K6	DOB_14	AA7	MAB14		
MDB15	M1	DOB_15	AA7	MAB15		
MDB16	M3	DOB_16	AA7	MAB16		
MDB17	M5	DOB_17	AA7	MAB17		
MDB18	N4	DOB_18	AA7	MAB18		
MDB19	P6	DOB_19	AA7	MAB19		
MDB20	P5	DOB_20	AA7	MAB20		
MDB21	T6	DOB_21	AA7	MAB21		
MDB22	T6	DOB_22	AA7	MAB22		
MDB23	T1	DOB_23	AA7	MAB23		
MDB24	U4	DOB_24	AA7	MAB24		
MDB25	V6	DOB_25	AA7	MAB25		
MDB26	V3	DOB_26	AA7	MAB26		
MDB27	V1	DOB_27	AA7	MAB27		
MDB28	Y6	DOB_28	AA7	MAB28		
MDB29	Y1	DOB_29	AA7	MAB29		
MDB30	Y1	DOB_30	AA7	MAB30		
MDB31	Y5	DOB_31	AA7	MAB31		
MDB32	AA4	DOB_32	AA7	MAB32		
MDB33	AB6	DOB_33	AA7	MAB33		
MDB34	AB1	DOB_34	AA7	MAB34		
MDB35	AB3	DOB_35	AA7	MAB35		
MDB36	AD6	DOB_36	AA7	MAB36		
MDB37	AD1	DOB_37	AA7	MAB37		
MDB38	AD3	DOB_38	AA7	MAB38		
MDB39	AD6	DOB_39	AA7	MAB39		
MDB40	AF1	DOB_40	AA7	MAB40		
MDB41	AF3	DOB_41	AA7	MAB41		
MDB42	AF6	DOB_42	AA7	MAB42		
MDB43	AG4	DOB_43	AA7	MAB43		
MDB44	AH6	DOB_44	AA7	MAB44		
MDB45	AH6	DOB_45	AA7	MAB45		
MDB46	A14	DOB_46	AA7	MAB46		
MDB47	AK3	DOB_47	AA7	MAB47		
MDB48	AF3	DOB_48	AA7	MAB48		
MDB49	AF9	DOB_49	AA7	MAB49		
MDB50	AG8	DOB_50	AA7	MAB50		
MDB51	AG7	DOB_51	AA7	MAB51		
MDB52	AK3	DOB_52	AA7	MAB52		
MDB53	AL7	DOB_53	AA7	MAB53		
MDB54	AM8	DOB_54	AA7	MAB54		
MDB55	AM7	DOB_55	AA7	MAB55		
MDB56	AK1	DOB_56	AA7	MAB56		
MDB57	AL4	DOB_57	AA7	MAB57		
MDB58	AM6	DOB_58	AA7	MAB58		
MDB59	AM4	DOB_59	AA7	MAB59		
MDB60	AP3	DOB_60	AA7	MAB60		
MDB61	AP3	DOB_61	AA7	MAB61		
MDB62	AP1	DOB_62	AA7	MAB62		
MDB63	AP5	DOB_63	AA7	MAB63		

MAB[13..0] → MAB[13..0] <42>

B_BA[2..0] → B_BA[2..0] <42>

DQMB#[7..0] <42>

QSB[7..0] <42>

QSB#[7..0] <42>

ODTB0 ODTB1 <42>

ODTB0 ODTB1 <42>

CLKB0 CLKB0# <42>

CLKB0# CLKB0# <42>

CLKB1 CLKB1# <42>

CLKB1# CLKB1# <42>

RASB0# RASB1# <42>

RASB1# RASB1# <42>

CASB0# CASB1# <42>

CASB1# CASB1# <42>

CSB0#_0 CSB0#_0 <42>

CSB0#_0 CSB0#_0 <42>

CSB1#_0 CSB1#_0 <42>

CSB1#_0 CSB1#_0 <42>

CKEB0 CKEB1 <42>

CKEB1 CKEB1 <42>

WEB0# WEB1# <42>

WEB1# WEB1# <42>

MSX@ RV132 4.7K_0402_5% 0.1U_0402_16V4Z

MSX@ RV132 4.7K_0402_5% 0.1U_0402_16V4Z

MSX@ RV132 4.7K_0402_5% 0.1U_0402_16V4Z

MSX@ RV132 4.7K_0402_5% 0.1U_0402_16V4Z

MSX@ RV132 4.7K_0402_5% 0.1U_0402_16V4Z

MSX@ RV132 4.7K_0402_5% 0.1U_0402_16V4Z

MSX@ RV132 4.7K_0402_5% 0.1U_0402_16V4Z

MSX@ RV132 4.7K_0402_5% 0.1U_0402_16V4Z

MSX@ RV132 4.7K_0402_5% 0.1U_0402_16V4Z

MSX@ RV132 4.7K_0402_5% 0.1U_0402_16V4Z

MSX@ RV132 4.7K_0402_5% 0.1U_0402_16V4Z

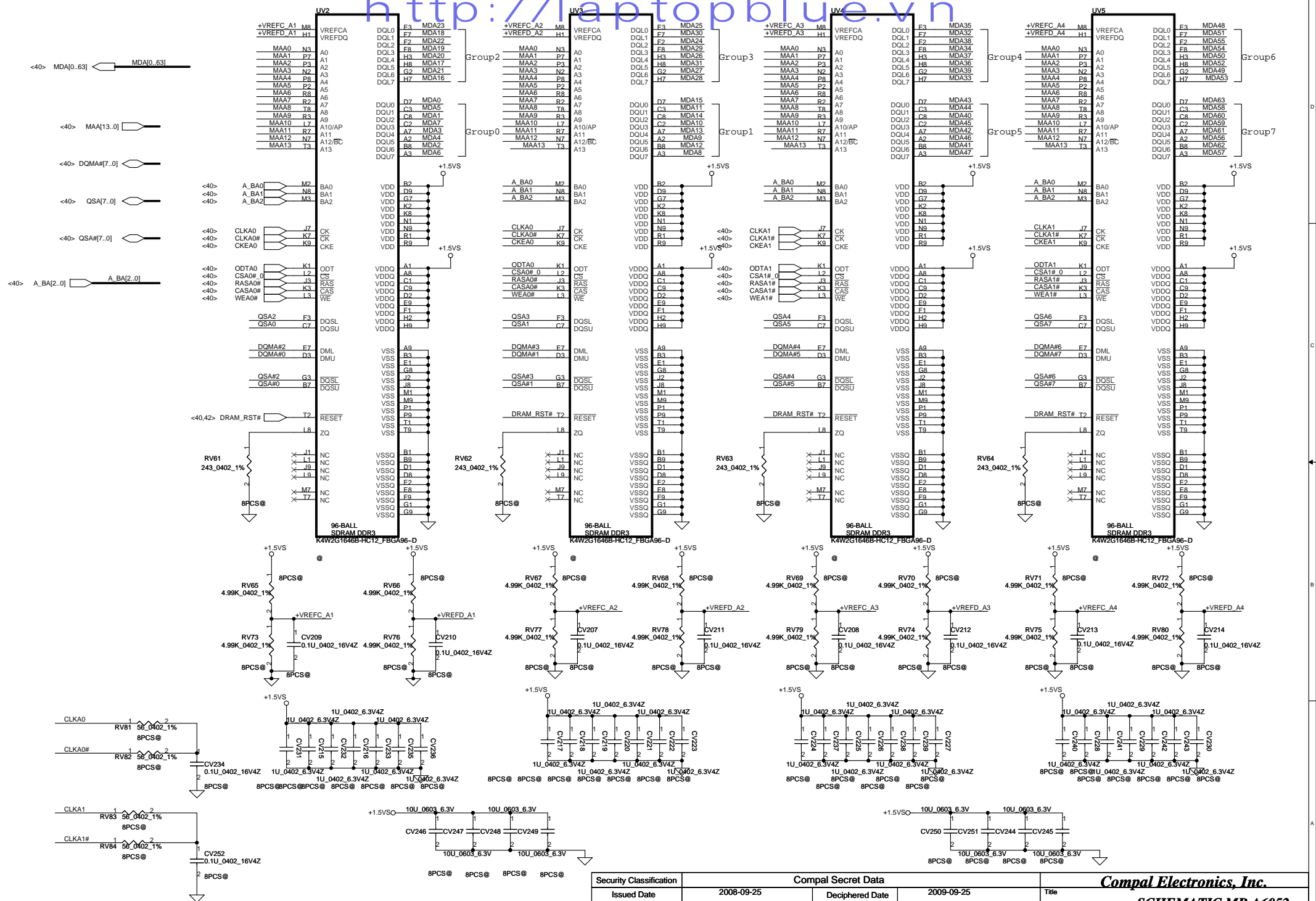
MSX@ RV132 4.7K_0402_5% 0.1U_0402_16V4Z

MSX@ RV132 4.7K_0402_5% 0.1U_0402_16V4Z

MSX@ RV132 4.7K_0402_5% 0.1U_0402_16V4Z

MSX@ RV132 4.7K_0402_5% 0.1U_0402_16V4Z

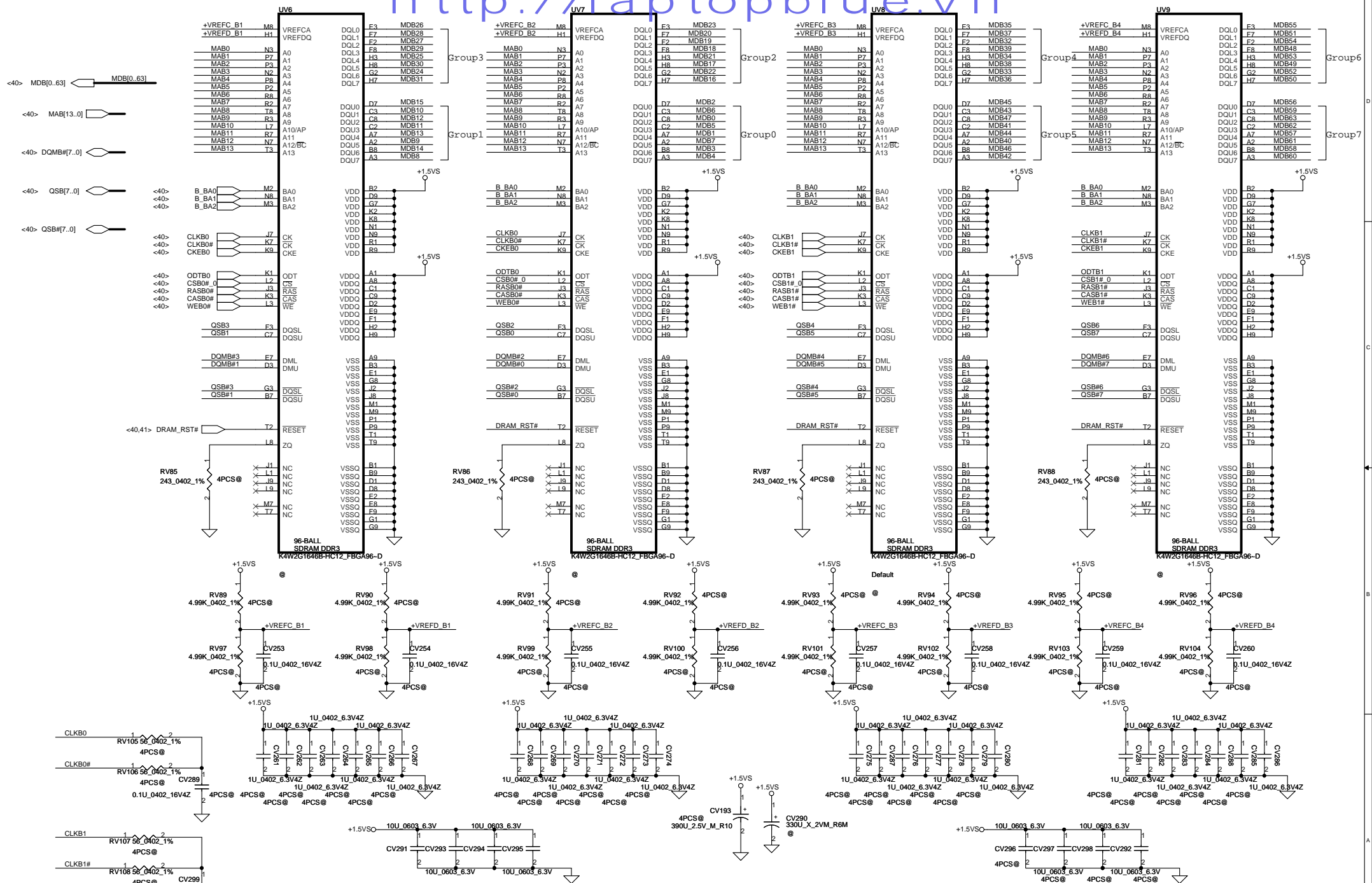
Security Classification	Compal Secret Data	Compal Electronics, Inc.
Issued Date	2008-09-25	Deciphered Date
2008-09-25	2009-09-25	2009-09-25
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		
Size	Document Number	Rev
401851	401851	A
Date	Wednesday, January 20, 2010	Sheet
40	40	53



Security Classification			Compal Secret Data		Title
Issued Date	2008-09-25	Deciphered Date	2009-09-25		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					Document Number
					401851
					Rev A
					Date: Wednesday, January 20, 2010
					Sheet 41 of 53

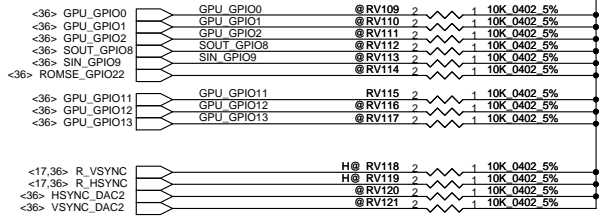
Compal Electronics, Inc.

SCHEMATIC, MB A6052



Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2008-09-25				Deciphered Date			
								2009-09-25			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.											
Title				Document Number				401851			
Date				Wednesday, January 20, 2010				Sheet 42 of 53			

GPU by the system BIOS		GPU by VBIOS
GPIO22 = 0 (BIOS_ROM_EN = 0)		GPIO22 = 1 (BIOS_ROM_EN = 1)
GPIO[13:11]	MEMORY SIZE	GPIO[13:11]
0 0 0	128MB	1 0 0 (M25P05A)
0 0 1	256MB	
0 1 0	64MB	

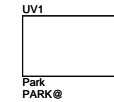
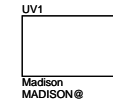
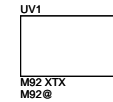
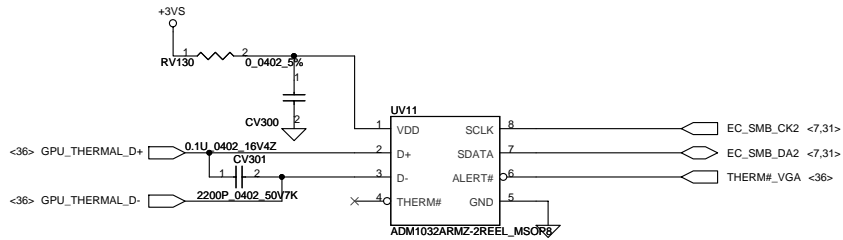


STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	0
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	0
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0
BIF_VGA_DIS	GPIO9	VGA Controller ENABLED	0 (Enable)
BIOS_ROM_EN	GPIO_22_ROMCSB	Enable External BIOS device	0
ROMIDCFG(2:0)	GPIO[13:11]	ROM Configurations	0 0 1
VIP_DEVICE_STRAP_ENA	VSYNC_DAC2	IGNORE VIP DEVICE STRAPS	0
AUD[1]	HSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	1 1
AUD[0]	VSYNC		
RSVD	HSYNC_DAC2		0
RSVD	GENERICC		0

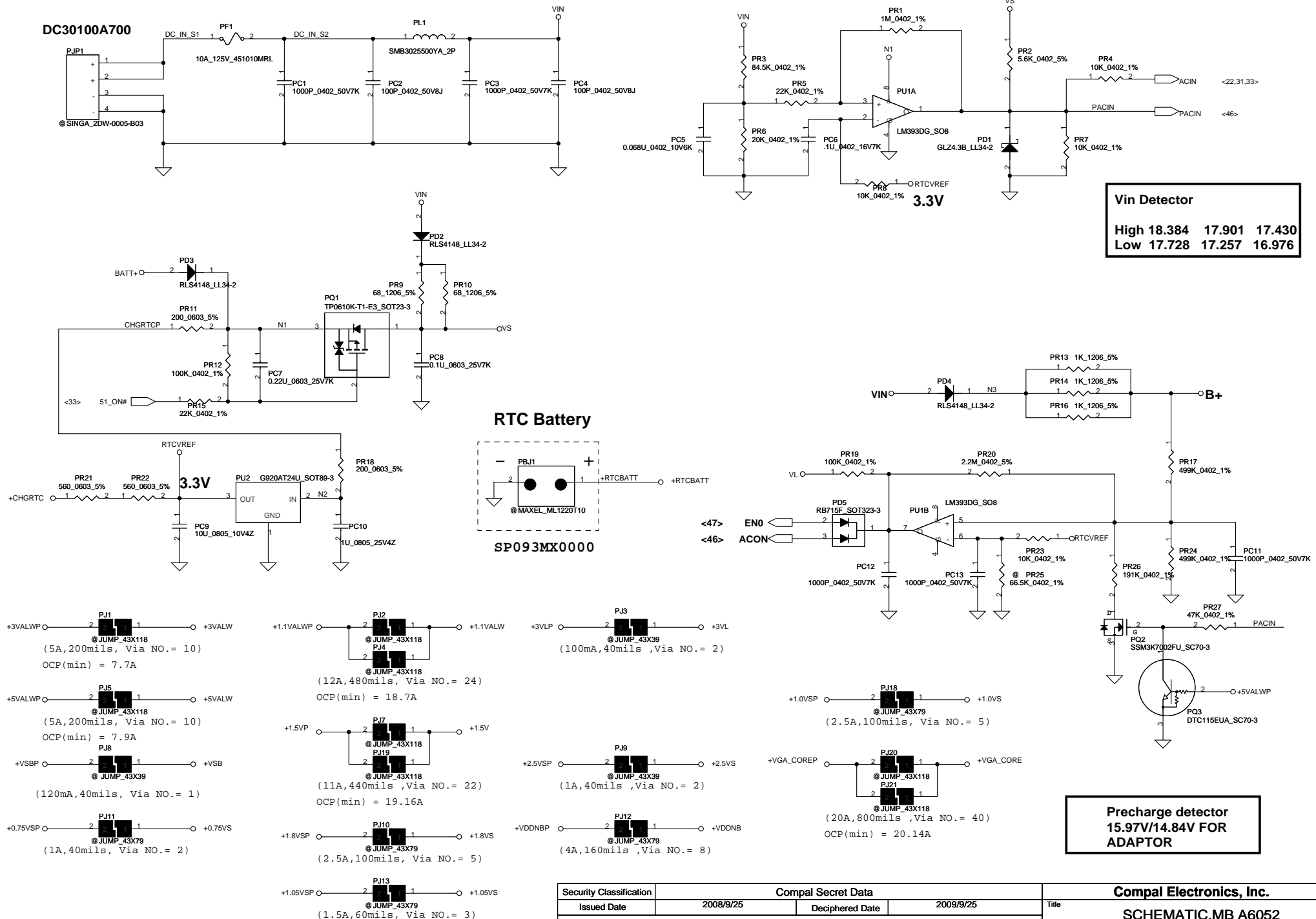
AMD RESERVED CONFIGURATION STRAPS	
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET	
HSYNC_DAC2	GENERICC
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET	
GPIO_28_TDO	GPIO21_BB_EN

STRAPS	PIN	GPU	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 2,1,0
VRAM_ID[2:0]	DVPPDATA (2,1,0)	Park M2	512M 64Mx16 (x4)	HYN H5TQ1G63BFR-12C	SA000032400	0 0 0
			512M 64Mx16 (x4)	SAM K4W1G1646E-HC12	SA000035700	0 0 1
			1G 128Mx16 (x4)	HYN		0 1 0 (Reserve)
			1G 128Mx16 (x4)	SAM K4W2G1646B-HC12	SA00003MQ00	0 1 1 (Reserve)
		Madison M2	1G 64Mx16 (x8)	HYN H5TQ1G63BFR-12C	SA000032400	1 0 0
			1G 64Mx16 (x8)	SAM K4W1G1646E-HC12	SA000035700	1 0 1
			2G 128Mx16 (x8)	HYN		1 1 0 (Reserve)
			2G 128Mx16 (x8)	SAM K4W2G1646B-HC12	SA00003MQ00	1 1 1 (Reserve)

External VGA Thermal Sensor



Security Classification	Compal Secret Data		Title	
Issued Date	2008-09-25	Deciphered Date	2009-09-25	Rev A
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number 401851
Date: Wednesday, January 20, 2010				Sheet 43 of 53



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/9/25	Deciphered Date	2009/9/25	Title	SCHEMATIC, MB A6052
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	401851
				Date	Wednesday, January 20, 2010
				Sheet	44 of 53

PH1 under CPU botten side :

CPU thermal protection at 95 degree C

Recovery at 56 degree C

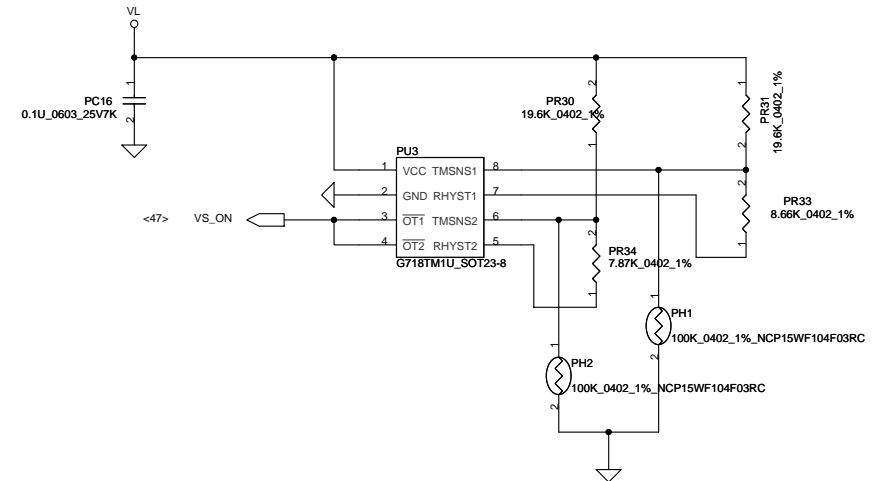
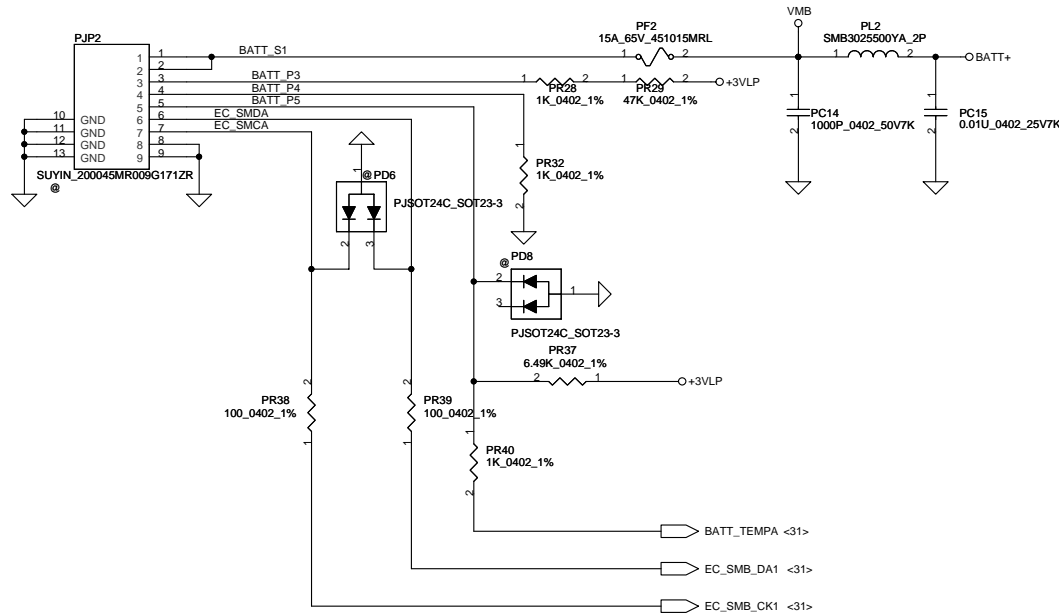
$$R_{set} = 3 * R_{tmh}$$

$$R_{hyst} = (R_{set} * R_{tml}) / (3 * R_{tml} - R_{set})$$

$$R_{tmh} \text{ at } 95C = 6.64K, R_{tml} \text{ at } 57C = 25.1K$$

$$R_{set} = 3 * 6.64K = 19.92K \Rightarrow 19.6K$$

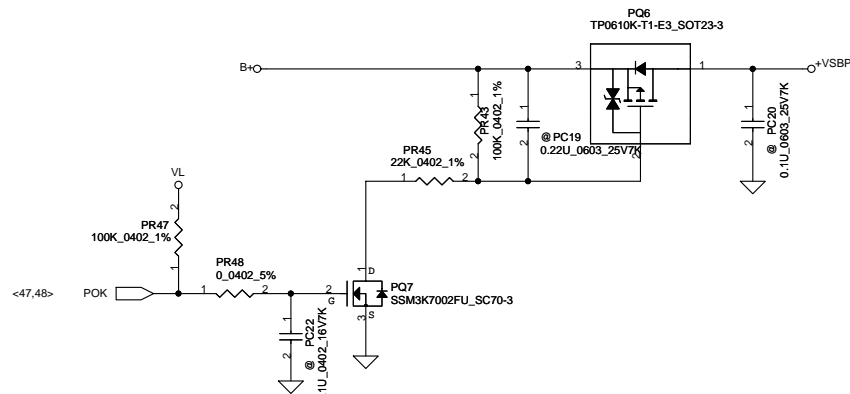
$$R_{hyst} = (20K * 25.1K) / (3 * 25.1K - 20K) = 9.078K \Rightarrow 9.09K$$

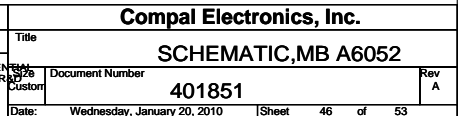


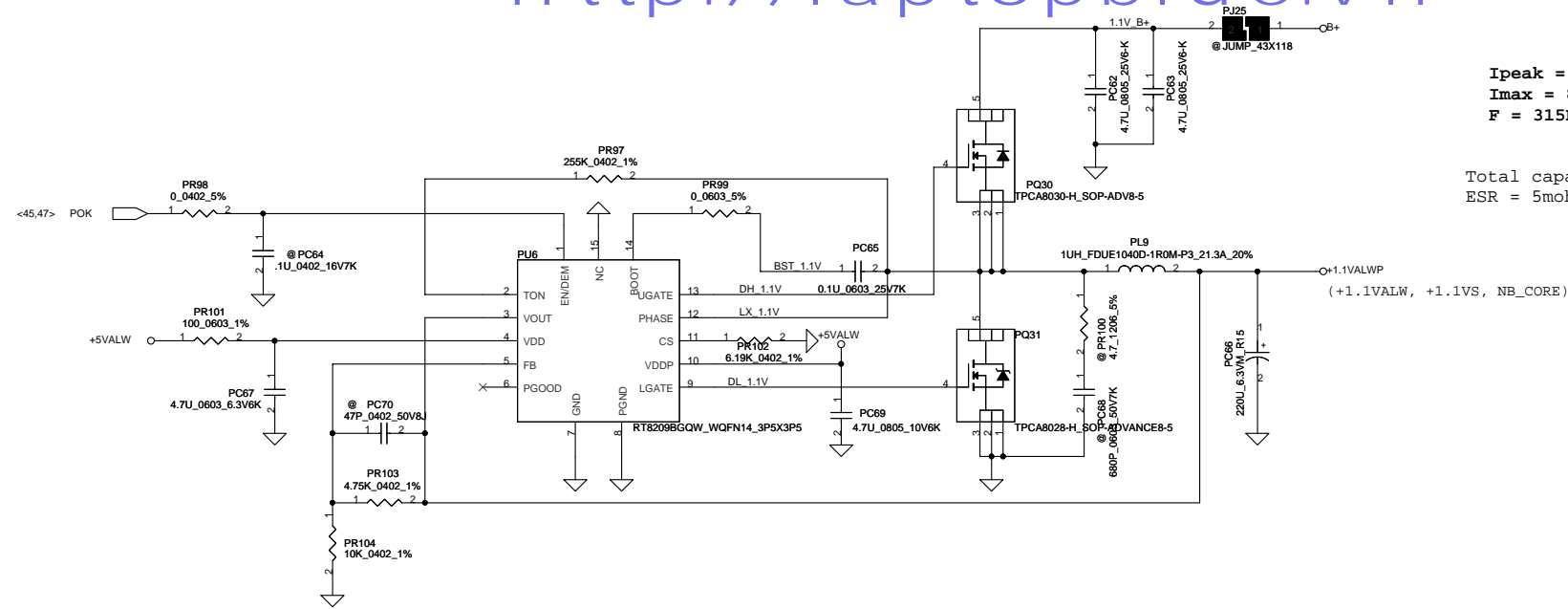
PH2 near main Battery CONN :

BAT. thermal protection at 95 degree C

Recovery at 48 degree C

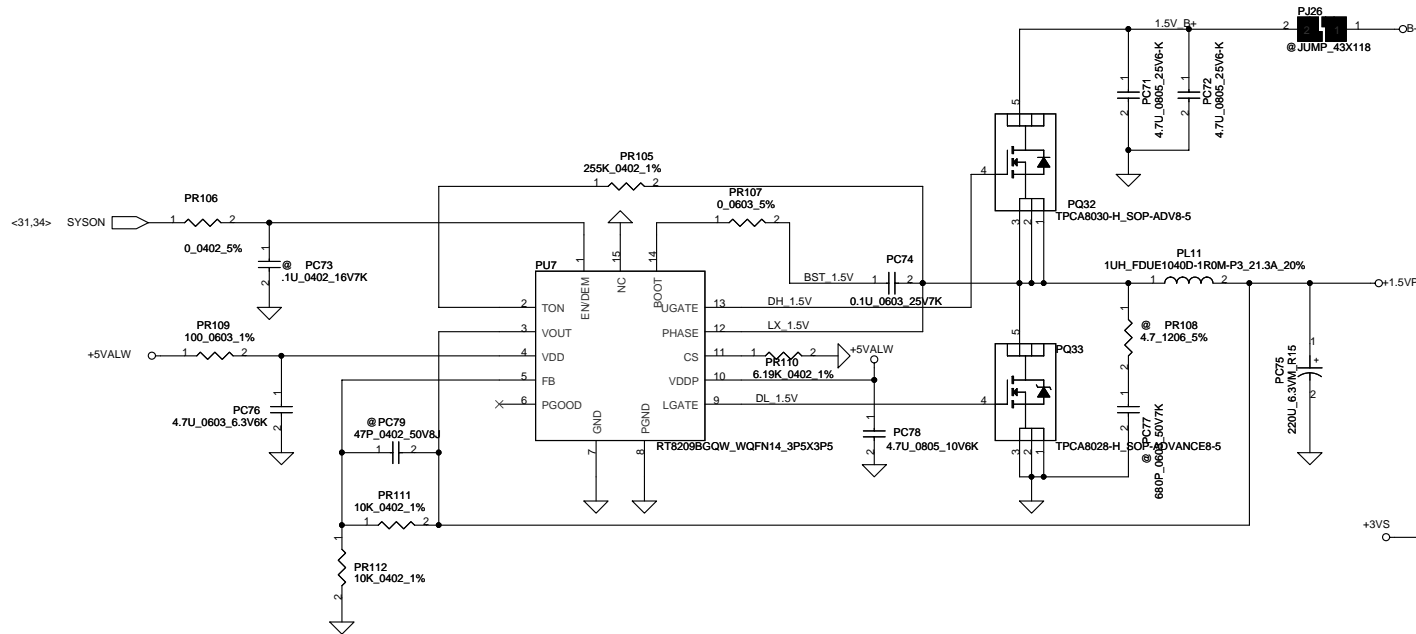






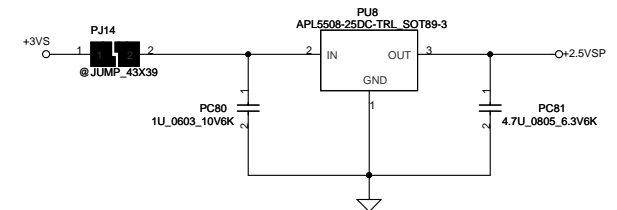
Ipeak = 12A
Imax = 8.4A
F = 315K

Total capacitor 880uF
ESR = 5mohm

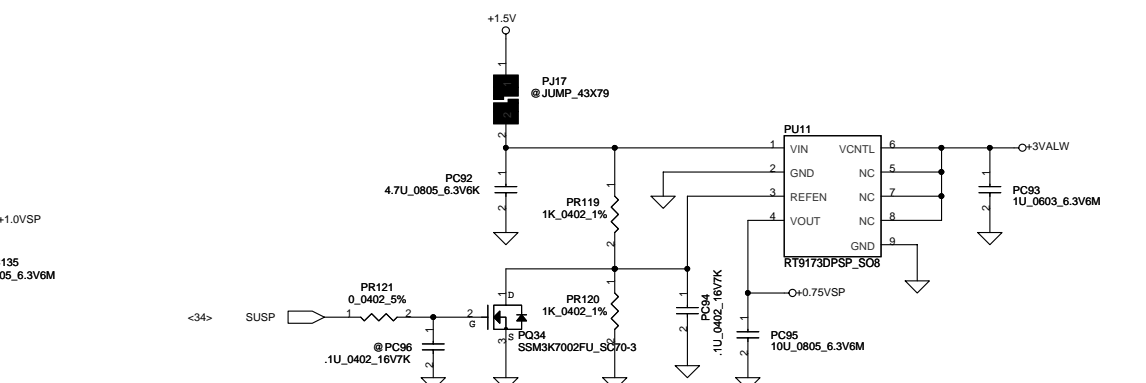
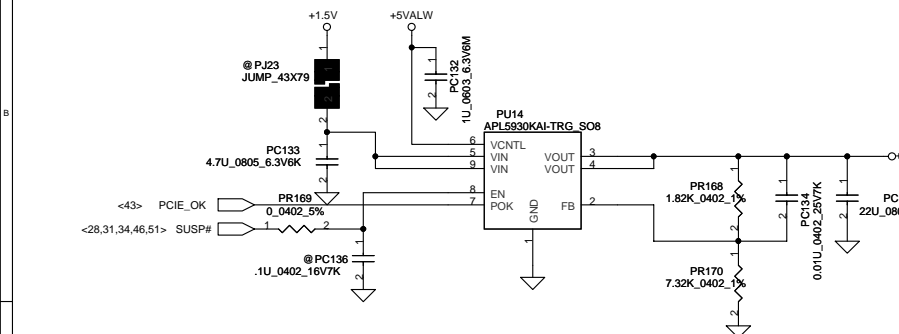
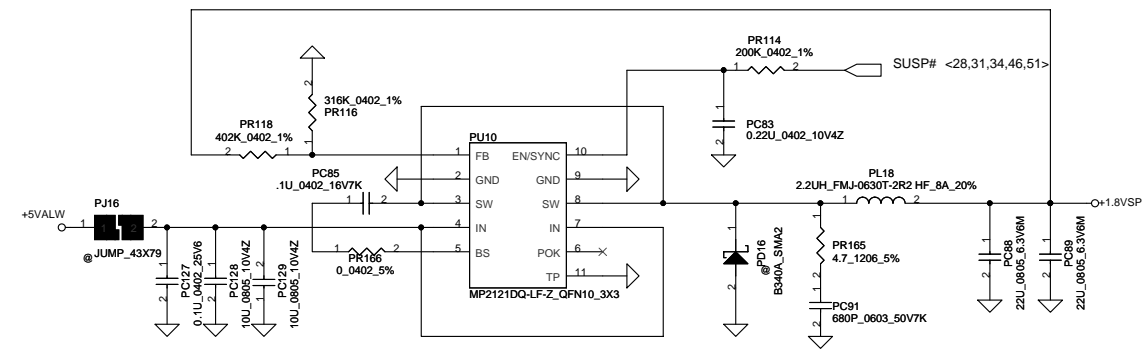
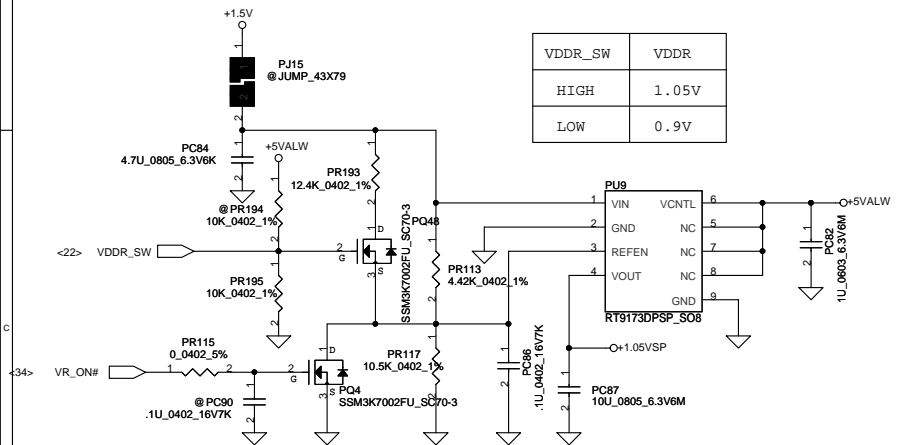


Ipeak = 11A
Imax = 7.7A
F = 315K

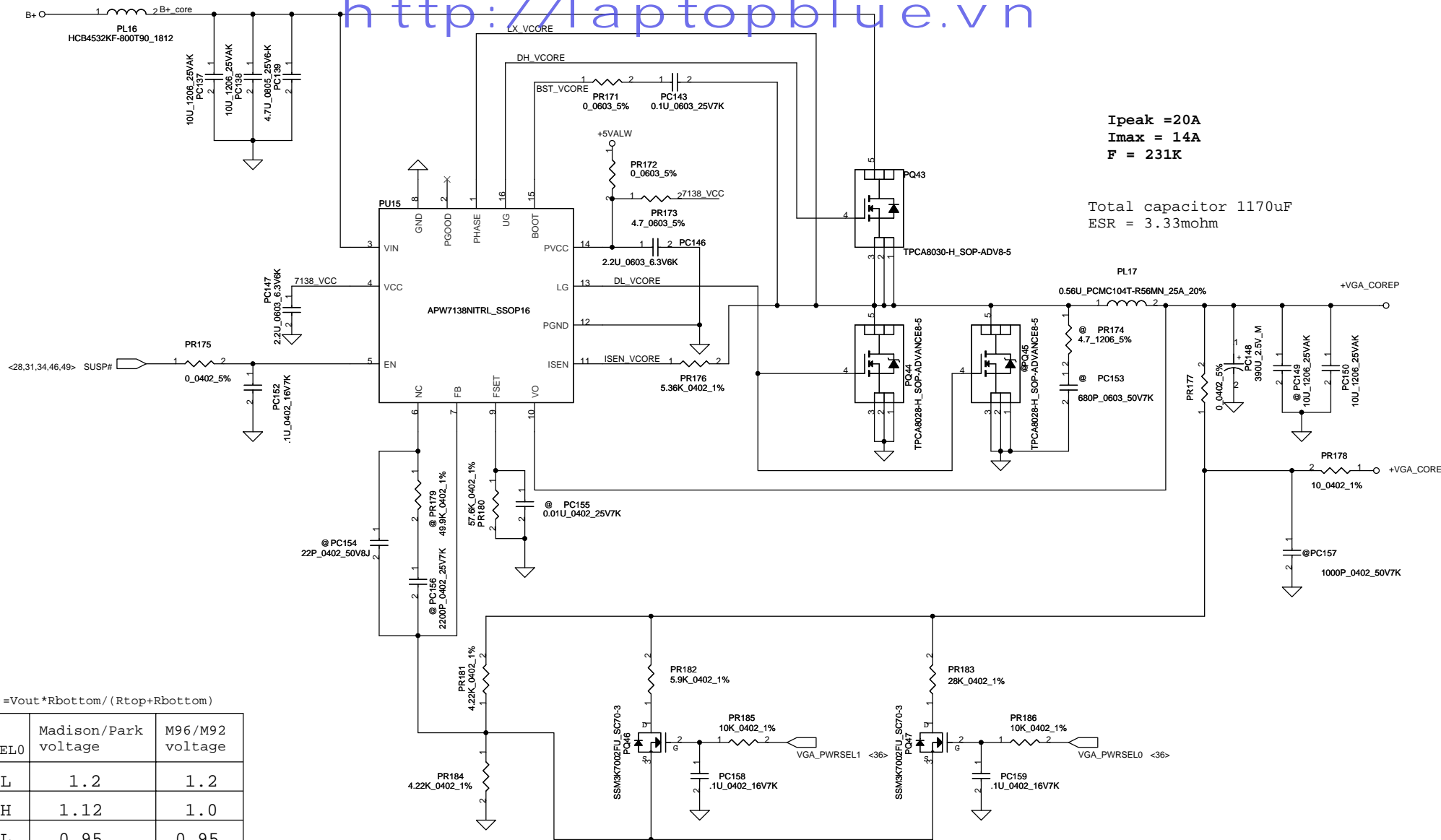
Total capacitor 1390uF
ESR = 2.73mohm



Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2008/9/25				Deciphered Date			
2008/9/25				2009/9/25				Title			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number				SCHEMATIC, MB A6052			
				401851				Rev A			
Date:				Wednesday, January 20, 2010				Sheet 48 of 53			



Madison / Park PCIE : 1.0V	M96 / M92 PCIE : 1.1V
PR170 = 7.32K	PR170 = 4.75K



I_{peak} = 20A
I_{max} = 14A
F = 231K

Total capacitor 1170uF
ESR = 3.33mohm

$$VFB(0.6) = V_{out} \cdot R_{bottom} / (R_{top} + R_{bottom})$$

SEL1	SEL0	Madison/Park voltage	M96/M92 voltage
L	L	1.2	1.2
L	H	1.12	1.0
H	L	0.95	0.95
H	H	0.9	0.9

$$FSW = 1 / (75E-12 \cdot 57.6K) = 231.48KHz$$

Madison Park	M96 M92
PR183 = 28K	PR183 = 12K

Security Classification		Compal Secret Data				Compal Electronics, Inc.															
Issued Date		2008/10/23		Deciphered Date		2009/10/23		Title		SCHEMATIC, MB A6052											
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.										Size		Document Number		401851		Rev A					
										Custom											
										Date:		Wednesday, January 20, 2010				Sheet		51		of	

PIR (Product Improve Record)
NALAE LA-6052P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2

NO	DATE	PAGE	MODIFICATION LIST
1	2009/12/14	33	Change JLEDB pin define as customer request
2	2009/12/14	25,28,30	Delete JODDB, JBT and JUSBB support pin
3	2009/12/14	33	Change JPOWER Pin2 from GND to NC
4	2009/12/15	28	Add R95 at JWLAN Pin5 for BT/WLAN combo Mini Card
5	2009/12/15	25,30	Change U11, U25 P/N from SA00002XX00 to SA000033H00
6	2009/12/15	28	Reverse JBT pin definition
7	2009/12/16	27	Change CC2 from 0.1u to 100P (SE071101J80), and add BOM structure @
8	2009/12/17	33	Cgange JPOWER footprint to ACES_87151-1207_12P (ZIF_上接點)
9	2009/12/17	33	Cgange JTPB footprint to P-TWO_161011-04021_4P-T (NO ZIF), and reverse pin definition
10	2009/12/17	33	Cgange JLEDB footprint to ACES_85201-1205N_12P (ZIF_上接點)
11	2009/12/17	25	Cgange JUSBB footprint to ACES_85201-20051_20P (ZIF_上接點)
12	2009/12/17	33	Change H36, H37 footprint from H_3P3 to H_3P8

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2007/5/18	Deciphered Date	2008/5/18	Title	SCHEMATIC,MB A6052	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	401851	Rev A
Date: Wednesday, January 20, 2010				Sheet	82	of 83

Version Change List (P. I. R. List) for Power Circuit

http://laptopblue.vn

Page#	Item Title	Solution Description
DVT : modification from EVT		
P48	change voltage divider to less than 10K	change PR104, PR111, PR112 to 10K; PR103 to 4.75K
P48	change 1.1V, 1.5V OCP value	change PR102, PR110 to 6.19K
P49	enlarge output cap	change PC88, PC89 to 22uF(S8000000110)
P50	don't use NIPPON cap	change PC98, PC99 to SF0000000S80
P50	pull high RTN1 1.5V	change PR150 to mount
P51	APW7138 pin6 is NC	change PR179, PC154, PC156 to unmount
P47	choke need to meet thermal module height	change PL6, PL7 to SH000006380
P46	change system power from 90W to 120W	change PR72 to 8.25K, PR75 to 26.7K; PQ11 to mount
P50	production line request	change PC98, PC99 to 68uF; add PC160, PC161 68uF
P46	EMI request for ISN issue	add PC162, PC163, PC164 10uF 1206
P49	mount snubber circuit	mount PR165, PC91
P45	OTP setting common	change PR30 and PR31 to 19.6K; PR34 to 7.87K; PR33 to 8.66K
P49	change IC to low cost	change PU9 and PU11 to RT9173
P49	change VDDR(1.05V) circuit to switchable	add PR193, PR194, PR195 & PQ48