

NBQAA

Bordeaux 10G

LA-6072P REV 1.0 Schematic

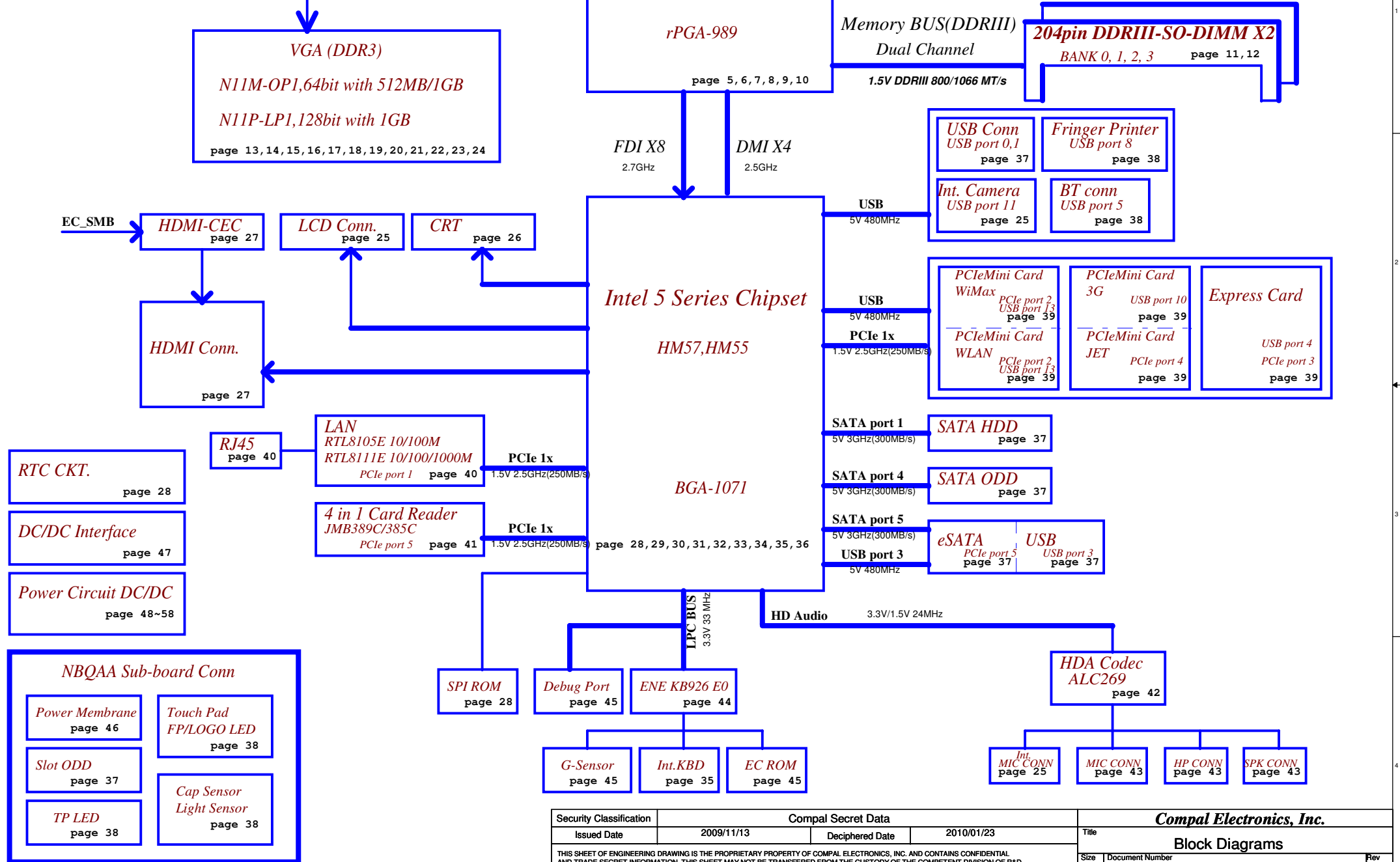
Intel Arrandale CPU / Intel 5 Series Chipset
2010-03-22 Rev 1.0

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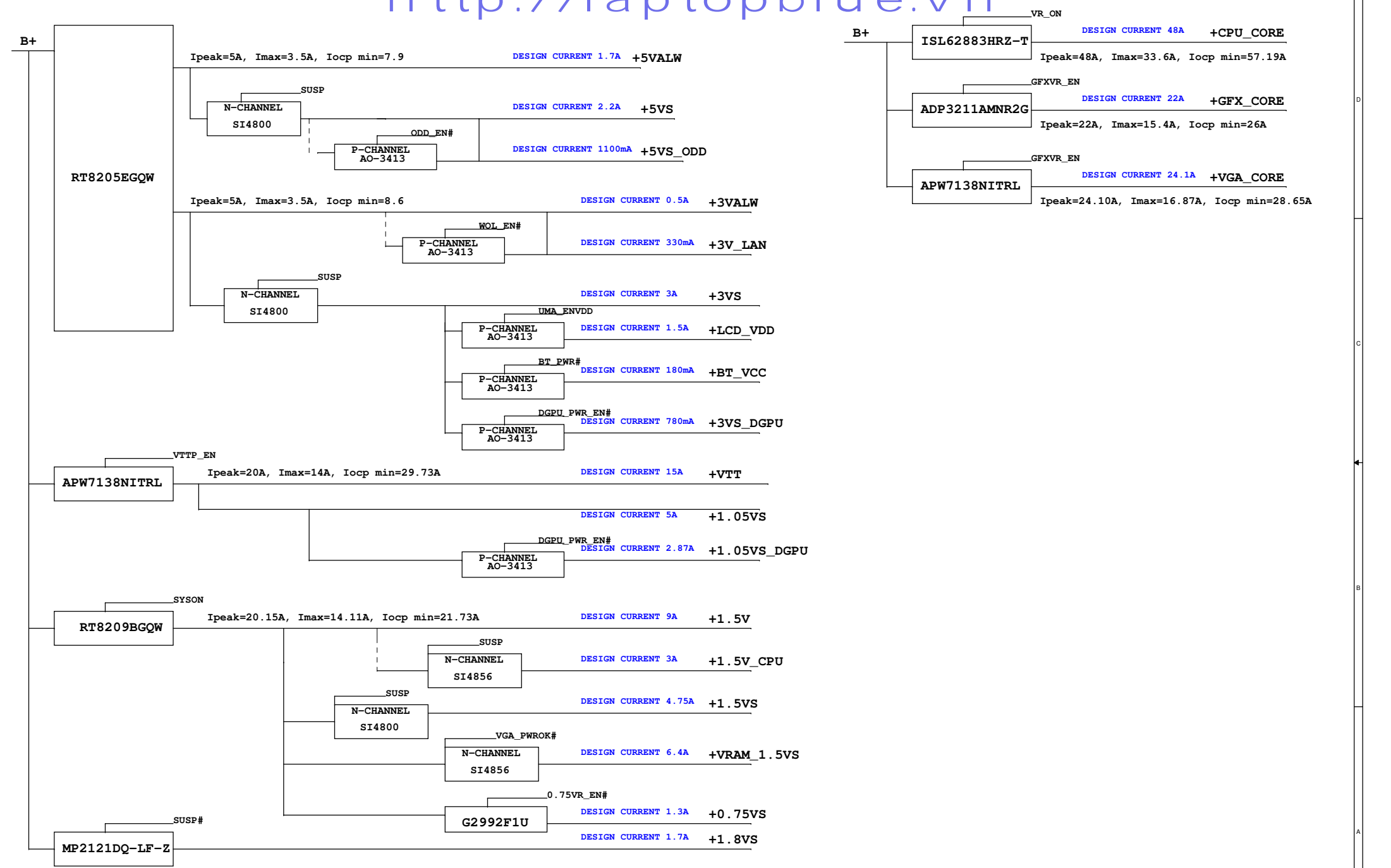
Compal Confidential

Model Name : NBQAA

File Name : LA-6072P



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Size		Document Number		Rev	
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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	+B	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.5VS +VGA_CORE +CPU_CORE +VTT +1.05VS +1.8VS +1.1VS +0.75VS
S0	O	O	O	O	O
S1	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC	O	O	O	X	X
S5 S4/ Battery only	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X

EC SM Bus1 address

EC SM Bus2 address

Power	Device	Address	Power	Device	Address
+3VL	EC KB926 D3		+3VS	EC KB926 D3	
+3VL	HDMI-CEC		+3VS	AMD GPU Thermal Sensor	
+3VL	Smart Battery	0001 011x b	+3VS	Ambient Ligh Sensor	
			+3VALW	PCH	
			+3VS	G-Sensor	

PCH SM Bus address

Power	Device	Address
+3VALW	PCH	
+3VS	Clock Generator	1101 001x b
+3VS	DDR DIMMA	1001 000x b
+3VS	DDR DIMMB	1001 010x b
+3VS	Express	
+3VS	Slot#1-WLAN/Wimax	
+3VS	Slot#2-JET/3G	

BTO Option Table

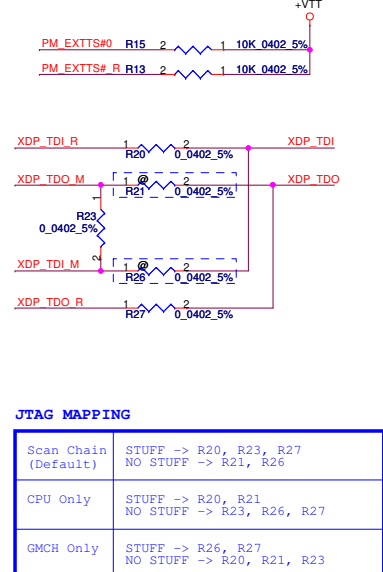
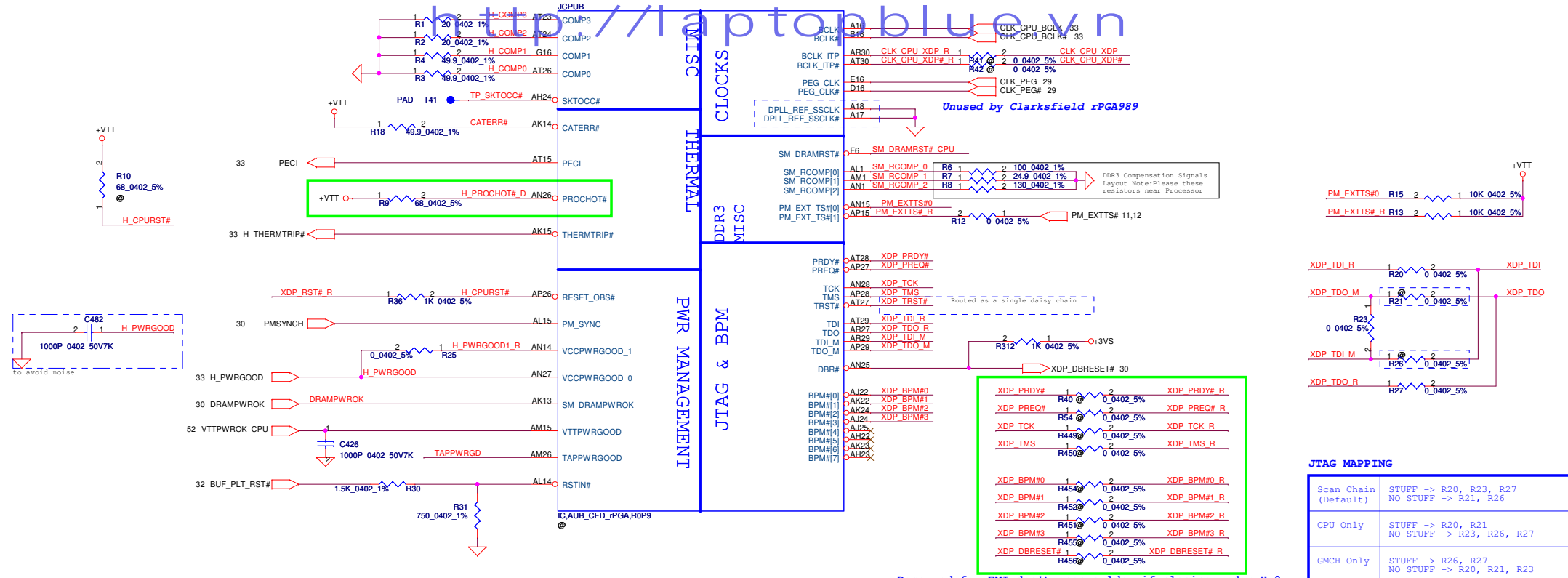
Function	Bluetooth	Card Reader		HDMI-CEC		LAN		CAM+MIC
description	B				Y	U	V	X
explain	Bluetooth	JMB389	JMB385	HDMI	HDMI+CEC	10/100	10/100/1000	CAM
BTO	BT@	JMB389@	JMB385@	IHDMI@	IHDMI@+CEC@	8105E@	8111E@	CAM@

Function	ODD		KB LED	Mini Card			GPU	
description		T	K	G	J		P	M
explain	Normal	Slot	KB LED	3G	JET	3G/JFT	WiMAX	N11M-OP1
BTO	ODD0@	ODD1@	KBL@	3G@	JET@	3GJFT@	WiMAX@	N11P@

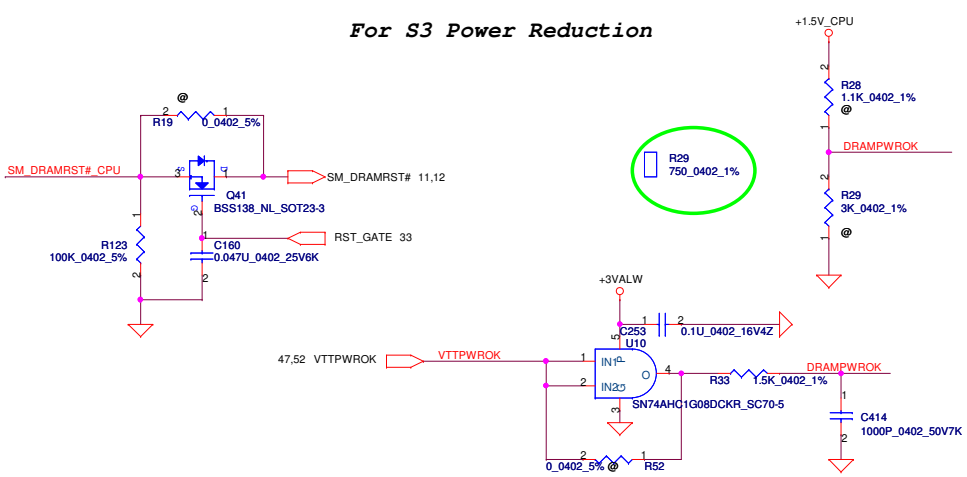
Function	PCH		VRAM	
description	H5	H7	512	1G
explain	HM55	HM57	512M	1G
BTO	HM55@	HM57@	4pcs@	4pcs@+8pcs@

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1 (Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

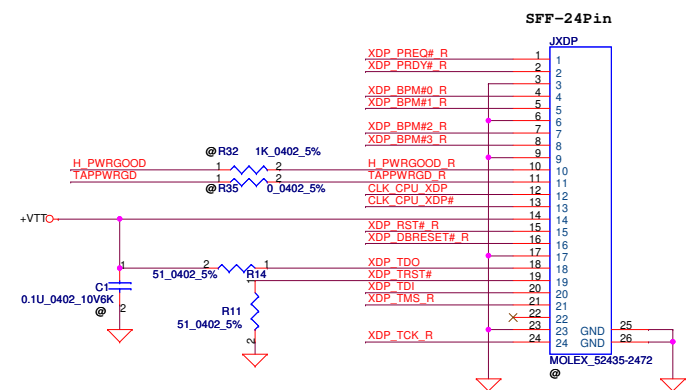
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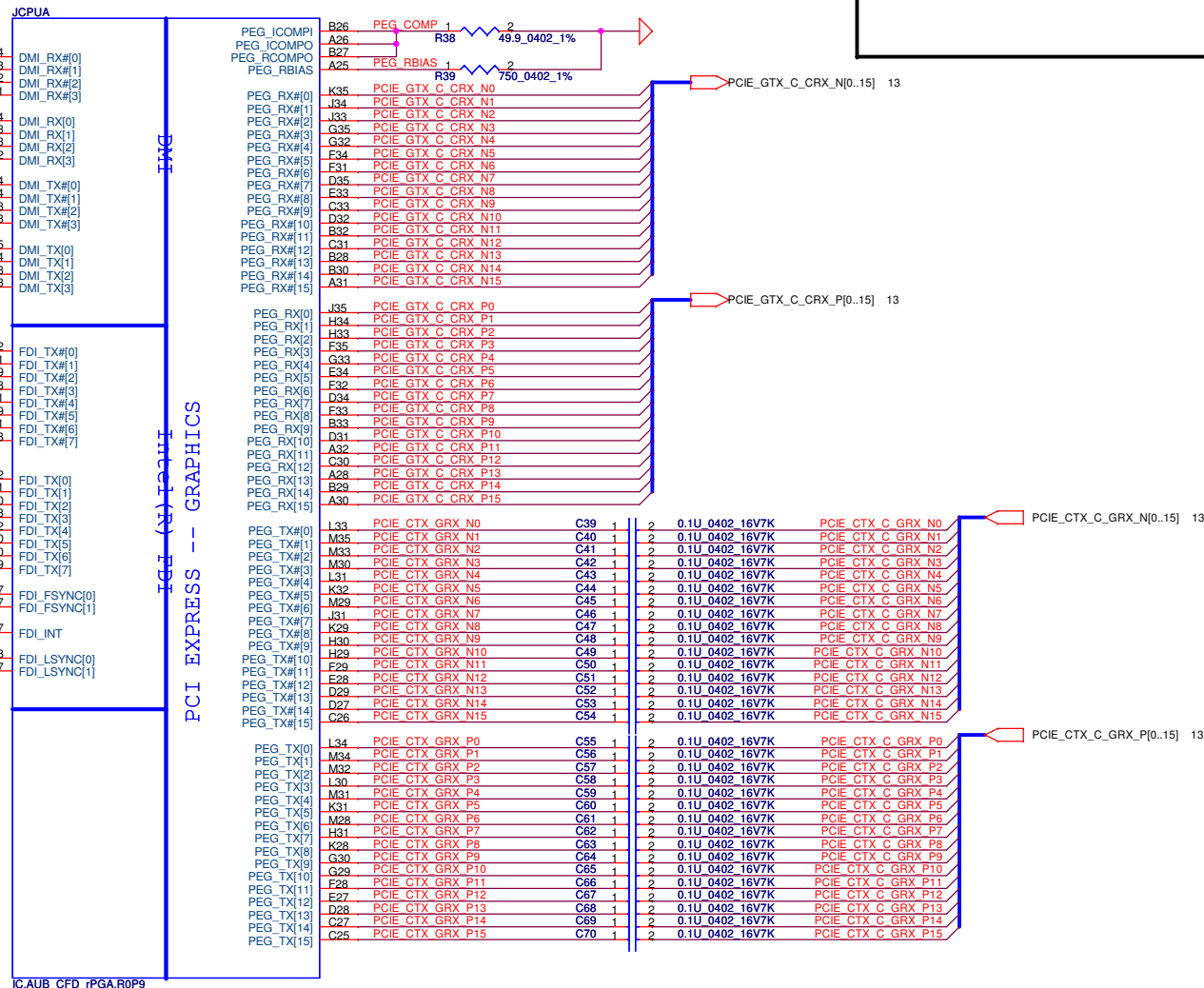
For S3 Power Reduction



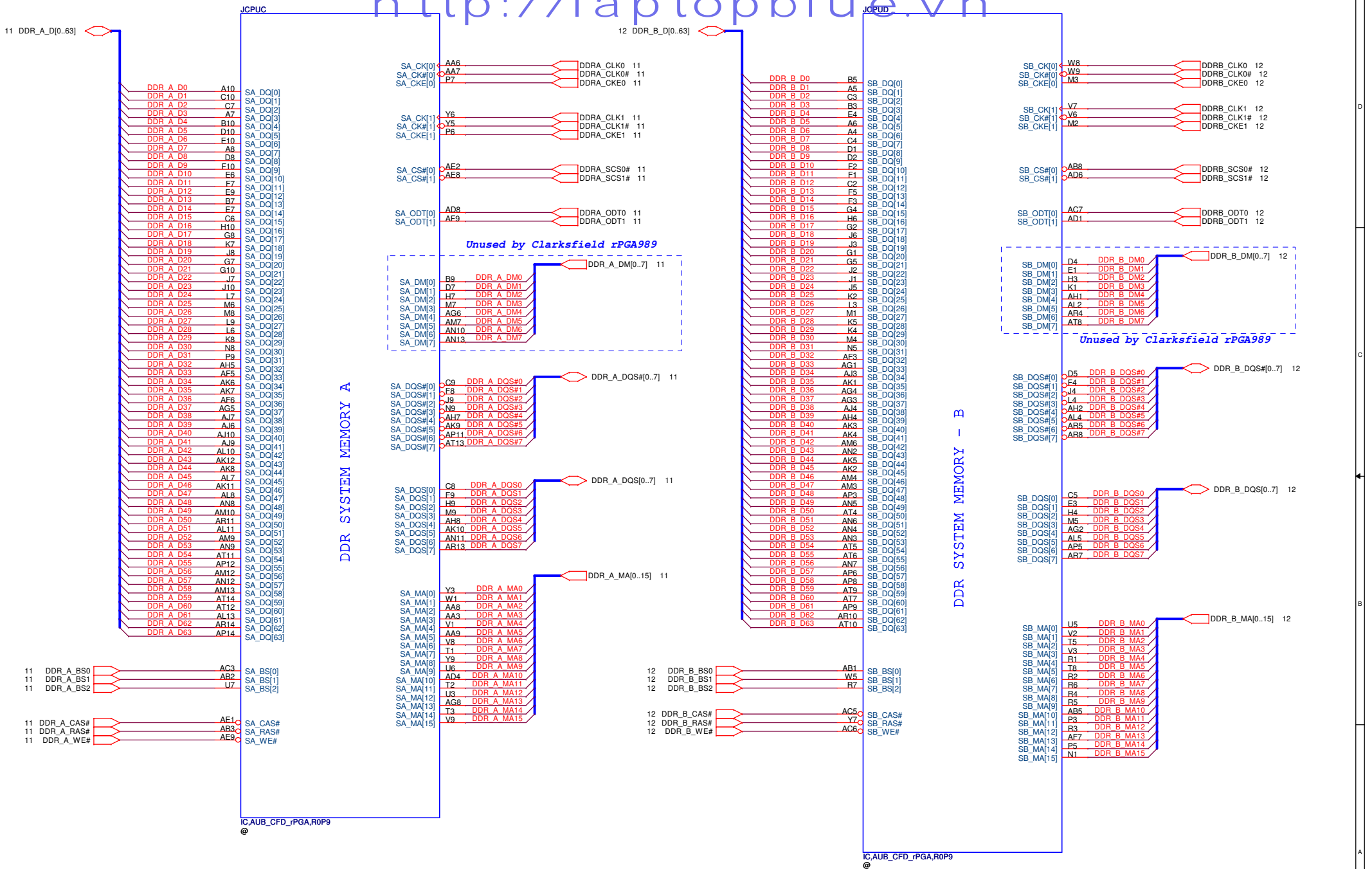
XDP Connector



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Custom		NBQAA LA6072P M/B		1.0	
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				Size B	Document Number	Rev 1.0
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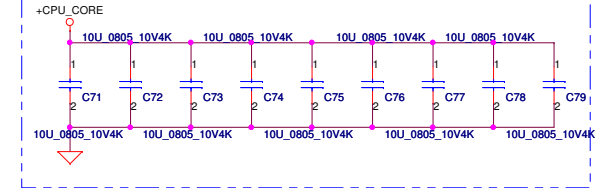


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						Size B		Document Number		Rev 1.0	
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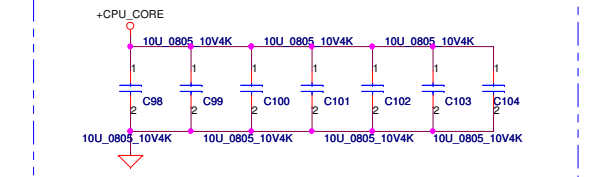
Material Note (+VTT):
330uF/ 6mohm, number are 3,
power x1, HW x2

(Place these capacitors under CPU socket Edge, top layer)

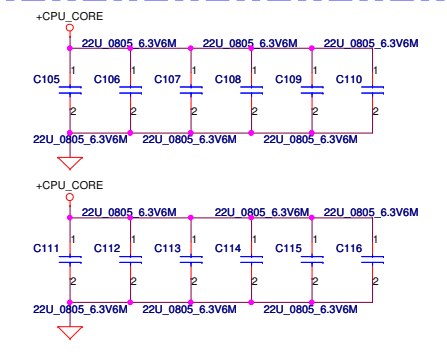
(Place these capacitors between inductor and socket on Bottom)



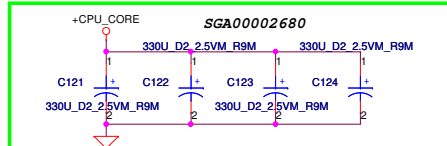
(Place these capacitors under CPU socket, top layer)



(Place these capacitors on CPU cavity, Bottom Layer)

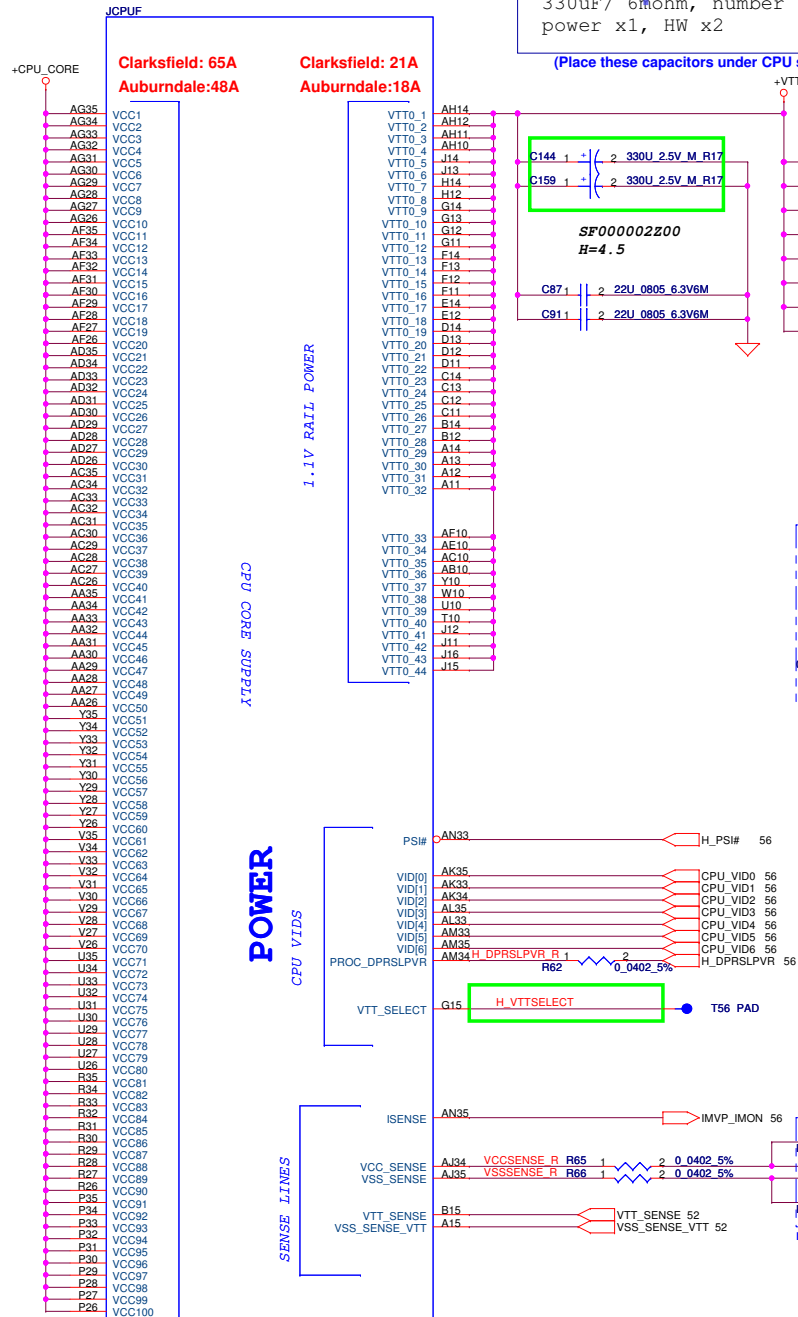


TOP side (under inductor)

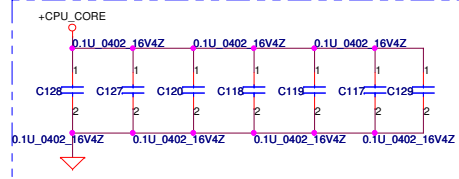


Check list:

+CPU_CORE: 6x 470uF, 12x 22uF, 17x 10uF
+VTT: 4x 330uF, 7x 22uF, 8x 10uF



Add on 2/8 to improve ESD

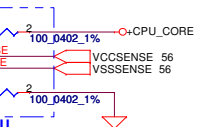


CRB default setting:
VID[6:0]=[0100111]

VTT Rail

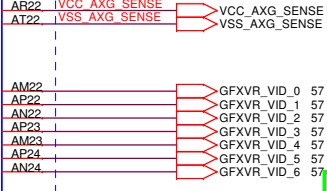
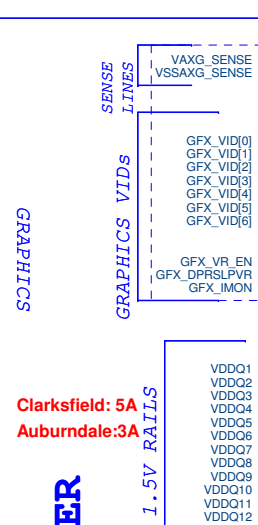
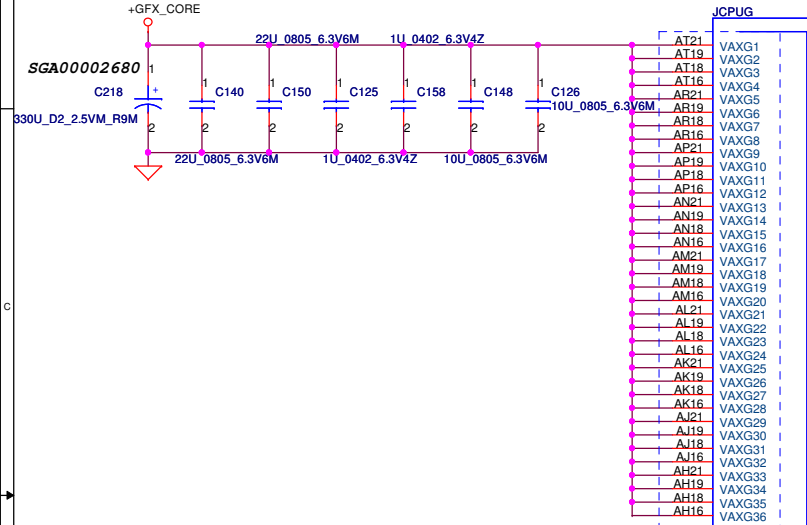
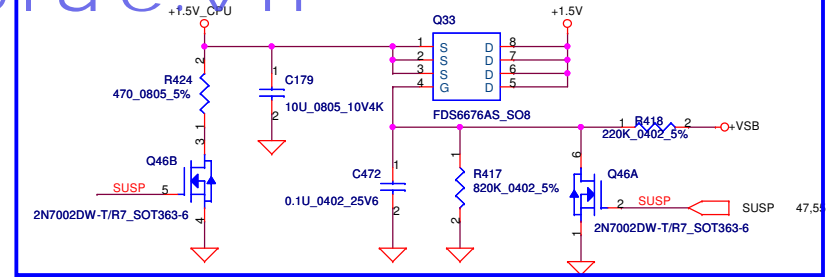
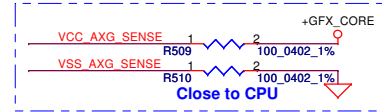
Auburndale +1.1VS_VTT=1.05V
Clarksfield +1.1VS_VTT=1.1V

H_VTTSELECT = low, 1.1V
H_VTTSELECT = high, 1.05V



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								CPU POWER-1			
								Size		Rev	
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To prevent glitch issue
R86 330 0402 5%

Reserved for Clarkfield
R87 1K 0402 5%

Clarkfield: 5A
Auburndale: 3A

POWER

DDR3 - 1.5V RAILS

Clarkfield: 21A
Auburndale: 18A

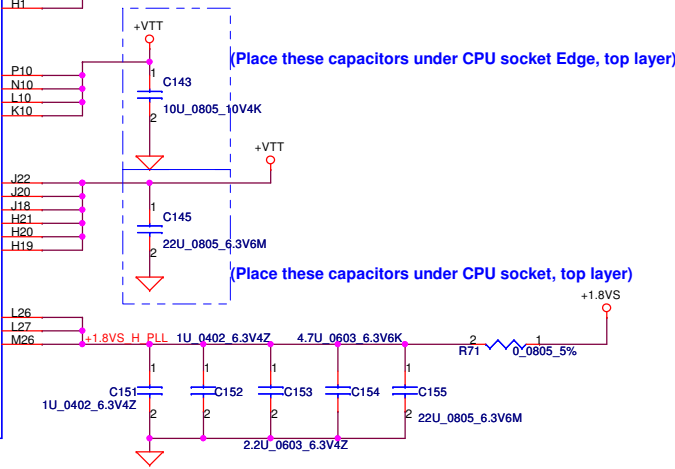
PEG & DMI

1.1V

1.8V

Clarkfield: 1.35A
Auburndale: 1.35A

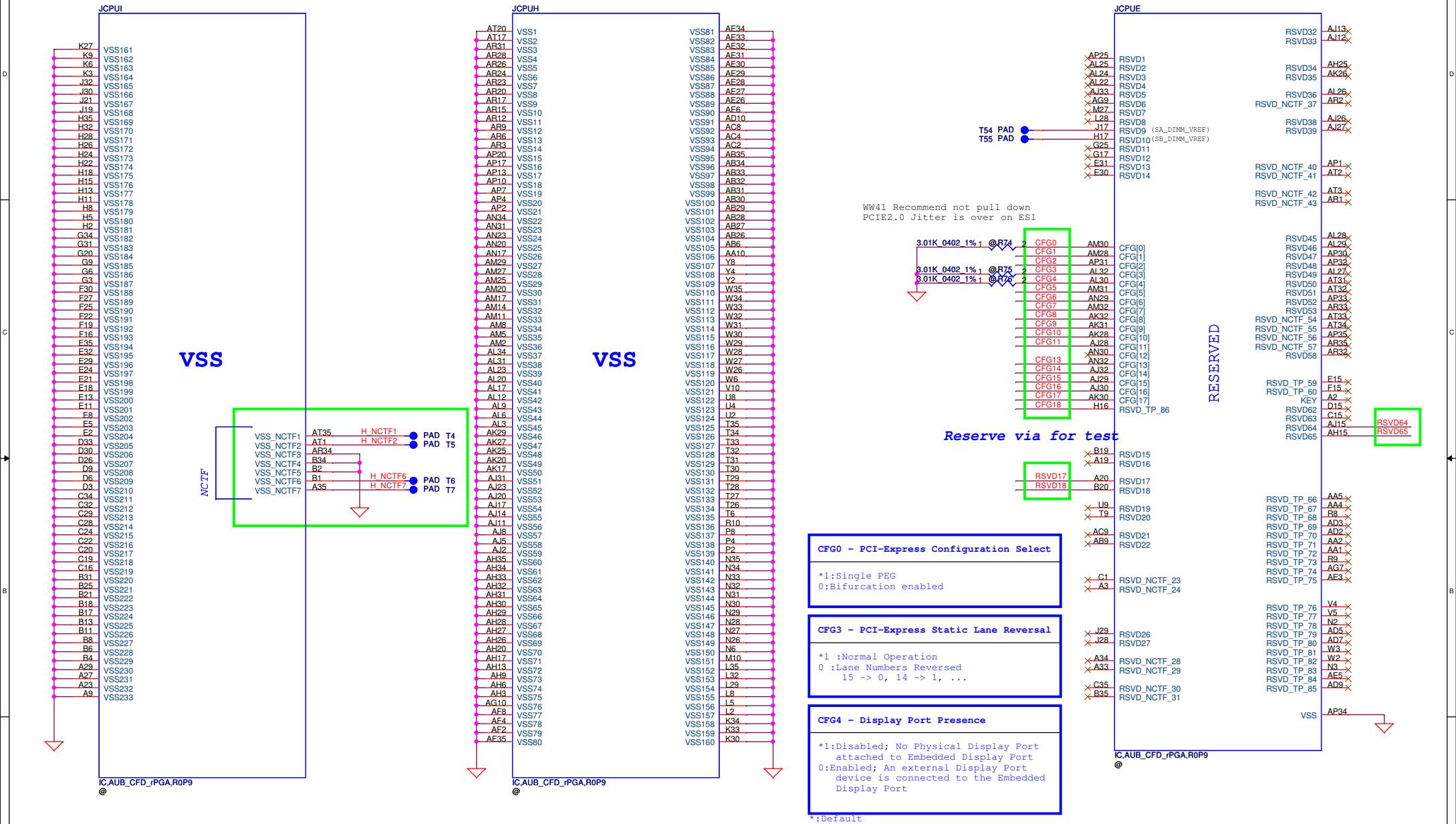
(Place these capacitors under CPU socket, top layer)

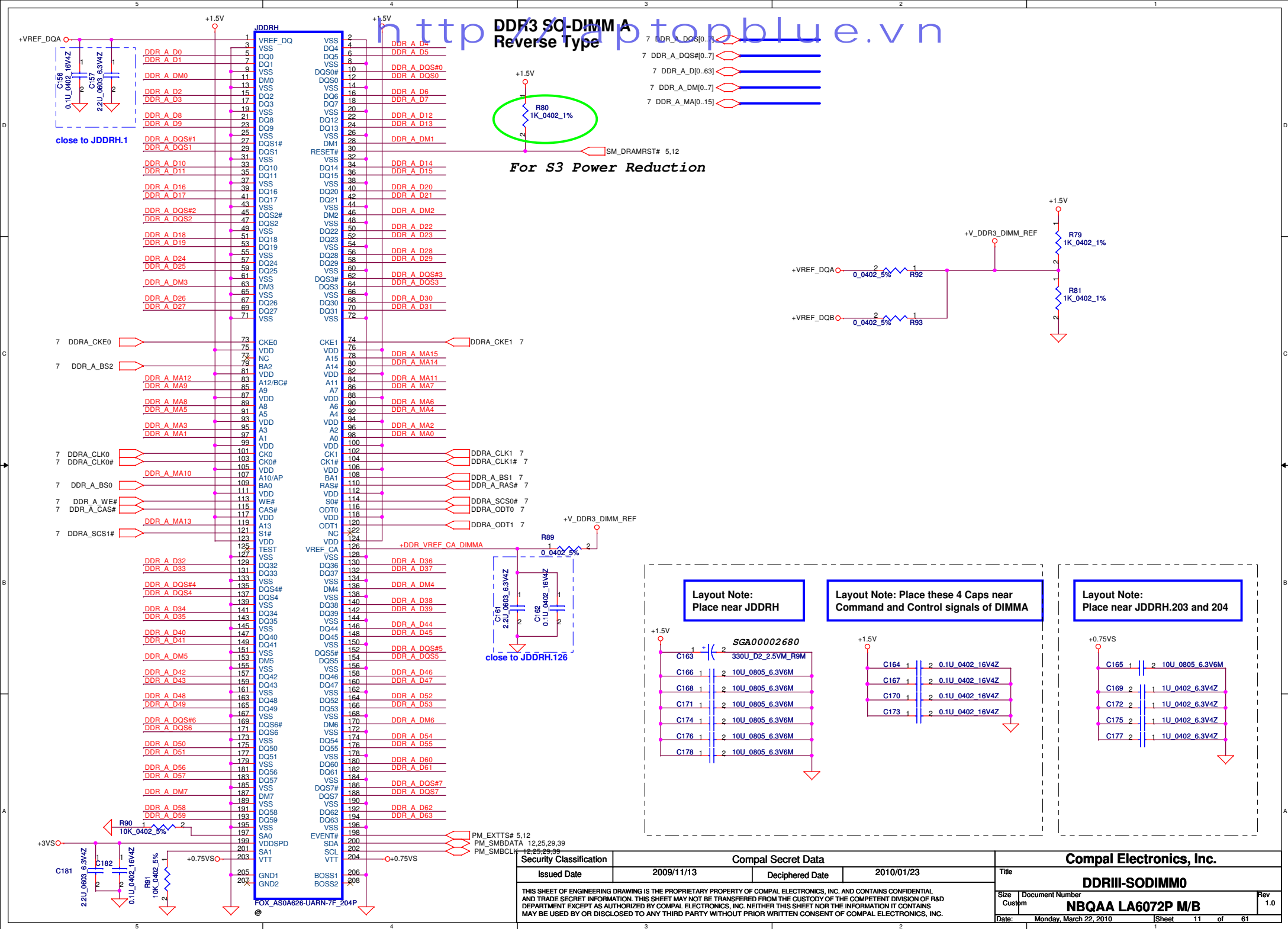


(Place these capacitors under CPU socket Edge, top layer)

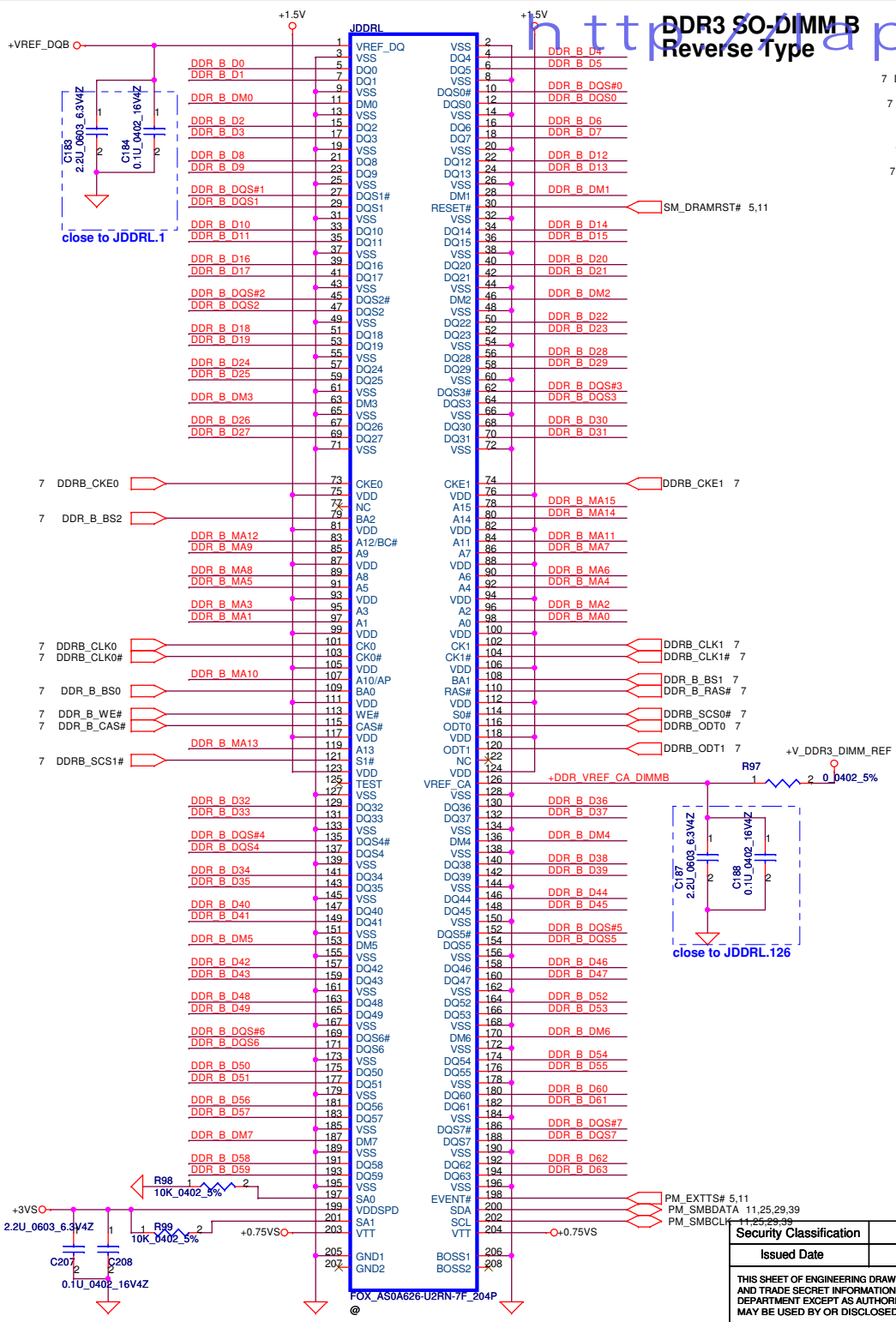
(Place these capacitors under CPU socket, top layer)

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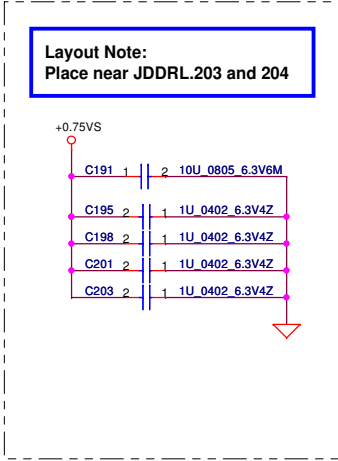
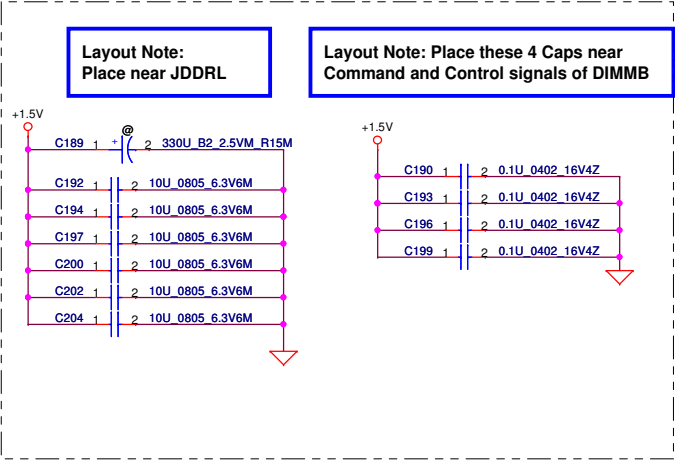
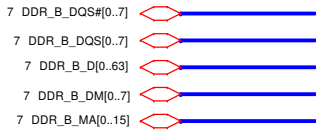


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				DDRIII-SODIMMO			
				Size	Document Number	Rev	
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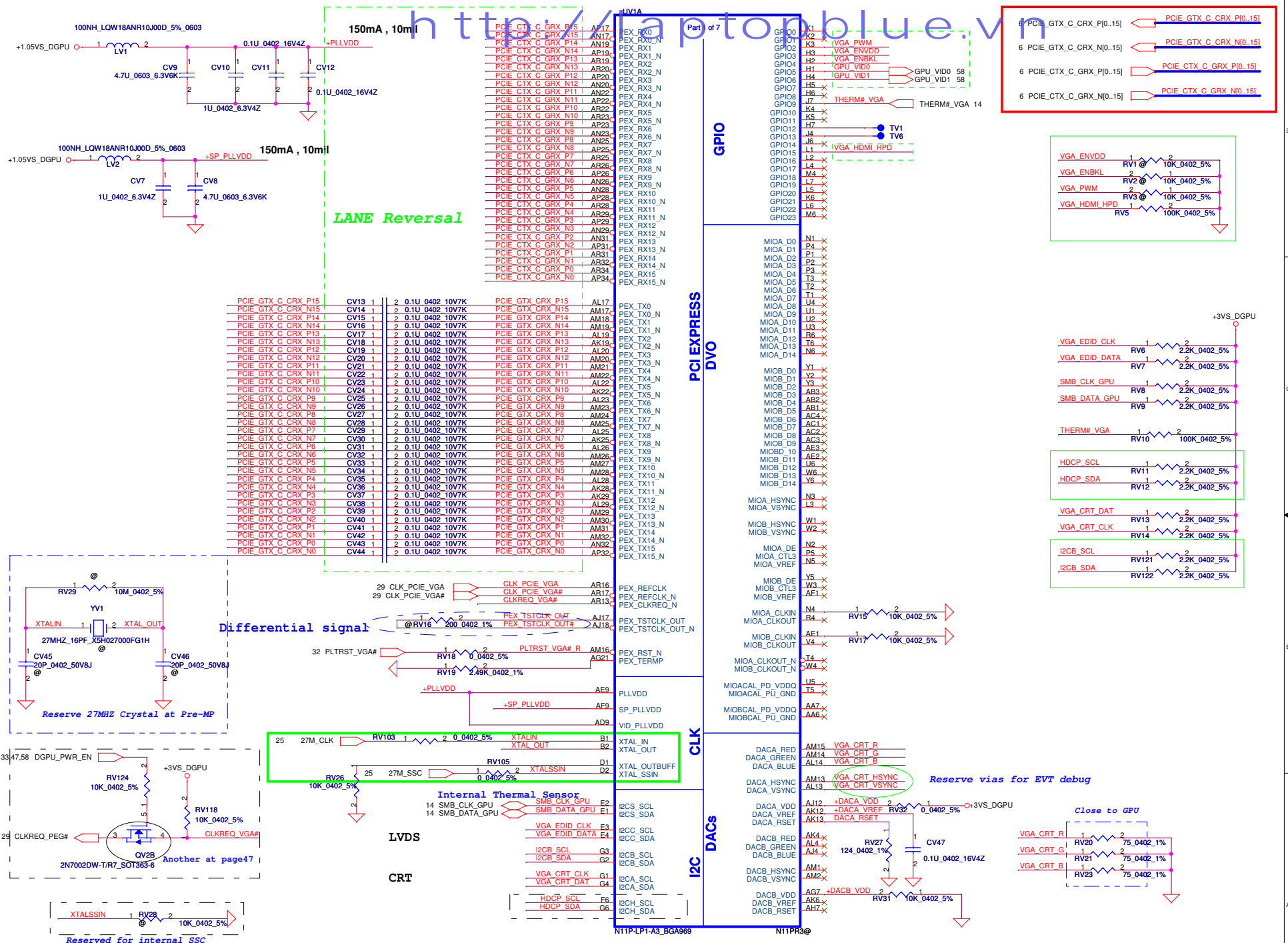


http://laptopblue.vn

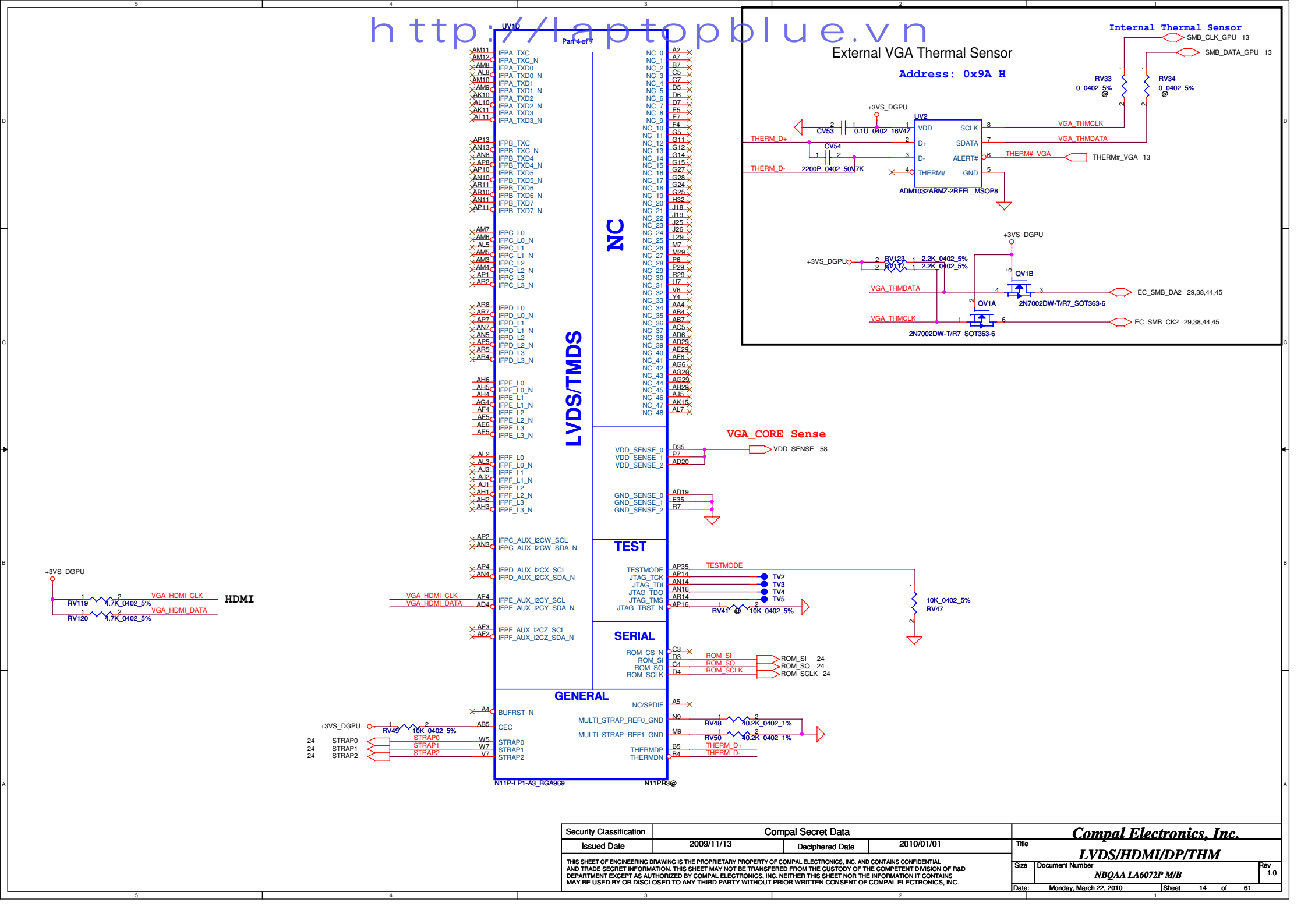
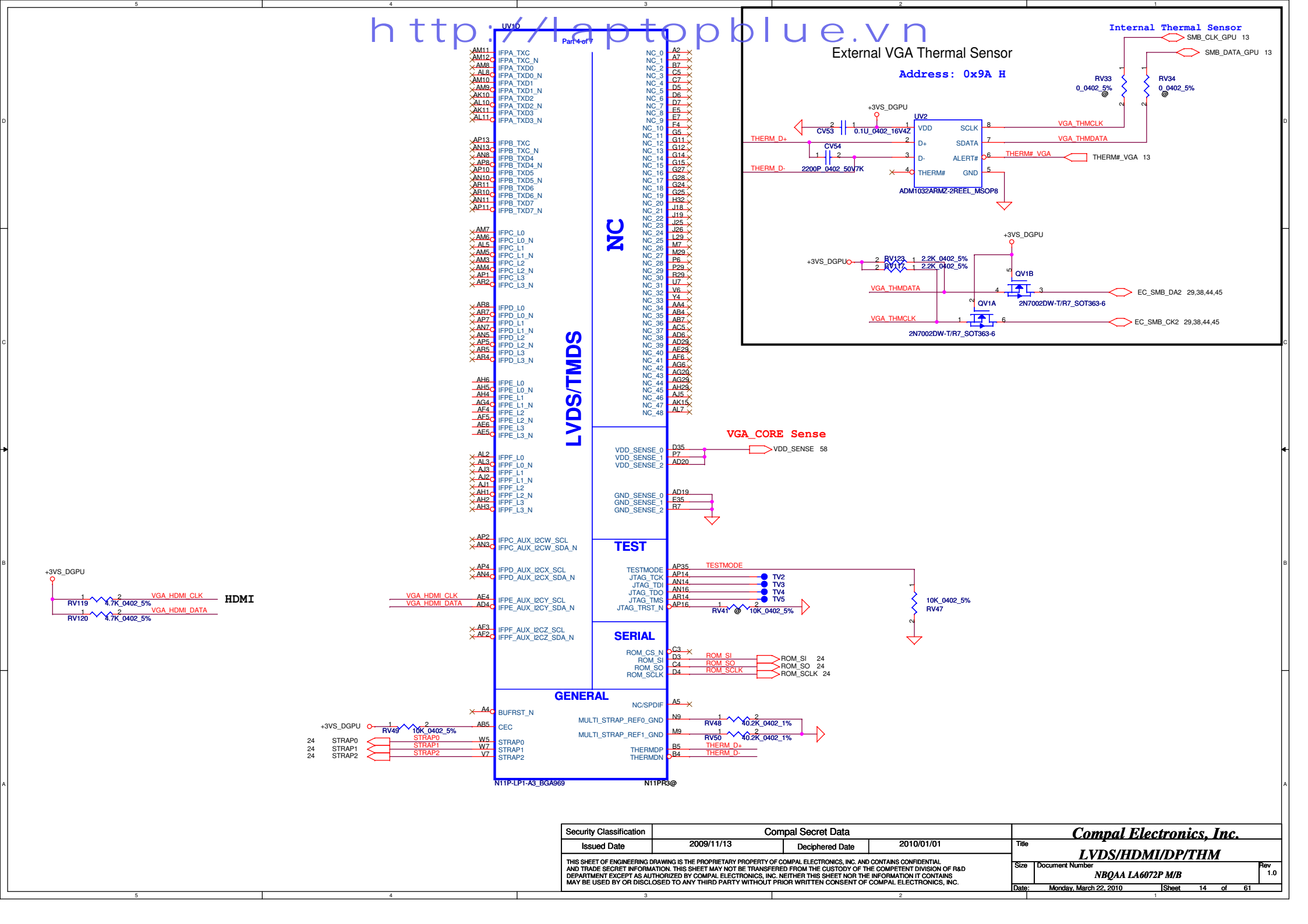
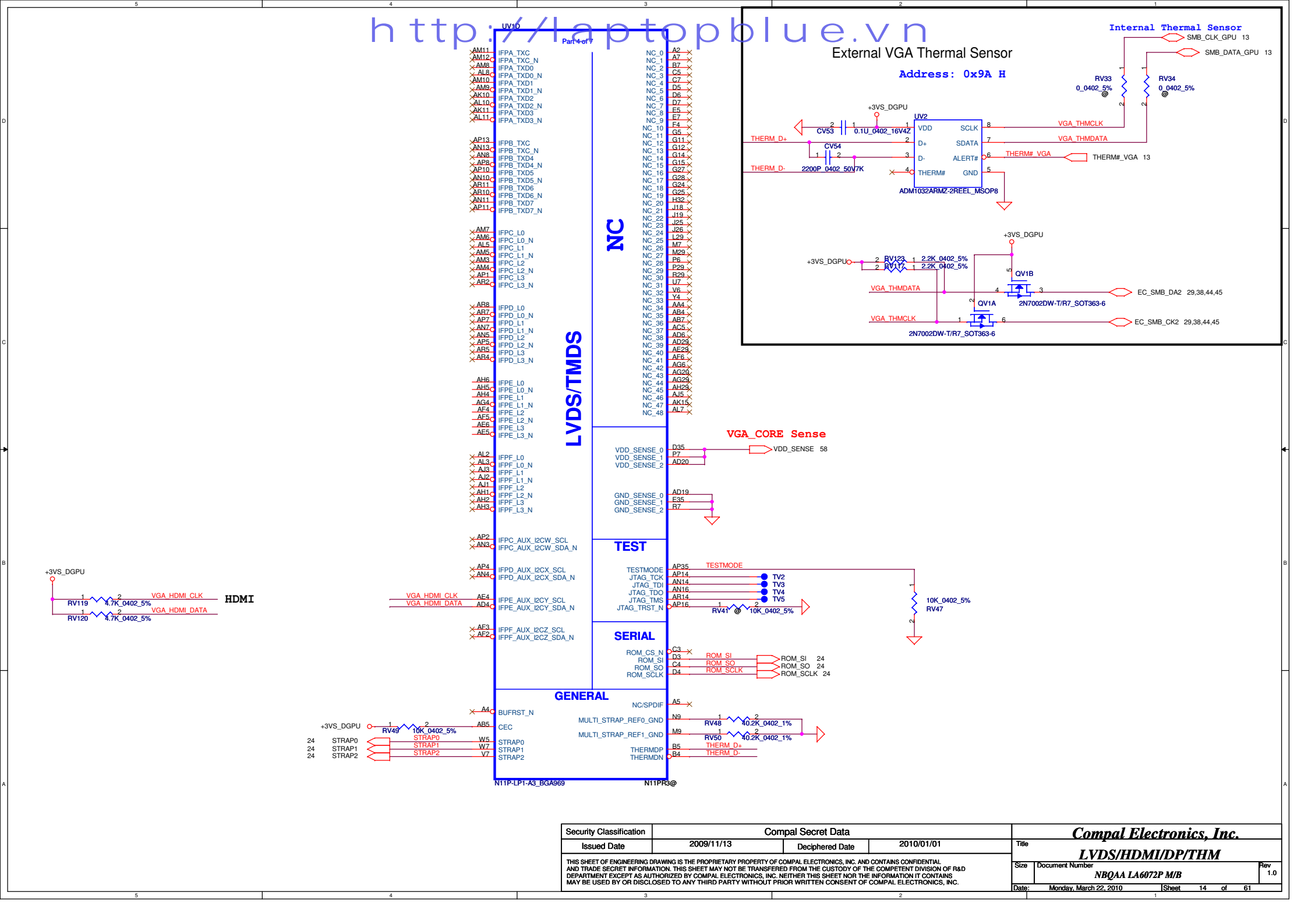
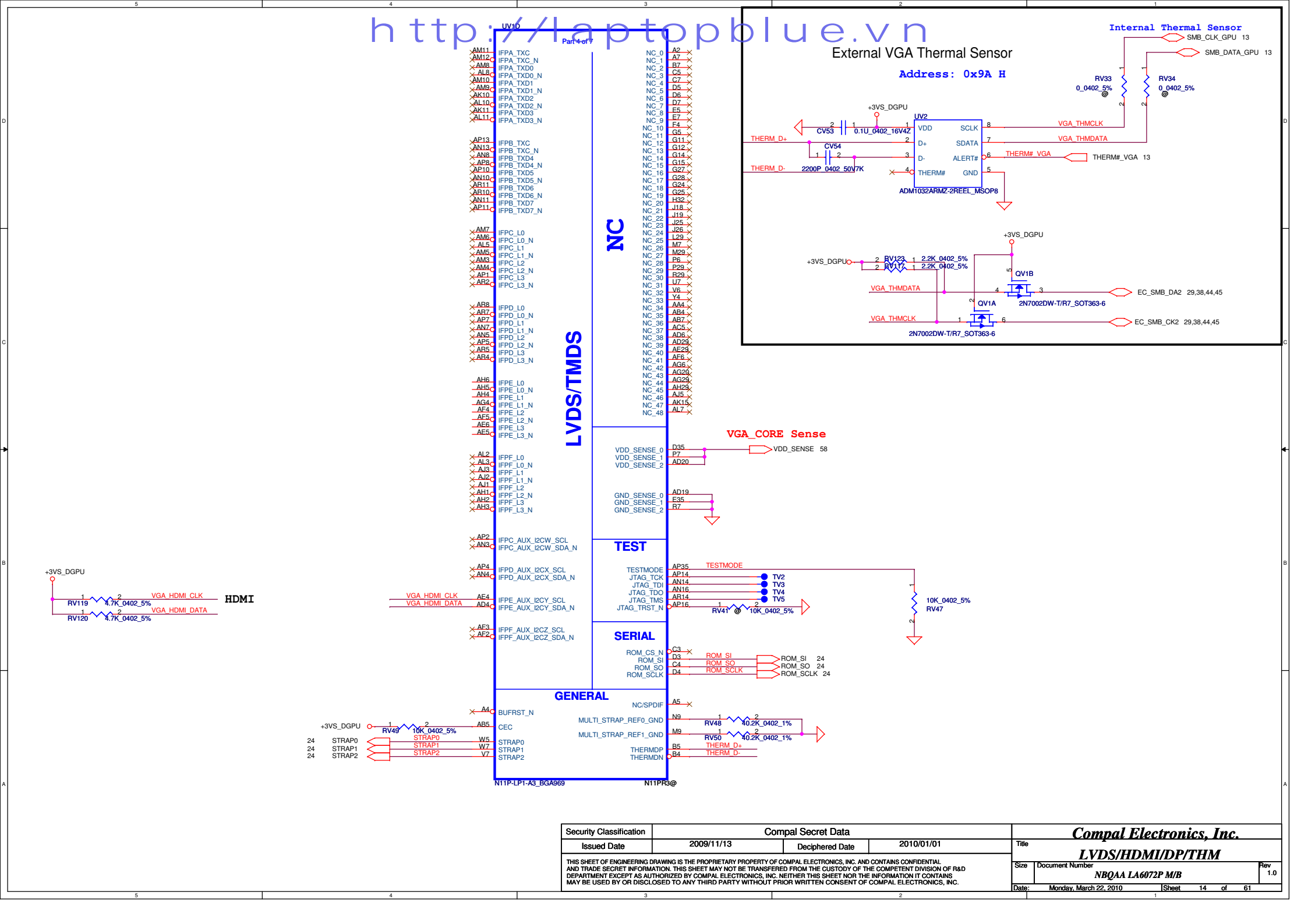
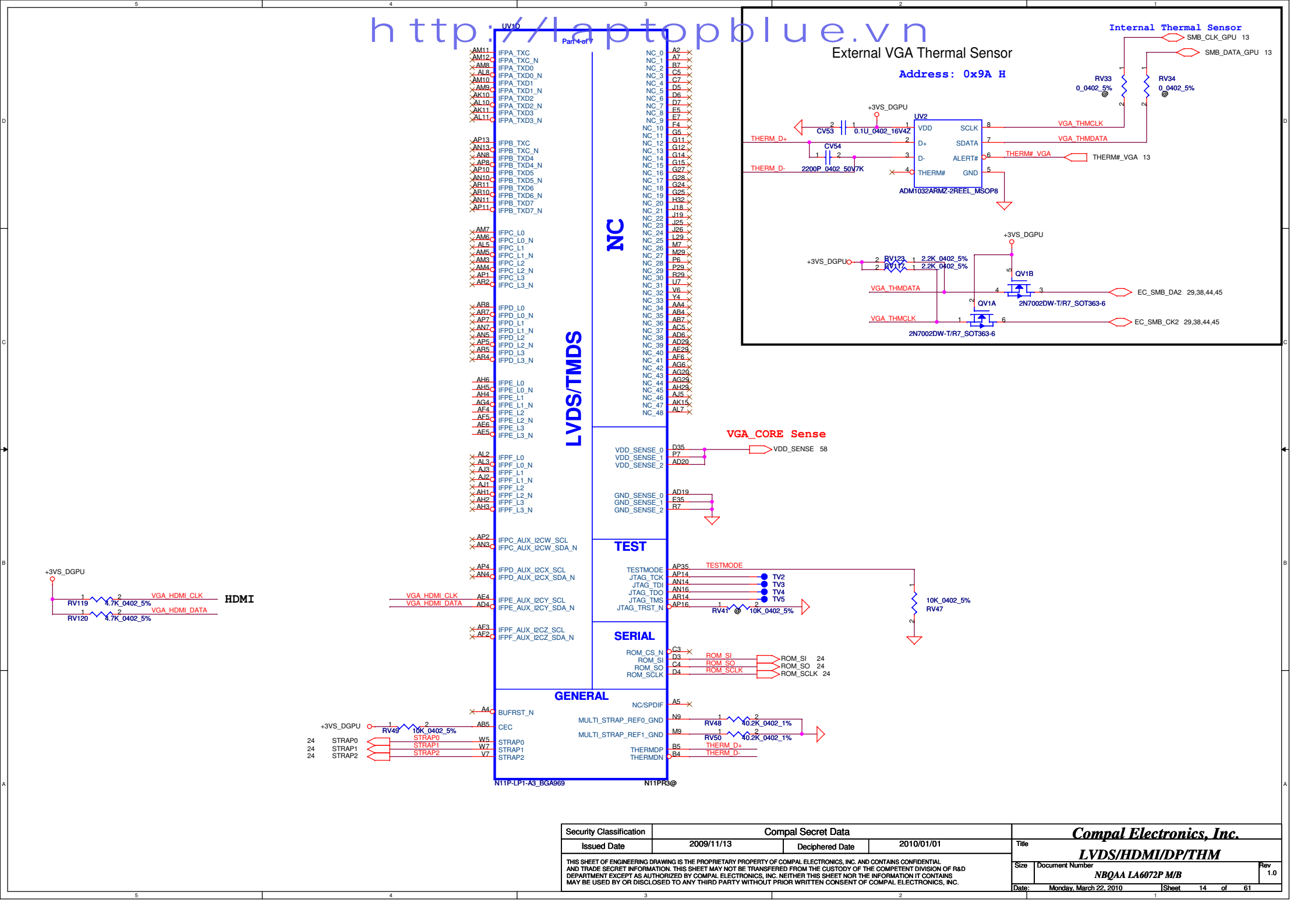
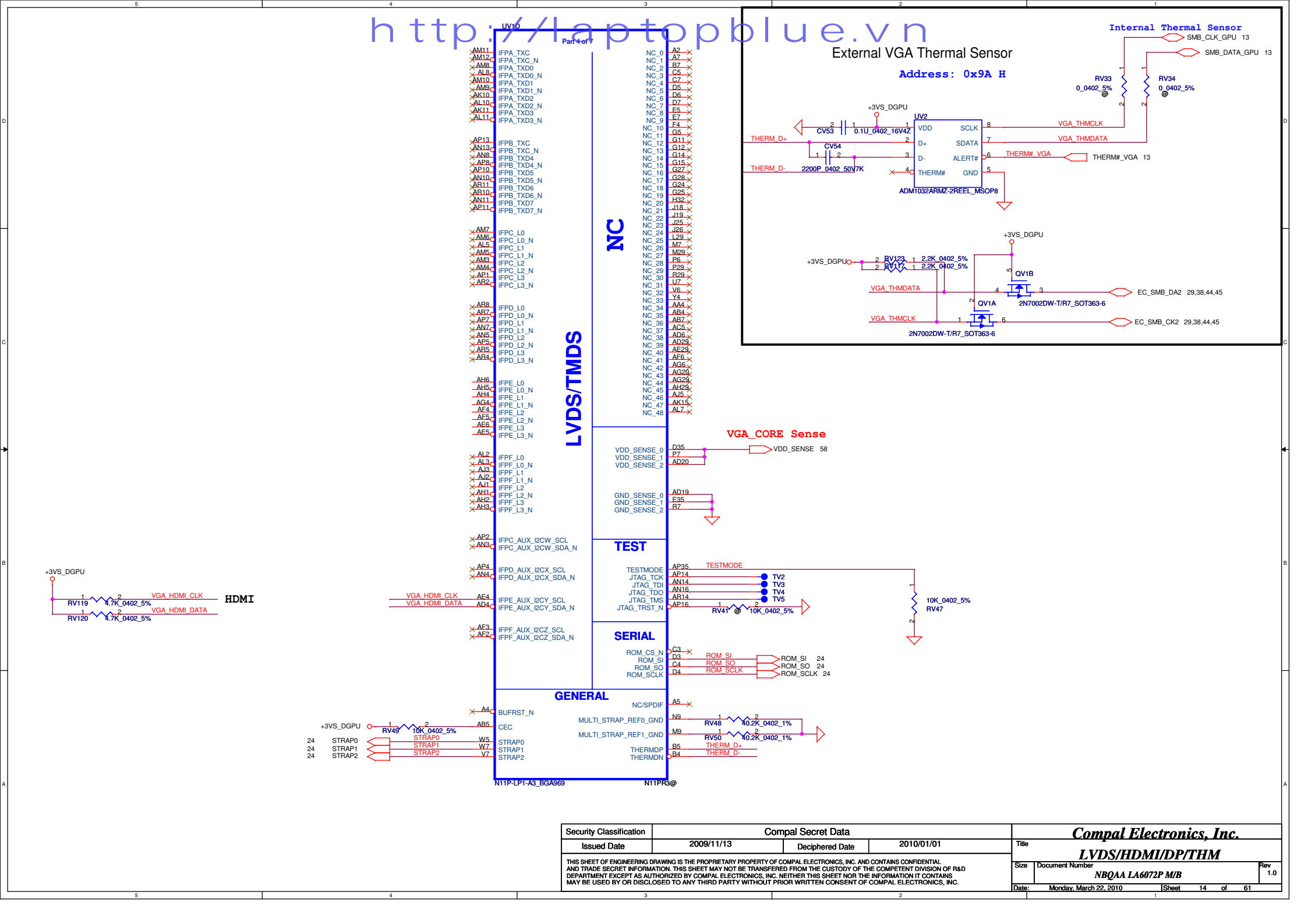
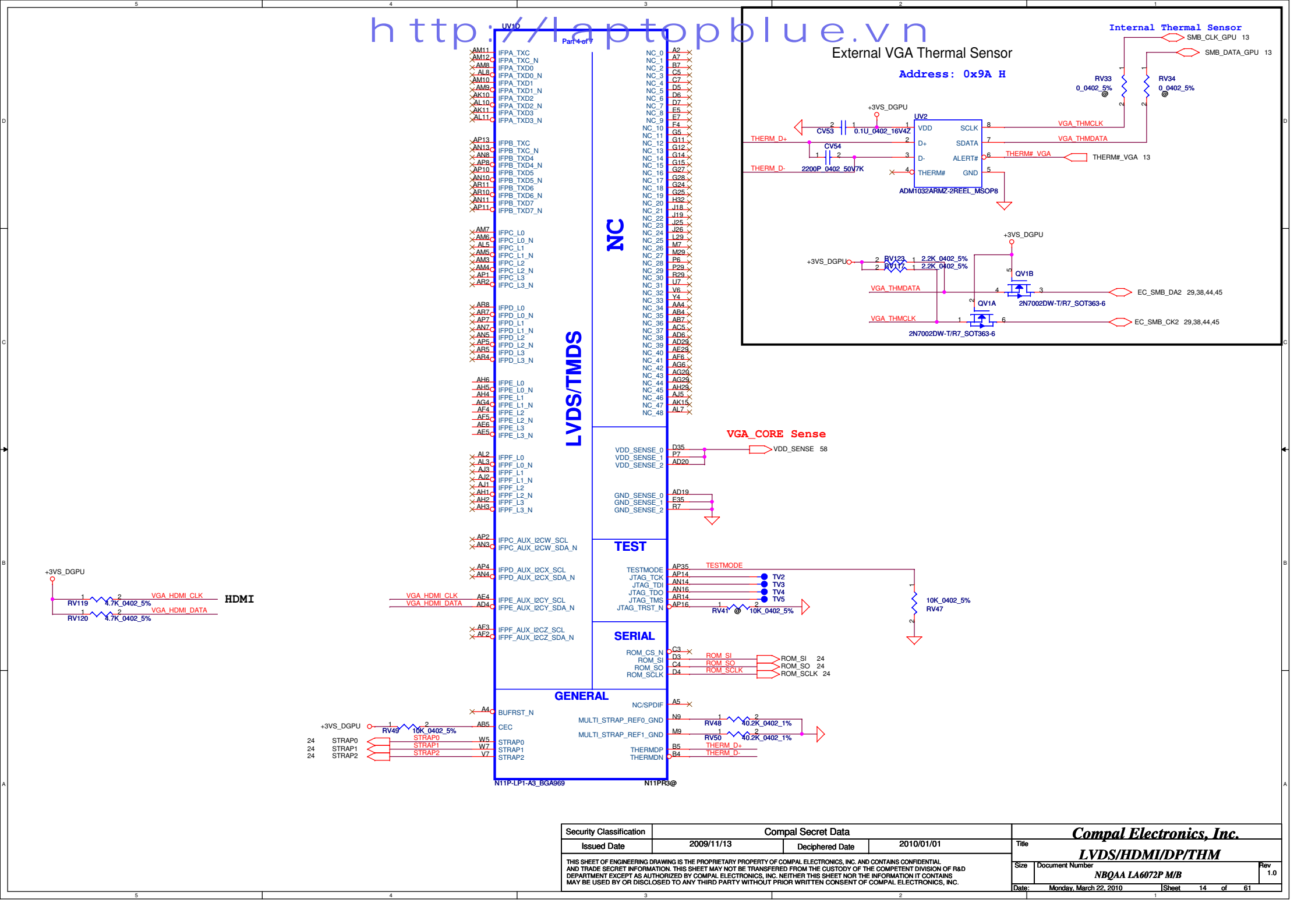
DDR3 SO-DIMM B Reverse Type



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								PCIE/DAC/GPIO			
								NBQAA LA6072P M/B			
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h t t p : // l a p t o p b l u e . v n

Part 4 of 7

External VGA Thermal Sensor

Address: 0x9A H

Internal Thermal Sensor

RV33 0.0402_5%

RV34 0.0402_5%

RV123 2.2K 0402_5%

RV124 2.2K 0402_5%

RV47 10K 0402_5%

RV48 40.2K 0402_1%

RV50 40.2K 0402_1%

RV119 4.7K 0402_5%

RV120 4.7K 0402_5%

RV49 10K 0402_5%

CV53 0.1U 0402_16V4Z

CV54 2200P 0402_50V7K

ADM1032ARMZ-3REEL_MSOP8

2N7002DW-T/R7_SOT363-6

2N7002DW-T/R7_SOT363-6

VGA_THMCLK

VGA_THMDATA

THERM#_VGA

THERM#_VGA

VGA_CORE Sense

VDD_SENSE_0

VDD_SENSE_1

VDD_SENSE_2

GND_SENSE_0

GND_SENSE_1

GND_SENSE_2

TESTMODE

JTAG_TCK

JTAG_TDI

JTAG_TDO

JTAG_TMS

JTAG_TRST_N

ROM_CS_N

ROM_SI

ROM_SO

ROM_SCLK

NC/SPDIF

BUFRST_N

CEC

MULTI_STRAP_REF0_GND

MULTI_STRAP_REF1_GND

THERMDP

THERMDN

N11P.LP1-A3_BGA969

N11PR3@

HDMI

VGA HDMI CLK

VGA HDMI DATA

LVDS/TMDS

NC

TEST

SERIAL

GENERAL

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Issued Date

2009/11/13

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2010/01/01

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Compal Electronics, Inc.

LVDS/HDMI/DP/THM

Size

Document Number

NBQAA LA6072P M/B

Rev

1.0

Date:

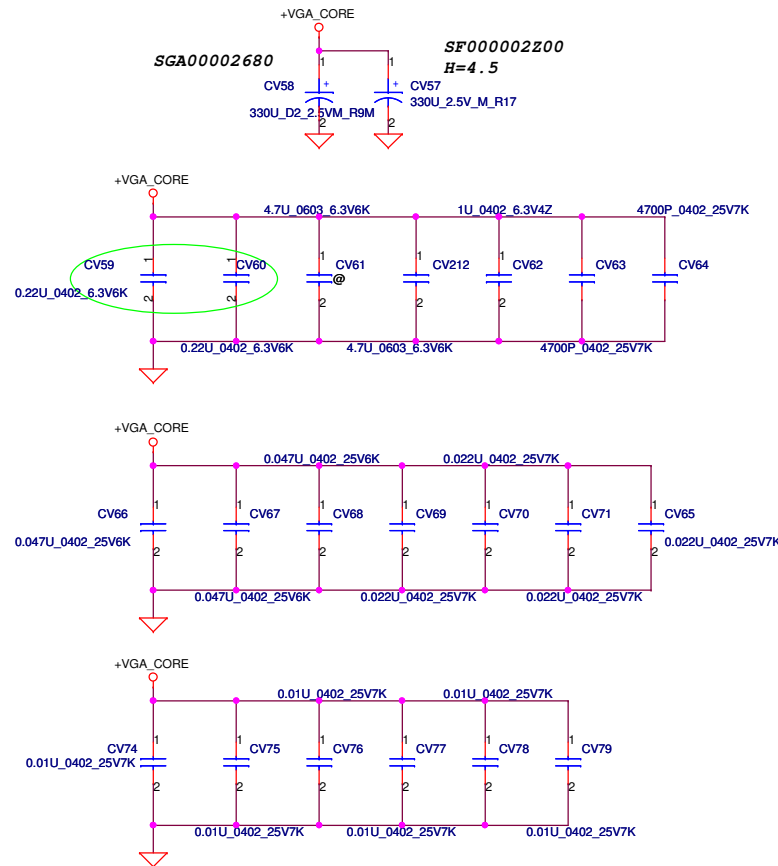
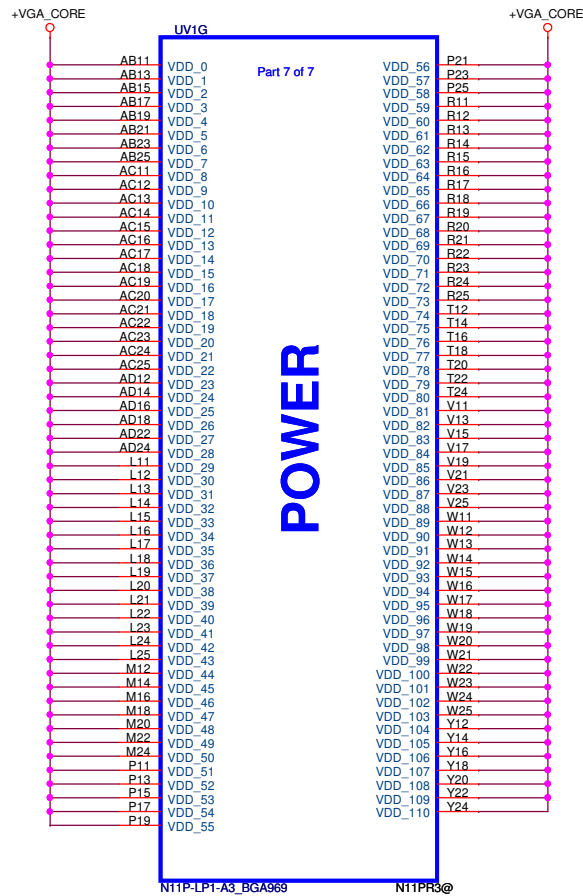
Monday, March 22, 2010

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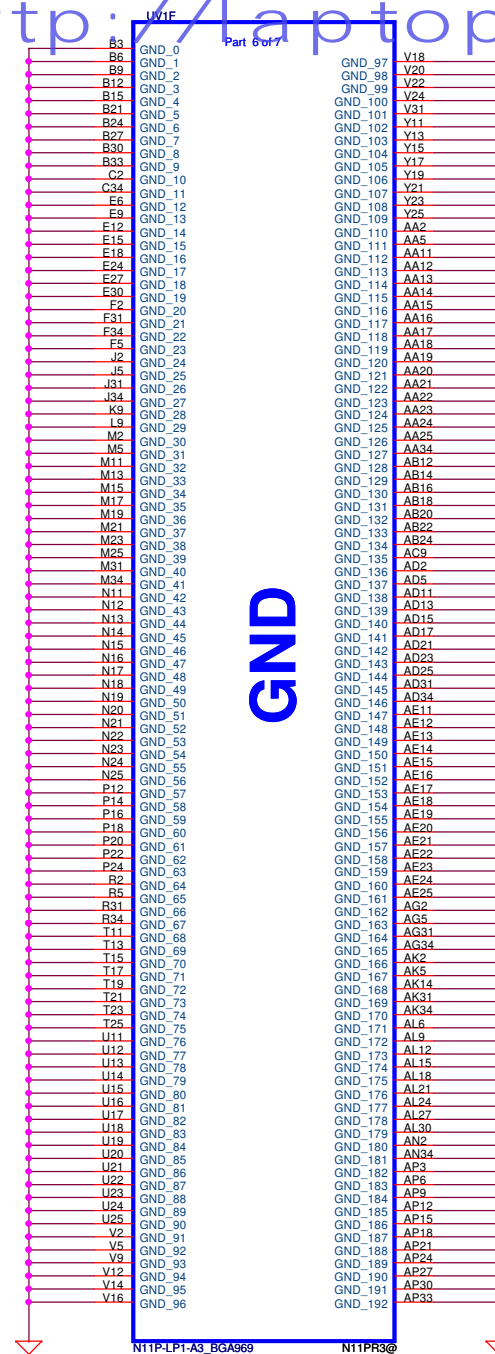
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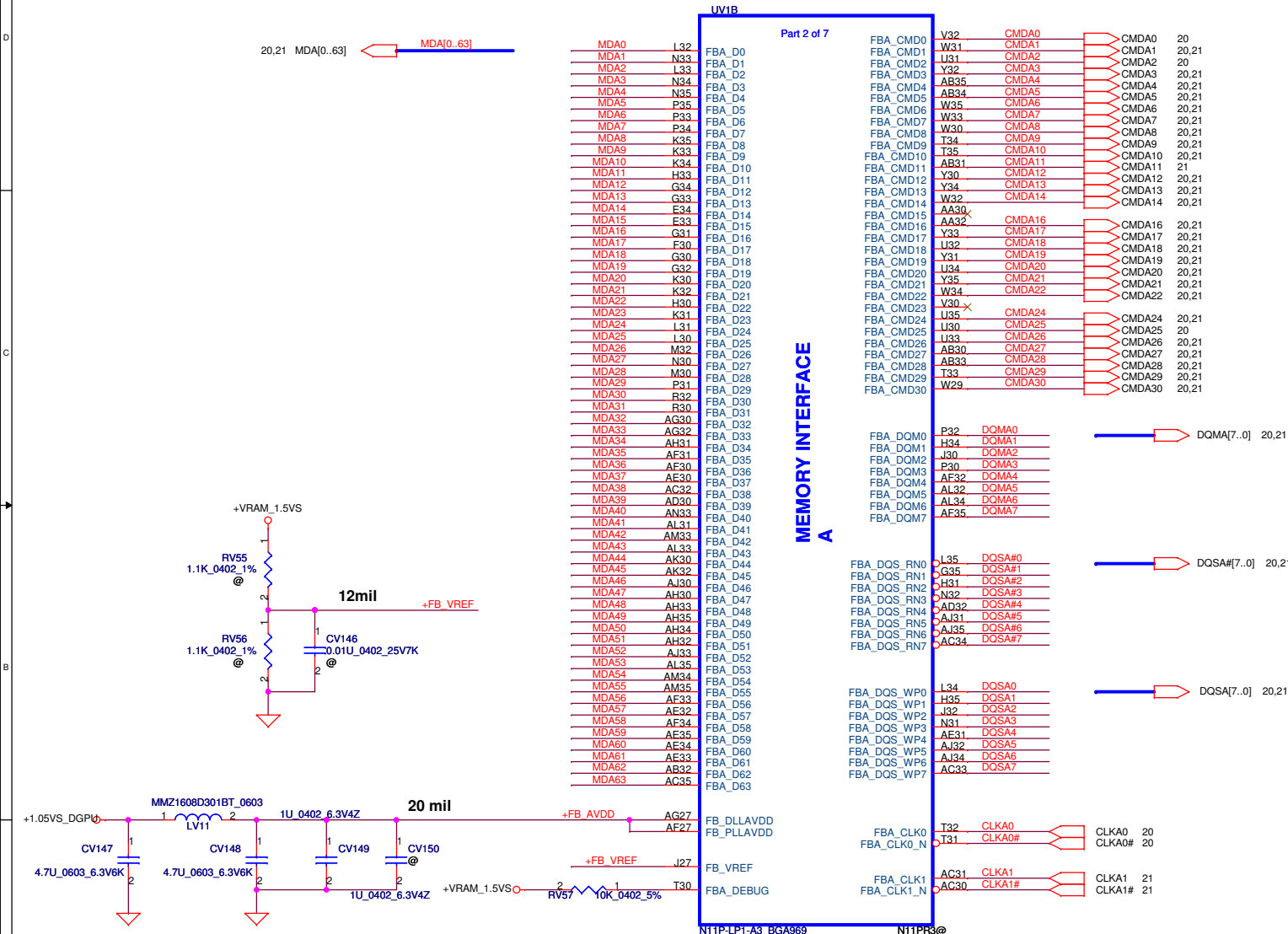
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				Size	Document Number
				NBQAA LA6072P M/B	
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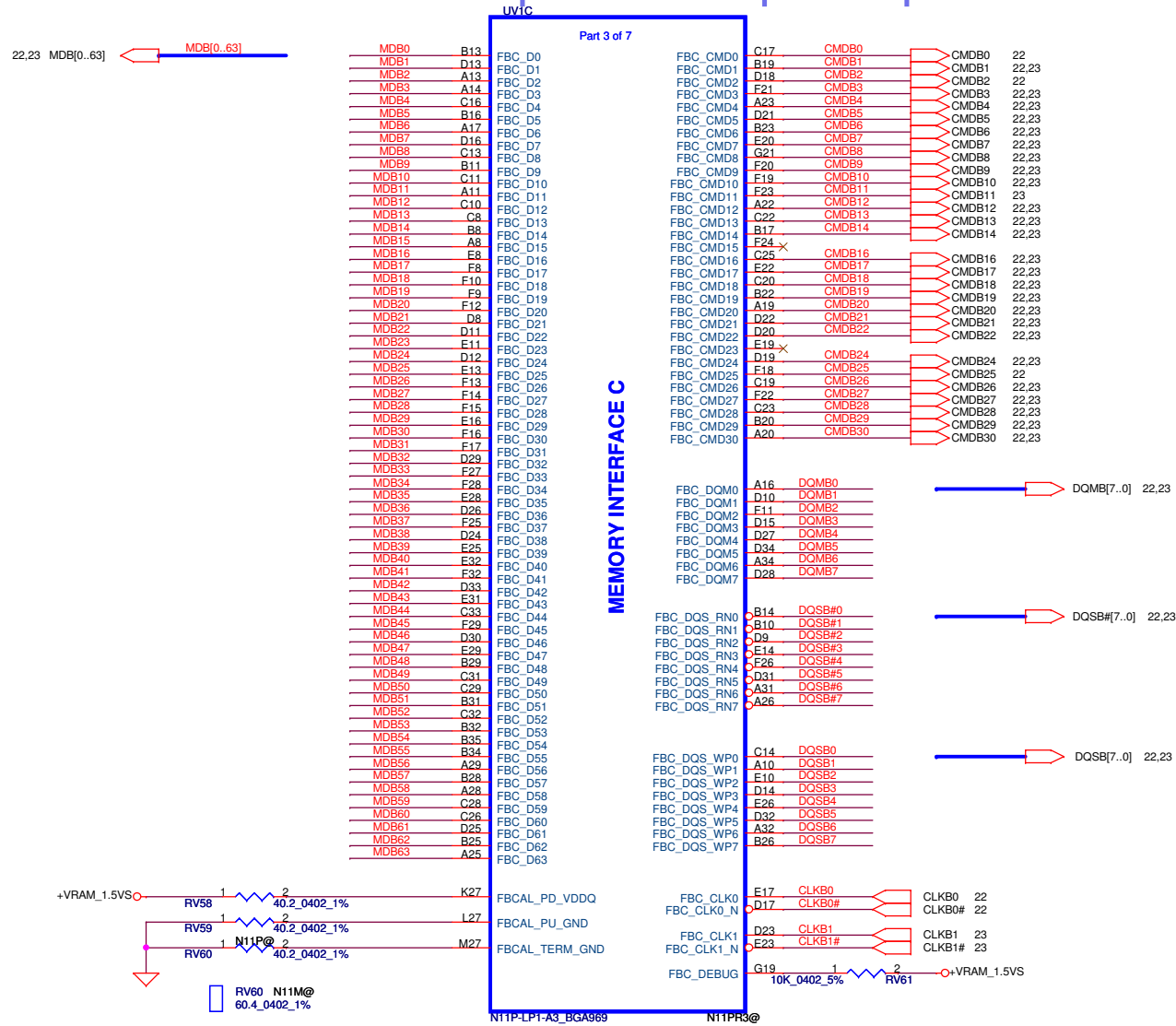
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Issued Date	2009/11/13	Deciphered Date	2010/01/01	Title GND		
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Mode C - Mirror Mode Mapping

DATA Bus		
Address	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

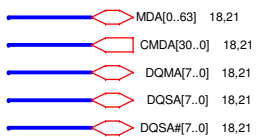
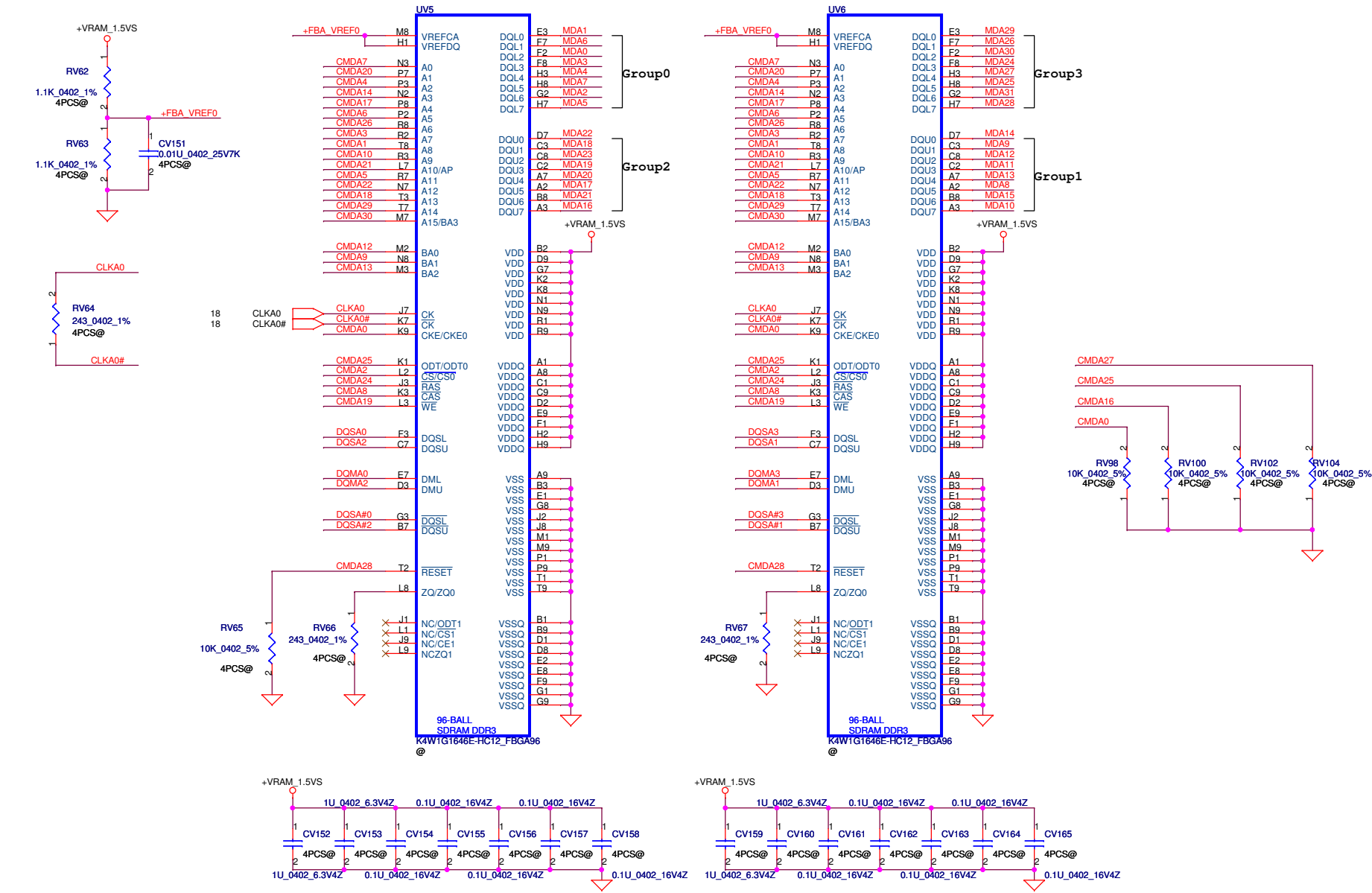
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Mode C - Mirror Mode Mapping

DATA Bus		
Address	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

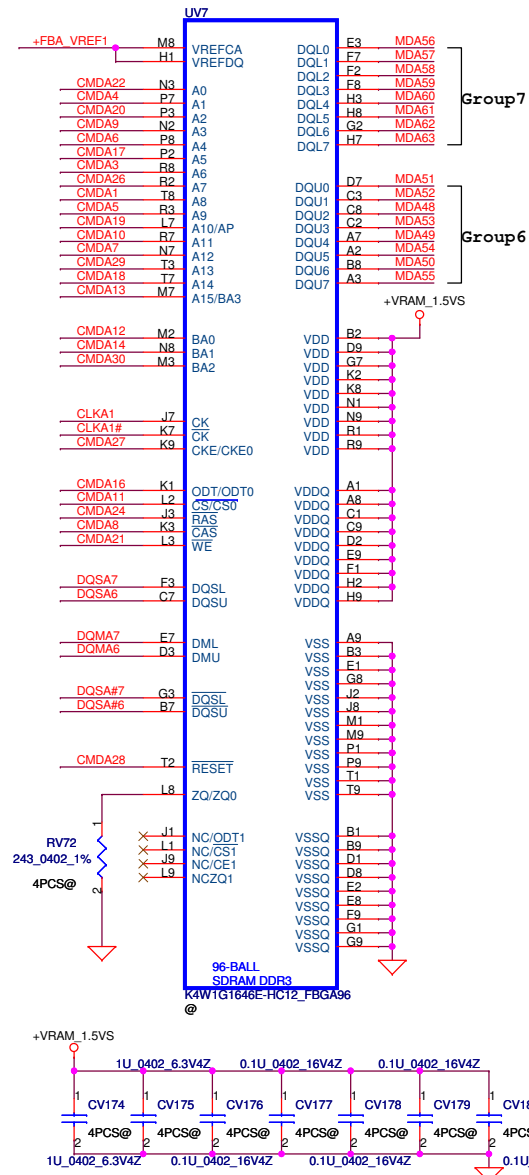
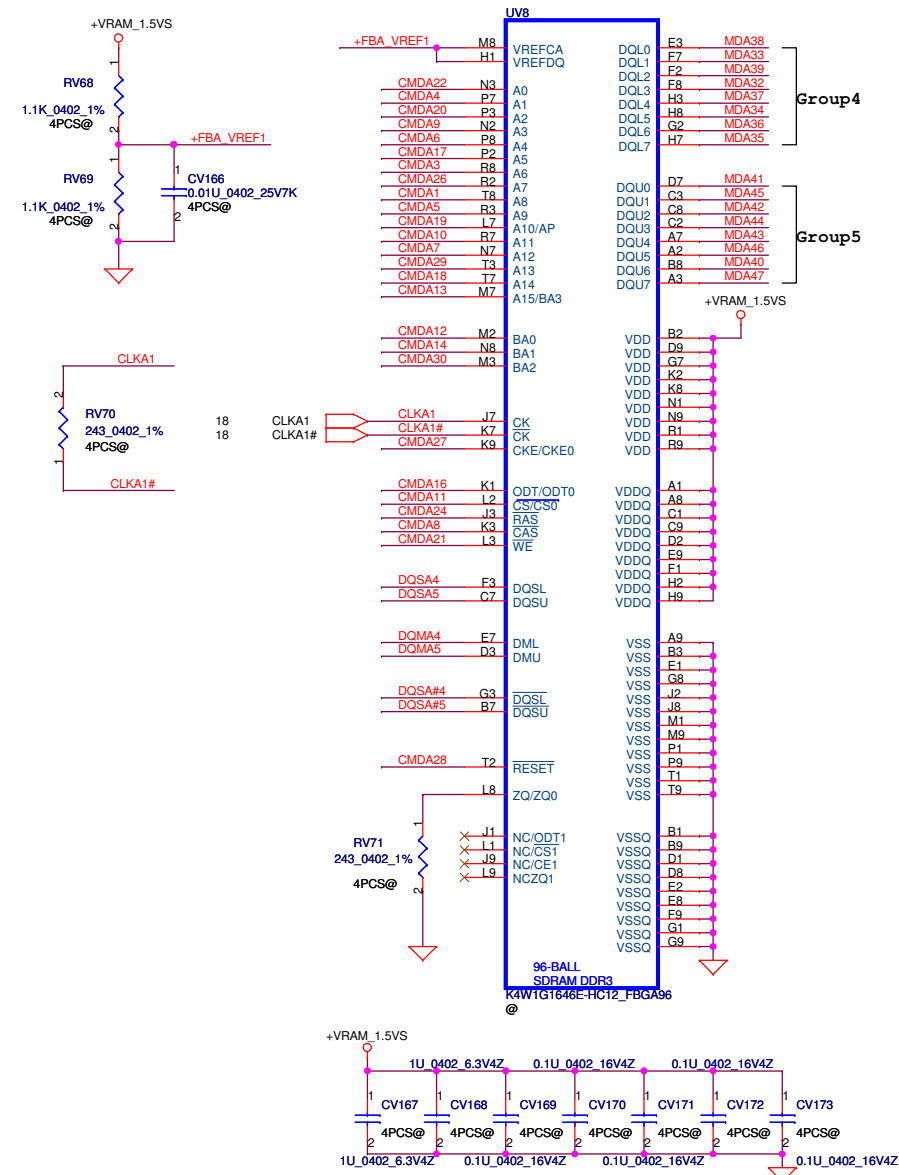
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Mode C - Mirror Mode Mapping

DATA Bus	
Address	0..31 32..63
CMD0	CKE_L
CMD1	A8
CMD2	CS0#_L
CMD3	A7
CMD4	A2
CMD5	A11
CMD6	A5
CMD7	A0
CMD8	CAS#
CMD9	BA1
CMD10	A9
CMD11	CS0#_H
CMD12	BA0
CMD13	BA2
CMD14	A3
CMD15	CS1#_H
CMD16	ODT_H
CMD17	A4
CMD18	A13
CMD19	WE#
CMD20	A1
CMD21	A10
CMD22	A12
CMD23	CS1#_L
CMD24	RAS#
CMD25	ODT_L
CMD26	A6
CMD27	CKE_H
CMD28	RST
CMD29	A14
CMD30	A15

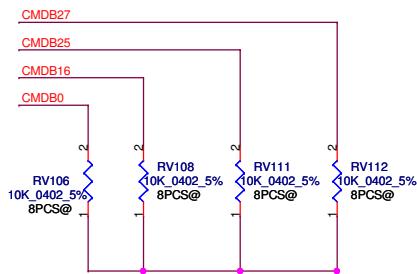
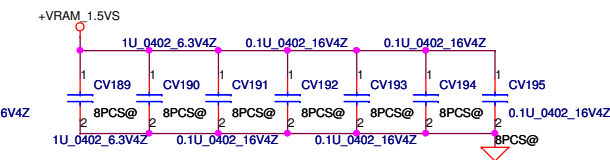
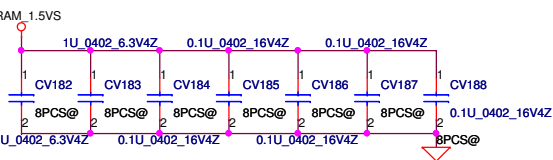
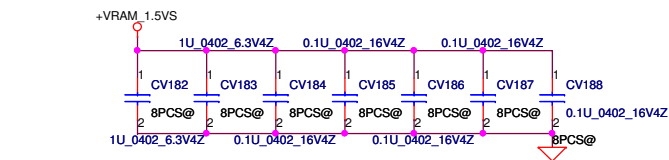
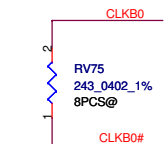
Memory Partition A - Upper 32:bits



Mode C - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

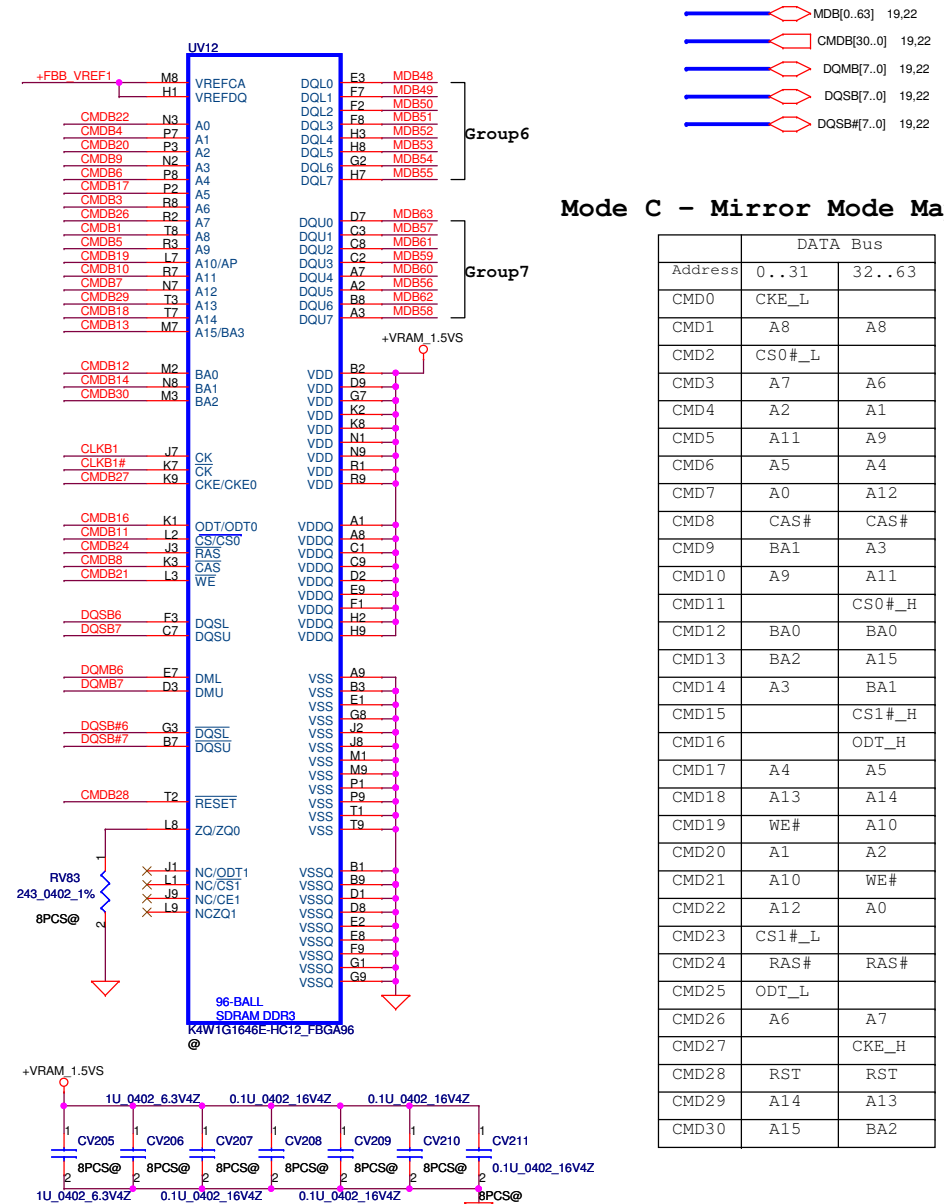
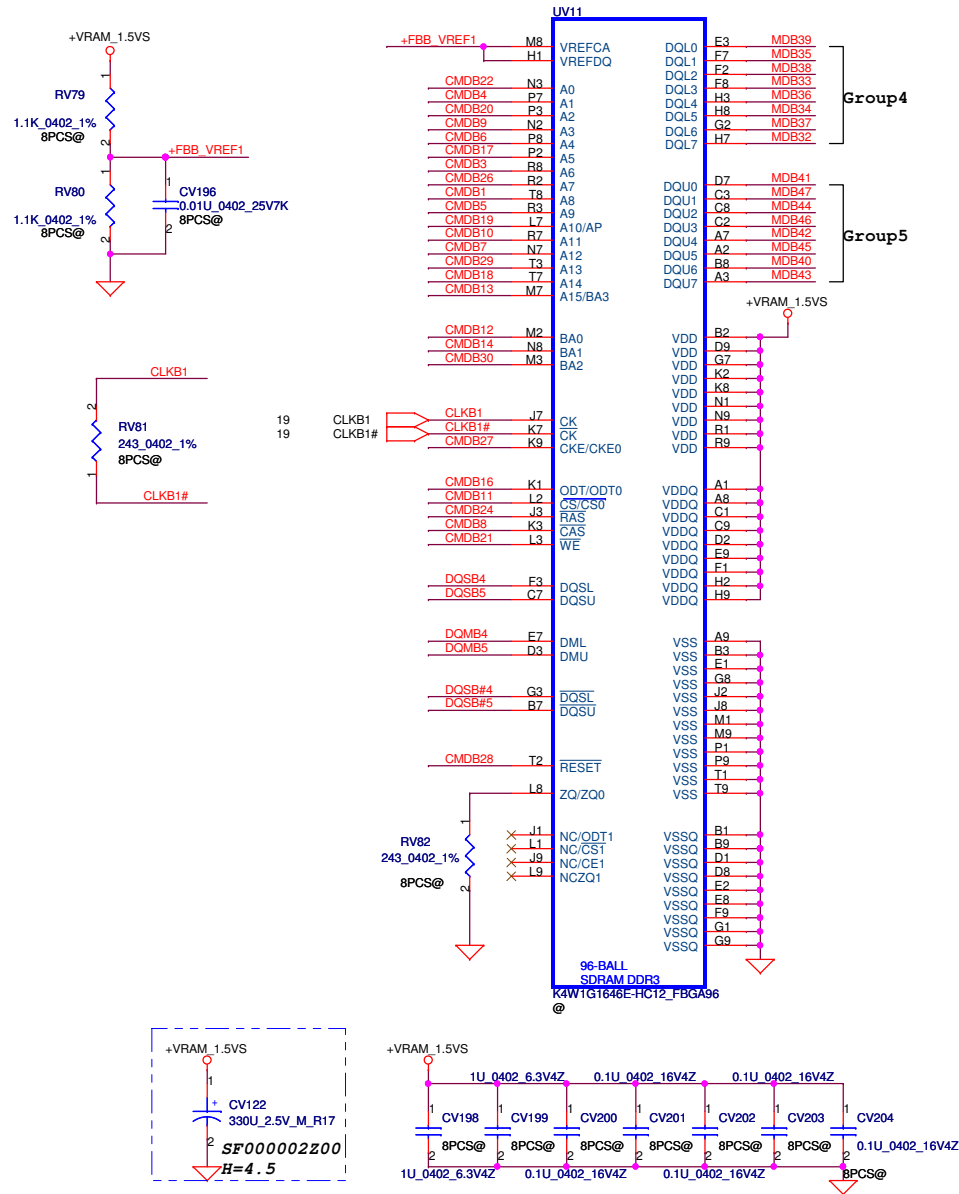
Lower 32 bits



	DATA Bus	
Address	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

	DATA Bus	
Address	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

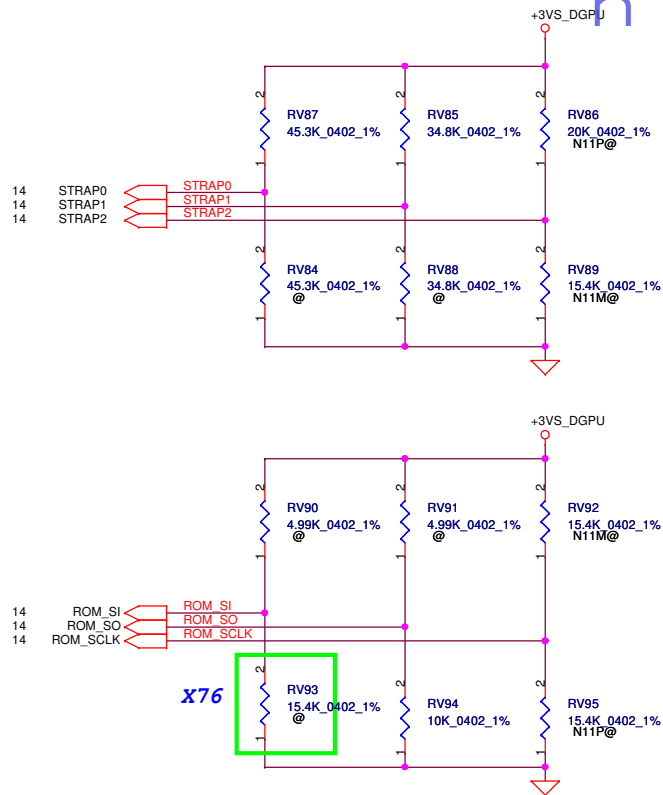
Memory Partition C - Upper 32 bits



Mode C - Mirror Mode Mapping

DATA Bus		
Address	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

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Device ID straps

	DeviceID	PCI_DEVID[4..0]	ROM_SCLK	STRAP2
N11P-LP1	0xA2B	[01011]	Pull down 15K	Pull up 20K
N11M-GE1	0xA75	[10101]	Pull up 15K	Pull down 30K
N11M-OP1	0xA72	[10010]	Pull up 15K	Pull down 15K

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

	VRAM		RAMCFG[3..0] RV93		
DDR3	Hynix H5TQ1G63BFR-12C SA000032400	512MB	0010	PD 15K	SD034154280
		1GB	0010	PD 15K	SD034154280
64M16	Samsung K4W1G1646E-HC12 SA000035700	512MB	0011	PD 20K	SD034200280
		1GB	0011	PD 20K	SD034200280
DDR3	Reserved for 128M16				

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	VDD33	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	VDD33	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLEN_TERM
ROM_SI	VDD33	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	VDD33	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	VDD33	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	VDD33	USER[3]	USER[2]	USER[1]	USER[0]

SUB_VENDOR		XCLK_417	
0	No VBIOS ROM (Default)	0	277MHz (Default)
1	BIOS ROM is present	1	Reserved

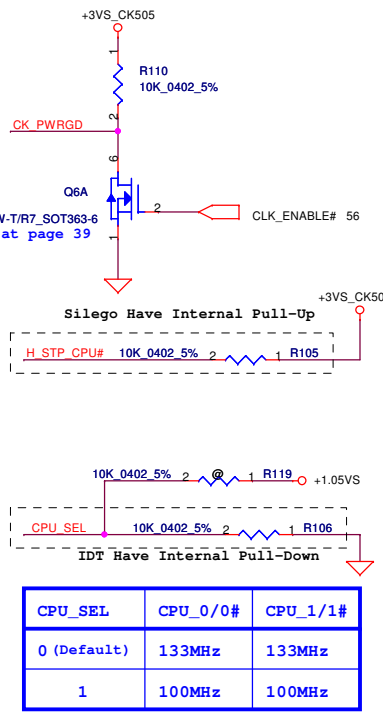
FB_0_BAR_SIZE		USER Straps	
0	256MB (Default)	User [3:0]	1110=EDID
1	Reserved	1000-1100	Customer defined

3GIO_PADCFG		PEX_PLL_EN_TERM	
3GIO_PADCFG[3:0]		0	Disable (Default)
1110	Notebook Default	1	Enable

SLOT_CLOCK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

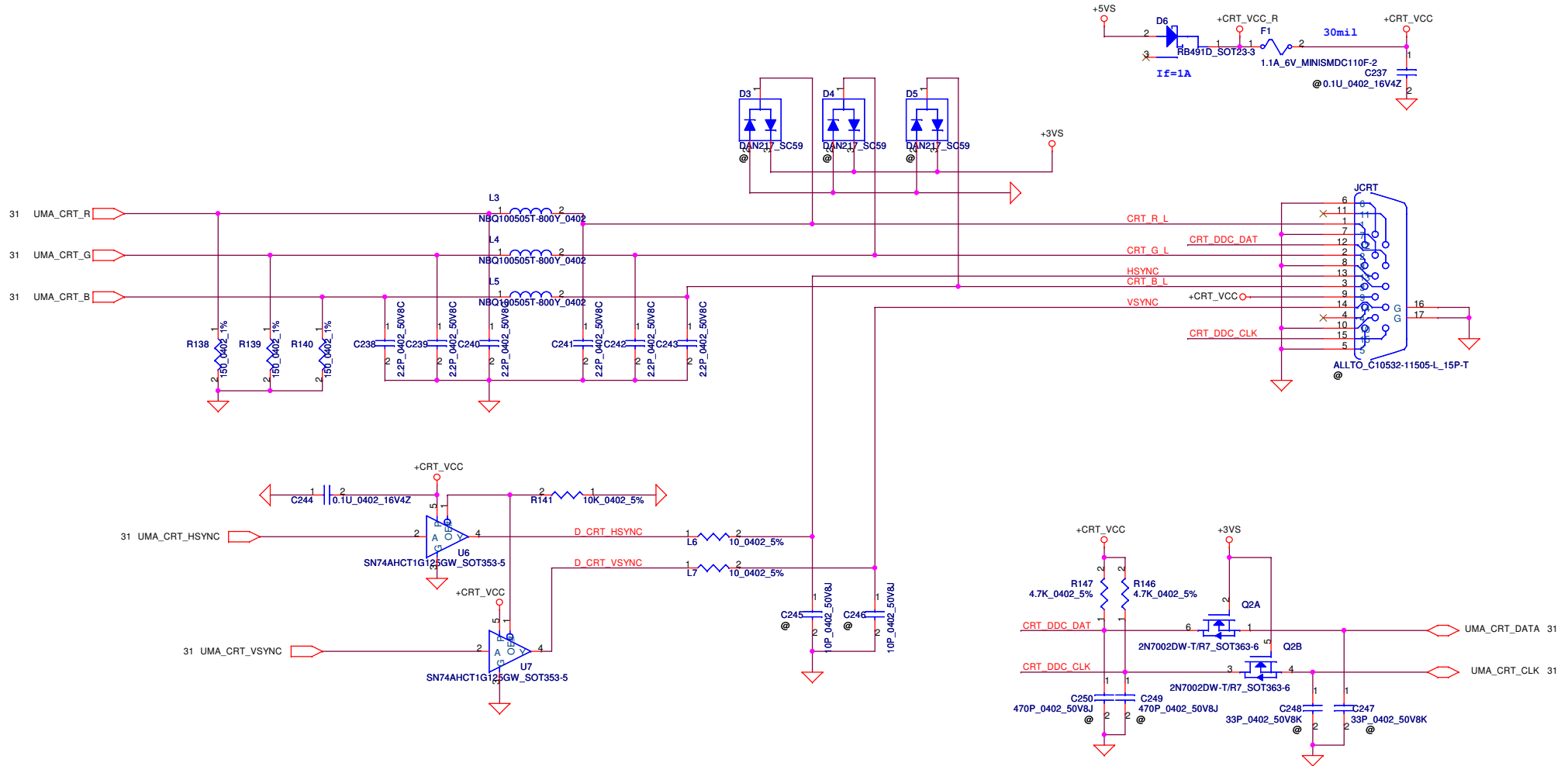
SMBUS_ALT_ADDR		VGA_DEVICE	
0	0x9E (Default)	0	3D Device
1	0x9C (Multi-GPU usage)	1	VGA Device (Default)

For SED

[illegible]

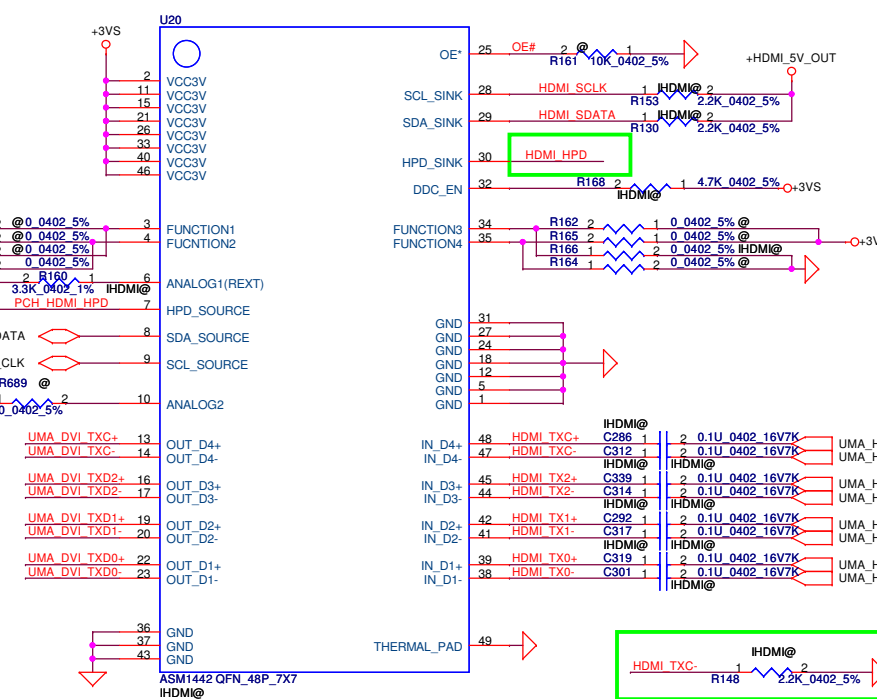
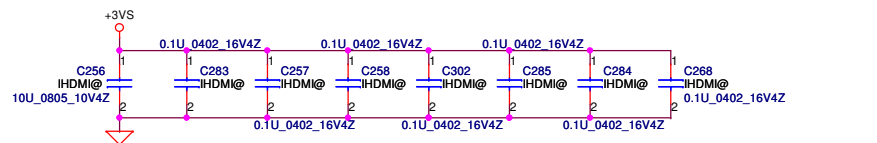
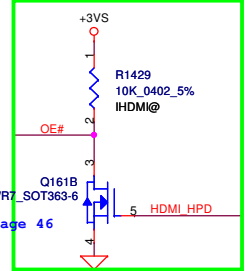
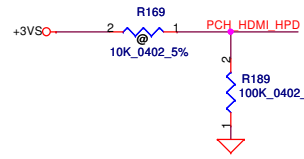
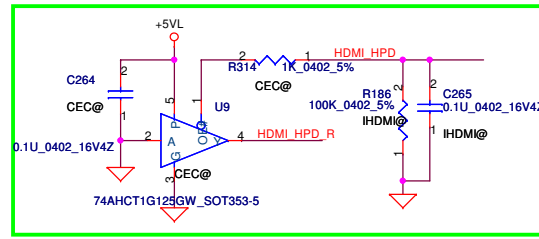
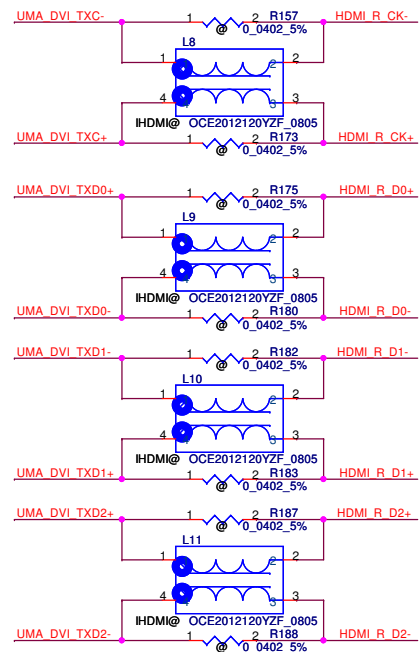
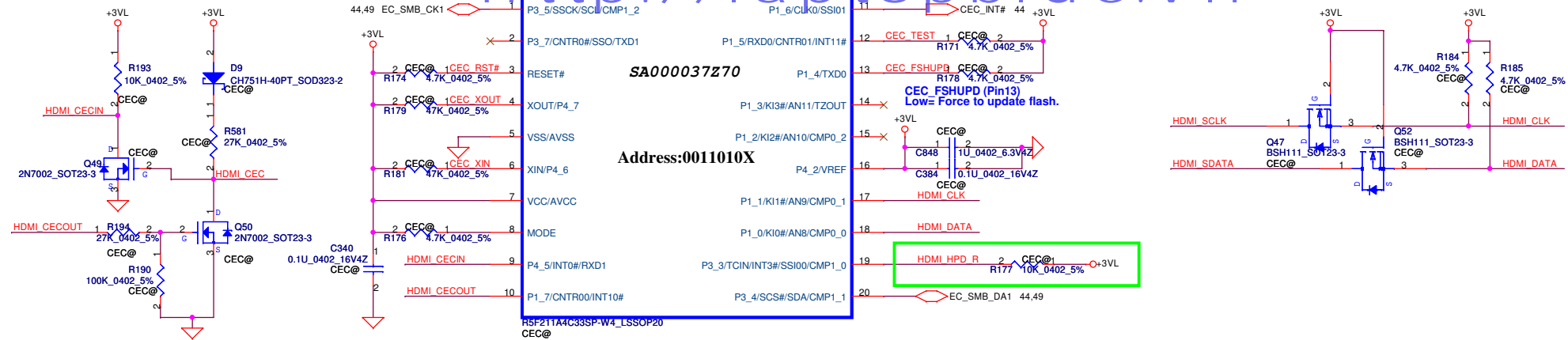
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CRT CONNECTOR

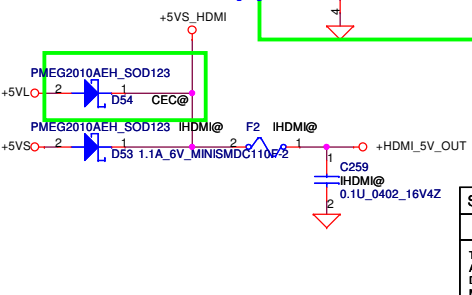
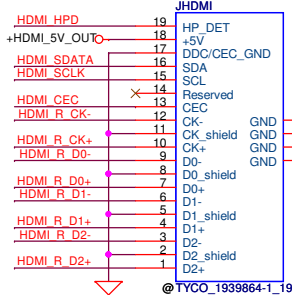


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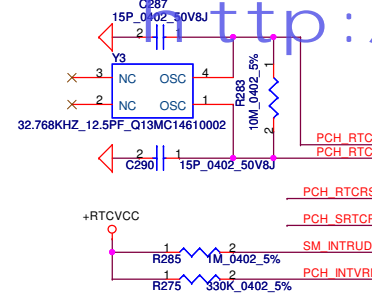
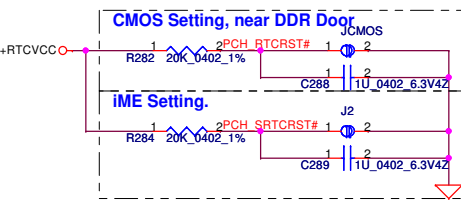
HDMI CEC Controller



HDMI Connector



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2009/11/13				2010/01/23				HDMI Connector			
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Integrated SUS 1.05V VRM Enable

PCH_INTVRMEN	High - Enable Internal VRs (must be always pulled high)
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HDA_SYNC

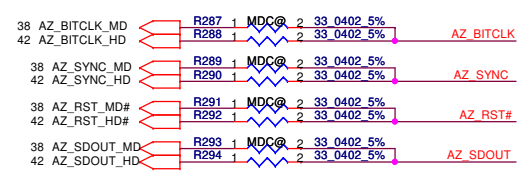
This signal has a weak internal pull down.
H=>On Die PLL is supplied by 1.5V
L=>On Die PLL is supplied by 1.8V

HDA_SDO

This signal has a weak internal pull down.
This signal can't PU

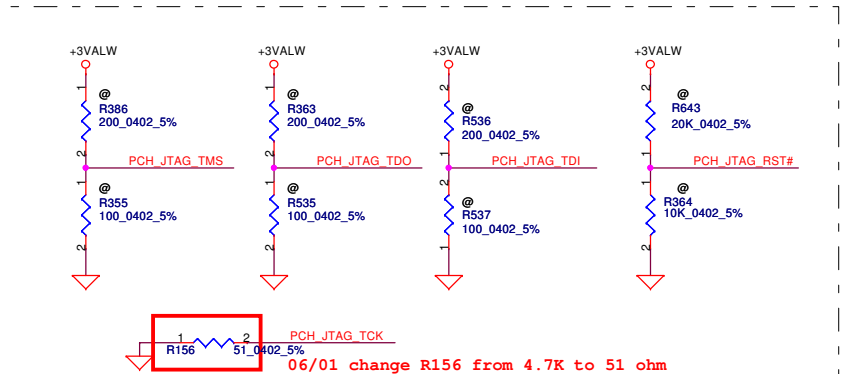
Flash Descriptor Security Override

HDA_DOCK_EN#	Low = Enabled High = Disabled *
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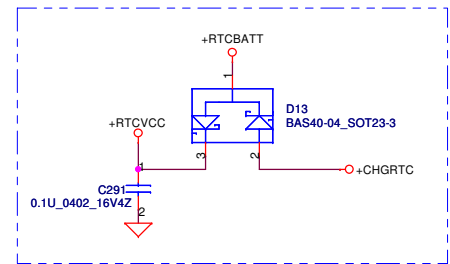
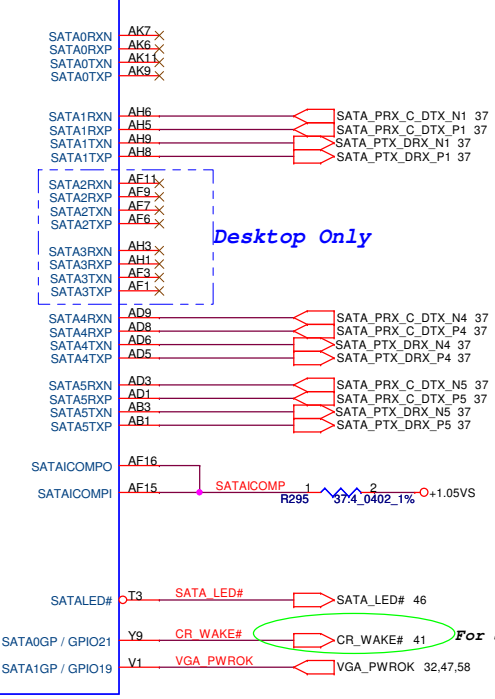
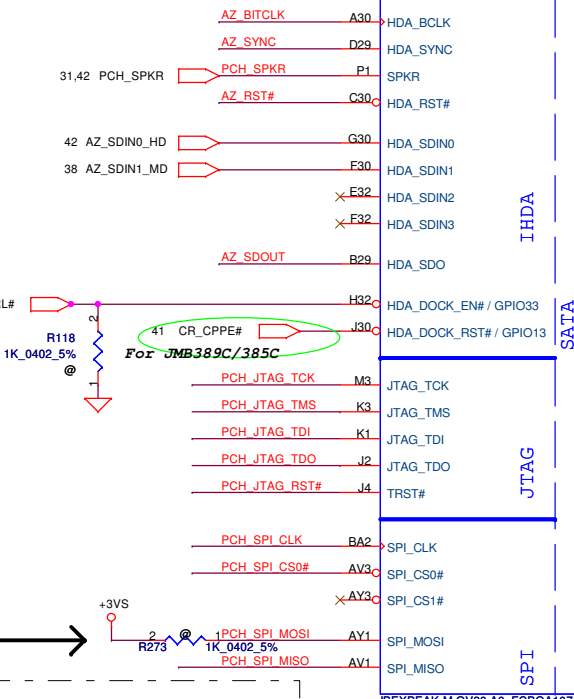
ITPM Enabled Internal: Pull down 20k

SPI_MOSI	High = Enabled Low = Disabled (Default)
----------	--



PCH Pin	RefDes	PCH JTAG Enable		PCH JTAG Disable (Default)	
		ES1	ES2	ES1	ES2
PCH_JTAG_TDO	R358	No Install	200ohm	No Install	No Install
PCH_JTAG_TMS	R355	No Install	100ohm	No Install	No Install
PCH_JTAG_TDI	R354	100ohm	100ohm	No Install	No Install
PCH_JTAG_TCK	R356	200ohm	200ohm	20kohm	No Install
PCH_JTAG_RST#	R537	100ohm	100ohm	10kohm	No Install
PCH_JTAG_TCK	R156	51ohm	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R643	20kohm	20kohm	No Install	No Install
PCH_JTAG_RST#	R353	10kohm	10kohm	No Install	No Install

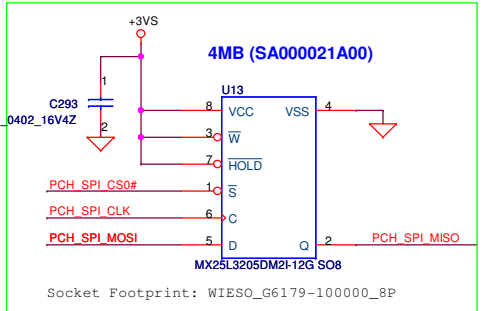
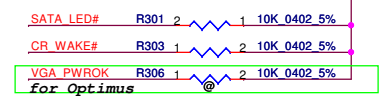
06/01 change R156 from 4.7K to 51 ohm



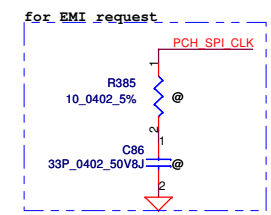
1ST HDD

SATA ODD

eSATA



Socket: SP07000F500 & SP07000H900



U11B

LAN

40 PCIE_PRX_C_LANTX_N1
40 PCIE_PRX_C_LANTX_P1
40 PCIE_PTX_C_LANRX_N1
40 PCIE_PTX_C_LANRX_P1

WLAN

39 PCIE_PRX_WLANTX_N2
39 PCIE_PRX_WLANTX_P2
39 PCIE_PTX_C_WLANRX_N2
39 PCIE_PTX_C_WLANRX_P2

New Card

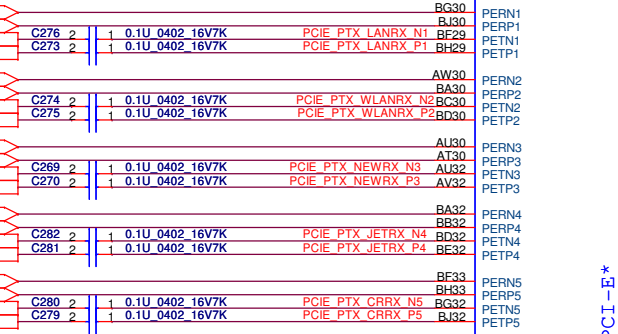
39 PCIE_PRX_NEWTX_N3
39 PCIE_PRX_NEWTX_P3
39 PCIE_PTX_C_NEWRX_N3
39 PCIE_PTX_C_NEWRX_P3

JET

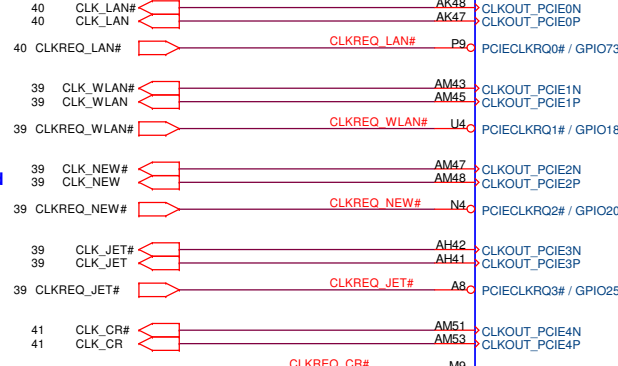
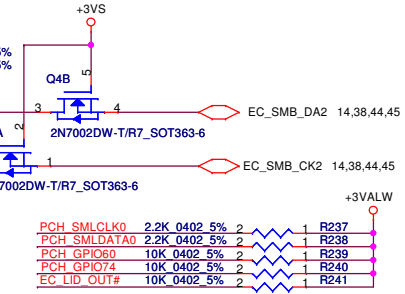
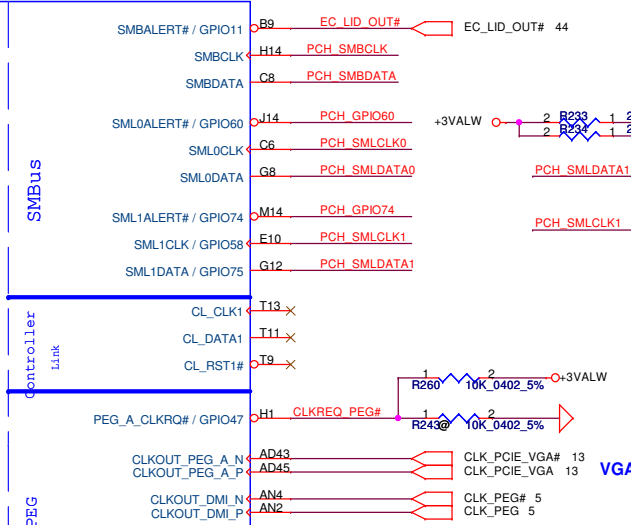
39 PCIE_PRX_JETTX_N4
39 PCIE_PRX_JETTX_P4
39 PCIE_PTX_C_JETRX_N4
39 PCIE_PTX_C_JETRX_P4

Card Reader

41 PCIE_PRX_C_CRTX_N5
41 PCIE_PRX_C_CRTX_P5
41 PCIE_PTX_C_CRRX_N5
41 PCIE_PTX_C_CRRX_P5

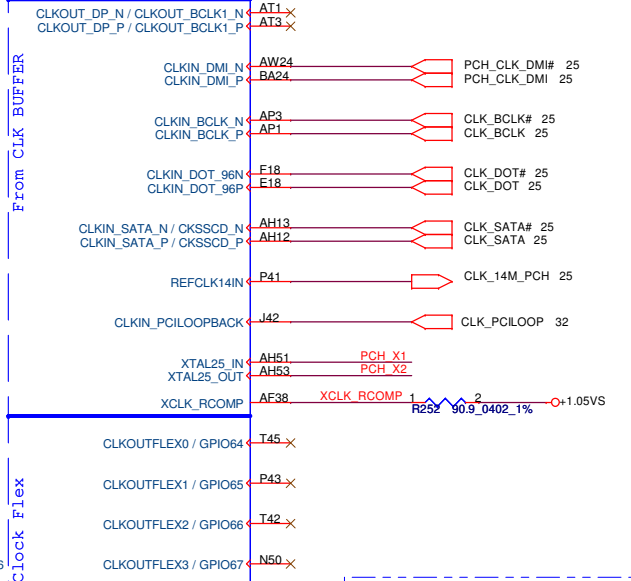


PCI-E*

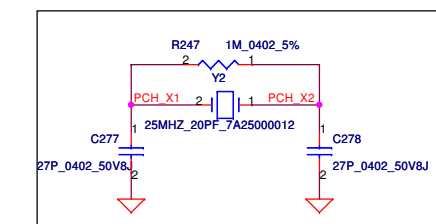


From CLK BUFFER

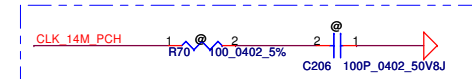
Clock Flex



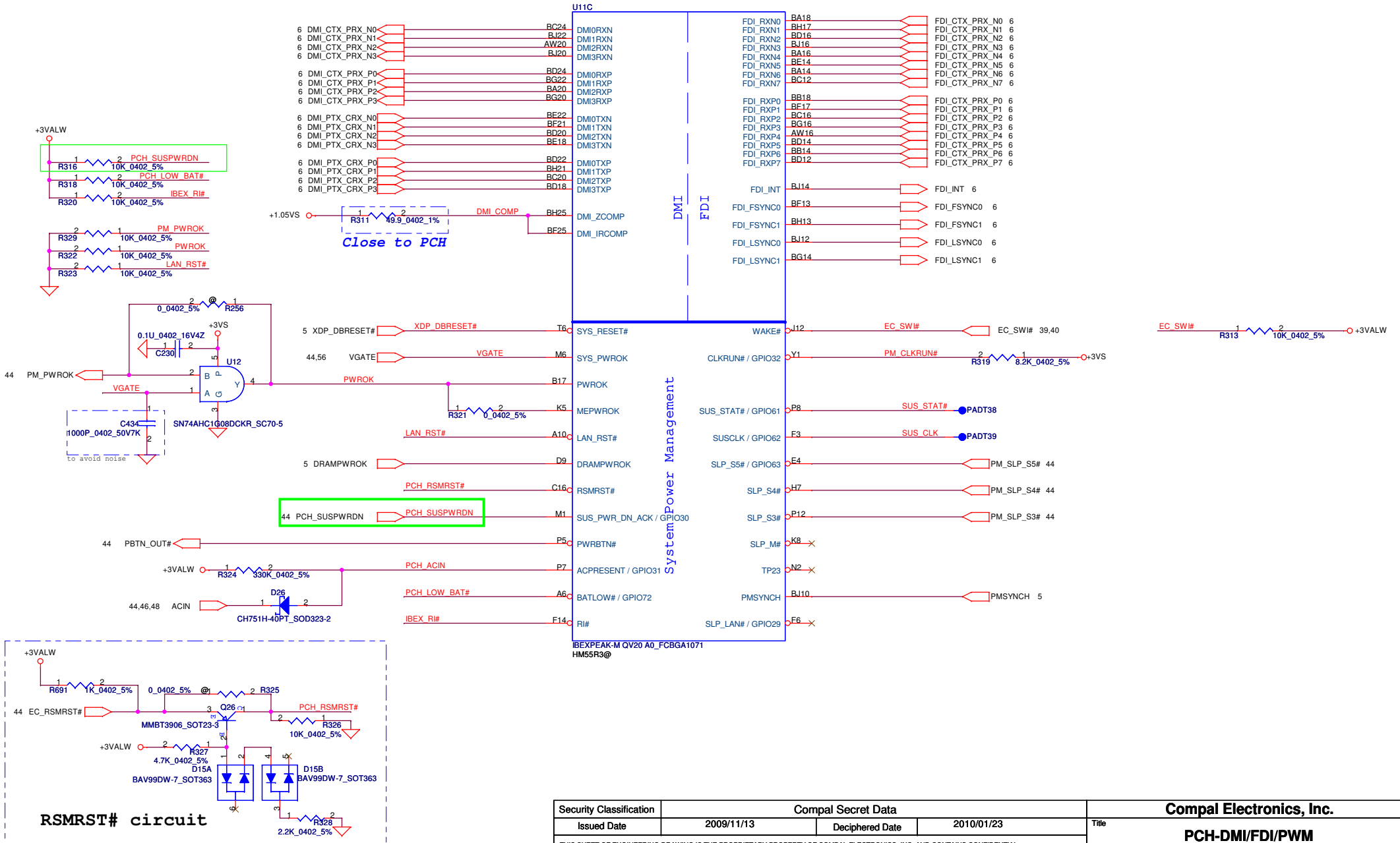
FROM CLK GEN FOR: 133/100/96/14.318 MHZ



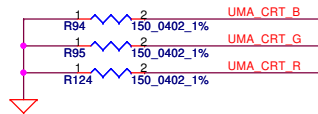
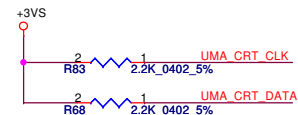
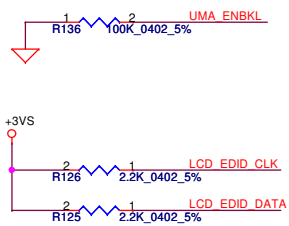
Note: Stuff 0 ohm if 25MHz crystal un-stuff



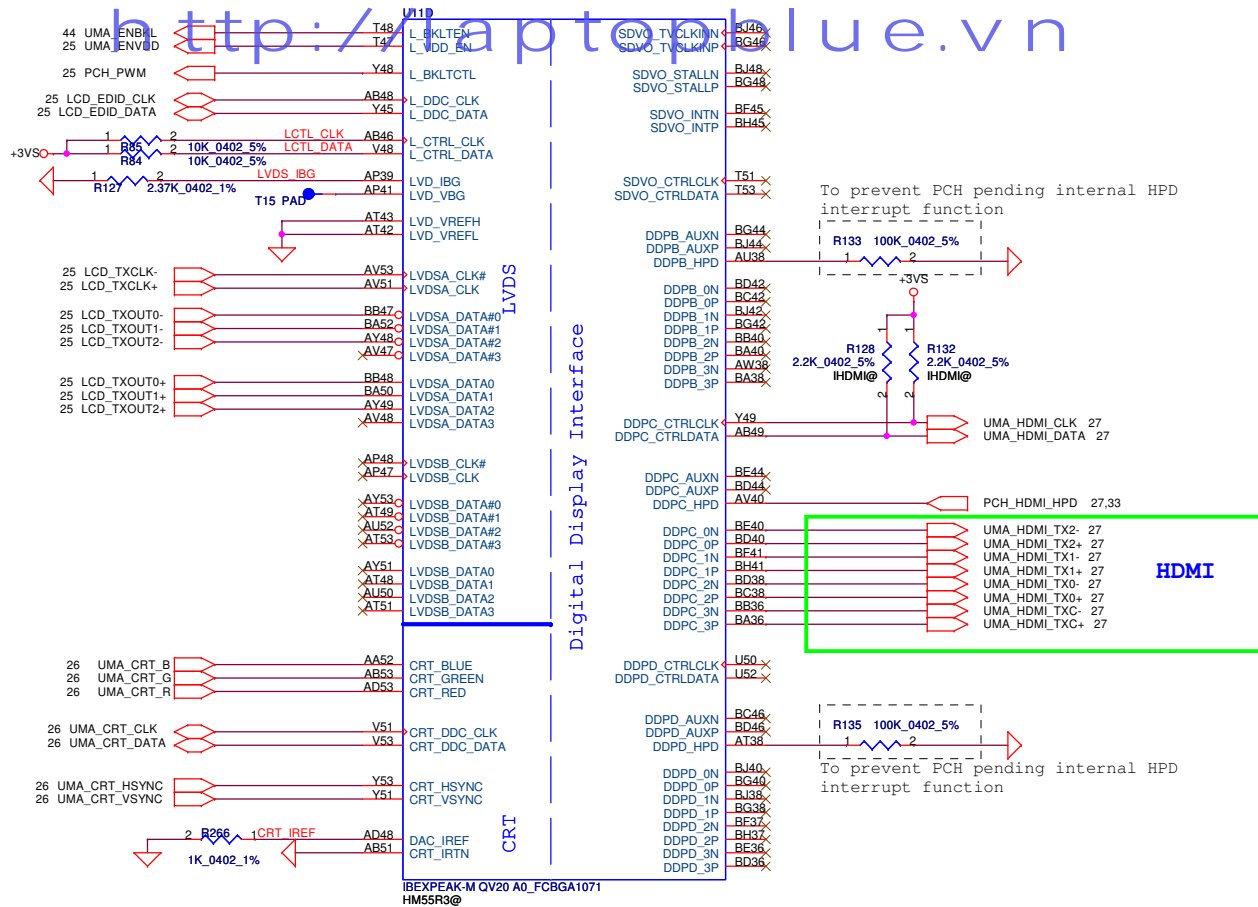
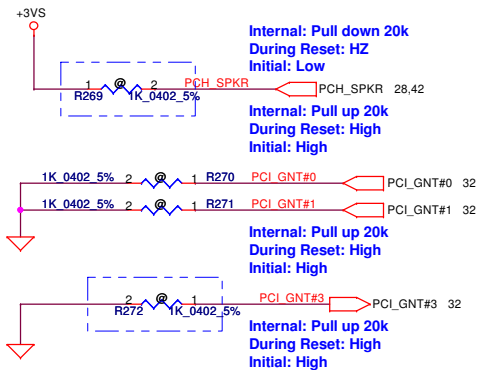
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				NBQAA LA6072P M/B	
				Date	Rev
				Tuesday, March 23, 2010	1.0
				Sheet	30 of 61



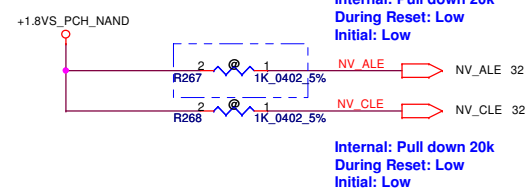
PCH Strap Pin



NO REBOOT Strap		
PCH_SPKR	Low= Disable	High= Enable

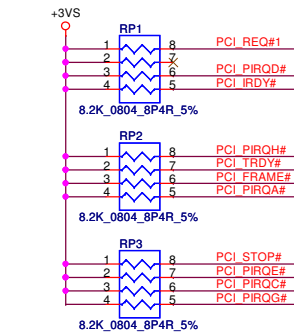
Boot BIOS Strap		
PCI_GNT#1	PCI_GNT#0	Boot BIOS Location
0	0	LPC (Default)
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= A16 swap override Disable

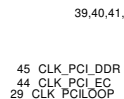
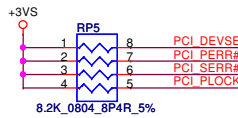
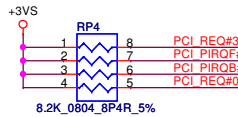


Danbury Technology Enabled	
NV_ALE	High = Enabled Low = Disabled (Default)

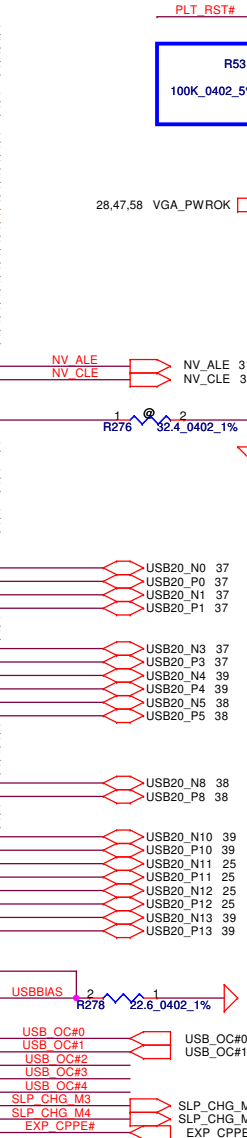
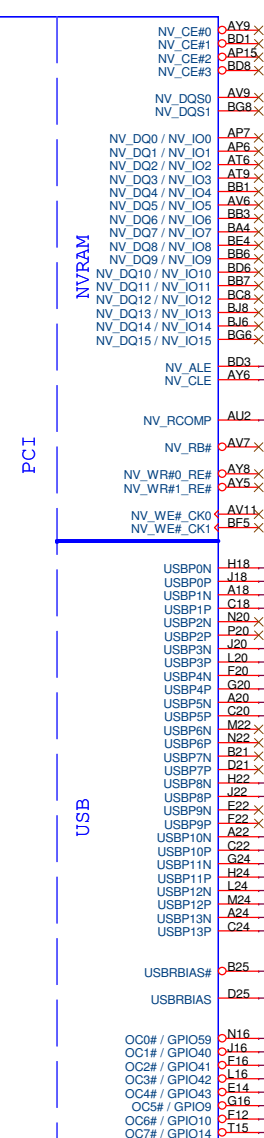
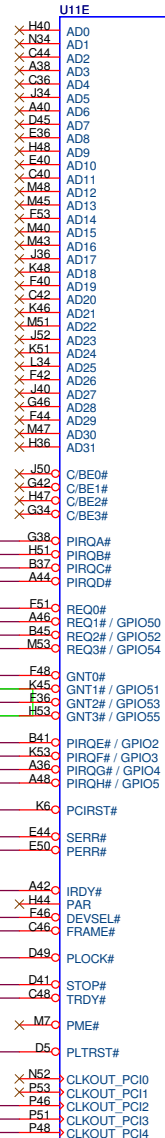
DMI Termination Voltage	
NV_CLE	Low= Set to Vss (Default) High= Set to Vcc



GNT2#/GPIO53: Not pull low, internal pull up 20K



Change to 47 ohm?



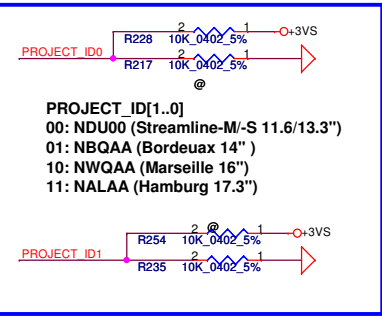
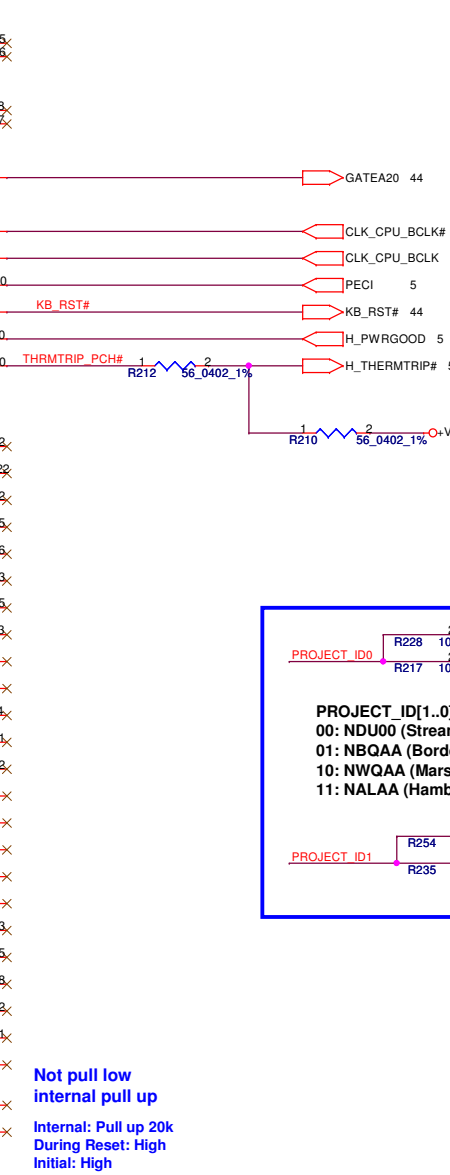
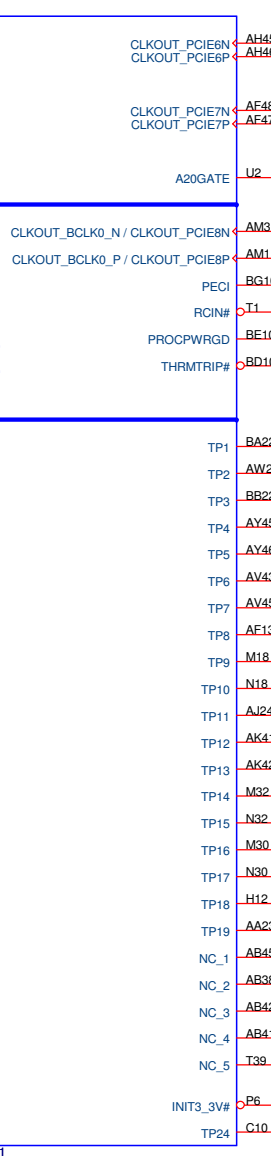
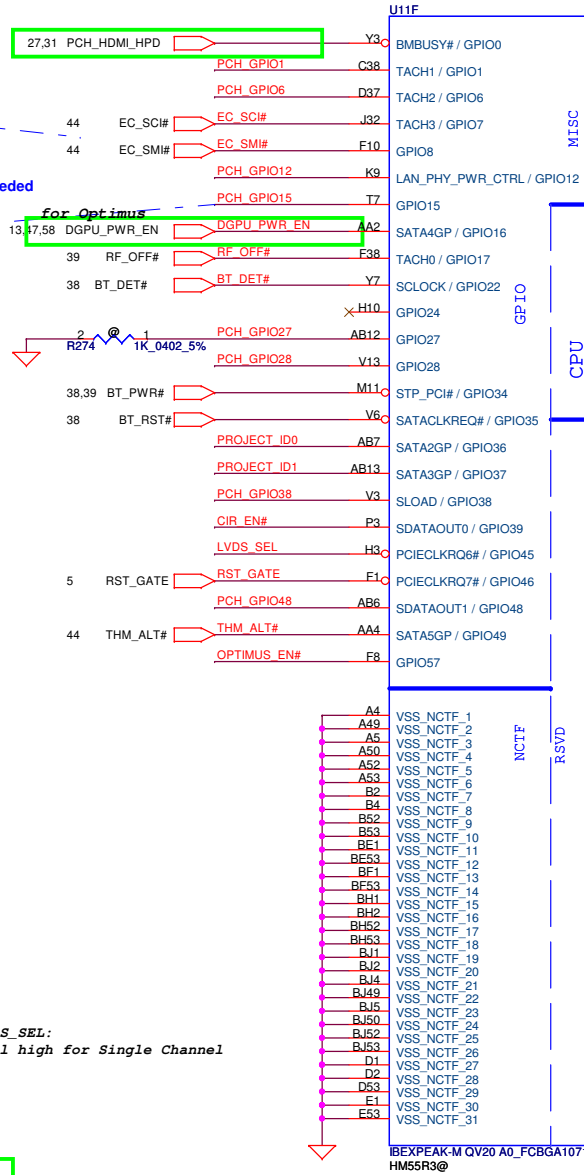
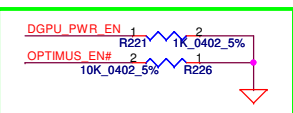
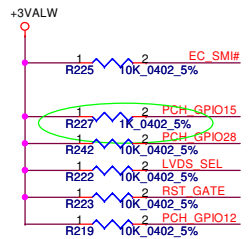
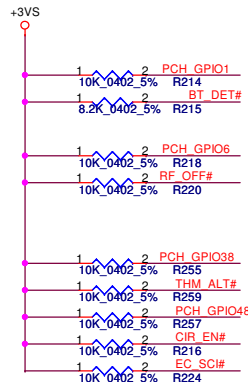
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GPIO8
Not pull down
Internal: Pull up 20k
During Reset: High
Initial: High

GPIO15
a Strong pull up may be needed
for GPIO Functionality
Internal: Pull down 20k
During Reset: Low
Initial: Low

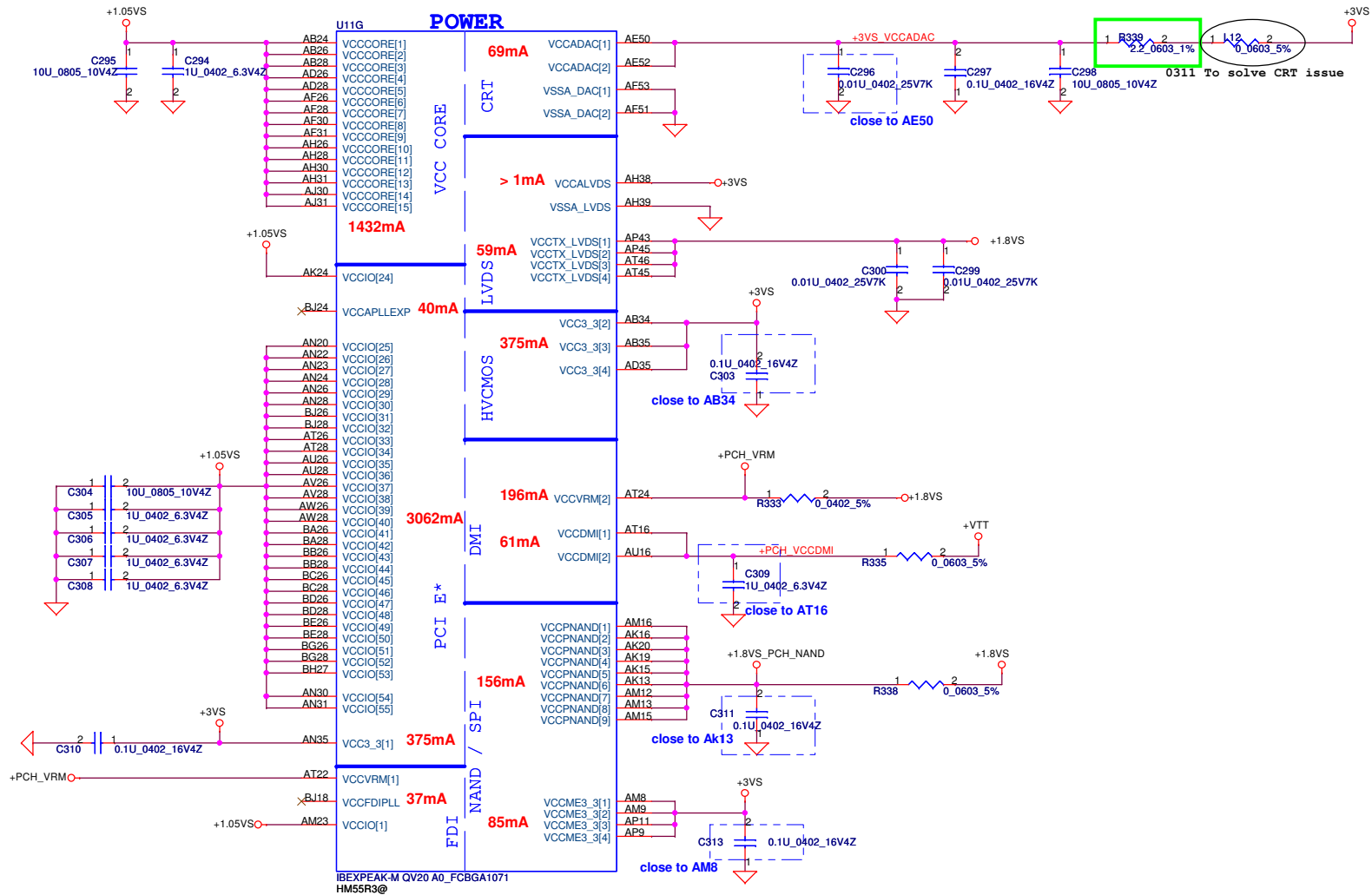
On-Die PLL VR

PCH_GPIO27 High = Enabled (Default)
Low = Disabled



Not pull low
internal pull up
Internal: Pull up 20k
During Reset: High
Initial: High

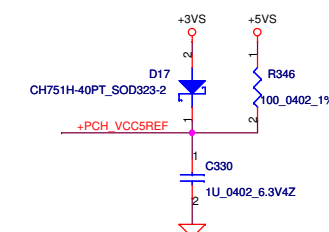
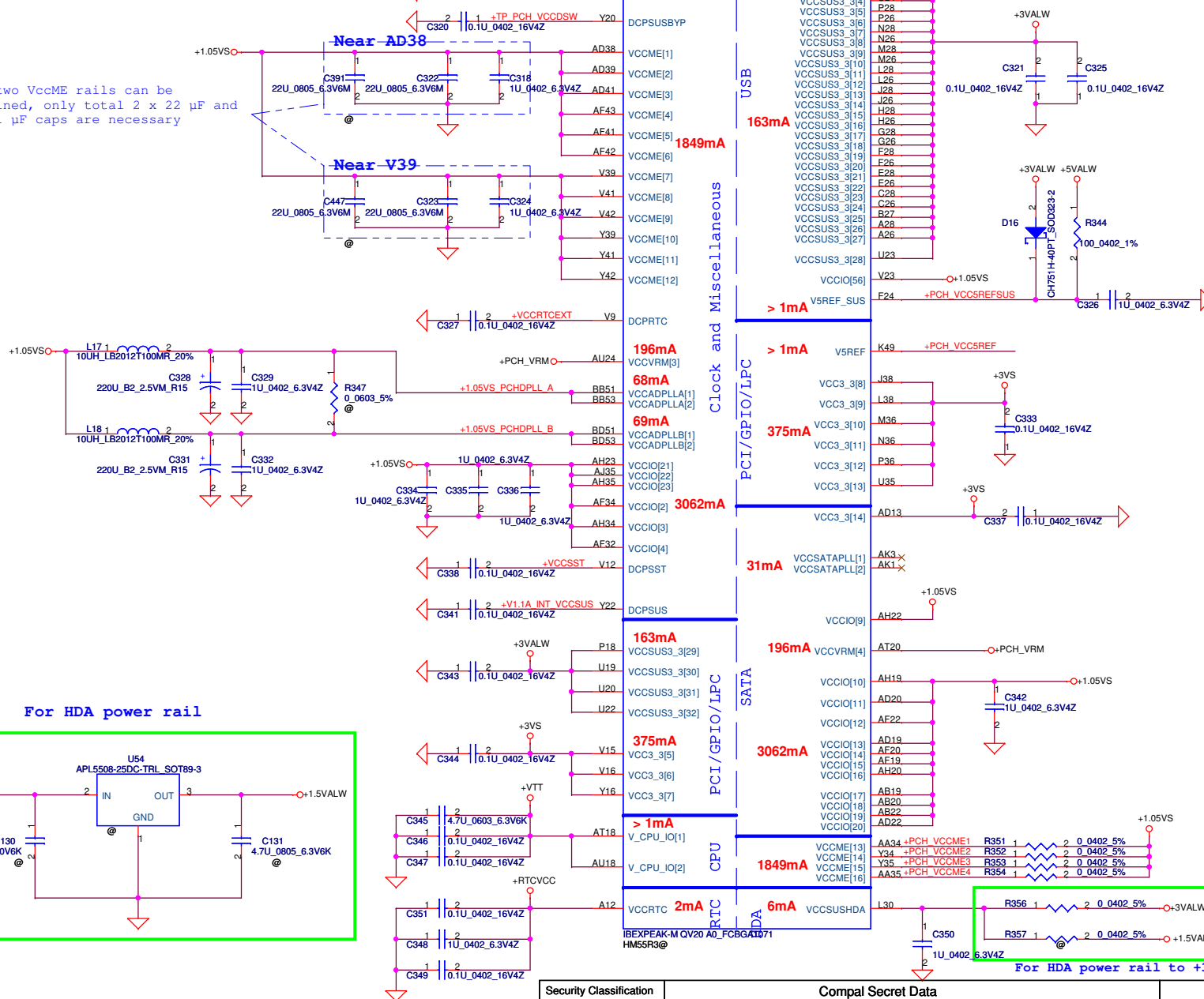
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				Rev	1.0



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VccLAN may be grounded if Intel LAN is disabled

If two VccME rails can be combined, only total 2 x 22 μ F and 2 x 1 μ F caps are necessary



VCCSUSHDA can be either 1.5V or 3.3V

For HDA power rail to +3.3V(default) /+1.5V

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								Customer		NBQAA LA6072P M/B	
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U11I			H49
AY7	VSS[159]	VSS[259]	H5
B11	VSS[160]	VSS[260]	J24
B15	VSS[161]	VSS[261]	K11
B19	VSS[162]	VSS[262]	K43
B23	VSS[163]	VSS[263]	K47
B31	VSS[164]	VSS[264]	K7
B35	VSS[165]	VSS[265]	L14
B39	VSS[166]	VSS[266]	L18
B43	VSS[167]	VSS[267]	L2
B47	VSS[168]	VSS[268]	L22
B7	VSS[169]	VSS[269]	L32
BC12	VSS[170]	VSS[270]	L36
BB12	VSS[171]	VSS[271]	L40
BB16	VSS[172]	VSS[272]	L52
BB20	VSS[173]	VSS[273]	M12
BB24	VSS[174]	VSS[274]	M16
BB30	VSS[175]	VSS[275]	M20
BB34	VSS[176]	VSS[276]	N38
BB38	VSS[177]	VSS[277]	M34
BB42	VSS[178]	VSS[278]	M38
BB49	VSS[179]	VSS[279]	M42
BB5	VSS[180]	VSS[280]	M46
BC10	VSS[181]	VSS[281]	M49
BC14	VSS[182]	VSS[282]	M5
BC18	VSS[183]	VSS[283]	M8
BC2	VSS[184]	VSS[284]	N24
BC22	VSS[185]	VSS[285]	P11
BC32	VSS[186]	VSS[286]	AD15
BC36	VSS[187]	VSS[287]	P22
BC40	VSS[188]	VSS[288]	P30
BC44	VSS[189]	VSS[289]	P32
BC52	VSS[190]	VSS[290]	P34
BH0	VSS[191]	VSS[291]	P42
BD48	VSS[192]	VSS[292]	P45
BD49	VSS[193]	VSS[293]	P47
BD5	VSS[194]	VSS[294]	R2
BE12	VSS[195]	VSS[295]	R52
BE16	VSS[196]	VSS[296]	T12
BE20	VSS[197]	VSS[297]	T41
BE24	VSS[198]	VSS[298]	T46
BE30	VSS[199]	VSS[299]	T49
BE34	VSS[200]	VSS[300]	T5
BE38	VSS[201]	VSS[301]	T8
BE42	VSS[202]	VSS[302]	U30
BE46	VSS[203]	VSS[303]	U31
BE48	VSS[204]	VSS[304]	U32
BE50	VSS[205]	VSS[305]	U34
BE6	VSS[206]	VSS[306]	P38
BE8	VSS[207]	VSS[307]	V11
BF3	VSS[208]	VSS[308]	P16
BF49	VSS[209]	VSS[309]	V19
BF51	VSS[210]	VSS[310]	V20
BG18	VSS[211]	VSS[311]	V22
BG24	VSS[212]	VSS[312]	V30
BG4	VSS[213]	VSS[313]	V31
BG50	VSS[214]	VSS[314]	V32
BH11	VSS[215]	VSS[315]	V34
BH15	VSS[216]	VSS[316]	V35
BH19	VSS[217]	VSS[317]	V38
BH23	VSS[218]	VSS[318]	V43
BH31	VSS[219]	VSS[319]	V45
BH35	VSS[220]	VSS[320]	V46
BH39	VSS[221]	VSS[321]	V47
BH43	VSS[222]	VSS[322]	V49
BH47	VSS[223]	VSS[323]	V5
BH7	VSS[224]	VSS[324]	V7
C12	VSS[225]	VSS[325]	V8
C50	VSS[226]	VSS[326]	W2
D51	VSS[227]	VSS[327]	W52
E12	VSS[228]	VSS[328]	Y11
E16	VSS[229]	VSS[329]	Y12
E20	VSS[230]	VSS[330]	Y15
E24	VSS[231]	VSS[331]	Y19
E30	VSS[232]	VSS[332]	Y23
E34	VSS[233]	VSS[333]	Y28
E38	VSS[234]	VSS[334]	Y30
E42	VSS[235]	VSS[335]	Y31
E46	VSS[236]	VSS[336]	Y32
E48	VSS[237]	VSS[337]	Y38
E6	VSS[238]	VSS[338]	Y43
F8	VSS[239]	VSS[339]	Y46
F49	VSS[240]	VSS[340]	P49
F5	VSS[241]	VSS[341]	Y5
G10	VSS[242]	VSS[342]	Y6
G14	VSS[243]	VSS[343]	Y8
G18	VSS[244]	VSS[344]	P24
G2	VSS[245]	VSS[345]	T43
G22	VSS[246]	VSS[346]	AD51
G32	VSS[247]	VSS[347]	AT8
G36	VSS[248]	VSS[348]	AD47
G40	VSS[249]	VSS[349]	Y47
G44	VSS[250]	VSS[350]	AT12
G52	VSS[251]	VSS[351]	AM6
AF39	VSS[252]	VSS[352]	AT13
H16	VSS[253]	VSS[353]	AM5
H20	VSS[254]	VSS[354]	AK45
H30	VSS[255]	VSS[355]	AK38
H34	VSS[256]	VSS[356]	AV14
H38	VSS[257]	VSS[357]	
H42	VSS[258]	VSS[358]	

IBEXPEAK-M QV20 A0_FCBGA1071

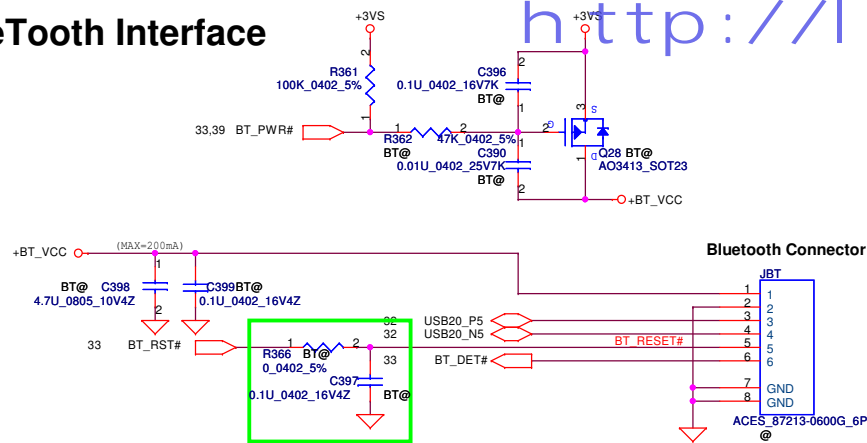
HM55R3@

U11H			AK30
AB16	VSS[0]	VSS[80]	AK31
AA19	VSS[1]	VSS[81]	AK32
AA20	VSS[2]	VSS[82]	AK34
AA22	VSS[3]	VSS[83]	AK35
AM19	VSS[4]	VSS[84]	AK38
AA24	VSS[5]	VSS[85]	AK43
AA26	VSS[6]	VSS[86]	AK46
AA28	VSS[7]	VSS[87]	AK49
AA30	VSS[8]	VSS[88]	AK5
AA31	VSS[9]	VSS[89]	AK8
AA32	VSS[10]	VSS[90]	AL2
AB11	VSS[11]	VSS[91]	AL52
AB15	VSS[12]	VSS[92]	AM11
AB23	VSS[13]	VSS[93]	BB44
AB30	VSS[14]	VSS[94]	AD24
AB31	VSS[15]	VSS[95]	AM20
AB32	VSS[16]	VSS[96]	AM22
AB39	VSS[17]	VSS[97]	AM24
AB43	VSS[18]	VSS[98]	AM26
AB47	VSS[19]	VSS[99]	AM28
AB5	VSS[20]	VSS[100]	BA42
AB6	VSS[21]	VSS[101]	AM30
AC3	VSS[22]	VSS[102]	AM32
AC52	VSS[23]	VSS[103]	AM34
AD11	VSS[24]	VSS[104]	AM35
AD12	VSS[25]	VSS[105]	AM38
AD16	VSS[26]	VSS[106]	AM39
AD23	VSS[27]	VSS[107]	AM42
AD30	VSS[28]	VSS[108]	AM44
AD31	VSS[29]	VSS[109]	AM7
AD32	VSS[30]	VSS[110]	AA50
AD34	VSS[31]	VSS[111]	BB10
AIJ22	VSS[32]	VSS[112]	AN32
AD42	VSS[33]	VSS[113]	AN50
AD46	VSS[34]	VSS[114]	AN52
AD49	VSS[35]	VSS[115]	AP12
AD7	VSS[36]	VSS[116]	AP42
AE2	VSS[37]	VSS[117]	AP46
AE4	VSS[38]	VSS[118]	AP49
AF12	VSS[39]	VSS[119]	AP5
Y13	VSS[40]	VSS[120]	AP8
AA49	VSS[41]	VSS[121]	AP92
AF35	VSS[42]	VSS[122]	AT11
AP13	VSS[43]	VSS[123]	AT32
AN34	VSS[44]	VSS[124]	AT36
AF45	VSS[45]	VSS[125]	AT41
AF46	VSS[46]	VSS[126]	AT47
AF49	VSS[47]	VSS[127]	AT7
AF5	VSS[48]	VSS[128]	AV12
AF8	VSS[49]	VSS[129]	AV16
AG2	VSS[50]	VSS[130]	AV20
AG52	VSS[51]	VSS[131]	AV24
AH11	VSS[52]	VSS[132]	AV30
AH15	VSS[53]	VSS[133]	AV34
AH16	VSS[54]	VSS[134]	AV38
AH24	VSS[55]	VSS[135]	AV42
AH32	VSS[56]	VSS[136]	AV46
AV18	VSS[57]	VSS[137]	AV49
AH43	VSS[58]	VSS[138]	AV5
AH47	VSS[59]	VSS[139]	AV8
AH7	VSS[60]	VSS[140]	AW14
AJ19	VSS[61]	VSS[141]	AW18
AJ2	VSS[62]	VSS[142]	AW2
AJ20	VSS[63]	VSS[143]	BF9
AJ22	VSS[64]	VSS[144]	AW32
AJ23	VSS[65]	VSS[145]	AW36
AJ25	VSS[66]	VSS[146]	AW40
AJ26	VSS[67]	VSS[147]	AW52
AJ28	VSS[68]	VSS[148]	AY11
AJ32	VSS[69]	VSS[149]	AY43
AJ34	VSS[70]	VSS[150]	AY47
AT5	VSS[71]	VSS[151]	
AJ4	VSS[72]	VSS[152]	
AK12	VSS[73]	VSS[153]	
AM41	VSS[74]	VSS[154]	
AN19	VSS[75]	VSS[155]	
AK26	VSS[76]	VSS[156]	
AK22	VSS[77]	VSS[157]	
AK23	VSS[78]	VSS[158]	
AK28	VSS[79]		

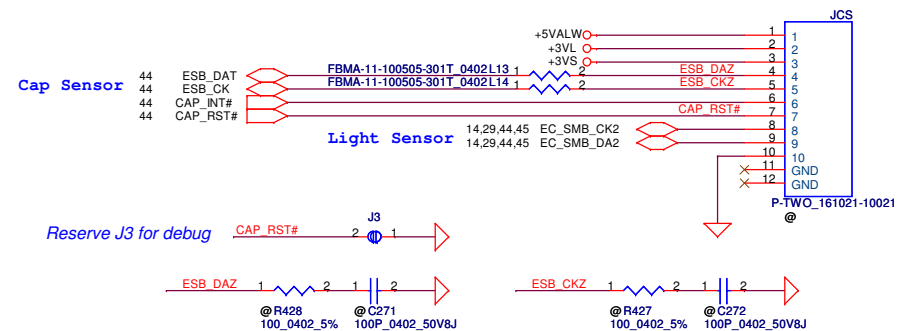
IBEXPEAK-M QV20 A0_FCBGA1071
HM55R3@

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				Date:	Monday, March 22, 2010
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				Rev	1.0

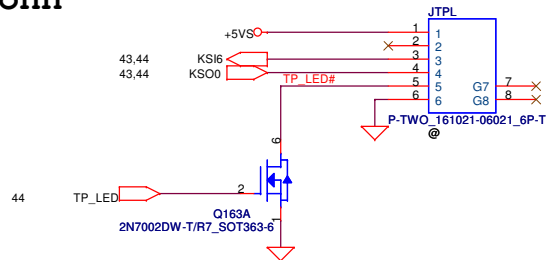
BlueTooth Interface



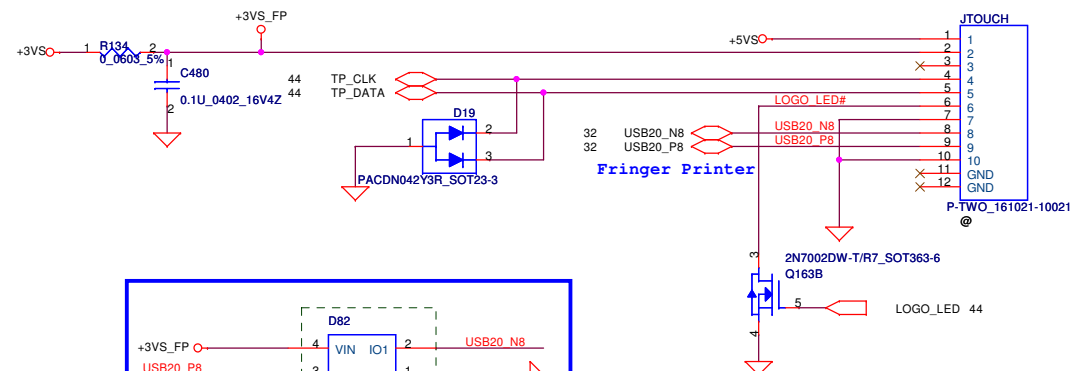
Cap Sensor / Light Sensor Conn



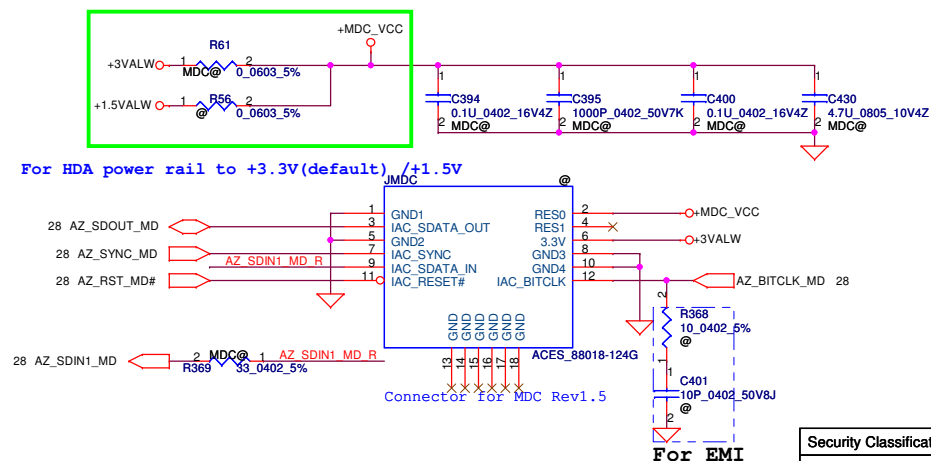
TP LED Conn



TP/B LED/B FP/B Conn

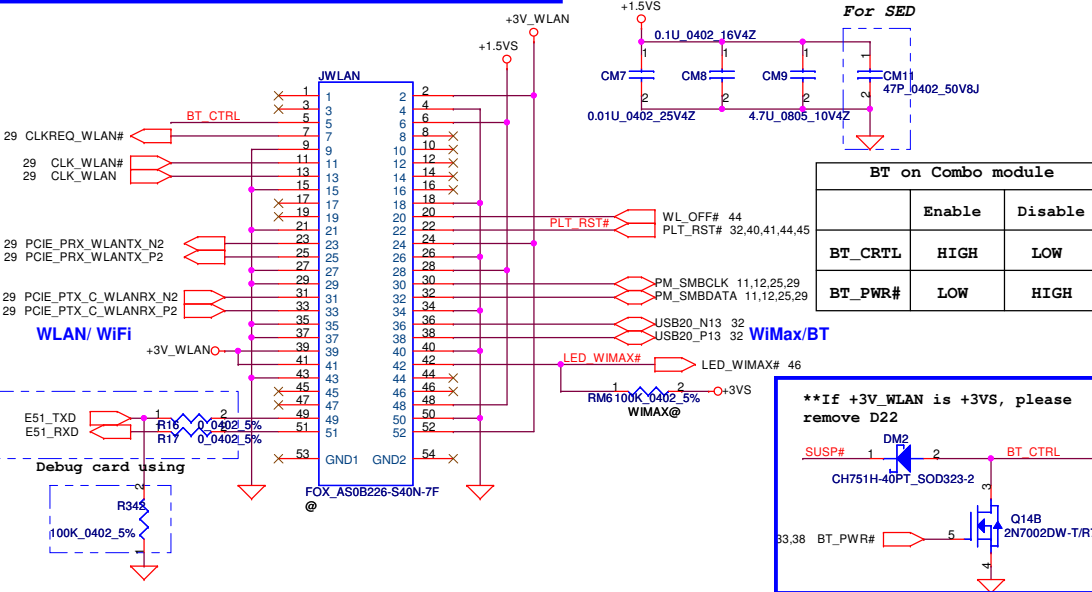
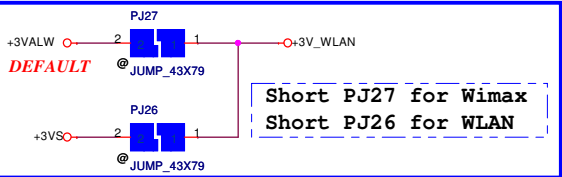


MDC 1.5 Conn

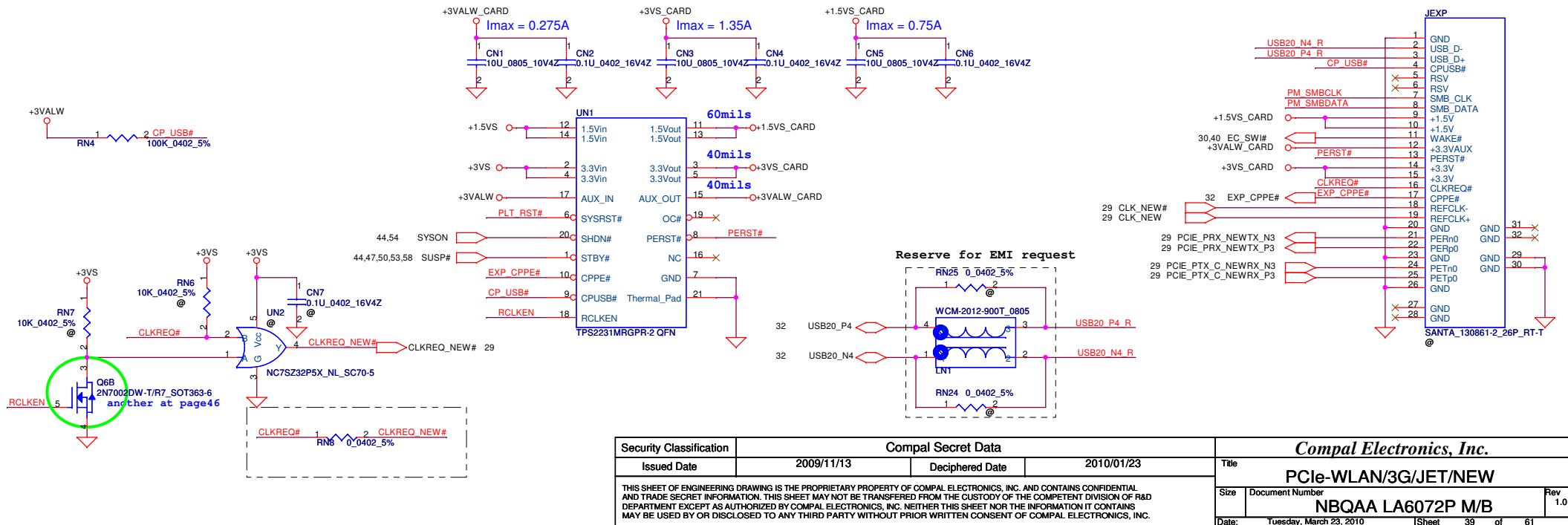
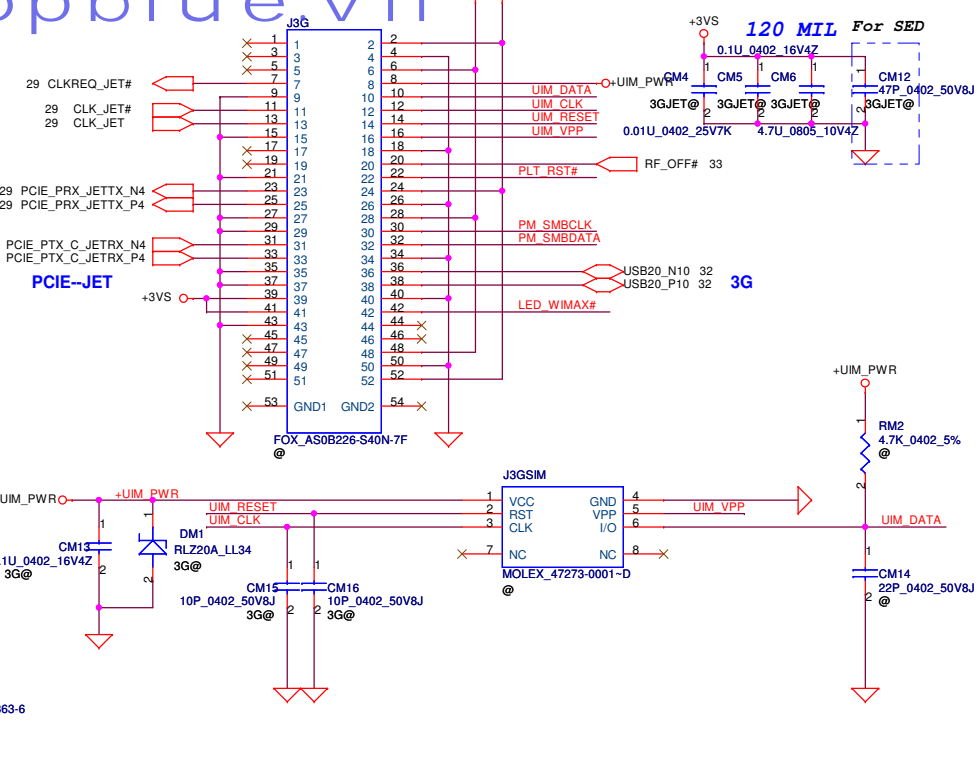


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PCIe Mini Card-WLAN/WiMax



PCIe Mini Card-3G/JET

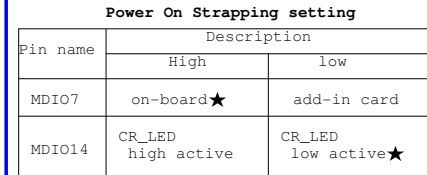


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JMB389



TAITW_R015-300-LM_RV @



The schematic shows the MDIO interface connections. MDIO7 is connected to RC28 (10K_0402_5%) and MDIO14 is connected to RC26 (10K_0402_5%) and RC25 (200K_0402_5%). A +3VS supply is connected to the top of the network, and a ground symbol is connected to the bottom.



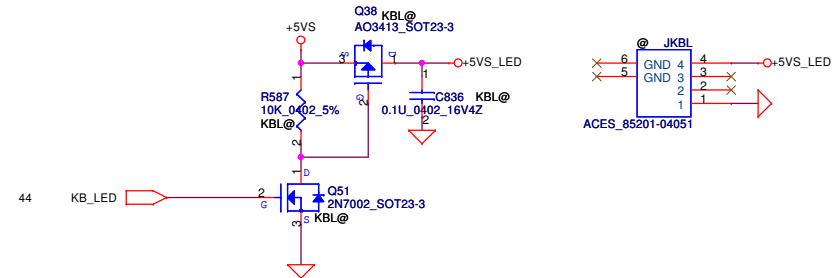
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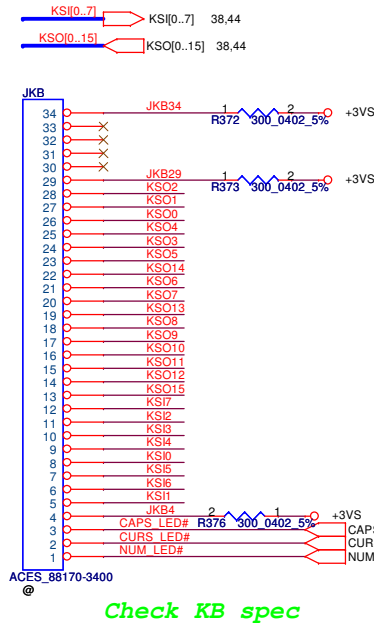
Card Reader-JMB389C/385C

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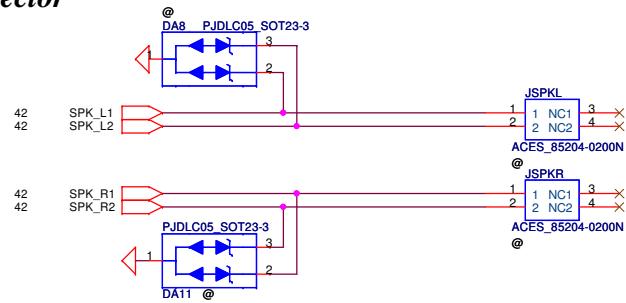
Keyboard LED



KEYBOARD CONN.

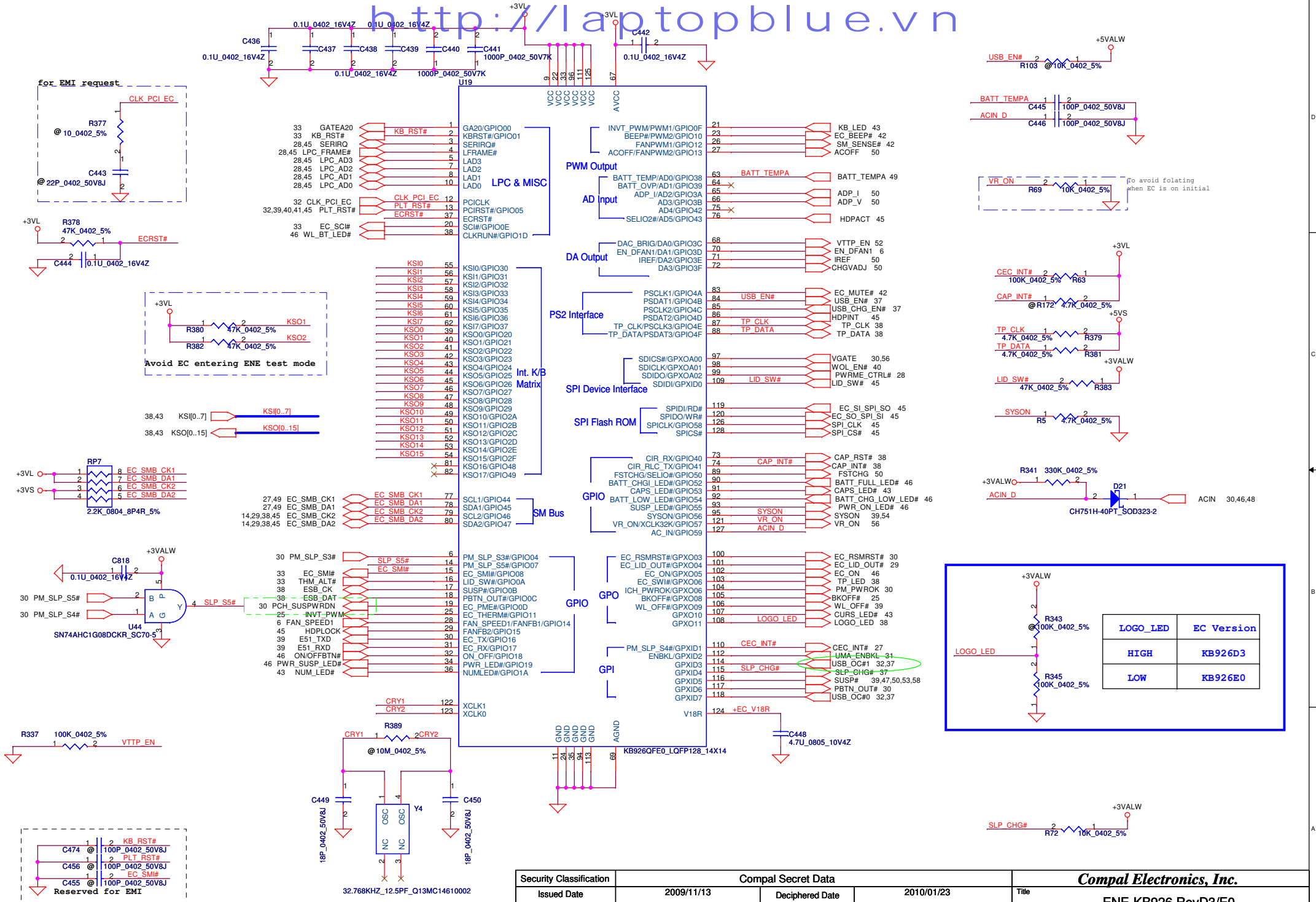


please close to JKB		
<u>CURS_LED#</u>	C402	2 100P_0402_50VBJ
<u>KSO2</u>	C404	2 100P_0402_50VBJ
<u>KSO1</u>	C405	2 100P_0402_50VBJ
<u>KSO0</u>	C406	2 100P_0402_50VBJ
<u>KSO4</u>	C407	2 100P_0402_50VBJ
<u>KSO3</u>	C408	2 100P_0402_50VBJ
<u>KSO5</u>	C409	2 100P_0402_50VBJ
<u>KSO14</u>	C410	2 100P_0402_50VBJ
<u>KSO6</u>	C411	2 100P_0402_50VBJ
<u>KSO7</u>	C412	2 100P_0402_50VBJ
<u>KSO13</u>	C413	2 100P_0402_50VBJ
<u>KSO8</u>	C415	2 100P_0402_50VBJ
<u>KSO9</u>	C416	2 100P_0402_50VBJ
<u>KSO10</u>	C417	2 100P_0402_50VBJ
<u>KSO11</u>	C418	2 100P_0402_50VBJ
<u>KSO12</u>	C419	2 100P_0402_50VBJ
<u>KSO15</u>	C420	2 100P_0402_50VBJ
<u>KS17</u>	C421	2 100P_0402_50VBJ
<u>KS12</u>	C422	2 100P_0402_50VBJ
<u>KS13</u>	C423	2 100P_0402_50VBJ
<u>KS14</u>	C424	2 100P_0402_50VBJ
<u>KS10</u>	C425	2 100P_0402_50VBJ
<u>KS15</u>	C427	2 100P_0402_50VBJ
<u>KS16</u>	C429	2 100P_0402_50VBJ
<u>KS11</u>	C431	2 100P_0402_50VBJ
<u>CAPS_LED#</u>	C433	2 100P_0402_50VBJ
<u>NUM_LED#</u>	C435	2 100P_0402_50VBJ



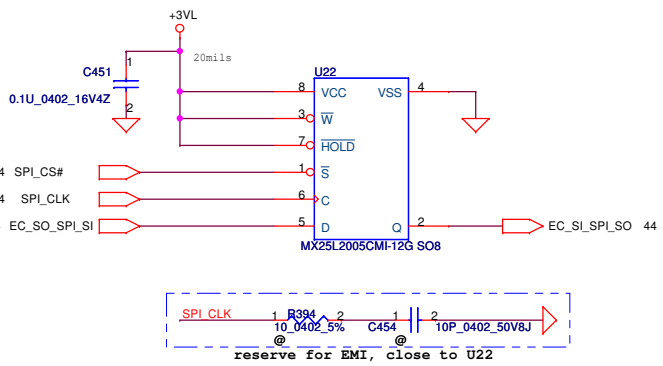
Check KB spec

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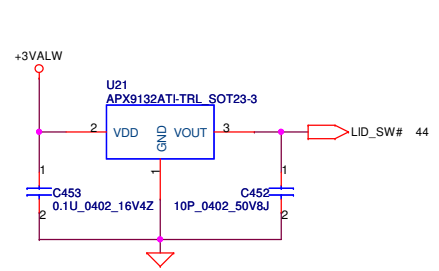


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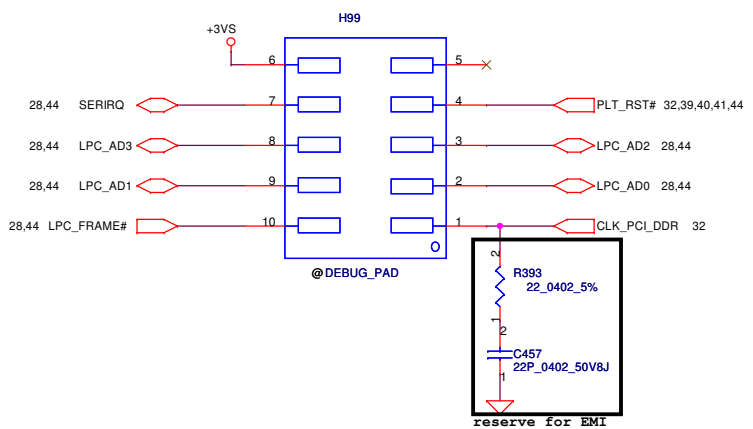
SPI Flash (256KB)
Socket: SP07000F500 & SP07000H900



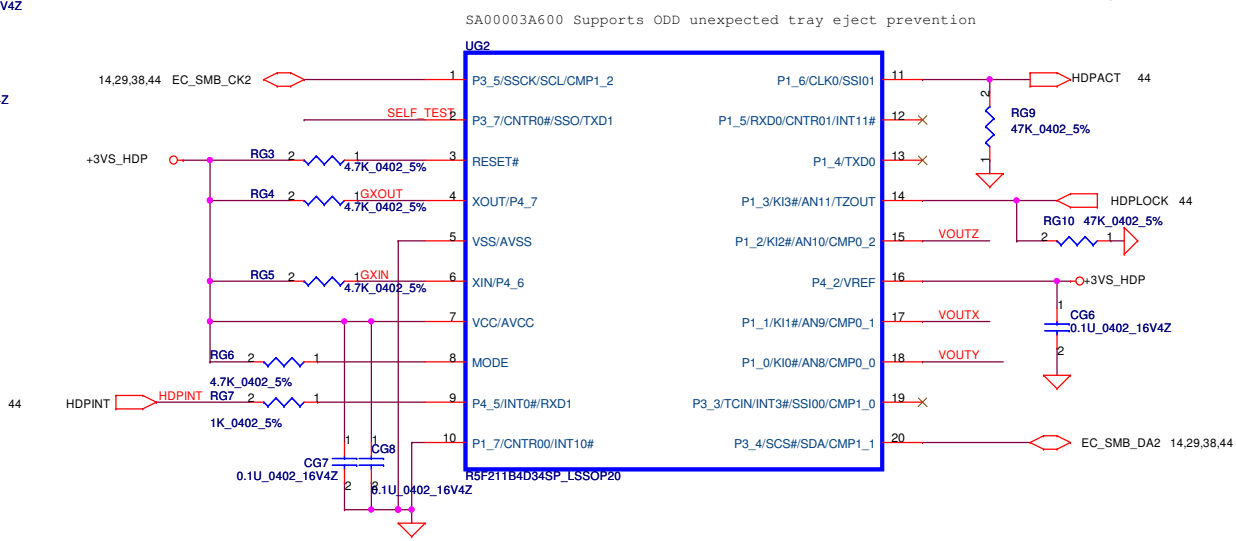
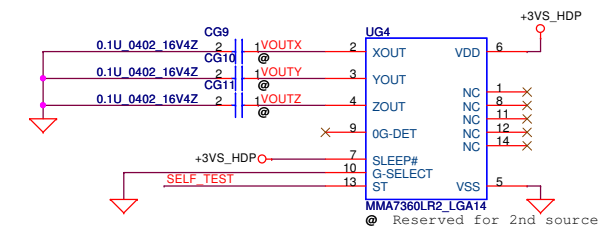
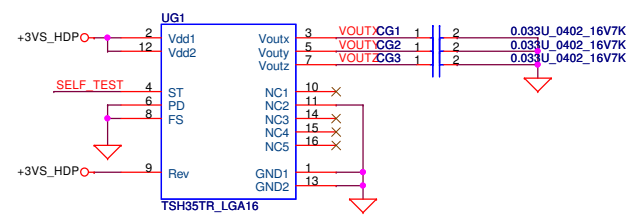
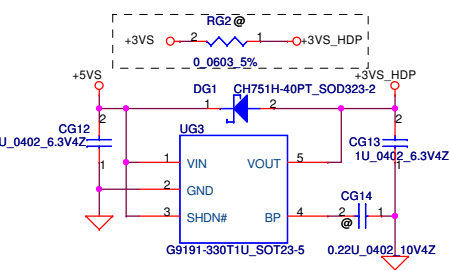
Lid SW



LPC Debug Port
Please place the PAD under DDR DIMM.

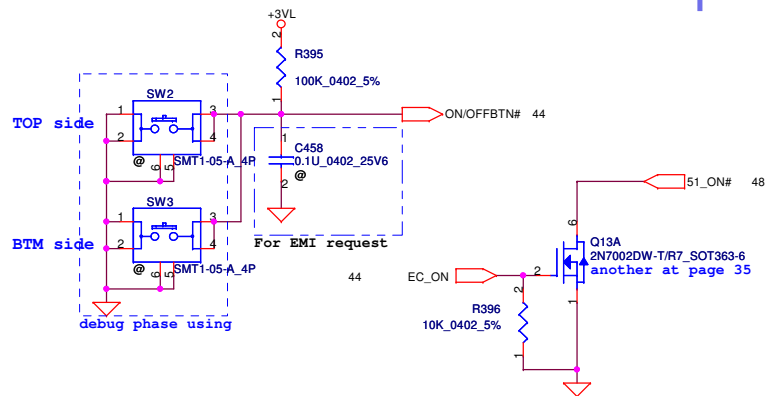


G-Sensor

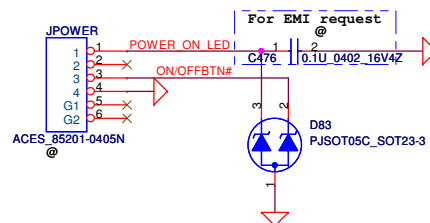


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Size		Document Number		Rev	
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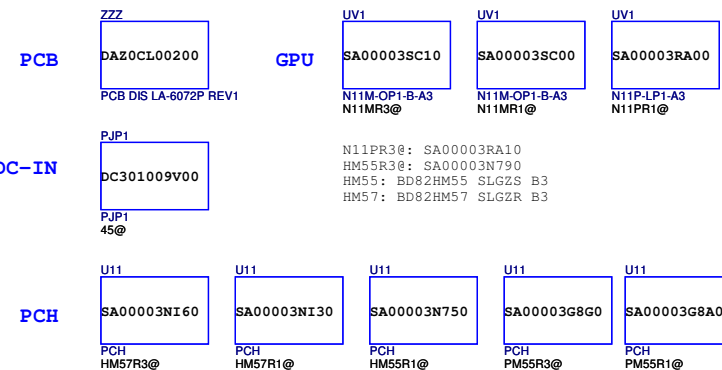
Power Button



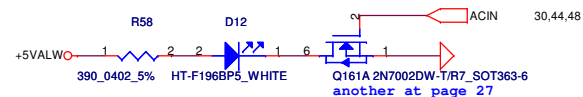
PWR/B Conn



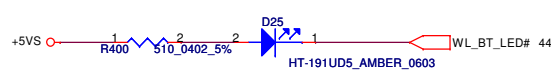
ISPD



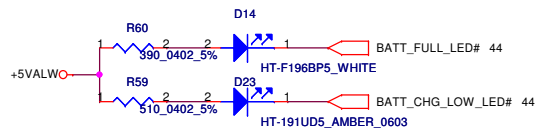
DC-IN LED



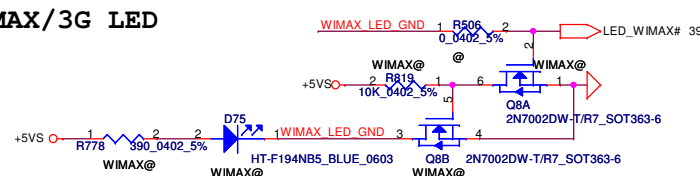
WL/BT LED



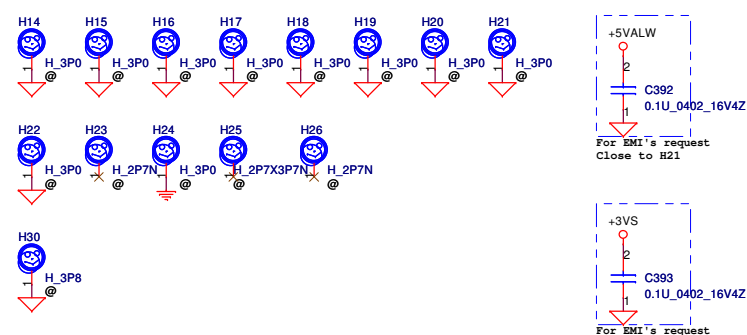
BATT CHARGE/FULL LED



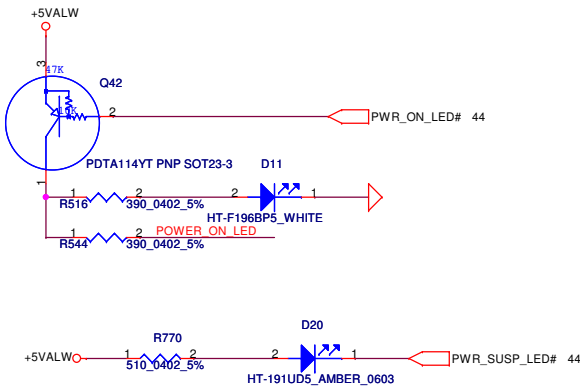
WiMAX/3G LED



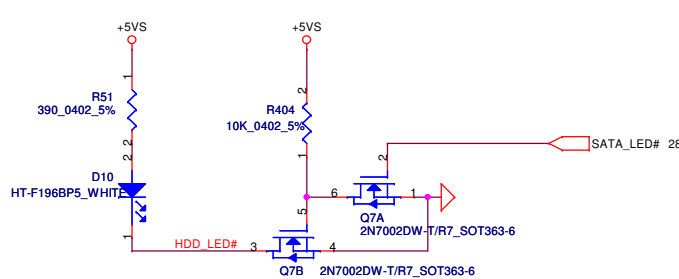
Screw Hole



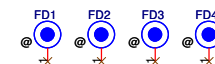
POWER/SUSPEND LED



HDD LED

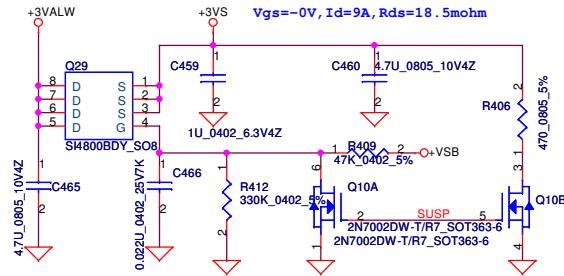


PCB Federal Mark PAD

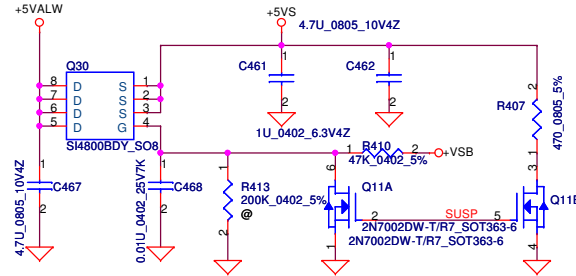


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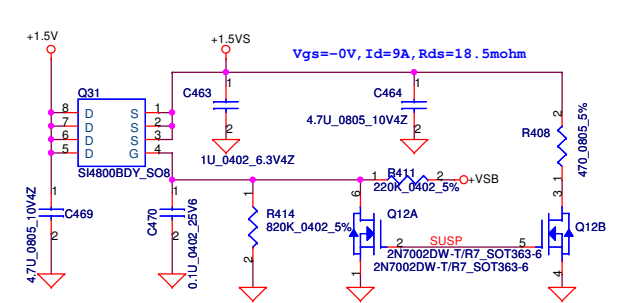
+3VALW TO +3VS



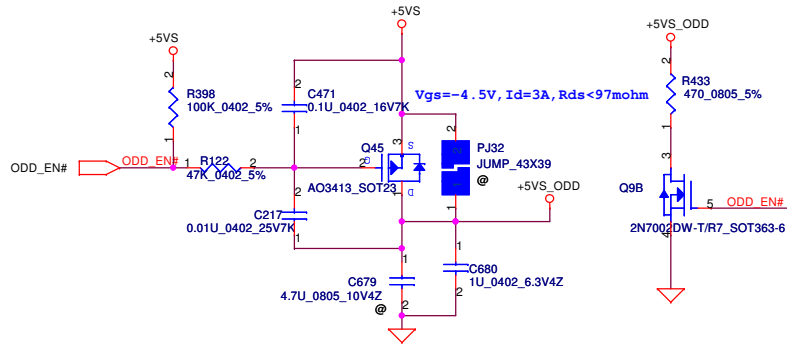
+5VALW TO +5VS



+1.5V to +1.5VS

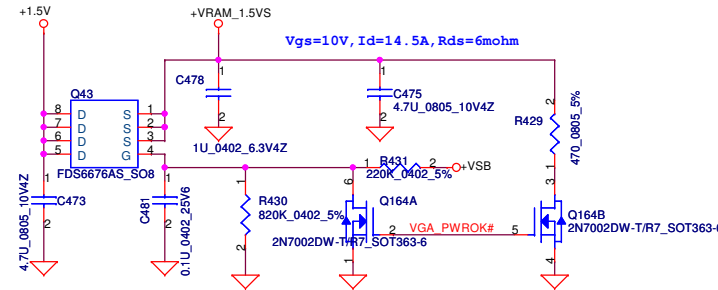


+5VS TO +5VS_ODD



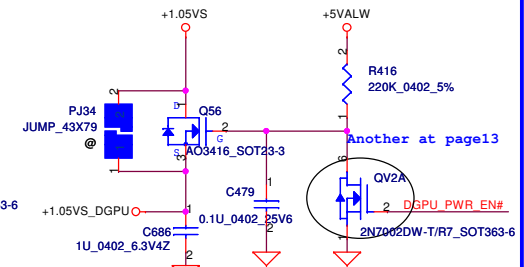
+1.5V to +VRAM_1.5VS

(11A, 440mils, Via NO.= 22)



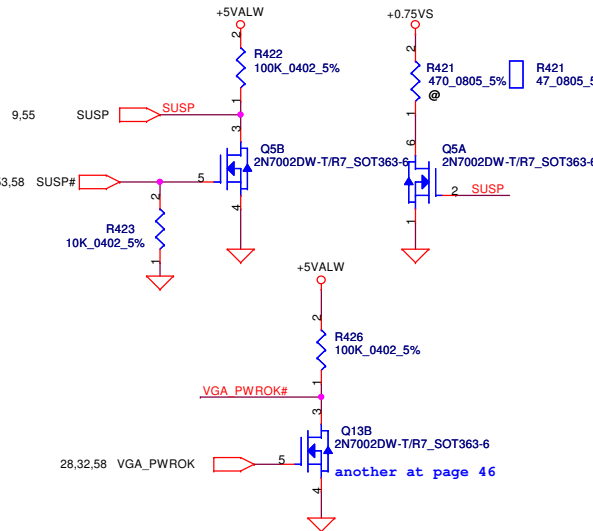
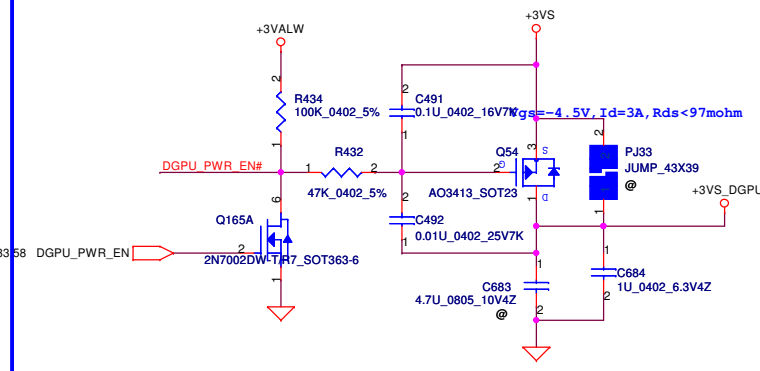
+1.05VS to +1.05VS_DGPU

(2.87A, 120mils, Via NO.= 6)

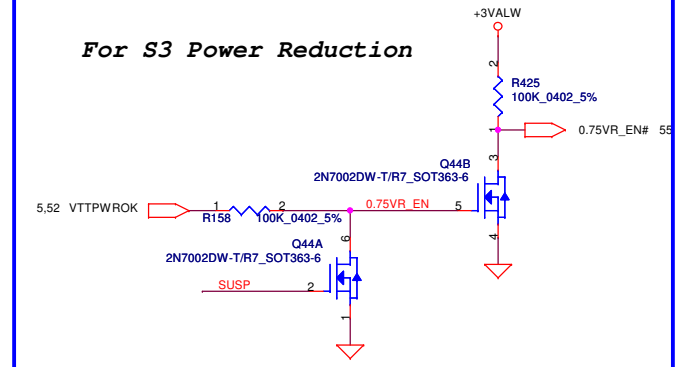


+3VS to +3VS_DGPU

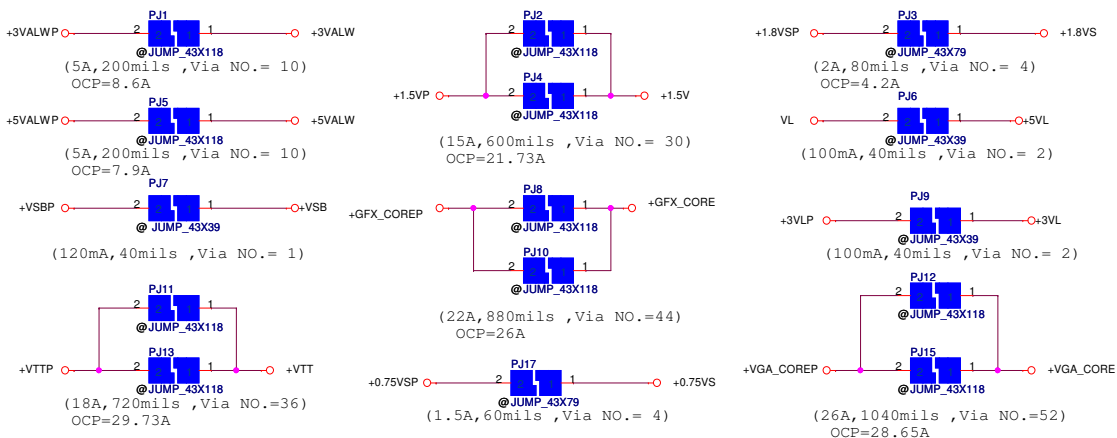
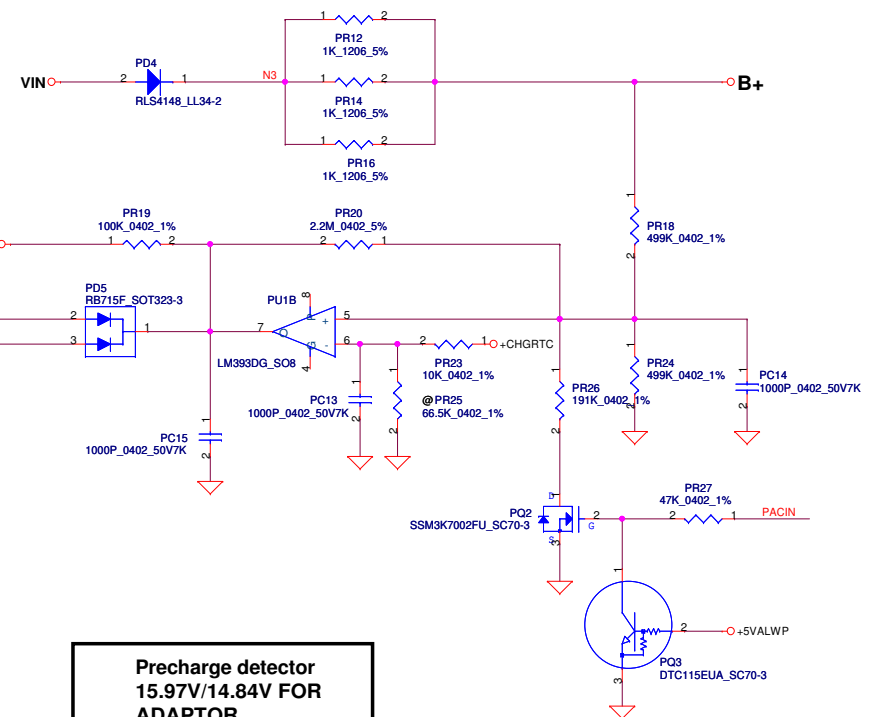
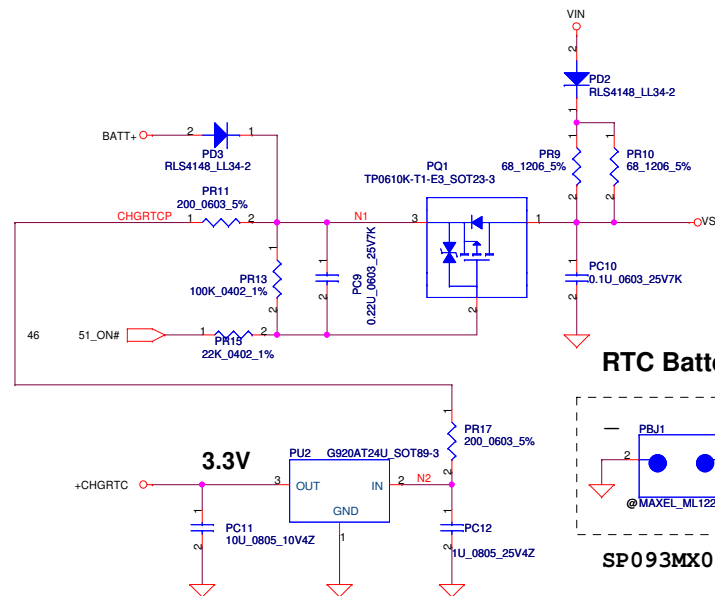
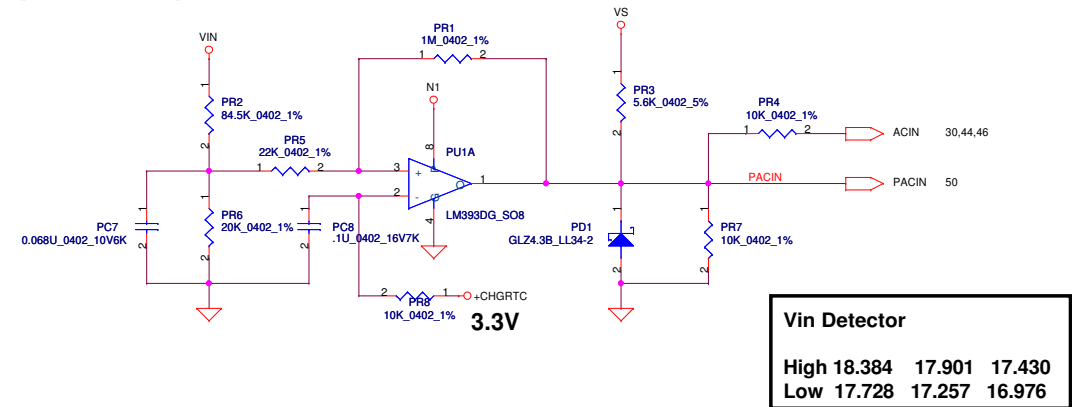
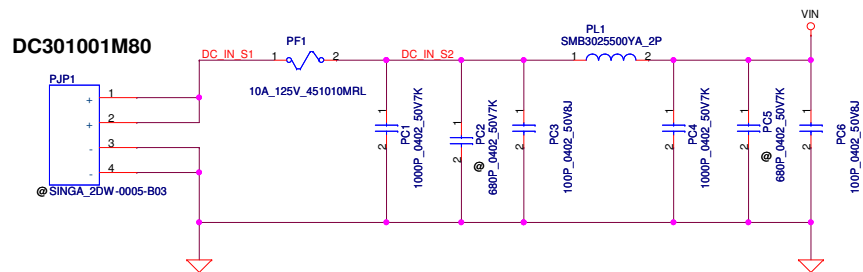
(780mA, 40mils, Via NO.= 2)



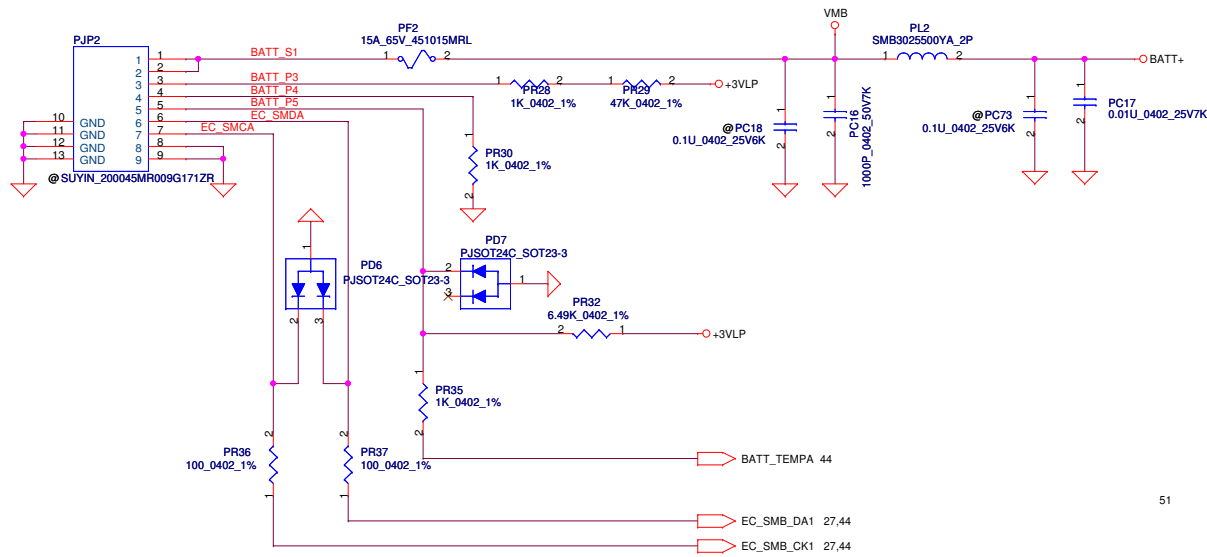
For S3 Power Reduction



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						Size		Document Number		Rev	
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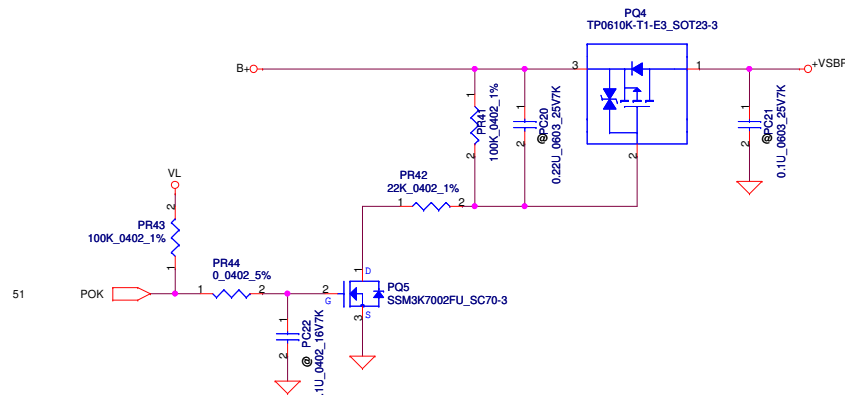
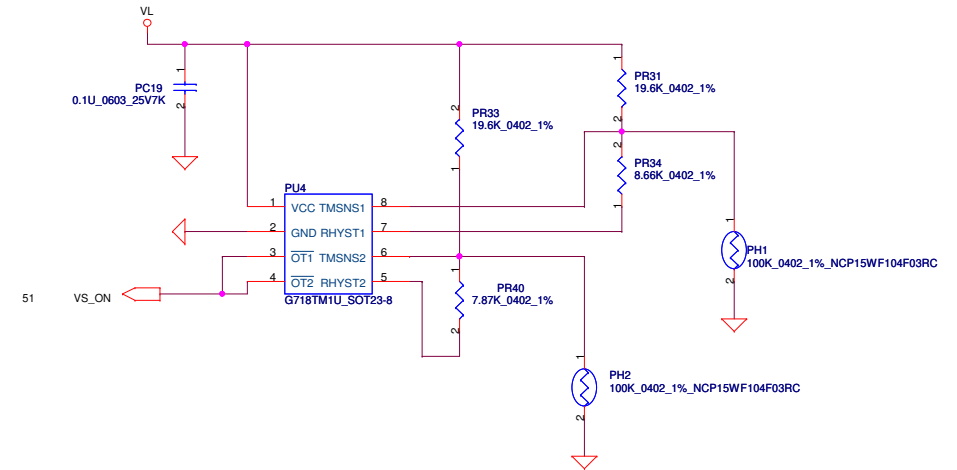


PH1 under CPU botten side :

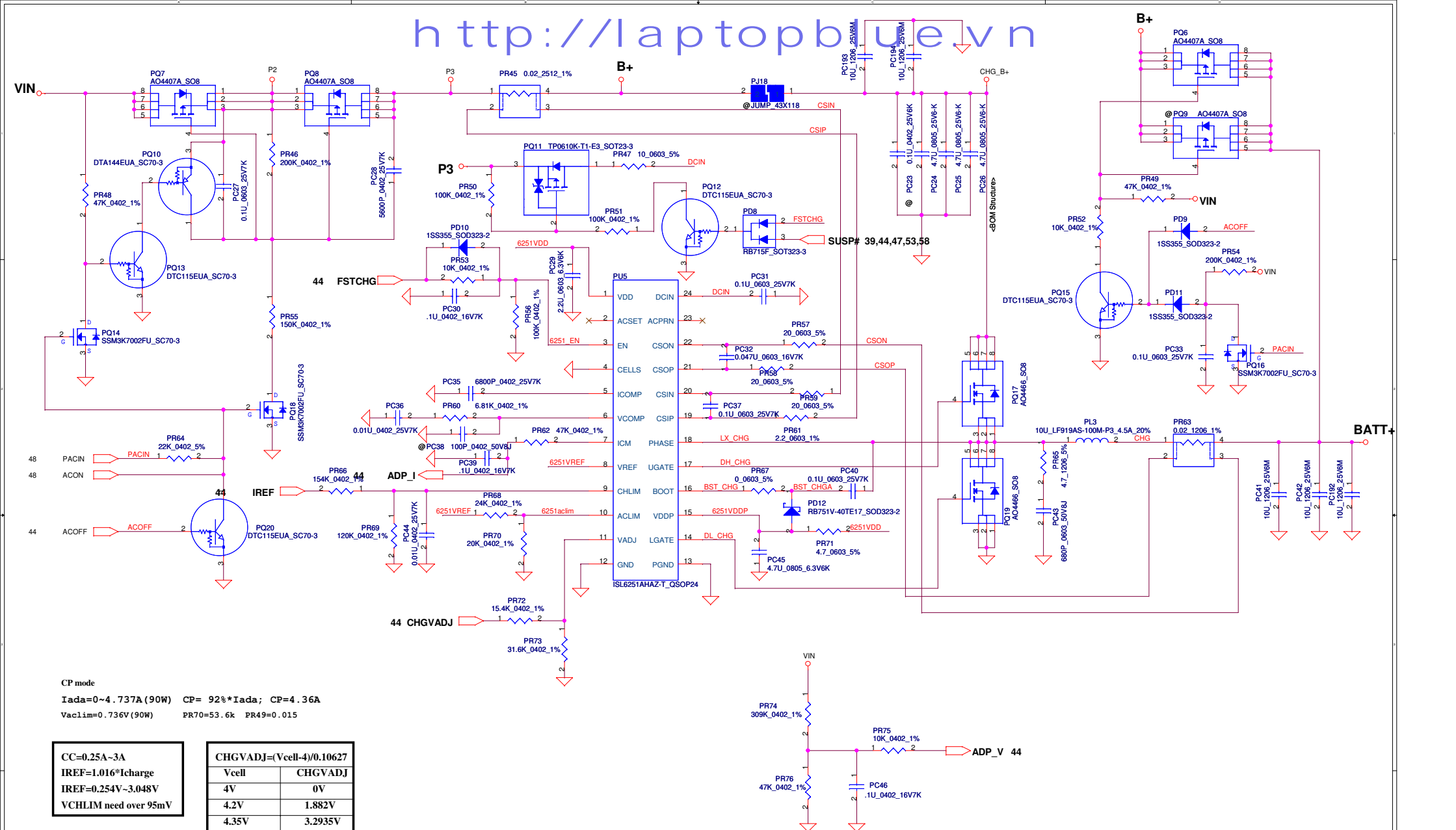
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CPU thermal protection at 95 degree C
Recovery at 56 degree C
```

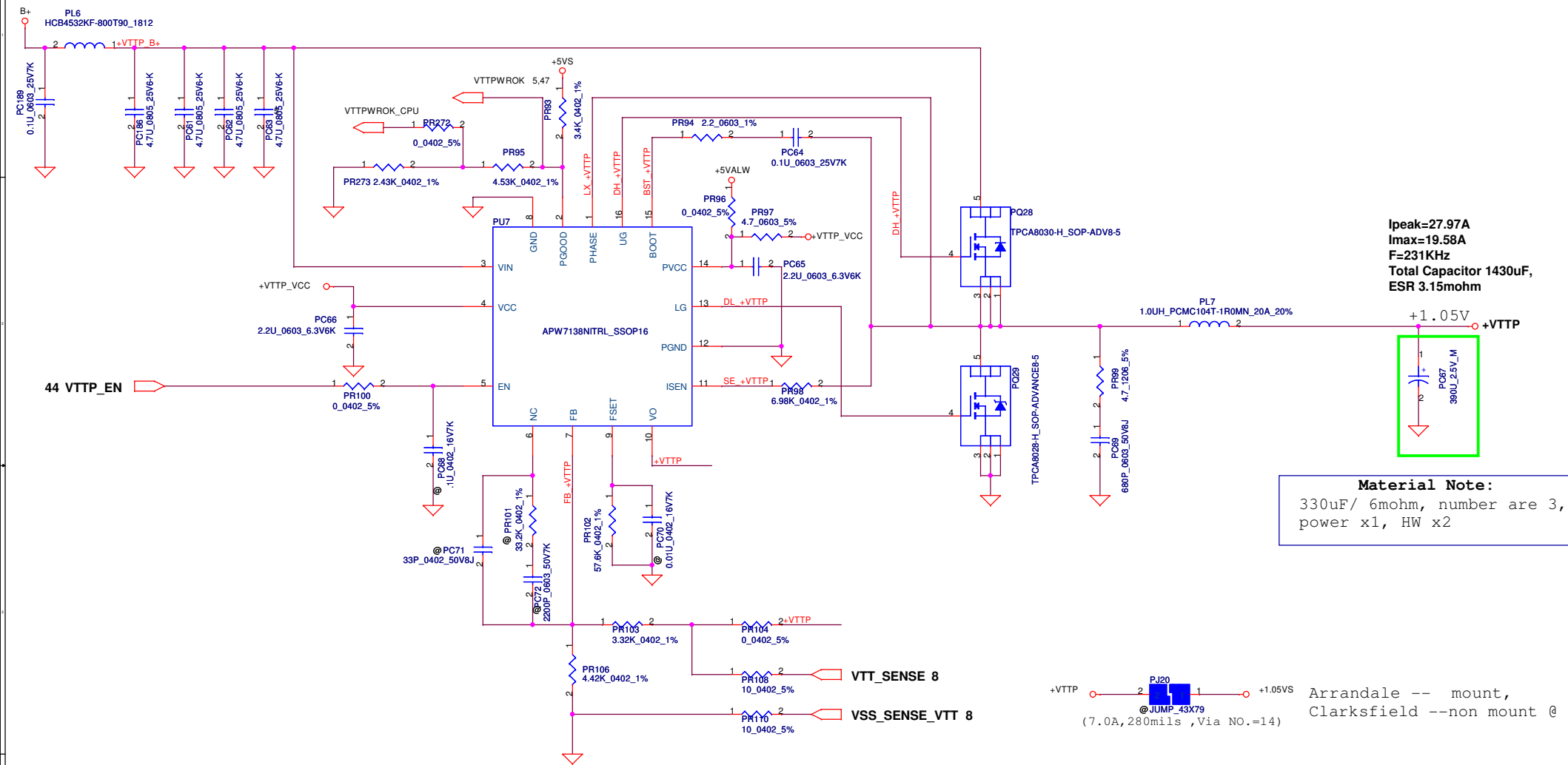
PH2 near main Battery CONN :

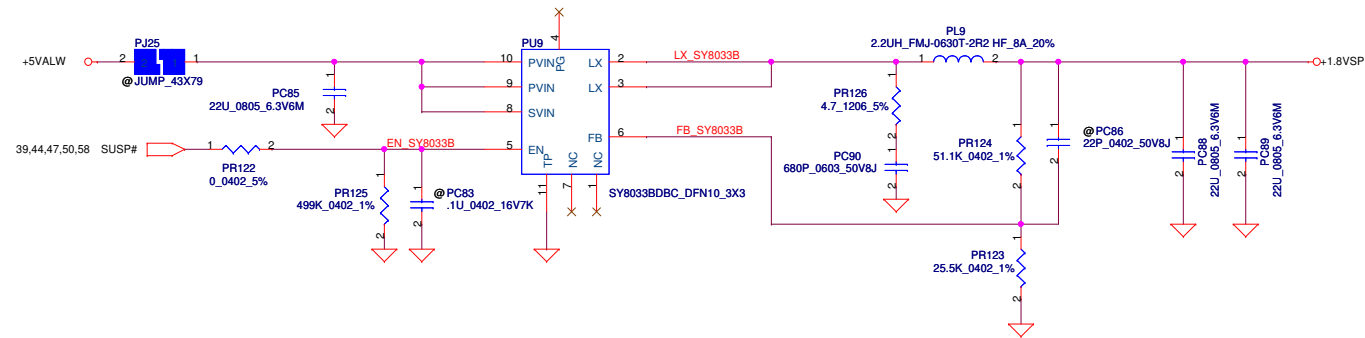
BAT. thermal protection at 95 degree C
Recovery at 48 degree C



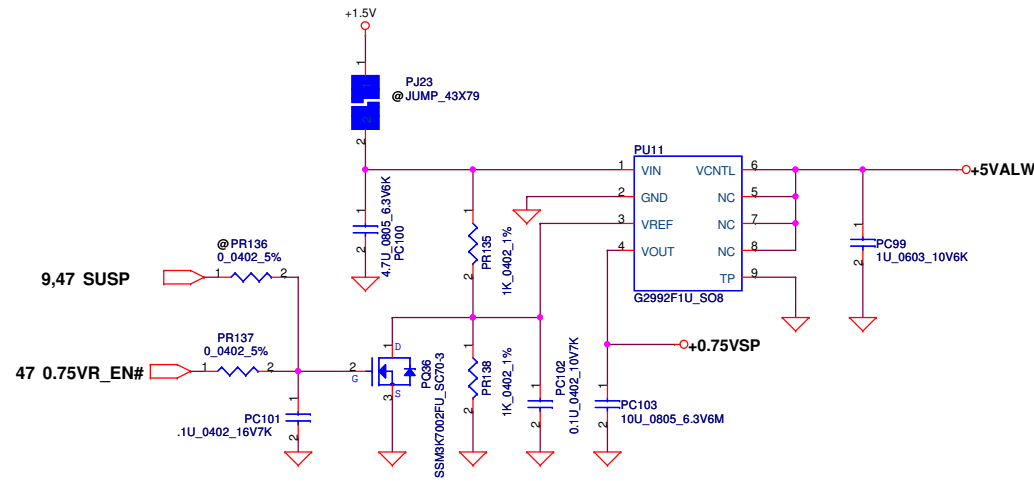
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								Size	Document Number			NBQAA		Rev	1.0
								Date:		Monday, March 22, 2010		ISheet	49	of	61



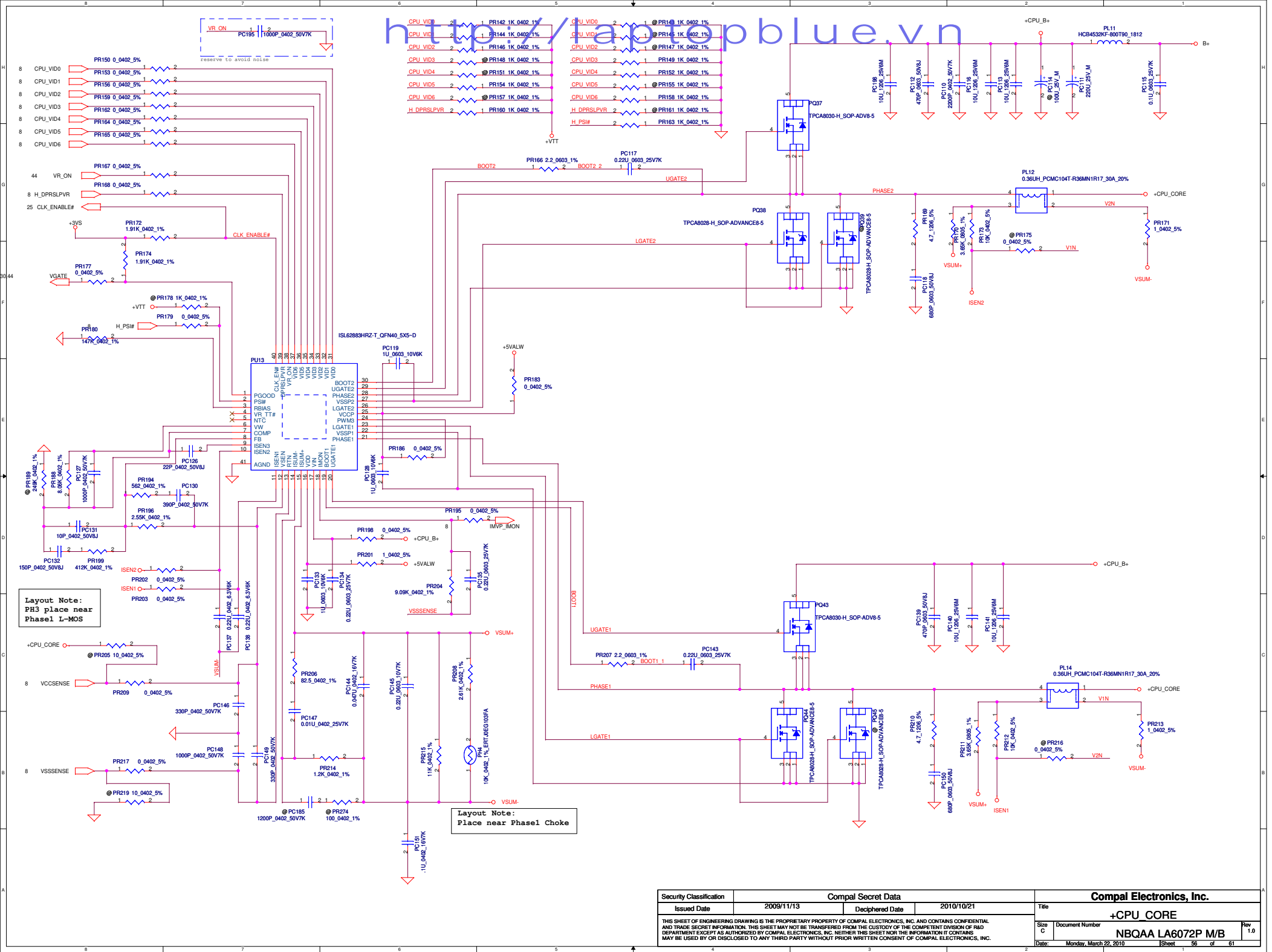


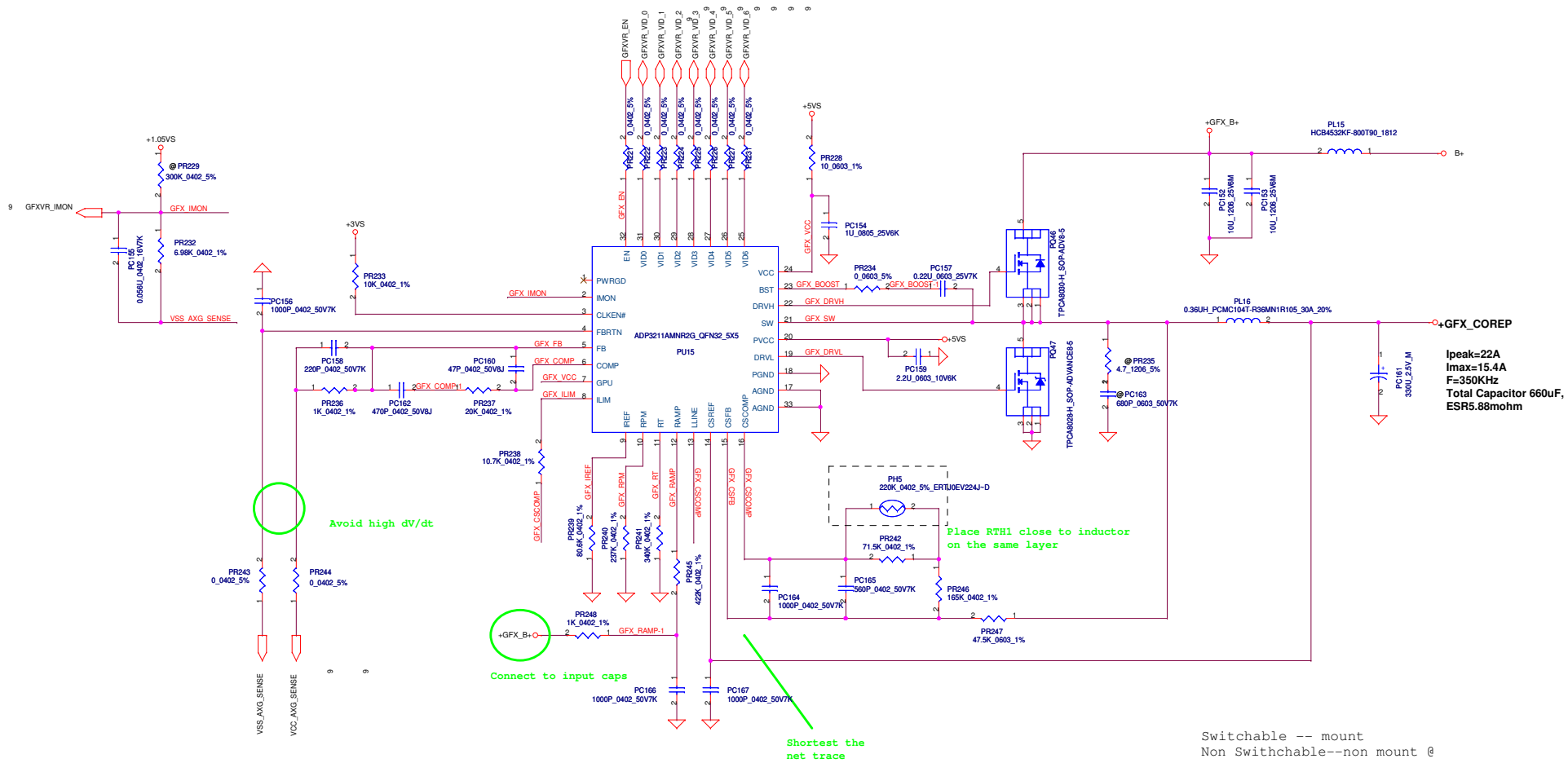


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				1.0	



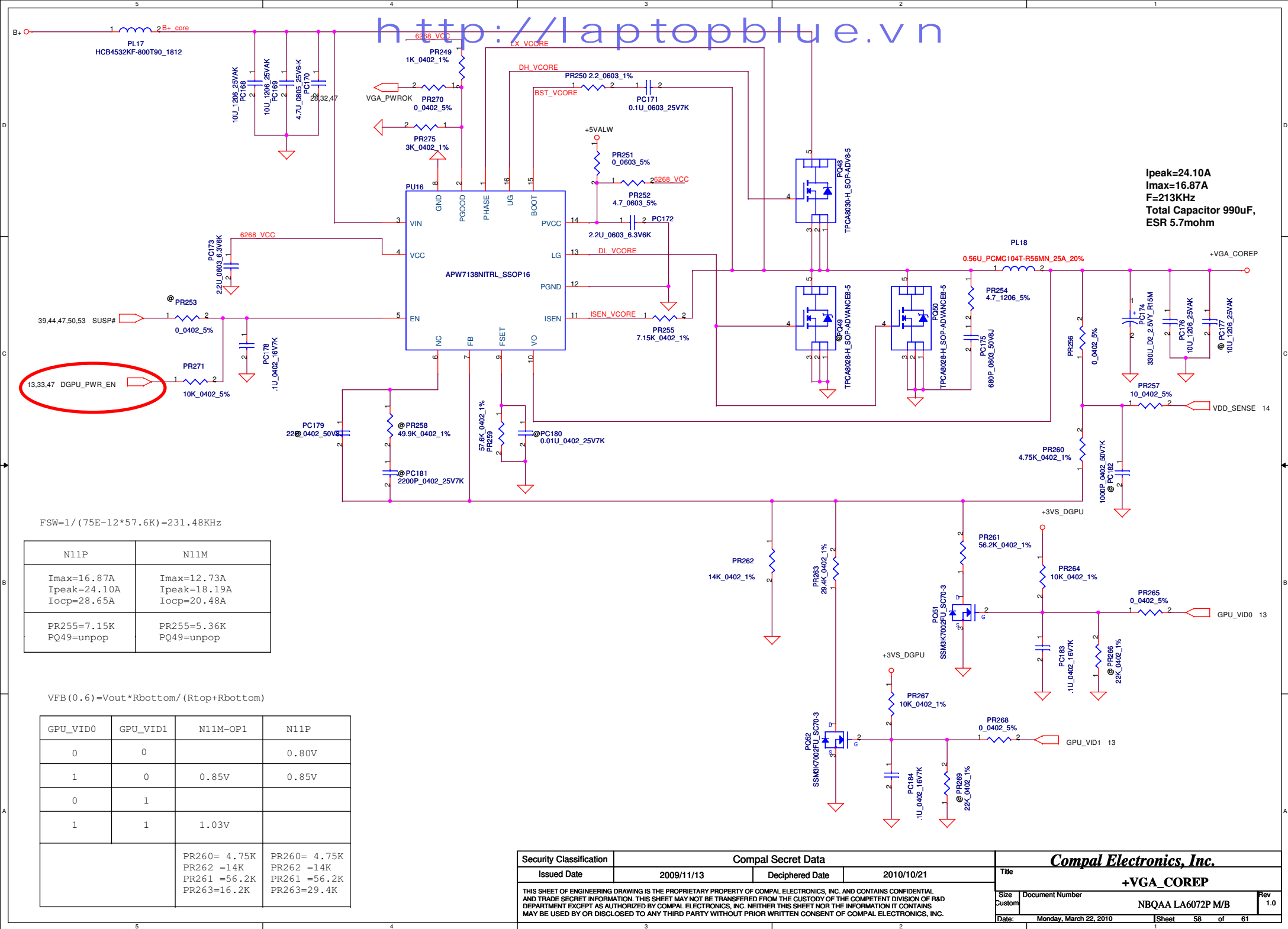
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Ipeak=22A
Imax=15.4A
F=350KHz
Total Capacitor 660uF,
ESR5.88mohm

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Issued Date	2009/11/13	Deciphered Date	2010/10/21	Title +VGA_COREP			
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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
2009/12/06	P48-59	Release		
2009/12/18	P49	PR31,PR33,PR34,PR40		PH1,PH2 setting point change
2009/12/18	P52	PR98		VTT adjust OCP
2009/12/18	P55	Remove PR136,Add PR137,PC101		0.75VSP Enable signal (EVT added by memo)
2009/12/18	P58	Add PR254,PC175		VGA add snubber (EVT added by memo)
2009/12/18	P58	PC174		VGA output cap change to lower
2009/12/28	P51,P52	Add PC188,PC189,PC115		Add EMC,EMI solution.
2009/12/28	P51	change PR83,PR84,Add PR85,PC55		For EMI,EMC solution
2010/01/06	P51	PR81,PR132,PR255		OCP setting.
2010/01/06	P58	change PR249,PR271,PC178		HW request
2010/02/05	P53	change PU9 solution		change 1.8V Solution
2010/02/05	P51	change PL4,PL5		Change to lower height to solve ME request
2010/01/28	P43	PC197		Reserve 10uF at B+ shape for ripple improvement.
2010/02/08	P50	Add PD6,PD7		ESD solution.
2010/02/08	P57	Change PR247		GFX load-line
2010/02/08	P50	Add PC192,PC193,PC194		ISN issue
2010/03/16	P50	Change PR45,PR68		CP setting
2010/03/16	P50	Change PL3		ME issue
2010/03/16	P51	Change PC53,PC54		ME issue
2010/03/16	P53	PR122,PC83 unmount		1.8V enable signal adjust
2010/03/16	P56	Add PC195		VR_ON prevent noise,same as UMA
2010/03/16	P58	Change PC174		ME issue
2010/03/16	P58	Change PR264,PR265,PR267,PR268,PR263,PC184,PQ52		GPU voltage adjust
2010/03/18	P57	Add PC198		High frequency noise
2010/03/22	P58	Add PR275		Adjust VGA POK voltage level for HW request

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PIR (Product Improve Record)
NBQAA LA-6072P SCHEMATIC CHANGE LIST

http://laptopblue.vn

REVISION CHANGE: 0.1 TO 0.2

MODIFICATION LIST				PURPOSE
1.	12/22	25	Change JLVDS routing	To prevent workmanship and burn issue
2.	12/22	09	Change Q33 routing	For common design
3.	12/22	47	Change Q43 routing	For common design
4.	12/22	39	Change JEXP footprint to SANTA_130861-2_26P_RT-T	Modify footprint
5.	12/22	38	Change JTPL footprint to P-TWO_161021-06021_6P-T	For ME's request
6.	12/22	43	Change JKBL footprint to ACES_85201-04051_4P-T	For ME's request
7.	12/22	13	Delete DV2, Add RV124, QV2 for CLKREQ_VGA#	CLKREQ_VGA# circuit for NV's Optimus
8.	12/23	38	Change JCS footprint to P-TWO_161021-10021_10P-T	For ME's request
9.	12/23	38	Change JTOUCH footprint to P-TWO_161021-10021_10P-T	For ME's request
10.	12/23	33	Change PCF's GPIO57 netname to OPTIMUS_EN# and pull down to GND	For BIOS recognizing Optimus
11.	12/23	33	Change PCF's GPIO45 netname to LVDS_SEL	For Common design
12.	12/23	33	Change PCF's GPIO39 netname to CIR_EN#	For Common design
13.	12/24	39	Add DM2, QM1, BT_CTRL on JWLAN.5	For WLAN/BT combo module
14.	12/24	42	Add RA43 on EC_MUTE#	For Audio issue
15.	12/24	43	Detele JEXMIC.5 from GND	For Audio issue
16.	12/24	44	Change PWRME_CTRL to PWRME_CTRL#	Active low signal
17.	12/24	33	Delete GND guide pins of JTOUCH, JCS, JTPL, JODD1	For common design
18.	12/29	29	Add C254 on CLKREQ_WLAN#	For EMI's Request
19.	12/29	43	Exchange JKBL pin1 and pin4	To meet correct footprint
20.	12/29	37	Add C389 on U14	For EMI's Request
21.	12/29	46	Add C392 on H21 for +5VALW	For EMI's Request
22.	12/29	40	Stuff CL7, CL23, CL24	For EMI's Request
23.	12/29	46	Add C393, close to C7 for +3VS	For EMI's Request
24.	12/29	32	Add R55 on DGPU_RST#	For common design
25.	12/29	27	Add R314 on HDMI_HPD and U9	To prevent ESD damage to U9
26.	01/03	47	change +1.05VS_DGPU routing	To turn on/off normally

REVISION CHANGE: 0.2 TO 0.3

MODIFICATION LIST				PURPOSE
1.	02/01	31	Change RA40 to pull up +5VL	Support S/M function in battery mode
2.	02/01	30	Change RA34 to pull up +3VL	Support S/M function in battery mode
3.	02/01	44	Add R103 to USB_EN# and pull up +5VALW	For common code with NWQAA
4.	02/01	44	Add R69 to VR_ON and pull low to GND	To avoid folating when EC is on initial
5.	02/01	30	Add C434 to VGATE	Reserve to avoid noise
6.	02/01	05	Add C482 to H_PWRGOOD	Reserve to avoid noise
7.	02/01	40	Add UL4	for 10/100/1000 transformer co-layout
8.	02/01	38	Add MDC circuits	For A51's request, Add MDC in DIS SKU
9.	02/01	35	Reserve U54 for +1.5VALW LDO and change VCCSUSHDA power rail	For MDC design change
10.	02/01	28	Add R287, R289, R291, R293 for Azalia bus to MDC	For MDC design change
11.	02/02	46	Add H31, H32	For MDC design change
12.	02/02	44	Add CAP_RST# on EC pin73 and link to JCS	For Cap sensor design change
13.	02/04	31	Stuff R133, R135 to 100Kohm PD GND	To prevent PCH pending internal HPD
14.	02/04	14	Reserve UV4, RV54, CV56, RV44	Reserved for VBIOs
15.	02/04	42	Add RA45, un-stuff RA43	To solve audio issue
16.	02/06	32	Exchange USB port 4&8	Design change, for A51's request
17.	02/08	08	Change C117,C118,C119,C120,C127,C128,C129	To improve ESD
18.	02/08	40	Change LL1, CL13	For design change
19.	02/09	41	Change RC7, RC8, RC9, RC12, RC13, RC14 from 0 ohm to 22 ohm	For EMI's request

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NBQAA LA-6072P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.3 TO 1.0

NO DATE PAGE MODIFICATION LIST				PURPOSE
1.	03/11	27	Add R148	To solve display compatibility issue
3.	03/11	15	Change CV58 from OSCON to POLY type	Due to the keyboard stress test is fail
4.	03/11	09	Change C216 from OSCON to POLY type	Due to the keyboard stress test is fail
5.	03/11	11	Change C163 from OSCON to POLY type	Due to the keyboard stress test is fail
6.	03/11	14	Delete UV4, RV54, CV56, RV44	Design change, no need extra BIOS ROM
7.	03/11	25	Stuff D84, D82, D19, D83	For ESD's request
8.	03/11	34	Change L12 from bead to R389 2.2 ohm+- 1%	For CRT issue
9.	03/14	13	Reserve YV1, RV29, CV45, CV46	Reserved for design change
10.	03/14	33	Change R221 to 1K ohm	For NV's Optimus sequence
11.	03/14	32	Change R55 to 1K ohm	For NV's Optimus sequence
12.	03/14	32	Reserve R334, add R336	For NV's Optimus sequence
13.	03/14	39	Change QM1 to Q14B	For cost down
14.	03/15	42	Un-mount CA16	For audio noise issue
15.	03/15	46	Un-mount SW2, SW3	Power button is no need after pre-MP
16.	03/16	42	Change CA12.1, RA12.2, CA18.2 from GND to AGND	For audio noise issue
17.	03/16	42	Change CA9 and CA10 to from 4700pF tp 1uF	For audio noise issue
18.	03/16	42	Add CA34-CA40 and CA51	For audio noise issue
19.	03/18	41	Change Card reader solution from 02 to JMB389C/385C	For design change
20.	03/19	27	Add D54	For HDMI CEC
21.	03/19	34	Add L12 that reserved 0 ohm for EMI	For CRT issue
22.	03/19	46	H22 from 6.0 to 3.0	For ME's request
23.	03/20	20	Change BIOS ROM footprint to M25P80-VMW6TP_S08	No need the debug connector in MP phase
24.	03/22	13	Stuff RV28, un-stuff RV105	Reserved for 27M_SSC from clock gen
25.	03/22	43	Add RA22, RA23	Reserved to solve GPRS noise
26.	03/22	05	Stuff C482	To avoid noise
27.	03/22	30	Stuff C434	To avoid noise