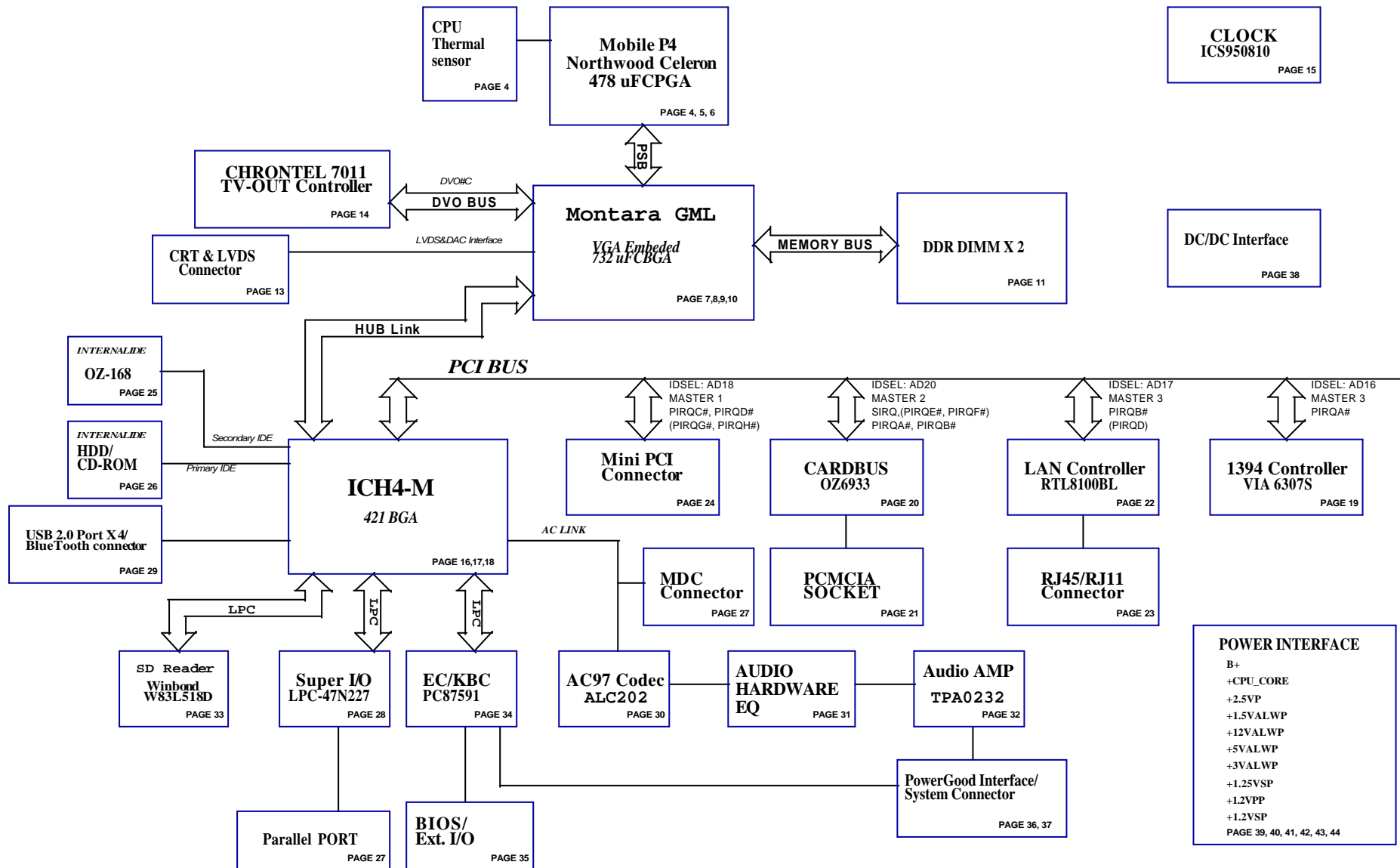


# **LA-1641 REV0.2 Schematic Document**

Intel Mobile P4 uFCBGA/uFCPGA Northwood Celeron  
with Montara GML / ICH4-M / Integrated VGA

2002-11-20

<b>Compal Electronics, Ltd.</b>			
Title			
Cover Page			
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## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A
+CPU_VCC	Core voltage for CPU	ON	OFF	OFF
+1.2VP	1.2V switched power rail for CPU AGTLBus	ON	OFF	OFF
+1.2VS	1.2V switched power rail for Montara core	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	AGP 4X	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD20	2	PIRQA/PIRQB(PIRQE/PIRQF)
LAN	AD17	3	PIRQB(PIRQD)
Mini-PCI	AD18	1/1	PIRQC/PIRQD(PIRQG/PIRQH)
1394	AD16	0	PIRQA

## EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 110X b
EEPROM(24C16/02)	1010 000X b	OZ168	0011 0100 b
(24C04)	1011 000Xb	Smart Battery	0001 011X b
		Docking	0011 011X b
		DOT Board	XXXX XXXXb

## ICH4 SM Bus address

Device	Address
Clock Generator (ICS-950810)	1101 001X

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	0.6
6	0.7
7	0.8

## Sapporo Z to ZJ BOM modify list :

- 1.Remove R594
- 2.Add R112

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Note List			
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Mobile  
NorthWood

7 HA# [3..31] HA# [3..31]

- HA#3 K2
- HA#4 L6
- HA#5 K1
- HA#6 M6
- HA#7 L3
- HA#8 M6
- HA#9 L2
- HA#10 M3
- HA#11 M4
- HA#12 N1
- HA#13 M1
- HA#14 N2
- HA#15 N4
- HA#16 N5
- HA#17 T1
- HA#18 R2
- HA#19 P8
- HA#20 R4
- HA#21 R3
- HA#22 T2
- HA#23 U1
- HA#24 F6
- HA#25 U3
- HA#26 U4
- HA#27 V2
- HA#28 R6
- HA#29 W1
- HA#30 T5
- HA#31 U4

7 HREQ# [0..4] HREQ# [0..4]

- HREQ#0 J1
- HREQ#1 K5
- HREQ#2 J4
- HREQ#3 J3
- HREQ#4 G1

7 H\_ADS# H\_ADS#

+CPU\_CORE R91 Close to U37 pinM23

R53 56 0402 5%

7 H\_BREQ# H\_BREQ#

7 H\_BNR# H\_BNR#

7 H\_LOCK# H\_LOCK#

15 CLK\_CPU\_BCLK# CLK\_CPU\_BCLK#

15 CLK\_CPU\_BCLK# CLK\_CPU\_BCLK#

7 H\_HIT# H\_HIT#

7 H\_HITM# H\_HITM#

7 H\_DEFER# H\_DEFER#

AP#0

AP#1

BI#0

BI#1

BI#2

BI#3

BI#4

BI#5

BI#6

BI#7

BI#8

BI#9

BI#10

BI#11

BI#12

BI#13

BI#14

BI#15

BI#16

BI#17

BI#18

BI#19

BI#20

BI#21

BI#22

BI#23

BI#24

BI#25

BI#26

BI#27

BI#28

BI#29

BI#30

BI#31

BI#32

BI#33

BI#34

BI#35

REQ#0

REQ#1

REQ#2

REQ#3

REQ#4

REQ#5

REQ#6

REQ#7

REQ#8

REQ#9

REQ#10

REQ#11

REQ#12

REQ#13

REQ#14

REQ#15

REQ#16

REQ#17

REQ#18

REQ#19

REQ#20

REQ#21

REQ#22

REQ#23

REQ#24

REQ#25

REQ#26

REQ#27

REQ#28

REQ#29

REQ#30

REQ#31

REQ#32

REQ#33

REQ#34

REQ#35

REQ#36

REQ#37

AP#0

AP#1

BI#0

BI#1

BI#2

BI#3

BI#4

BI#5

BI#6

BI#7

BI#8

BI#9

BI#10

BI#11

BI#12

BI#13

BI#14

BI#15

BI#16

BI#17

BI#18

BI#19

BI#20

BI#21

BI#22

BI#23

BI#24

BI#25

BI#26

BI#27

BI#28

BI#29

BI#30

BI#31

BI#32

BI#33

BI#34

BI#35

REQ#0

REQ#1

REQ#2

REQ#3

REQ#4

REQ#5

REQ#6

REQ#7

REQ#8

REQ#9

REQ#10

REQ#11

REQ#12

REQ#13

REQ#14

REQ#15

REQ#16

REQ#17

REQ#18

REQ#19

REQ#20

REQ#21

REQ#22

REQ#23

REQ#24

REQ#25

REQ#26

REQ#27

REQ#28

REQ#29

REQ#30

REQ#31

REQ#32

REQ#33

REQ#34

REQ#35

REQ#36

REQ#37

AP#0

AP#1

BI#0

BI#1

BI#2

BI#3

BI#4

BI#5

BI#6

BI#7

BI#8

BI#9

BI#10

BI#11

BI#12

BI#13

BI#14

BI#15

BI#16

BI#17

BI#18

BI#19

BI#20

BI#21

BI#22

BI#23

BI#24

BI#25

BI#26

BI#27

BI#28

BI#29

BI#30

BI#31

BI#32

BI#33

BI#34

BI#35

REQ#0

REQ#1

REQ#2

REQ#3

REQ#4

REQ#5

REQ#6

REQ#7

REQ#8

REQ#9

REQ#10

REQ#11

REQ#12

REQ#13

REQ#14

REQ#15

REQ#16

REQ#17

REQ#18

REQ#19

REQ#20

REQ#21

REQ#22

REQ#23

REQ#24

REQ#25

REQ#26

REQ#27

REQ#28

REQ#29

REQ#30

REQ#31

REQ#32

REQ#33

REQ#34

REQ#35

REQ#36

REQ#37

AP#0

AP#1

BI#0

BI#1

BI#2

BI#3

BI#4

BI#5

BI#6

BI#7

BI#8

BI#9

BI#10

BI#11

BI#12

BI#13

BI#14

BI#15

BI#16

BI#17

BI#18

BI#19

BI#20

BI#21

BI#22

BI#23

BI#24

BI#25

BI#26

BI#27

BI#28

BI#29

BI#30

BI#31

BI#32

BI#33

BI#34

BI#35

REQ#0

REQ#1

REQ#2

REQ#3

REQ#4

REQ#5

REQ#6

REQ#7

REQ#8

REQ#9

REQ#10

REQ#11

REQ#12

REQ#13

REQ#14

REQ#15

REQ#16

REQ#17

REQ#18

REQ#19

REQ#20

REQ#21

REQ#22

REQ#23

REQ#24

REQ#25

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REQ#28

REQ#29

REQ#30

REQ#31

REQ#32

REQ#33

REQ#34

REQ#35

REQ#36

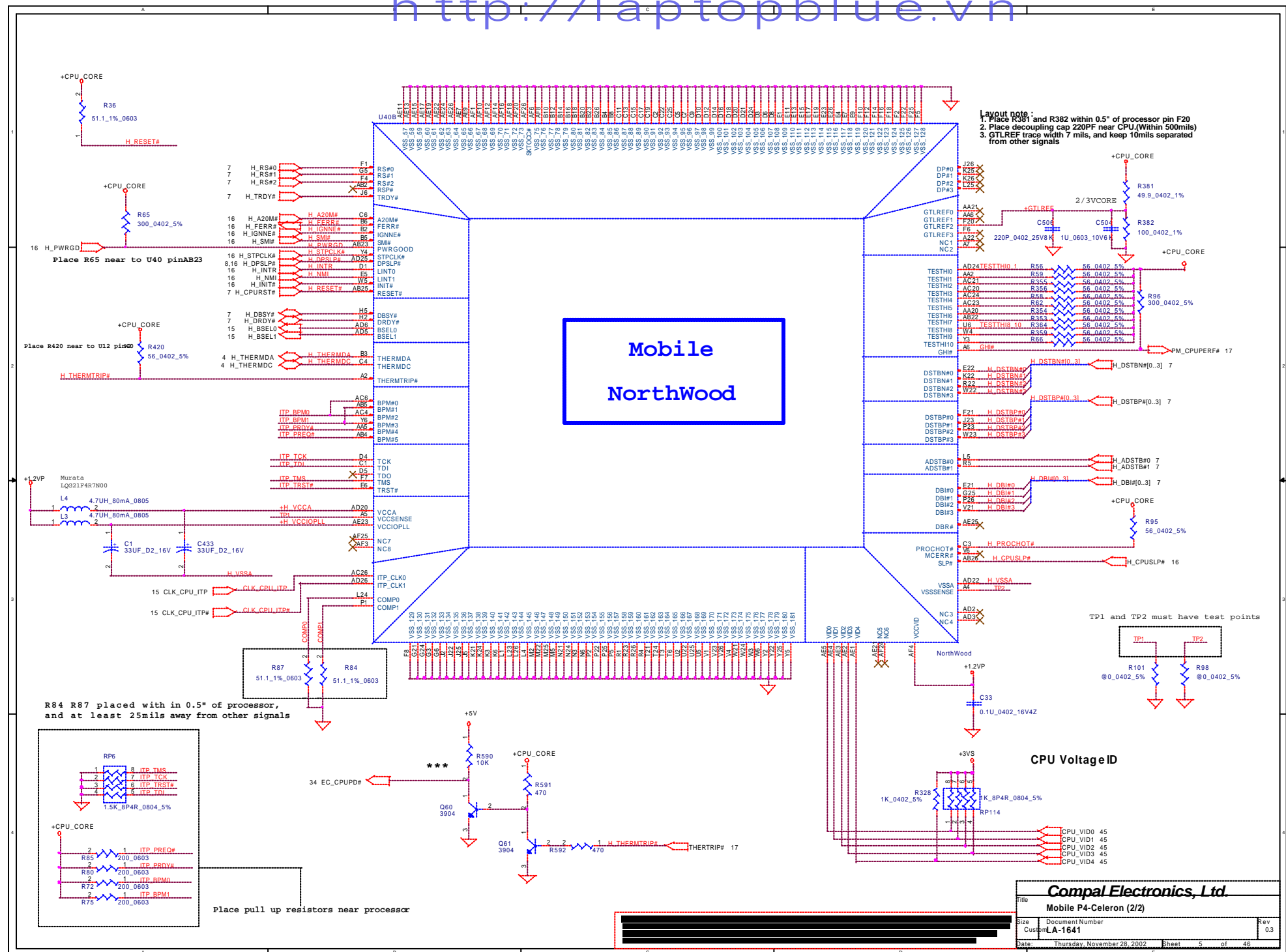
REQ#37

AP#0

AP#1

BI#0

BI#1



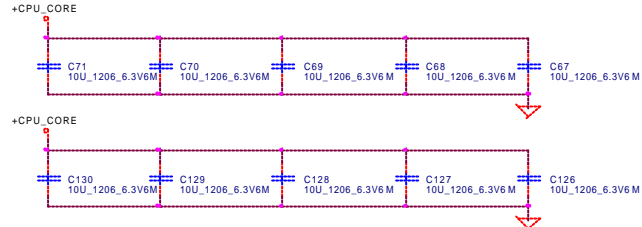
**Layout note :**

Place close to CPU, Use 2-3 vias per PAD.  
Place .22uF caps underneath balls on solder side.  
Place 10uF caps on the peripheral near balls.  
Use 2-3 vias per PAD.

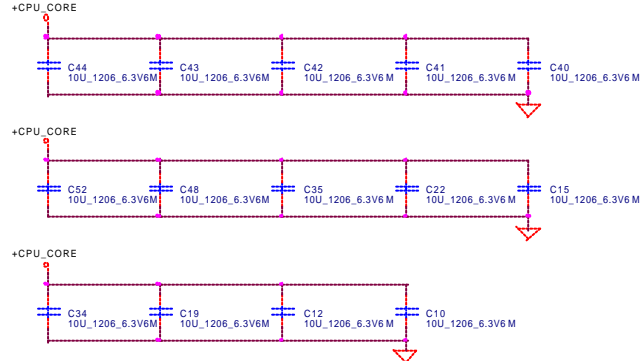
**Layout note :**

Place close to CPU power and ground pin as possible (<1inch)

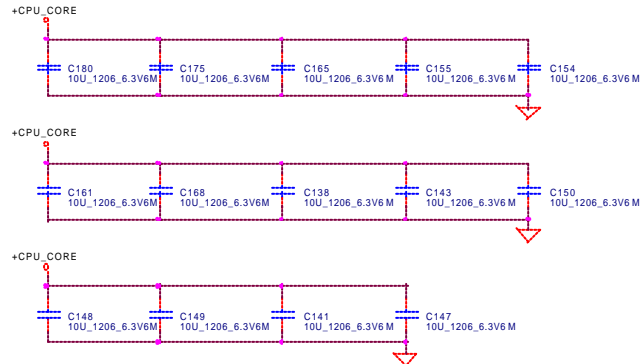
**Please place these cap in the socket cavity area**



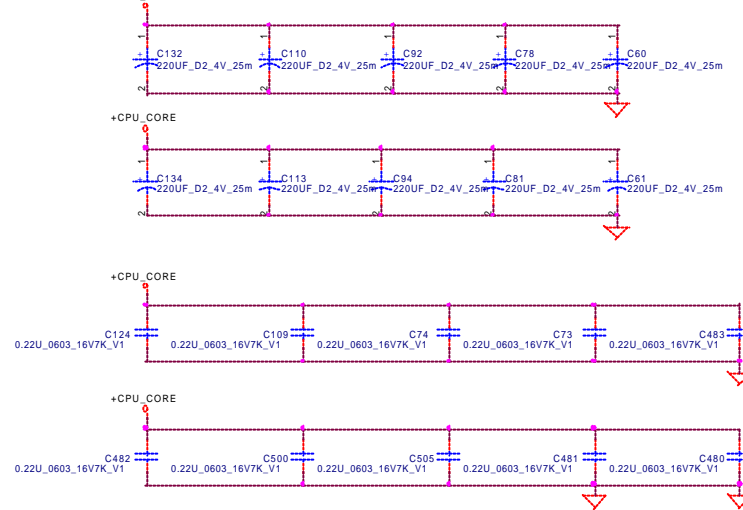
**Please place these cap on the socket north side**

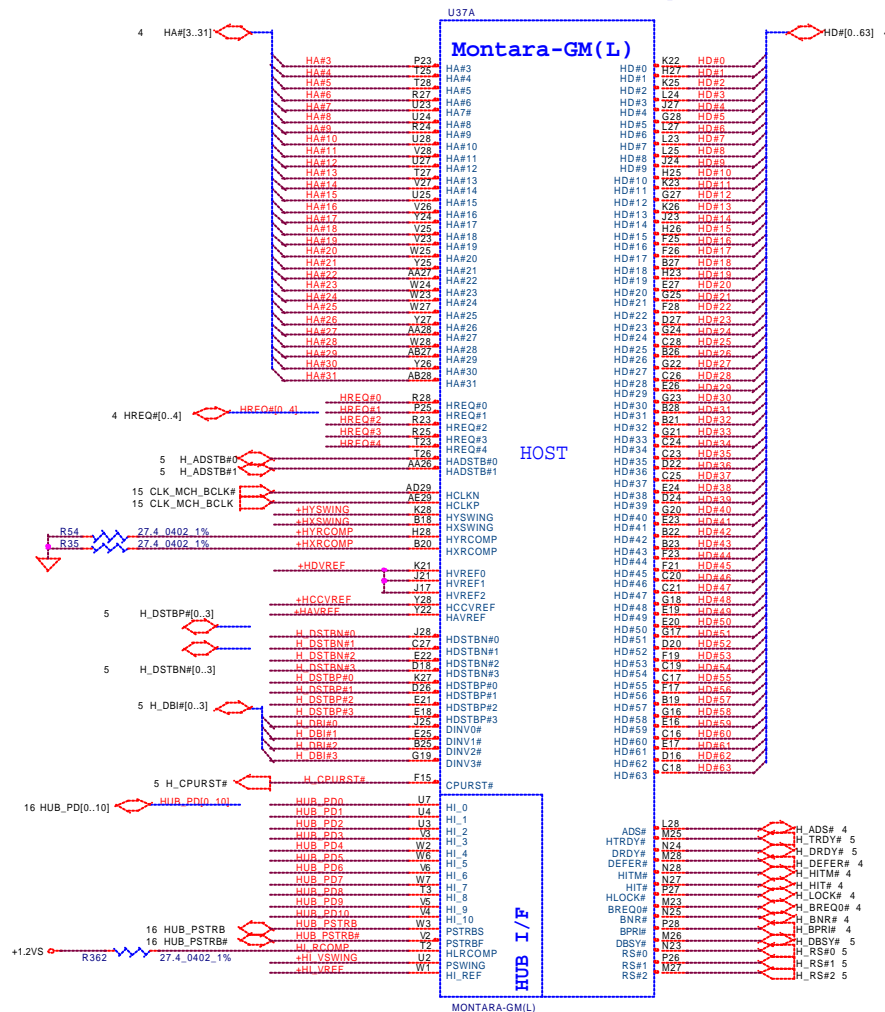


**Please place these cap on the socket south side**



**Used ESR 25m ohm cap total ESR=2.5m ohm**

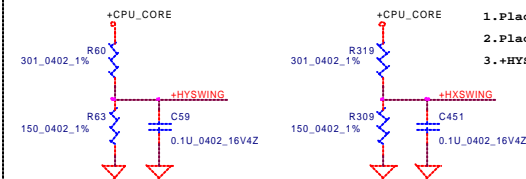




**Layout Note:**

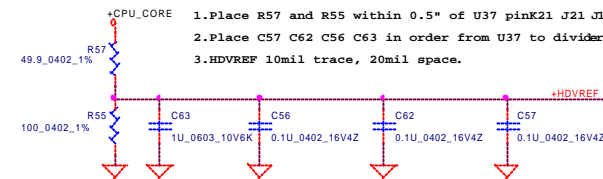
1. Place R35 and R54 within 0.5" of U37 pinH28 B20
2. Both HYRCOMP and HXRCOMP trace width are 18mil and 25mils away from other signals

**HXSWING and HYSWING Ref. Voltage**



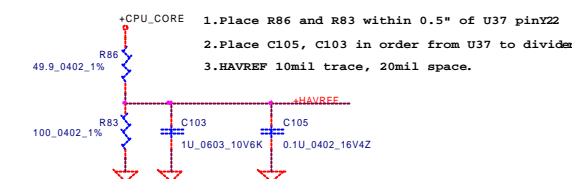
1. Place R60 and R63 within 0.5" of U37 pinK28
2. Place R319 and R309 within 0.5" of U37 pinB18
3. +HYSWING, +HXSWING 10mil trace, 20mil space.

**Host data Ref. Voltage**



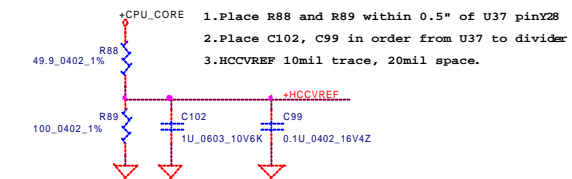
1. Place R57 and R55 within 0.5" of U37 pinK21 J21 J17
2. Place C57 C62 C56 C63 in order from U37 to divider
3. HDVREF 10mil trace, 20mil space.

**Host address Ref. Voltage**



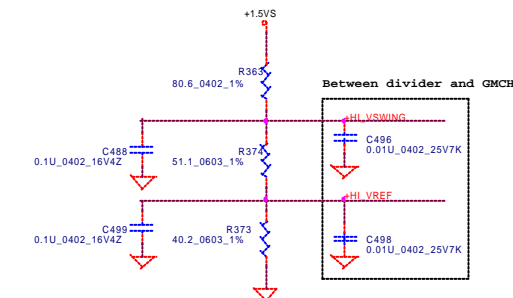
1. Place R86 and R83 within 0.5" of U37 pinY22
2. Place C105, C103 in order from U37 to divider
3. HAVREF 10mil trace, 20mil space.

**Host common clock Ref. Voltage**

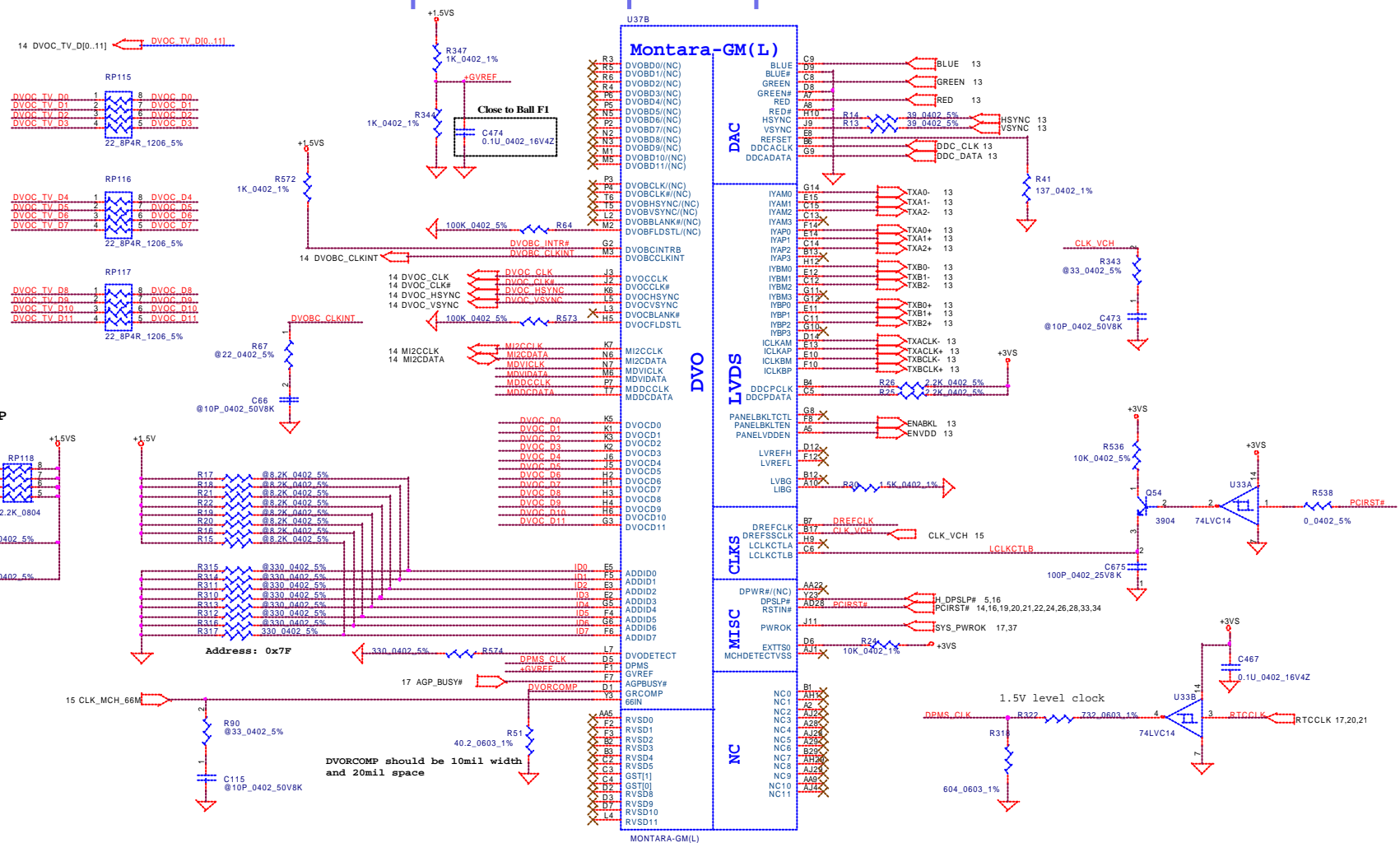


1. Place R88 and R89 within 0.5" of U37 pinY28
2. Place C102, C99 in order from U37 to divider
3. HCCVREF 10mil trace, 20mil space.

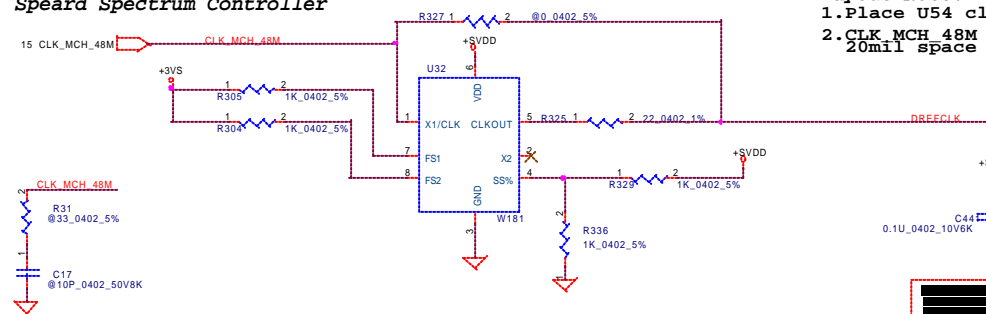
**HUB I/F REF VOLTAGE**



Place this schematic close to GMCH

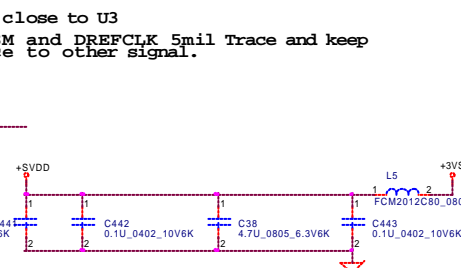


## Speard Spectrum Controller



**Layout Note:**

- 1.Place U54 close to U3
- 2.CLK\_MCH\_48M and DREFCLK 5mil Trace and keep 20mil space to other signal.

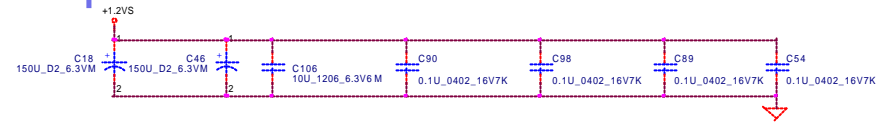
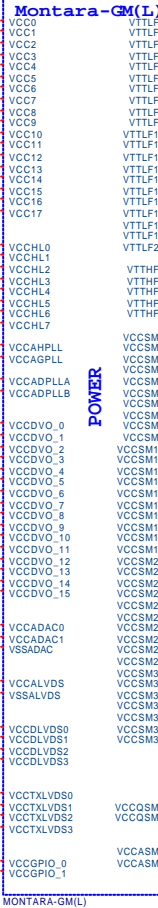




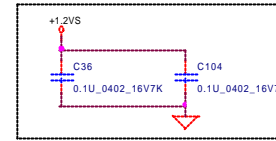
# Montara-GM(L)

## Montara-GM(L)

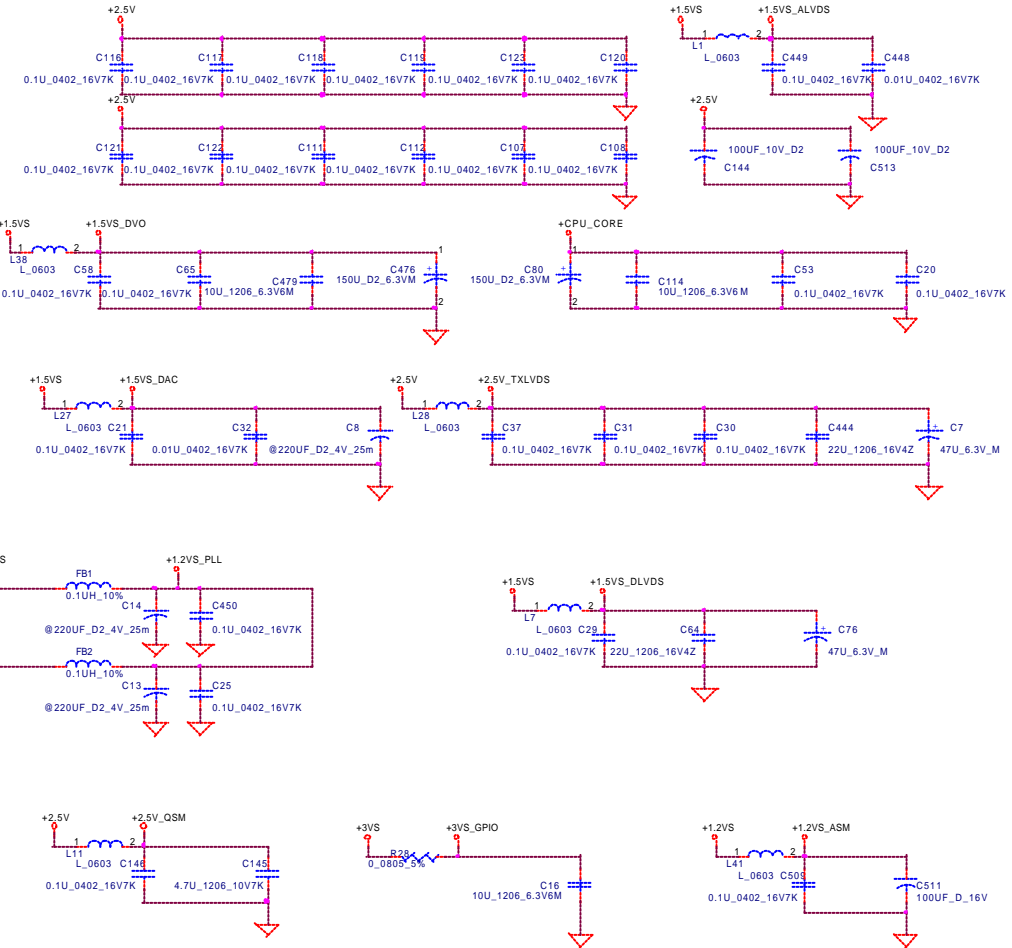
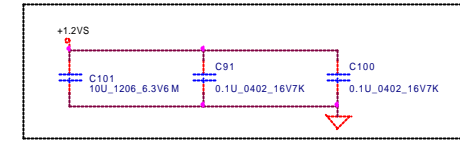
### POWER



One close to D29, one close to Y2



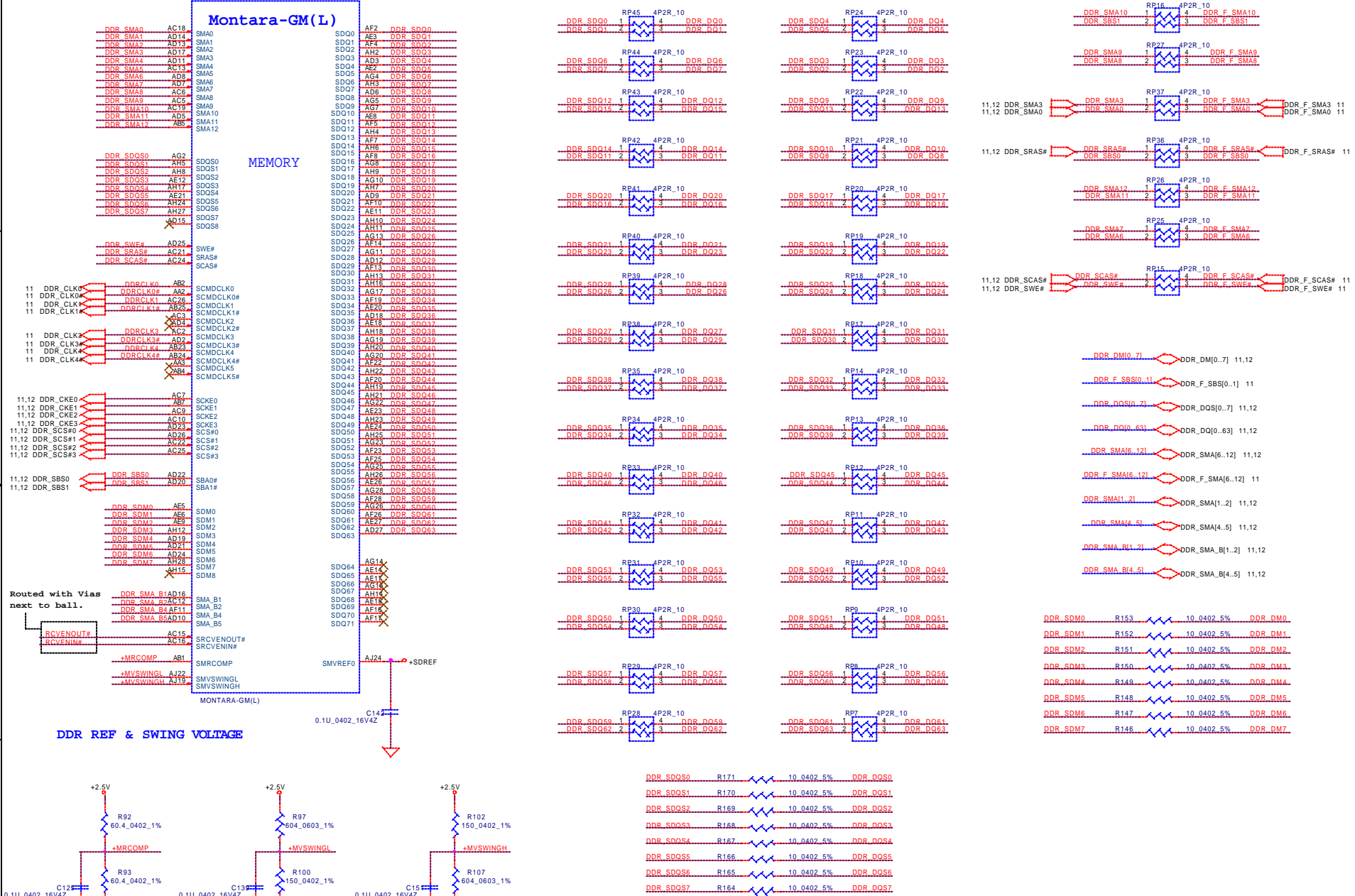
Close to VCCHL0-7



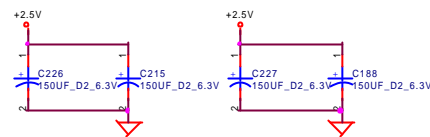
U37C

### Montara-GM(L)

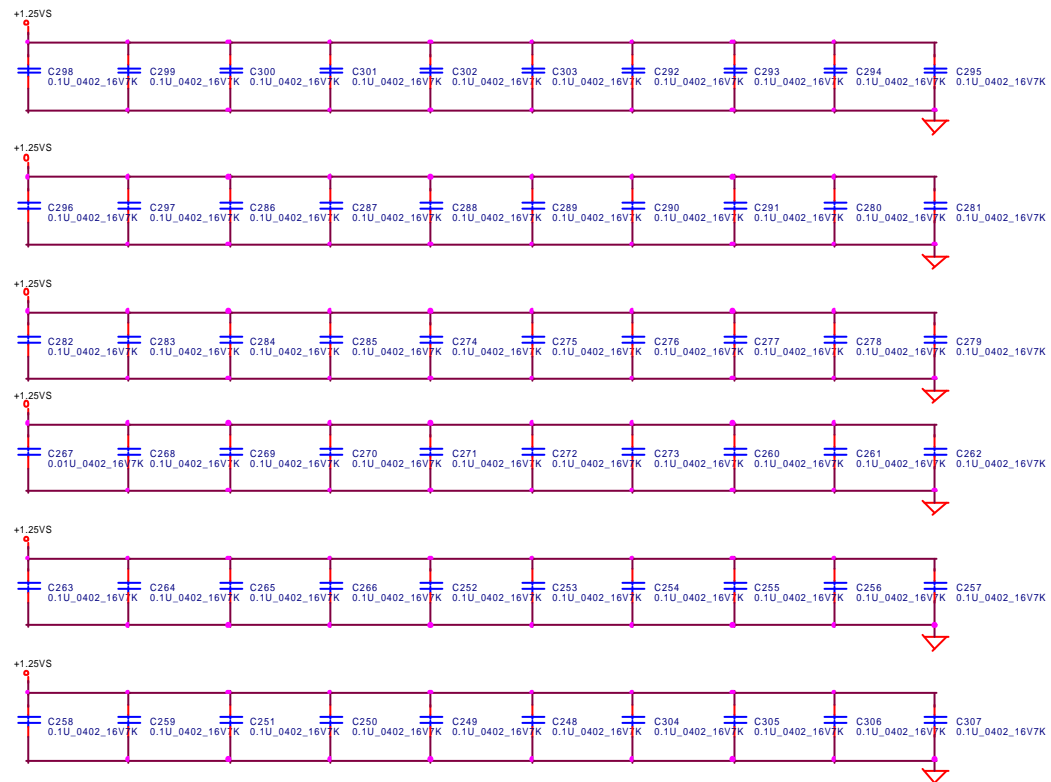
### MEMORY

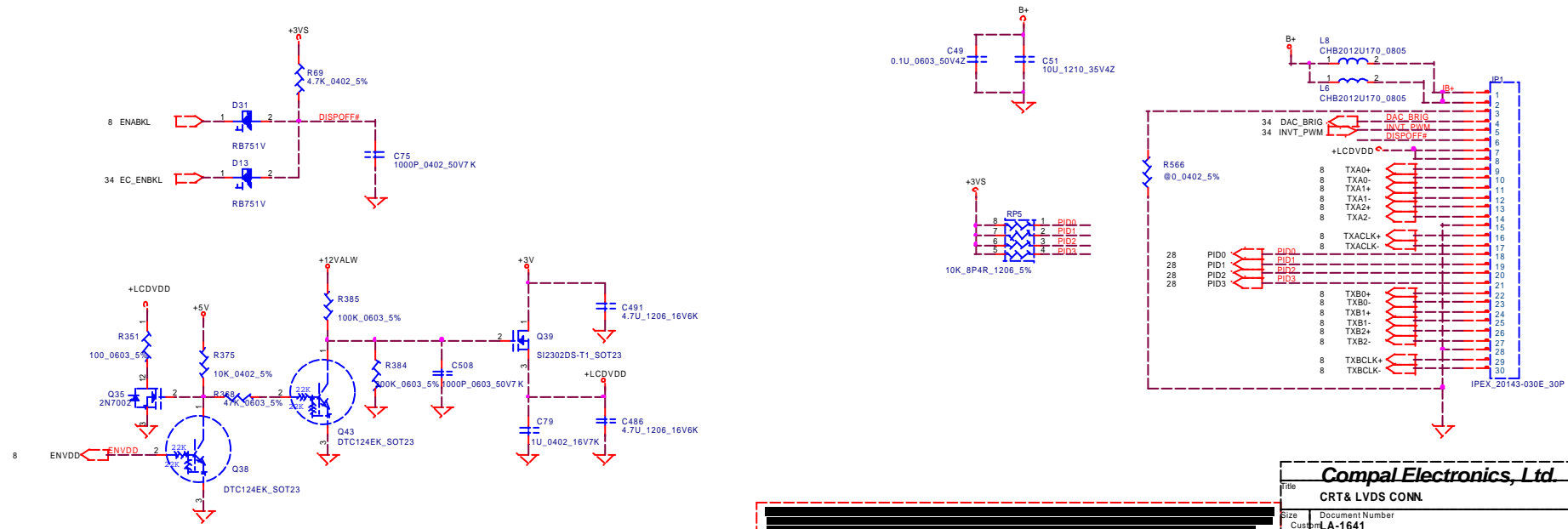
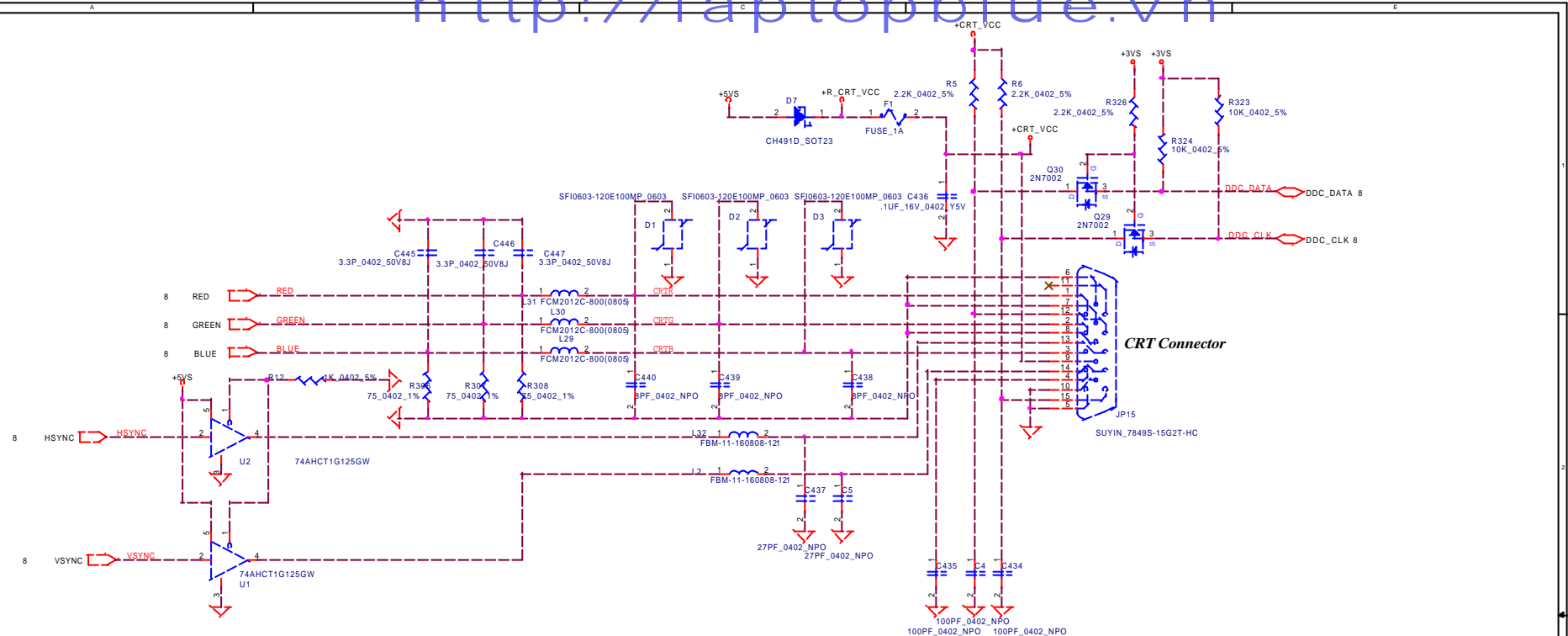


DIMM1  
Bottom Side



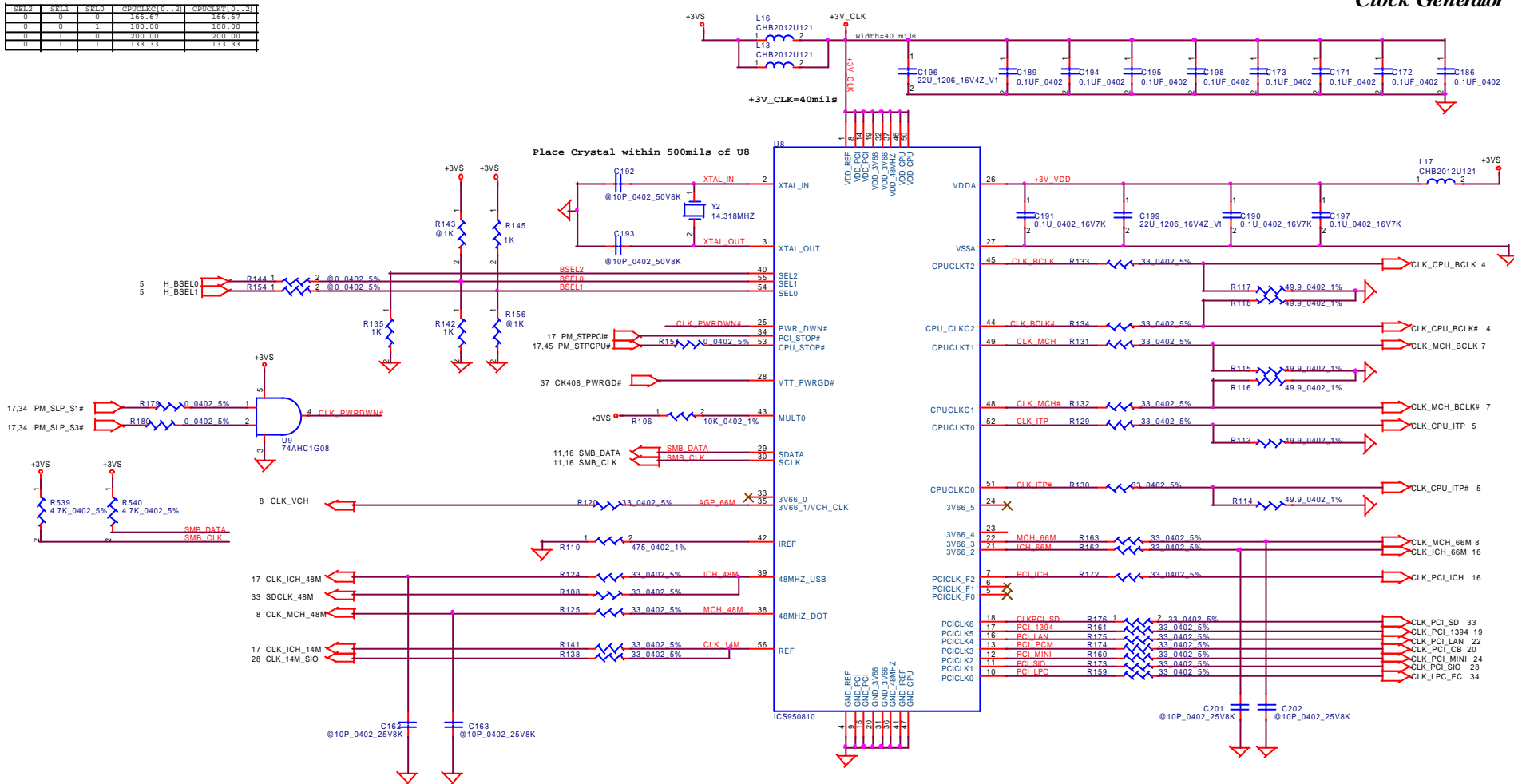
**Layout note :**  
Place one cap close to every 2 pull up resistors termination to +1.25V



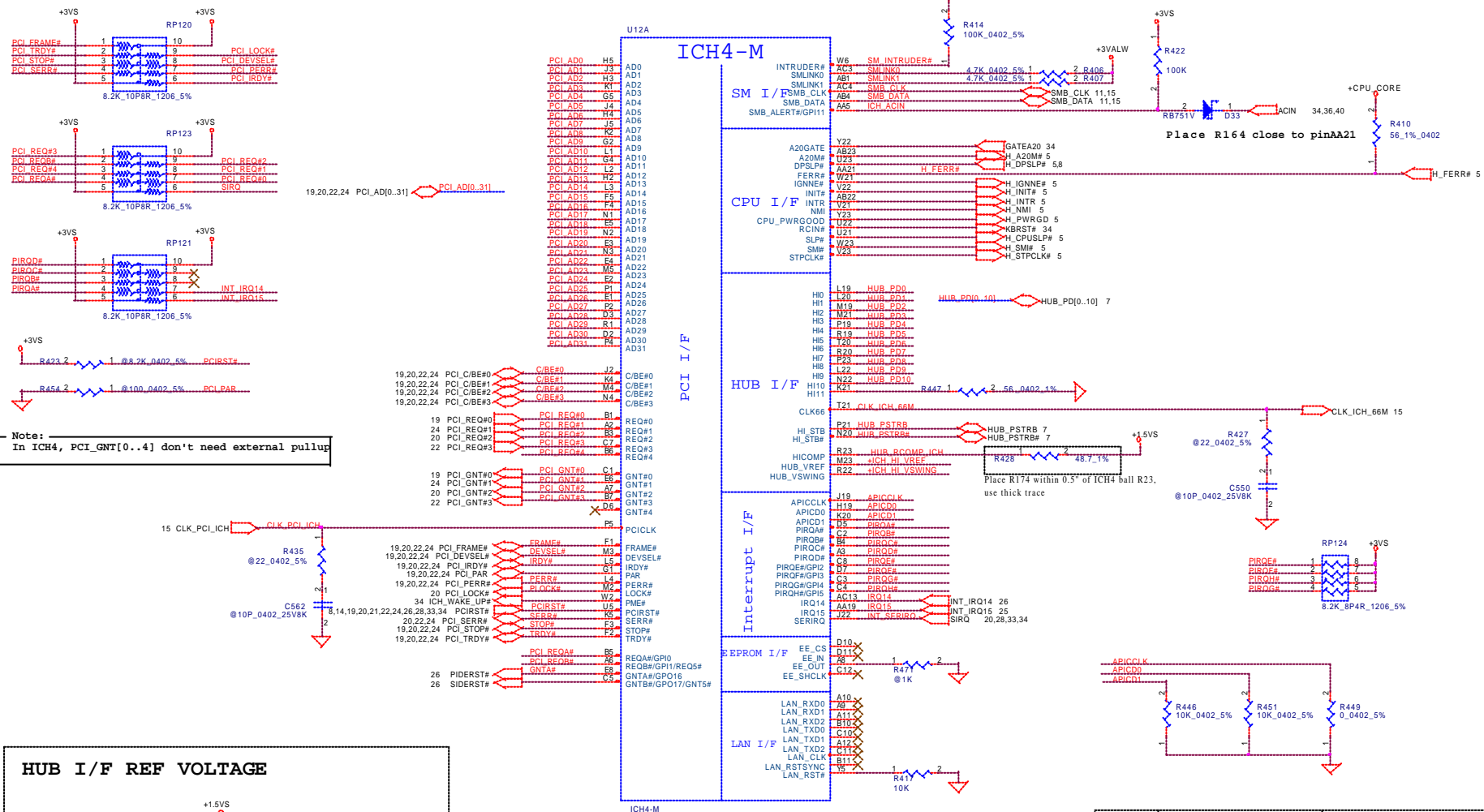




SEL2	SEL1	SEL0	CPUCLKC[0..2]	CPUCLKT[0..2]
0	0	0	166.67	166.67
0	0	1	100.00	100.00
0	1	0	200.00	200.00
0	1	1	133.33	133.33

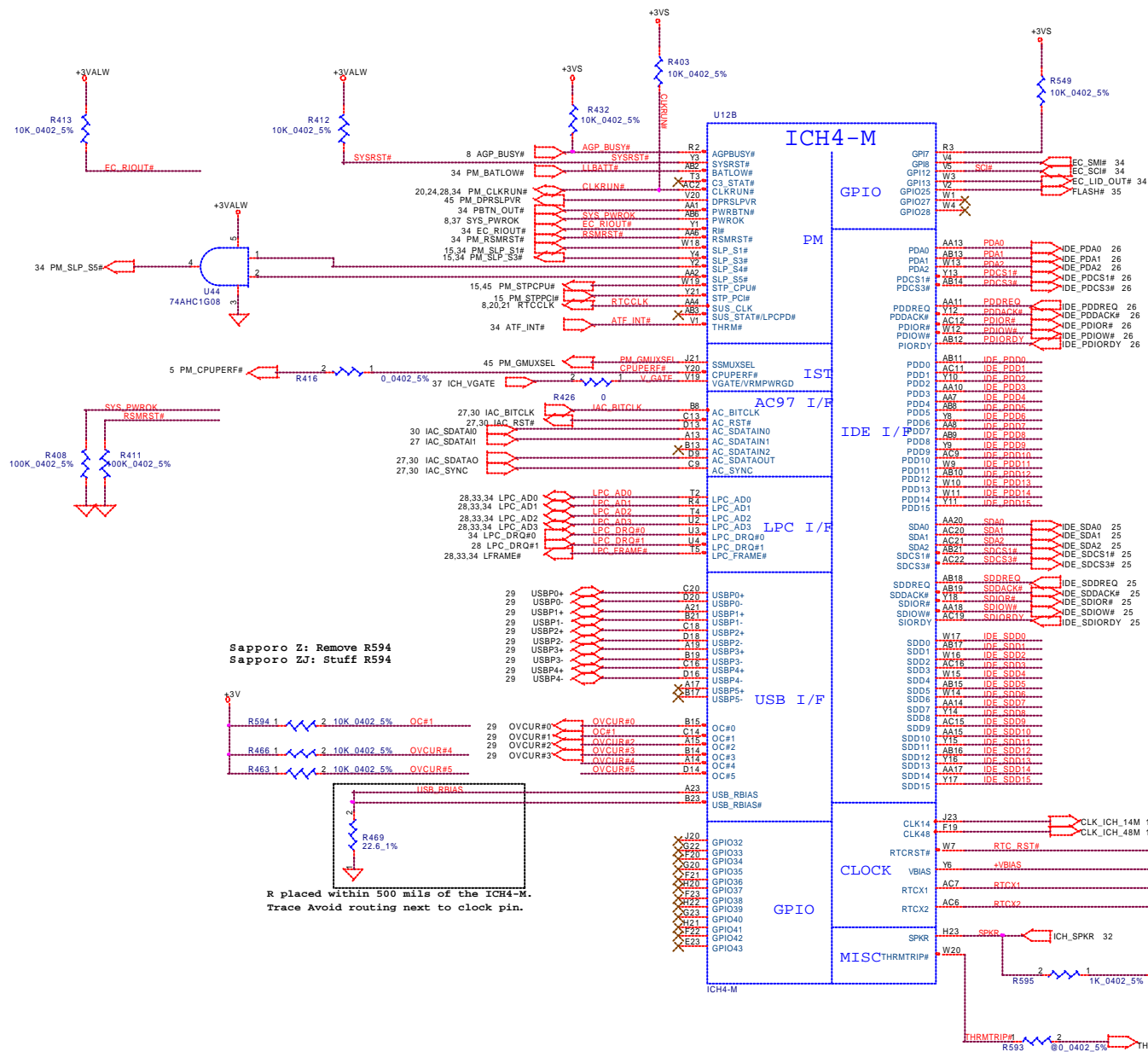






	Topology 1: Mount R458 RP122 R533 Unmount R474 RP125	Topology 2: Mount R458 R474 RP125 Unmount RP122 R533
1394	Trace: PIRQA#_1394 Use IRQA	Trace: PIRQA#_1394 Use IRQA
CardBus	Trace:PIRQA#/E# PIRQB#/F#/D# Use IRQA IRQB	Trace:PIRQA#/E# PIRQB#/F#/D# Use IRQE IRQF
LAN	Trace:PIRQ_LAN/B#/D# Use IRQB	Trace:PIRQB#/F#/D# Use IRQD
MINIPCI	Trace:PIRQC#/G# PIRQD#/H# Use IRQC IRQD	Trace:PIRQC#/G# PIRQD#/H# Use IRQC IRQH





Sapporo Z: Remove R594  
Sapporo ZJ: Stuff R594

R placed within 500 mils of the ICH4-M.  
Trace Avoid routing next to clock pin.

Place J1 close to JP3

**Compal Electronics, Ltd.**

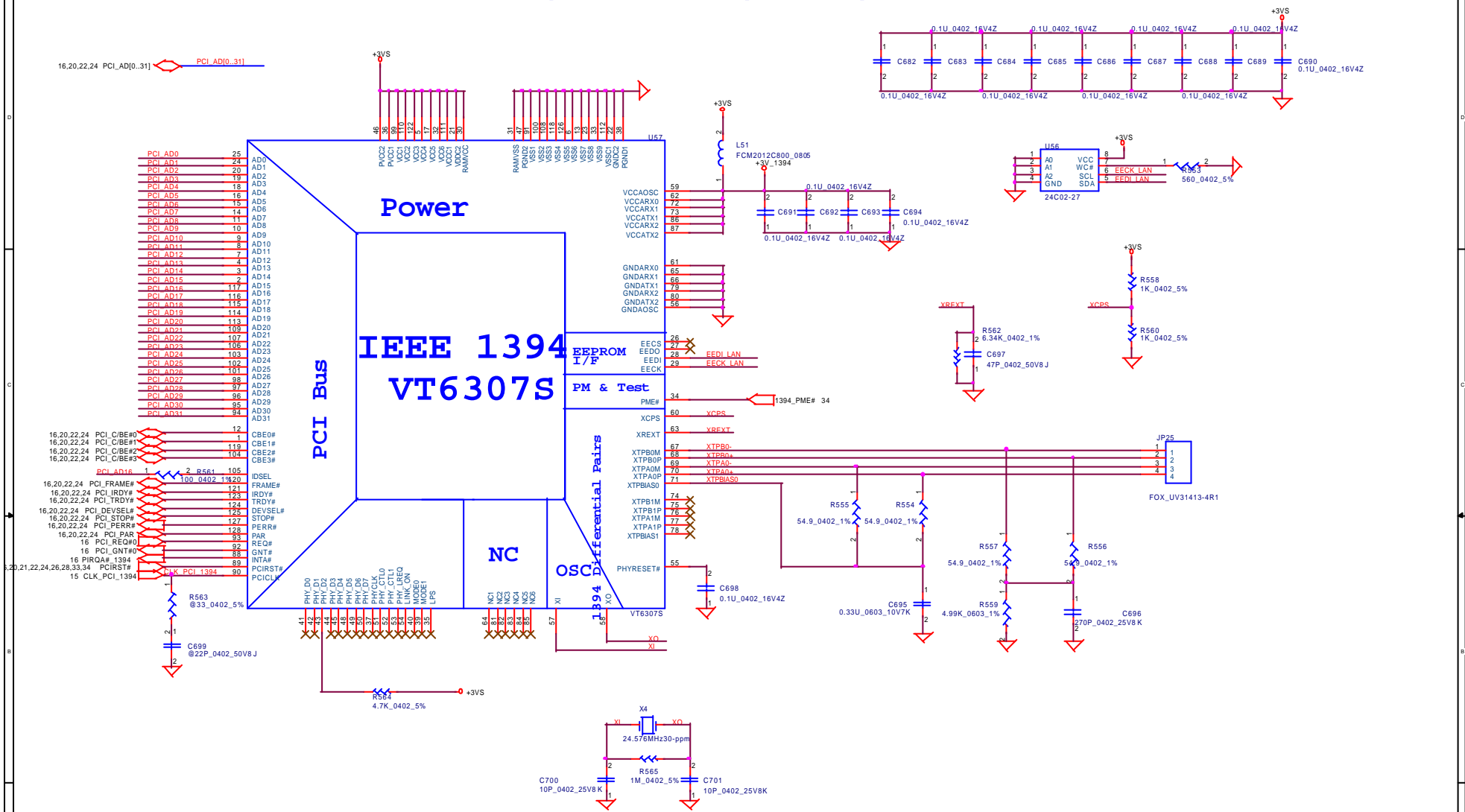
ICH4-M(2/2)

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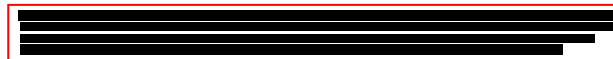
Date: Friday, November 29, 2002

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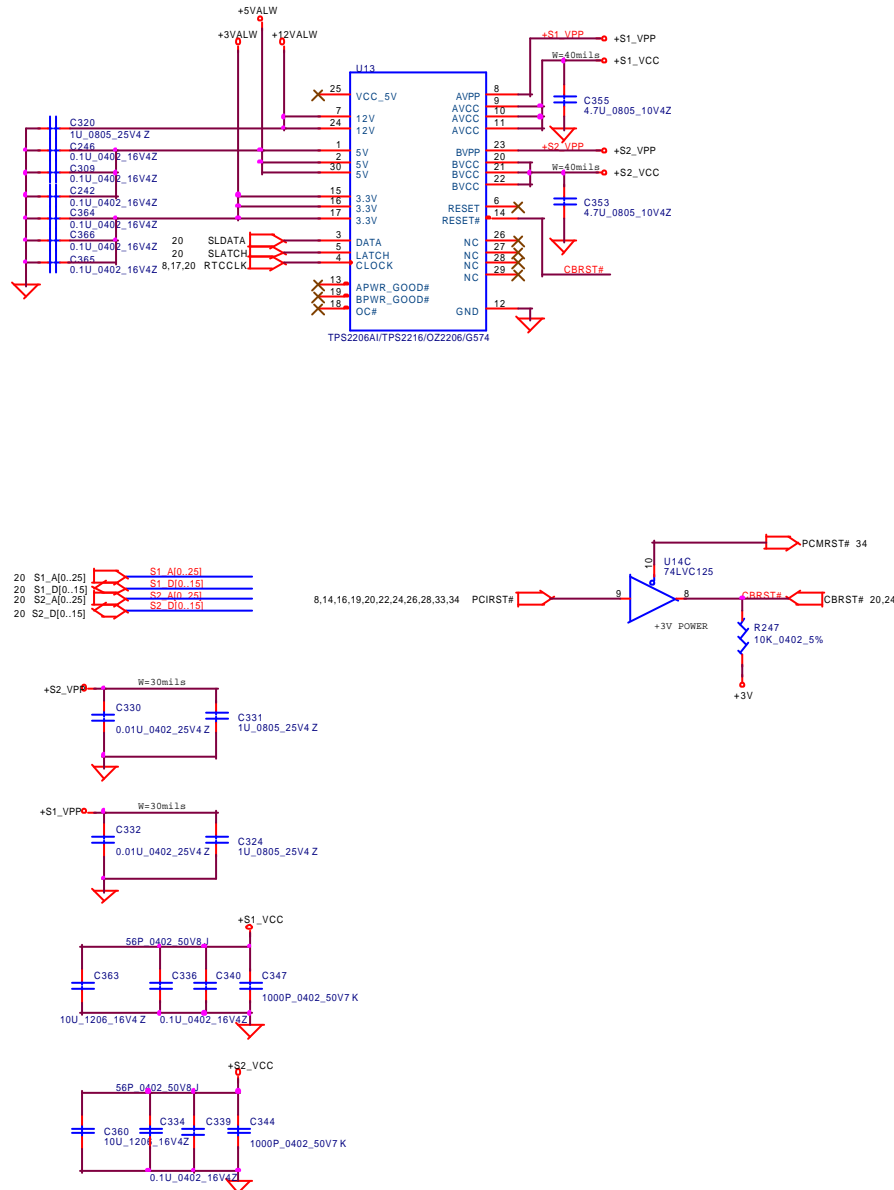
Note: These components need to close to chip pins.



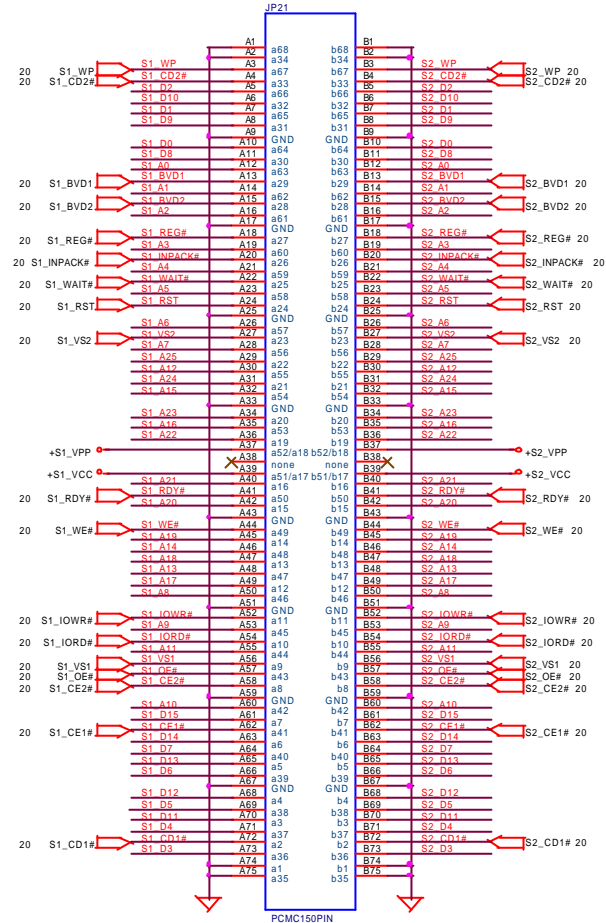
http://laptopblue.vn

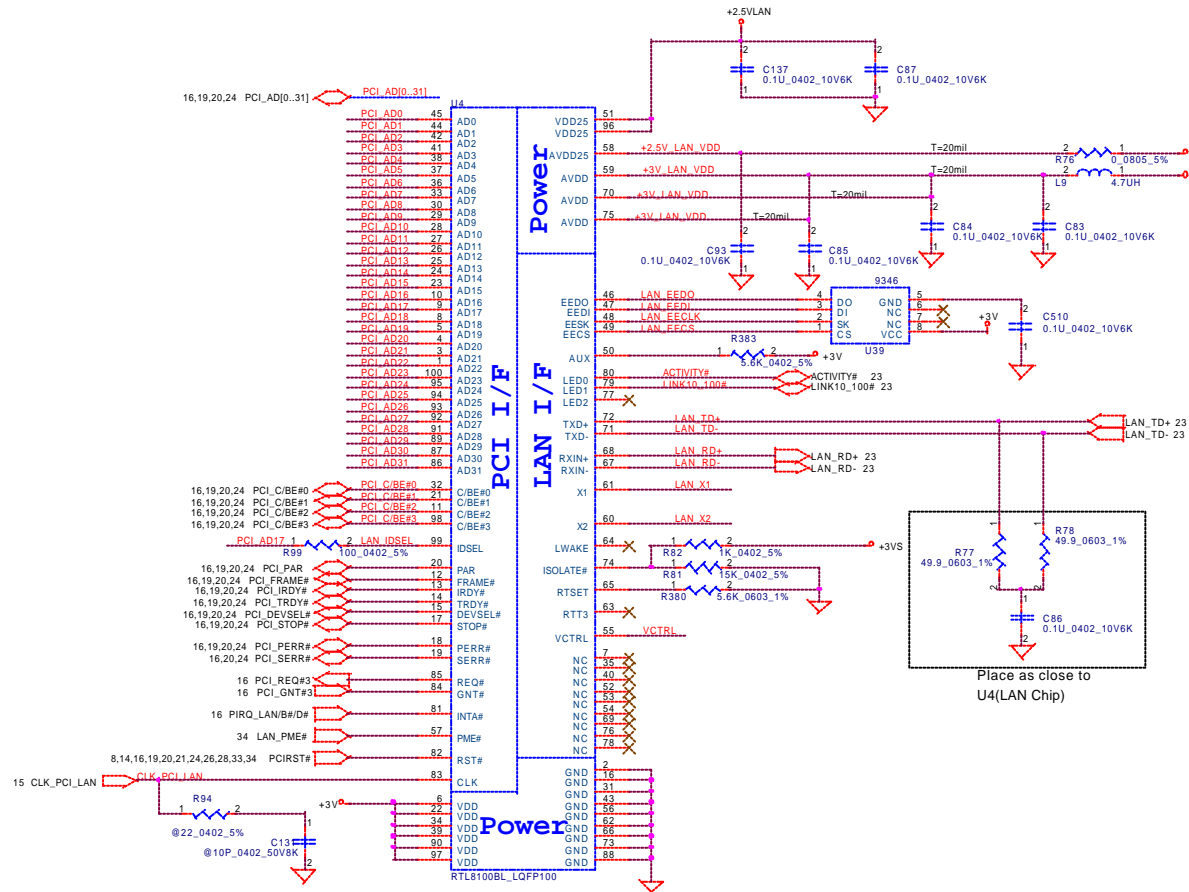


# PCMCIA POWER CTRL.

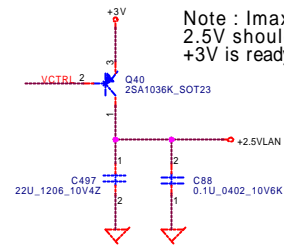


# CARDBUS SOCKET

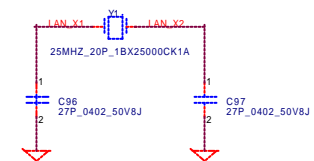
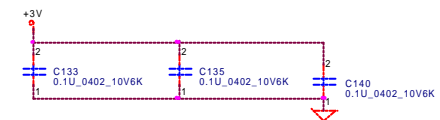
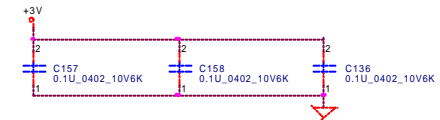




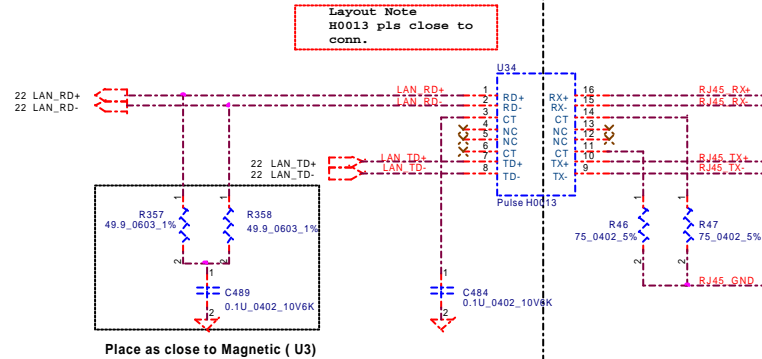
- 1.Q40 pin2 close to U4 pin55
- 2.C497 and C88 close to Q40 pin1



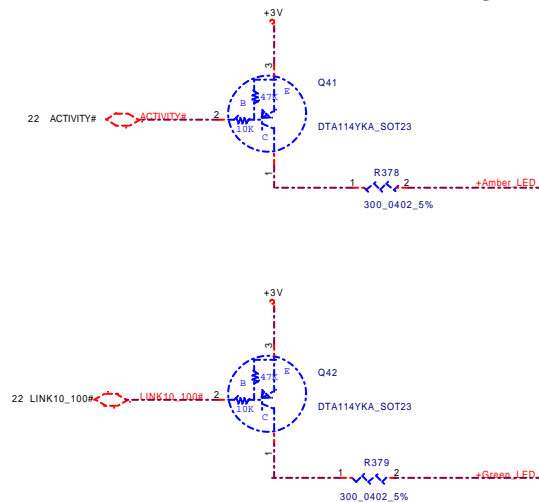
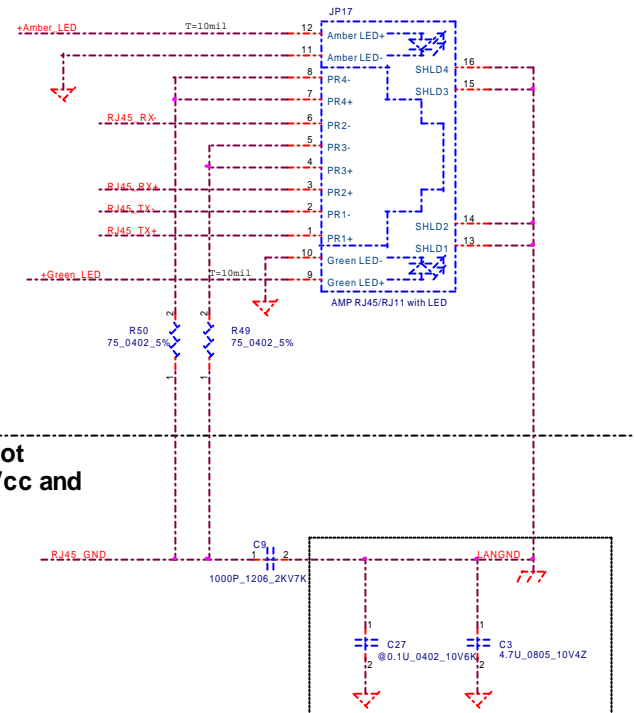
2.5VLAN power generated by VCTRL.

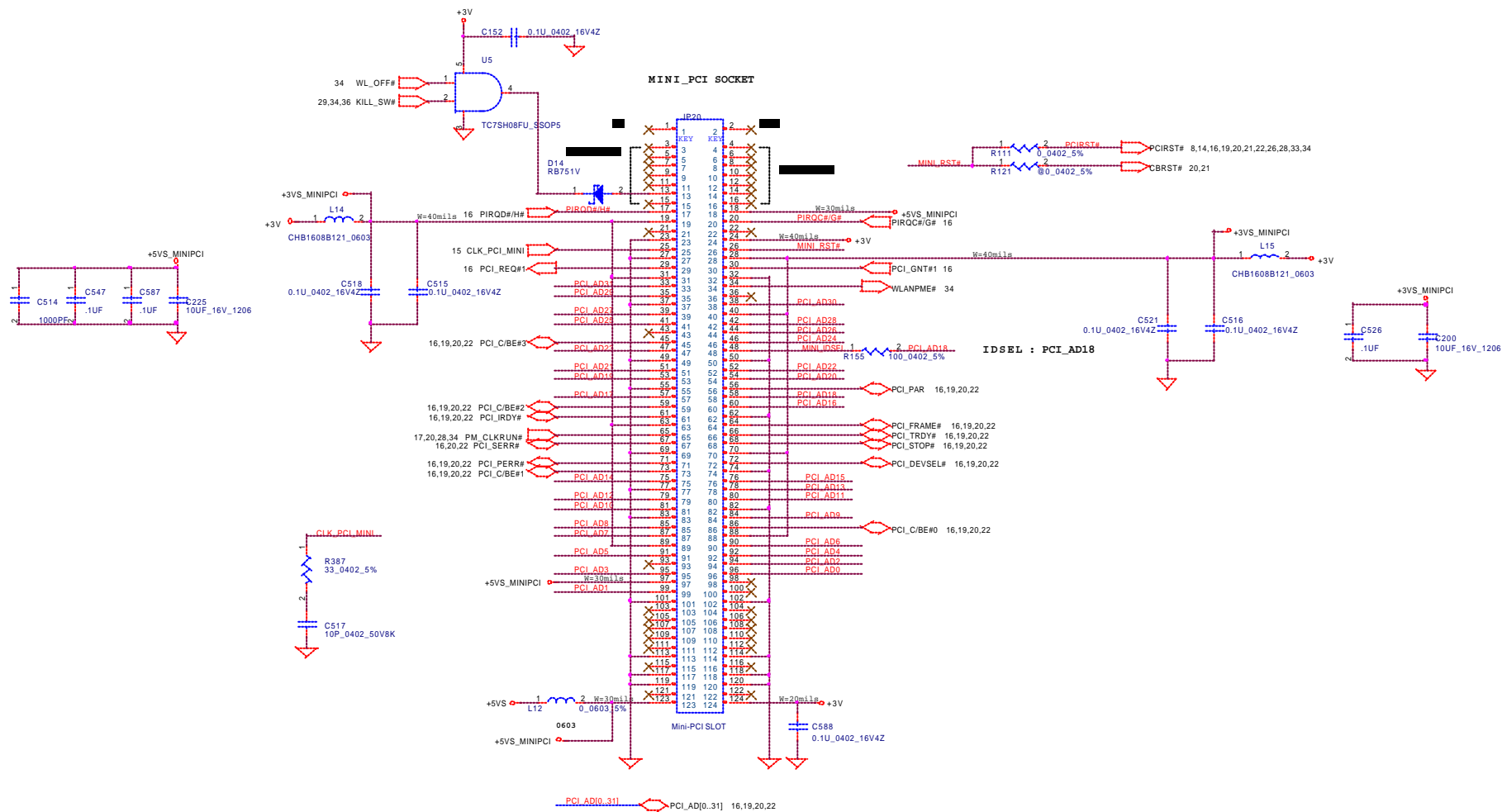


# Keep Out 40mil

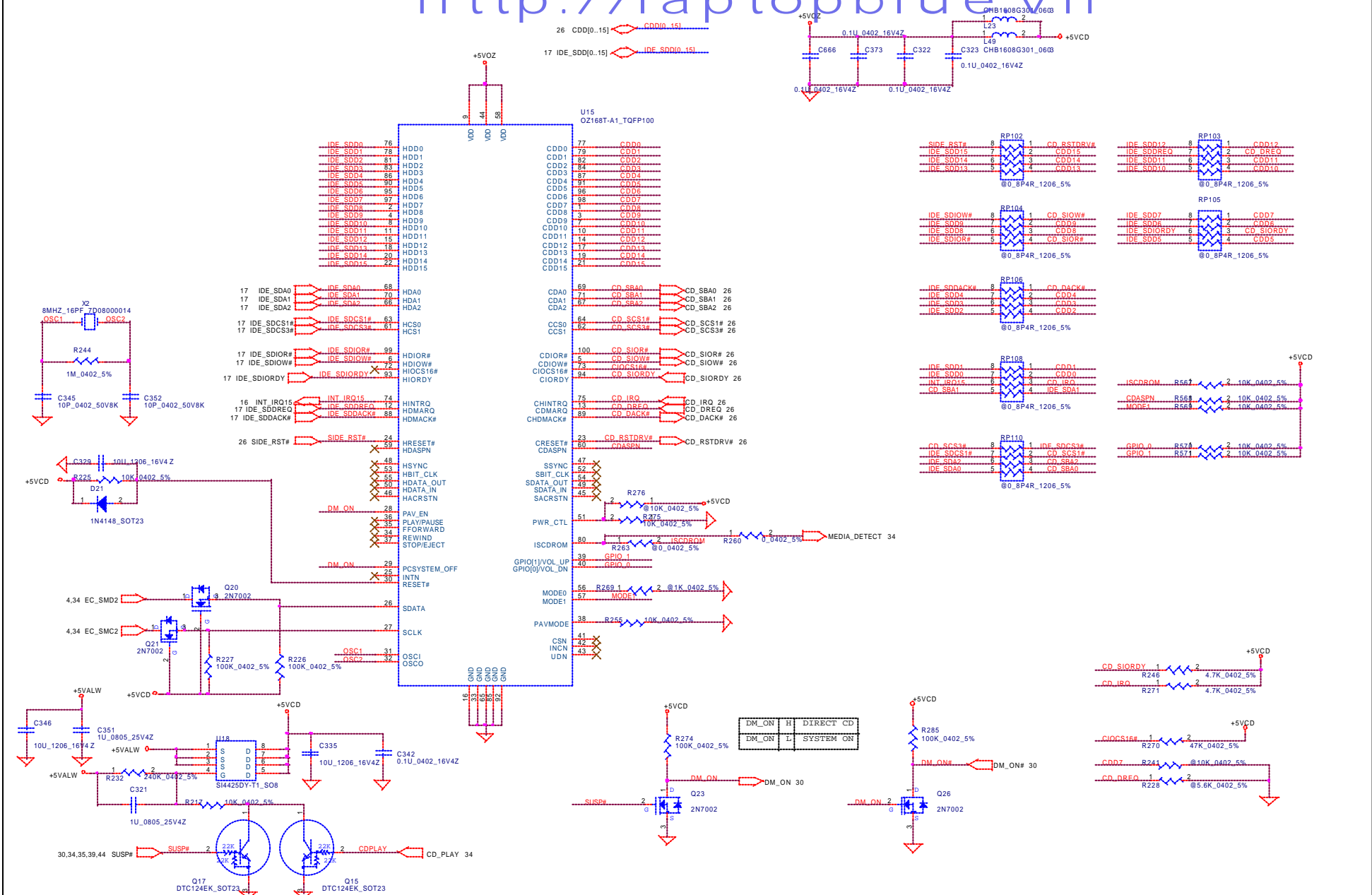


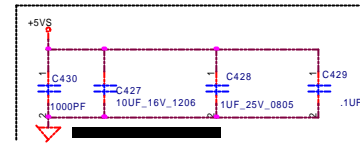
**LAYOUT NOTICE:** This area do not connect to power plan include Vcc and GND in any layer



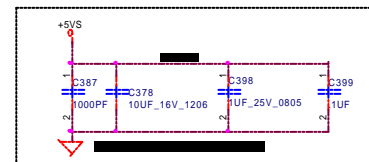




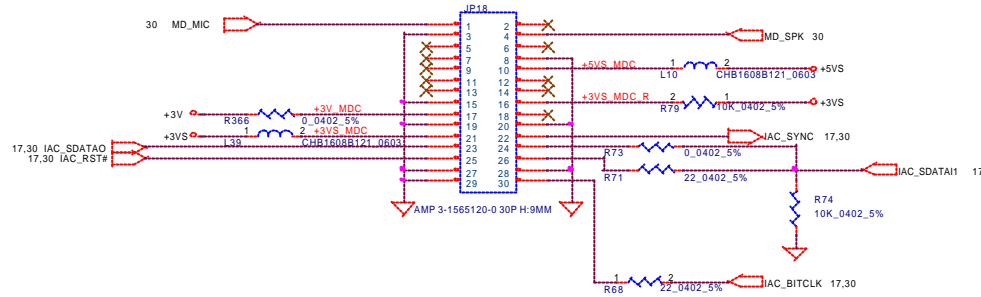




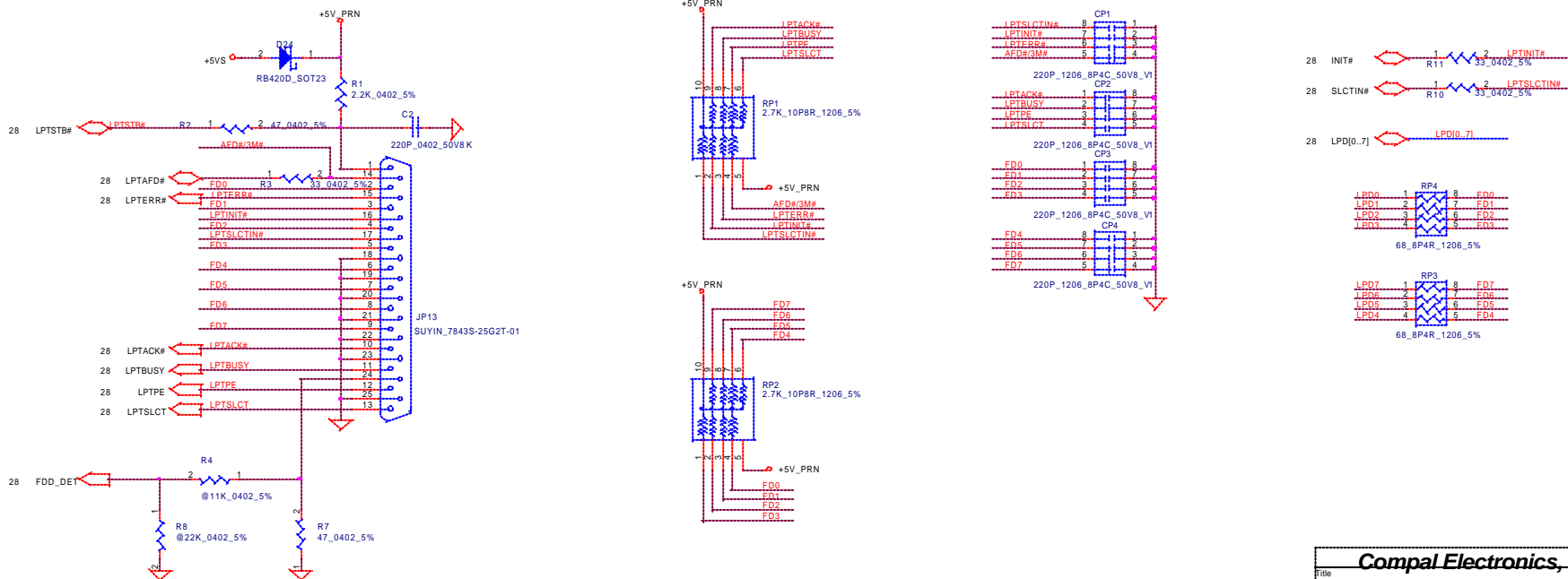
**CD-ROM Module CONN.**



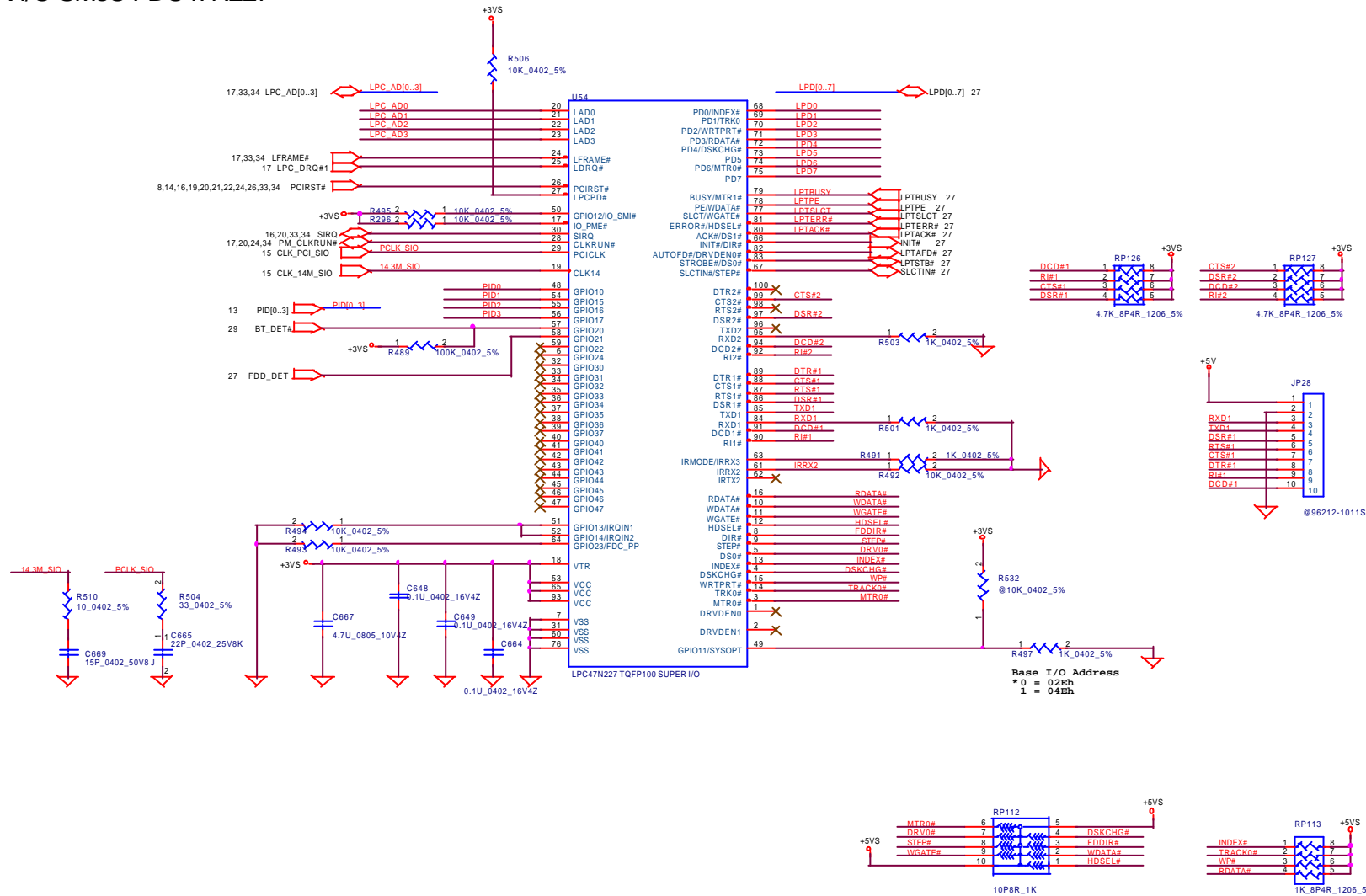
## MDC Connector



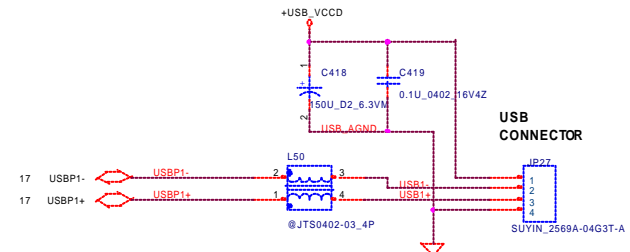
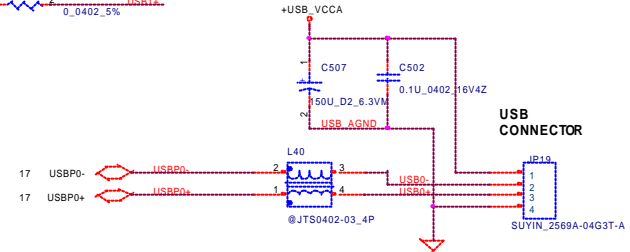
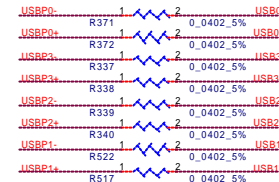
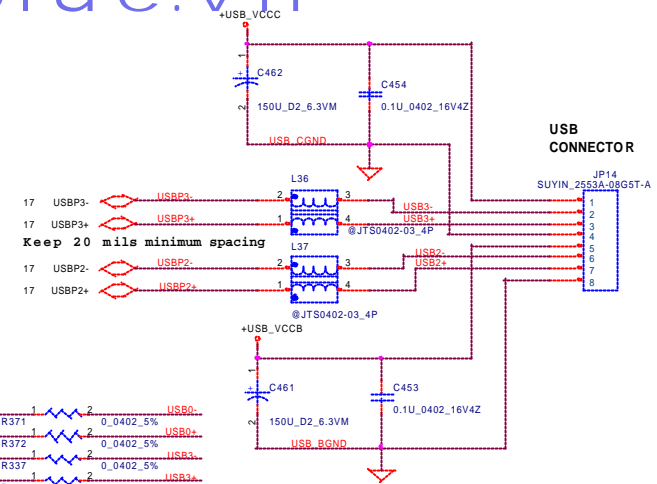
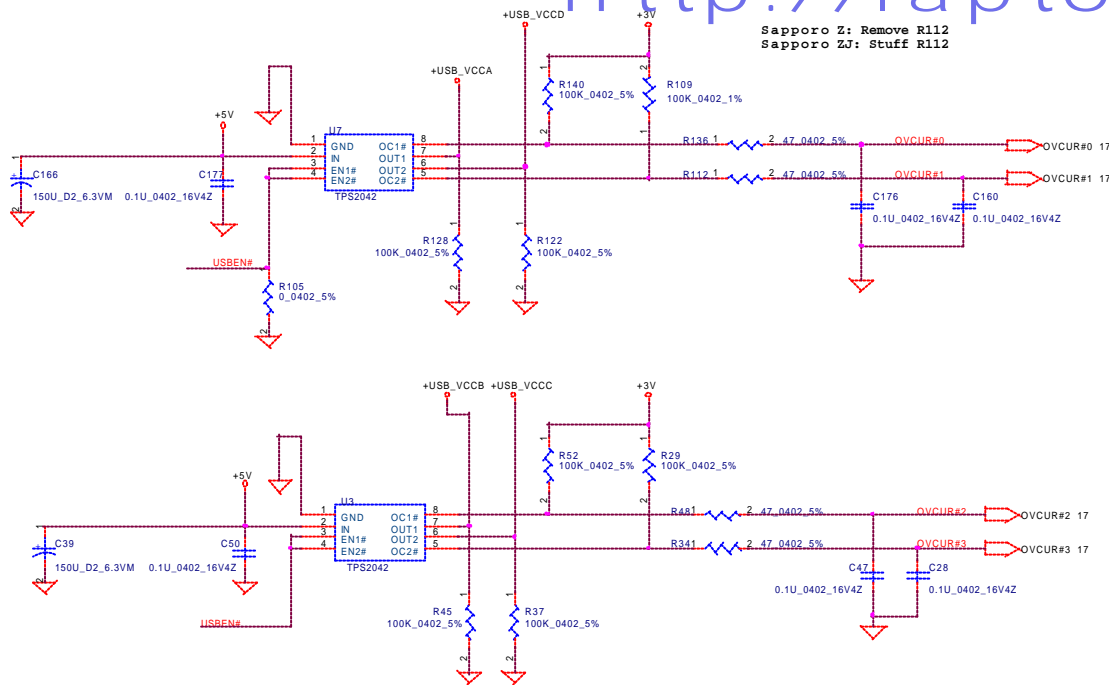
## Parallel Port



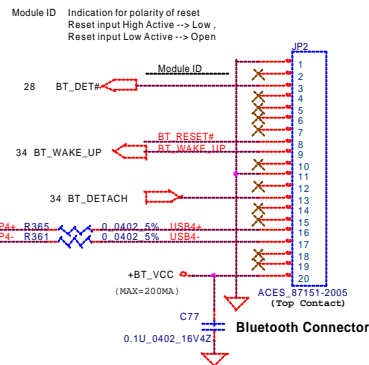
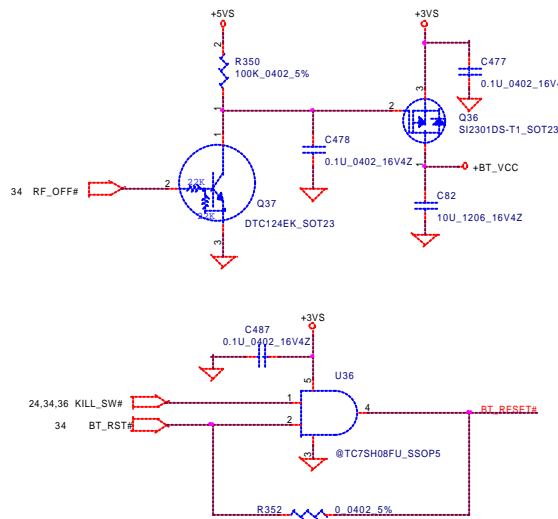
# SUPER I/O SMCs FDC47N227



Sapporo Z: Remove R112  
Sapporo ZJ: Stuff R112



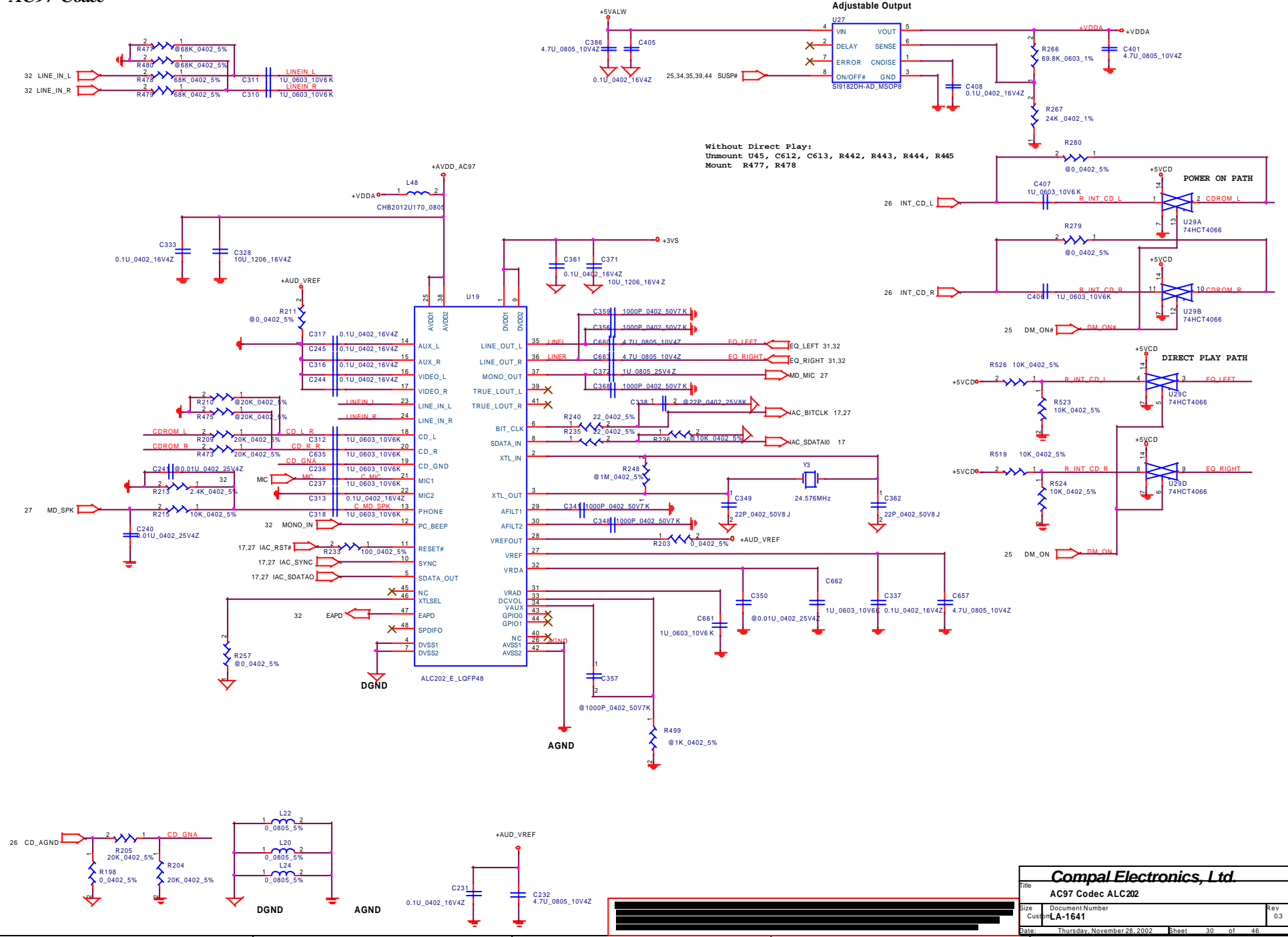
## BlueTooth Interface

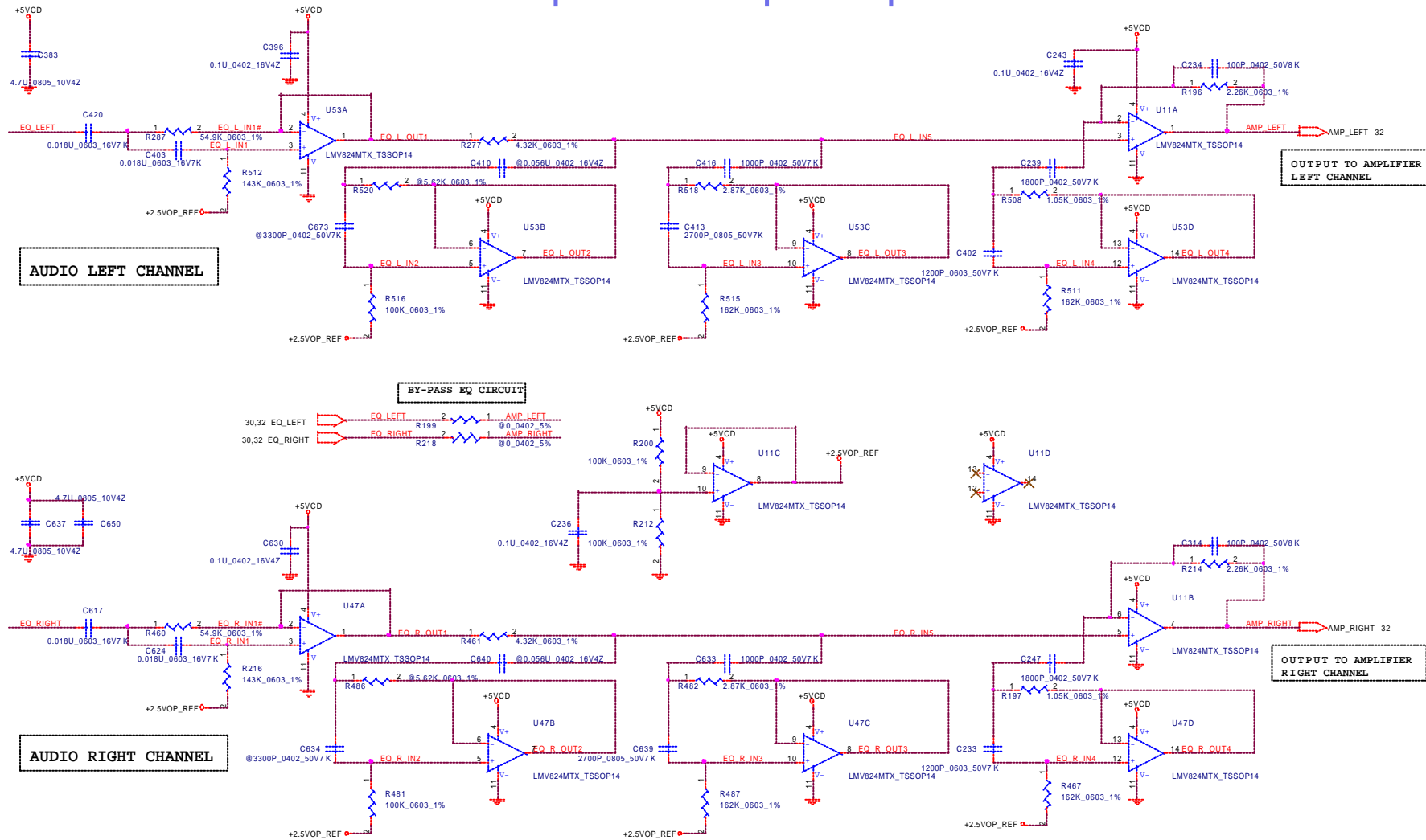


Compal Electronics, Ltd.

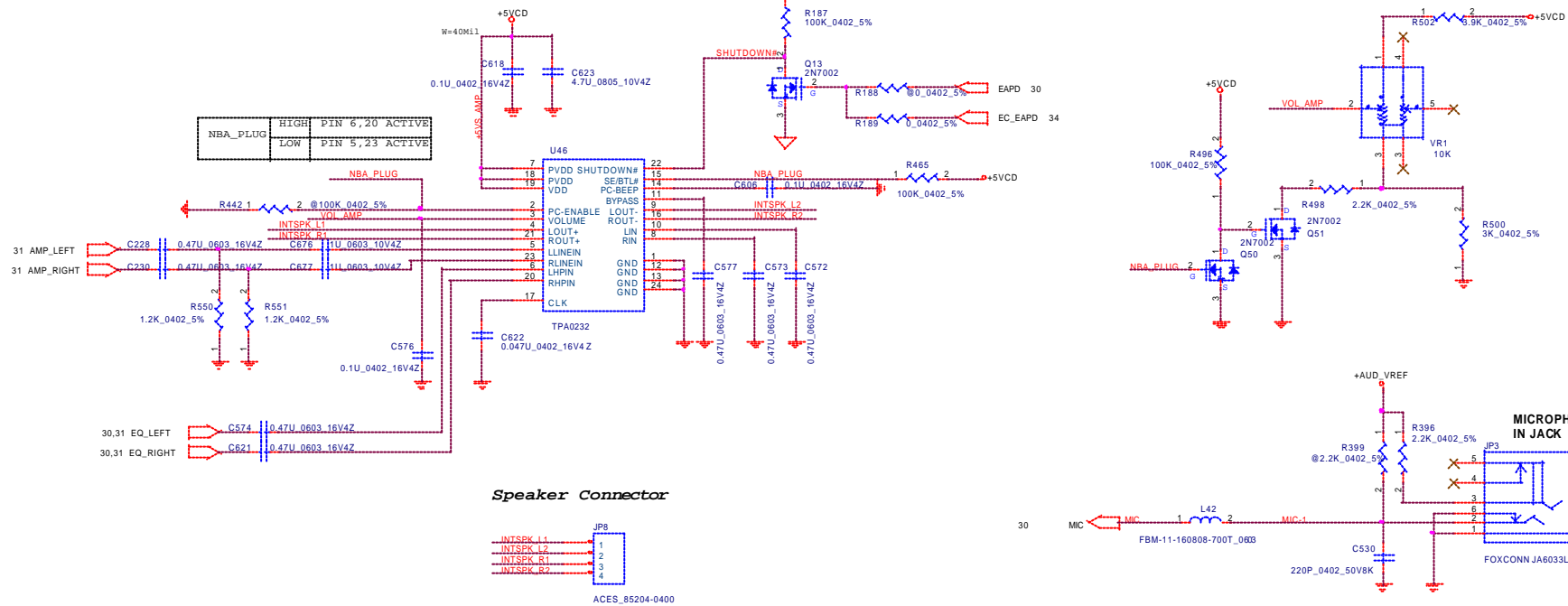
USB & Bluetooth

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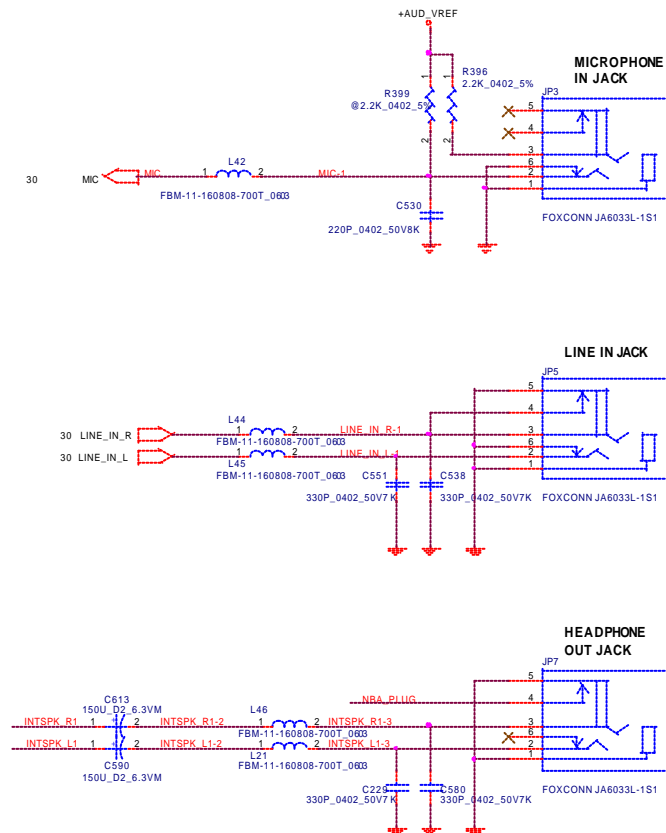
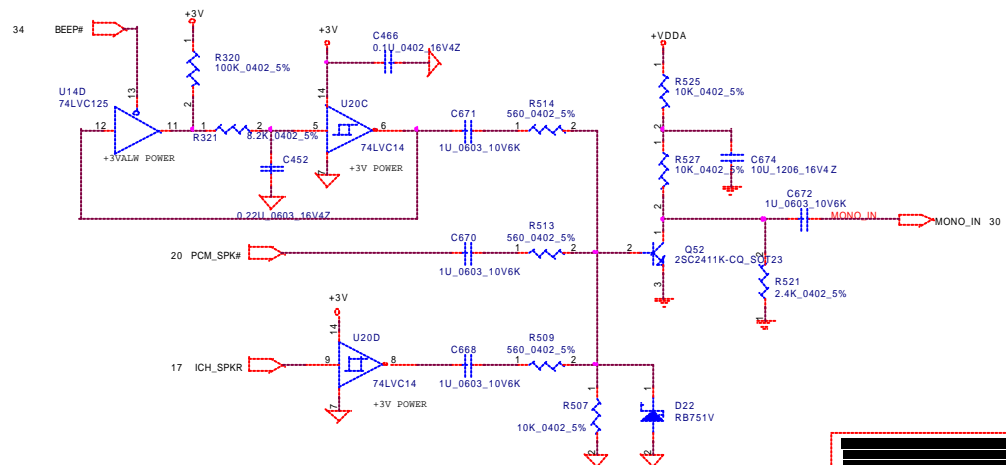




## Audio AMP

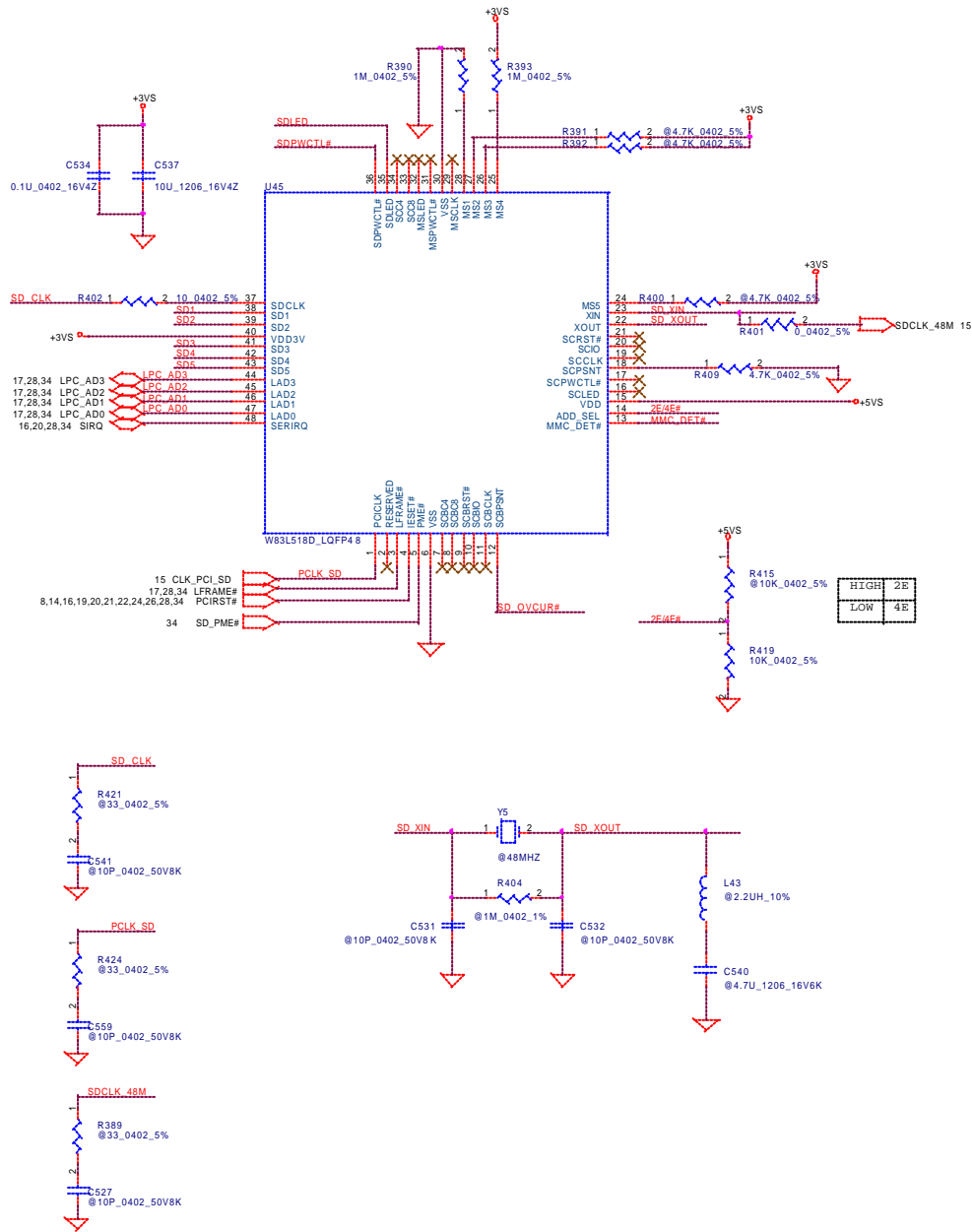


### System Sound

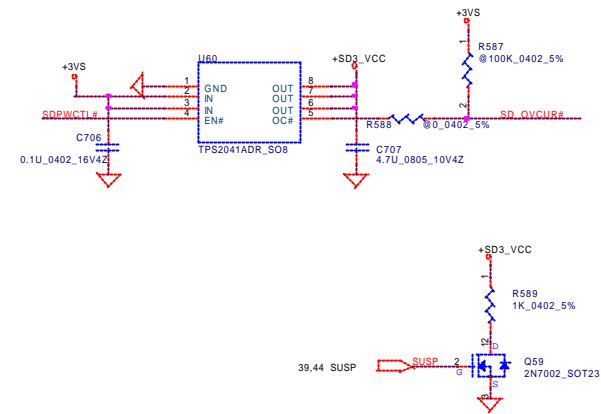




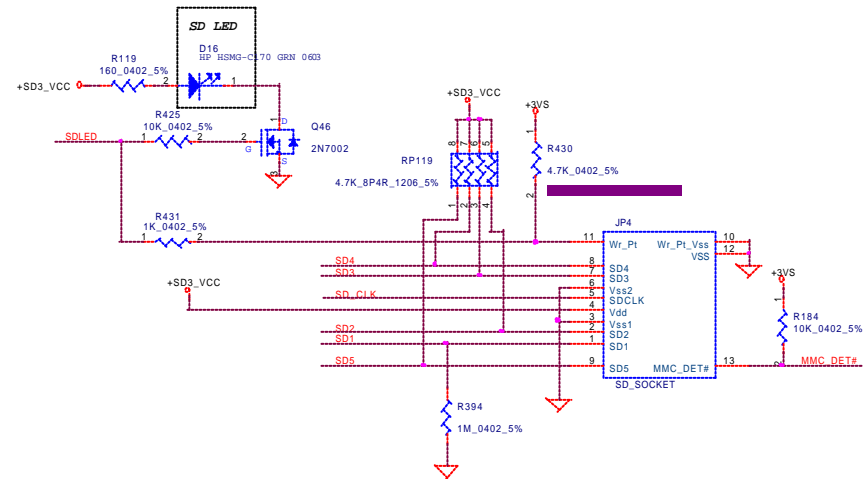
## SD Card Reader

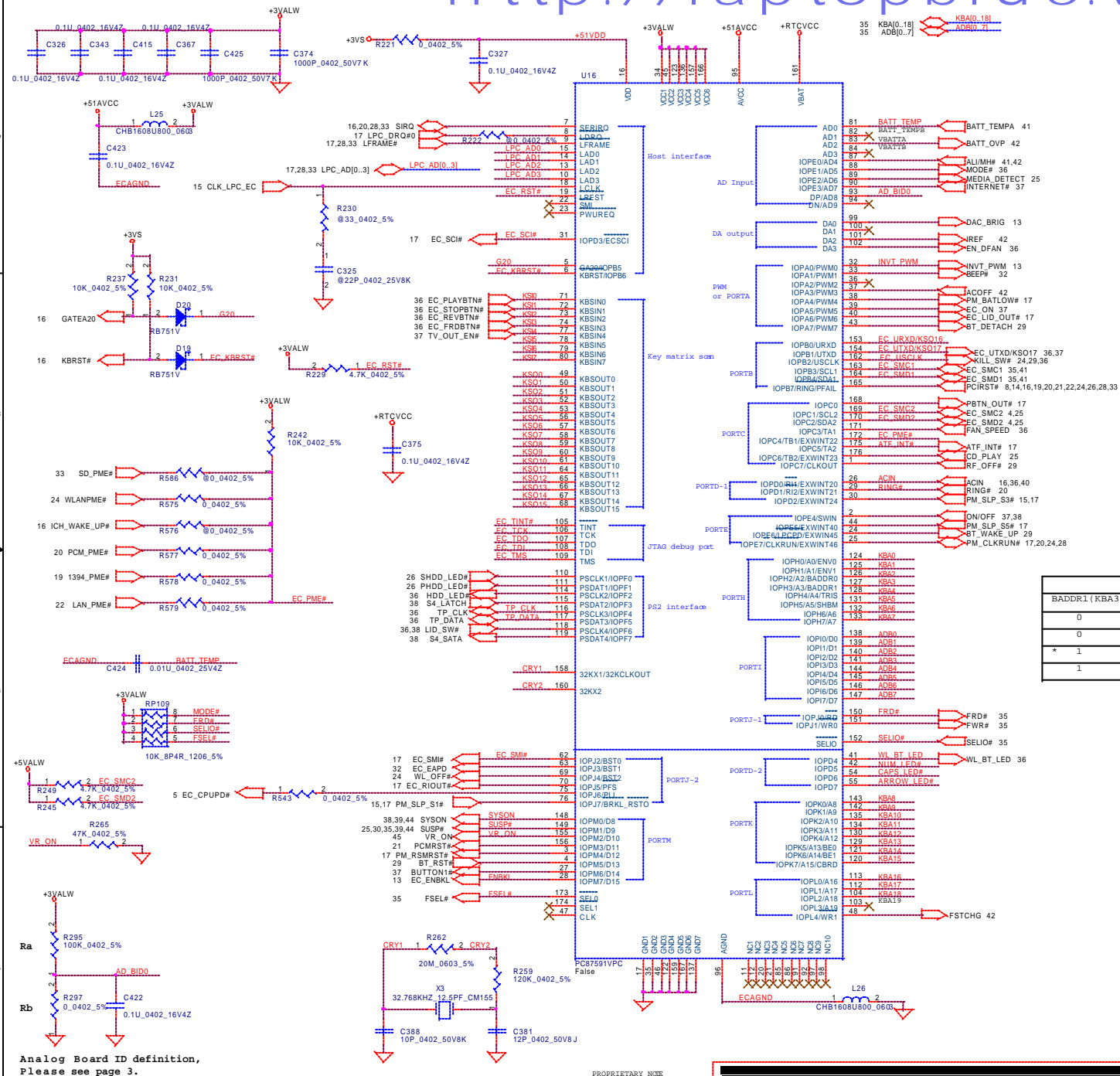


## SD Power Switch

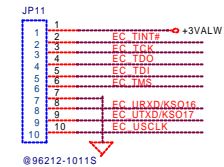


## SD SOCKET

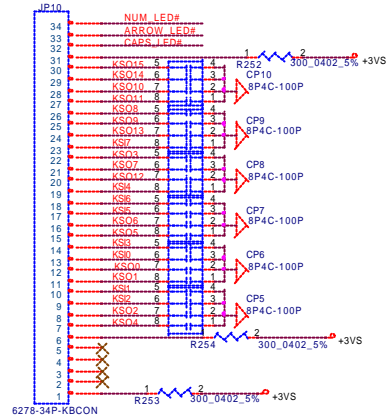




*For EC Tools*



KEYBOARD CONN.

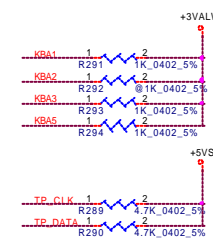


		I/O Address	
BADDR1(KBA3)	BADDR0(KBA2)	Index	Data
0	0	2E	2F
0	1	4E	4F
*	1	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)
1	1	Reserved	

ENV0 (KBA0) ENV1 (KBA1) TRIS (KBA4)

IRE	0	0	0
* OBD	0	1	0
DEV	1	0	0
PROG	1	1	0

```
SHBM(KBA5)=1: Enable shared memory with host BIOS
TRIS(KBA4)=1: While in IRE and OBD, float all the
    signals for clip-on ISE use
```



Analog Board ID definition,  
Please see page 3.

PROPRIETARY NOTE

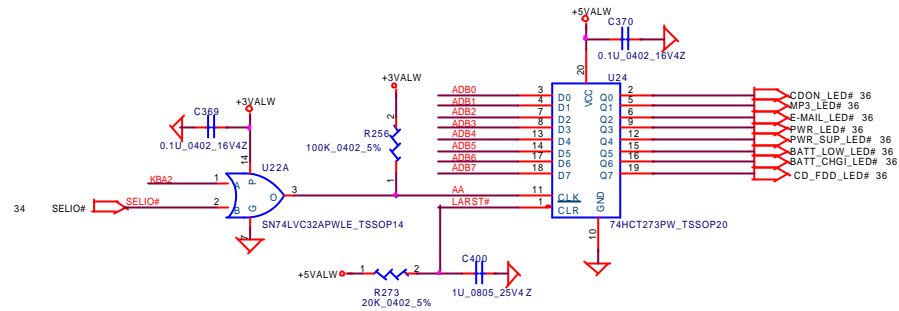
**Compal Electronics, Ltd.**

Title **LPC- PC87591**

Size	Document Number
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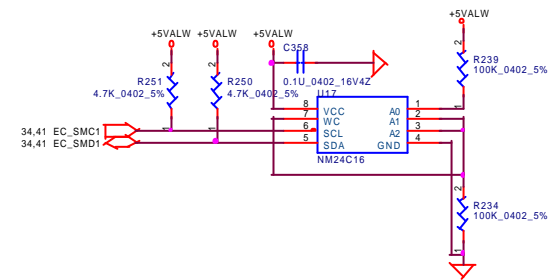
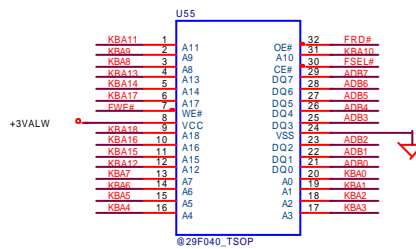
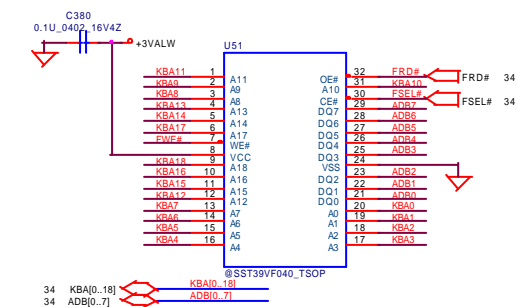
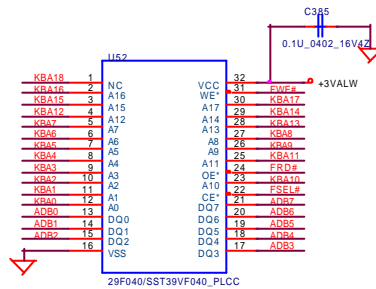
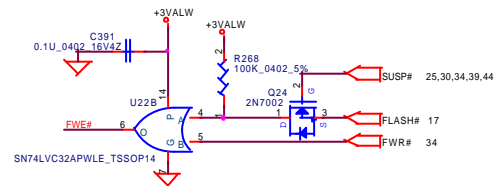
Custom **LA-1641**

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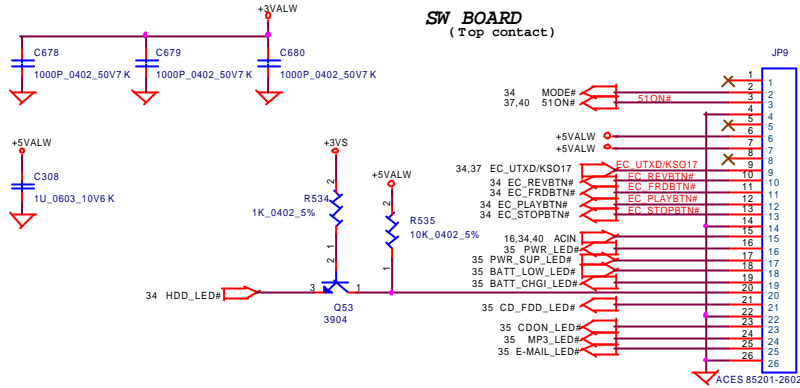


## System BIOS

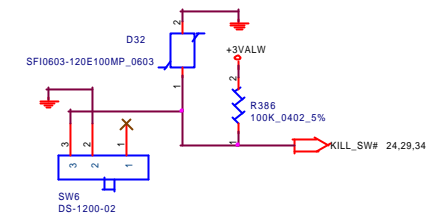
## SMBus EEPROM



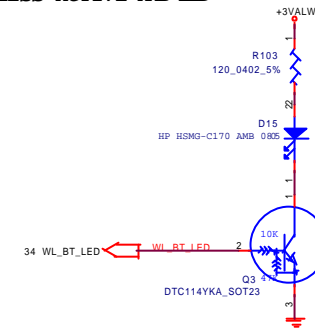
# SW BOARD (Top contact)



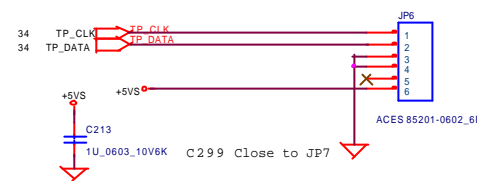
## Kill SWITCH



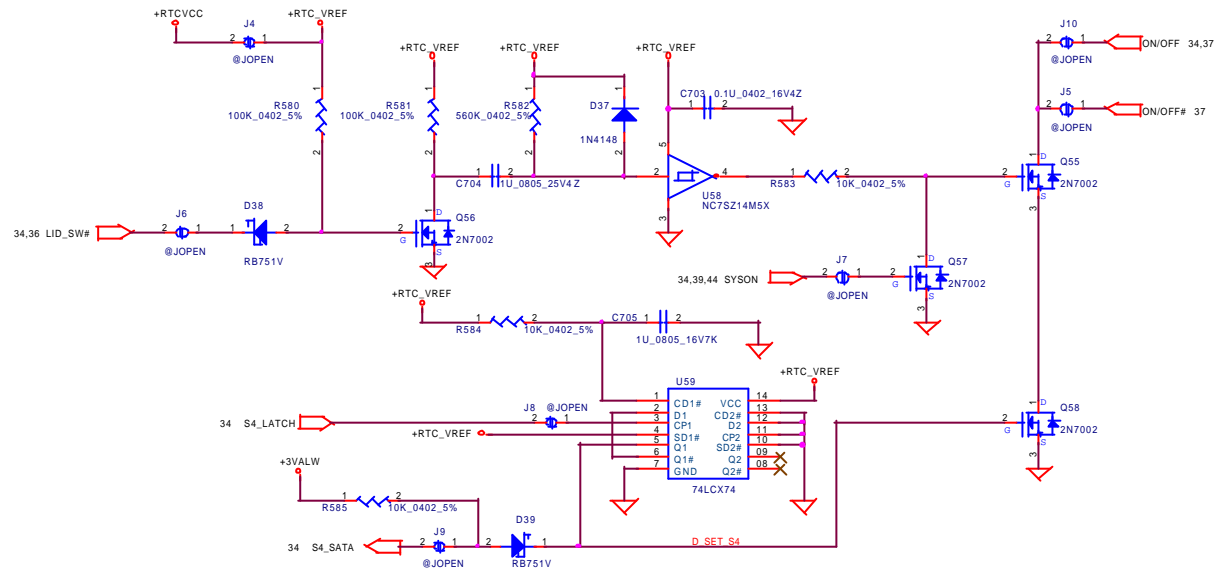
## WIRELESS ACTIVE AMB LED



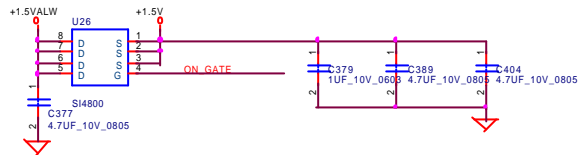
## Touch Pad Connector



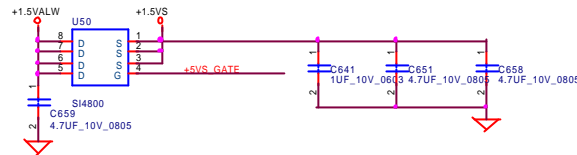




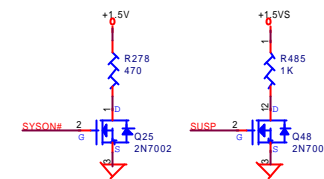
**+1.5VALW To +1.5V Transfer**



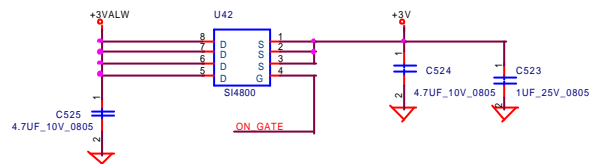
**+1.5VALW To +1.5VS Transfer**



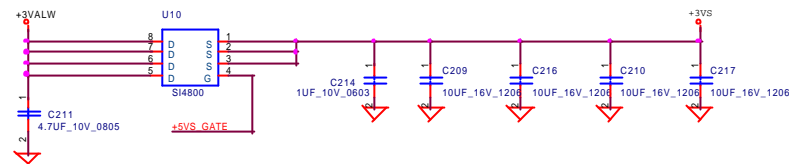
**+1.5V & +1.5VS Discharge**



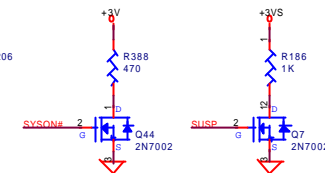
**+3VALW To +3V Transfer**



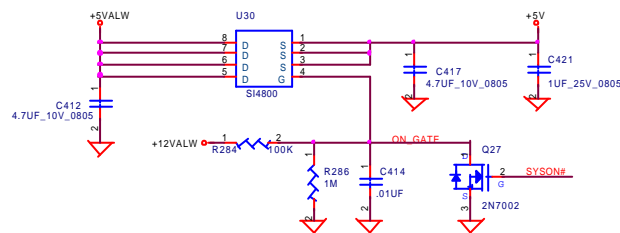
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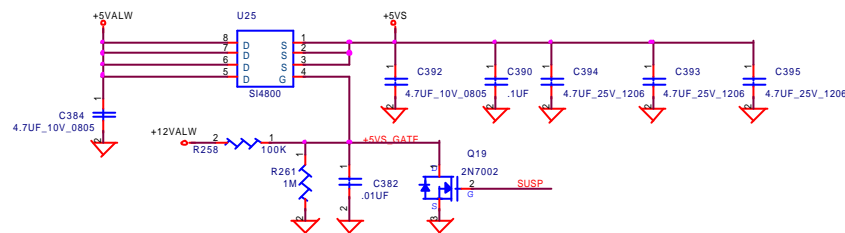
**+3V & +3VS Discharge**



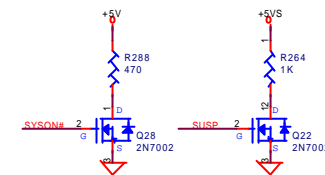
**+5VALW To +5V Transfer**



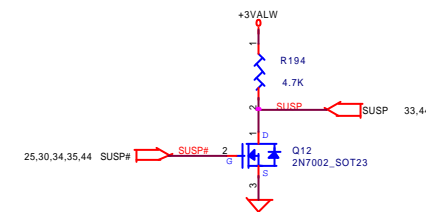
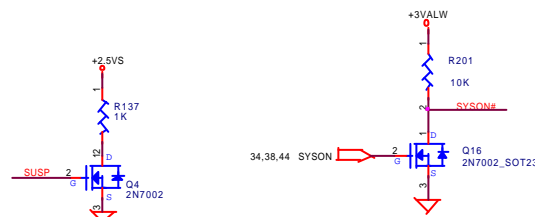
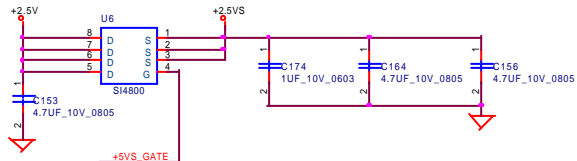
**+5VALW To +5VS Transfer**

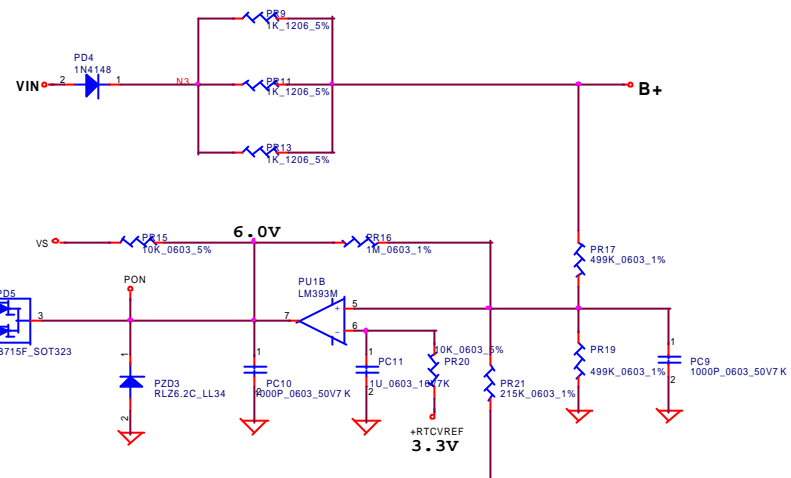
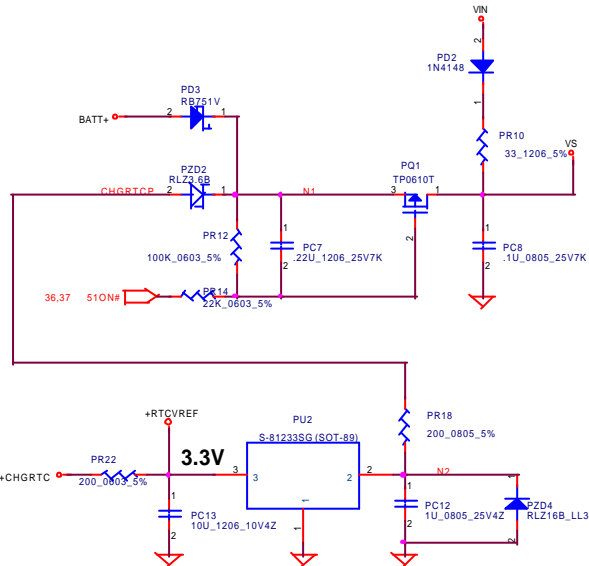
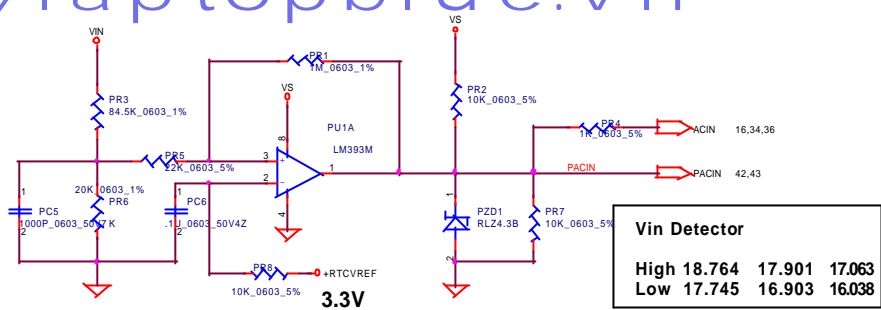
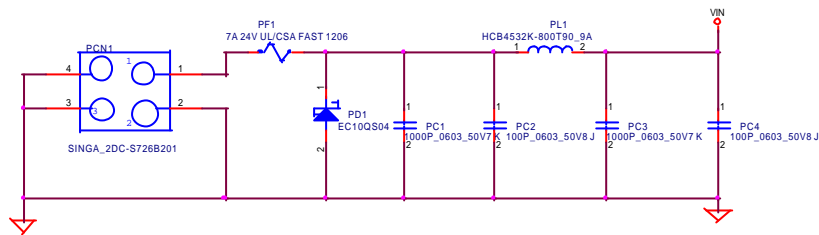


**+5V & +5VS Discharge**

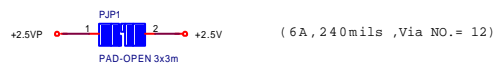


**+2.5V To +2.5VS Transfer**





Precharge detector		
15.34	15.90	16.48
13.13	13.71	14.20



(3A, 120mils, Via NO.= 6)



(300mA, 40mils, Via NO.= 2)



(5A, 200mils, Via NO.= 10)



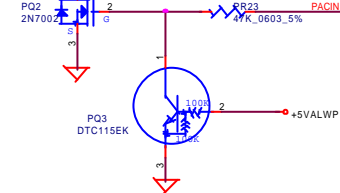
(5A, 200mils, Via NO.= 10)



(5A, 200mils, Via NO.= 10)



(5A, 200mils, Via NO.= 10)



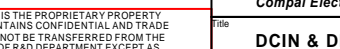
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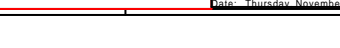
(5A, 200mils, Via NO.= 10)



(5A, 200mils, Via NO.= 10)



(5A, 200mils, Via NO.= 10)



(5A, 200mils, Via NO.= 10)

Compal Electronics, Inc.

DCIN & DETECTOR

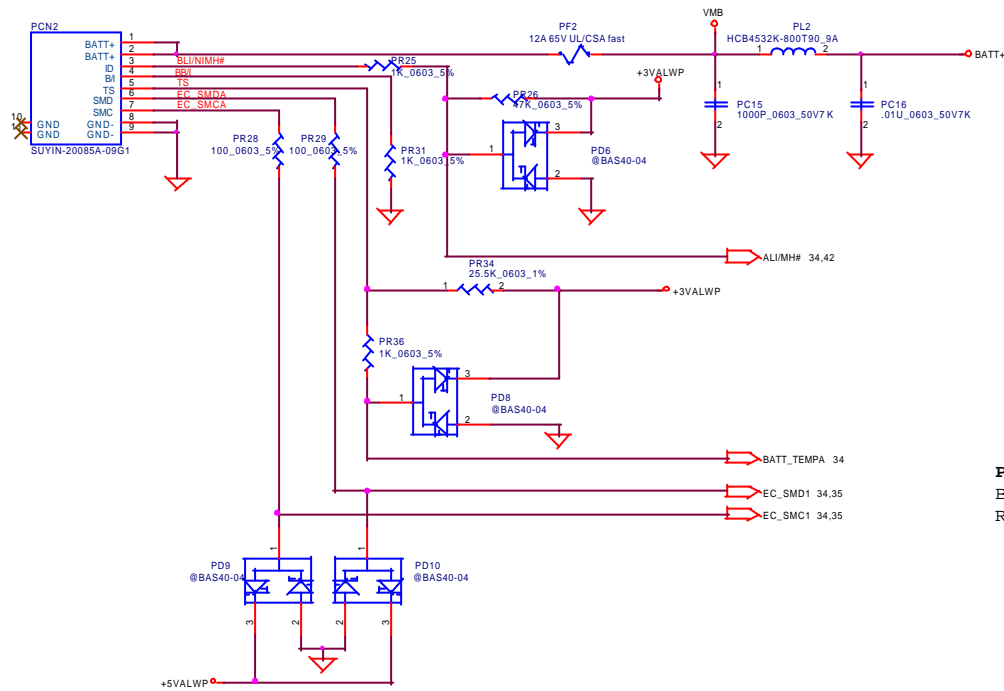
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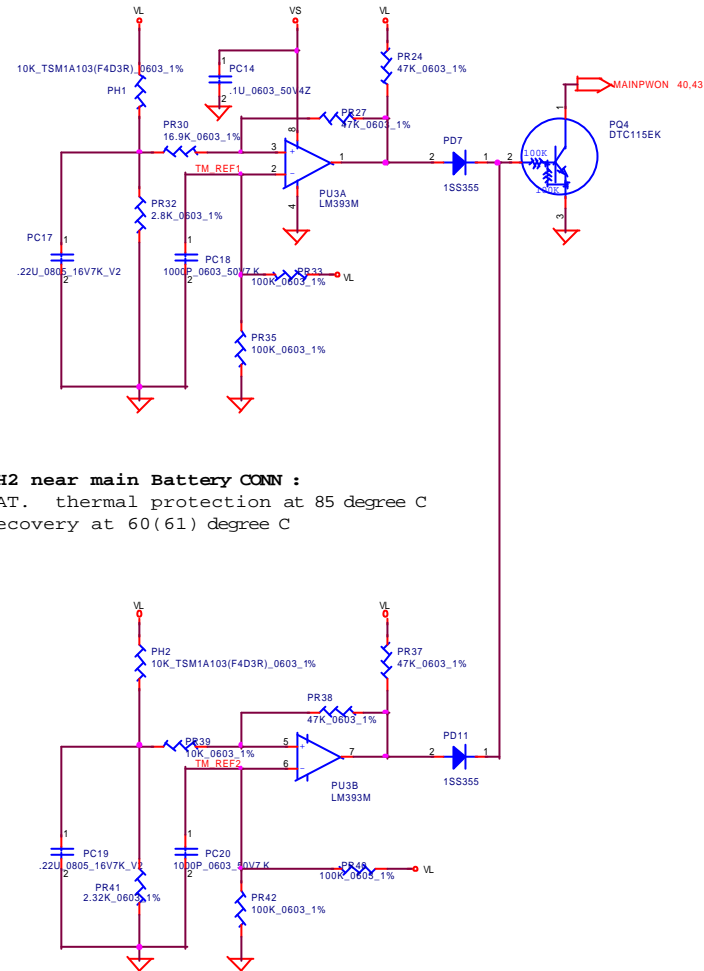
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**PH1 under CPU botten side :**  
CPU thermal protection at 90(91) degree C  
Recovery at 50 degree C

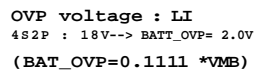


**PH2 near main Battery CONN :**  
BAT. thermal protection at 85 degree C  
Recovery at 60(61) degree C



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Compal Electronics, Inc.			
BATTERY CONN / OTP			
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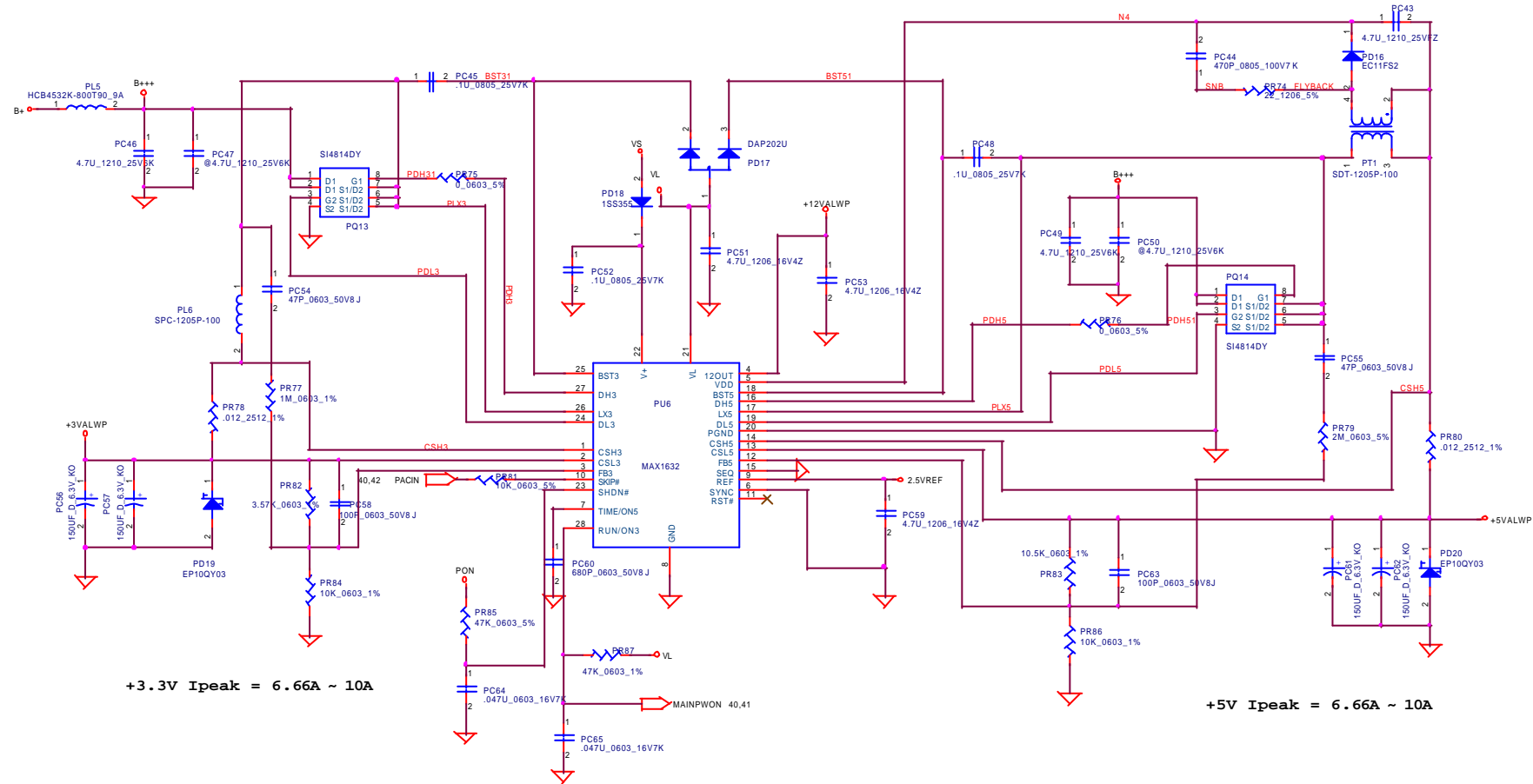


**Compal Electronics, Inc.**

## CHARGER

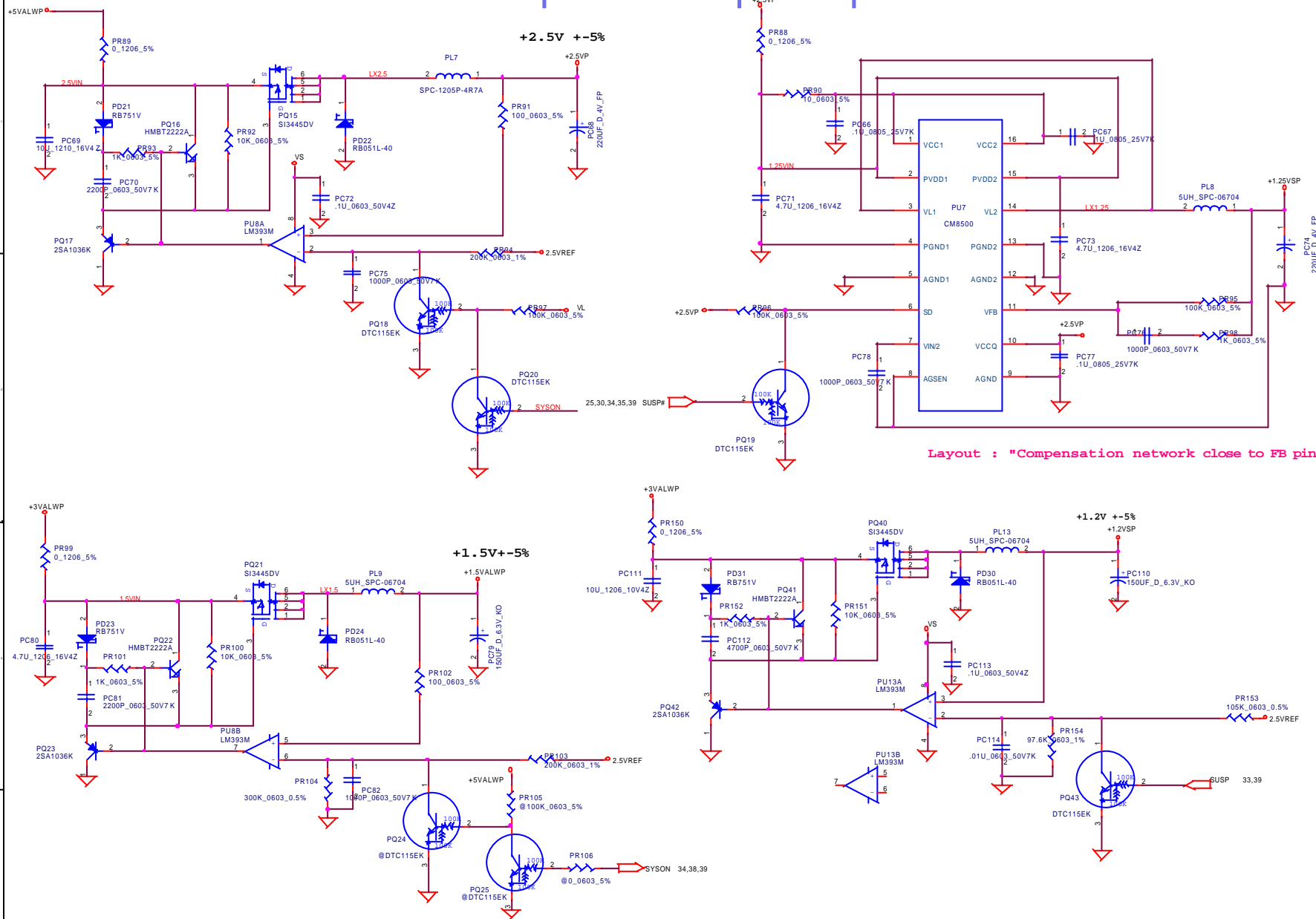
Size	Document Number
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0.3



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Compal Electronics, Inc.			
Title		5V/3.3V/12V	
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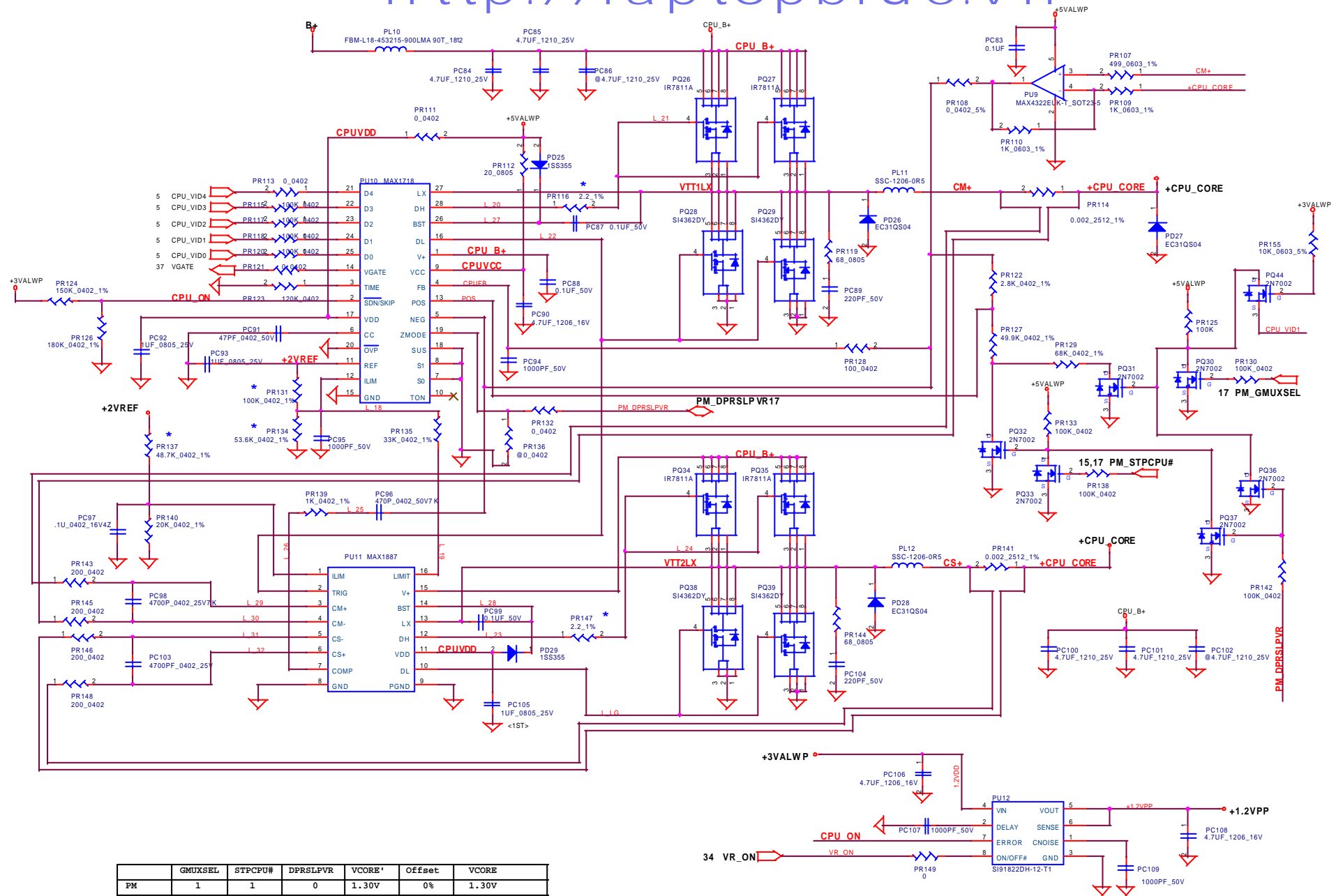


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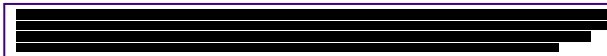
Compal Electronics, Inc.

DDR / 2.5V / 1.25V/1.5V

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	GMUXSEL	STPCPU#	DPRSLEVR	VCORE'	Offset	VCORE
PM	1	1	0	1.30V	0%	1.30V
PM D-S	1	0	0	1.239V	4.62%	1.239V
BM	0	1	0	1.20V	2.0%	1.176V
BM D-S	0	0	0	1.144V	4.62%	1.144V
Deeper	X	0	1	1.0V	0%	1.0V



REV 0.2

Date	Page	Description
09/27		Update Rev0.1 to Rev.0.2
10/16	8	Change U32(SSC) source from CLK_VCH to CLK_MCH_48M
	8	Change Q55 R537 R538 to U33A
	13	Add zero Ohm resistor between pin3 of JP1 and GND.
	15	Add R539 R540 2.2K pull high to +3VALW on net SMB_DATA and SMB_CLK
10/17	17	Add R549 on ICH4 GPI7 pull high to +3VS
	26	Add J3 between +5VS and +5VS_IDE
	17	Delete net USB_EN# and PAL/NTSC# on U12 pinW4 & pinW1
	29	Modify BlueTooth schematic
	32	Add Pass-High Filter (R550, R551, C676, C677) on net AMP_LEFT, AMP_RIGHT
	32	Change R465 power plan from +5VS to +5VCD
	34	Add Net Thertrip#, PM_SLP_S1#, BT_RST# on EC
10/18	35	Change U23 to U22B
	36	Change FAN Schematic from PWM to RPM
10/18	37	Add R541 and R542 100K pull high to +3VALW on net Button1#, Internet#
10/22		Formal release Schematic Rev0.2
10/24	44	Add P4-M/P4-C auto detection schematic, PQ44, PR155
11/18	42	Change PC43 to 4.7U
11/18	40	Change PR32 to 2.8K, PR41 to 2.32K
11/20	34	Add R575, R576, R577, R578, R579 between device PME#s and EC_PME#

Compal Electronics, Ltd.			
Title			
PIR			
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