

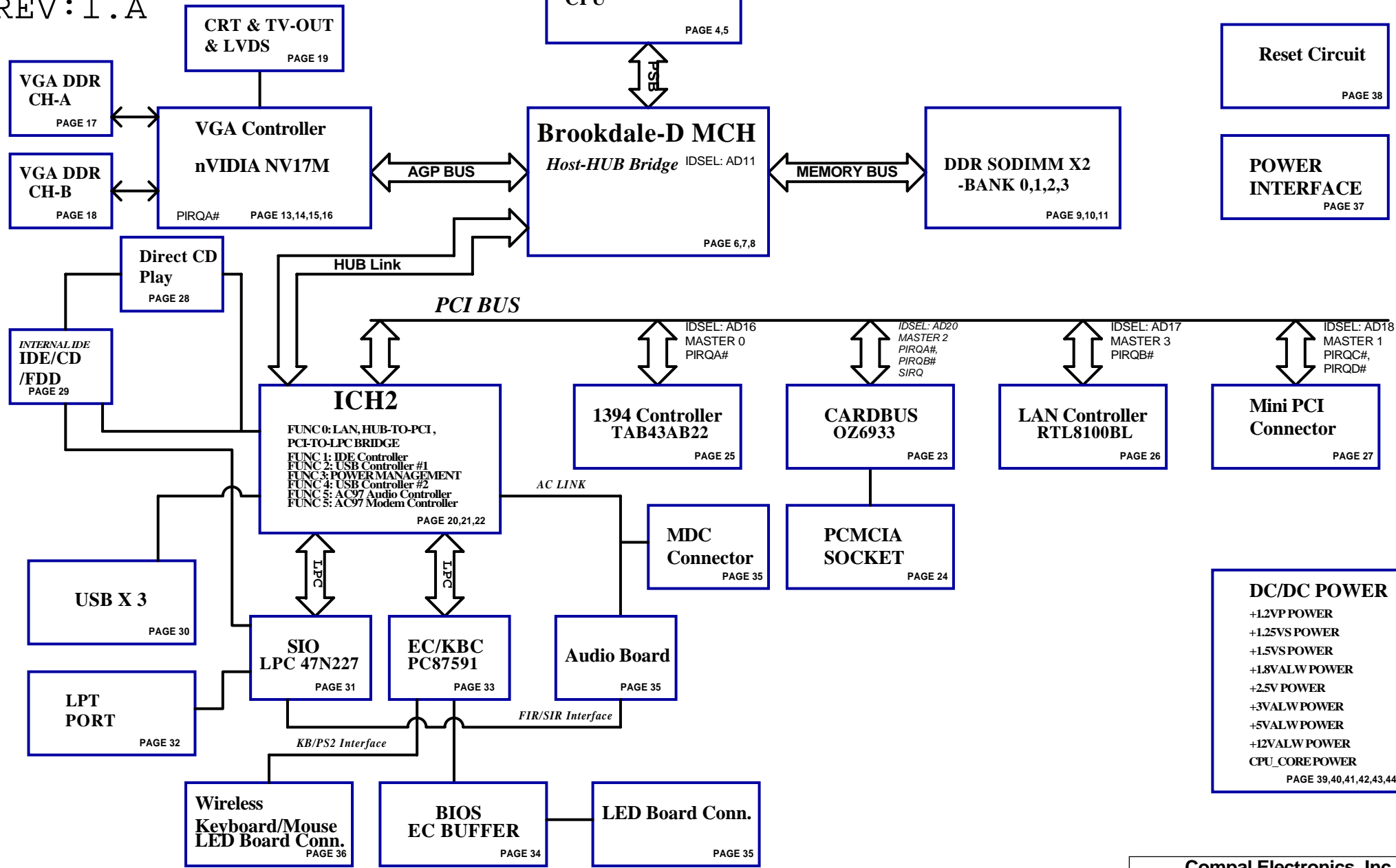
# ***ATR60 LA-1432 REV1.A Schematics Document***

**Intel Pentium 4 Processor it the 478-pin  
Package      with 845D chipset**

Title			<b><i>Compal Electronics, Ltd.</i></b>		
Size			Document Number		
B			LA1432		
Date:			Sheet 1 of 45		
Rev			1.A		

MODEL NAME : ATR60 LA-1432

REV:1.A



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## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_VCC	Core voltage for CPU	ON	OFF	OFF
+1.2VP	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	AGP 4X	ON	OFF	OFF
+1.8VALW	1.8V power rail	ON	ON	ON*
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
VGA			PIRQA
CardBus	AD20	2	PIRQA/PIRQB
LAN	AD17	3	PIRQB
Mini-PCI	AD18	1/4	PIRQC/PIRQD
1394	AD16	0	PIRQA

## EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	MAX1617MEE	1001 110X b
EEPROM(24C16/02)	1010 000X b	OZ163	0011 0100 b
(24C04)	1011 000Xb	Smart Battery	0001 011X b
		Docking	0011 011X b
		DOT Board	XXXX XXXXb

## ICH2 SM Bus address

Device	Address
Clock Generator ( ICS9238-50)	1101 0000
SDRAM Select ( 74HC4052 )	1010 0000
CPU Voltage VID select ( F3565 )	0110 111Xb

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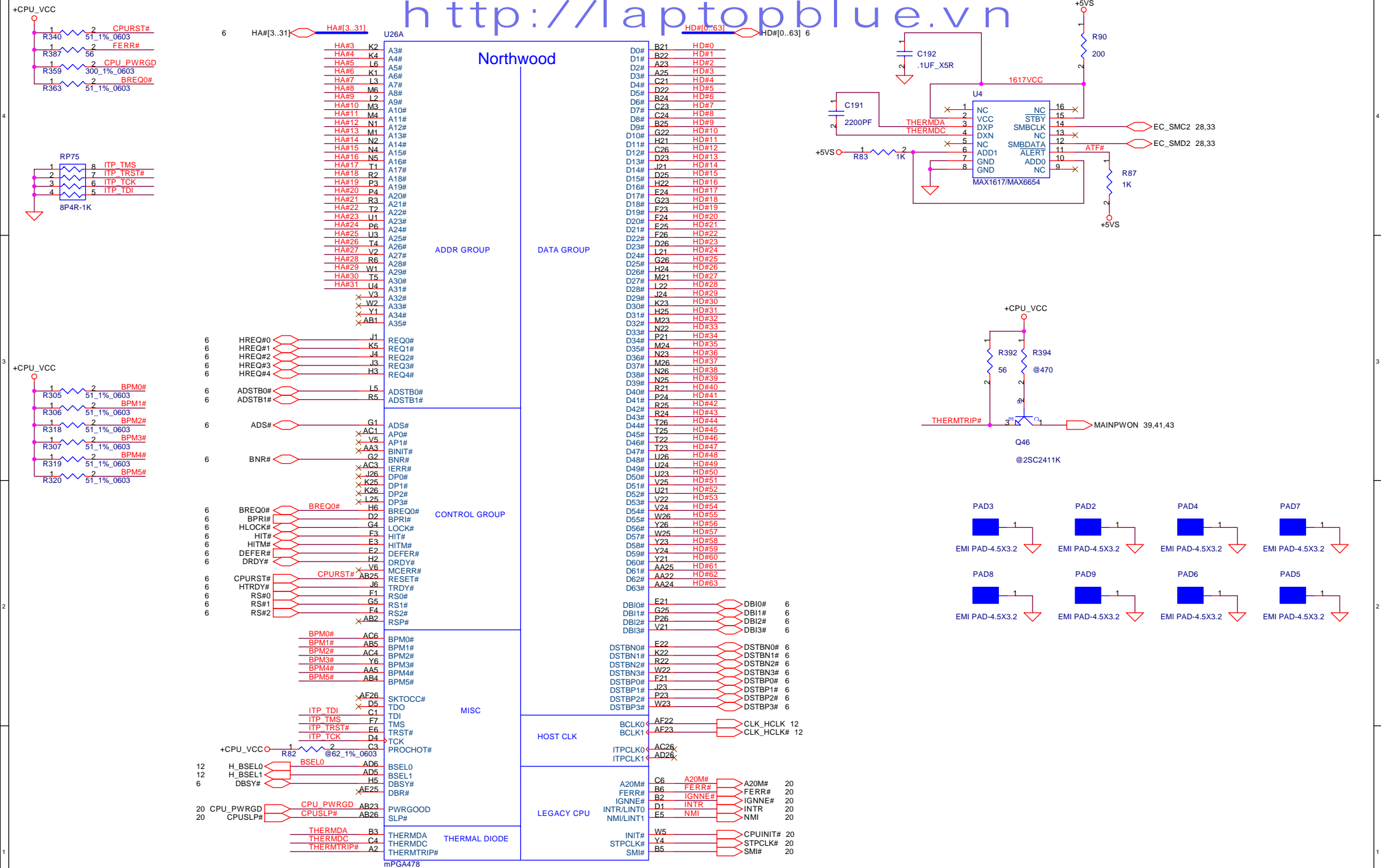
## Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID0	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0V	0V	0V
1	47K +/- 5%	0.921 V	1.055 V	1.204 V
2	100K +/- 5%	1.453 V	1.650 V	1.759 V
3	NC	2.5 V	3.3 V	3.465 V

Vcc	3.3V +/- 5%			
Rc	100K +/- 5%			
Board ID1	Rd	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0V	0V	0V
1	47K +/- 5%	0.921 V	1.055 V	1.204 V
2	100K +/- 5%	1.453 V	1.650 V	1.759 V
3	NC	2.5 V	3.3 V	3.465 V

Real Board ID	Board ID1	Board ID0	PCB Revision
0	0	0	0.1
1	0	1	1.0
2	0	2	
3	0	3	
4	1	0	
5	1	1	
6	1	2	
7	1	3	
8	2	0	
9	2	1	
10	2	2	
11	2	3	
12	3	0	
13	3	1	
14	3	2	
15	3	3	

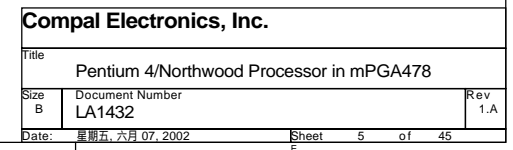
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Title	Notes & PIR		
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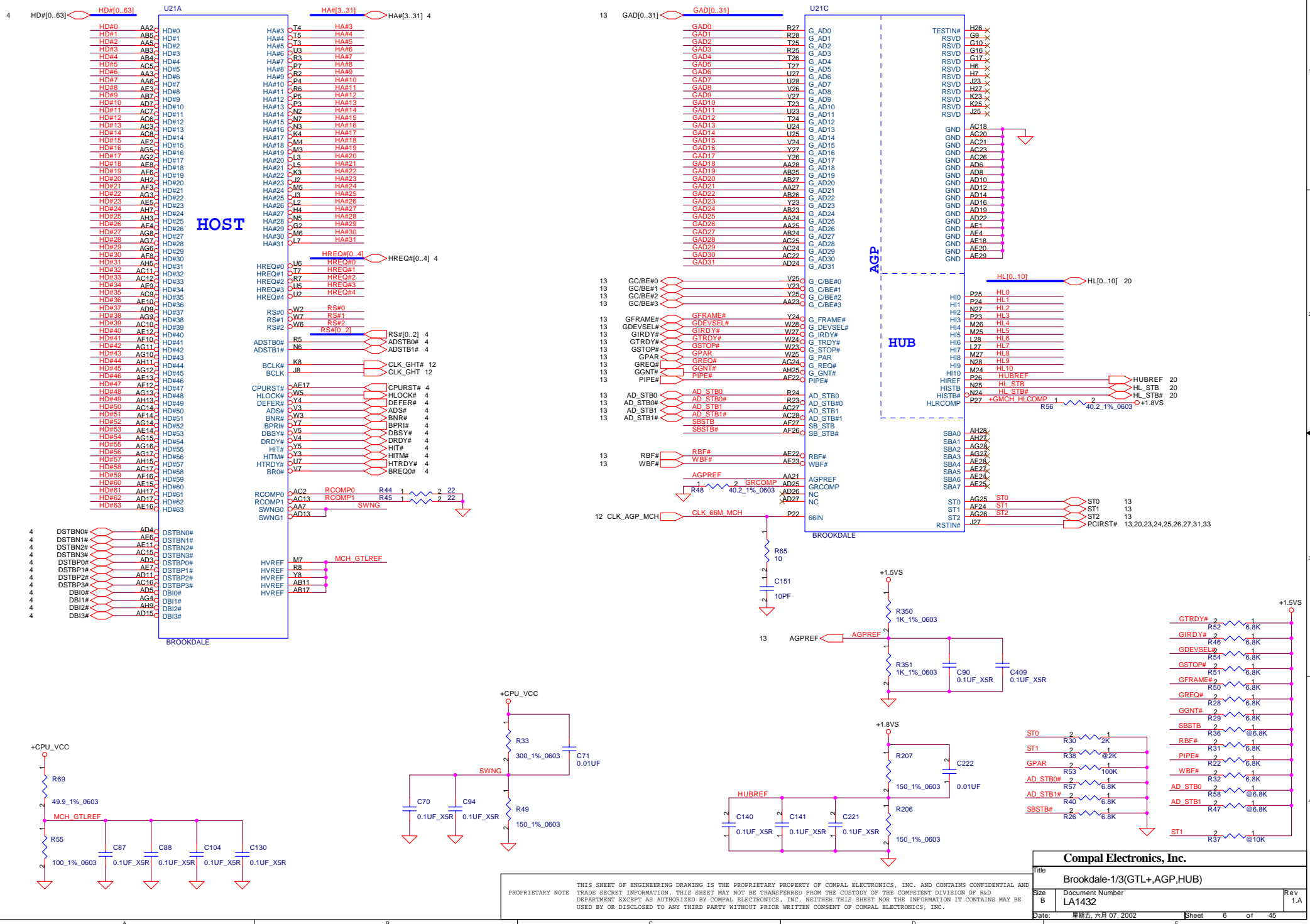


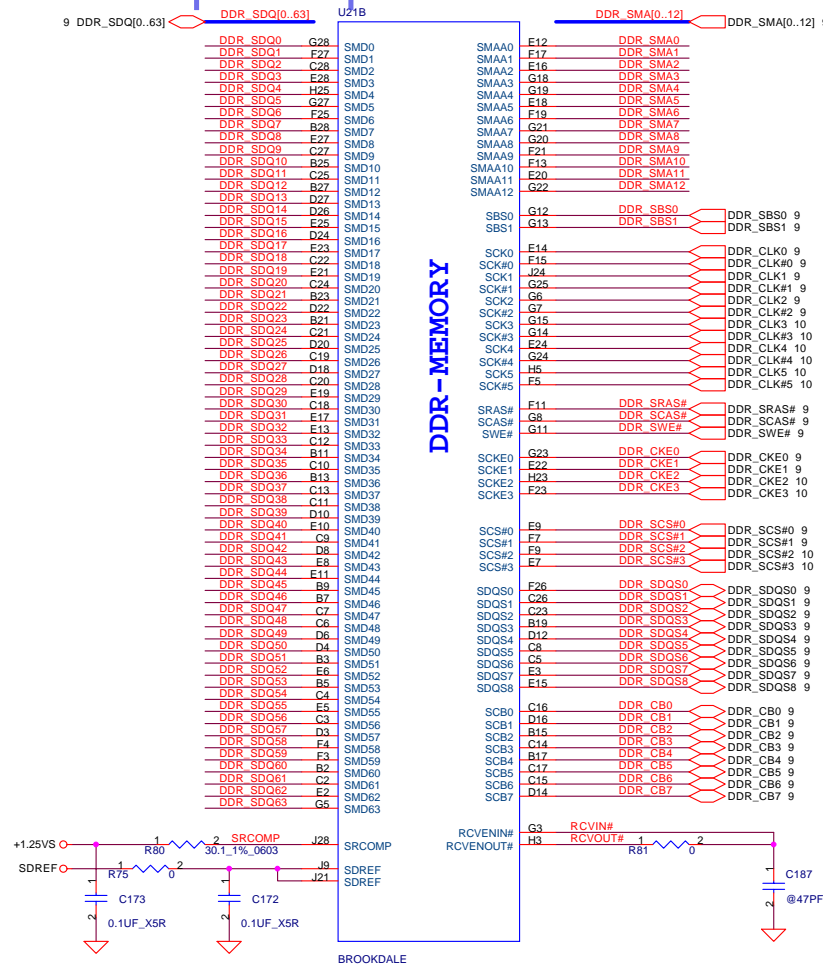
SELPSB[1:0]	STSEM BUS FREQUENCY
00	100MHZ
01	RESERVED
10	RESERVED
11	RESERVED

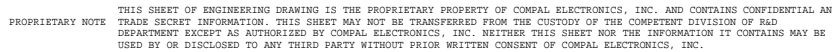
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Title			
Pentium 4/Northwood Processor in mPGA478			
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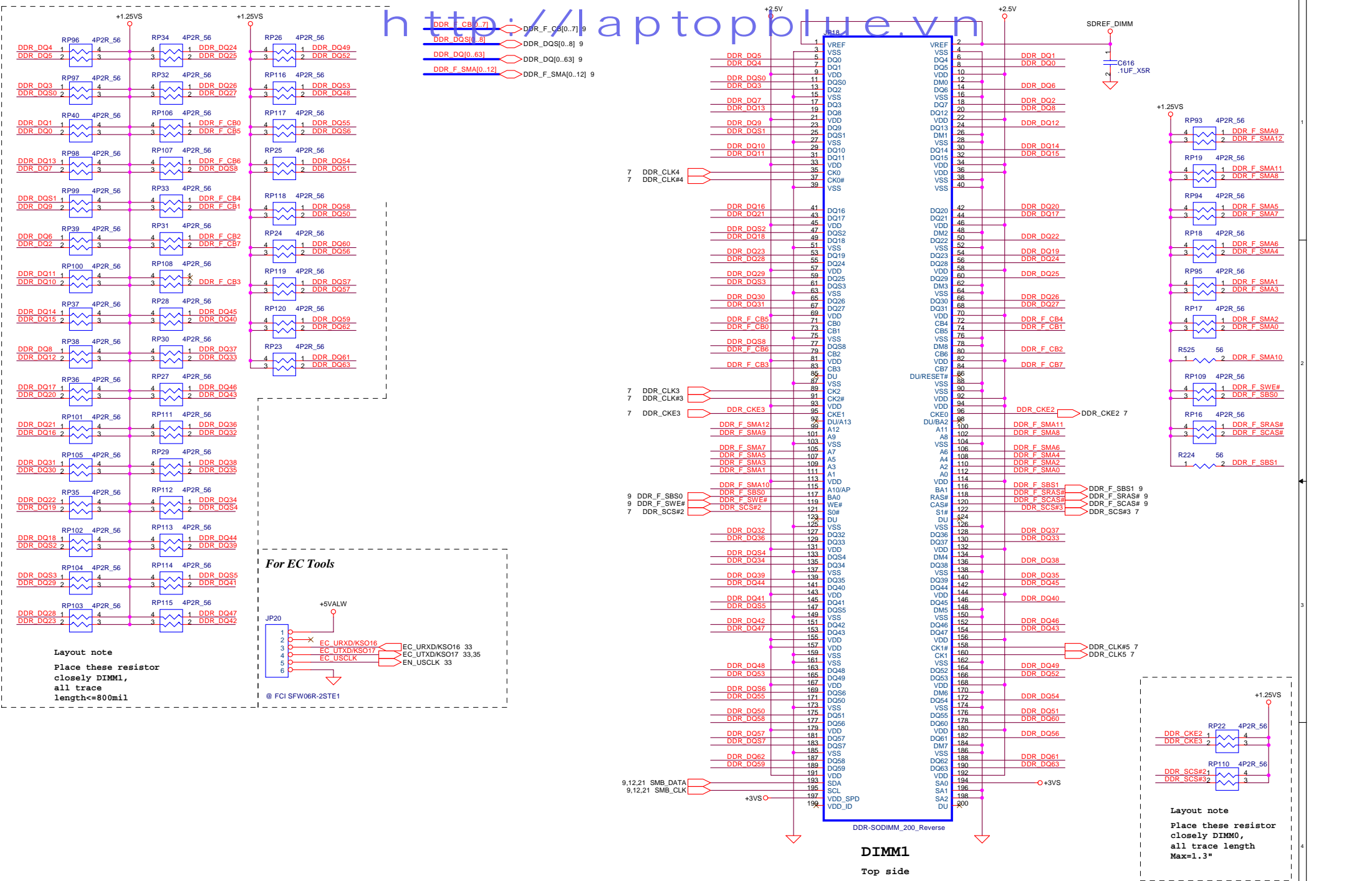






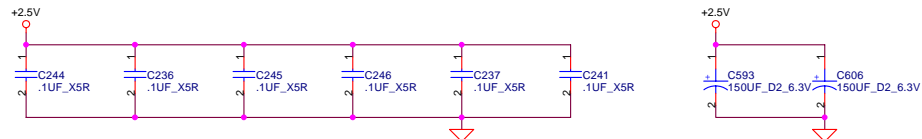
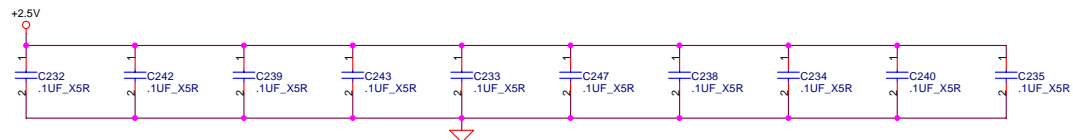


<b>Compal Electronics, Inc.</b>					
Title	<b>DDR-SODIMM SLOT1</b>				
Size B	Document Number <b>LA1432</b>				Rev 1.A
Date:	星期五, 六月 07, 2002		Sheet	9	of 45

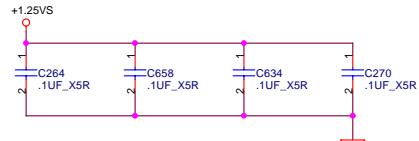
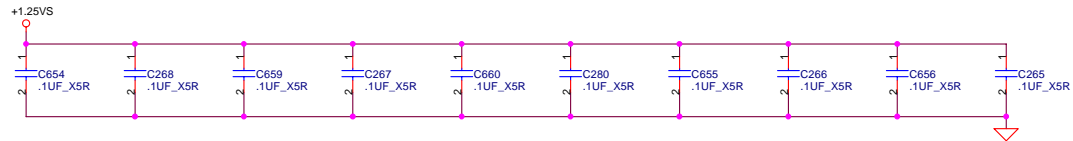
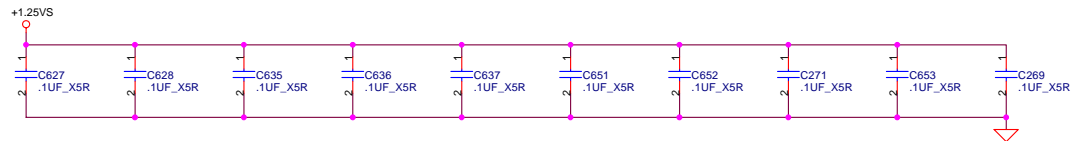
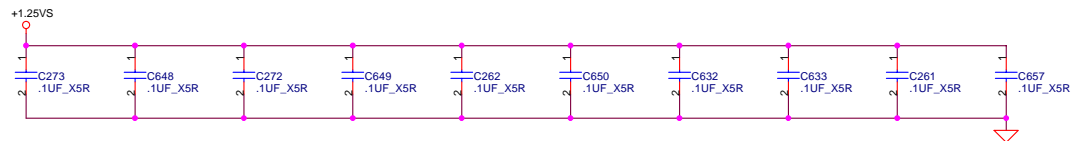
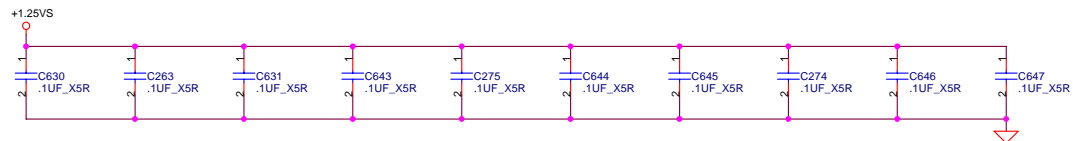
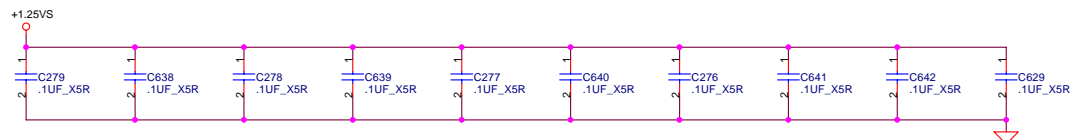


Layout note :  
Distribute as close as possible  
to DDR-SODIMM.

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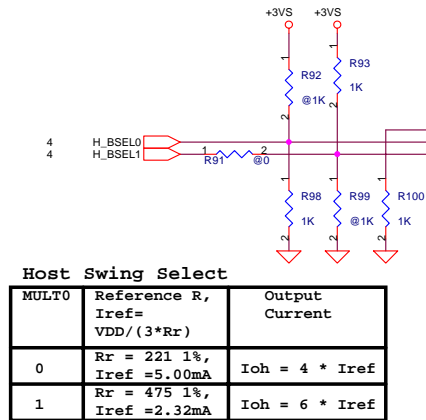
Layout note :  
Place one cap close to every 2 pull up resistors termination to  
+1.25V



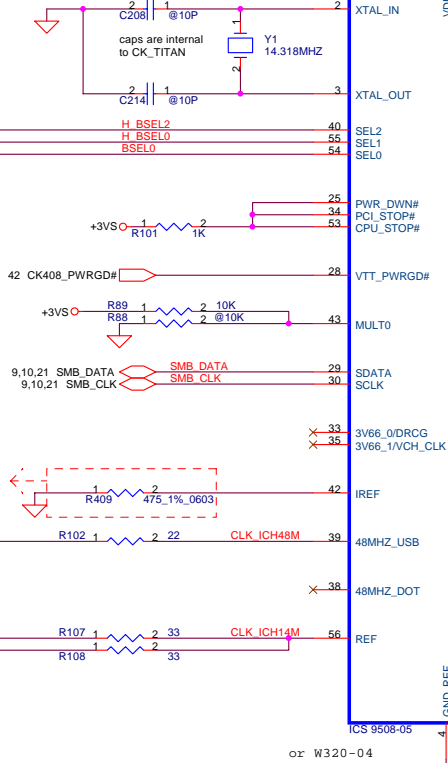
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Title			
DDR SODIMM Decoupling			
Size	Document Number		Rev
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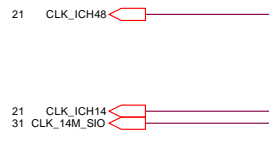
SEL1	SEL0	Function
0	0	66MHz Host CLK
0	1	100MHz Host CLK
1	0	200MHz Host CLK
1	1	133MHz Host CLK

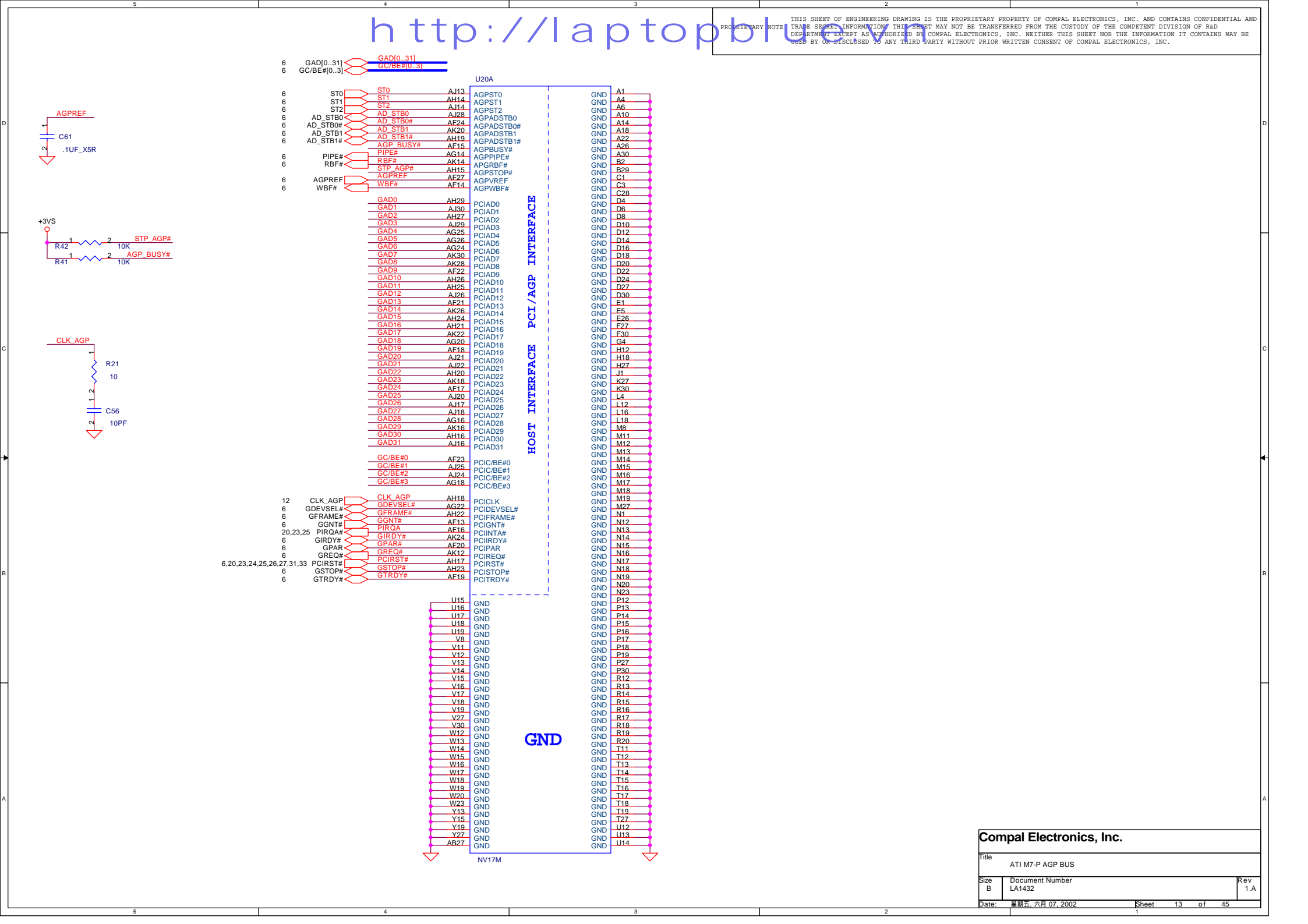


Place Crystal within 500 mils of CK\_Titan



Please closely pin42

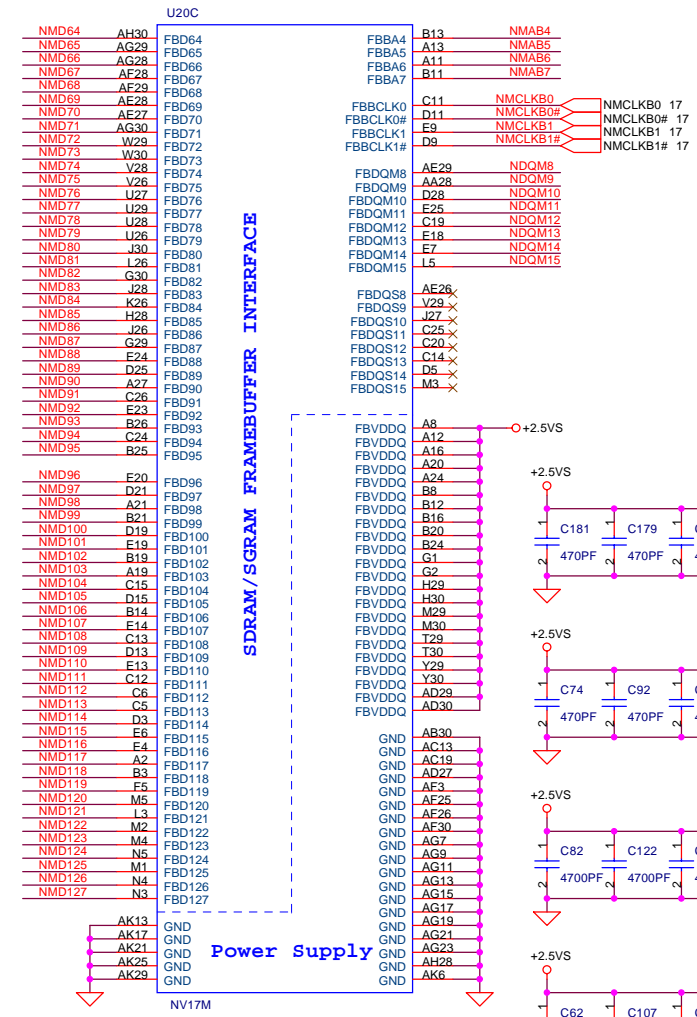
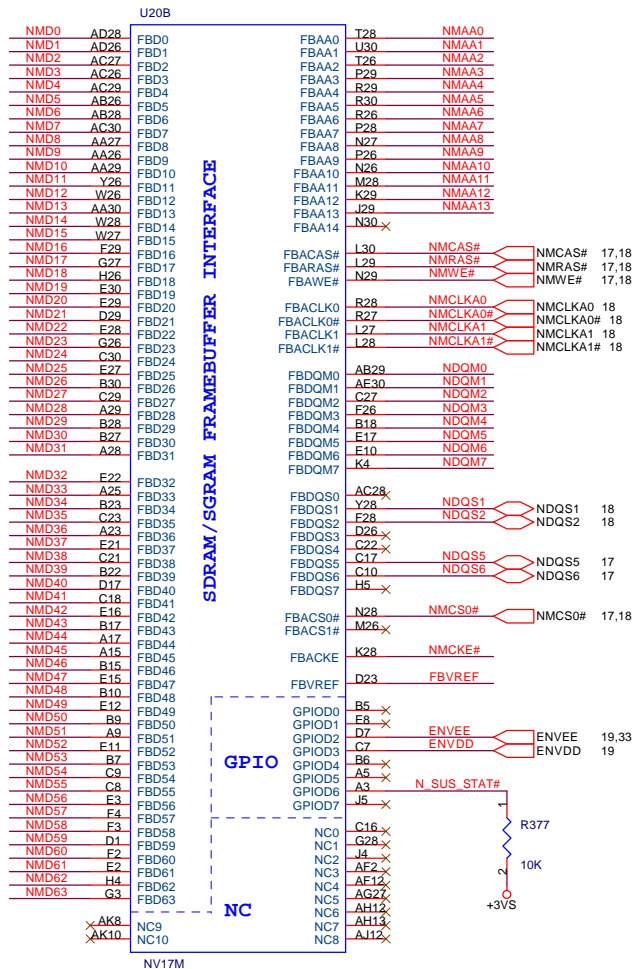


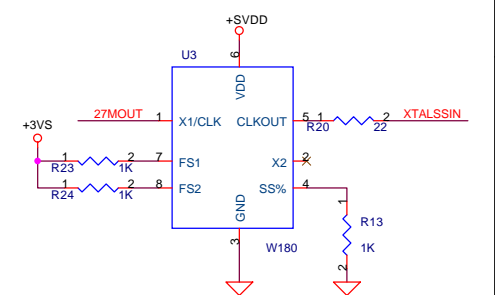
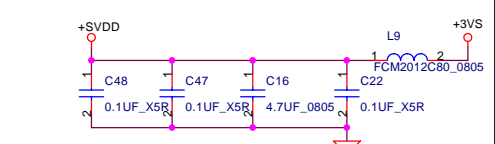
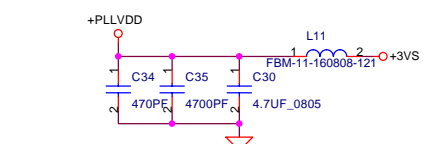
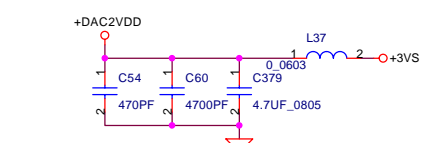
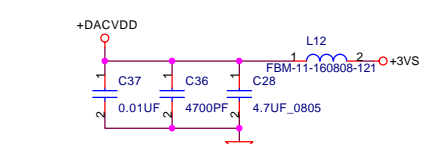
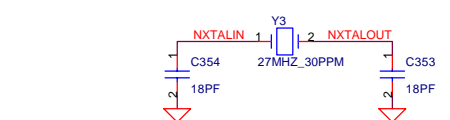
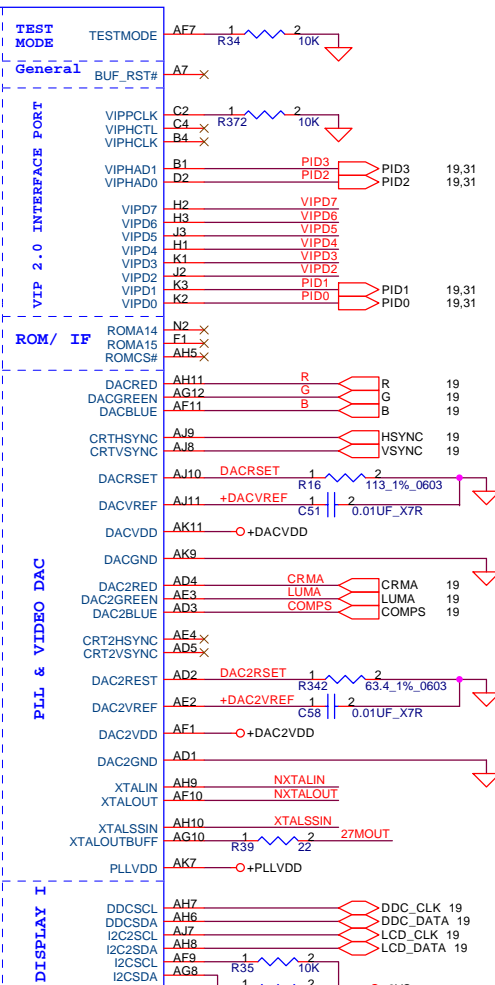
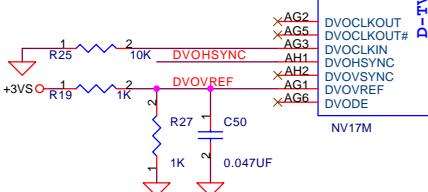
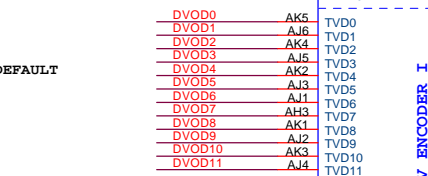
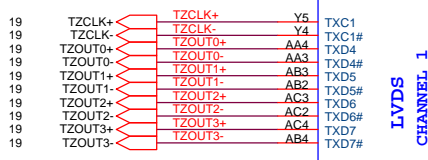
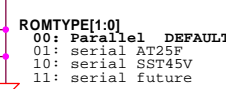
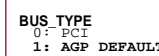
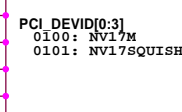
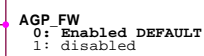
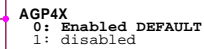
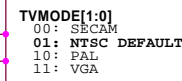
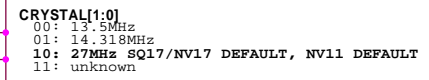
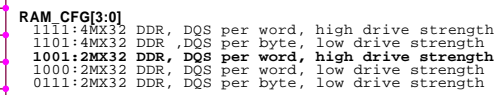
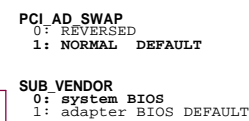
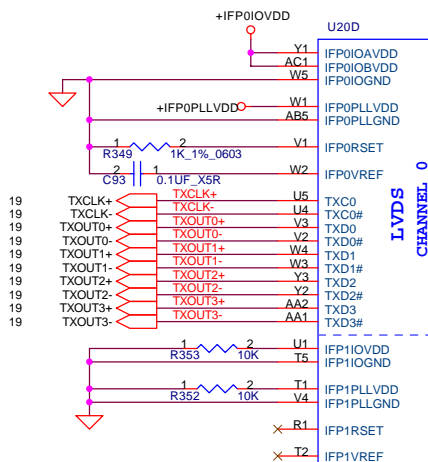
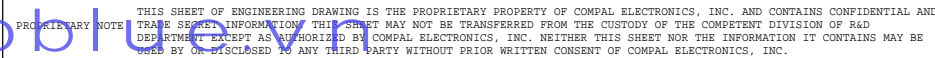


17,18 NMD[0..127] NMDA[0..13] NMD[0..127] NMDQ[0..15]

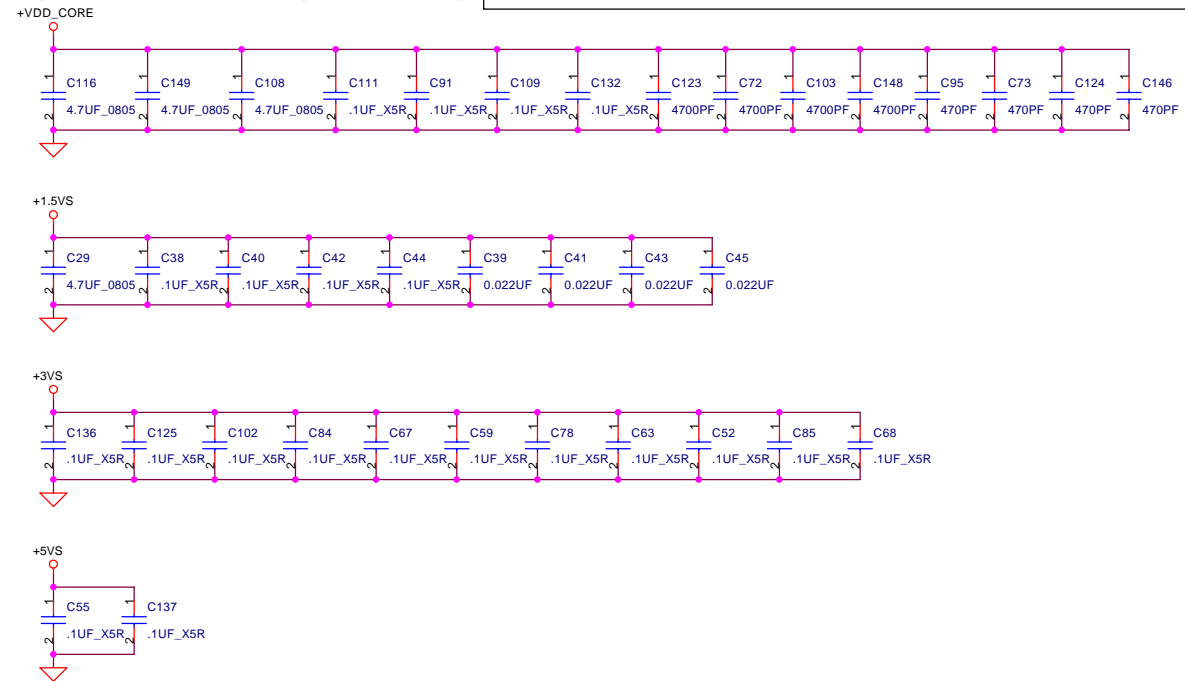
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17,18 NMDA[4..7] NMDA[4..7]









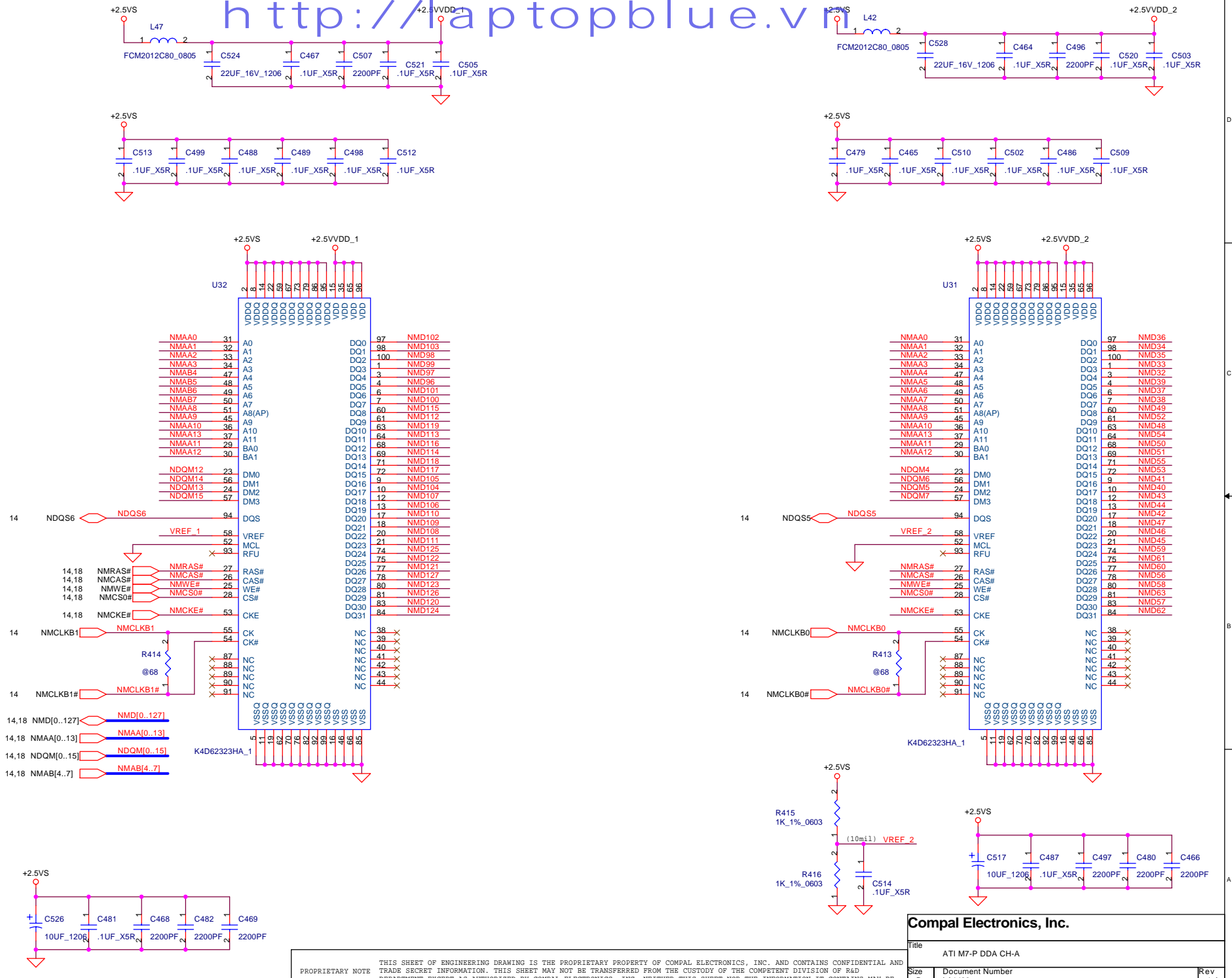
+1.2V +/-50mV, 3.5A



Title			
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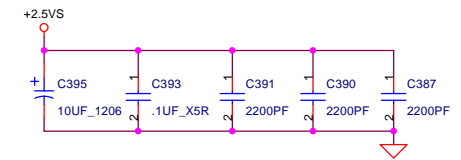
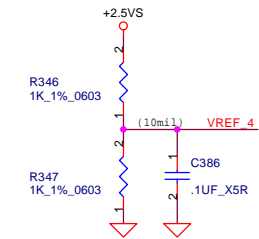
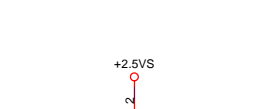
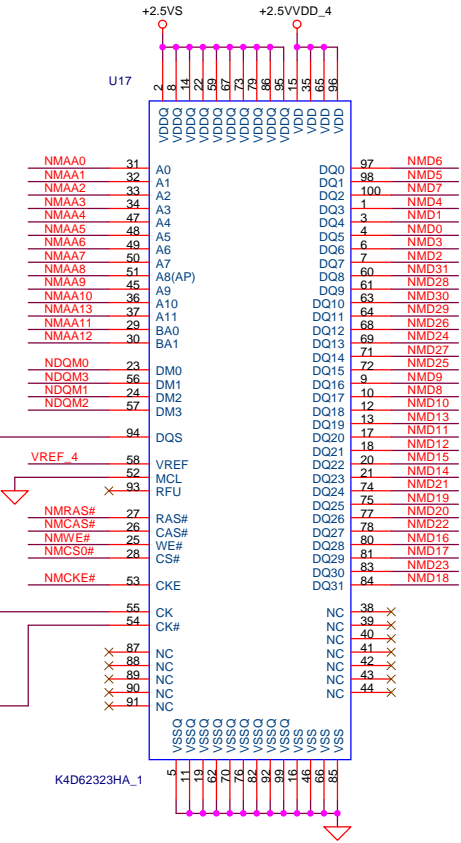
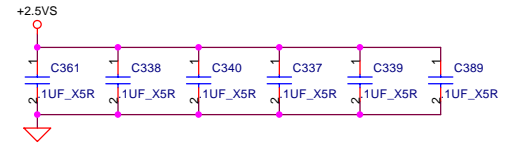
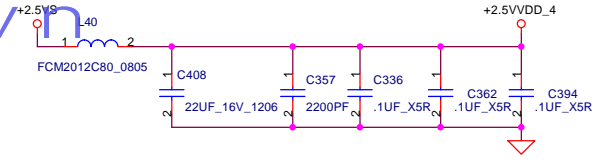
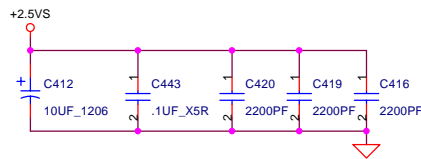
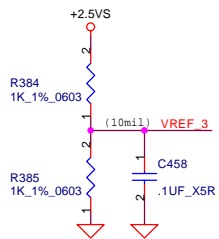
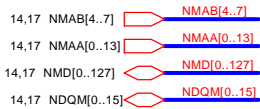
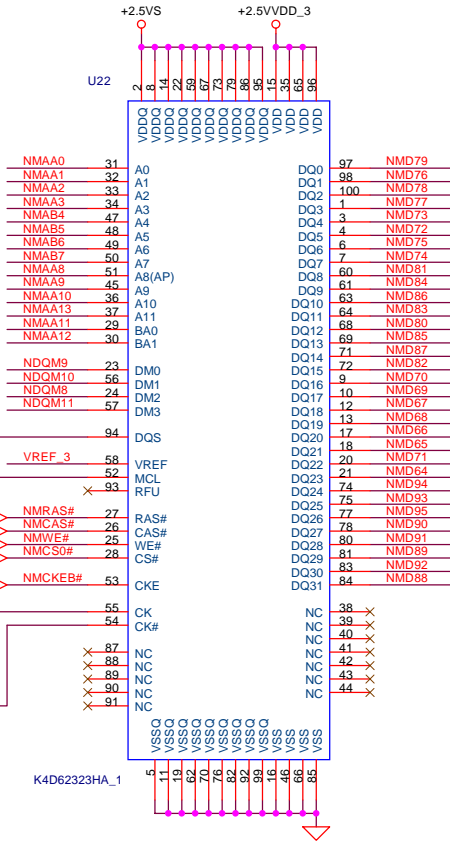
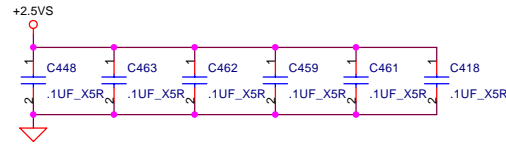
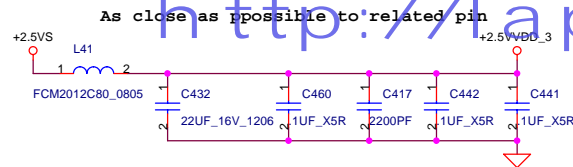
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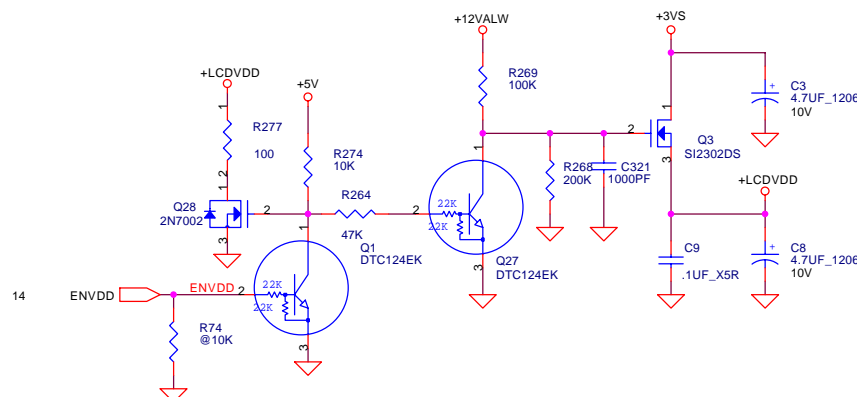
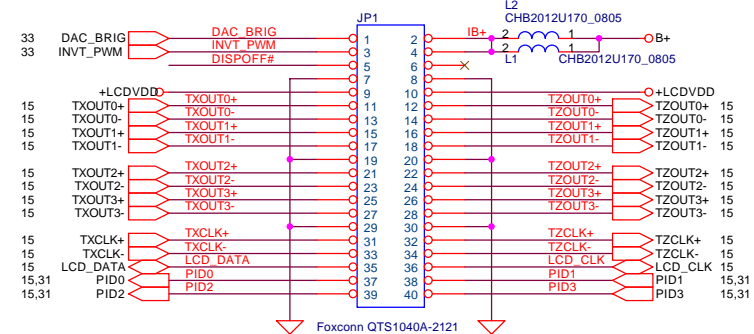
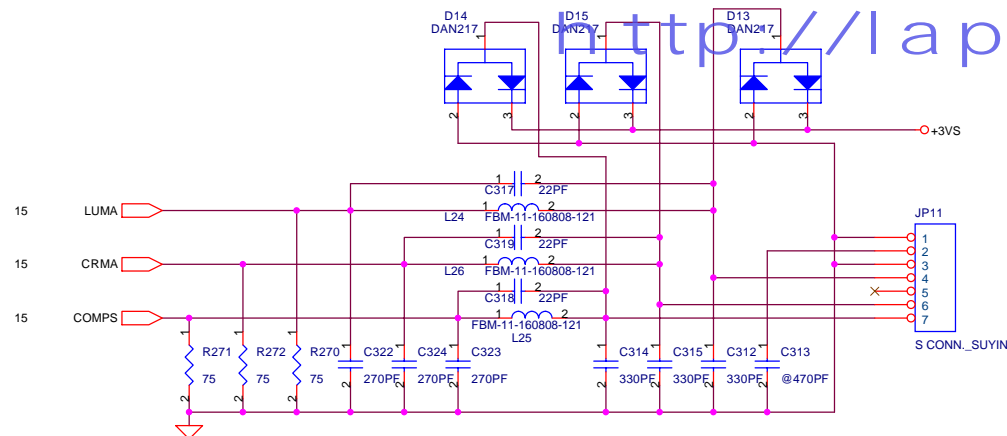
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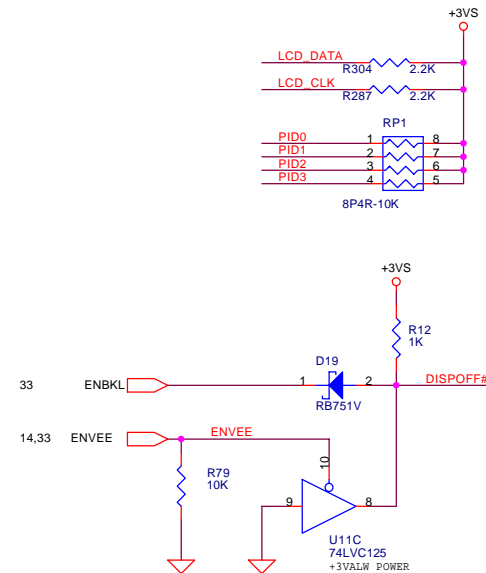
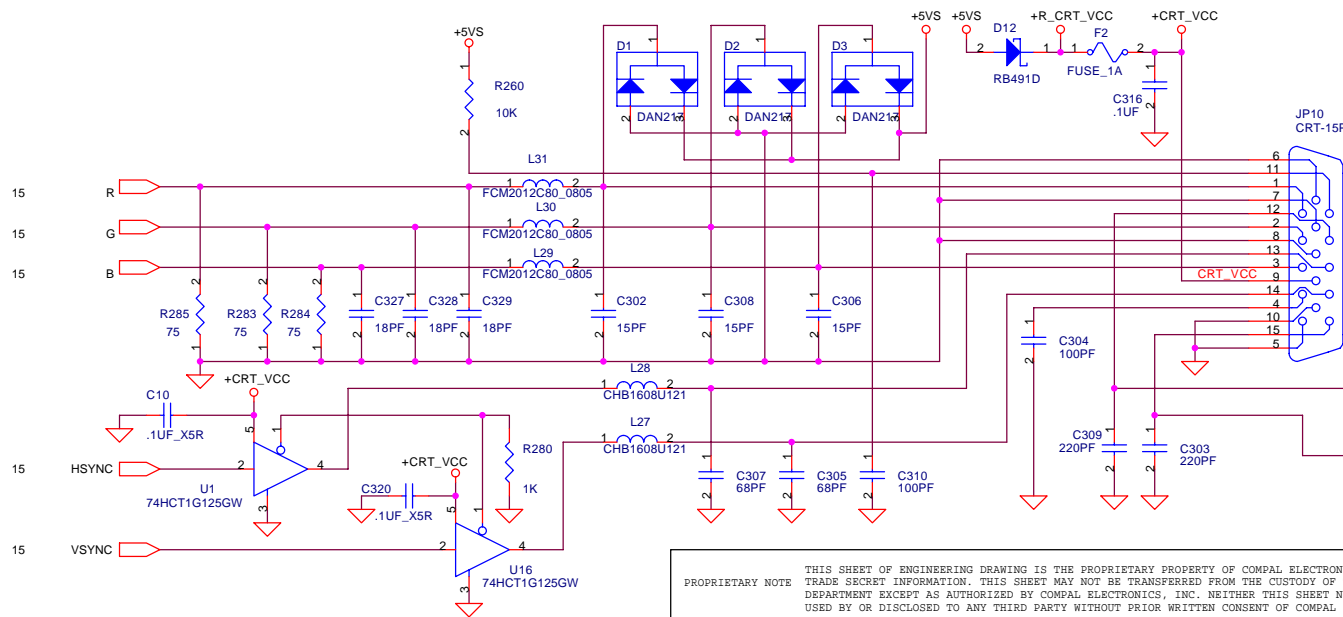


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Title: ATI DDR CH-B for M7P Only		
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## CRT Connector

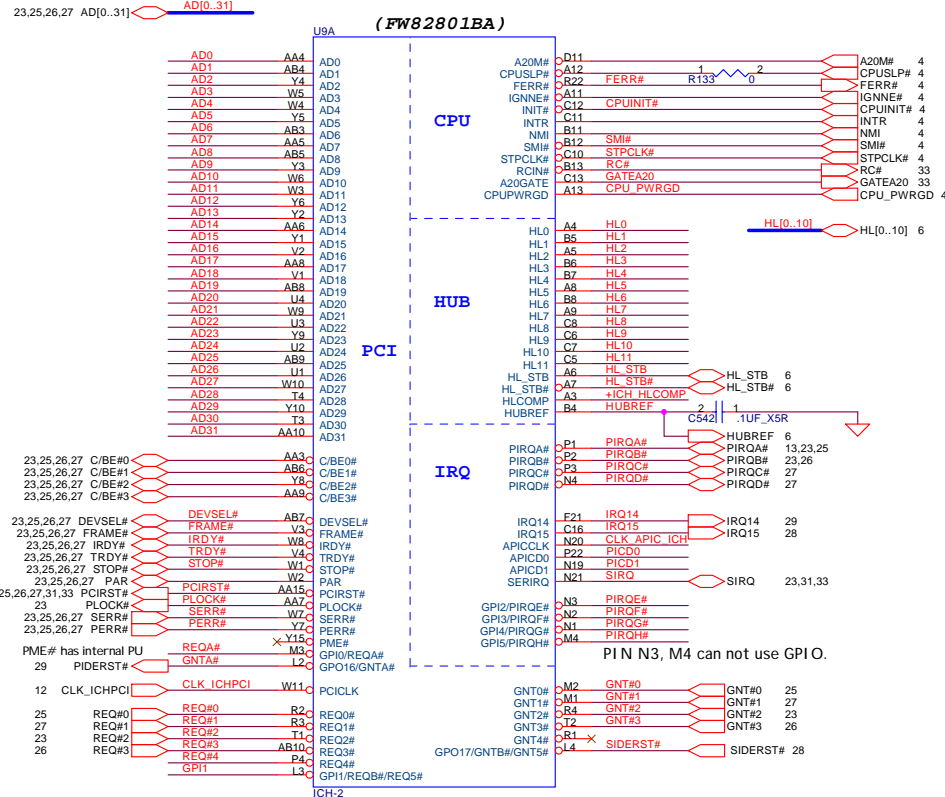


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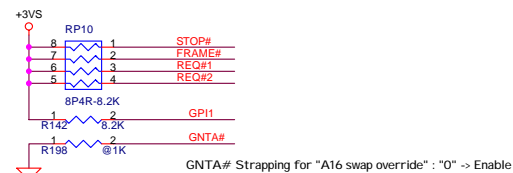
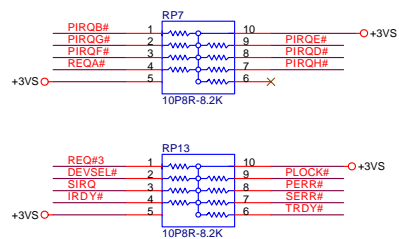
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B	LA1432		
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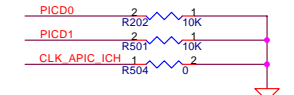
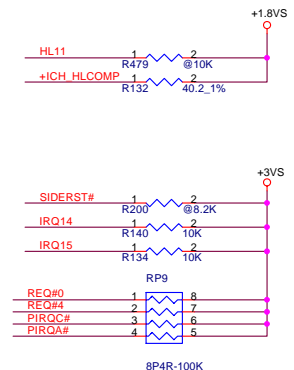
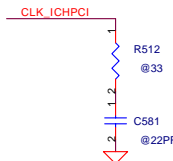
# ICH-2



## PCI Pullups



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REQ#1	WLAN
REQ#2	PCMCIA CONTROLLER
REQ#3	LAN
REQ#4	NC

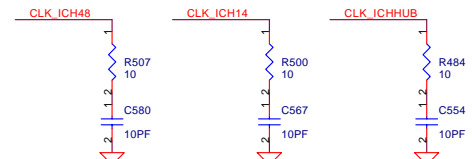
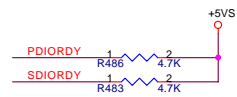
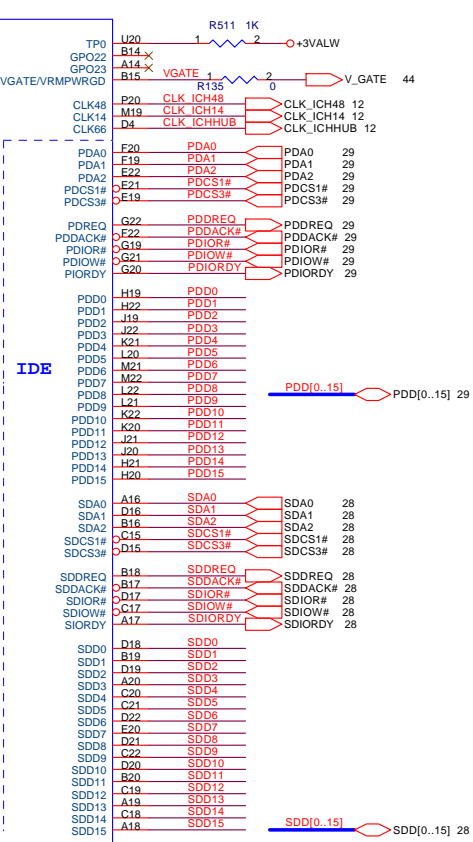
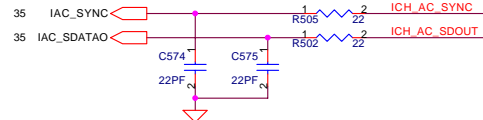
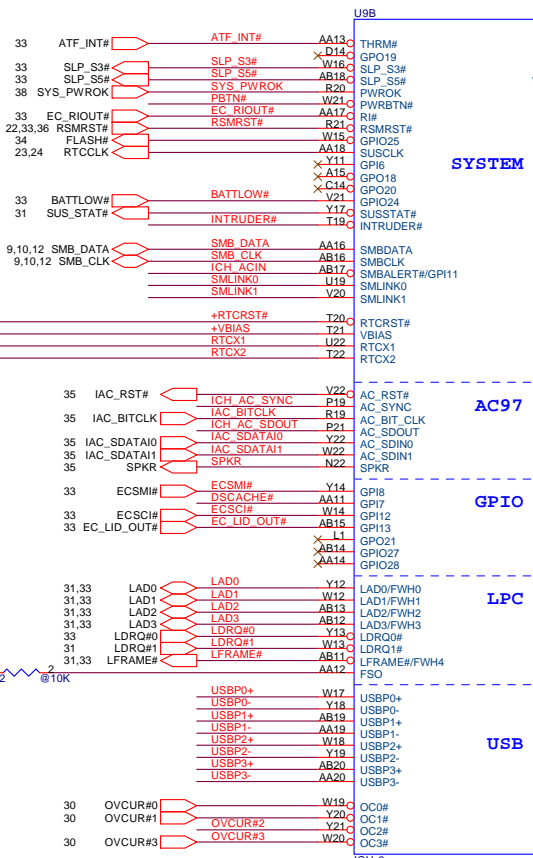
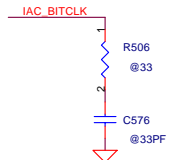
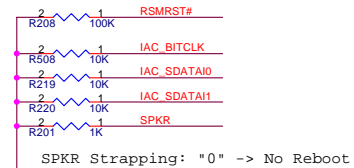
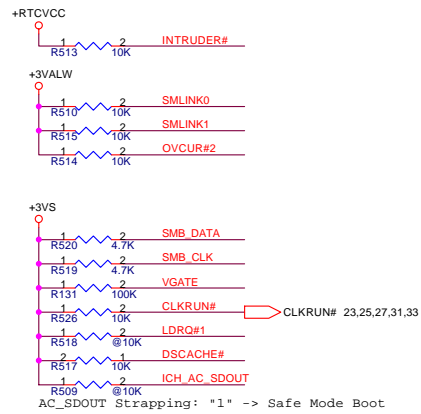
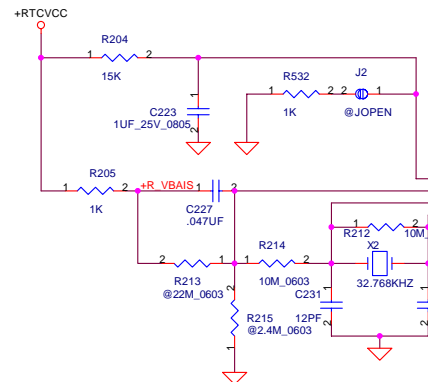
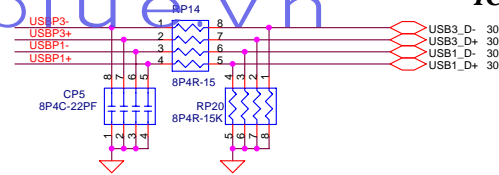
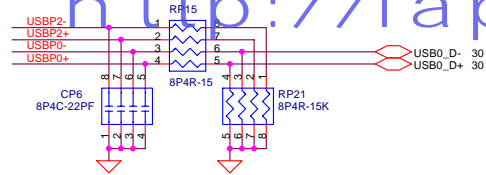
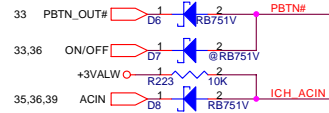


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ICH2-A(PCI,HUB,CPU) & FWH

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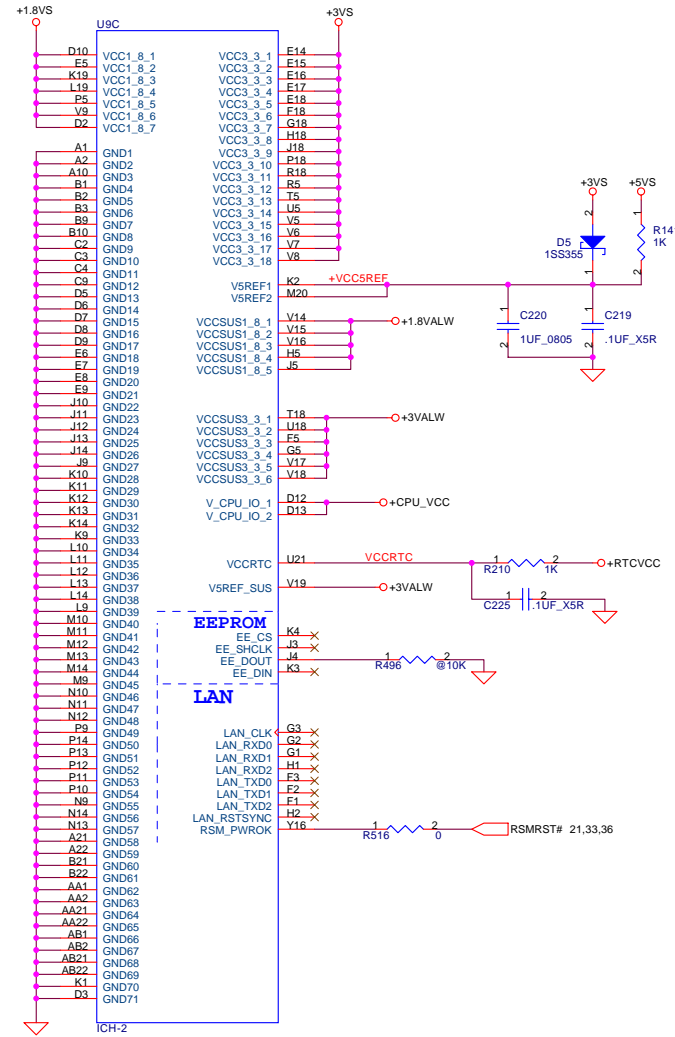
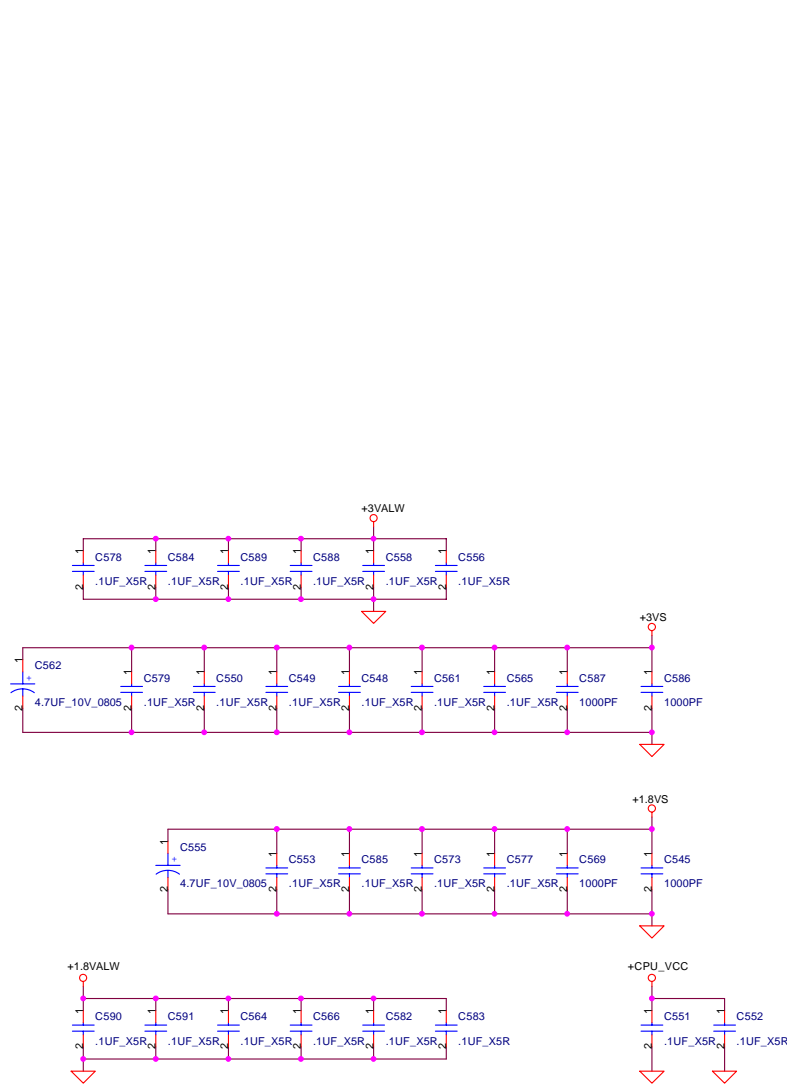
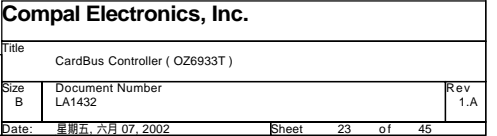
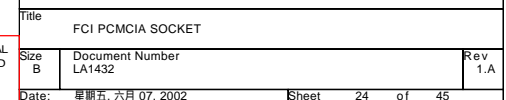
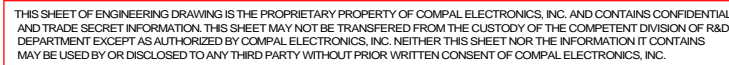


Diagram illustrating the address bus configuration for a 16MB memory system. The address is split into a 16-bit data bus (S1\_IOWR#, S1\_IORD#, S1\_OE#) and a 16-bit address bus (S1\_CBRST#, S1\_IOWR#, S1\_IORD#, S1\_OE#, S1\_OF#). The address bus is connected to a 16MB memory system.

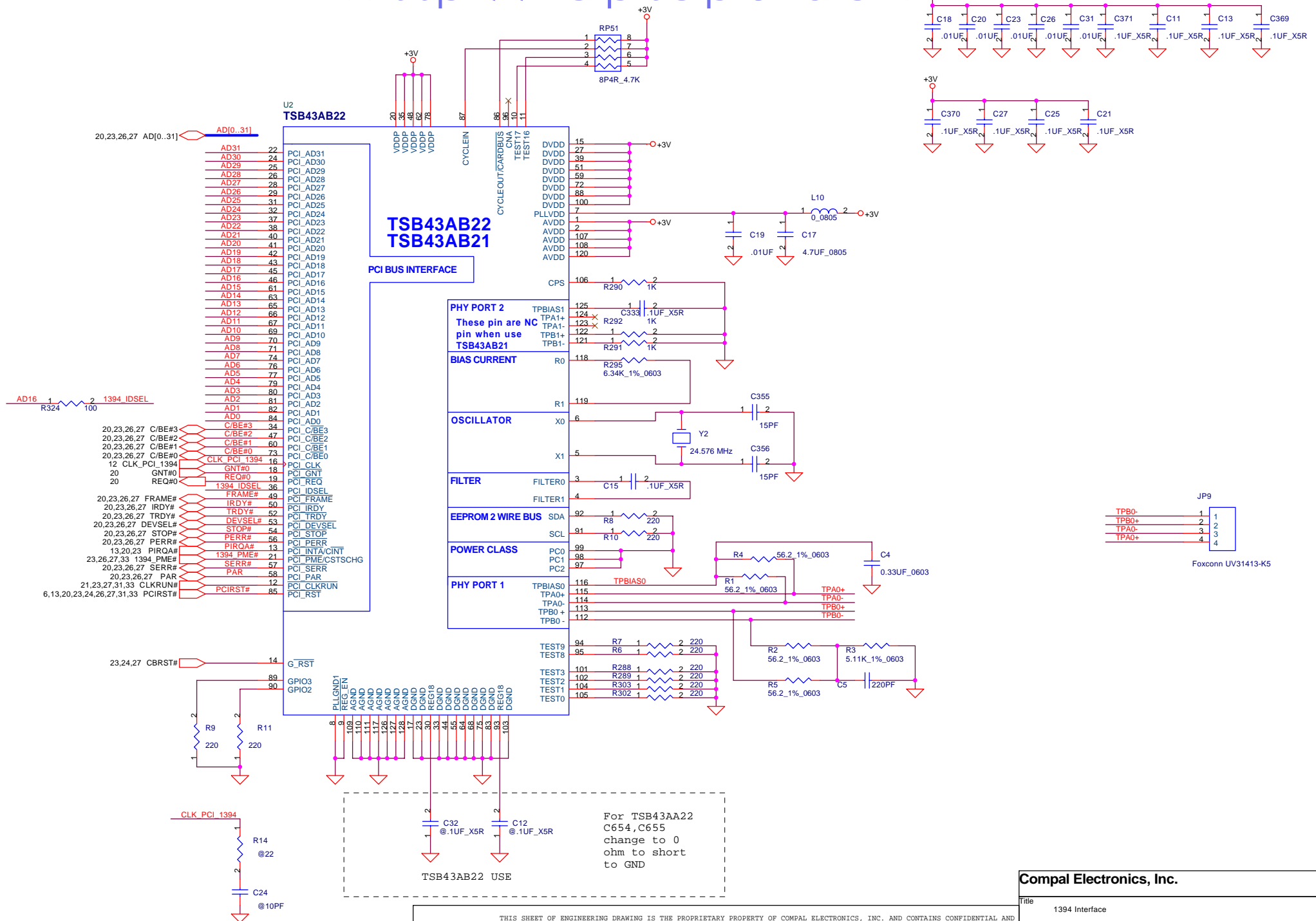


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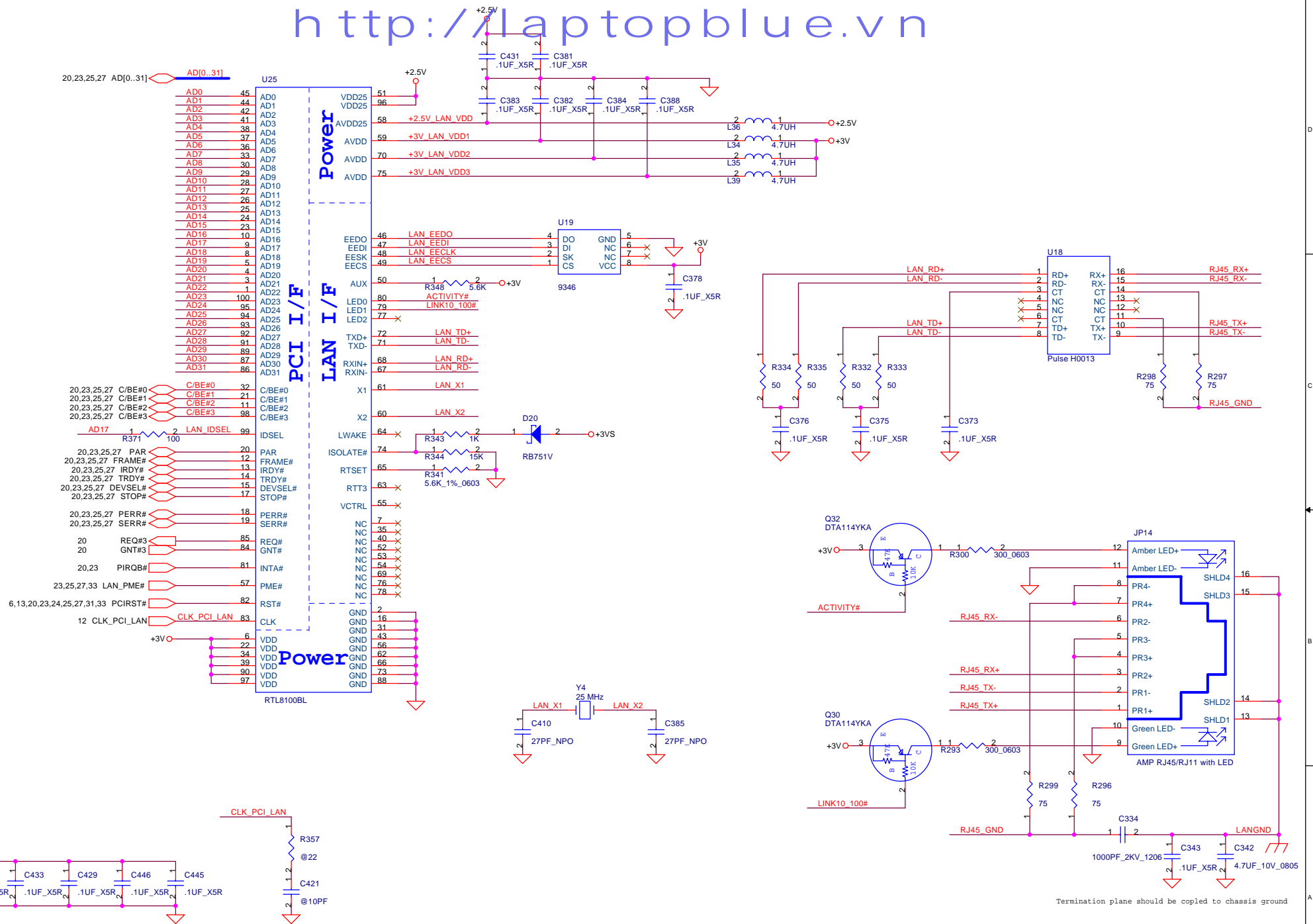
**Compal Electronics, Inc**

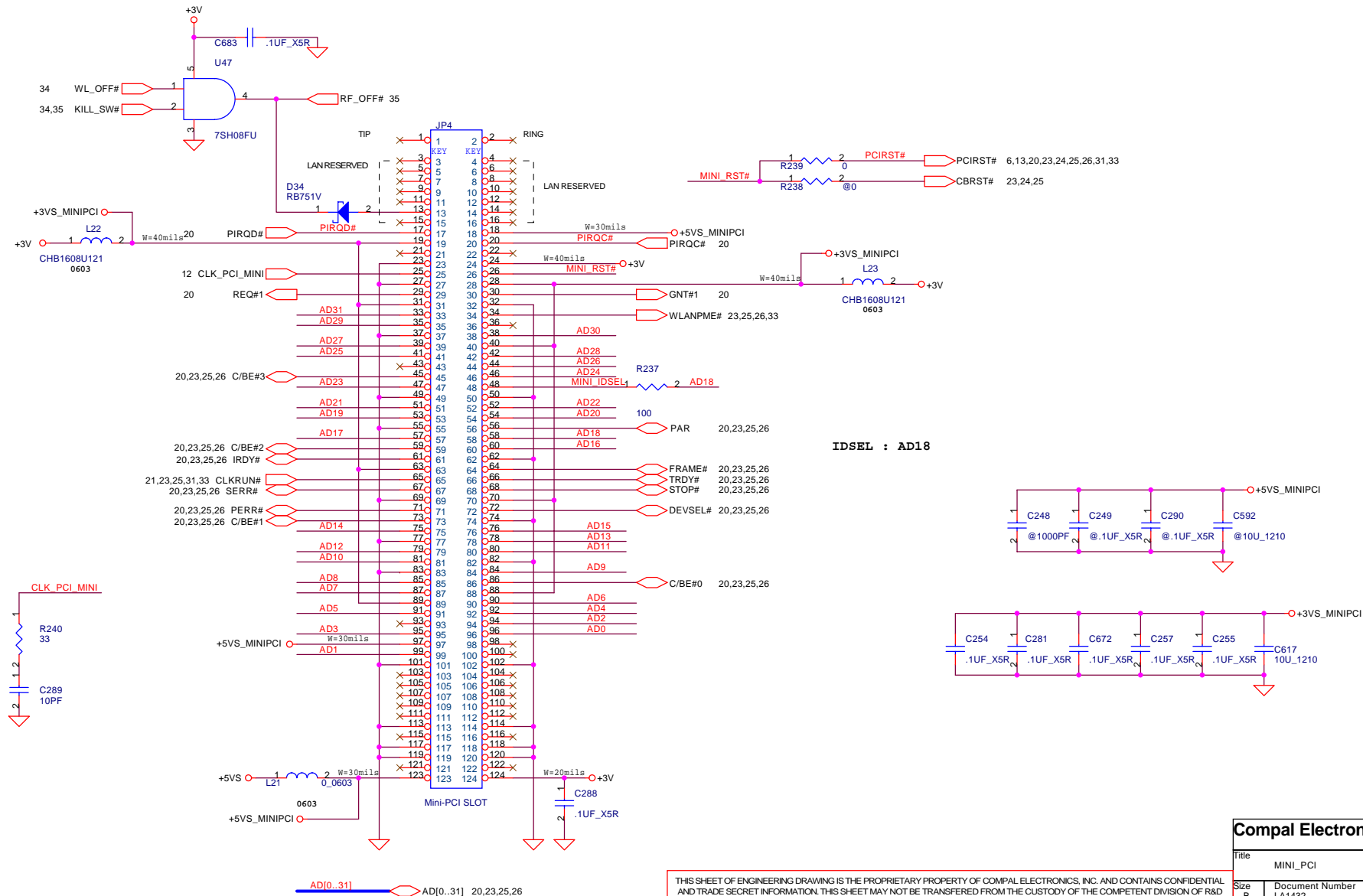


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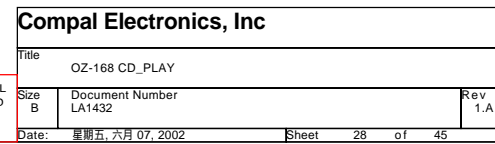


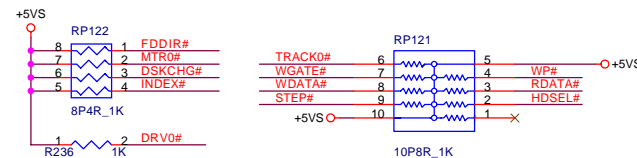
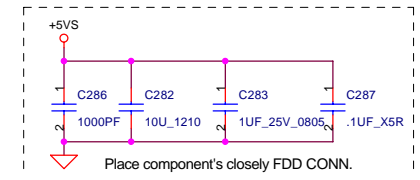
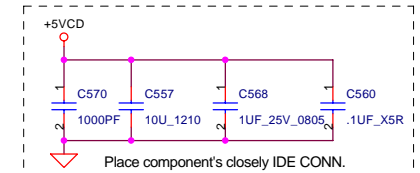
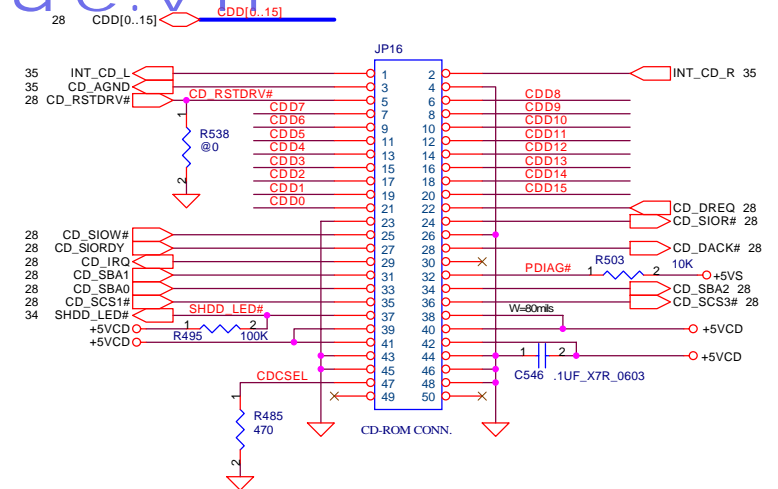
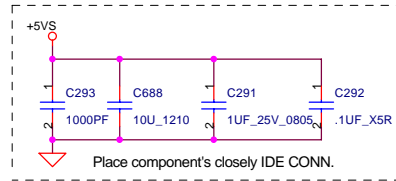
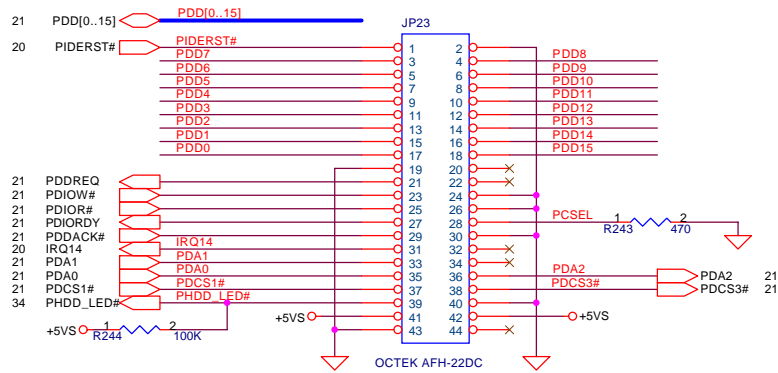


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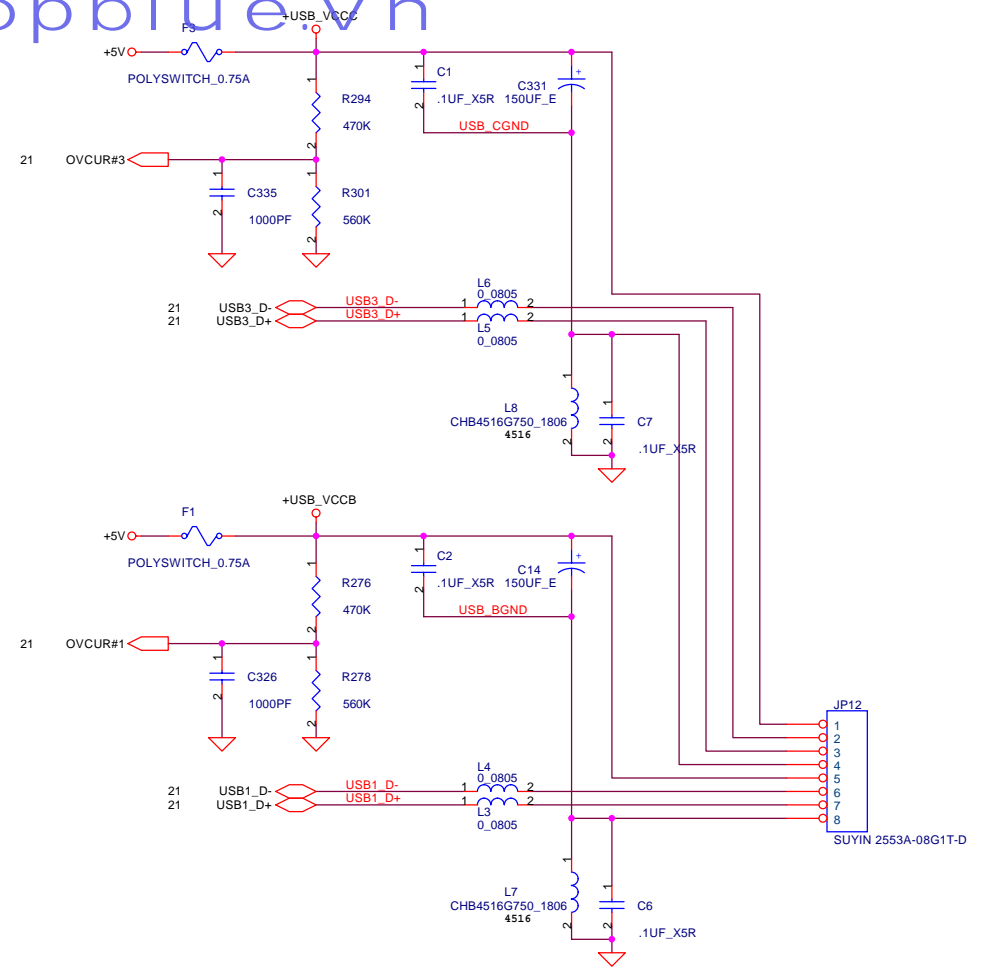
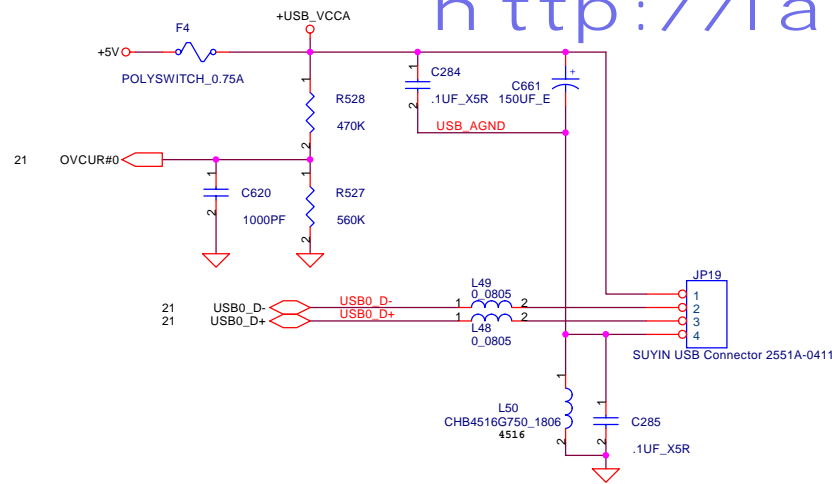
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IDE/ FDD MODULE CONN.

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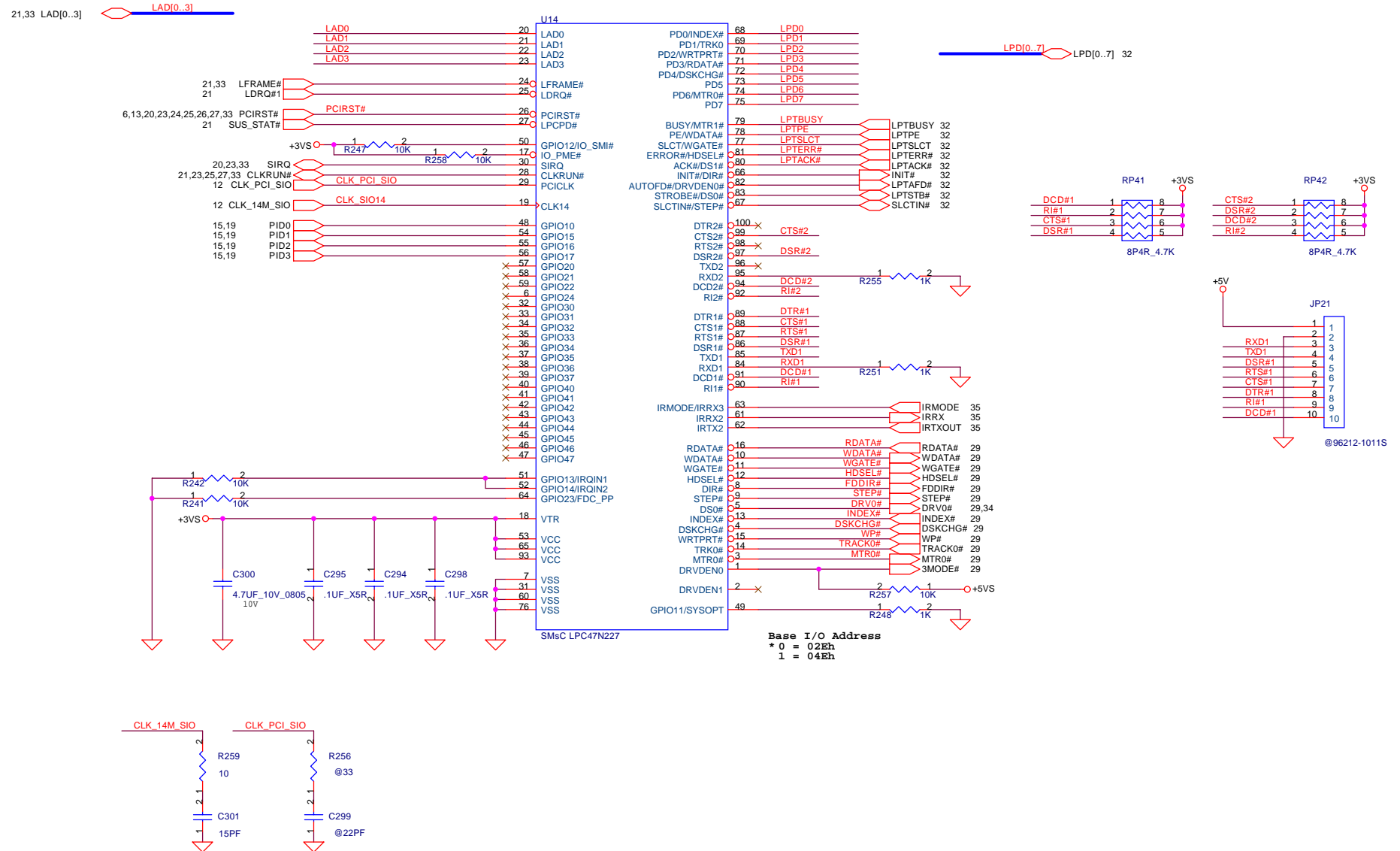


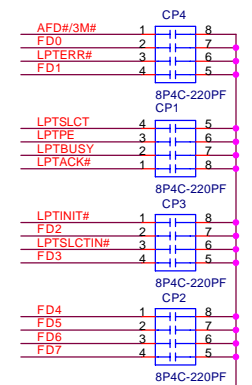
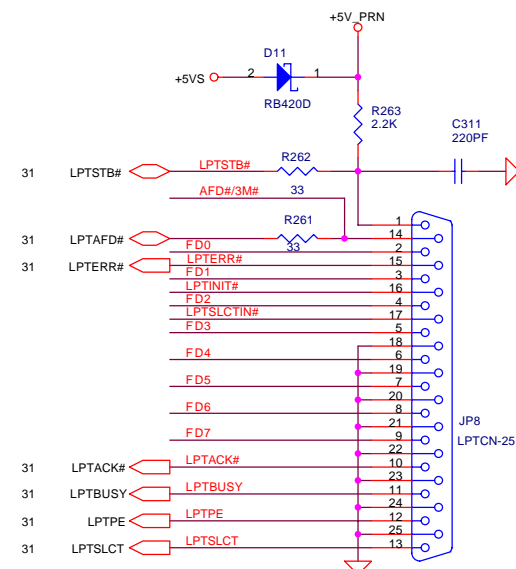
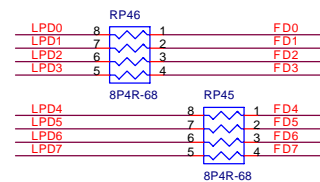
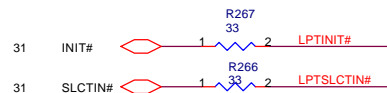
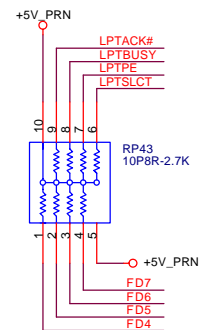
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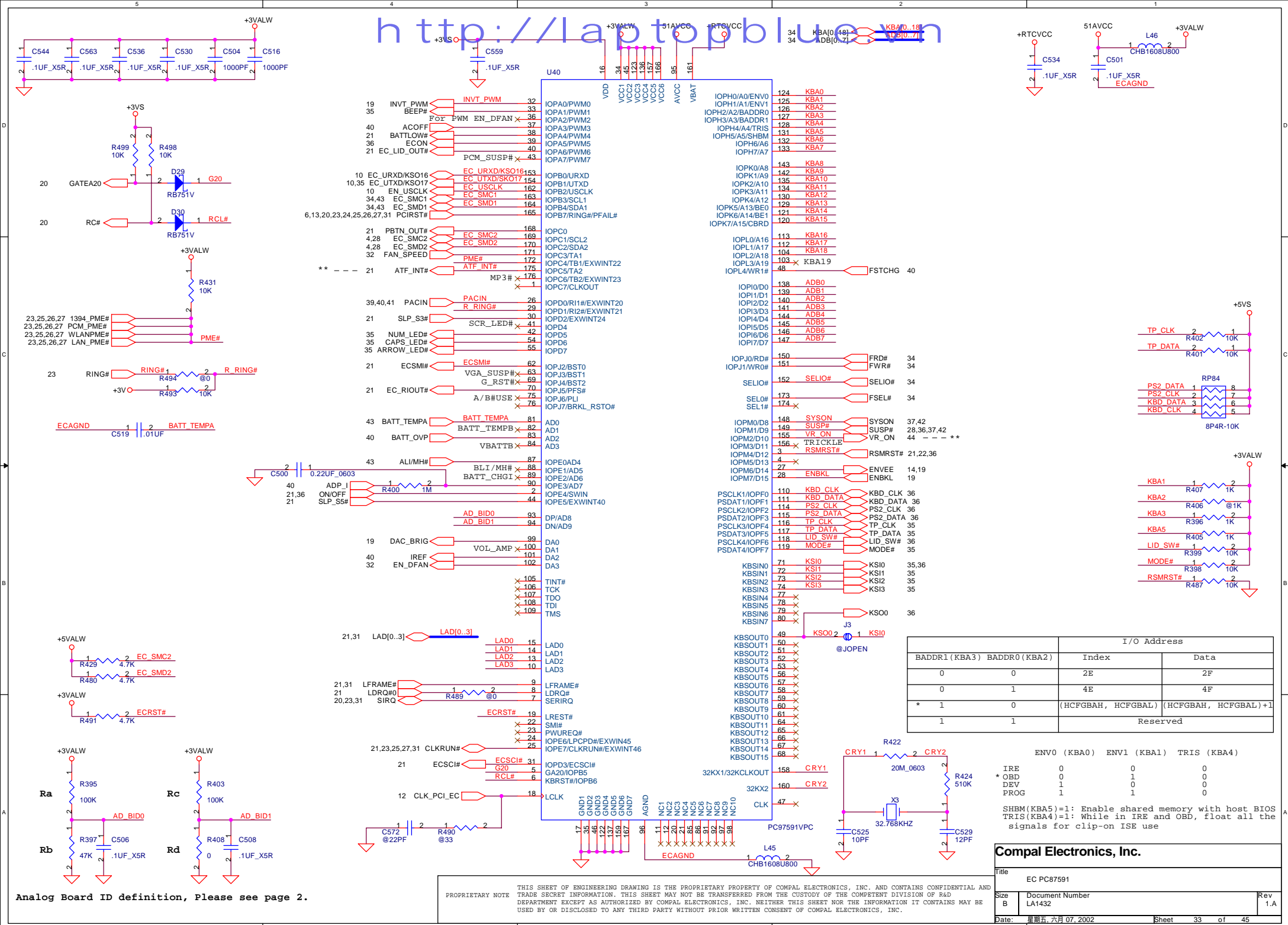
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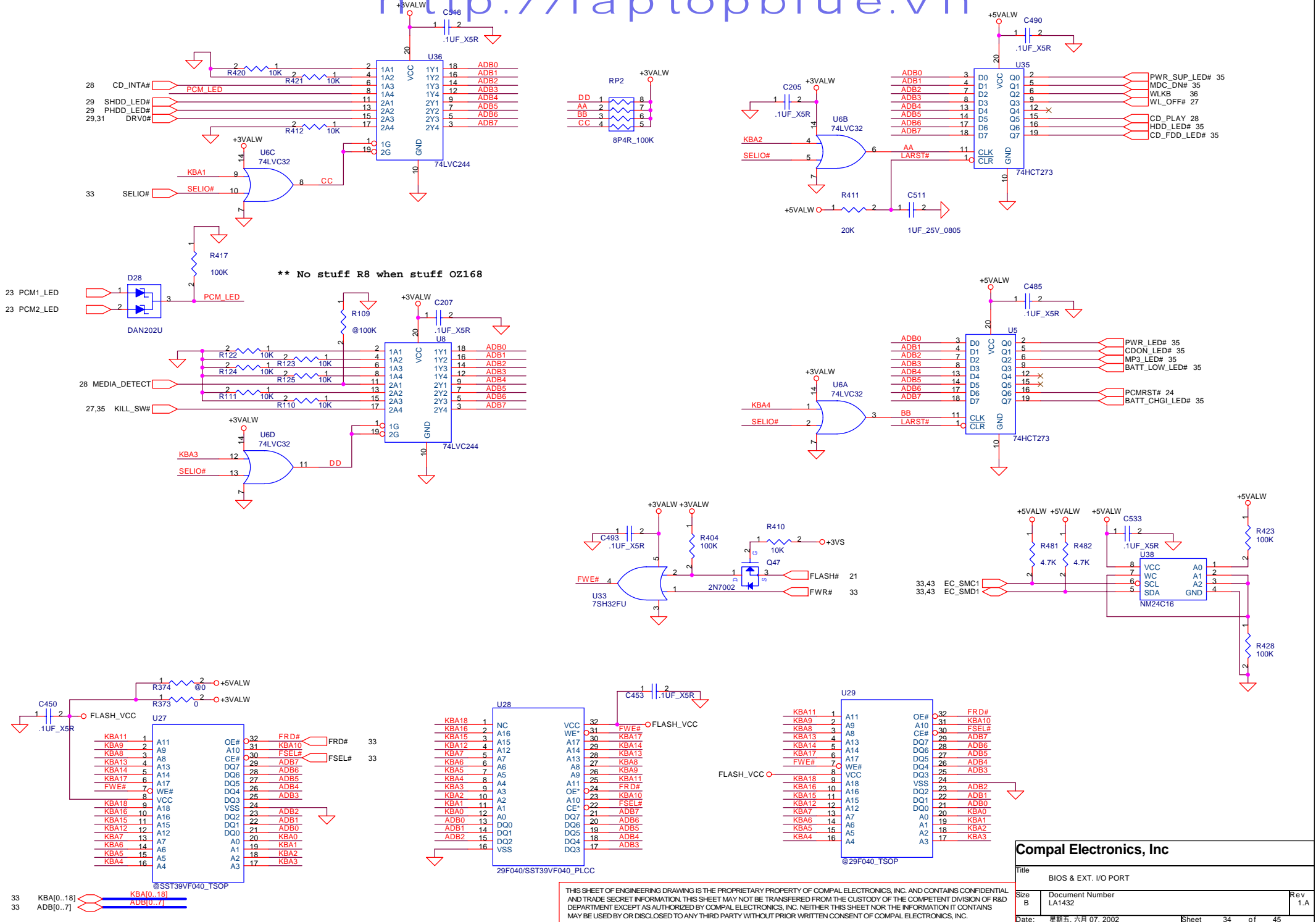
Analog Board ID definition, Please see page 2.

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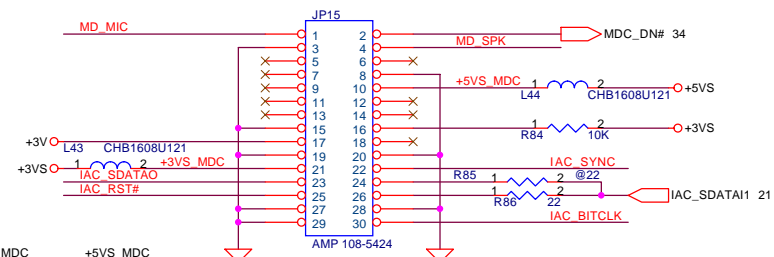
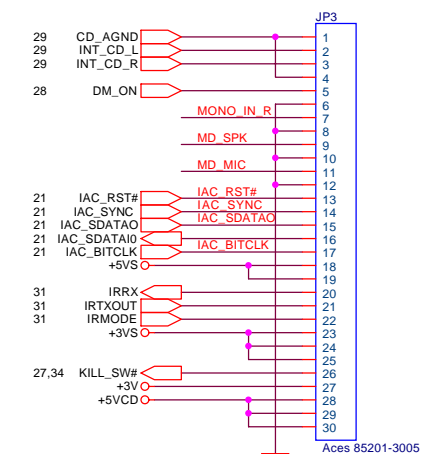
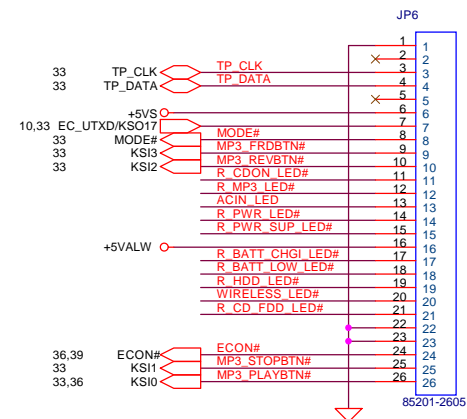
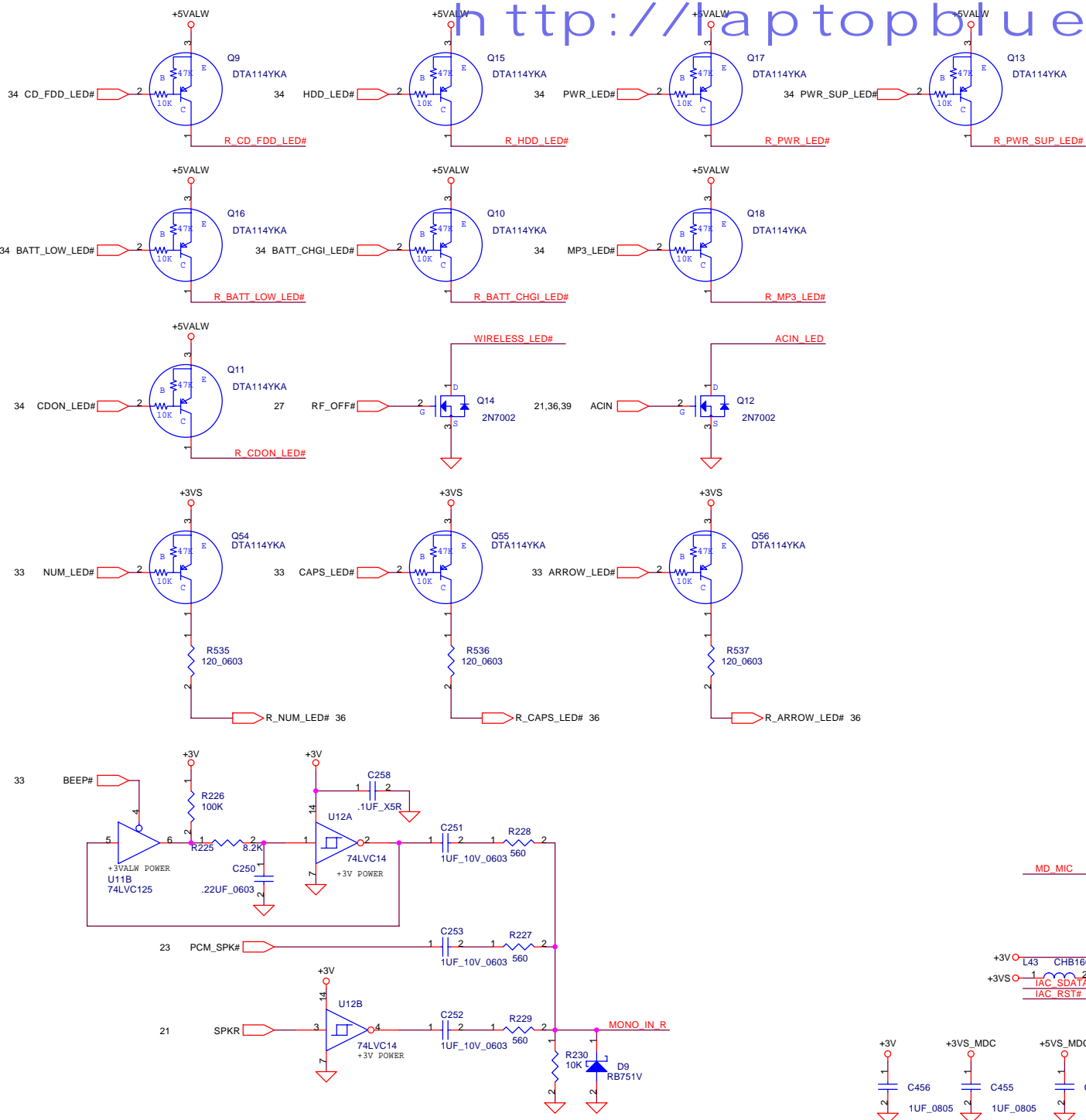
```
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TRIS(KBA4)=1: While in IRE and OBD, float all the
  signals for clip-on ISE use
```

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Title				EC PC87591			
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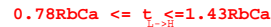
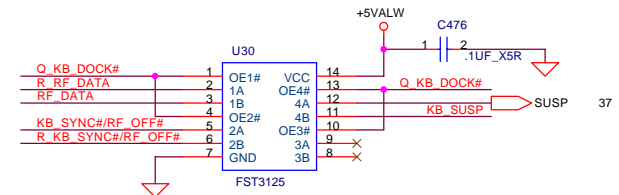
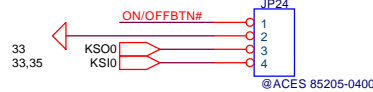
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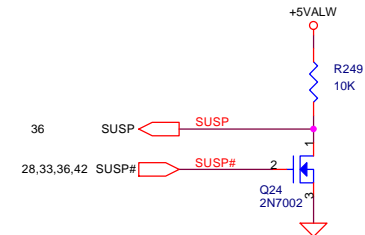
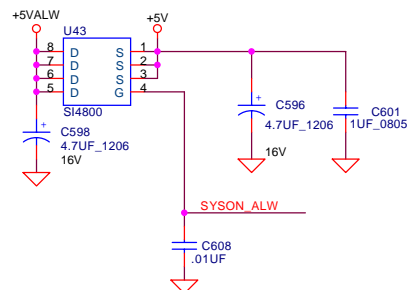
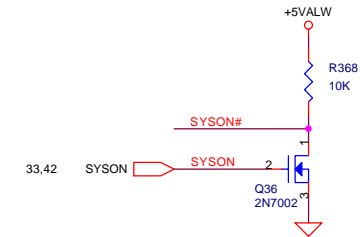
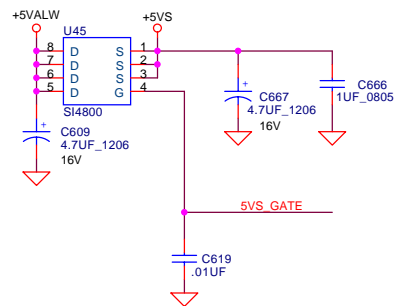
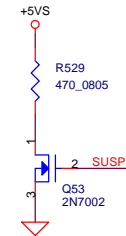
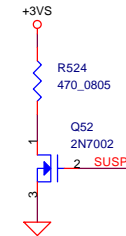
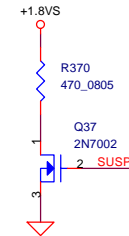
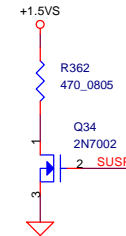
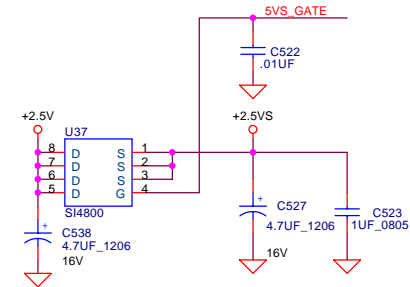
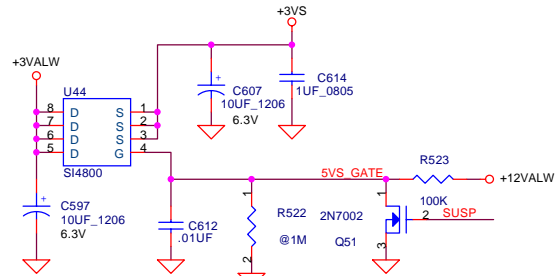
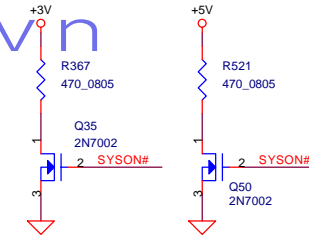
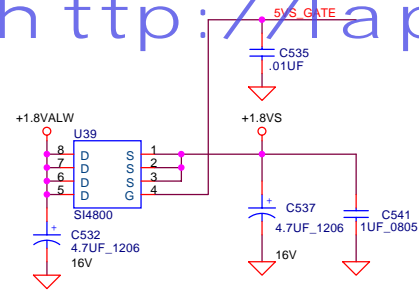
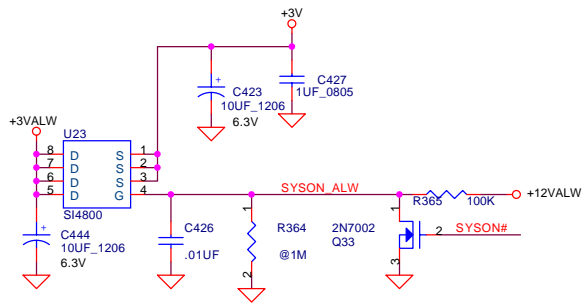
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Diagram illustrating a circuit connection for a laptop. The circuit shows a 5V GATE signal connected to the C535 pin, and a +3V signal connected to the P367 pin.



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Title	POWER CONTROL CKT
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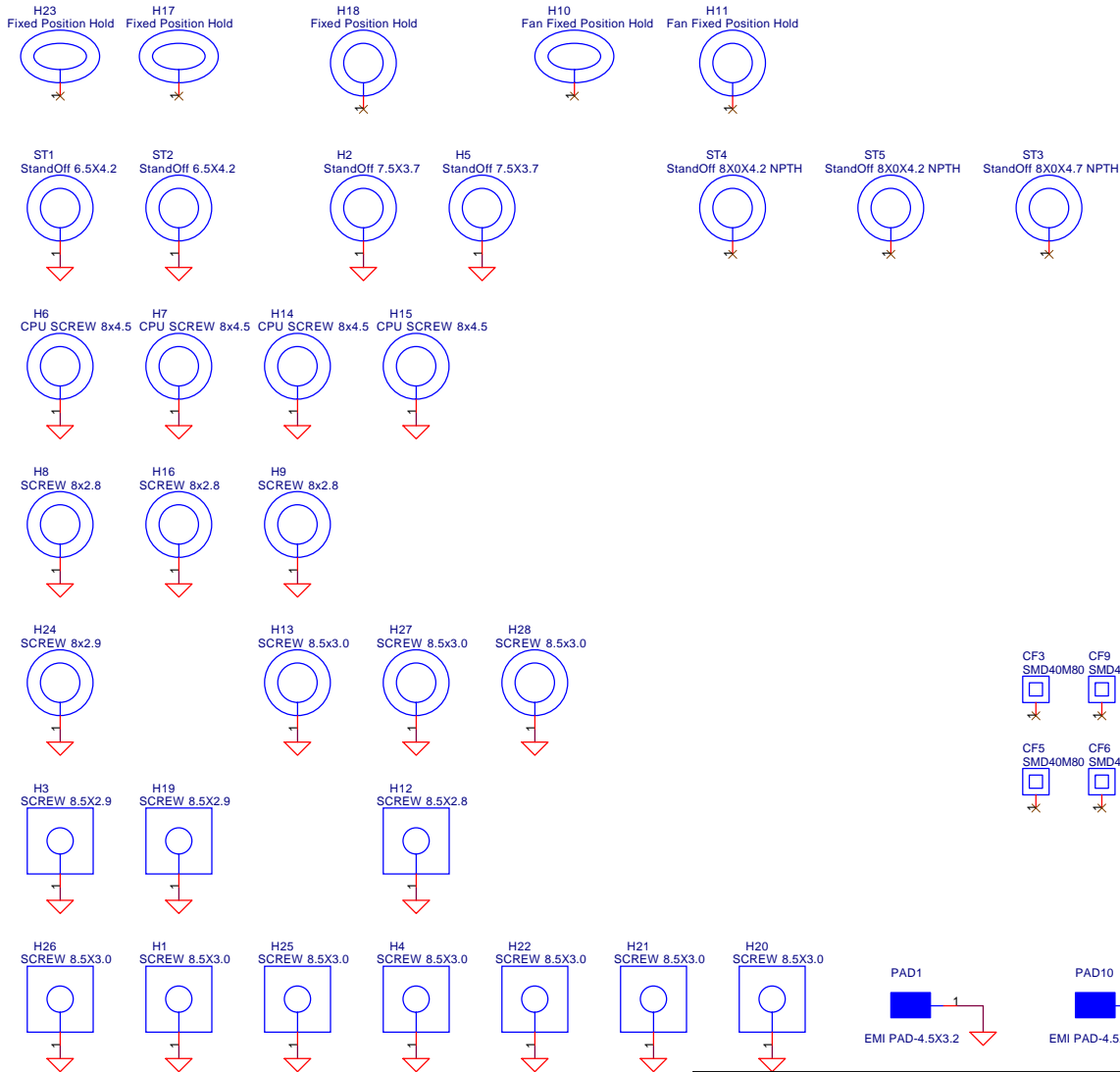
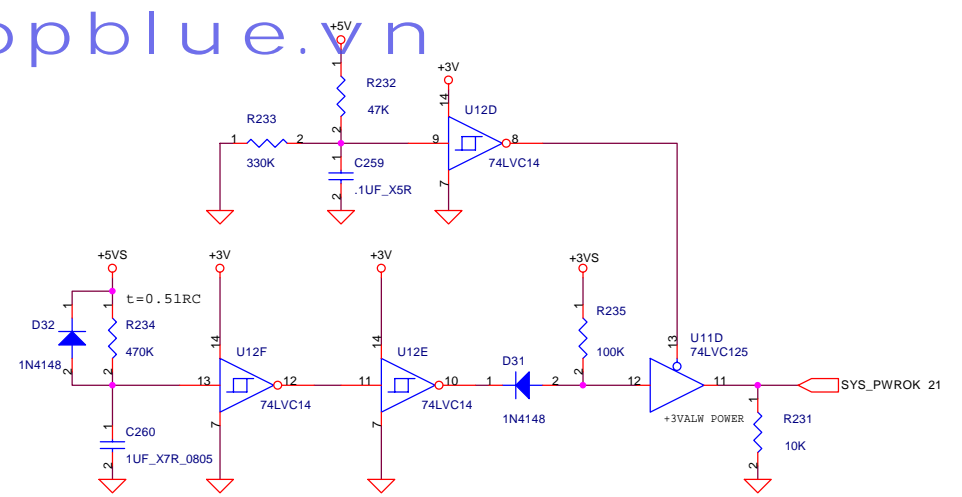
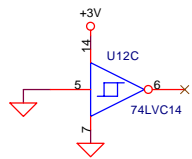
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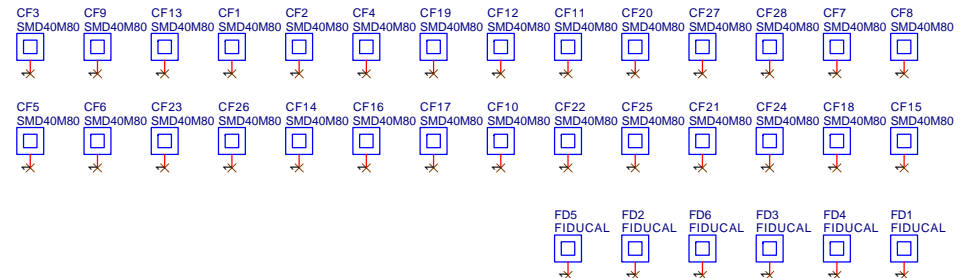
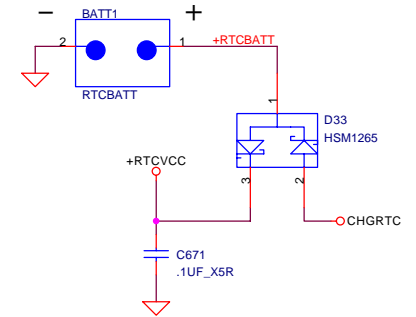
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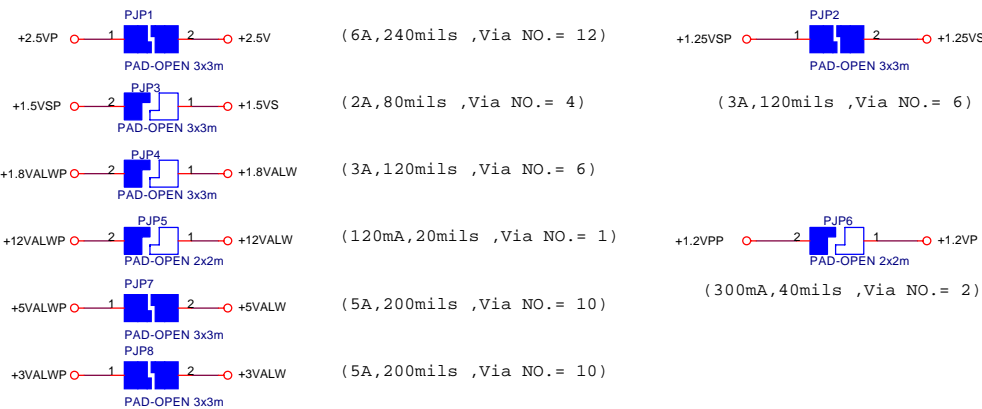
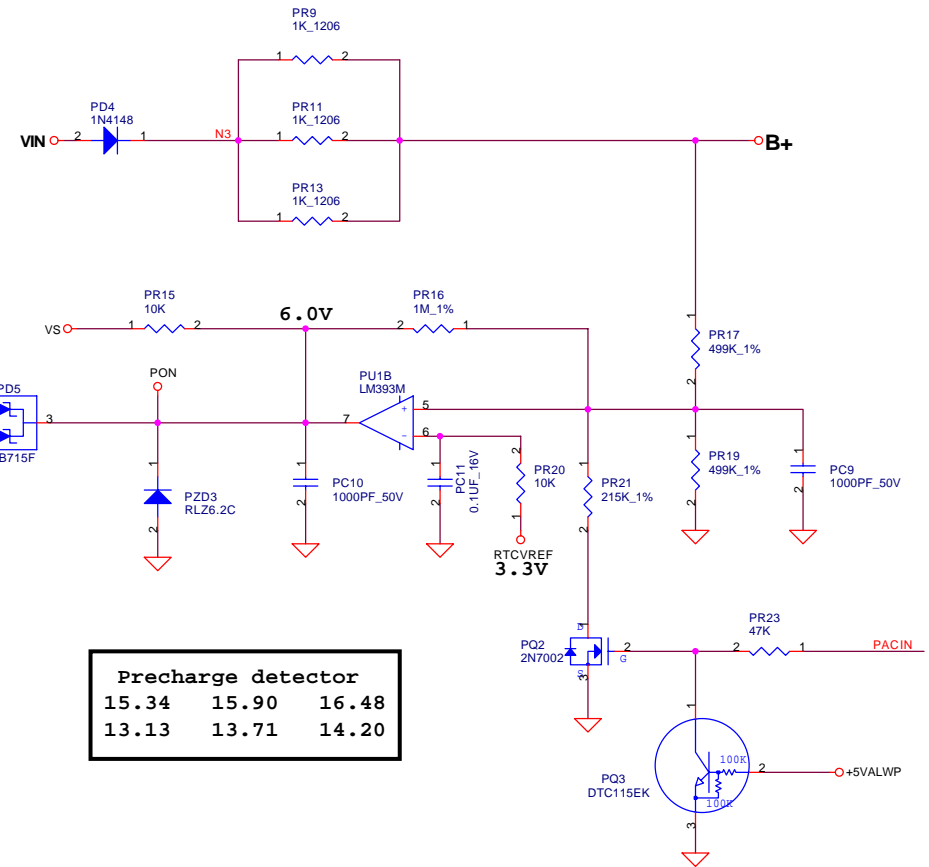
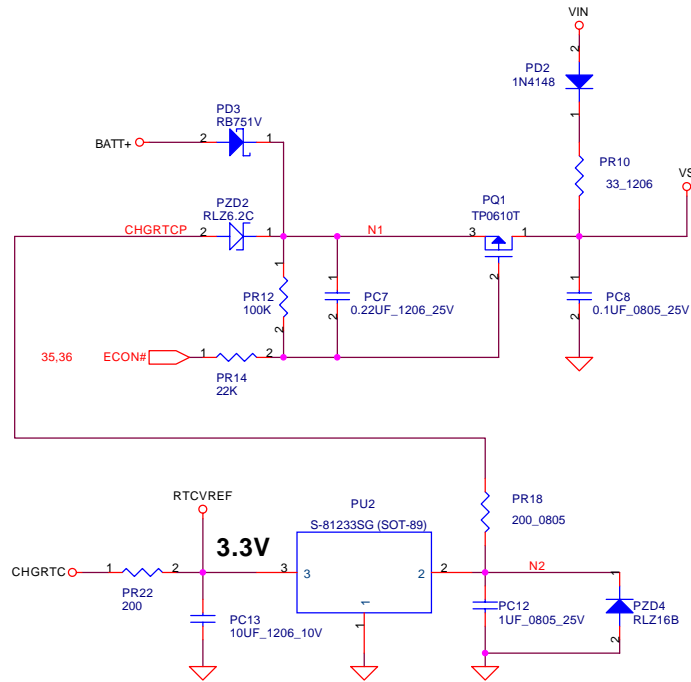
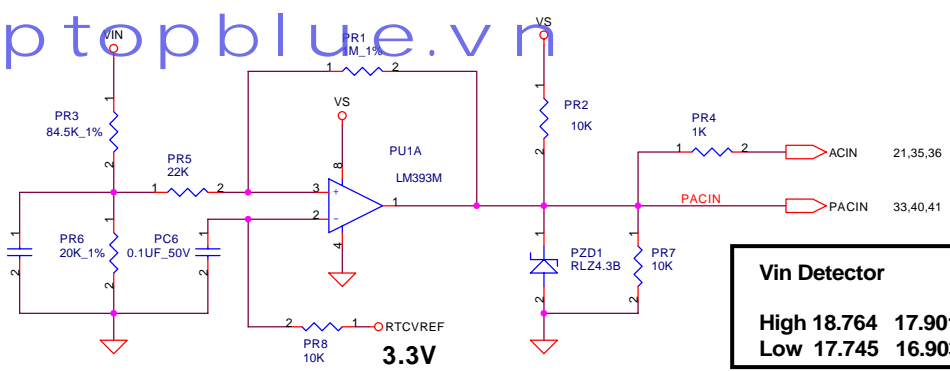
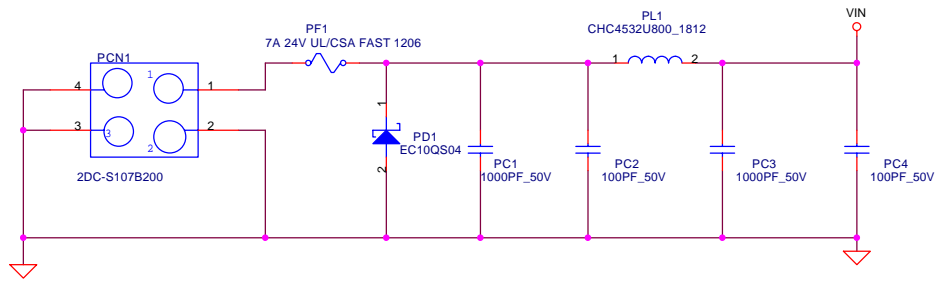
## RTC BATT



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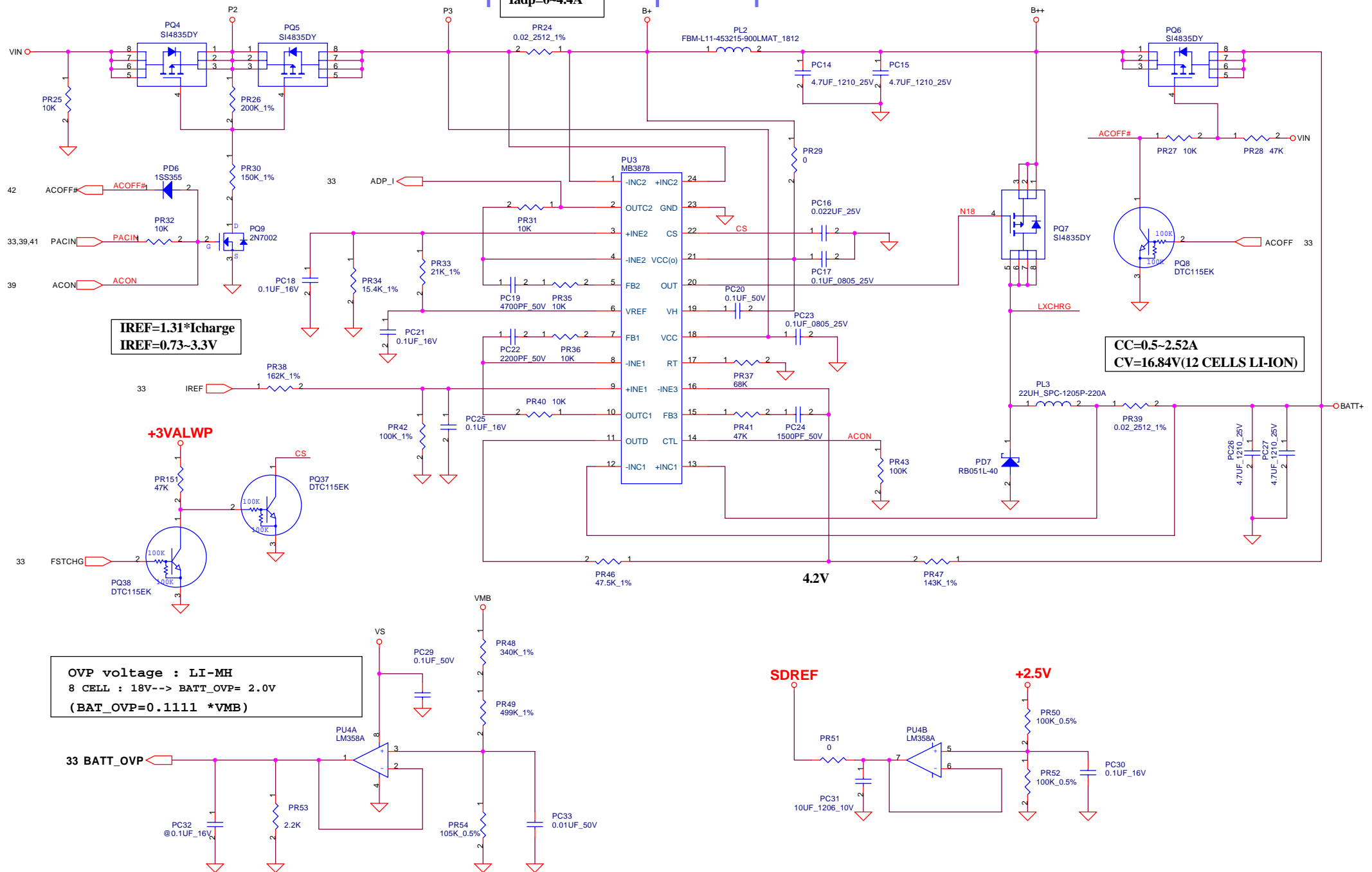


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DCIN & DETECTOR

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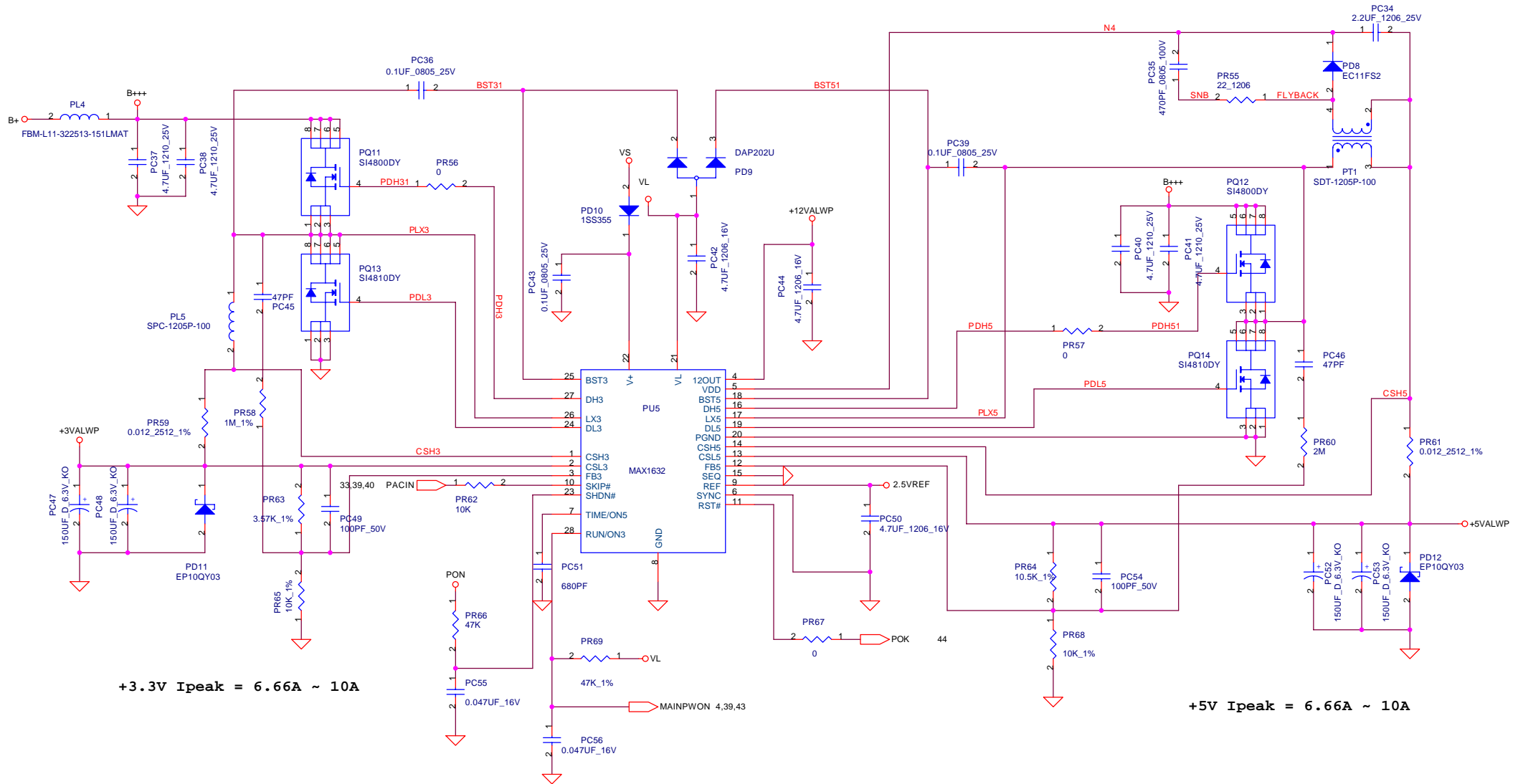


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Title		<b>CHARGER</b>	
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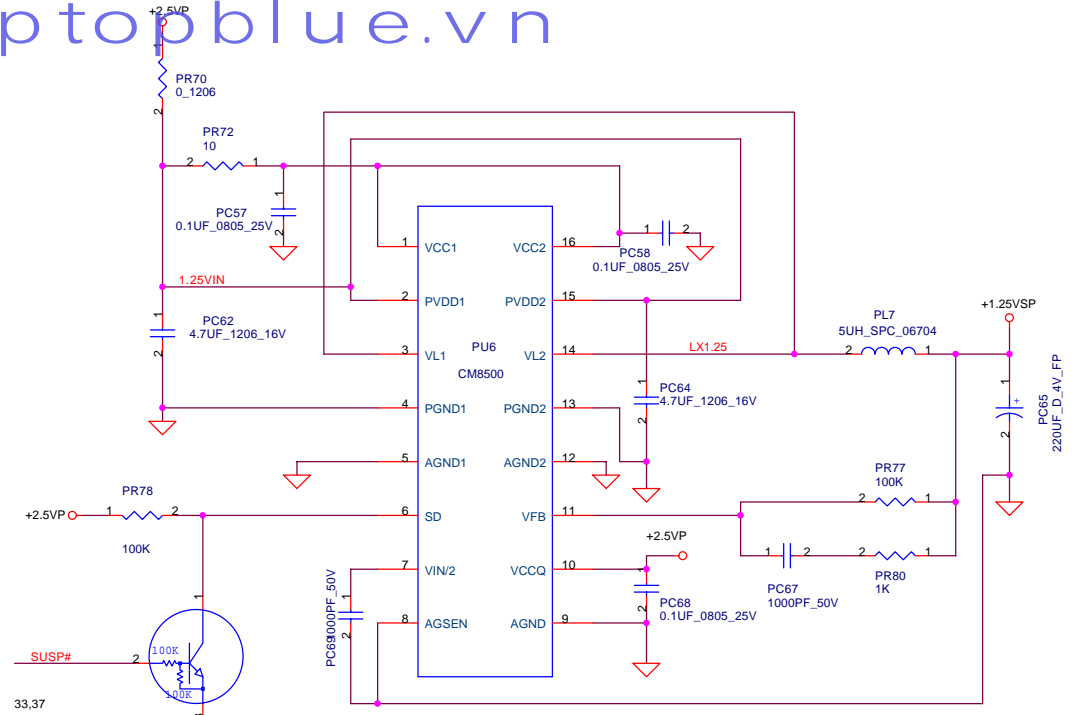
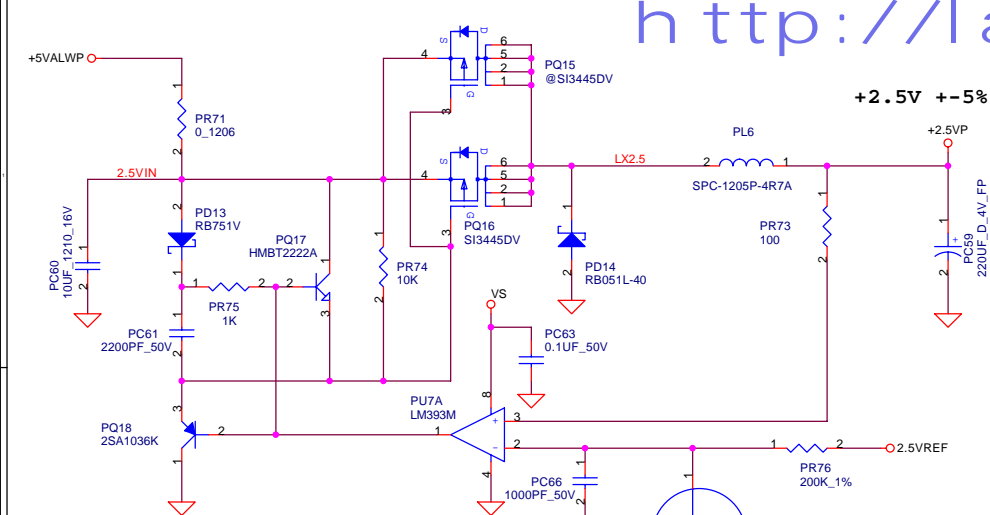




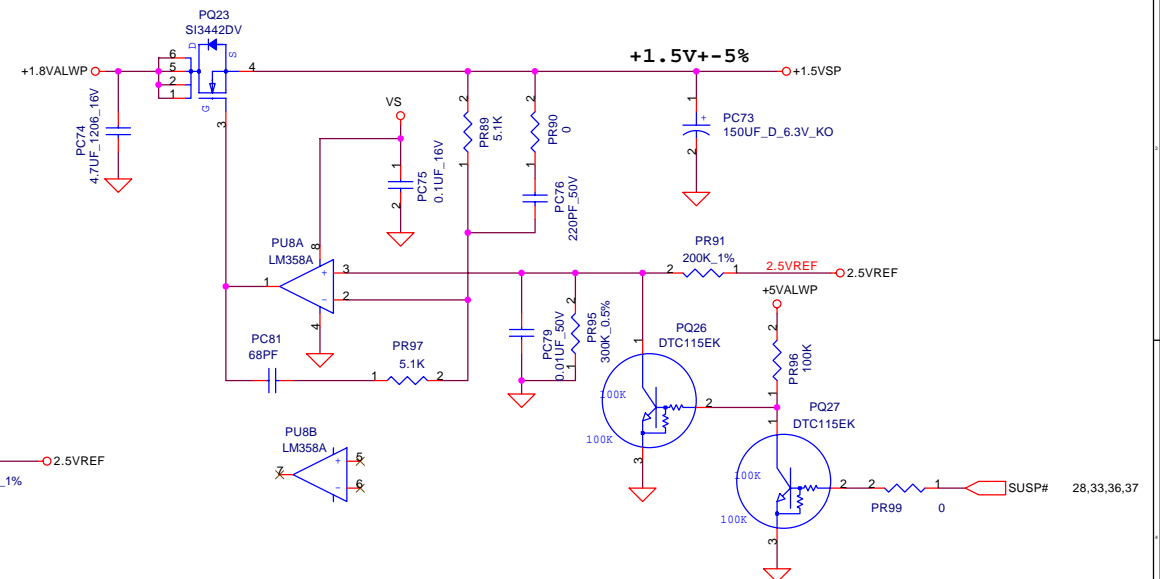
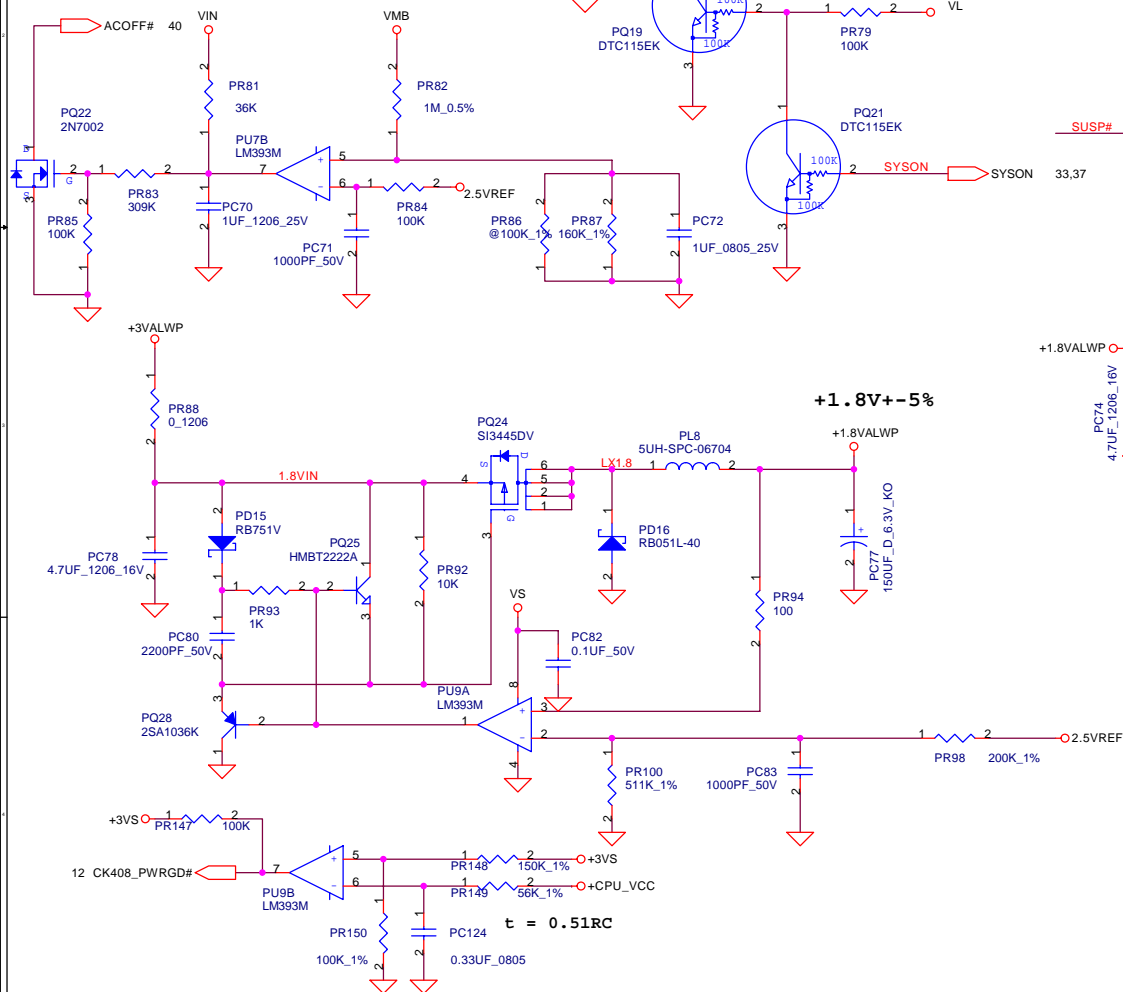
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Title		5V/3.3V/12V	
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Layout : "Compensation network close to FB pin"



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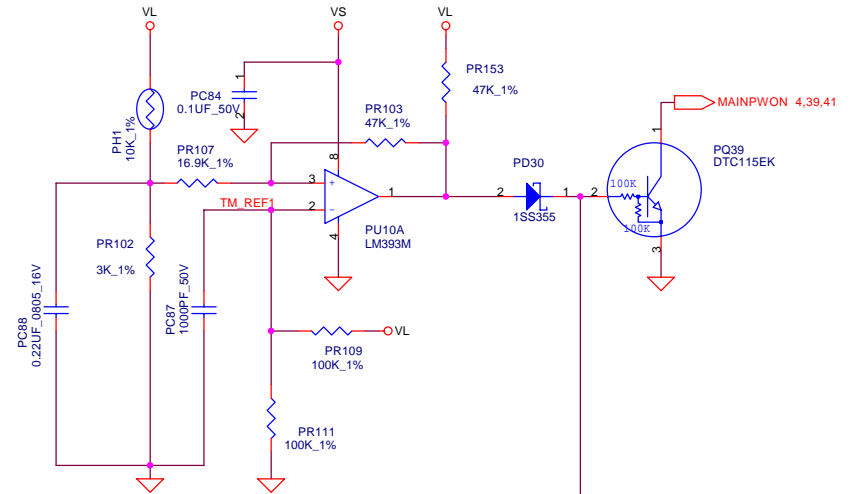
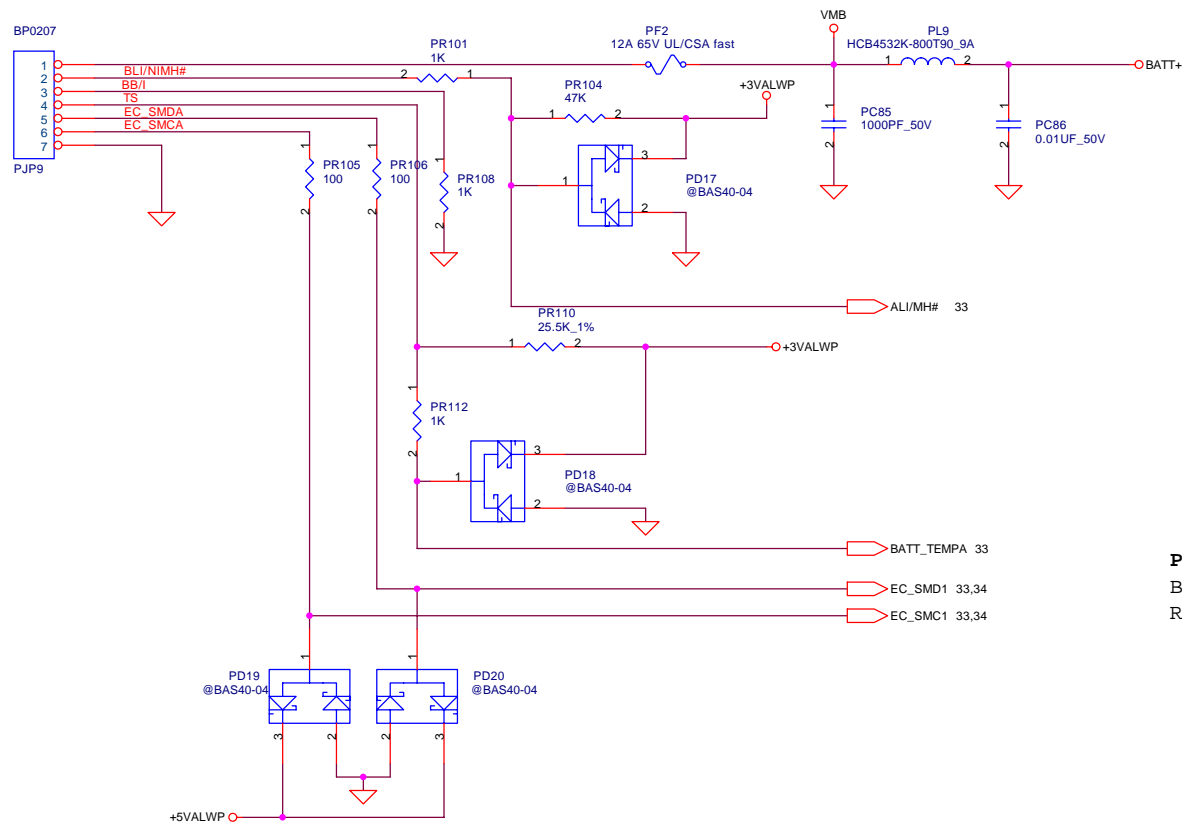
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DDR /2.5V / 1.8V/1.25V

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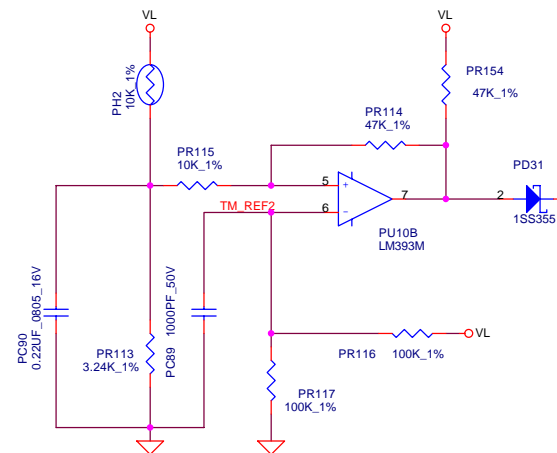
**PH1 under CPU botten side :**

CPU thermal protection at 87 degree C  
Recovery at 48 degree C



**PH2 near main Battery CONN :**

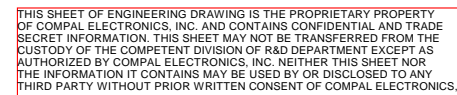
BAT. thermal protection at 73 degree C  
Recovery at 50(51) degree C



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BATTERY CONN / OTP		
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# ATR60 PIR LIST

# http://laptopblue.vn

\*\*\*\*\* Rev0.2 PIR List \*\*\*\*\*

04/15/02 Written by Jerry

P26:Delete C372 and Remove +3V at pin6 of U18  
P33: Remove @ at R492 and add @ at R488  
Change value of R397 to 47K

04/26/02 Written by Sam

P14: Remove @ at C134  
P17: Delete RP70, RP77, RP88, RP83, RP81, RP86, RP79, RP69, RP90, RP92  
RP67, RP76, RP87, RP82, RP80, RP85, RP78, RP68, RP89, RP91  
R386, R383  
Remove @ at R413, R414  
P18: Delete RP65, RP64, RP71, RP72, RP62, RP63, RP73, RP66, RP61, RP74  
RP52, RP49, RP57, RP58, RP48, RP47, RP59, RP56, RP50, RP60  
R325, R369  
Remove @ at R345, R382  
P33: Delete R425, R426, R427, R430, R488, R492  
Add U40 Signal Pins for Keyboard Led NUM\_LED# , CAPS\_LED#, ARROW\_LED#  
P35: Add R535, R536 ,R537 ,Q54, Q55, Q56  
P36: Add Q57  
Change D25 to Be PSOT24C, Pin 1 : Floating,Pin 2 : Connect to JP2 Pin 8,  
Pin 3 : Ground  
Change R376 Pin 2 Connect with RTCVREF,Change R390 Pin 2 Connect with RTCVREF,

04/26/02 Written by Jerry

P17,P18: Modify net name R\_NDQM\* TO NDQM\*

05/01/02 Written by Sam

P29: Add @ at R538  
P34: Add U35 Pin 6 Signl for WLKB  
P36: Add R539,R540,D35,Q58  
Del D10  
Change R250 Pin 1 from +12VALW to +5VALW\_RX

05/06/02 Written by Sam  
P35: Q12, Q14 Change Material to 2N7002

05/07/02 Written by Sam  
P15: L37 Change Material to 0\_0603

05/17/02 Written by Sam  
P36: Change J3 footprint to JUMP\_2MM  
P36: Add JP24 and Change J1,J4 footprint to JUMP\_2MM

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