



Compal Confidential

HTW20 LA-3171P Schematics Document

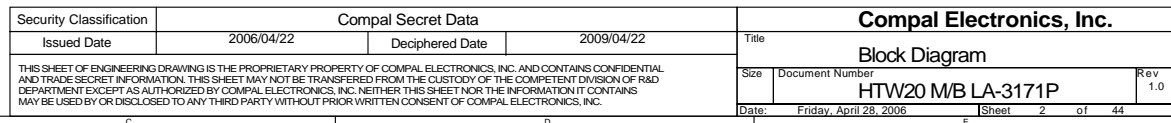
Intel Yonah/Merom with 945PM/GM + DDRII + ICH7M
(+VGA/B ATi M52P/M54P/56P)

2006-04-26

REV: 1.0

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/04/22	Deciphered Date	2009/04/22	Title	
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NAPA Platform



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+VCCP	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	+VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	PCI Device ID	IDSEL #	REQ/GNT #	PIRQ
1394	D0	AD16	0	E
CARD BUS	D4	AD20	2	A,B
5IN1	D4	AD20	2	A,B

KB910 I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
SM1 24C16	A0H	1 0 1 0 0 0 0 X b
SM1 SMART BATTERY	16H	0 0 0 1 0 1 1 X b
SM2 ADM0132	98H	1 0 0 1 1 0 0 X b
CPU THERMAL MONITOR		

ICH7-M SM Bus address

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

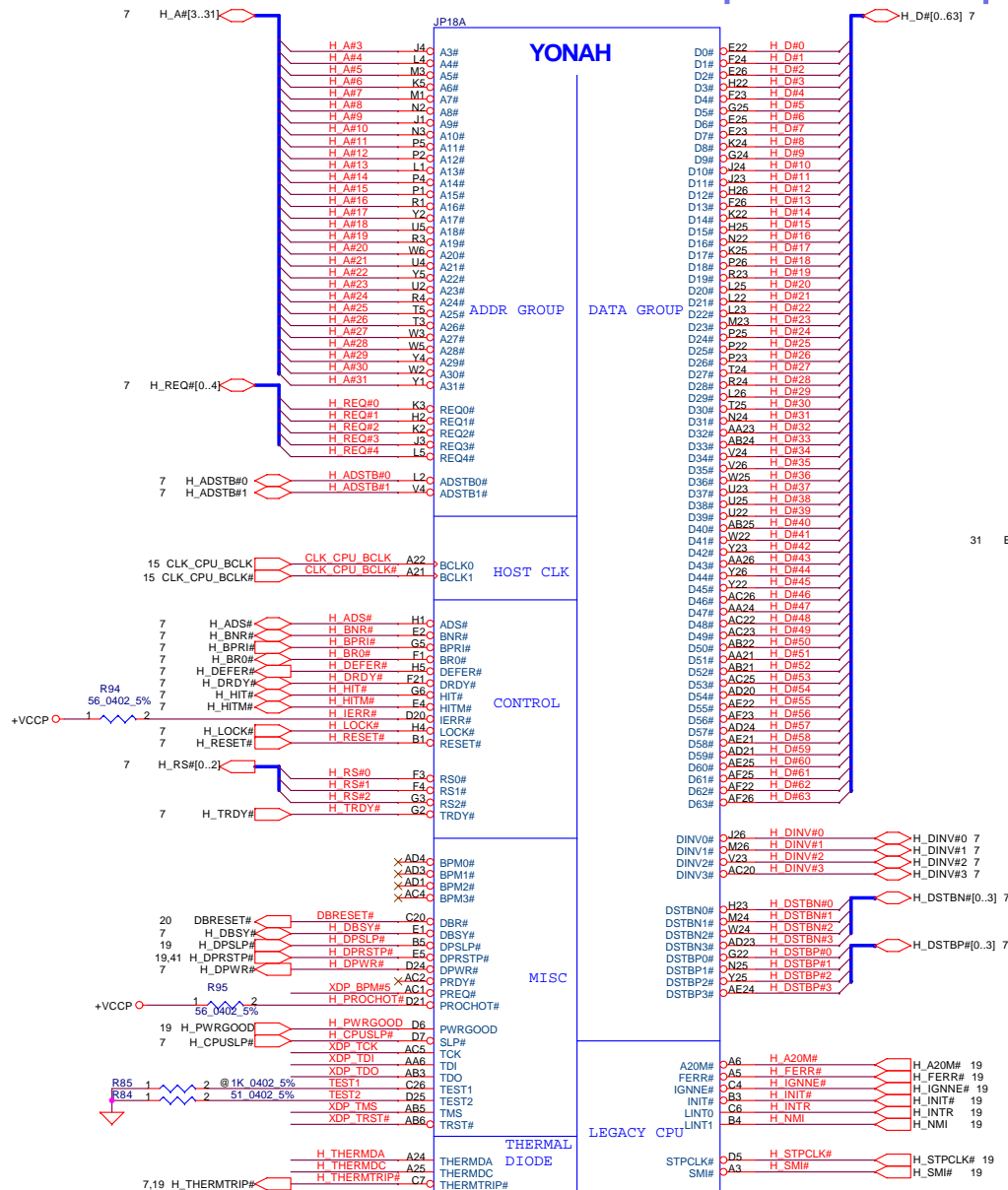
Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	
4	
5	
6	
7	

SKU ID Table

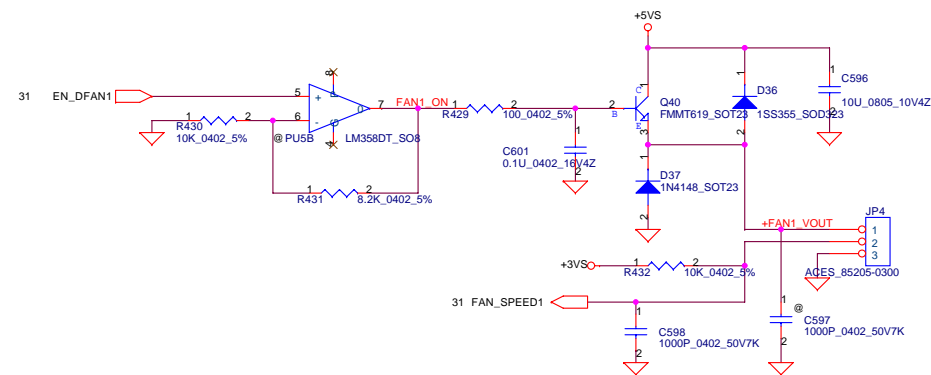
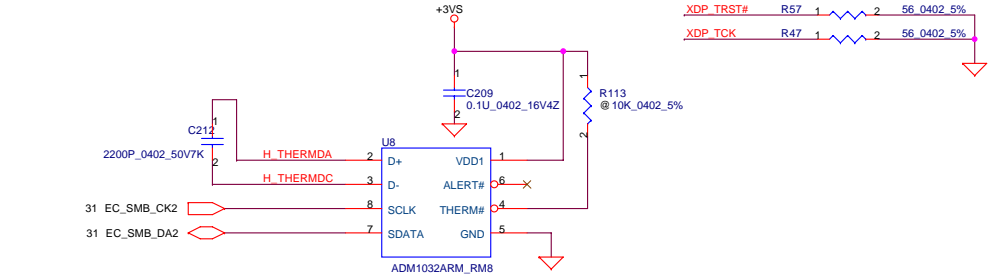
SKU ID	SKU
0	
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

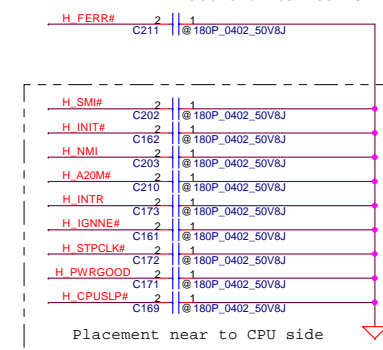
BTO Item	BOM Structure
VGA	GM@ PM@
New Card	NEWCARD@
Giga LAN	100M@ 1000M@
KILL SW	WLAN@
BlueTooth	BT@
5IN1	5IN1@



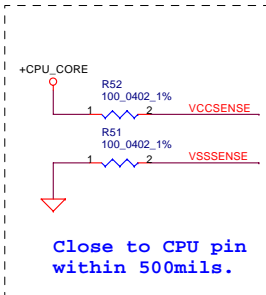
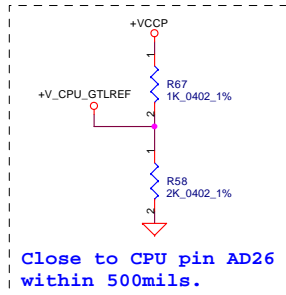
Thermal Sensor ADM1032ARM



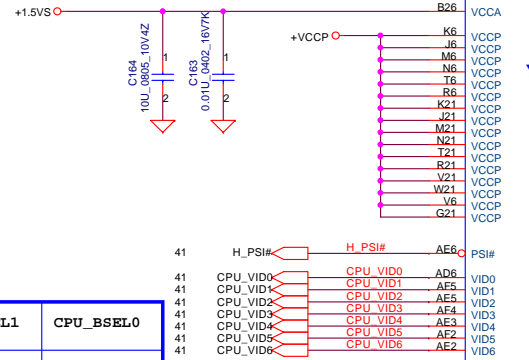
Close to Fan Conn.
Placement near to ICH7



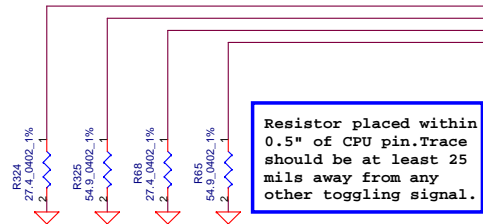
Security Classification		Compal Secret Data		Title	
Issued Date	2006/04/22	Deciphered Date	2009/04/22	Yonah CPU in mFCPGA479	
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Length match within 25 mils
The trace width 18 mils space
7 mils



CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1



YONAH

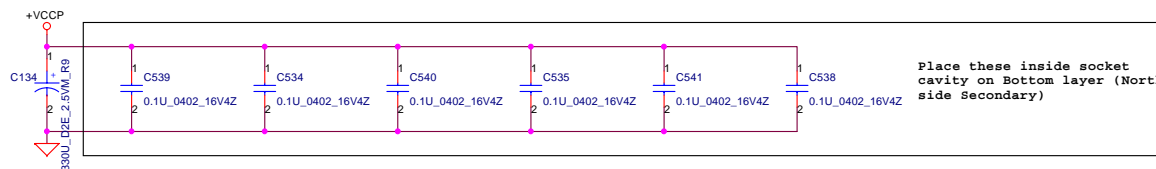
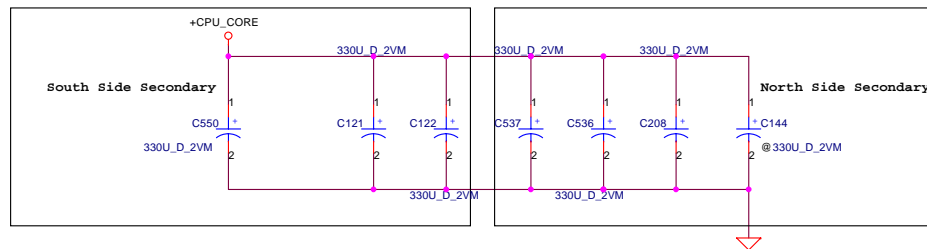
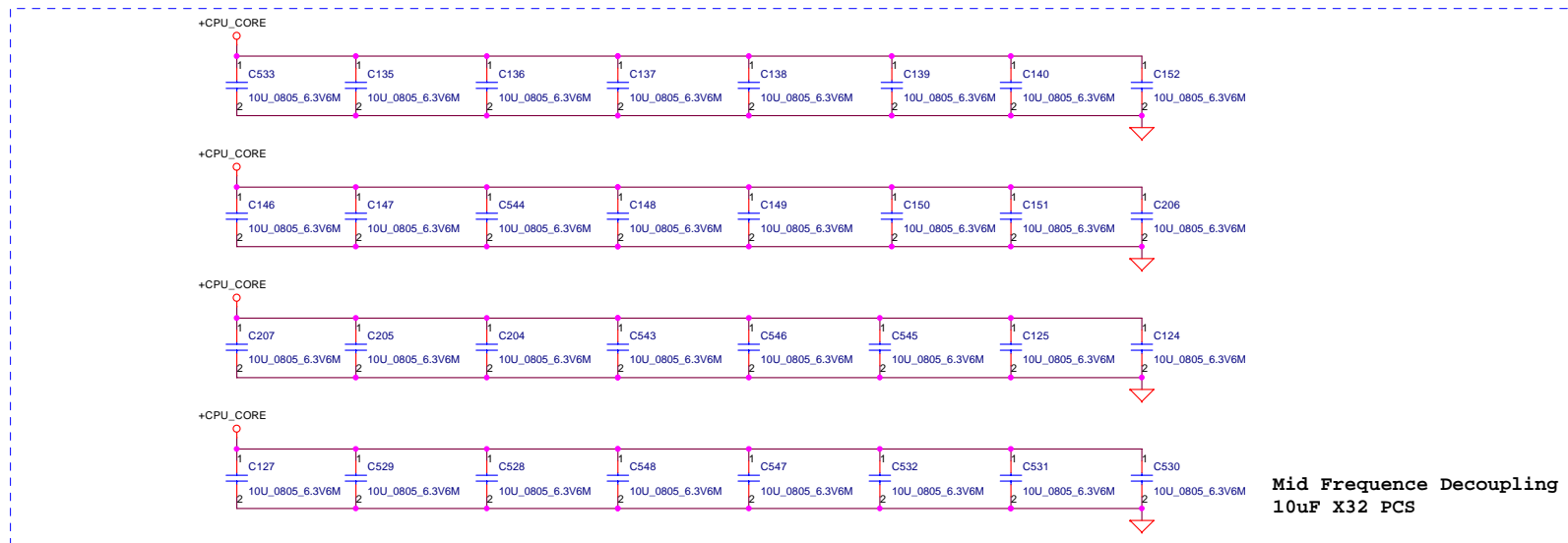
POWER, GROUND, RESERVED SIGNALS AND NC

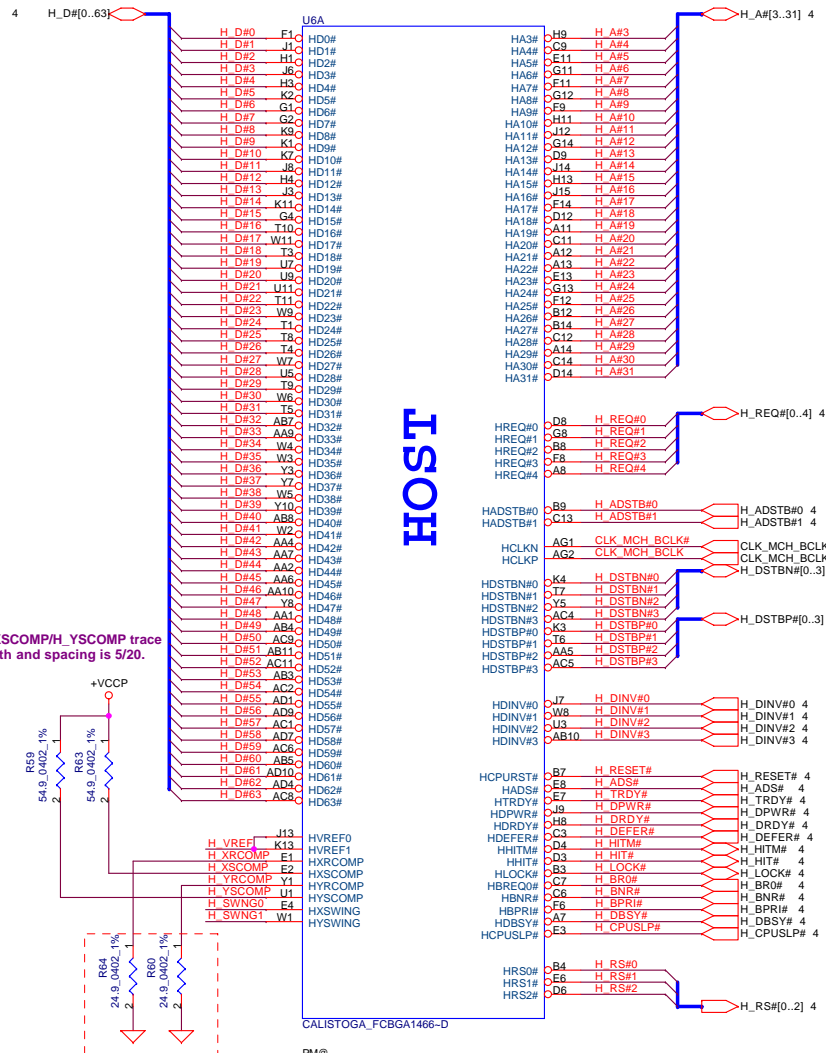
YONAH

POWER, GROUND

FOX_P247903-2741-42_YONAH

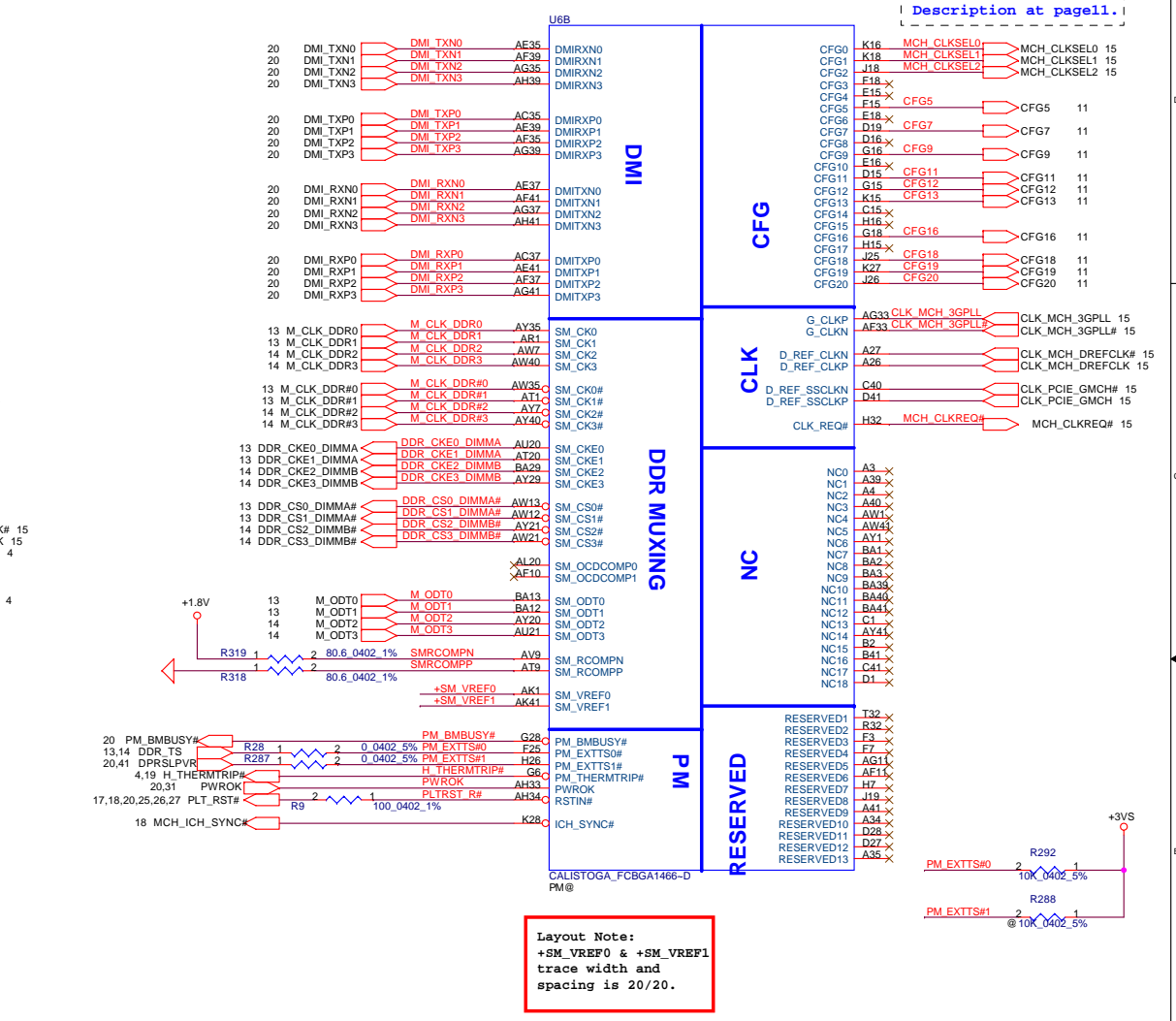
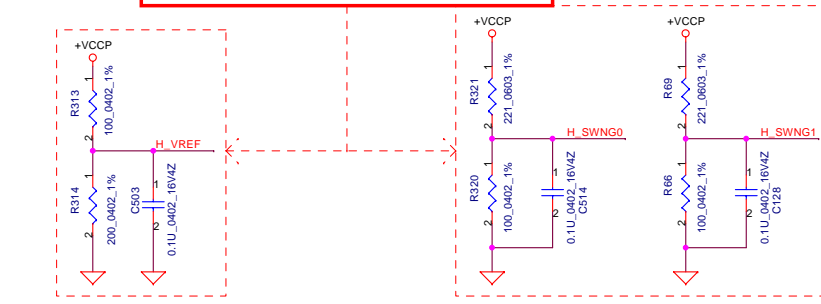
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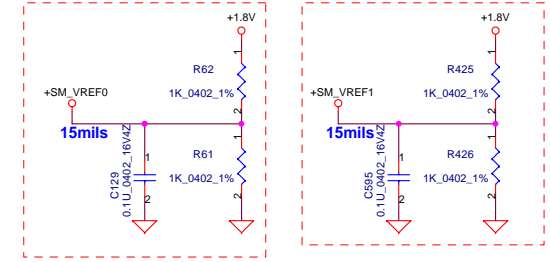


H_XSCOMP/H_YSCOMP trace width and spacing is 5/20.

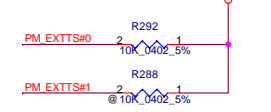
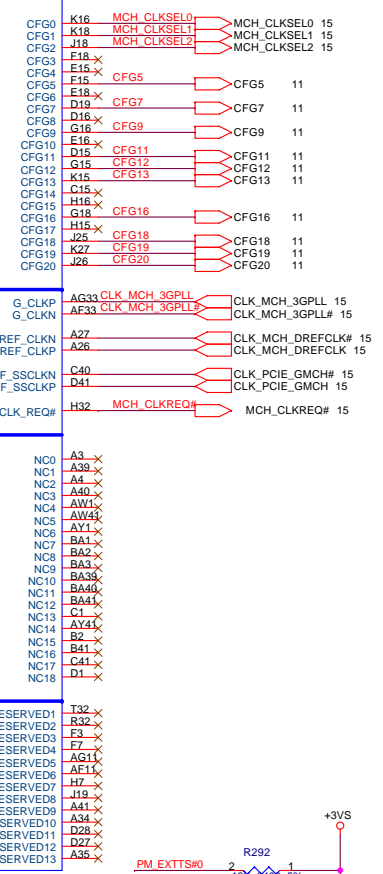
Layout Note:
H_XRCOMP / H_YRCOMP / H_VREF / H_SWNG0 / H_SWNG1 trace width and spacing is 18/20.

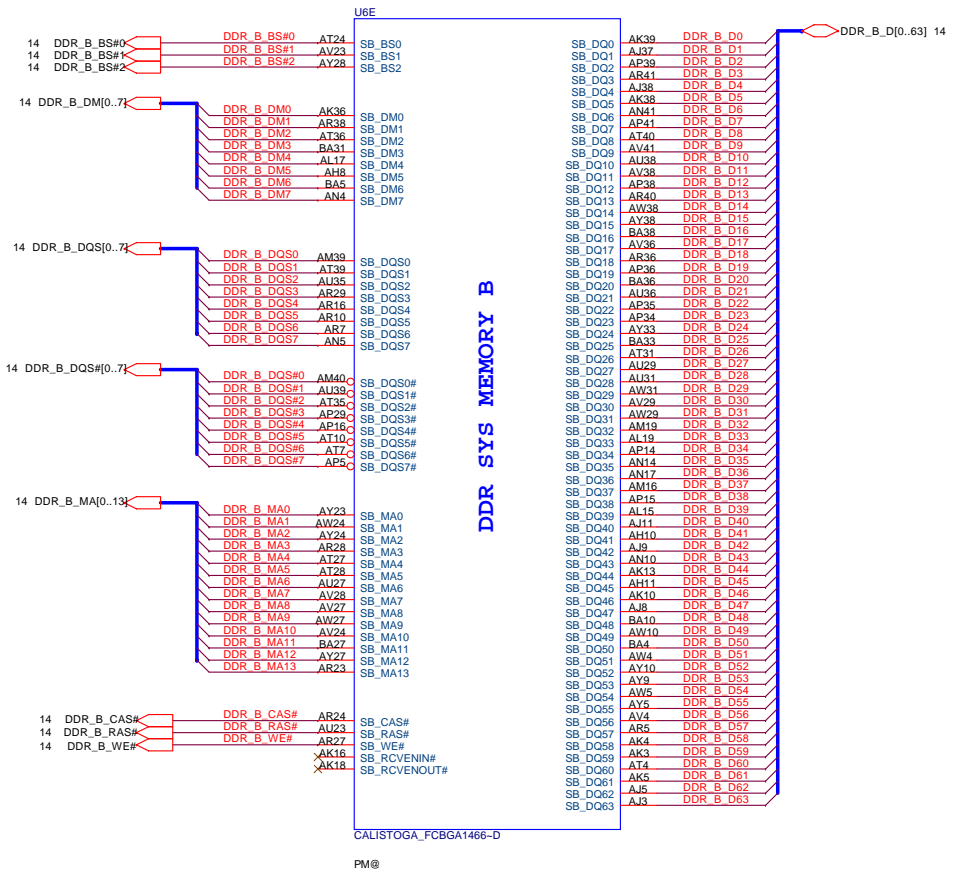
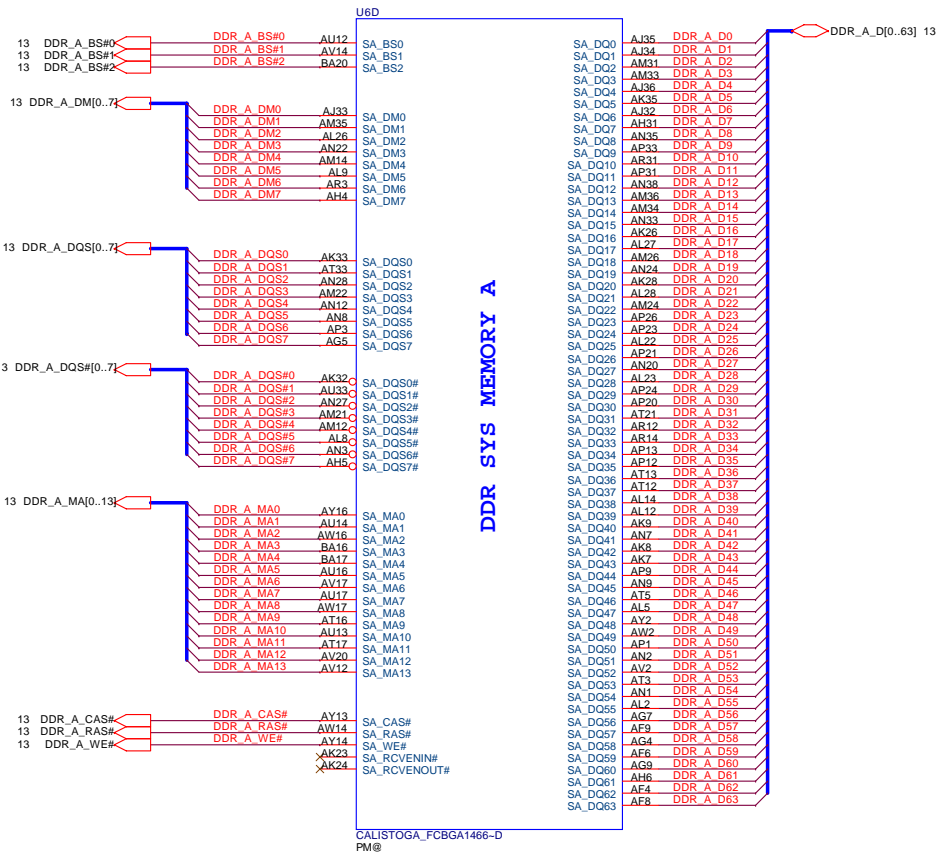


Layout Note:
+SM_VREF0 & +SM_VREF1 trace width and spacing is 20/20.

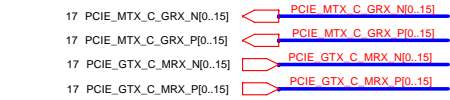
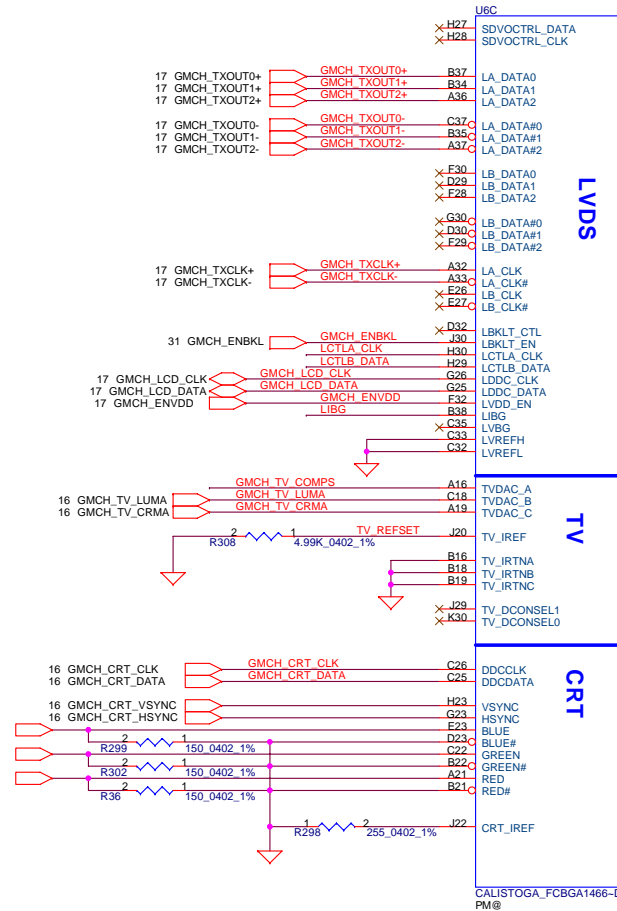
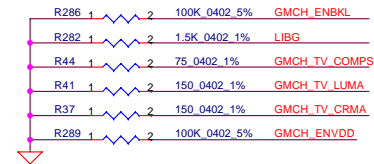
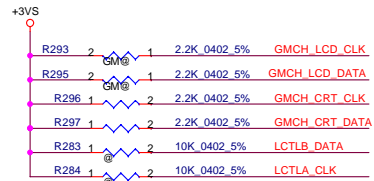


Description at page1.





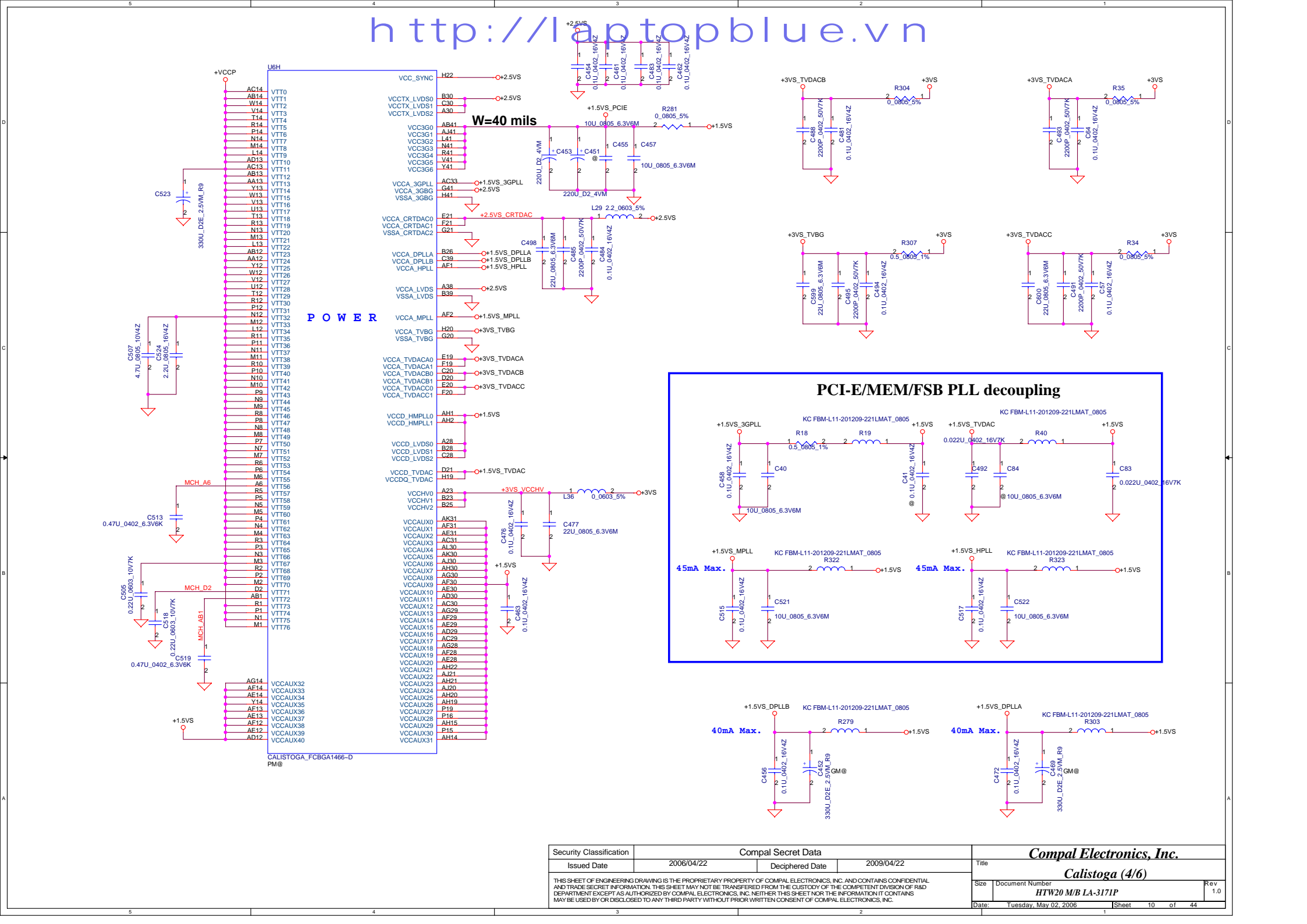
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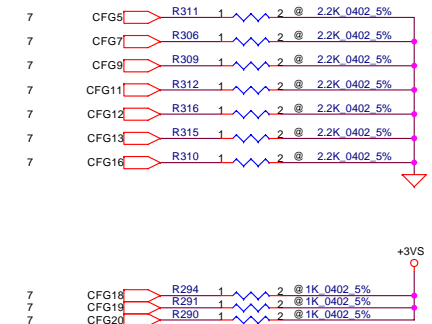
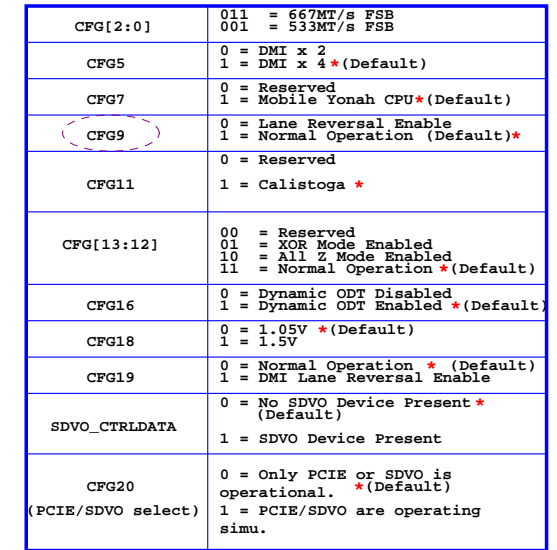


PEGCOMP trace width and spacing is 18/25 mils.

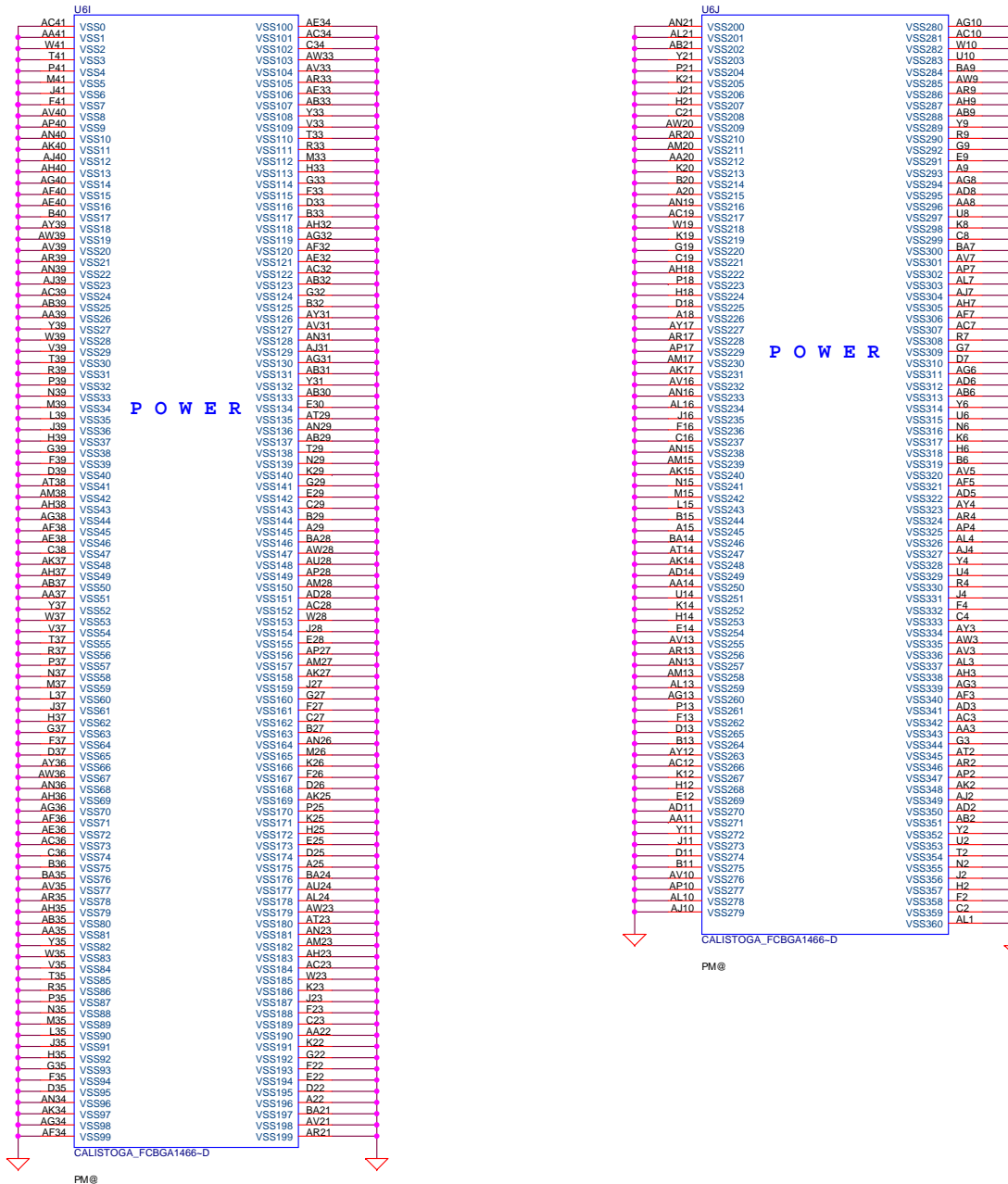


EXP_RXN0	F34	PCIE GTX C MRX N0			
EXP_RXN1	G38	PCIE GTX C MRX N1			
EXP_RXN2	H34	PCIE GTX C MRX N2			
EXP_RXN3	J38	PCIE GTX C MRX N3			
EXP_RXN4	L34	PCIE GTX C MRX N4			
EXP_RXN5	M38	PCIE GTX C MRX N5			
EXP_RXN6	N34	PCIE GTX C MRX N6			
EXP_RXN7	P38	PCIE GTX C MRX N7			
EXP_RXN8	R34	PCIE GTX C MRX N8			
EXP_RXN9	T38	PCIE GTX C MRX N9			
EXP_RXN10	V34	PCIE GTX C MRX N10			
EXP_RXN11	W38	PCIE GTX C MRX N11			
EXP_RXN12	Y34	PCIE GTX C MRX N12			
EXP_RXN13	AA38	PCIE GTX C MRX N13			
EXP_RXN14	AB34	PCIE GTX C MRX N14			
EXP_RXN15	AC38	PCIE GTX C MRX N15			
EXP_RXP0	D34	PCIE GTX C MRX P0			
EXP_RXP1	F38	PCIE GTX C MRX P1			
EXP_RXP2	G34	PCIE GTX C MRX P2			
EXP_RXP3	H38	PCIE GTX C MRX P3			
EXP_RXP4	J34	PCIE GTX C MRX P4			
EXP_RXP5	L38	PCIE GTX C MRX P5			
EXP_RXP6	M34	PCIE GTX C MRX P6			
EXP_RXP7	N38	PCIE GTX C MRX P7			
EXP_RXP8	P34	PCIE GTX C MRX P8			
EXP_RXP9	R38	PCIE GTX C MRX P9			
EXP_RXP10	T34	PCIE GTX C MRX P10			
EXP_RXP11	V38	PCIE GTX C MRX P11			
EXP_RXP12	W34	PCIE GTX C MRX P12			
EXP_RXP13	Y38	PCIE GTX C MRX P13			
EXP_RXP14	AA34	PCIE GTX C MRX P14			
EXP_RXP15	AB38	PCIE GTX C MRX P15			
EXP_TXN0	F36	PCIE MTX GRX N0	C449	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N0
EXP_TXN1	G40	PCIE MTX GRX N1	C433	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N1
EXP_TXN2	H36	PCIE MTX GRX N2	C447	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N2
EXP_TXN3	J40	PCIE MTX GRX N3	C431	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N3
EXP_TXN4	L36	PCIE MTX GRX N4	C445	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N4
EXP_TXN5	M40	PCIE MTX GRX N5	C429	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N5
EXP_TXN6	N36	PCIE MTX GRX N6	C443	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N6
EXP_TXN7	P40	PCIE MTX GRX N7	C427	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N7
EXP_TXN8	R36	PCIE MTX GRX N8	C441	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N8
EXP_TXN9	T40	PCIE MTX GRX N9	C425	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N9
EXP_TXN10	V36	PCIE MTX GRX N10	C439	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N10
EXP_TXN11	W40	PCIE MTX GRX N11	C423	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N11
EXP_TXN12	Y36	PCIE MTX GRX N12	C437	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N12
EXP_TXN13	AA40	PCIE MTX GRX N13	C421	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N13
EXP_TXN14	AB36	PCIE MTX GRX N14	C435	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N14
EXP_TXN15	AC40	PCIE MTX GRX N15	C419	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX N15
EXP_TXP0	D36	PCIE MTX GRX P0	C450	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P0
EXP_TXP1	F40	PCIE MTX GRX P1	C434	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P1
EXP_TXP2	G36	PCIE MTX GRX P2	C448	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P2
EXP_TXP3	H40	PCIE MTX GRX P3	C432	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P3
EXP_TXP4	J36	PCIE MTX GRX P4	C446	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P4
EXP_TXP5	L40	PCIE MTX GRX P5	C430	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P5
EXP_TXP6	M36	PCIE MTX GRX P6	C444	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P6
EXP_TXP7	N40	PCIE MTX GRX P7	C428	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P7
EXP_TXP8	P36	PCIE MTX GRX P8	C442	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P8
EXP_TXP9	R40	PCIE MTX GRX P9	C426	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P9
EXP_TXP10	T36	PCIE MTX GRX P10	C440	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P10
EXP_TXP11	V40	PCIE MTX GRX P11	C424	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P11
EXP_TXP12	W36	PCIE MTX GRX P12	C438	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P12
EXP_TXP13	Y40	PCIE MTX GRX P13	C422	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P13
EXP_TXP14	AA36	PCIE MTX GRX P14	C436	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P14
EXP_TXP15	AB40	PCIE MTX GRX P15	C420	PM@ 0.1U 0402 16V7K	PCIE MTX C GRX P15

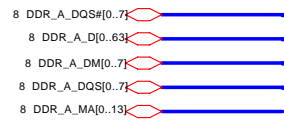
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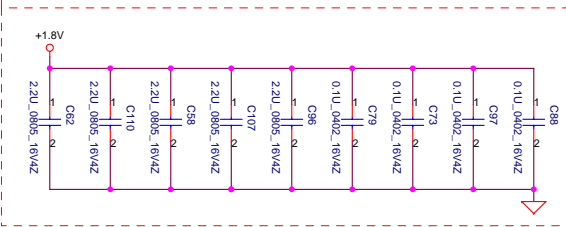
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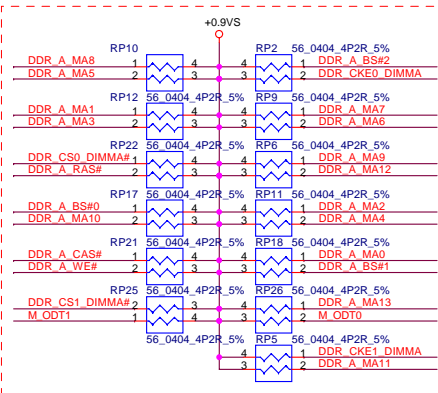
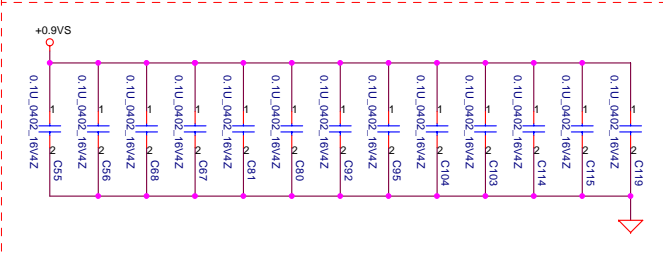
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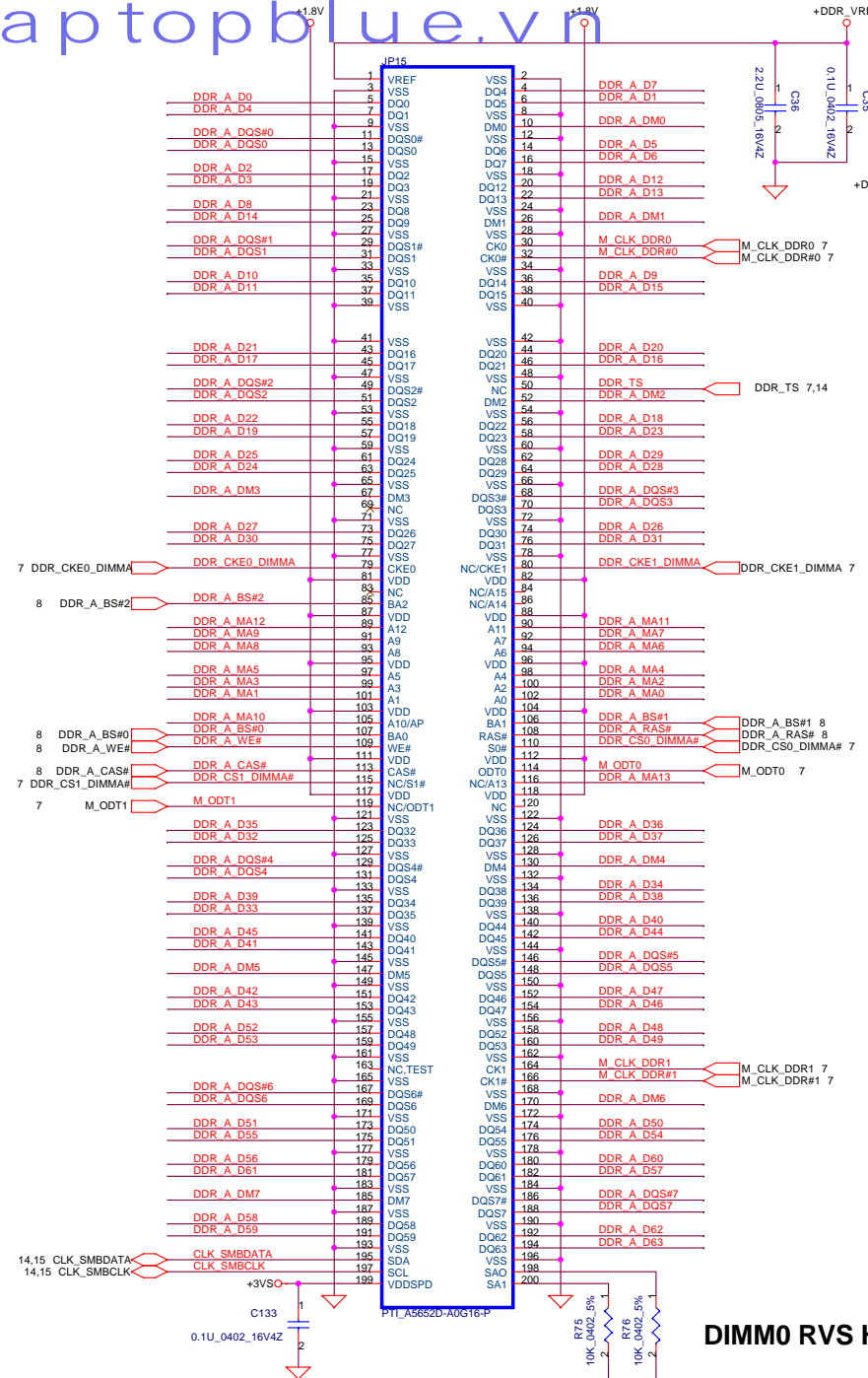
Layout Note:
Place near JP27



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor closely JP27, all trace length Max=1.5"

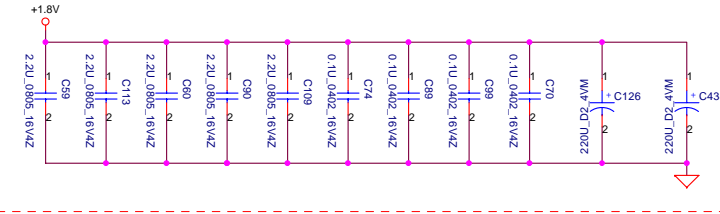


DIMM0 RVS H:5.2mm (BOT)

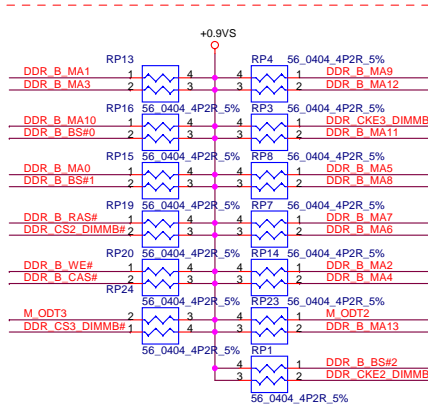
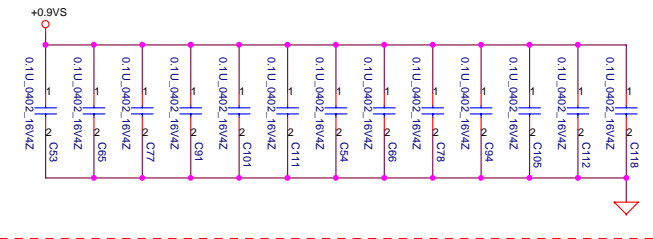
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8 DDR_B_DQS#[0..7]
8 DDR_B_D[0..63]
8 DDR_B_DM[0..7]
8 DDR_B_DQS#[0..7]
8 DDR_B_MA[0..13]

Layout Note:
Place near JP26

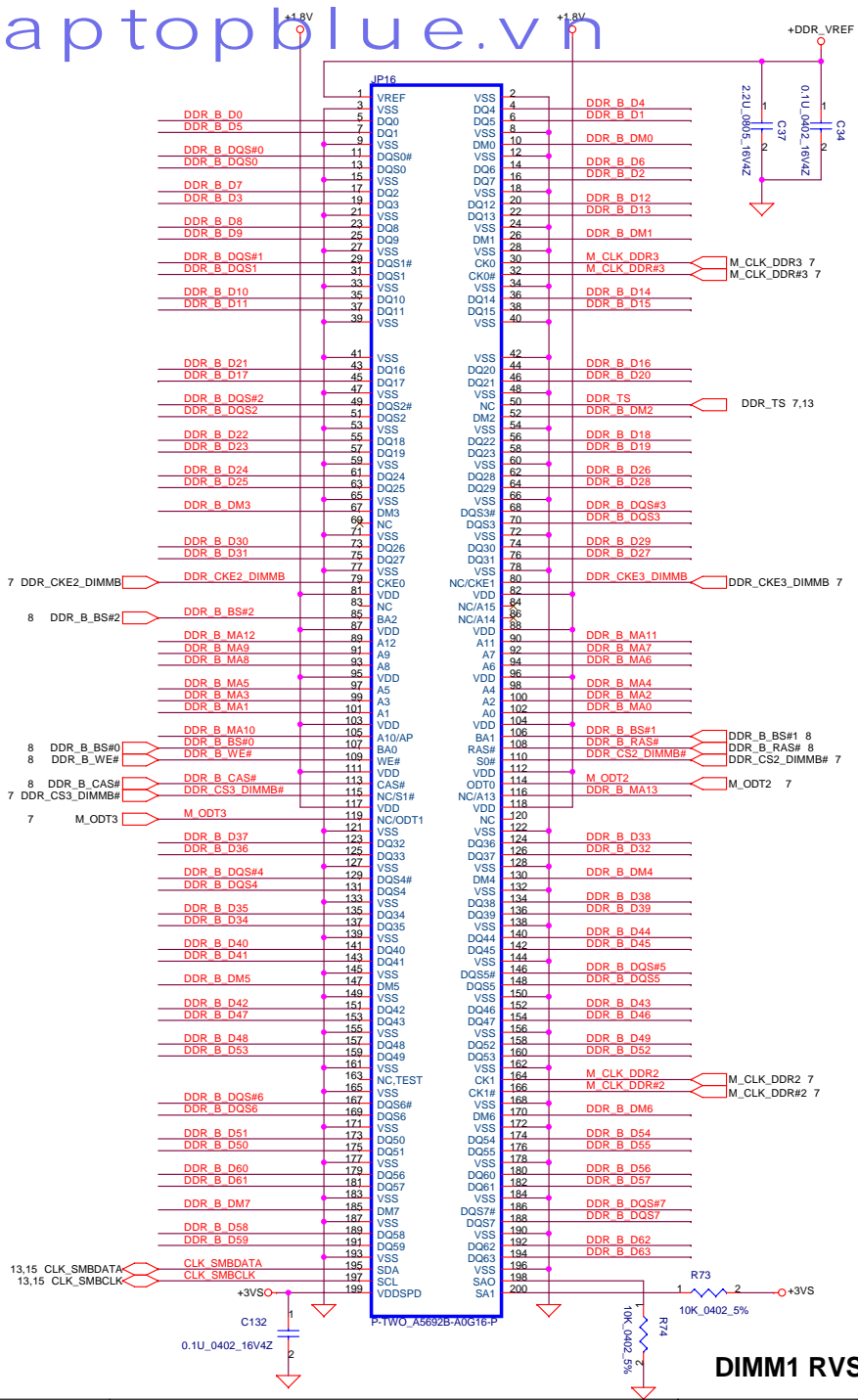


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor closely JP26, all trace length Max=1.5"

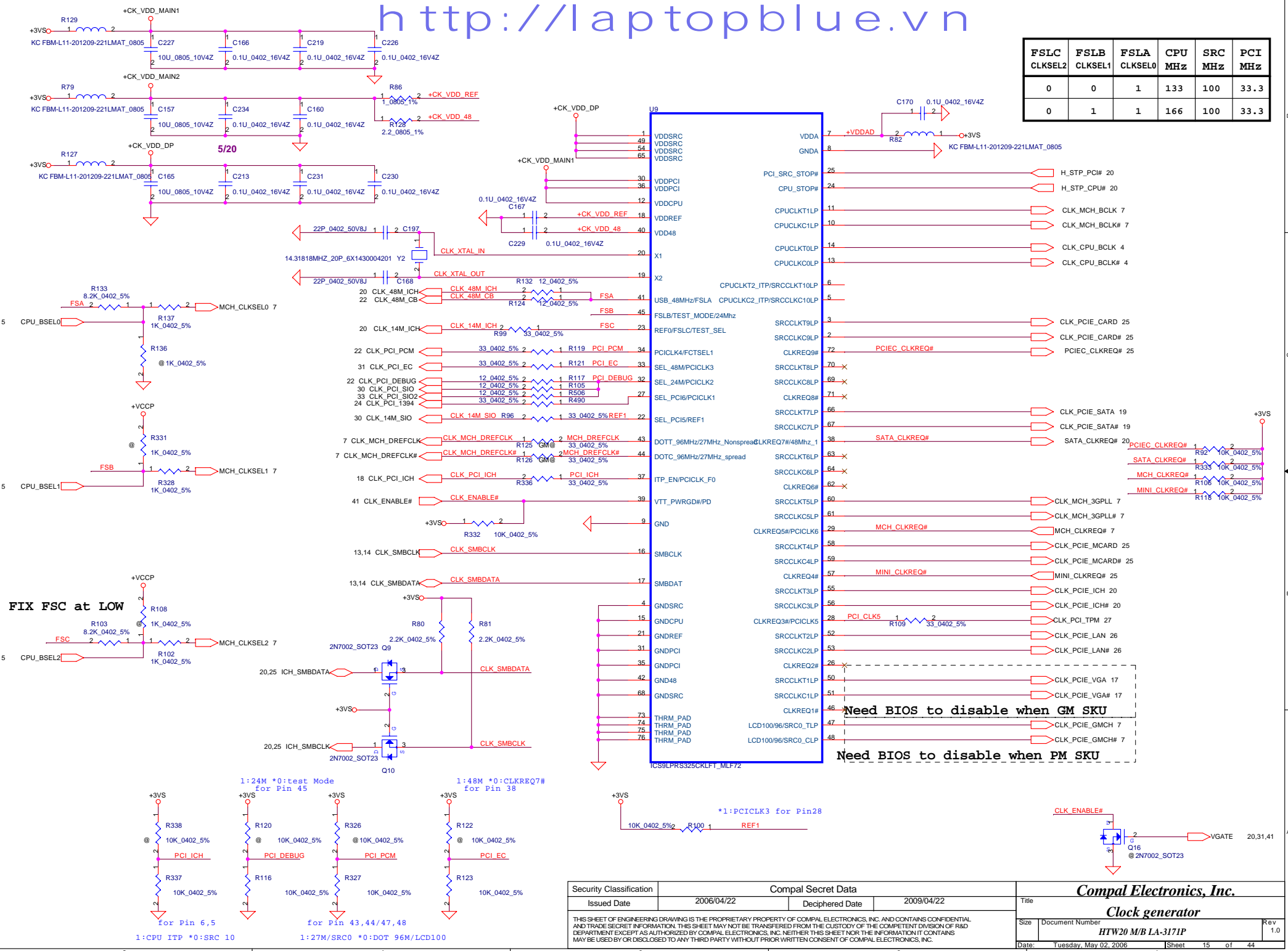
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DIMM1 RVS H:9.2mm (BOT)

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Deciphered Date								2009/04/22			
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Date:				Friday, April 28, 2006				Sheet 14 of 44			

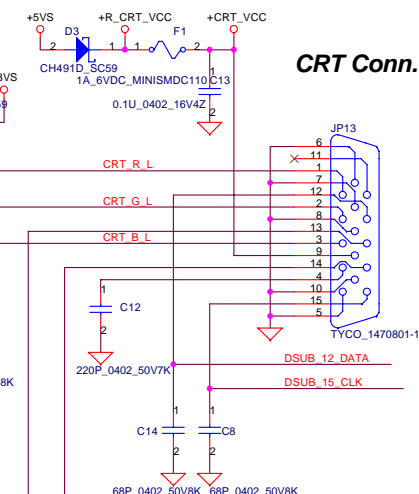
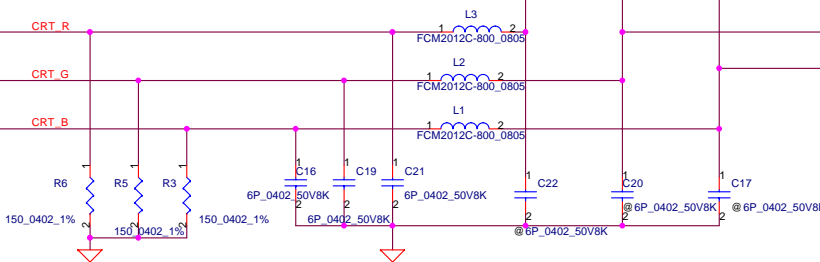
FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3



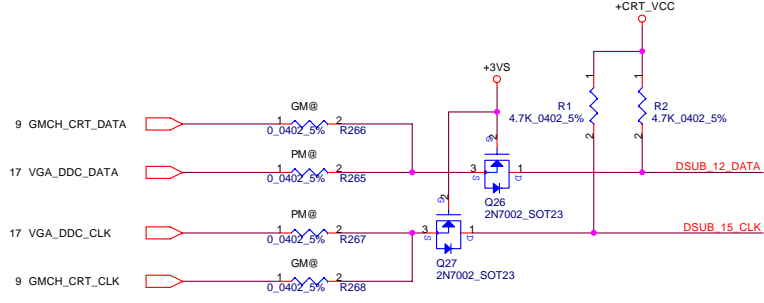
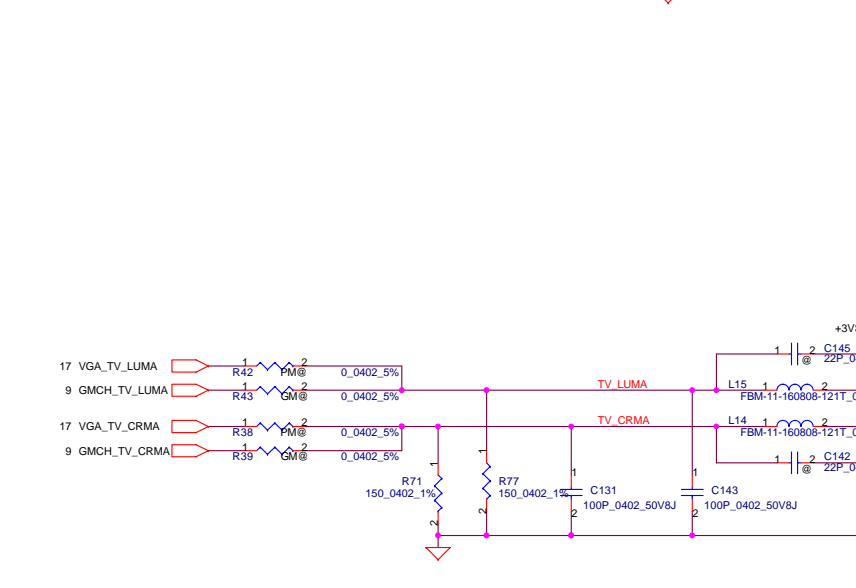
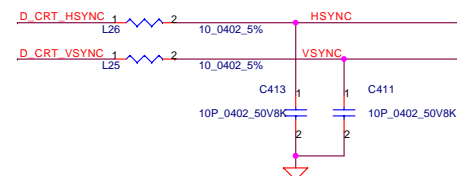
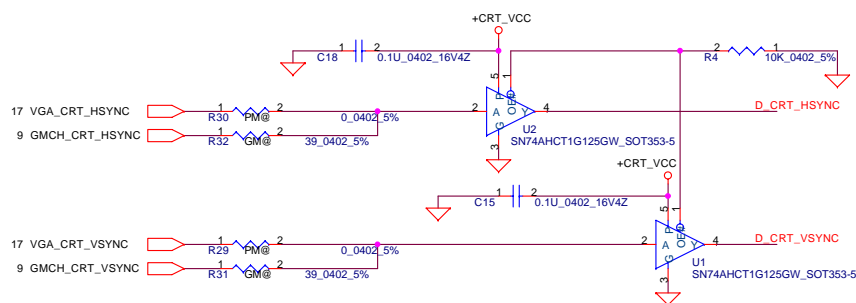
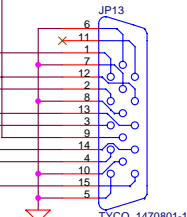
CRT Connector

17 VGA_CRT_R
9 GMCH_CRT_R
17 VGA_CRT_G
9 GMCH_CRT_G
17 VGA_CRT_B
9 GMCH_CRT_B

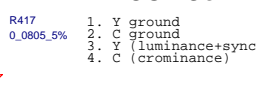
R277 1 2 PM@ 0.0402_5%
R278 1 2 GM@ 0.0402_5%
R275 1 2 PM@ 0.0402_5%
R276 1 2 GM@ 0.0402_5%
R273 1 2 PM@ 0.0402_5%
R274 1 2 GM@ 0.0402_5%



CRT Conn.



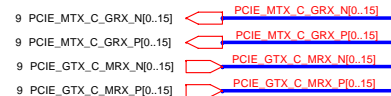
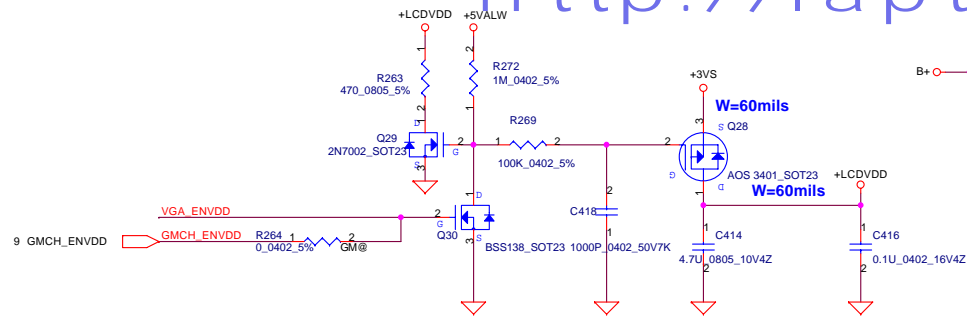
TV-OUT Conn.



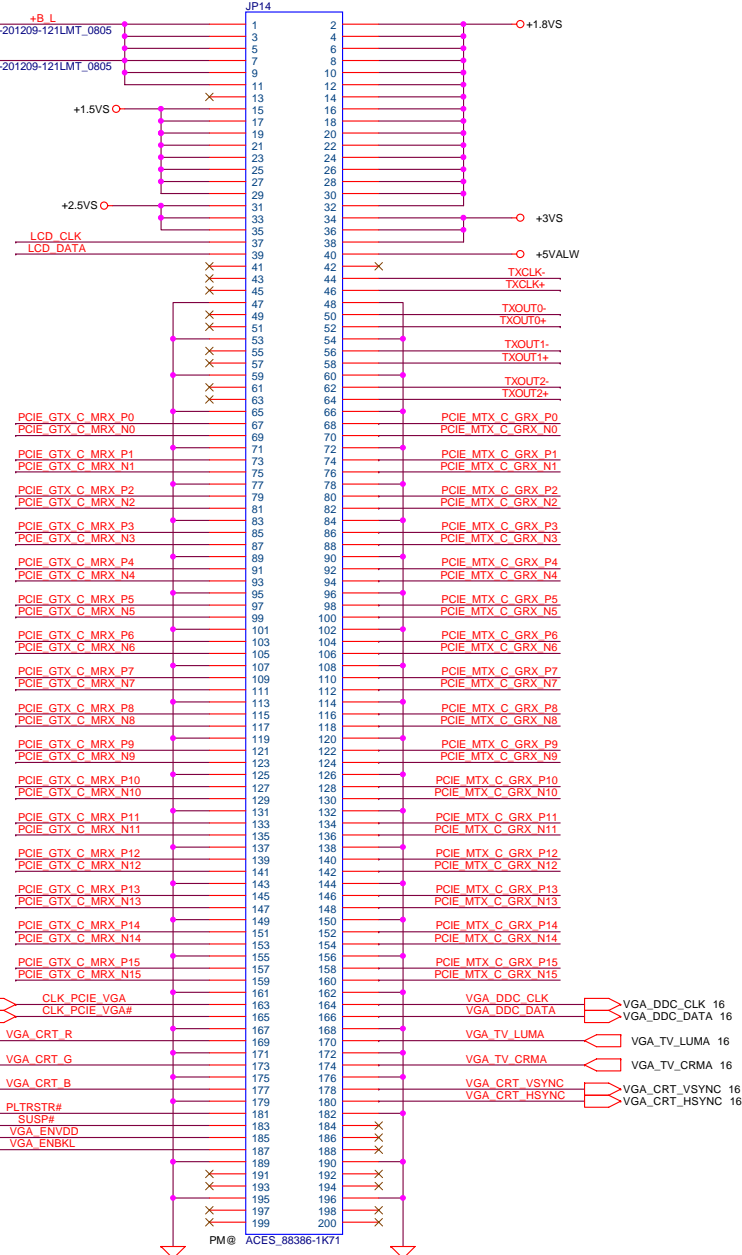
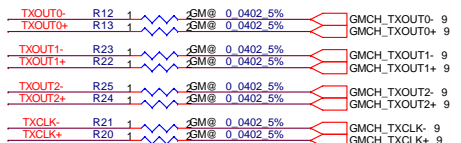
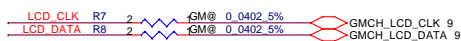
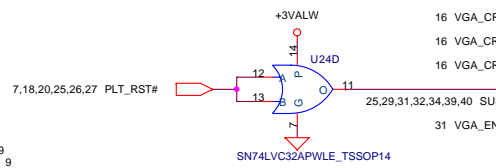
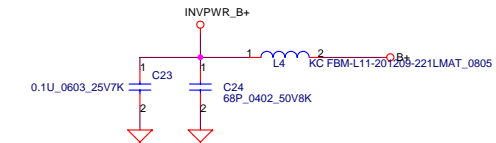
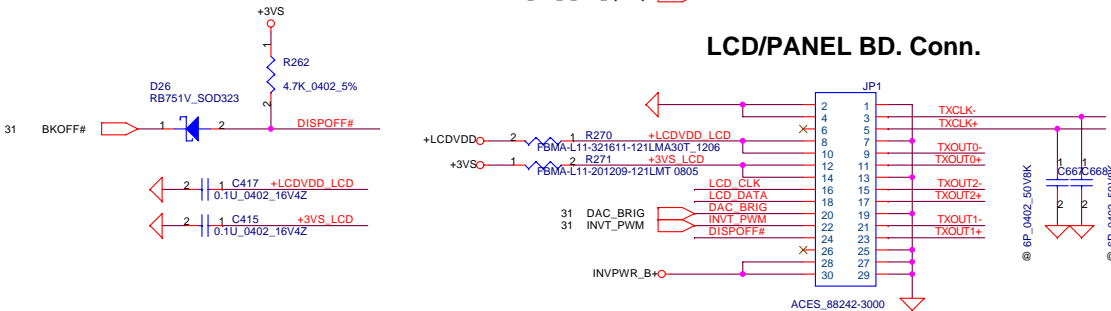
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2006/04/22				Title			
				Deciphered Date				CRT & Tvout Connector			
				2009/04/22				HTW20 M/B LA-3171P			
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				Date				1.0			
				Tuesday, May 02, 2006				Sheet 16 of 44			

LCD POWER CIRCUIT

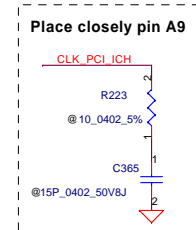
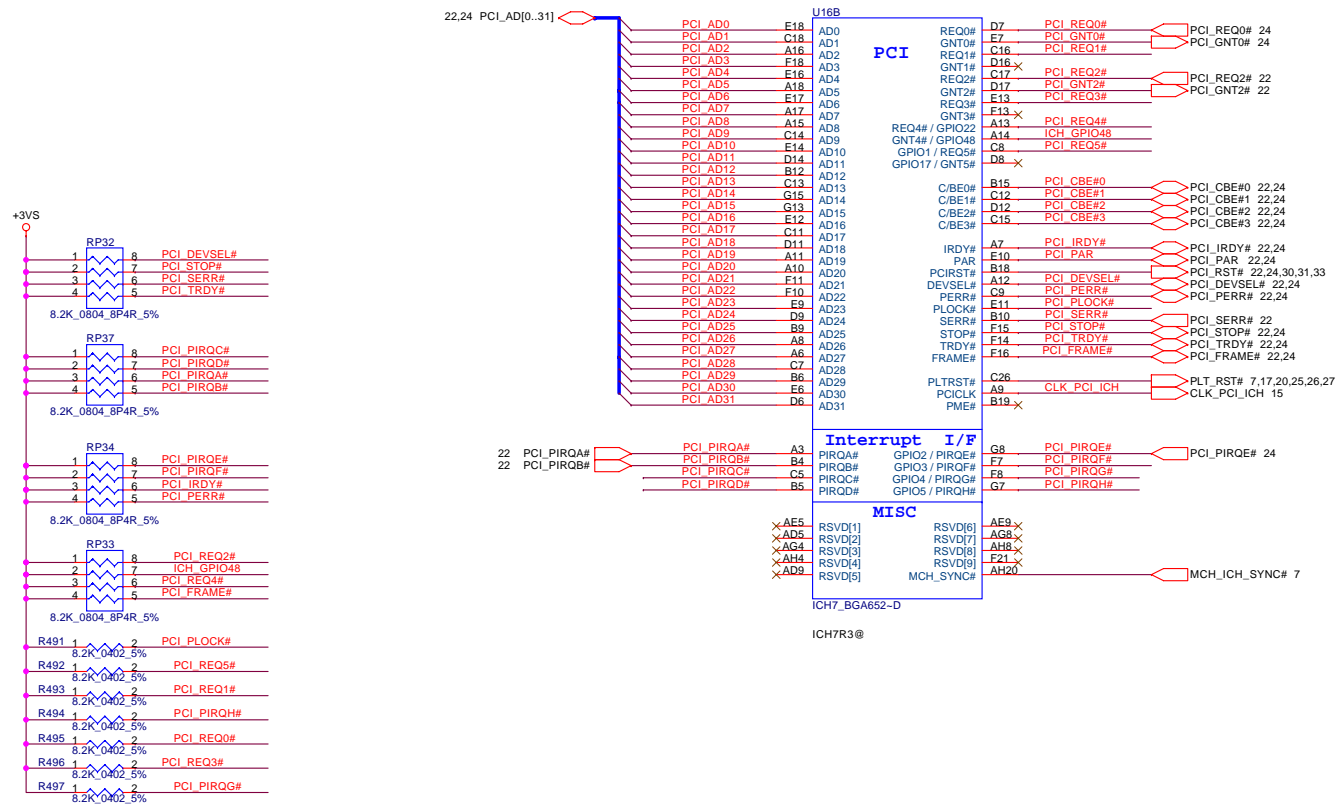
VGA BOARD Conn.



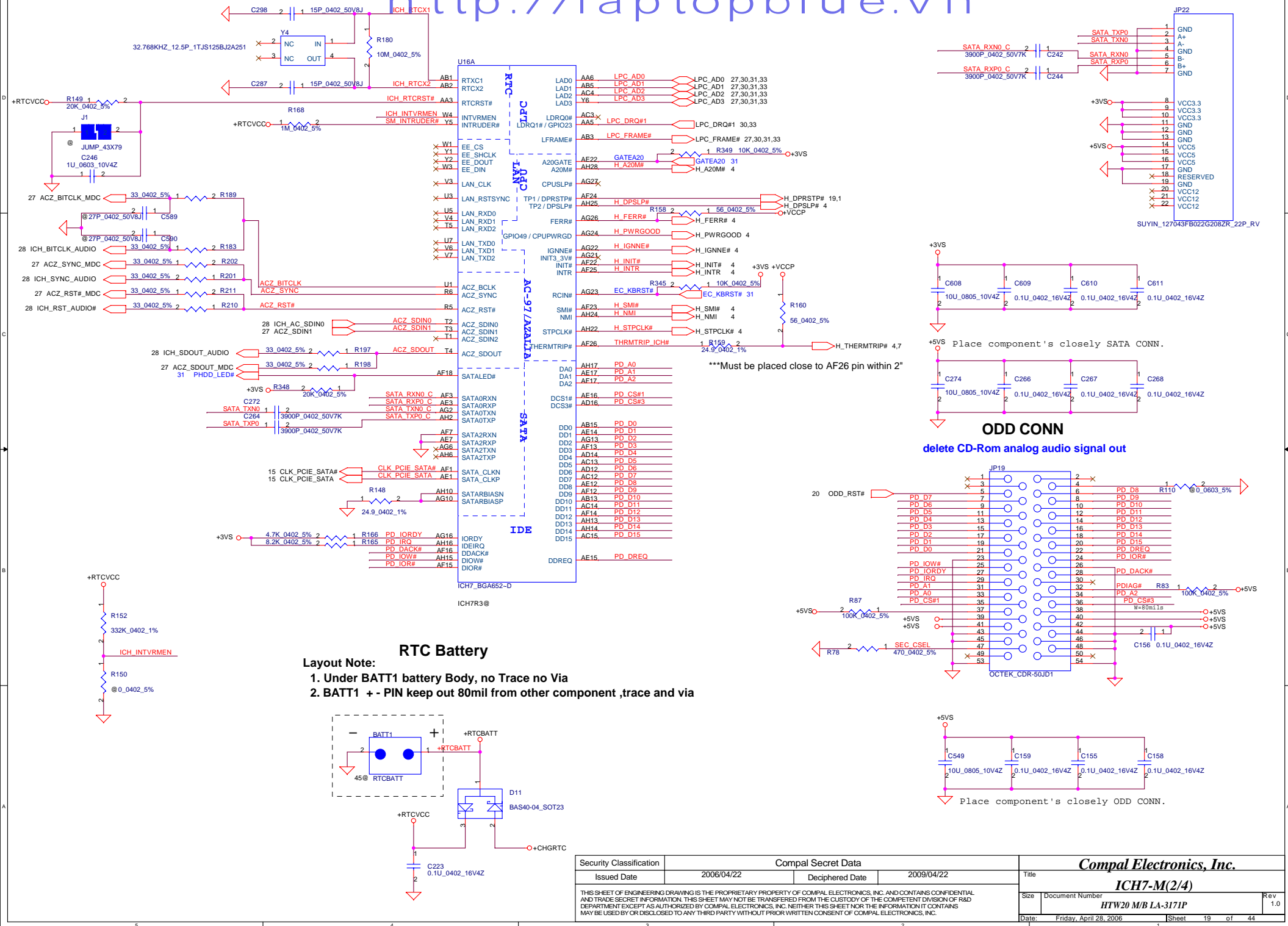
LCD/PANEL BD. Conn.



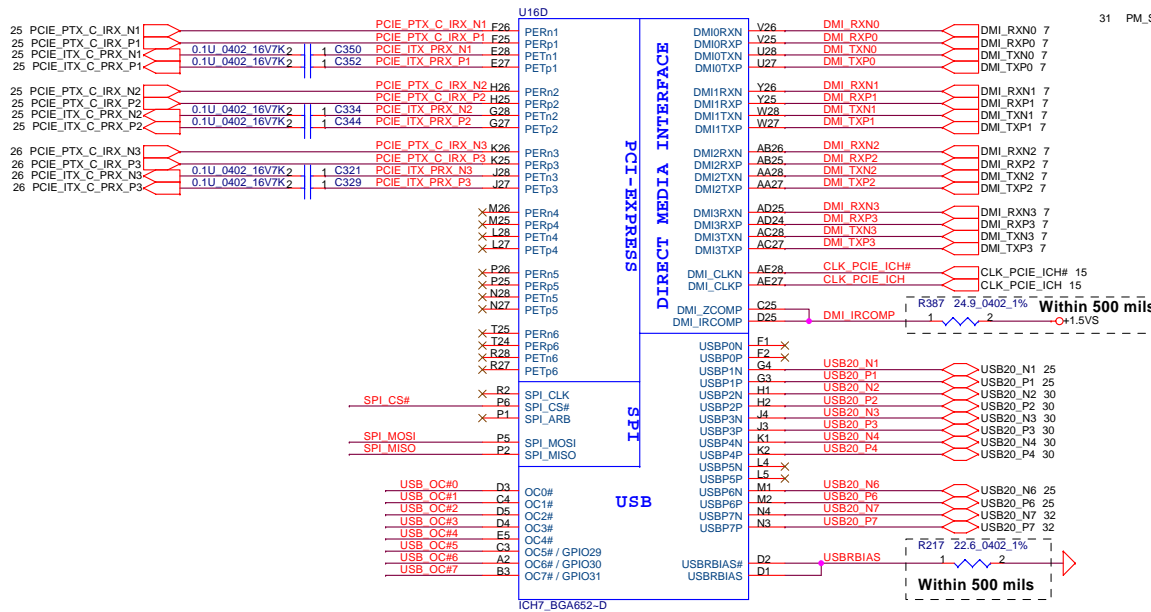
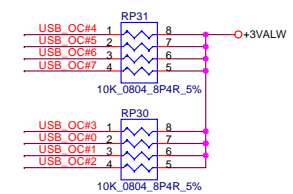
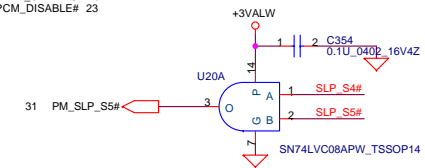
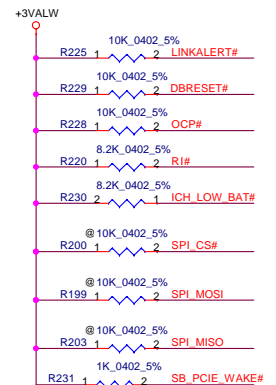
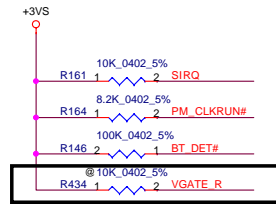
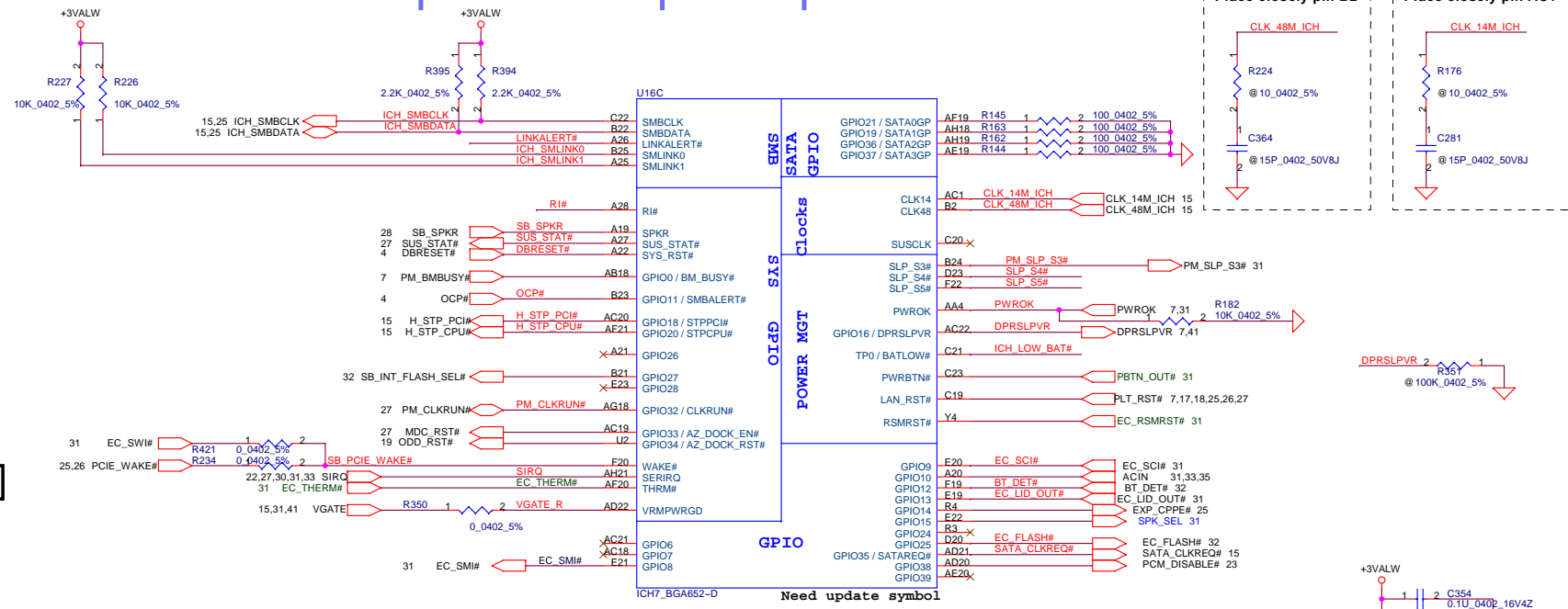
Security Classification		Compal Secret Data		Title	
Issued Date	2006/04/22	Deciphered Date	2009/04/22	VGA / LCD CONN.	
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				Rev	1.0



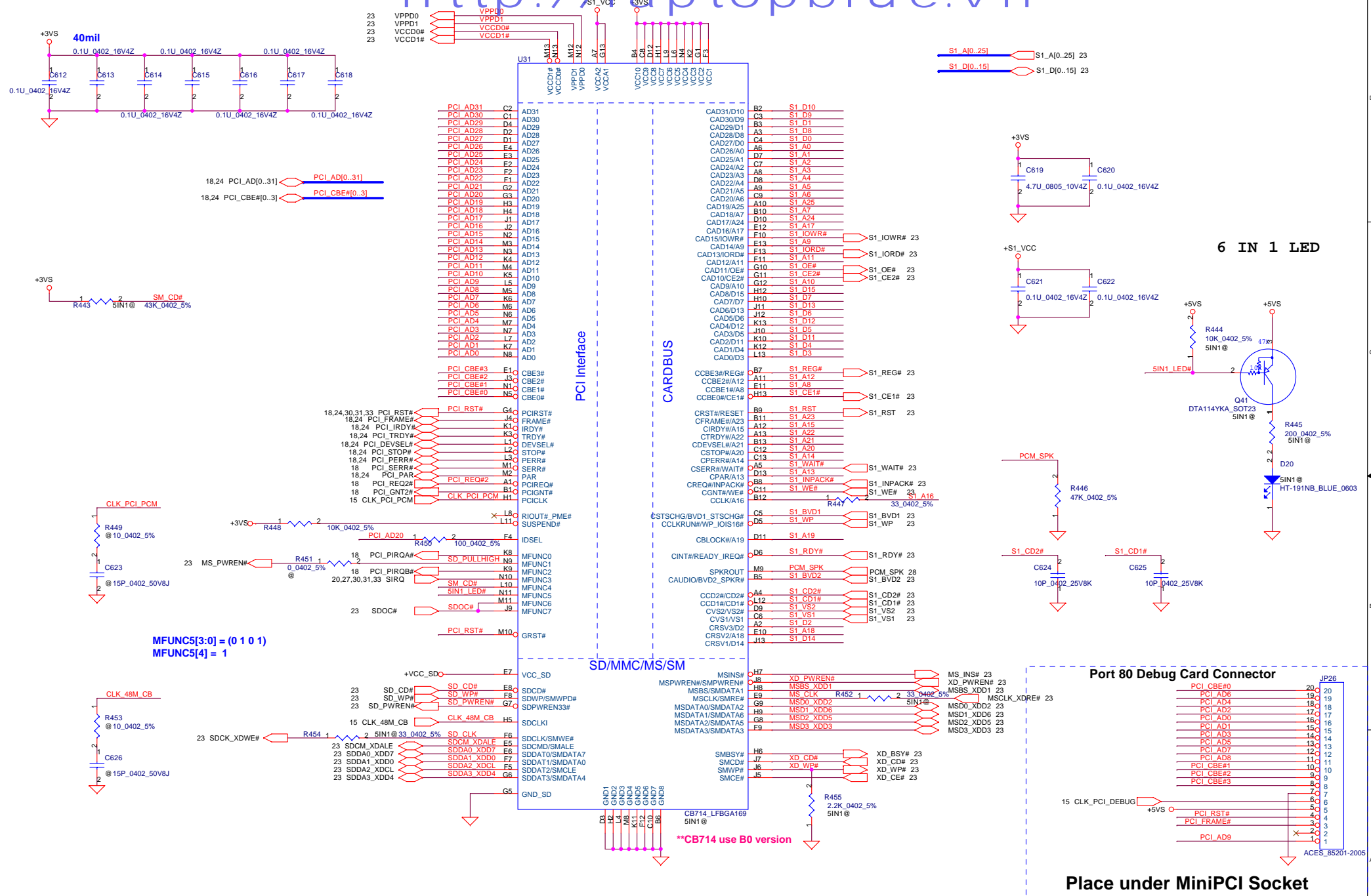
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Issued Date				2006/04/22				Title			
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								HTW20 M/B LA-3171P			
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								Date: Friday, April 28, 2006			
								Sheet 18 of 44			



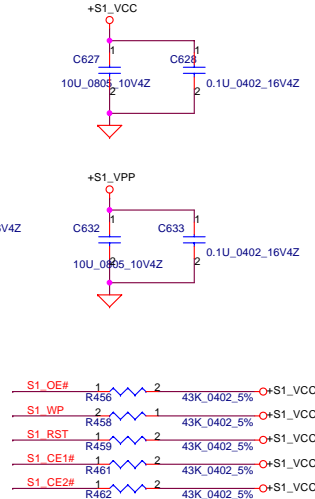
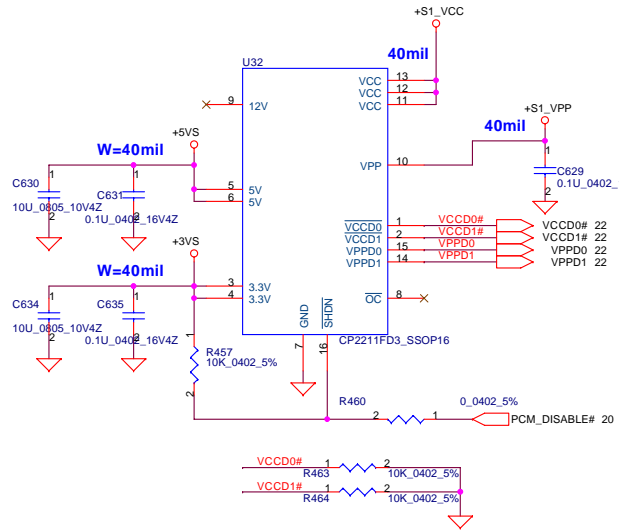
<http://laptopblue.vn>



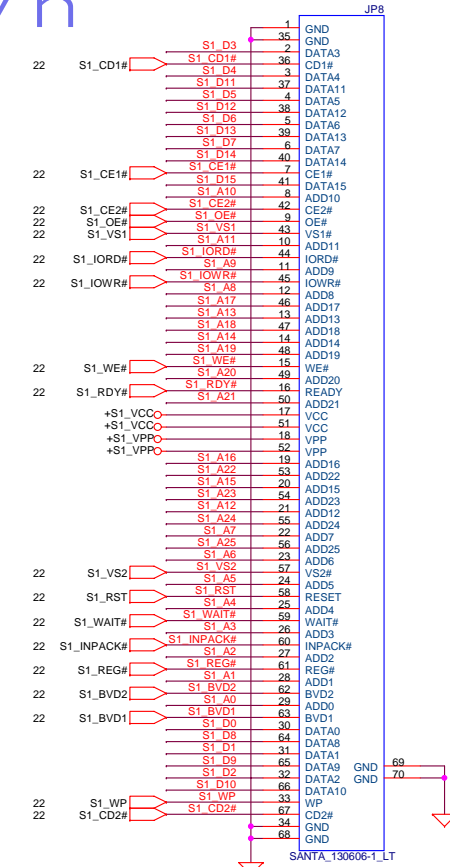
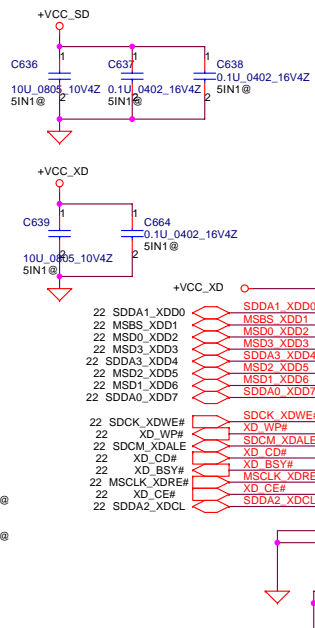
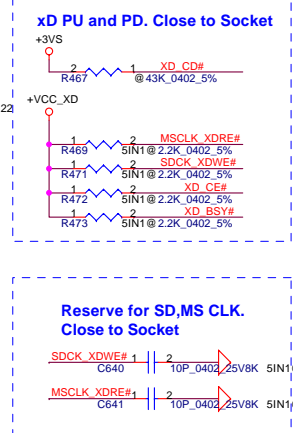
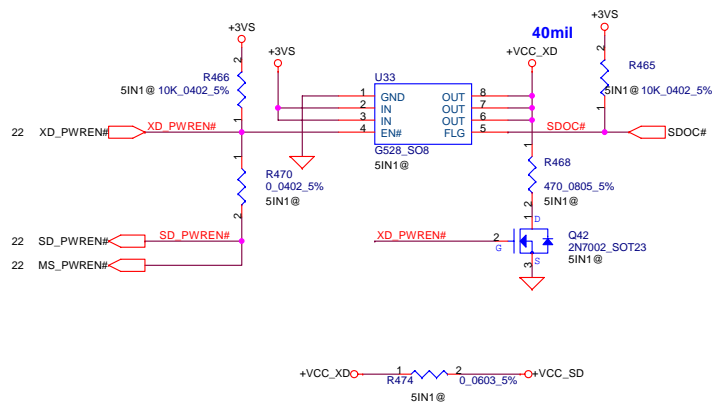
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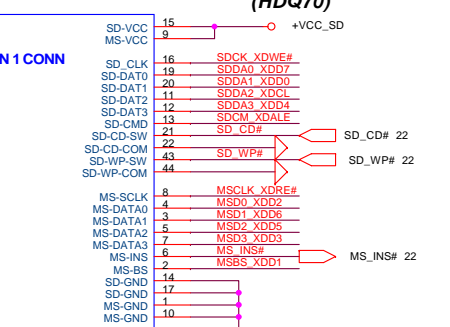
PCMCIA Power Control

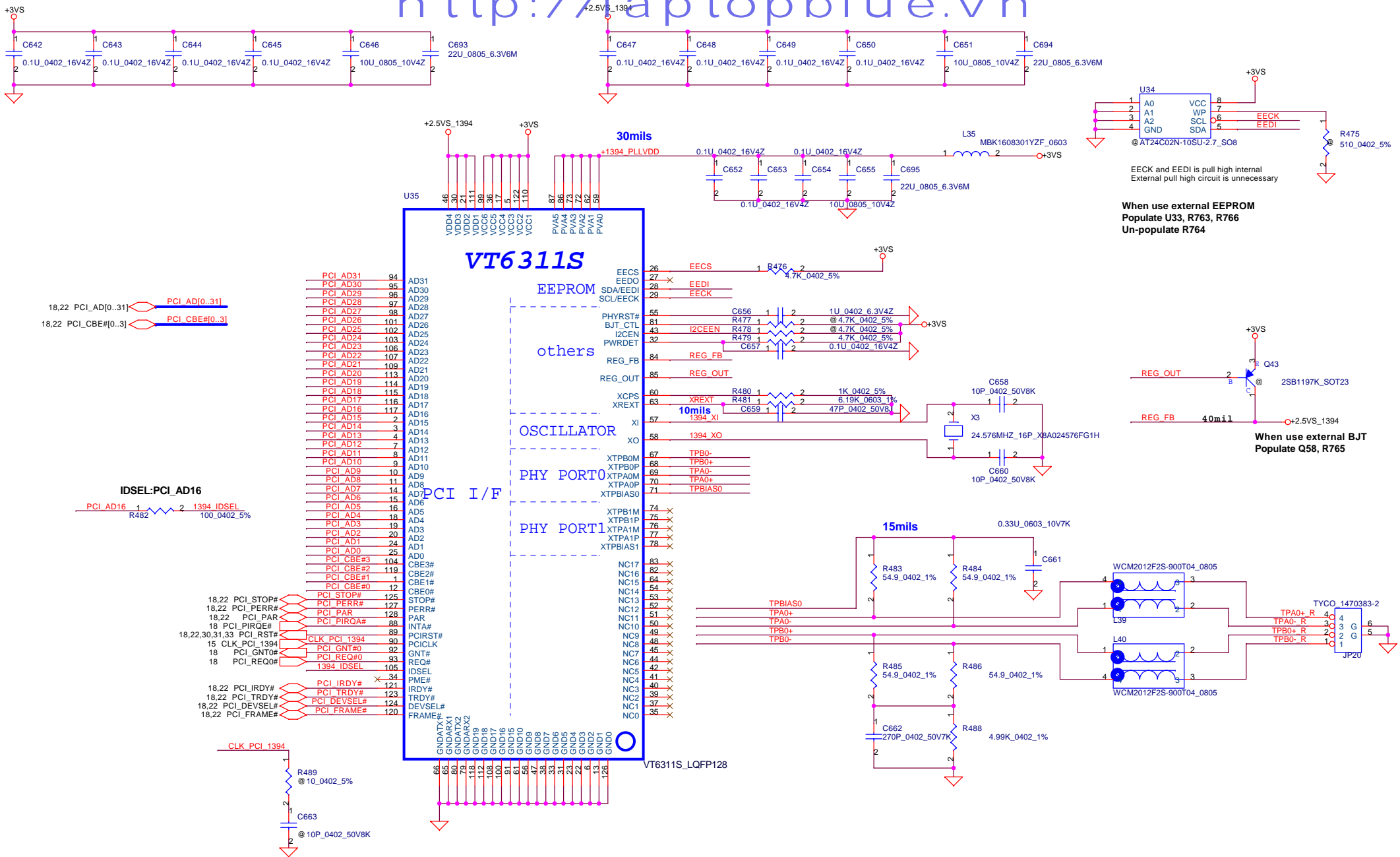


SD/MS Power Control XD Power Control

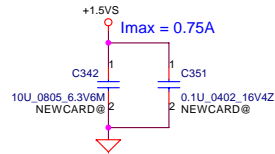
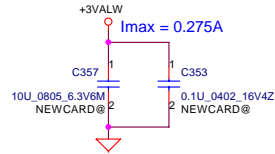
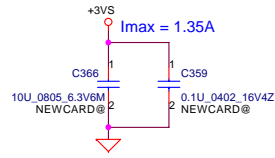


6 IN 1 Socket (HDQ70)

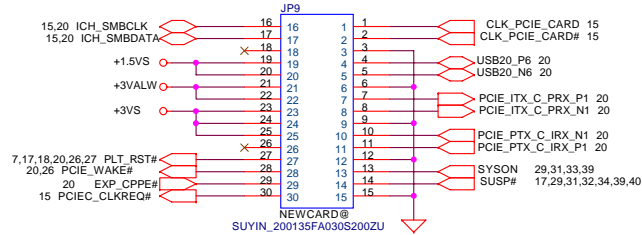




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New Card Connector

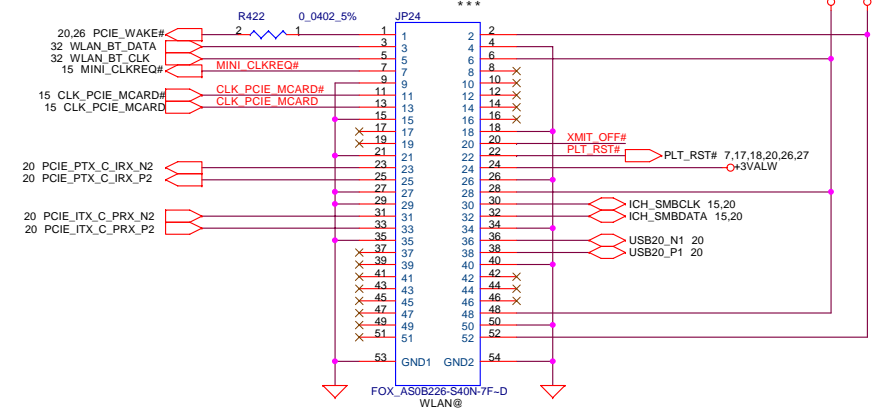
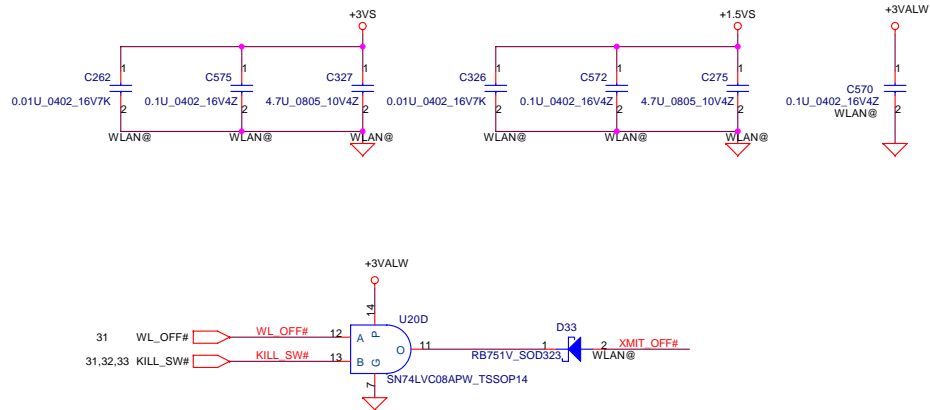


60mils I_max = 1.35A

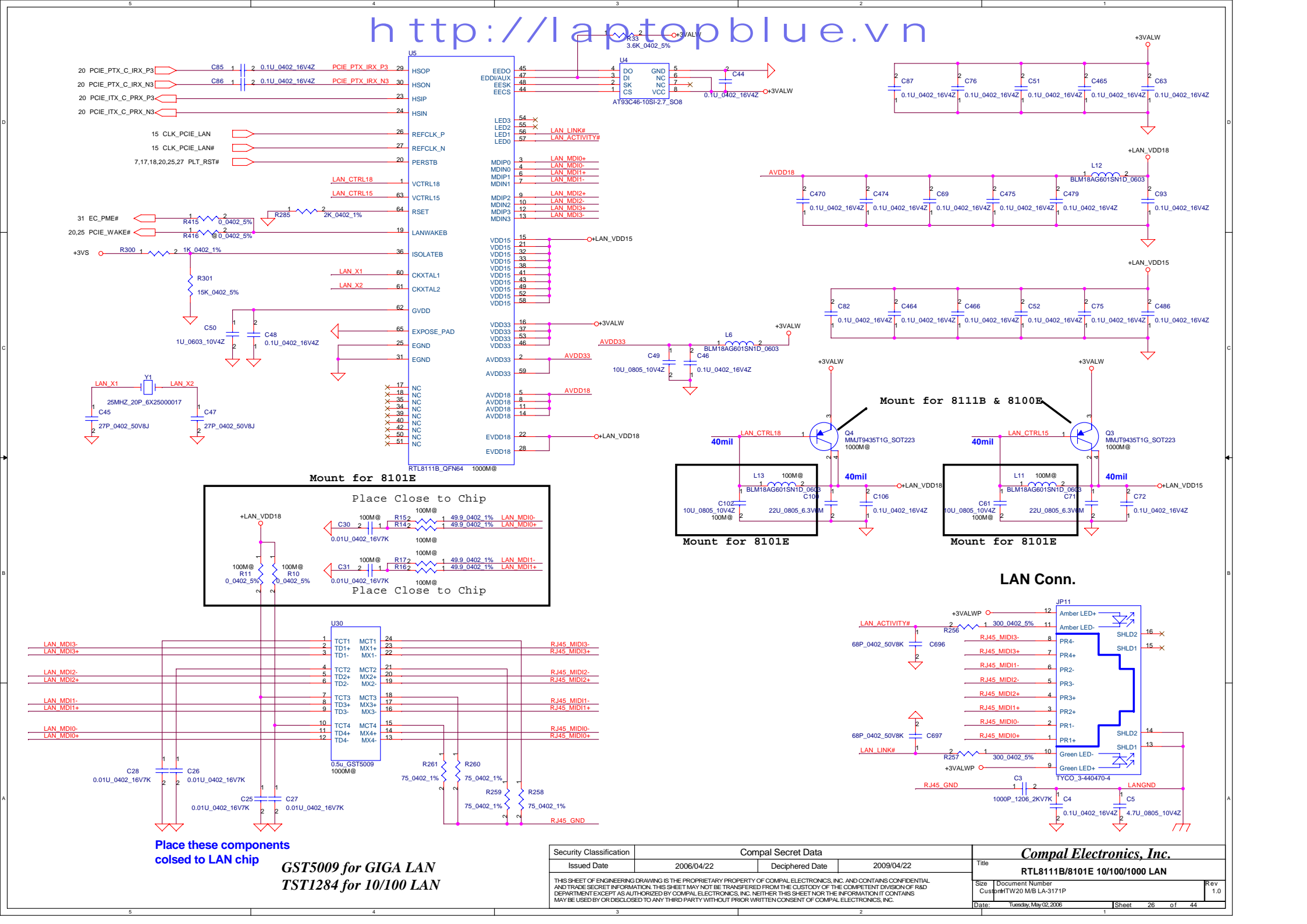
40mil I_max = 0.275A

40mil I_max = 0.75A

Mini-Express Card



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[illegible]

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The schematic diagram illustrates the electrical connections for the RTL8111B/8101E LAN controller. Key components include:

- U5 (RTL8111B_0FN64)**: The main LAN controller chip.
- U4 (AT93C46-10SI-2.7_S08)**: A non-volatile memory device connected to the controller's EEDO, EEDI/AUX, EESK, and EECS pins.
- Power Management**: Includes +3VLS, +3VALW, +LAN_VDD18, +LAN_VDD15, and AVDD33 supply rails with various decoupling capacitors (e.g., C85, C86, C87, C88).
- Signal Connections**: Shows connections for PCIe signals (PCIE_PTX_C_IRX_P3, PCIE_ITX_C_PRX_P3), clock signals (CLK_PCIE_LAN), reset signals (PLT_RST#), and LAN status signals (LAN_LINK#, LAN_ACTIVITY#).
- Magnetics**: Features two transformer models (BLM18AG601SN1D_0603) used for signal conditioning at the RJ45 ports.
- LED Indicators**: Connects the controller's LED pins to external LEDs (Amber LED+, Green LED+) through current-limiting resistors (R257, R258).

Place these components colsed to LAN chip

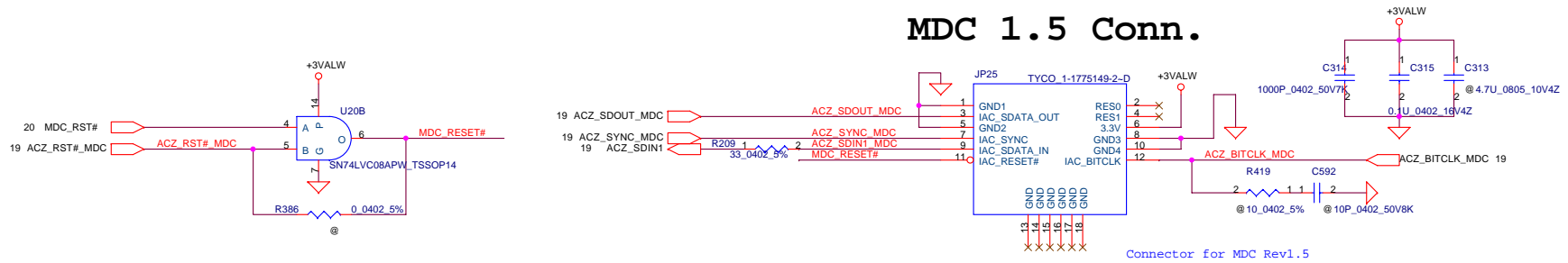
**GST5009 for GIGA LAN
TST1284 for 10/100 LAN**

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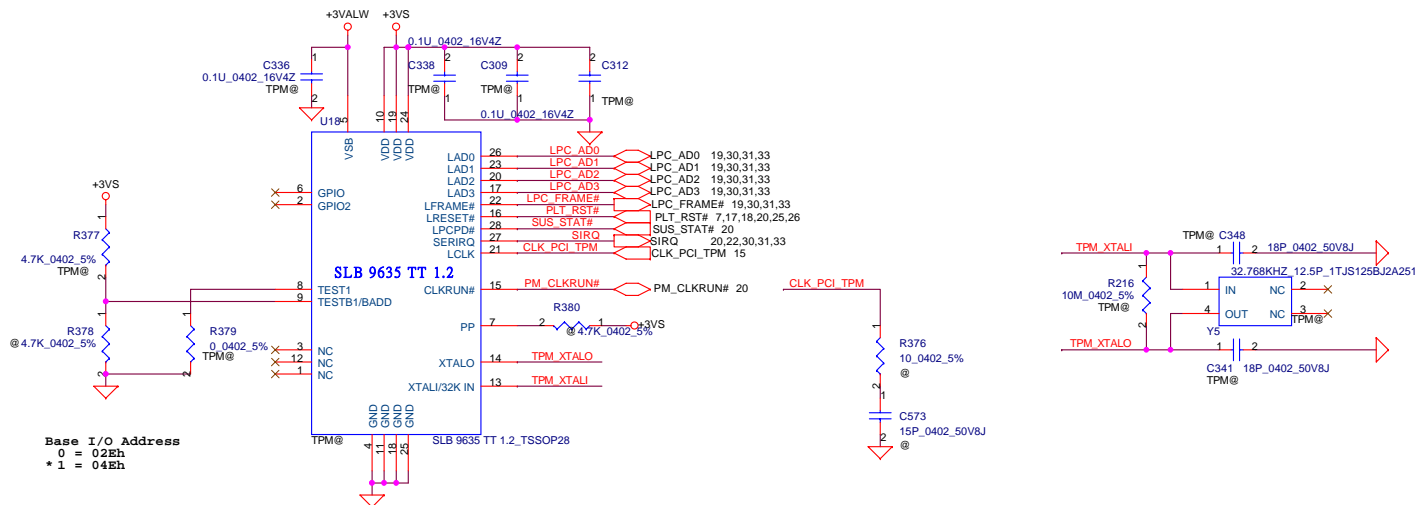
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RTL8111B/8101E 10/100/1000 LAN			
Size	Document Number	Date	Rev
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Sheet		of	
26		44	

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MDC 1.5 Conn.

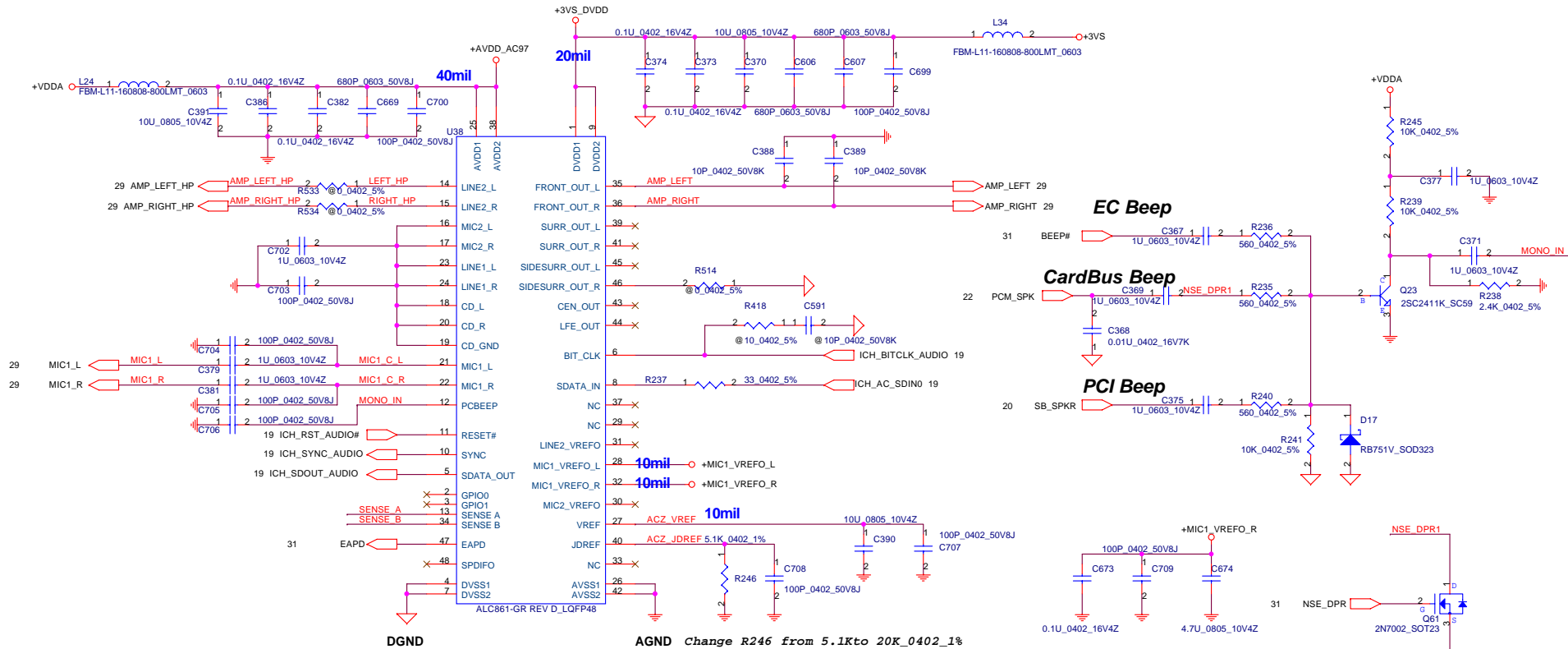


TPM1.2 on board



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					HTW20 M/B LA-3171P	1.0
				Date:	Tuesday, May 02, 2006	Sheet 27 of 44

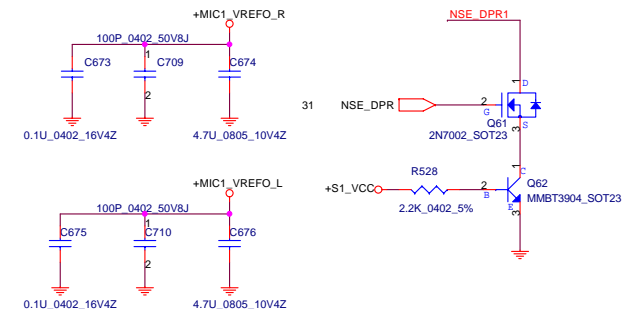
HD Audio Codec



EC Bleep

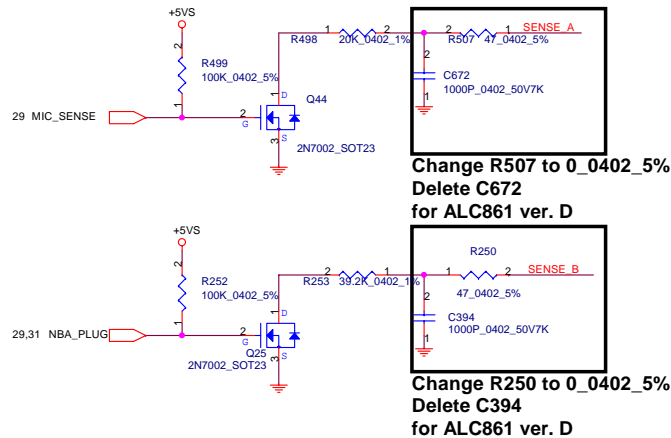
CardBus Bleep

PCI Bleep



DGND

AGND Change R246 from 5.1K to 20K_0402_1%

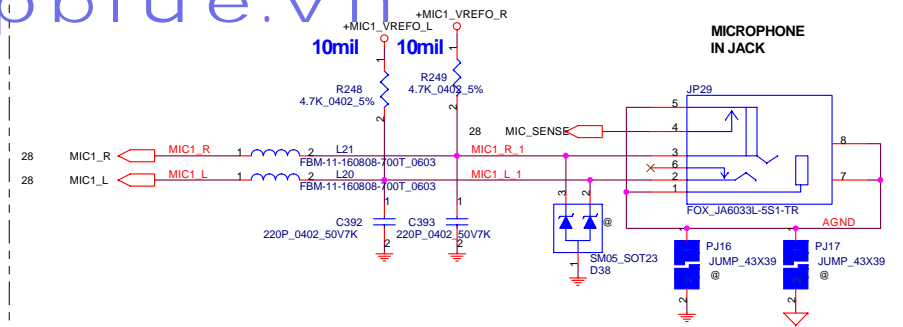


Change R507 to 0.0402_5%
Delete C672
for ALC861 ver. D

Change R250 to 0.0402_5%
Delete C394
for ALC861 ver. D

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

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Headset : 32 ~100Ohm (C > 248UF)
Paassive Speakers: 4 ~ 16Ohm (C >1989UF)
Active Speakers: 3K ~ 15K Ohm (C >2.65UF)

[illegible]

INTSPK_R1
INTSPK_R2
INTSPK_L1
INTSPK_L2

L7 1 2 HLMA-160808-39NKT
L10 1 2 HLMA-160808-39NKT
L8 1 2 HLMA-160808-39NKT
L9 1 2 HLMA-160808-39NKT

SPK_R1
SPK_R2
SPK_L1
SPK_L2

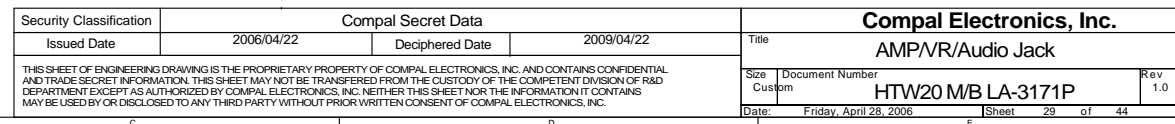
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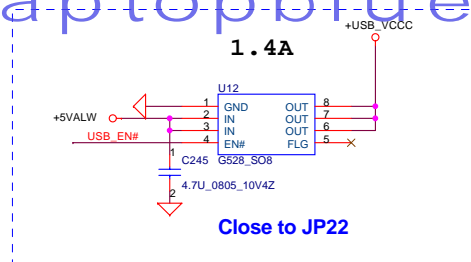
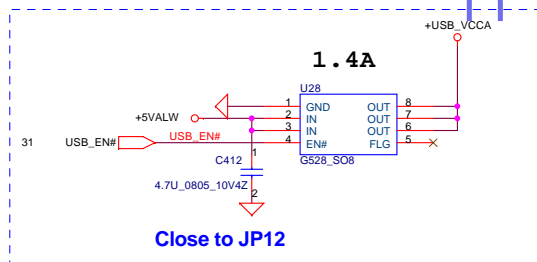
D4
SM05_SOT23

D5
@ SM05_SOT23

Gain Setting		
	DB	VOL AMP
SPK	10	0.66-3.7
HP	0	1.18-3.9

The schematic shows the power supply circuitry. A +5VS input is connected through resistor R530 (100K_0402_5%) to the drain of MOSFET Q6A (2N7002_SOT23). The gate of Q6A is driven by the NBA_PLUG signal. The source of Q6A is connected to ground. The output of the MOSFET is connected to the drain of MOSFET Q6B (2N7002_SOT23), which has its source grounded. The gate of Q6B is connected to the drain of Q6A through resistor R531 (4.3K_0402_5%). The output of Q6B is connected to the positive terminal of the output capacitor C698 (0.01W_10KC_EVUF_R849C14 @ 0.1U_0402_16V4Z) and also passes through resistor R532 (4.3K_0402_5%) to ground. The negative terminal of the output capacitor is connected to ground. A +5VS input is also shown at the top right, connected to a network of resistors (R529, 3.9K_0402_5%) and a diode (VR1, 0.01W_10KC_EVUF_R849C14 @ 0.1U_0402_16V4Z) before reaching the output capacitor.

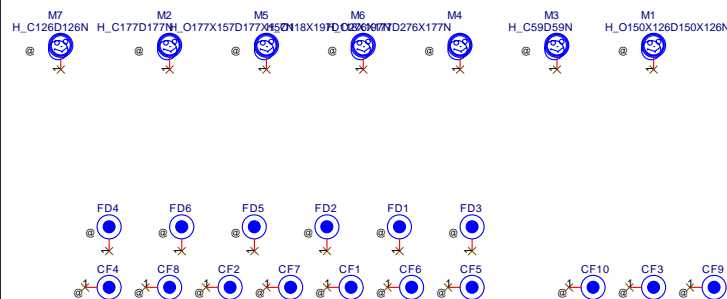
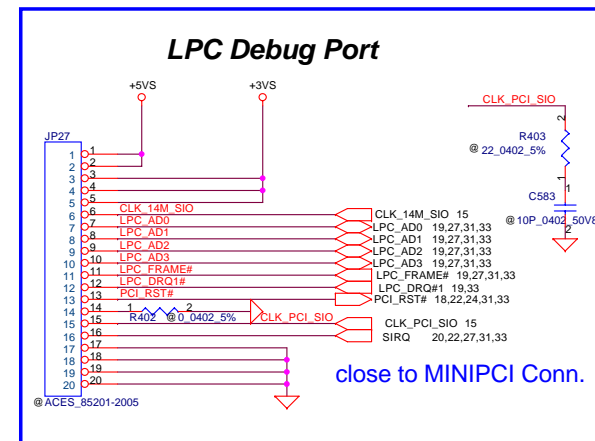
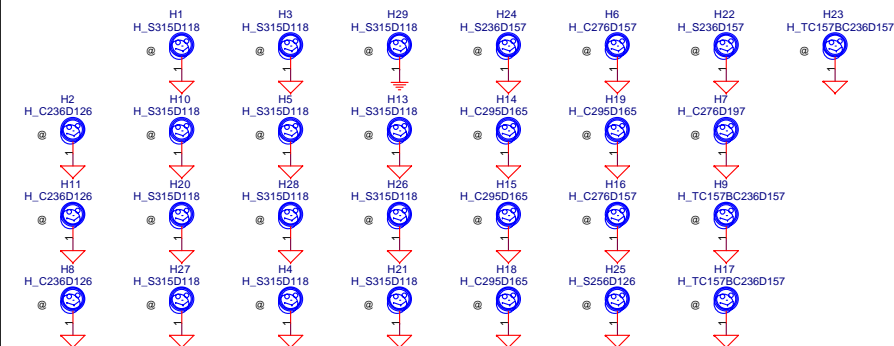
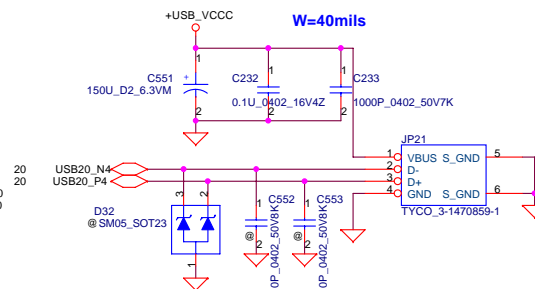
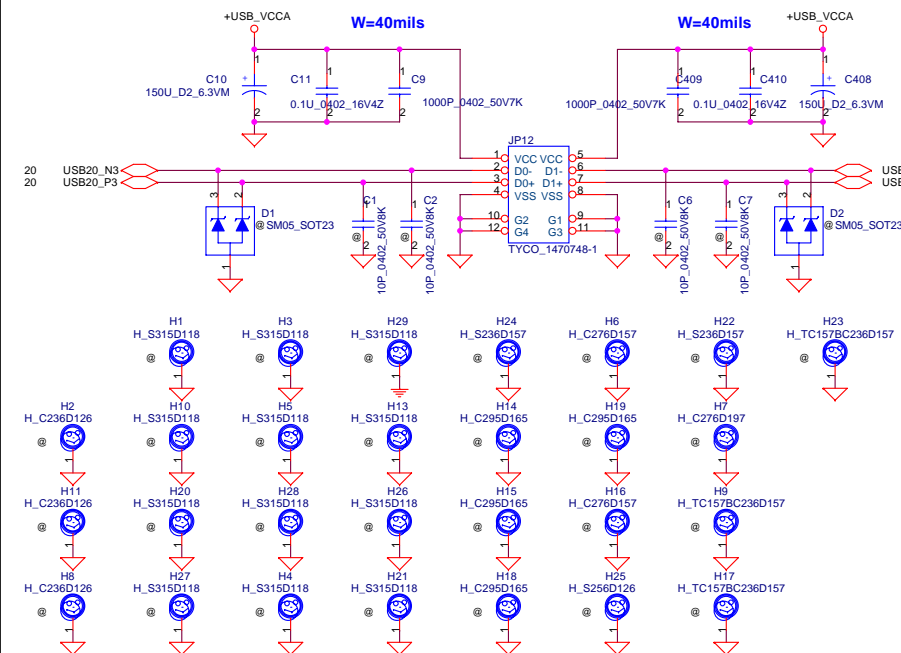




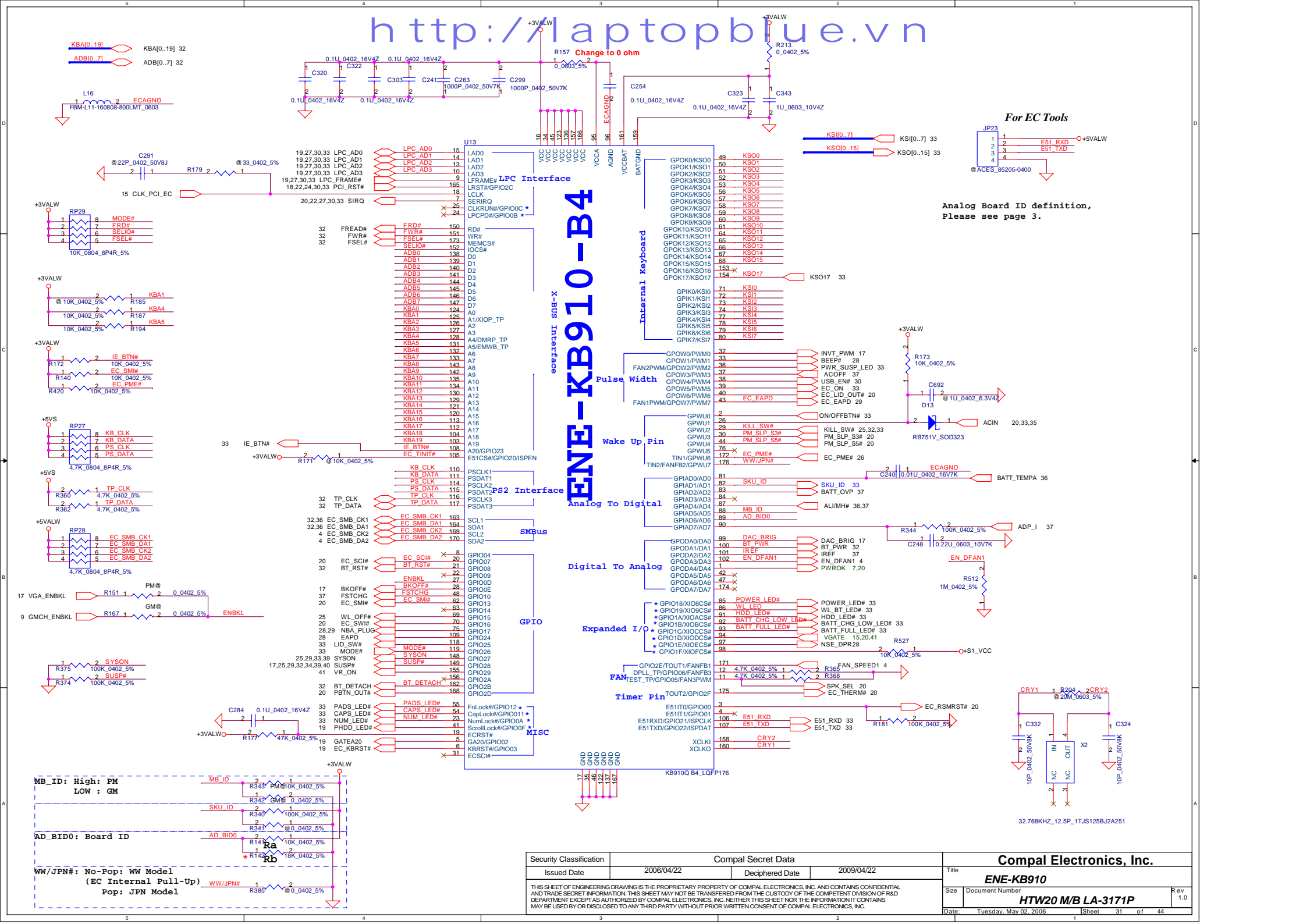
USB CONN. 1

USB CONN. 2

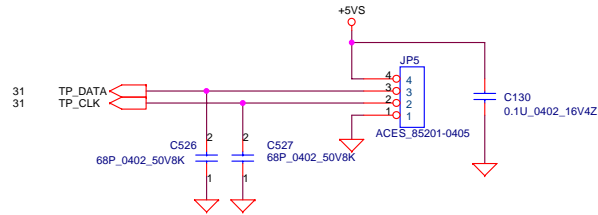
USB CONN. 3



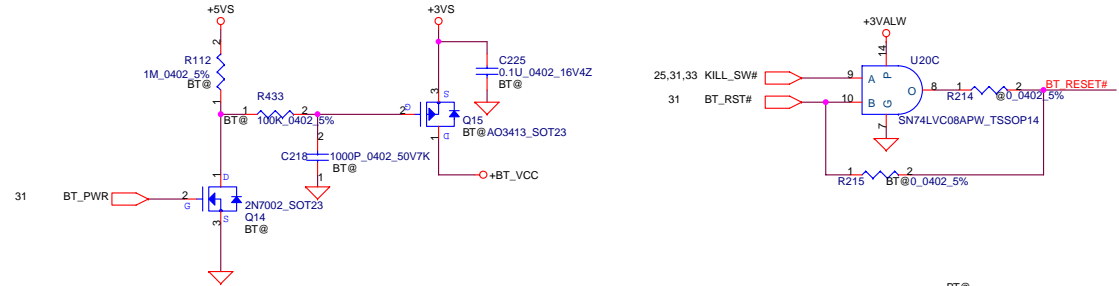
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Issued Date	2006/04/22	Deciphered Date	2009/04/22	Title	
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				Rev	1.0



TP CONN.

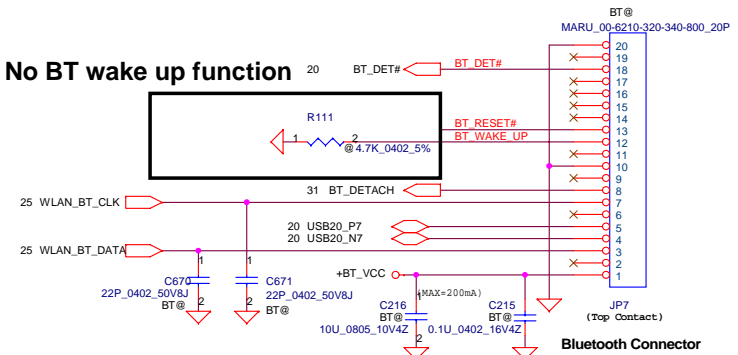


BlueTooth Interface



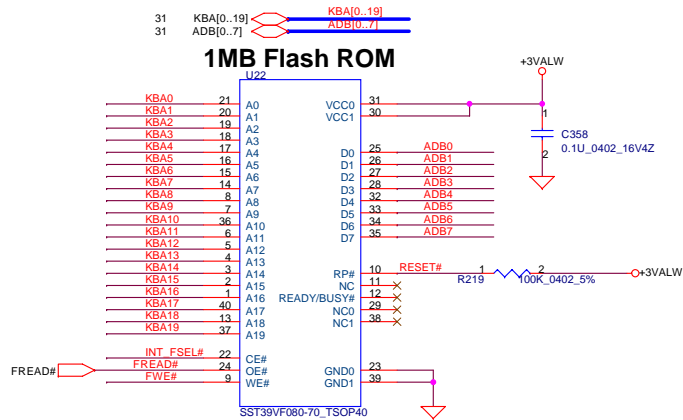
Module ID
Indication for polarity of reset
Reset input High Active -> Low.
Reset input Low Active -> Open

No BT wake up function

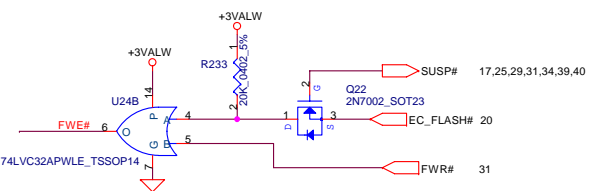
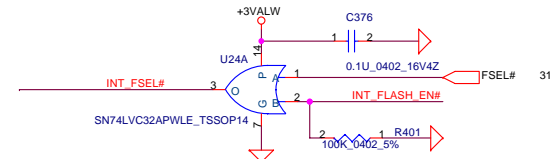
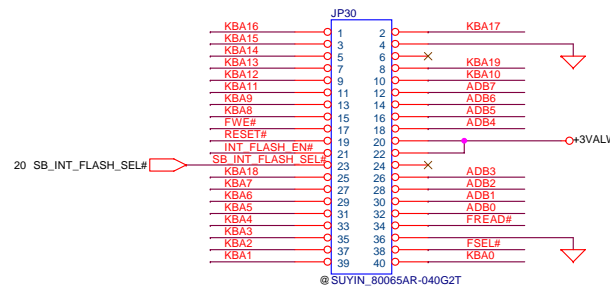


Bluetooth Connector

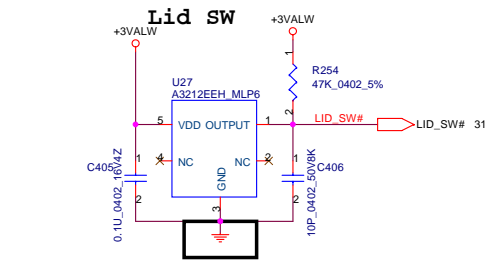
1MB Flash ROM



1MB ROM Socket



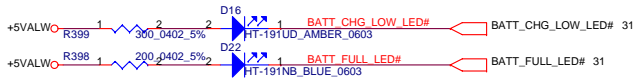
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				Size	Document Number
				HTW20 MB LA-3171P	
				Date	Rev
				Friday, April 28, 2006	1.0
				Sheet	32 of 44



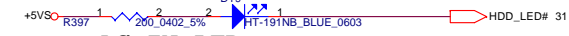
**POWER/ON(Green Pin2,1)
Suspend (Amber Pin3,4) LED**



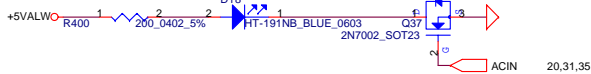
**BATTERY CHG(Green Pin2,1)
BATTERY LOW(Amber Pin3,4) LED**



HDD LED

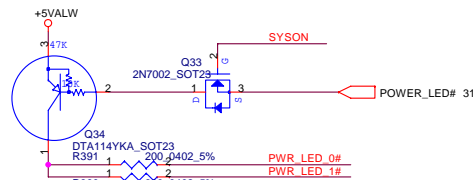
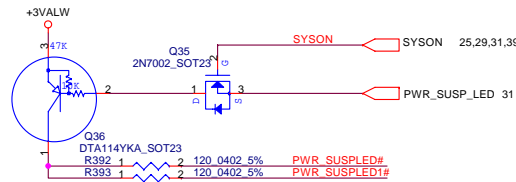
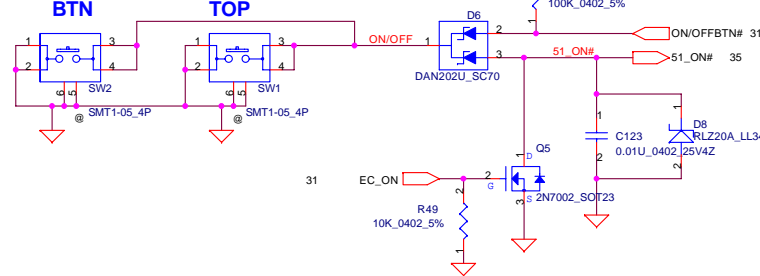


AC IN LED

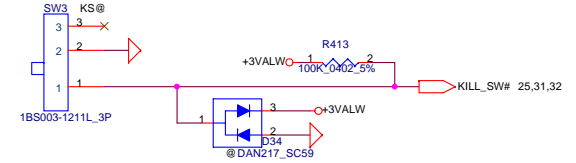


ON/OFF BUTTON

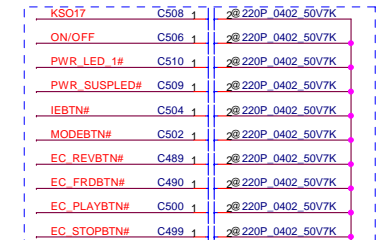
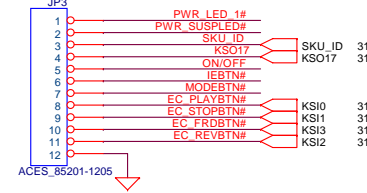
for debug only



Kill SWITCH

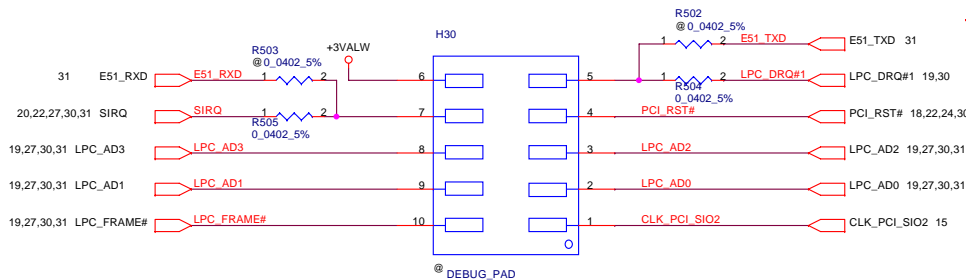


SW/LED Connector



For EMI Request

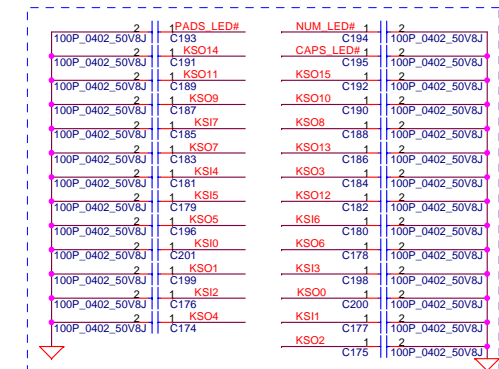
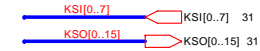
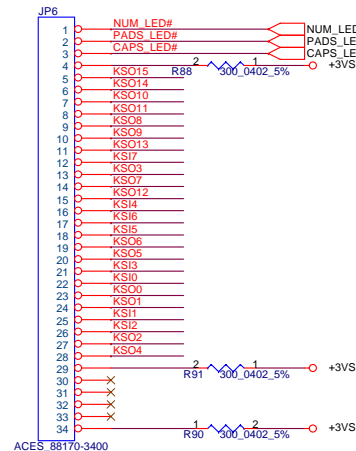
New LPC Debug Pad ---- MB side



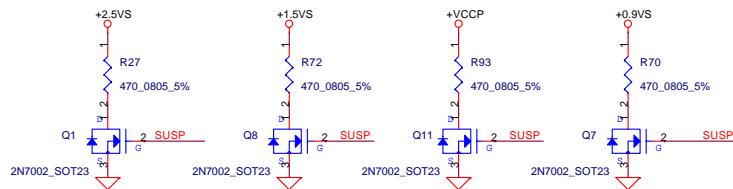
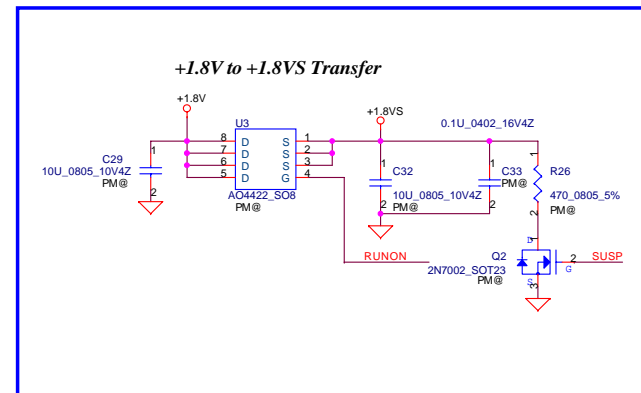
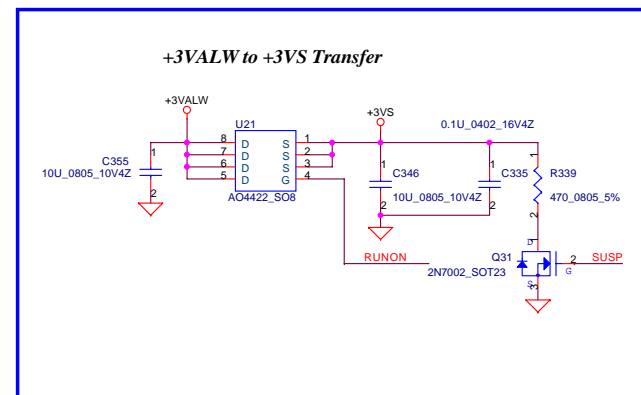
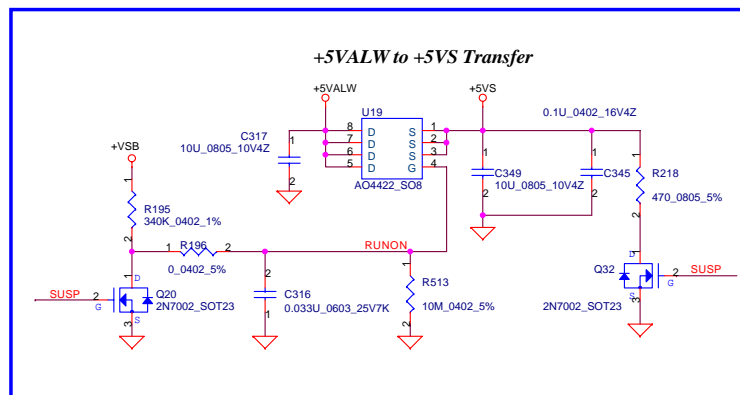
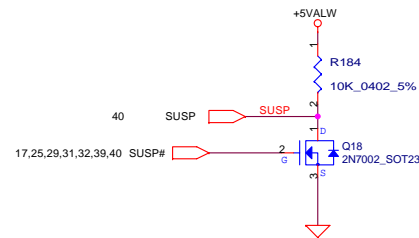
Under DDR ME Assignment Area

**Keep Resistor near Debug Pad and in the same side
Reverse side DIMM ---- Pin 1 keep away DIMM**

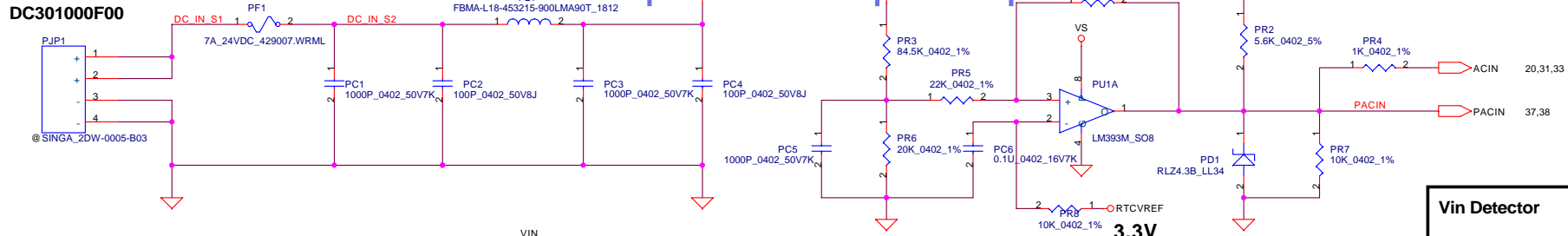
KEYBOARD CONN.



For EMI Request

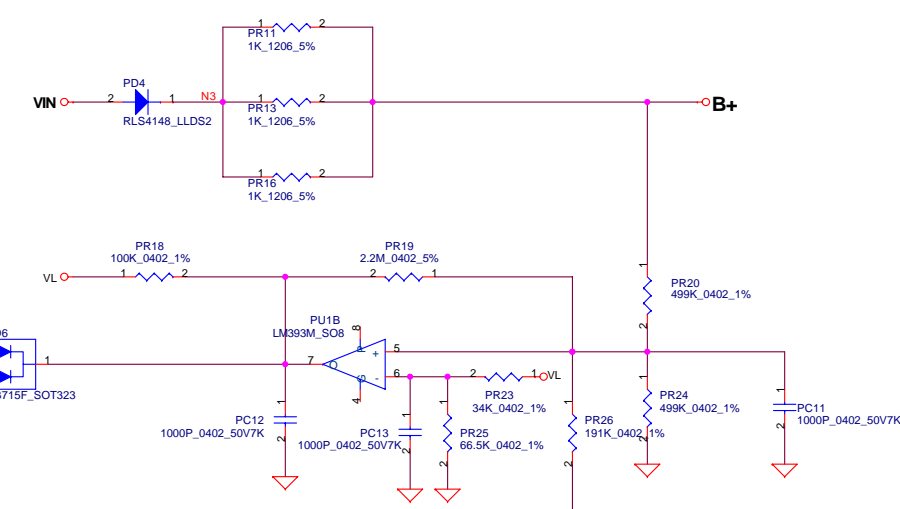
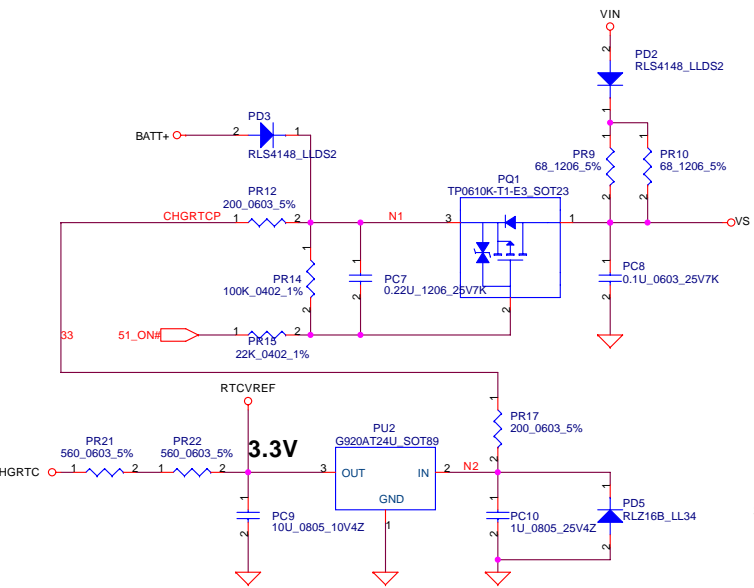


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Vin Detector

High	18.384	17.901	17.430
Low	17.728	17.257	16.976

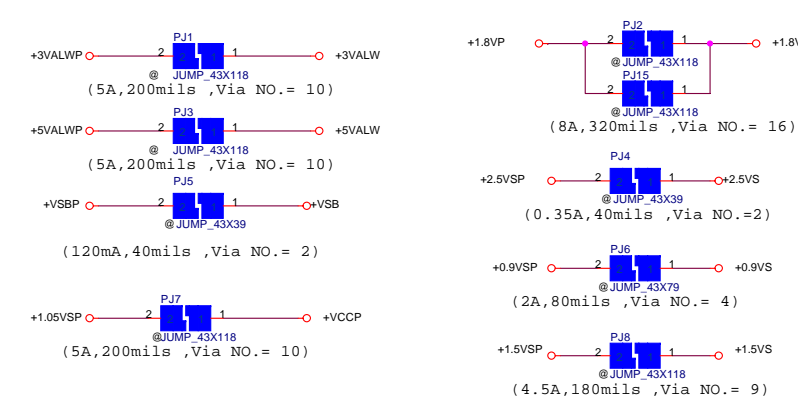


36,38 MAINPWON

37 ACON

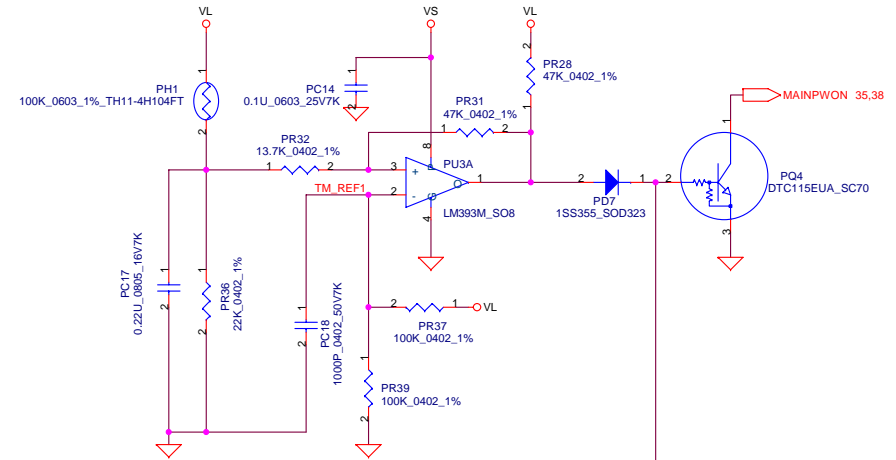
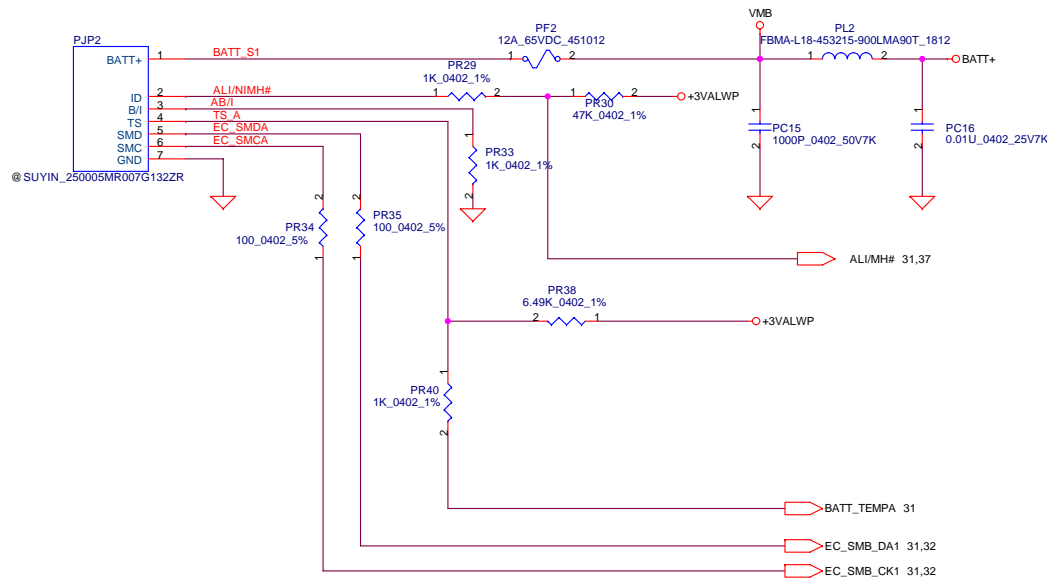
Precharge detector

15.97V/14.84V FOR ADAPTOR



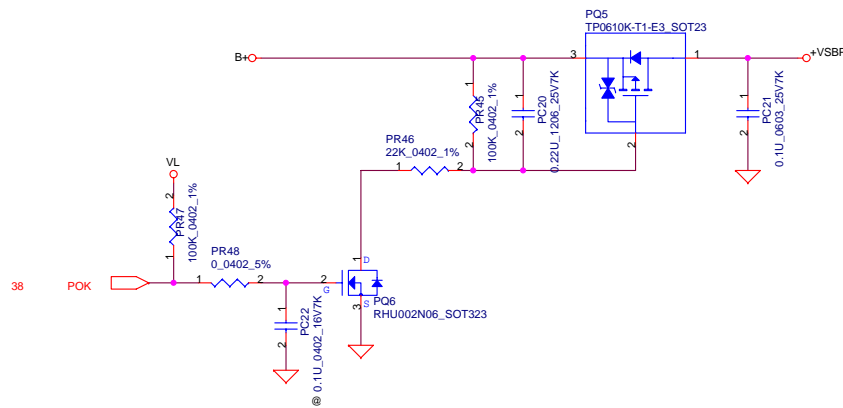
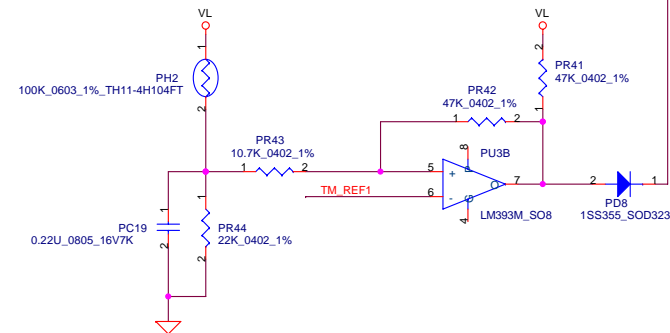
PH1 under CPU bottom side :

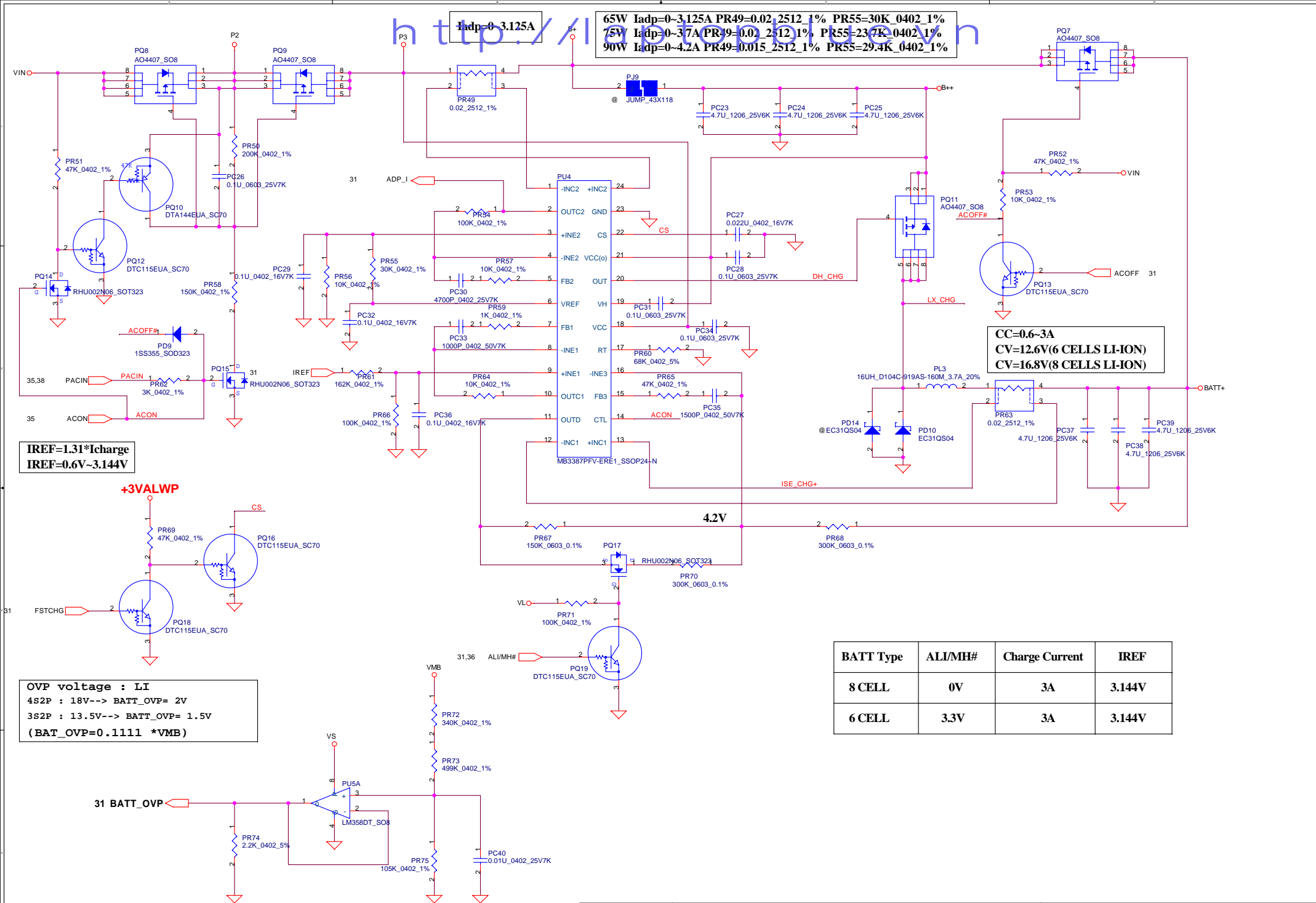
CPU thermal protection at 84 degree C
Recovery at 45 degree C

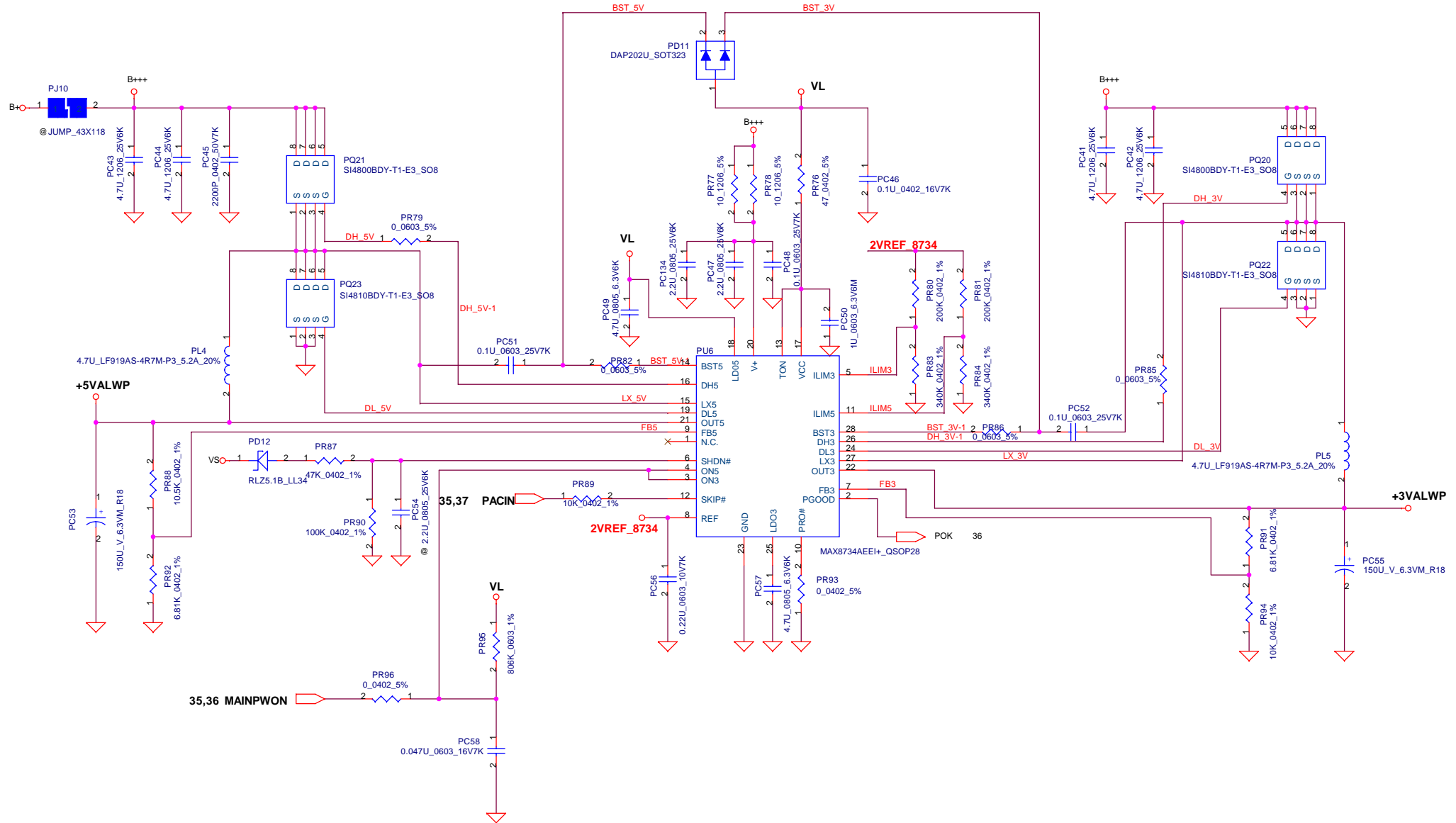


PH2 near main Battery CONN :

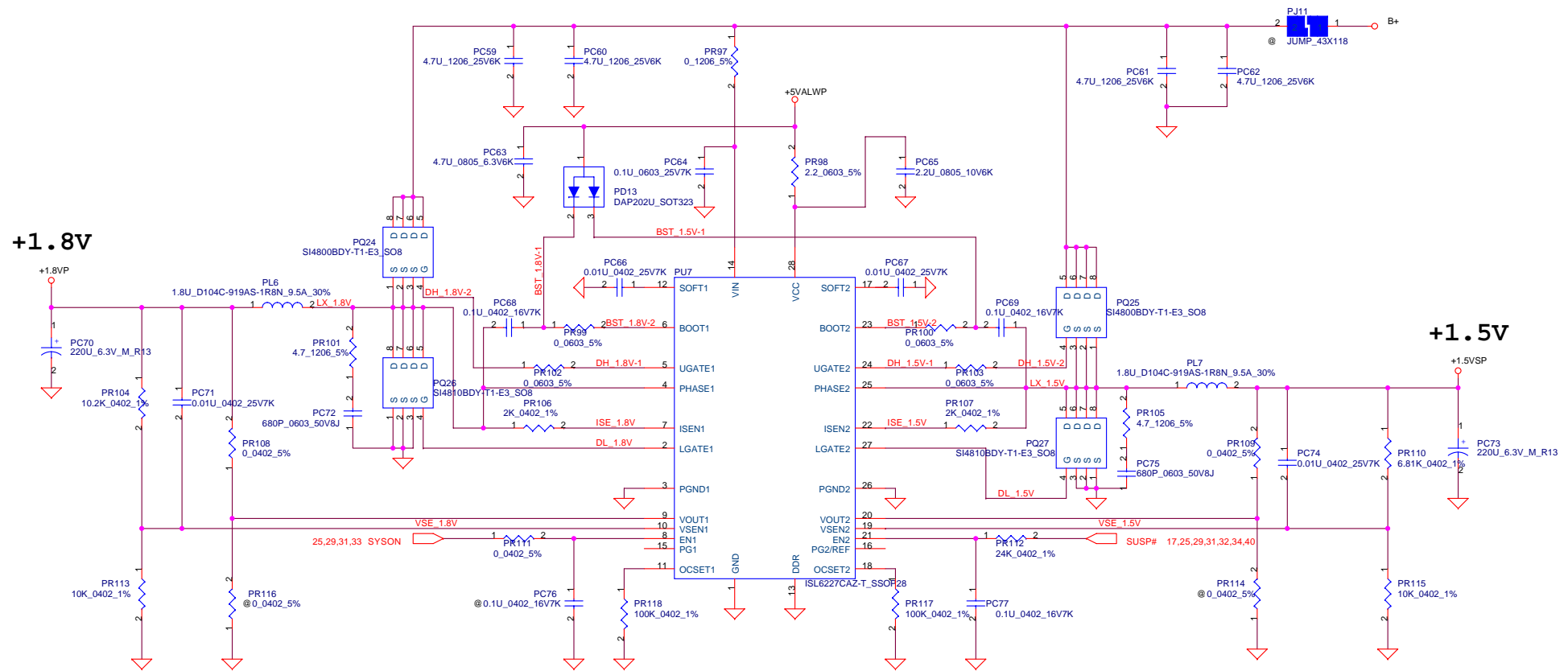
BAT. thermal protection at 79 degree C
Recovery at 45 degree C

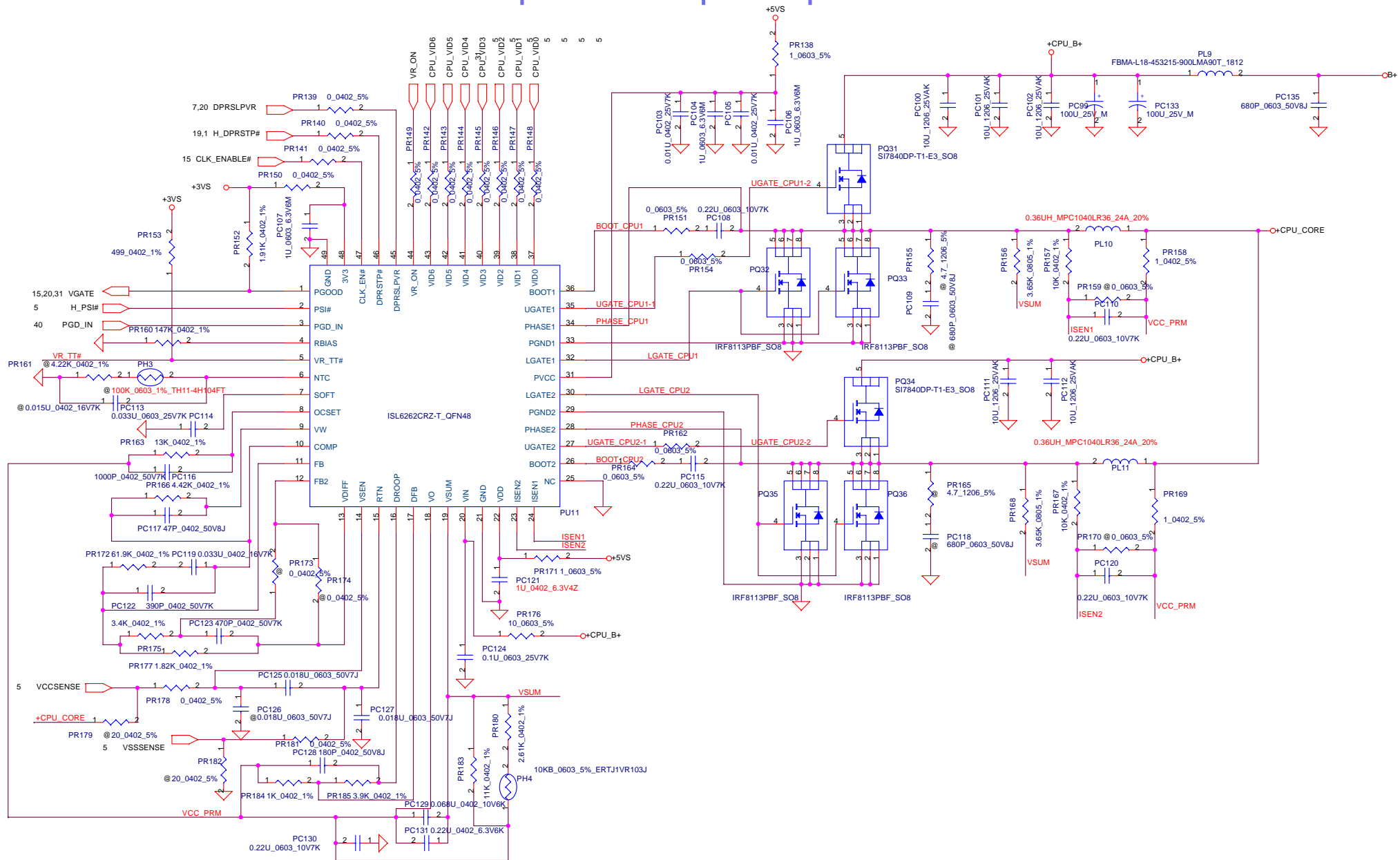






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POWER PIR LIST

page	Reason for change
EVT->DVT	
40	Add 680P at B+ for EMI
38	Change 1.5V sequence for HW
39	Change 2.5V sequence for HW
39	Change 2.5V sequence for HW
38	Adjust 3V/5V OCP to 8A
41	Adjust CPU loadlone

DVT->PVT	
40	Add snubber at 1.05V
41	Adjust switching frequence for intersil suggest
40	Adjust 1.05 OCP to 8A

Modify list
Add 680P_0402_25V at B+
Change PR112 from 22K_0402_1% to 24K_0402_1%
Unpop PR135,PC98 Pop PR186=11_K0402_1%, PQ37, PC132=0.1u_0402_16V
Change PR104 from 10K_0402_1% to 10.2K_0402_1%
Change PR80,PR81 to 200K_0402_1%, PR83,PR84 to 340K_0402_1% , PL4,PL5 to 4.7uH
Change PC119 to 33n_0402_16V, PR185 to 3.9K_0402_1%

Add 4.7_1206_5% and 680P_0603_50V at PR187,PC136
Change PC117 from 5600P to 47P_0402_50V
Change PR166 from 3.57K to 4.42K_0402_1%
Change PR127 from 11.5K to 8.25K_0402_1%

PROPRIETARY NOTE

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						PIR					
						Size		Document Number		Rev	
										1.0	
Date:						Tuesday, May 02, 2006		Sheet	42 of 44		

HW4 Product Improvement Record (P.I.R.)

Phase: A to B		Date: 2006/01/04			Writer: Lion Wang		
Page #	Action Plan (add; del; change)	Location or Net_List	Before value (Attached file)	After value (Attached file)	Detail Discretion and Root Cause	Rev.	DL/DM Check
22, 23	none	none			change TI8412 to ENE 714 for CB & 5in1 function	0.2	
24	none	none			change TI8412 to VIA6311S for 1394 function	0.2	
28	Add	C606,C607			Add for EMI request	0.2	
28	Add	L32			Add for EMI request	0.2	
31	Unmount	R171,R185			update after check ENE FAE	0.2	
31	Change	R365,R368 R187,R194	1K_5%_0402	10K_5%_0402	update after check ENE FAE	0.2	
31	Change	L33	Bead	0_5%_0603	update after check ENE FAE	0.2	
19	Change	JP22			change HDD CONN.	0.2	
31	Change	R142	0_5%_0402	8.2k_5%_0402	update BID from REV0.1 to REV0.2	0.2	
29					change U27,D38 ,D39 connect from GND to AGND	0.2	
26	Del	L33			LAN PCIE detect issue cause system boot black screen	0.2	
29	Change	SW4			Change VR to Rock Type switch	0.2	
29	Change	R514,R517,R516			Change AMP HP gain from -6 dB to 0 dB	0.2	
28	Add	Q44,R507,R498 C672,R499			Add for MIC Jack present function	0.2	
26	Change	R10,R11			change R10,R11 connect to U30 PIN7 & PIN10 to fix 10/100 Lan cannot connect issue	0.3	
20	Change				change ODD_RST# from GPIO 24 to GPIO34	0.3	
24	Change				delete R508~R511 and add L39 & L40 for EMI request	0.3	
						0.3	

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Size	Document Number			Rev	1.0
Date: Wednesday, May 03, 2006		Sheet		43	of 44

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	0327	29	REMOVE C680,R516,R518 REMOVE SW4 REMOVE CONNECTION OF VOL_UP,VOL_DOWN,VOL_MUTE,KSO17 ADD CONNECTION OF NBA_PLUG ON U39.13 ADD R529_3.9K_0402_5%,R530_100K_0402_5%,R531_4.3K_0402_5% R532_4.3K_0402_5%,Q62,Q63 RESERVE C698_0.1U_0402	MODIFY VOL_AMP FUNCTIONAL CIRCUIT ADD VR CIRCUIT
2	0327	28	RESERVE R533 CONNECT BETWEEN AMP_LEFT_HP & LEFT_HP RESERVE R534 CONNECT BETWEEN AMP_RIGHT_HP & RIGHT_HP	MODIFY EARPHONE GAIN CONTROL CIRCUIT
		29	ADD R535 CONNECT BETWEEN INTSPK_R1 & AMP_RIGHT_HP ADD R536 CONNECT BETWEEN INTSPK_L1 & AMP_LEFT_HP	
3	0327	28	ADD C699_100P_0402 ON +3VS_DVDD ADD C700_100P_0402 ON +AVDD_AC97 ADD C702_1U,C703_100P ON U38 PIN 16,17,18,19,20,23,24 ADD C704_100P_0402 ON MIC1_C_L ADD C705_100P_0402 ON MIC1_C_R ADD C706_100P_0402 ON MONO_IN ADD C707_100P_0402 ON ACZ_VREF ADD C708_100P_0402 ON ACZ_JDREF ADD C709_100P_0402 ON +MIC1_VREFO_R ADD C710_100P_0402 ON +MIC1_VREFO_L	FOR EMI PURPOSE

LAN

TRANSFORMER

PCB

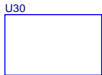
Card BUS

SB

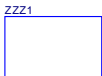
NB



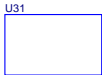
RTL8101E
100M@



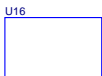
TST1284-LF
100M@



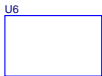
PCB ZKU LA-3171P REV0



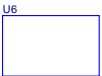
CB 1410
1410@



ICH7
ICH7R1@



945GM
GMR3@



945GM
GMR1@

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	0417	33	ADD R537 10_0402 AND C711 10P_0402 ON CLK_PCI_SIO2	PREVENT PCI CLOCK TRACE FLOATING
2	0419	16	CHANGE L26,L25 TO 39_0402 CHANGE C411,C413 TO RESERVED	BASE ON INTEL CRB SCHEMATIC TO DO MODIFICATION (CRB REV:1.601)
3	0419	29	CONNECT VR1.1,VR1.2 TO AGAD	BASE ESD TEST RESULT, CONNECT TO AGND TO PASS ESD TEST
4	0419	29	CHANGE L7,L8,L9,L10 TO BEAD 39OHM@100MHZ CHANGE C395,C399 TO 10P_0402	TO SOLVE 3G NOISE ISSUE
		28	CHANGE C388,C389 TO 10P_0402	
4	0426	06	Add C122,C537 to 330UF	TO SOLVE ESD ISSUE