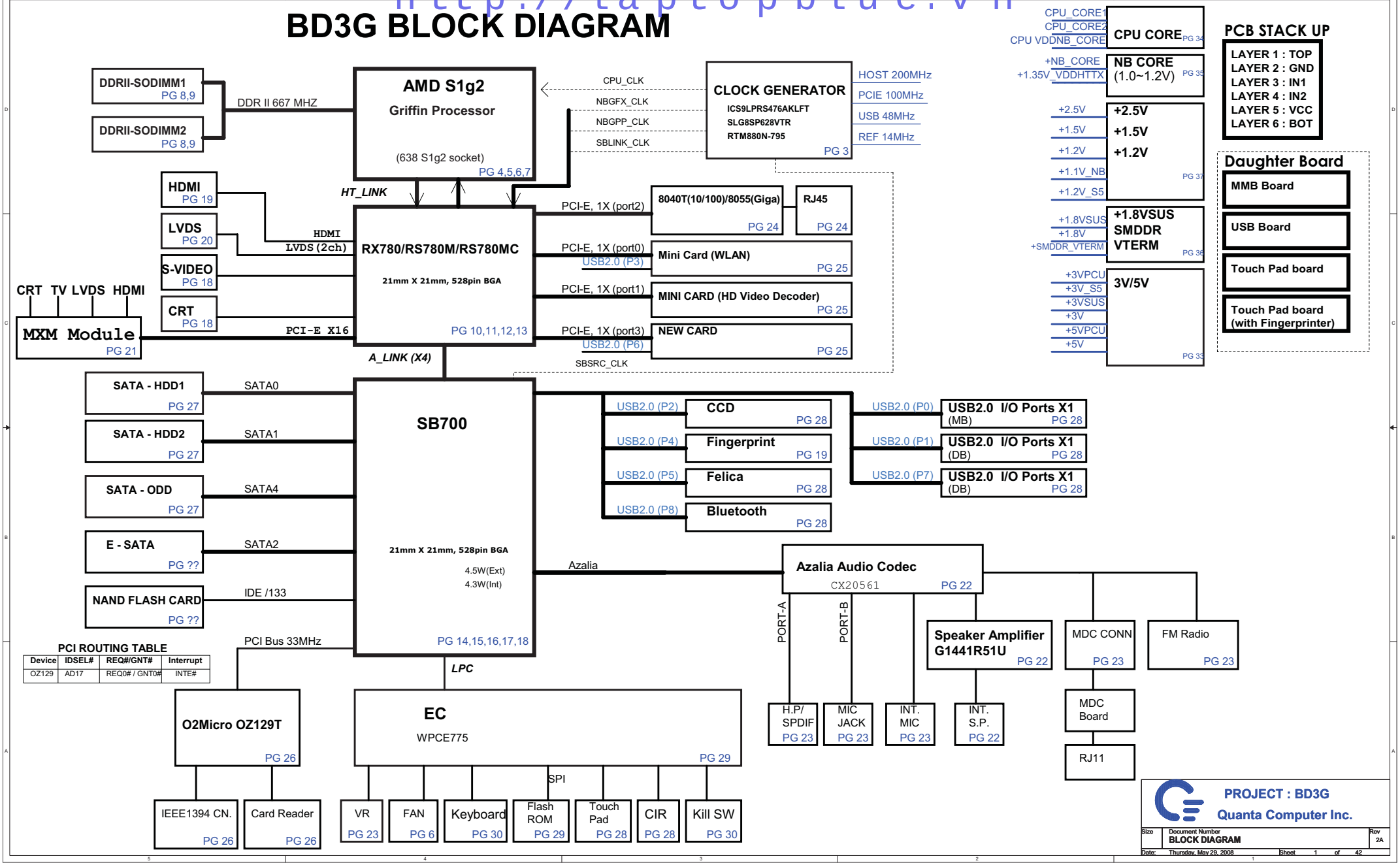
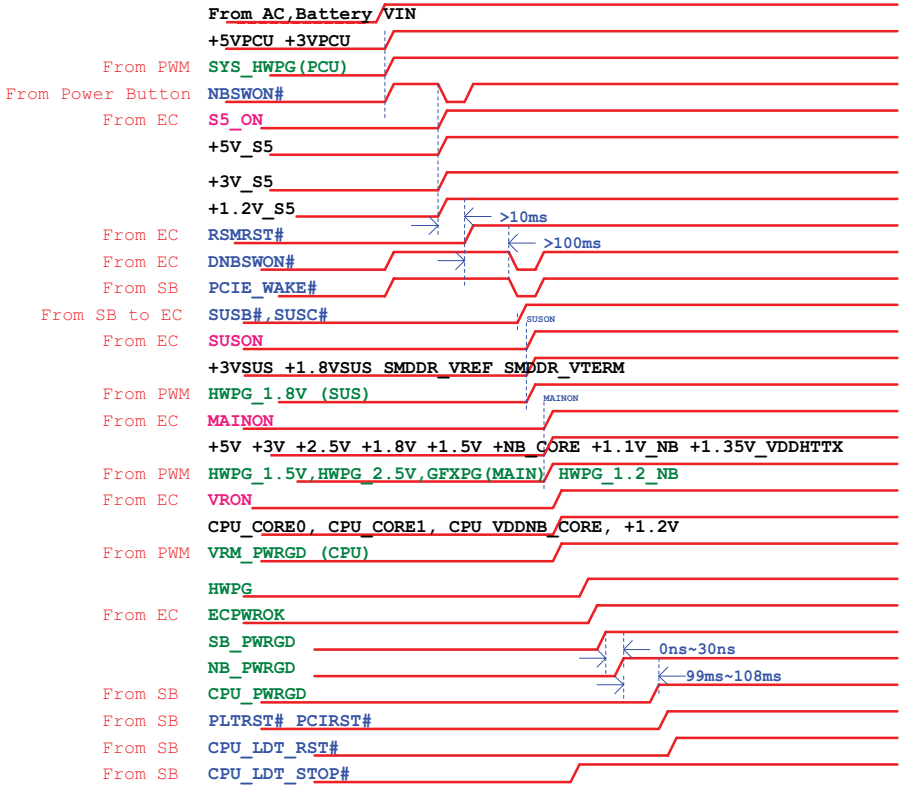
BD3G BLOCK DIAGRAM



BD3G Power On Sequence



BOM naming rule

Items	Function	BTO	Name	Description
1	CIR	v	CIR@	
2	HDMI port	v	HDM@	
3	HDMI transmitter	v	SI@	Silicon image SiI 1392/1932
4	HDMI-CEC	v	CEC@	Renesas R8C/1B
5	Discrete VGA		EV@	External VGA stuff
6	UMA		IV@	Internal VGA stuff
7	New Card		NEW@	
8	RJ11	v	MD@	Modem
9	RJ45-10/100		40@	Marvell 8040T(10/100)
10	RJ45-1000		55@	Marvell 8055(Giga)
11	Option for RJ45-10/100 and RJ45-1000		40@55@	Option for 8040/8055
12	TV	v	TV@	
13	Cardbus		CB@	
14	FM transmitter	v	FM@	
15	Mainstream ID LED		MID@	
16	Low cost ID LED		LID@	
17	CCD	v	CCD@	
18	INT MIC	v	I_MIC@	
19	AMD Hyper Flash		HF@	Only for AMD platform
20	North bridge(690MC/RS780MC)		MC@	Only for AMD platform
21	North bridge(RX780)		RX@	Only for AMD platform
22	PowerXpress		PX@	Only for AMD platform
23	PowerXpress with UMA SKU		PX@IV@	Only for AMD platform
24	PowerXpress with Discrete VGA SKU		PX@EV@	Only for AMD platform
25	Power player/Power Shift		PP@	Only for AMD platform

*Note: EC will sampling SUSB# & SUSC# every 5ms.

AMD SB700 SMBUS Table

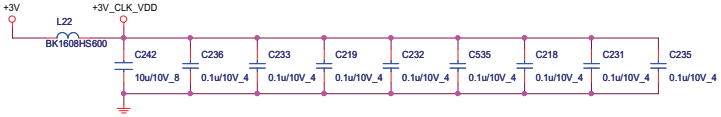
	CLK GEN	RAM	Mini Card (HD-Decoder)	Mini-card(WL)	New Card	HDMI
SB700 SDATA0/SCLK0(+3V)	V	V	V	V	V	
SB700 SDATA1/SCLK1(+3V_S5)						V
SB700 SDATA2/SCLK2(+3V_S5)						
Power	+3V	+3V	+3V	+3V (Atheros)	+3V	+3V_S5
Reserve MOS ckt	V	V	V	V	V	V

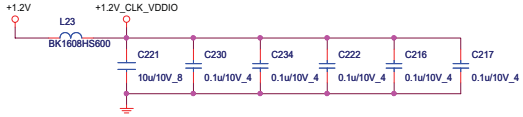
EC SMBUS Table

	Battery	CPU thermal Sensor	EC EEPROM	VGA thermal Sensor	Touch Sensor	HDMI CEC
EC775 SDATA1/SCLK1(+3VPCU)	V					
EC775 SDATA2/SCLK2(+3VPCU)		V	V			
EC775 SDATA3/SCLK3(+3VPCU)				V	V	V
EC775 SDATA4/SCLK4(+3VPCU)						
Power	+3VPCU	+3V	+3VPCU	+3V	+3VPCU	+5VPCU
Reserve MOS ckt	X	V	X	V	X	V

PROJECT : BD3G
Quanta Computer Inc.
Size | Document Number: SYSTEM INFORMATION | Rev 2A
Date: Thursday, May 29, 2008 | Sheet 2 of 42

CLK_GEN_SLG8SP628





ICS9LPRS480 P/N : ALPRS480000

SLG8SP628 P/N : AL8SP628000

RTM880N-796 P/N : AL000880000

Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.

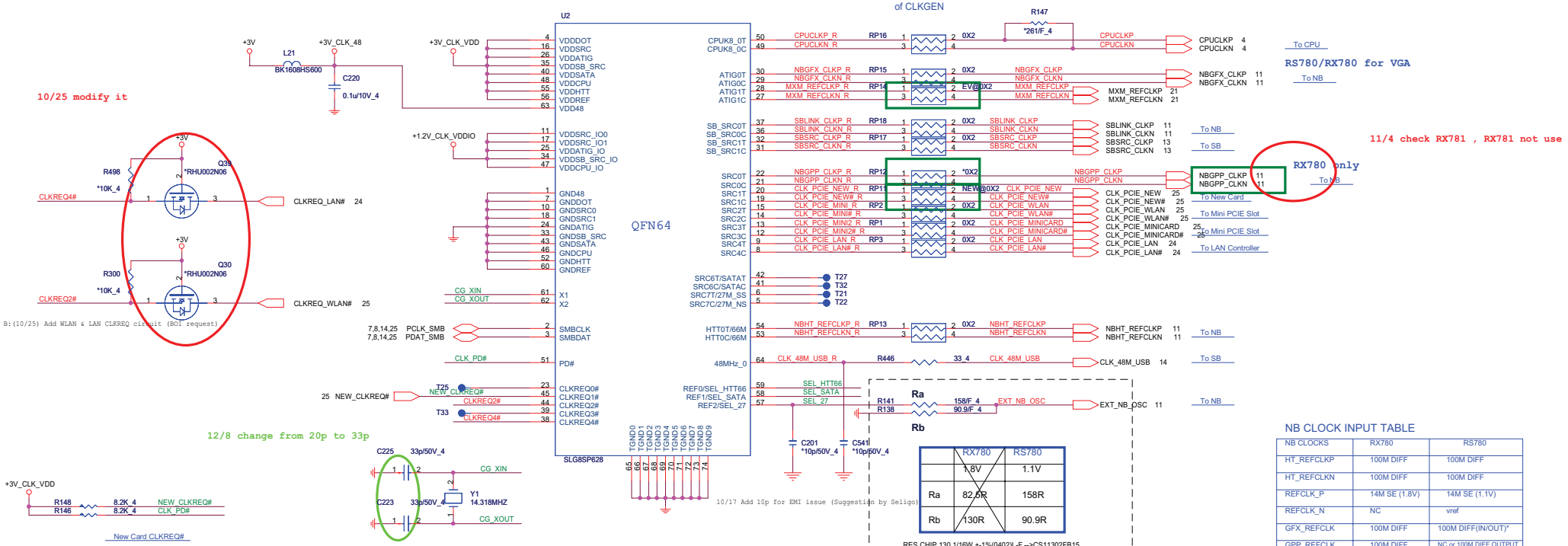
Place within 0.5" of CLKGEN

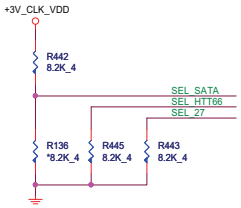
10/25 modify it

11/4 check RX781 , RX781 not use

RX780 only

12/8 change from 20p to 33p





CLOCKS name	RX780	RS780	Clock pin function
NBGFX_CLKP NBGFX_CLKN	RP1001 STUFF	RP1001 STUFF	to NB for VGA reference clock
MXM_REFCLKP MXM_REFCLKN	RP66 STUFF	RP66 NC	to M82-S external reference clock -RX780 only
NBGPP_CLKP NBGPP_CLKN	RP1005 STUFF	RP1005 NC	to NB for RX780 for PCIEX2 interface reference clock only RS780 is internal share with AC-LINK clock,RS780 not need
SBLINK_CLKP SBLINK_CLKN	RP1003 STUFF	RP1003 STUFF	to NB for AC-LINK reference clock

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27	1	27MHz and 27M SS outputs
	0*	100 MHz SRC clock

* default

	RX780	RS780
	1.8V	1.1V
Ra	82.5R	158R
Rb	130R	90.9R

RES CHIP 130 1/16W +-1%(0402)L-F -->CS11302FB15
RES CHIP 158 1/16W +-1%(0402) -->CS11582FB00
RES CHIP 90.9 1/16W +-1%(0402) -->CS09092FB15
RES CHIP 82.5 1/16W +-1%(0402) -->CS08252FB11

NB CLOCK INPUT TABLE

NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

PROJECT : BD3G

Quanta Computer Inc.

Size	Document Number	Rev
	CLOCK GENERATOR_SLG8SP628	1A

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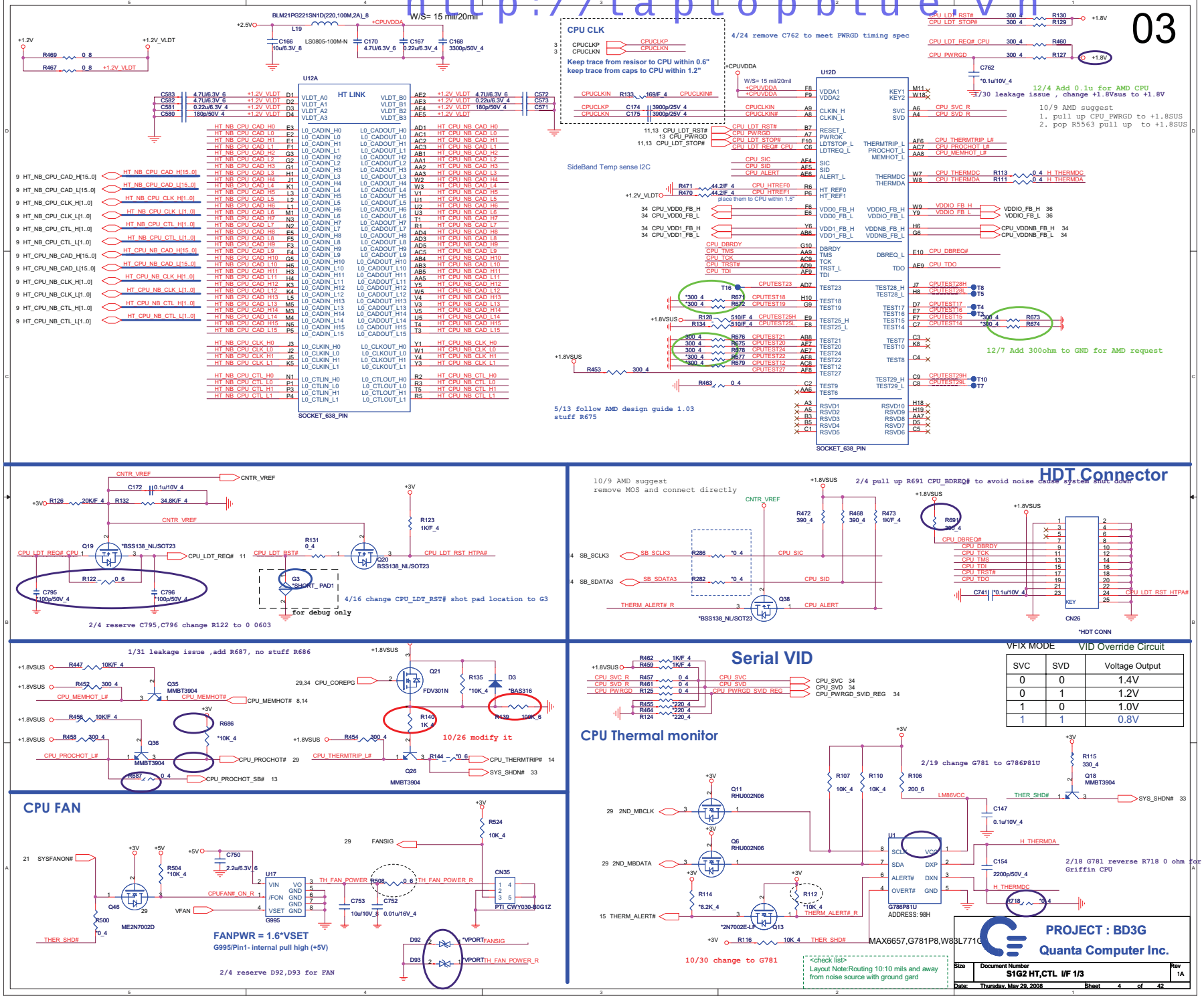

Processor Memory Interface

04

PLACE THEM CLOSE TO CPU WITHIN 1"

750 mA

11/05 change to RC0402-C

Place close to socket

Close to CPU within 1500 mils

U12B

SOCKET_638_PIN

U12C

MEM:DATA

SOCKET_638_PIN

PROJECT : BD3G

Quanta Computer Inc.

Size	Document Number	Rev
	S1G2 DDRII MEMORY I/F 2/3	1A
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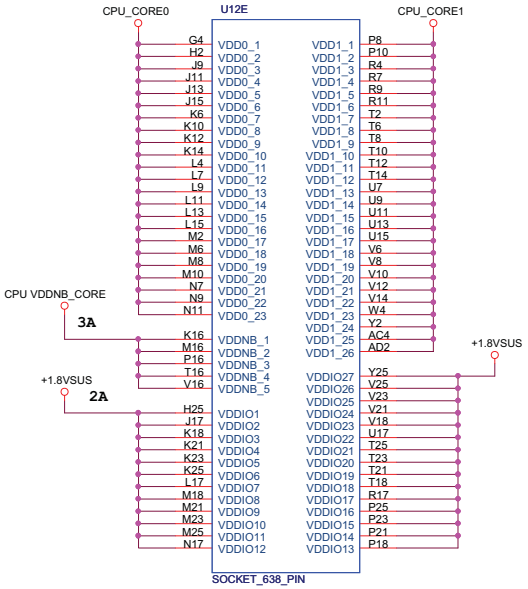
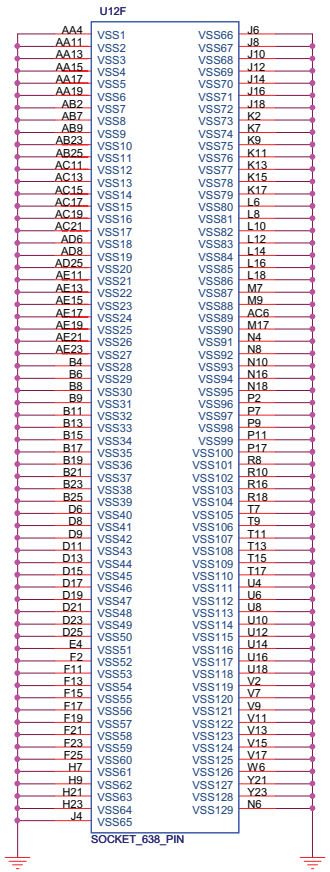
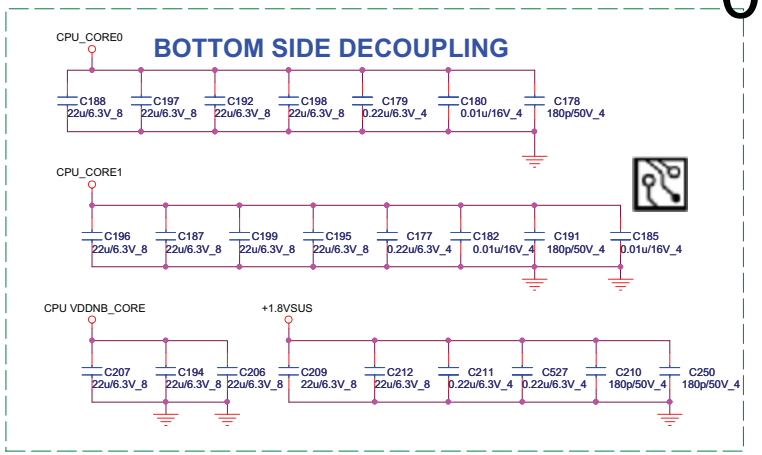
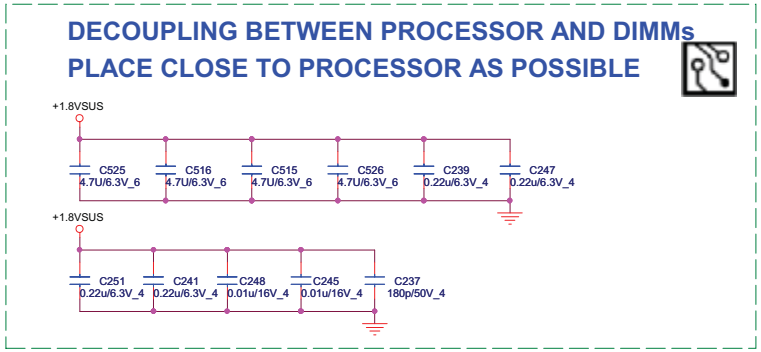






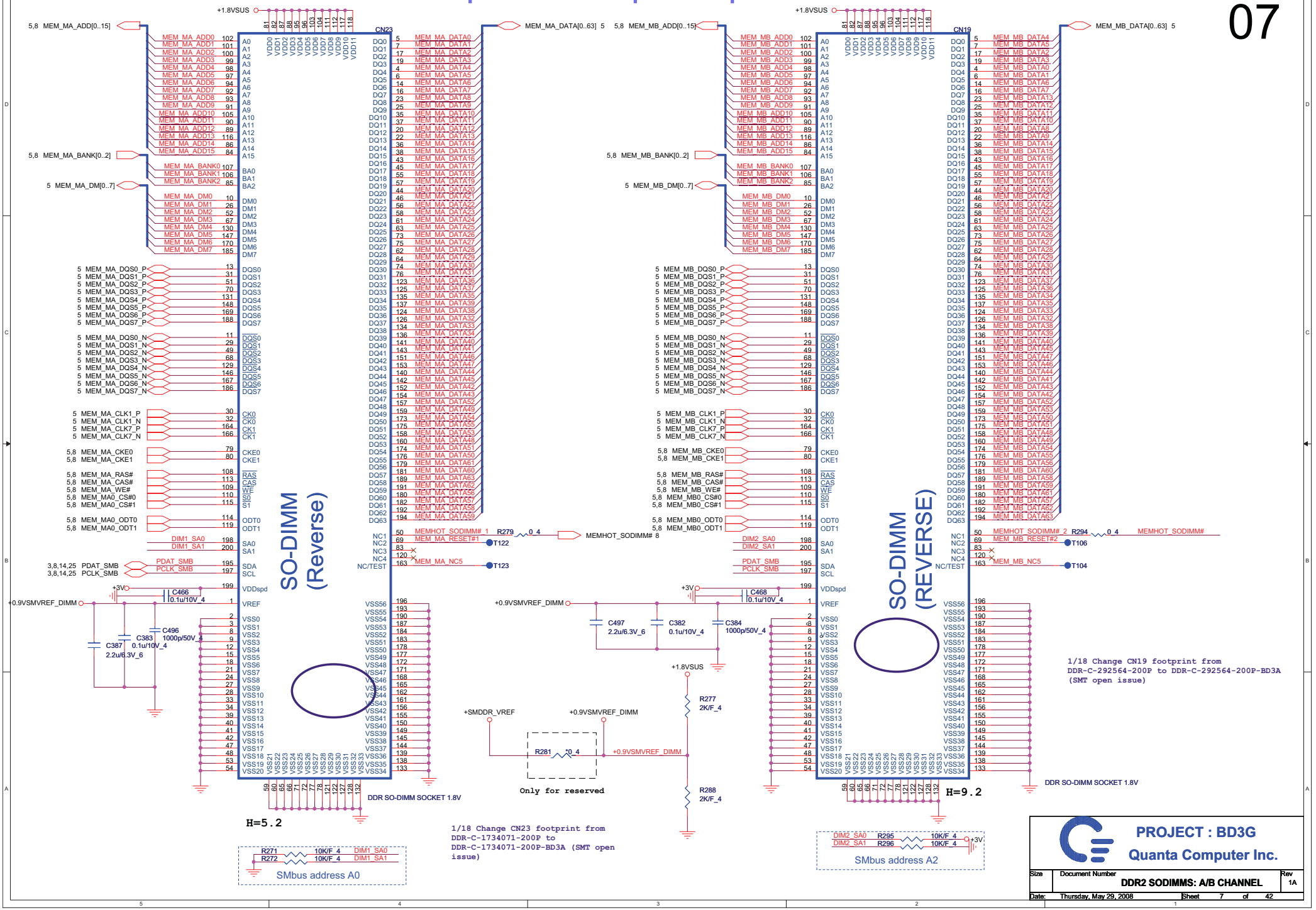


PROCESSOR POWER AND GROUND

PROJECT : BD3G

Quanta Computer Inc.

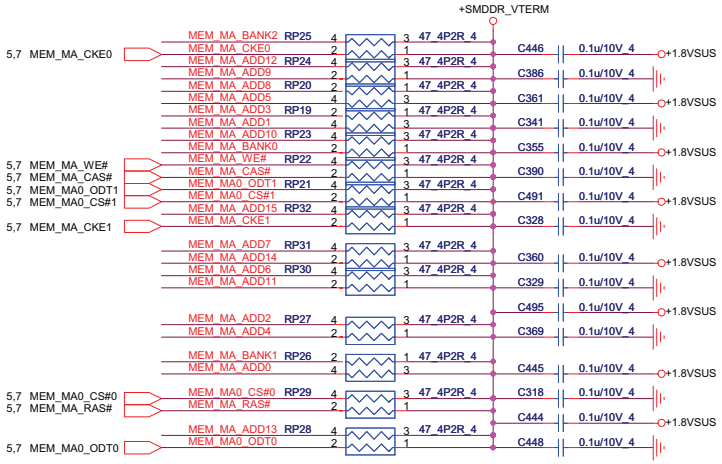
Size	Document Number	Rev
	S1G2 PWR & GND 3/3	1A
Date: Thursday, May 29, 2008	Sheet 6 of 42	

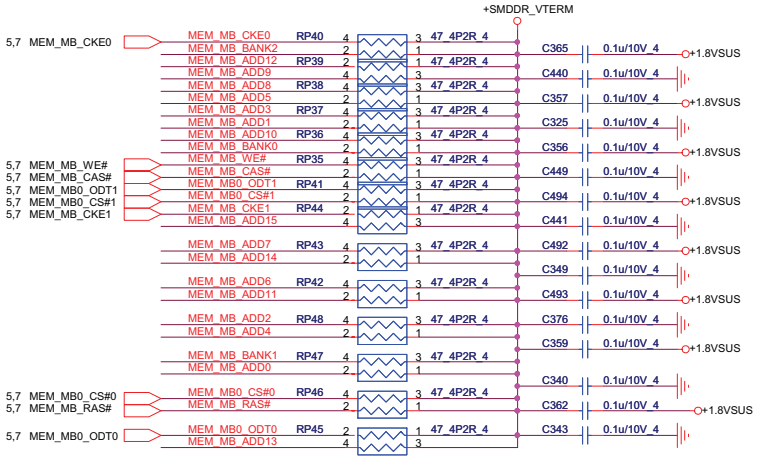


PROJECT : BD3G		
Quanta Computer Inc.		
Size	Document Number	Rev
	DDR2 SODIMMS: A/B CHANNEL	1A
Date: Thursday, May 29, 2008	Sheet 7 of 42	

5,7 MEM_MA_ADD[0..15] MEM_MA_ADD[0..15]
5,7 MEM_MA_BANK[0..2] MEM_MA_BANK[0..2]

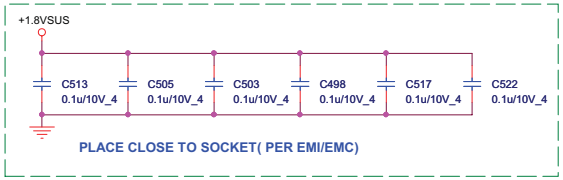
5,7 MEM_MB_ADD[0..15] MEM_MB_ADD[0..15]
5,7 MEM_MB_BANK[0..2] MEM_MB_BANK[0..2]

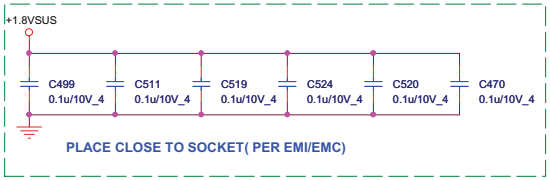


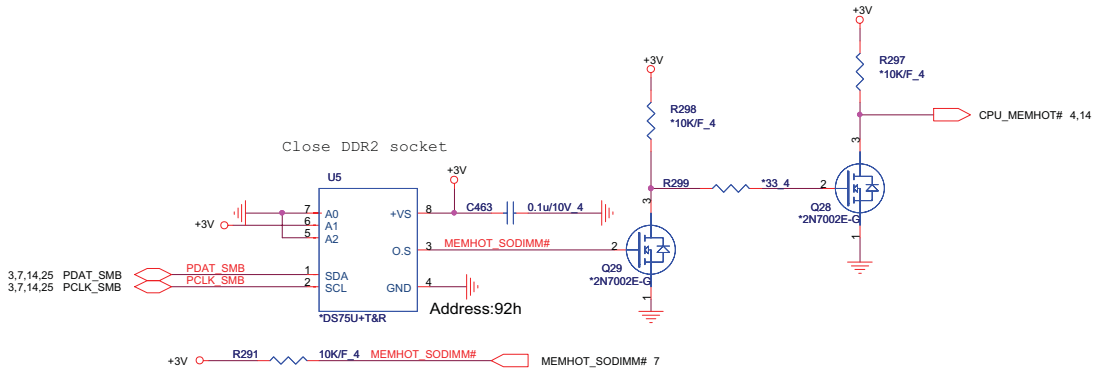


PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH

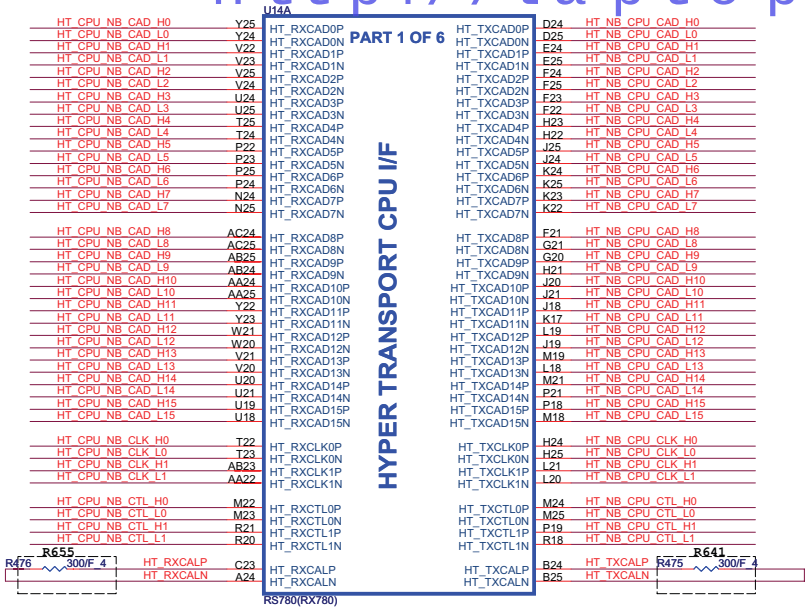
PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH

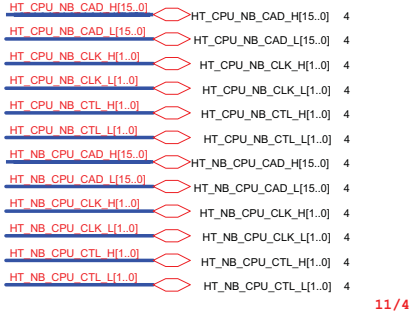






PROJECT : BD3G		
Quanta Computer Inc.		
Size	Document Number	Rev
	DDR2 SODIMMS TERMINATIONS	1A
Date: Thursday, May 29, 2008	Sheet 8 of 42	





11/4 modify

signals	RS780	RX780
HT_TXCALP	R641 300 ohm 1%	R641 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R655 300 ohm 1%	R655 1.21k ohm 1%
HT_RXCALN		

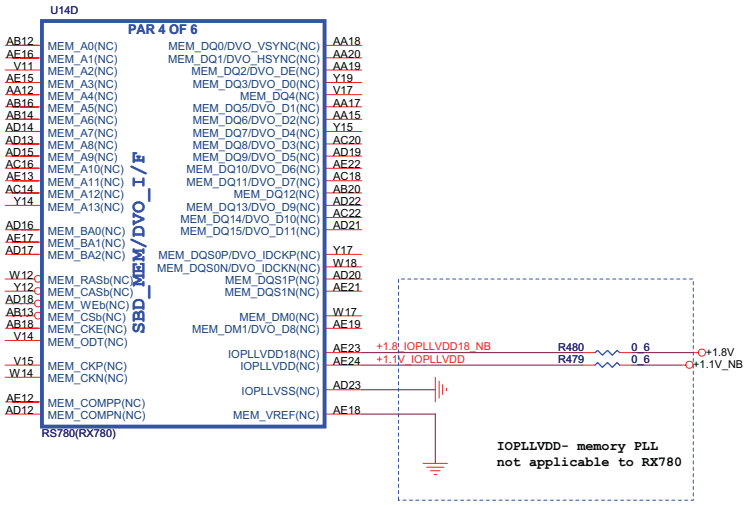
RES CHIP 1.21K 1/16W +-1%(0402)
P/N : CS21212FB18

RES CHIP 300 1/16W +-1%(0402)
P/N : CS13002FB00

A12 version
RS780M AJ067400T05 100-CK2612(216-0674008-00)
RS780MC AJ067400T06 100-CK2613(216-0674010-00)
RX781 AJ067400T10 100-CK2642(215-0674024)
SB700 AJA12FG0T18 100-CK2614(218S7EALA12FG)

A13 version
RS780M AJ067400T18 100-CK2699(216-0674022)
RS780MC AJ067400T20 100-CK2704(216-0674024)
RX781 AJ067400T21 100-CK2706(215-0674034)
A12 version
SB700 AJA12FG0T18

This block is for UMA RS780 only , RX780 can remove all component

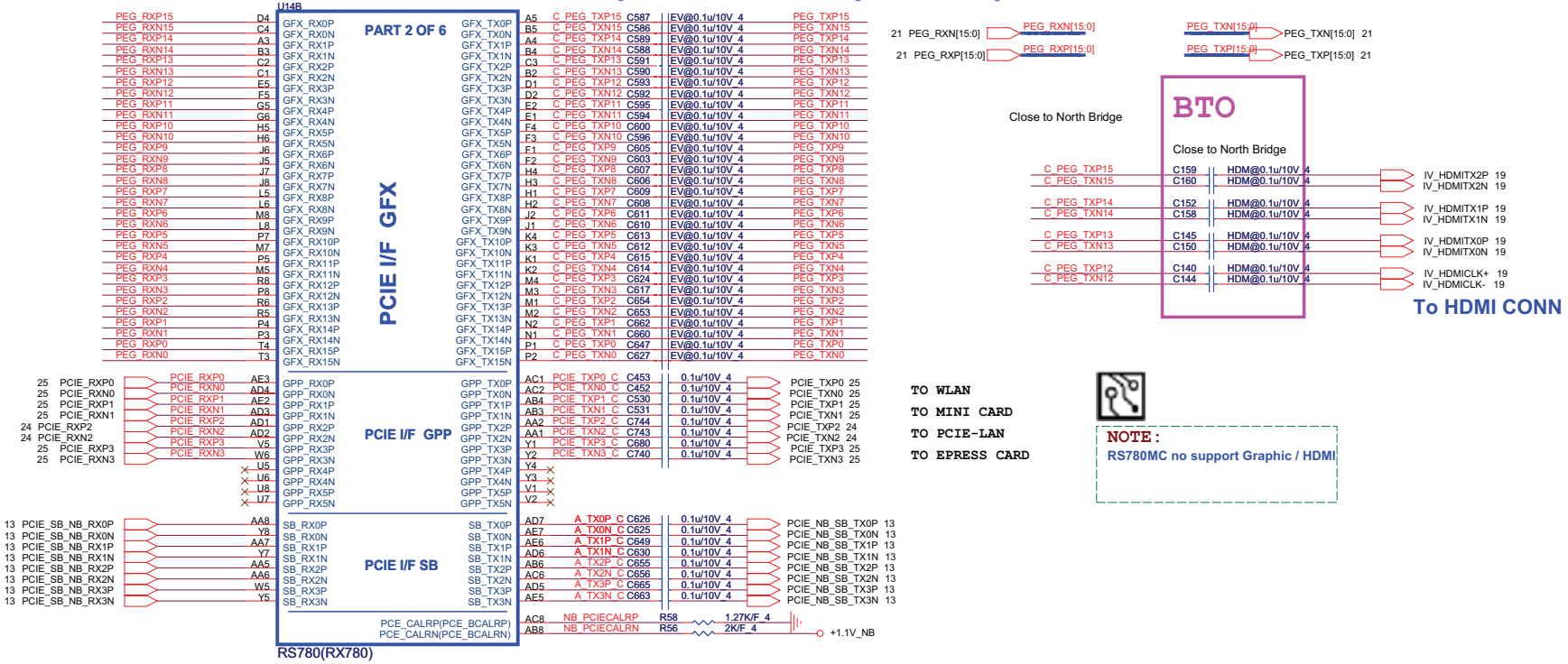


2/1 R480,R479 no stuff when RS780M without side port / RX781

4/24 stuff R480,R479

PROJECT : BD3G
Quanta Computer Inc.

Size	Document Number	Rev
	RS740/RS780-HT LINK I/F 1/5	1A
Date: Thursday, May 29, 2008	Sheet 9 of 42	



21 PEG_RXN[15:0] PEG_RXN[15:0]
21 PEG_RXP[15:0] PEG_RXP[15:0]
PEG_TXN[15:0] PEG_TXN[15:0] 21
PEG_TXP[15:0] PEG_TXP[15:0] 21

Close to North Bridge

BTO

Close to North Bridge

To HDMI CONN

TO WLAN
TO MINI CARD
TO PCIE-LAN
TO EPRESS CARD

NOTE :
RS780MC no support Graphic / HDMI

11/4 modify

RX780/RS740/RS780 difference table (PCIE LINK)

	RS740	RX780/RS780
NB_PCIECALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

PROJECT : BD3G
Quanta Computer Inc.

Size	Document Number	Rev
	RS740/RS780-PCIE I/F 2/5	1A
Date: Thursday, May 29, 2008	Sheet 10 of 42	

RX780: Powered from the 1.8-V rail and driven by SB600 LDT_RST#, or SB700 LDT_RST# or A_RST#.
RS780: Powered from the 3.3-V rail and driven by SB600 LDT_RST#, or SB700 LDT_RST# or A_RST#.

10/26 change to 4 pin S-video conn , no need TV_comp

2/1 follow A13 request change
R103 from 150 to 140 CS11402FB19

RX780 / RS780 — North Bridge RESET

11/4 stuff R5160 for RS780M/MC/RX781

RX780 — 10/9 add 2K pull up to DDCDAT /DDCCLK for RX780

11/4 no stuff for RS780M/MC/RX781

12/22 stuff R48 2.2K for power play

selects Loading of straps from EPROM
1 : use default vaule , default
0 : I2C Master can load strap values from EEPROM
if connected, or use default values if not connected
RX780 --RS780_AUX_CAL
RS780 -- SUS_ATAT

RX780

Enables Debug Bus acess through memory T/O pads and GPIO.
1 : Enable RX780 , Default
0 : Disable RX780

RX780 — Reserved only

12/22 stuff R65

Enables Debug Bus acess through memory T/O pads and GPIO.
1 : Enable RS780 , Default
0 : Disable RS780
(RS780 use VSYNC#)

RS780

Indicates if memory Side port is available or not
0: available RS780 , Default
1: Not available RS780
(RS780 use HSYNC#)

RS780

10/19 RS780M Databook rev 1.01 define High disable

U140 — RS780(RX780) — PART 3 OF 6

CRT/TVOUT: AVDD1(NC), AVDD2(NC), AVDDDI(NC), AVSSDI(NC), AVDDQ(NC), AVSSQ(NC), C_Pr(DFT_GPIO5), Y(DFT_GPIO2), COMP_Pb(DFT_GPIO4), RED(DFT_GPIO0), REDb(NC), GREEN(DFT_GPIO1), GREENb(NC), BLUE(DFT_GPIO3), BLUEb(NC), DAC_HSYNC(PWM_GPIO4), DAC_VSYNC(PWM_GPIO6), DAC_SDA(PCE_TCALRN), DAC_SCL(PCE_RCALRN), DAC_RSET(PWM_GPIO1)

PLL PWR: PLLVDD(NC), PLLVDD18(NC), PLLVSS(NC), VDDA18HTPLL, VDDA18PCIEPLL1, VDDA18PCIEPLL2

PM: SYSRESETb, POWERGOOD, LDTSTOPb, ALLOW_LDTSTOP

CLOCKs: HT_REFCLKP, HT_REFCLKN, REFCLK_P/OSCIN(OSCIN), REFCLK_N(PWM_GPIO3), GFX_REFCLKP I/O, GFX_REFCLKN I/O, GPP_REFCLKP I/O, GPP_REFCLKN I/O, GPPSB_REFCLKP(SB_REFCLKP), GPPSB_REFCLKN(SB_REFCLKN)

MIS.: I2C_DATA, I2C_CLK, DDC_DATA/AUX0N(NC), DDC_CLK/AUX0P(NC), AUX1P(NC), AUX1N(NC), STRP_DATA, RSVD, AUX_CAL(NC), TMDS_HPD(NC), HPD(NC), TVCLKIN(PWM_GPIO5), THERMALDIODE_P, THERMALDIODE_N, TESTMODE

LVTM: TXOUT_L0P(NC) … TXOUT_L3N(NC), TXOUT_U0P(NC) … TXOUT_U3N(NC), TXCLK_LP(DBG_GPIO1), TXCLK_LN(DBG_GPIO3), TXCLK_UP(PCIE_RESET_GPIO4), TXCLK_UN(PCIE_RESET_GPIO1), VDDLT18P(NC), VSSLT18P(NC), VDDLT18_1(NC), VDDLT18_2(NC), VDDLT33_1(NC), VDDLT33_2(NC), VSSLT1(VSS) … VSSLT7(VSS), LVDS_DIGON(PCE_TCALRP), LVDS_BLON(PCE_RCALRP), LVDS_ENA_BL(PWM_GPIO2)

11/01 exchange LVDS_PWM /LVDS_BLON

For RX780 only

1/17 RX781 connect to GND
C104,C110,C646,C98,C136,C103,C118 change to CS00003J951

AVDD-DAC Analog not applicable to RX780

PLLVDD - Graphics PLL not applicable to RX780

PLLVDD18 - Graphics PLL not applicable to RX780

AVDDI-DAC Digital not applicable to RX780

AVDDQ-DAC Bandgap Reference not applicable to RX780

VDDLTP18 - LVDS or DVI/HDMI PLL not applicable to RX780

1/17 RX781 no stuff them
L2,L12,C124,L52,R76,L17,L51,L10,C115

VDDLT18 - LVDS or DVI/HDMI digital not applicable to RX780

1/31 voltage leakage issue
remove Q5,Q3,R83,R80,R97
stuff R88,R77

VDDA18PCIEPLL -PCIE PLL

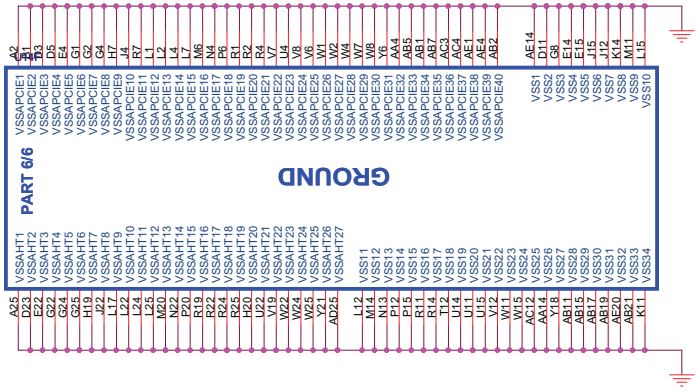
VDDA18HTPLL -HT LINK PLL

RX780 / RS780

VDDLT33 - LVDS or DVI/HDMI ANALOG RS740 only

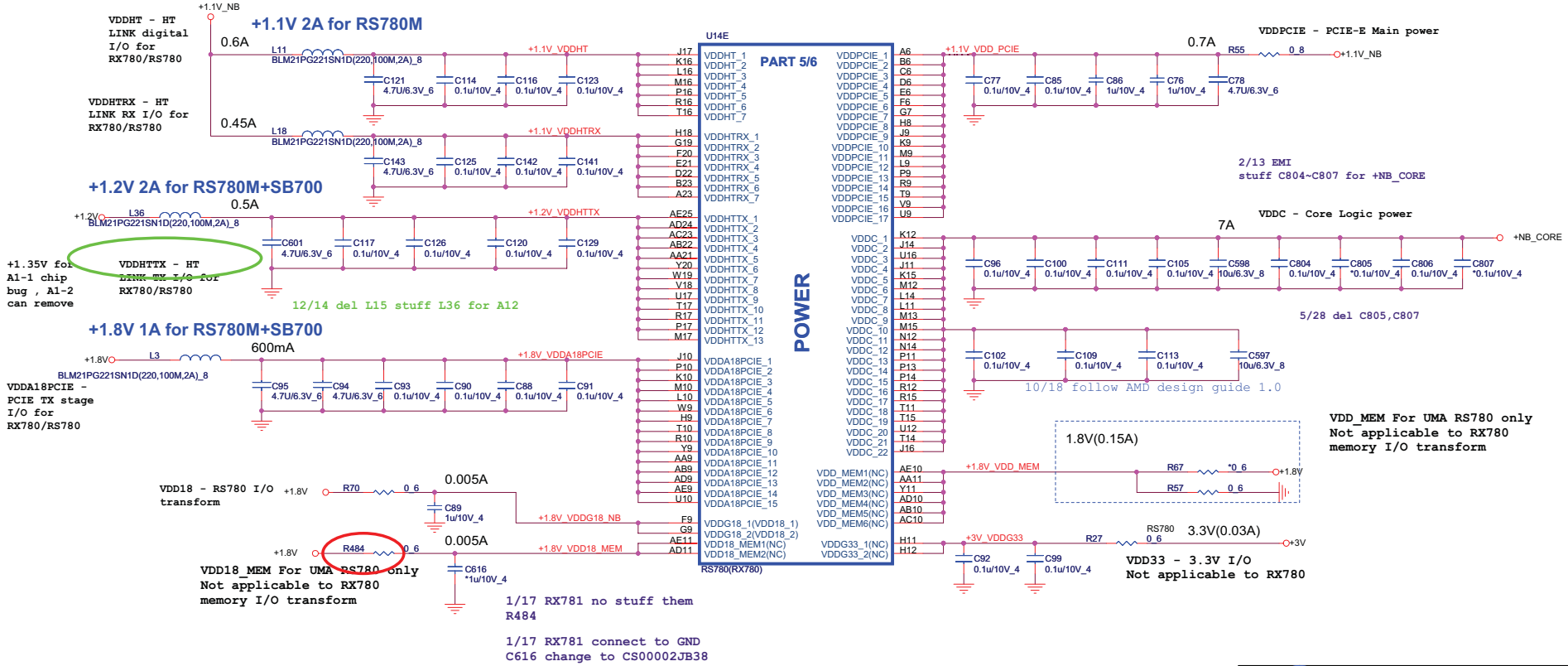
PROJECT : BD3G
Quanta Computer Inc.

Size	Document Number	Rev
	RS740/RS780-SYSTEM I/F 3/5	1A
Date: Thursday, May 29, 2008	Sheet 11 of 42	



RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVDD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVDD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVDD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDLT18	NC	+1.8V
IOPLLVDD18	NC	+1.8V	VDDLT33	NC	NC



PROJECT : BD3G			
Quanta Computer Inc.			
Size	Document Number		Rev
	RS740/RS780-POWER5/5		1A
Date: Thursday, May 29, 2008		Sheet 12 of 42	

2/4 reserve C800 PLTRST#

C800 *.1U_4

11 NB_PLTRST#
19,21,24,25,27,29 PLTRST#

R160 33_4
R165 33_4

PLACE THESE PCIE AC COUPLING CAPS CLOSE TO U600

To RS780

SB700
Part 1 of 5

U6A

A_RST# N2

PCI CLKS

PCICLK0 P4 PCI_CLK0_R R396 22_4 PCLK_OZ129 26
PCICLK1 P3 PCI_CLK2_R R369 22_4 T58 PCI_CLK2 17
PCICLK2 P1 PCI_CLK3_R R394 22_4 PCI_CLK3 17
PCICLK3 P2 PCI_CLK4_R R424 22_4 PCI_CLK4 17
PCICLK4 T4 PCI_CLK5_R R408 22_4 PCI_CLK5 17
PCICLK5/GPIO41 T3

A11 default PCICLK5
A12 default GPIO41

+3V
PE_GPIO1 R209 8.2K_4
R212 *8.2K_4
SB_GPIO65 R202 100K/F_4
Maybe can remove

PCIRST# N1 PCIRST# L R367 33_4 PCIRST# PCIRST# 25,26

All the PCI bus has build-in Pull-UP/Down resistors

AD[0..31] 17,26

10 PCIE_SB_NB_RX0P C509 0.1u/10V_4 A_RX0P_C V23 PCIE_TX0P
10 PCIE_SB_NB_RX0N C512 0.1u/10V_4 A_RX0N_C V22 PCIE_TX0N
10 PCIE_SB_NB_RX1P C510 0.1u/10V_4 A_RX1P_C V24 PCIE_TX1P
10 PCIE_SB_NB_RX1N C508 0.1u/10V_4 A_RX1N_C V25 PCIE_TX1N
10 PCIE_SB_NB_RX2P C502 0.1u/10V_4 A_RX2P_C U25 PCIE_TX2P
10 PCIE_SB_NB_RX2N C507 0.1u/10V_4 A_RX2N_C U24 PCIE_TX2N
10 PCIE_SB_NB_RX3P C500 0.1u/10V_4 A_RX3P_C T23 PCIE_TX3P
10 PCIE_SB_NB_RX3N C504 0.1u/10V_4 A_RX3N_C T22 PCIE_TX3N

10 PCIE_NB_SB_TX0P U22 PCIE_RX0P
10 PCIE_NB_SB_TX0N U21 PCIE_RX0N
10 PCIE_NB_SB_TX1P U19 PCIE_RX1P
10 PCIE_NB_SB_TX1N V19 PCIE_RX1N
10 PCIE_NB_SB_TX2P R20 PCIE_RX2P
10 PCIE_NB_SB_TX2N R21 PCIE_RX2N
10 PCIE_NB_SB_TX3P R18 PCIE_RX3P
10 PCIE_NB_SB_TX3N R17 PCIE_RX3N

PCI EXPRESS INTERFACE

+1.2V_PCIE_VDDR
R363 562/F_4 PCIE_CALRP_SB T25 PCIE_CALRP
R360 2.05K/F_4 PCIE_CALRN_SB T24 PCIE_CALRN

+1.2V L27 BLM18PG221SN1D(220,1.4A)_6 +1.2V_PCIE_PVDD P24 PCIE_PVDD
40mA
P25 PCIE_PVSS

PCIE_PVDD-- PCIE PLL POWER

C321 10u/6.3V_8
C322 1u/10V_4

AD0 U2 AD0
AD1 P7 AD1
AD2 V4 AD2
AD3 T1 AD3
AD4 V3 AD4
AD5 U1 AD5
AD6 V1 AD6
AD7 V2 AD7
AD8 T2 AD8
AD9 W1 AD9
AD10 T9 AD10
AD11 R6 AD11
AD12 R7 AD12
AD13 R5 AD13
AD14 U8 AD14
AD15 U5 AD15
AD16 Y7 AD16
AD17 W8 AD17
AD18 V9 AD18
AD19 Y8 AD19
AD20 AA8 AD20
AD21 Y4 AD21
AD22 Y3 AD22
AD23 Y2 AD23
AD24 AA2 AD24
AD25 AB4 AD25
AD26 AA1 AD26
AD27 AB3 AD27
AD28 AB2 AD28
AD29 AC1 AD29
AD30 AC2 AD30
AD31 AD1 AD31

PCI INTERFACE

CBE0# W2 CBE0# 26
CBE1# U7 CBE1# 26
CBE2# AA7 CBE2# 26
CBE3# Y1 CBE3# 26
FRAME# AA6 FRAME# 26
DEVSEL# W5 DEVSEL# 26
IRDY# AA5 IRDY# 26
TRDY# Y5 TRDY# 26
PAR U6 PAR 26
STOP# W6 STOP# 26
PERR# W4 T53
SERR# V7 T52
REQ0# AC3 REQ0# 26
REQ1# AD4 T131
REQ2# AB7 T44
REQ3#/GPIO70 AE6 PORT_C# PORT_C# 22
REQ4#/GPIO71 AB6 T45
GNT0# AD2 GNT0# 26
GNT1# AF4 T133
GNT2# AD5 T135
GNT3#/GPIO72 AC6 PE_GPIO1 T46
GNT4#/GPIO73 AE5 T134
CLKRUN# AD6 CLKRUN# R R437 0_4 CLKRUN# 26,29
LOCK# V5 T54

INTE#/GPIO33 AD3 INTE# INTE# 26
INTF#/GPIO34 AC4 INTF# T132
INTG#/GPIO35 AE2 INTG# R435 0_4 FM_INTX 28
INTH#/GPIO36 AE3 INTH# T130

SBSRC_CLKP N25 PCIE_RCLKP/NB_LNK_CLKP
SBSRC_CLKN N24 PCIE_RCLKN/NB_LNK_CLKN
NB_DISP_CLKP K23 NB_DISP_CLKP
NB_DISP_CLKN K22 NB_DISP_CLKN
NB_HT_CLKP M24 NB_HT_CLKP
NB_HT_CLKN M25 NB_HT_CLKN
CPU_HT_CLKP P17 CPU_HT_CLKP
CPU_HT_CLKN M18 CPU_HT_CLKN
SLT_GFX_CLKP M23 SLT_GFX_CLKP
SLT_GFX_CLKN M22 SLT_GFX_CLKN
GPP_CLK0P J19 GPP_CLK0P
GPP_CLK0N J18 GPP_CLK0N
GPP_CLK1P L20 GPP_CLK1P
GPP_CLK1N L19 GPP_CLK1N
GPP_CLK2P M19 GPP_CLK2P
GPP_CLK2N M20 GPP_CLK2N
GPP_CLK3P N22 GPP_CLK3P
GPP_CLK3N P22 GPP_CLK3N
25M_48M_66M_OSC L18
25M_X1 J21
25M_X2 J20

3 SBSRC_CLKP
3 SBSRC_CLKN
T80 T71 NB_DISP_CLKP NB_DISP_CLKN
T119 T111 NB_HT_CLKP NB_HT_CLKN
T69 T64 CPU_HT_CLKP CPU_HT_CLKN
T120 T87 SLT_GFX_CLKP SLT_GFX_CLKN
T110 T108 GPP_CLK0P GPP_CLK0N
T111 T75 GPP_CLK1P GPP_CLK1N
T72 T66 GPP_CLK2P GPP_CLK2N
T65 T60 GPP_CLK3P GPP_CLK3N
T103
T78
T85

100MHZ

CLOCK GENERATOR

RTC_X1
Y3
32.768KHZ
RTC_X2
R341 20M_6
R339 20M_6
C474 18p/50V_4
C473 18p/50V_4

10/18 AMD suggest to not connect to GND

RTC_X1 A3 X1
RTC_X2 B3 X2

RTC XTAL

LPC

LPCCLK0 G22 LPC_CLK0 R251 22_4 PCLK_591 17,29
LPCCLK1 E22 LPC_CLK1 R348 22_4 PCLK_DBC 17,25
LAD0 H24 LAD0 LAD0 25,29
LAD1 H23 LAD1 LAD1 25,29
LAD2 J25 LAD2 LAD2 25,29
LAD3 J24 LAD3 LAD3 25,29
LFRAME# H25 LFRAME# LFRAME# 25,29
LDRQ0# H22 LDRQ0# SB T81
LDRQ1#/GNT5#/GPIO68 AB8 LDRQ1# SB T51
BMREQ#/REQ5#/GPIO65 AD7 SB_GPIO65 T47
SERIRQ V15 SERIRQ SERIRQ 29

+1.8V R254 *10K/F_4
+1.8VSUS R349 *10K/F_4

11 ALLOW_LDTSTOP ALLOW_LDTSTOP F23 ALLOW_LDTSTP
4 CPU_PROCHOT_SB# CPU_PROCHOT_SB# F24 PROCHOT#
4 CPU_PWRGD CPU_PWRGD F22 LDT_PG
4,11 CPU_LDT_STOP# CPU_LDT_STOP# G25 LDT_STP#
4,11 CPU_LDT_RST# CPU_LDT_RST# G24 LDT_RST#

CPU

1/31 voltage leakage remove R349

RTC

RTCCLK C3 RTC_CLK RTC_CLK 17
INTRUDER_ALERT# C2 INTRUDER_ALERT# T107
VBAT B2 VCCRTC

VCCRTC
C486 0.1u/10V_4

SB700
IC CTRL(528P) SB700 A11(218S7EALA11FG)
P/N : AJALA110T00

RTC

All the PCI bus has build-in Pull-UP/Down resistors

4/16 change RTC pad location to G1

VCCRTC
+3VPCU D7 CH500H-40
D10 CH500H-40
R238 1K_6
G1 *SHORT_PAD
R350 0_4
C317 1u/10V_4
C316 0.1u/10V_4
CN24 ACS_85204-0200L

+5VPCU
R571+R667 = (5V - 0.2V-2V)/0.2mA = 14k
R302 2K/F_4
R301 2K/F_4
VCCRTC_3
Q33 MMBT3904
R332 6.8K_4
R333 15K_6

1/17
R301,R302 change from 8.66k to 2k.
R332 change from 4.7K to 6.8K

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Quanta Computer Inc.

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+3V_S5 NC only ,Can't be install
R249 *2.2K_4 SB_TEST0
R258 *2.2K_4 SB_TEST1
R255 *2.2K_4 SB_TEST2

11/01 chagne +3VSUS to +3V_S5

+3V_S5
R253 *10K/F_4 SW1#

10/31 add newcard DET#

+3V SCL0/SDATA0 is 3V tolerance
AMD datasheet define it
R166 2.2K_4 PCLK_SMB
R167 2.2K_4 PDAT_SMB

Clock gen
/DDR2 /MINI CARD/NEW CARD

+3V_S5 SCL1/SDATA1 is 3V/S5 tolerance
AMD datasheet define it
R362 2.2K_4 SB_SMBCLK1
R361 2.2K_4 SB_SMBDATA1

+3V_S5 SCL2/SDATA2 is 3V/S5 tolerance
AMD datasheet define it
R261 2.2K_4 SB_SCLK2
R263 2.2K_4 SB_SDATA2

+3V_S5
R719 10K_4 USB_OC5#
4/16 pull up USB_OC5# R719

10/26 modify it
11/06 check it

D29 CH501H-40PT
4,8 CPU_MEMHOT#
CPU_MEMHOT# IN
USB_OC5#
T102
28,29 USBOC#3
D57 BAS316
T83
25 NEW_DET#
28,29 USBOC#0
R689 0_4
D58 BAS316

1/31 NEW_DET# change from GEVEN5# to GPM1#

12/7 add D57,D58 to avoid voltage leakage

+3V
R358 4.7K_4 SUS_STAT#
G2
SYS_RST#
*SHORT_PAD1

HD audio interface is 3.3V voltage

To Azalia

ACZ_SDOUT R364 33_4 ACZ_SDOUT_AUDIO 22
C501 *10p/50V_4
ACZ_SYNC R239 33_4 ACZ_SYNC_AUDIO 22
C296 *10p/50V_4
ACZ_BCLK R241 BK1005HM121-T_4 BIT_CLK_AUDIO 22
C309 22P/50V_4
ACZ_RST# R357 33_4 ACZ_RST#_AUDIO 22
ACZ_SDIN0_R R243 0_4 ACZ_SDIN0 22

12/21EMI
change R241from 33 to BK1005HM121-T
stff C309 22p

+3V R233 10K_4 LOW_DET LOW_DET 28
R236 *1K_4
High : Main Strem
Low : Low Cost

+3V R292 10K_4 FM_DET FM_DET 28
High : W/O FM
Low : W FM

+1.8V R285 20K_4
27 HDD_AUX_RST#
10/25 modify it

1/31 voltage leakage
BOARD_ID4 change from GPIO66 to GPIO3

15 BOARD_ID3 BOARD_ID3
15 BOARD_ID2 BOARD_ID2
15 BOARD_ID4 BOARD_ID4

MB ID

R227 *1K_4 BOARD_ID0 R232 10K_4
R228 *1K_4 BOARD_ID1 R223 10K_4
R229 IV@1K_4 BOARD_ID2 R225 EV@10K_4
R248 *1K_4 BOARD_ID3 R246 TV@10K_4
R343 *1K_4 BOARD_ID4 R342 HDM@10K_4

12/4 change PD from 10K to 1K

10/25 Board ID define MXM

MB ID Selection Table

Board ID	ID4	ID3	ID2	ID1	ID0
NEW CARD CARD BUS					H L
CCFL Panel LED Panel				H L	
W/ MXM W/O MXM			H L		
W/ S-VIDEO W/O S-VIDEO		H L			
W/ HDMI W/O HDMI	H L				

SB700 Part 4 of 5

PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S2/GPM9#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST2
TEST1
TEST0
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT2#
NB_PWRGD
RSMRST#

ACPI / WAKE UP EVENTS

USBCLK/14M_25M_48M_OSC
USB_RCOMP

USB MISC

USB 1.1

USB_FSD13P
USB_FSD13N
USB_FSD12P
USB_FSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N

USB 2.0

SATA_IS0#/GPIO10
CLK_REQ3#/SATA_IS1#/GPIO6
SMARTVOLT/SATA_IS2#/GPIO4
CLK_REQ0#/SATA_IS3#/GPIO0
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
SCL1/GPOC2#
SDA1/GPOC3#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
LLB#/GPIO66
SHUTDOWN#/GPIO5
DDR3_RST#/GEVENT7#

GPIO

USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GPM5#
USB_OC4#/IR_RX0/GPM4#
USB_OC3#/IR_RX1/GPM3#
USB_OC2#/GPM2#
USB_OC1#/GPM1#
USB_OC0#/GPM0#

USB OC

AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO42
AZ_SDIN1/GPIO43
AZ_SDIN2/GPIO44
AZ_SDIN3/GPIO46
AZ_SYNC
AZ_RST#
AZ_DOCK_RST#/GPM8#

HD AUDIO

IMC_GPIO0
IMC_GPIO1
SPI_CS2#/IMC_GPIO2
IDE_RST#/F_RST#/IMC_GPO3
IMC_GPIO4
IMC_GPIO5
IMC_GPIO6
IMC_GPIO7

INTEGRATED uC

IMC_GPIO8
IMC_GPIO9
IMC_PWM0/IMC_GPIO10
SCL2/IMC_GPIO11
SDA2/IMC_GPIO12
SCL3_LV/IMC_GPIO13
SDA3_LV/IMC_GPIO14
IMC_PWM1/IMC_GPIO15
IMC_PWM2/IMC_GPIO16
IMC_PWM3/IMC_GPO17
IMC_GPIO18
IMC_GPIO19
IMC_GPIO20
IMC_GPIO21
IMC_GPIO22
IMC_GPIO23
IMC_GPIO24
IMC_GPIO25
IMC_GPIO26
IMC_GPIO27
IMC_GPIO28
IMC_GPIO29
IMC_GPIO30
IMC_GPIO31
IMC_GPIO32
IMC_GPIO33
IMC_GPIO34
IMC_GPIO35
IMC_GPIO36
IMC_GPIO37
IMC_GPIO38
IMC_GPIO39
IMC_GPIO40
IMC_GPIO41

INTEGRATED uC

SB700

C8 CLK_48M_USB CLK_48M_USB 3
G8 USB_RCOMP_SB R247 11.8K/F_6

CLK_48M_USB
R257 *10_6
C339 *10p/50V_4
for EMI

E6 USB_FSD13P T77
E7 USB_FSD13N T94
F7 USB_FSD12P T73
E8 USB_FSD12N T82
H11 T74
J10 T68

E11 C_USBP7+ R245 0_4 USBP7+ 27
F11 C_USBP7- R244 0_4 USBP7- 27
To M/B USB/ESATA

3/3 del Mini card USB10,Felica USB5 , change BT to port5 ,
ESATA to port 10

C10 NEW_USBP6+ 25
D10 NEW_USBP6- 25
To New Card

E12 C_USBP0+ R274 0_4 USBP0+ 28
E14 C_USBP0- R280 0_4 USBP0- 28
To M/B USB

10/25 change M.B USB to port 6/7

C12 BT_USBP8+ 28
D12 BT_USBP8- 28
To Bluetooth

B12 FP_USBP4+ 28
A12 FP_USBP4- 28
To Finger Printer

G12 C_USBP3+ R265 0_4 WL_USBP3+ 25
G14 C_USBP3- R267 0_4 WL_USBP3- 25
To WLAN

H14 C_USBP2+ R283 0_4 CCD_USBP2+ 20
H15 C_USBP2- R284 0_4 CCD_USBP2- 20
To Camera

A13 USBP1+ 28
B13 USBP1- 28
To USB BOARD

B14 USBP9+ 28
A14 USBP9- 28
To USB BOARD

10/18 USB swap for layout route

D21 SB_SCLK2 SB_SCLK2 19
F19 SB_SDATA2 SB_SDATA2 19
E20 SB_SCLK3 SB_SCLK3 4
F21 SB_SDATA3 SB_SDATA3 4
D19 SB_GPIO16 SB_GPIO16 17
E18 SB_GPIO17 SB_GPIO17 17
SPI/LPC define

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PLACE SATA AC COUPLING
CAPS CLOSE TO SB700

SATA PORT 0,1,2,3
can support AHCI
mode

SATA1

SATA2

E-SATA

2/22 change SATA ODD from port3 to port4 (solve ODD post detect fail)

ODD

SATA PORT 4,5 are
only support IDE
mode

PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF SB700

NOTE:
R361 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

10/25 modify it

PLVDD_SATA--
SATA PLL
POWER

XTLVDD_SATA-- SATA
crystal power

12/8 change from 10p to 27p

U6B

SB700
Part 2 of 5

SERIAL ATA

SATA PWR

ATA 66/100/133

SPI ROM

HW MONITOR

12/4 change BOARD ID3 from GEVENT7 to GPIO48

11/02 modify it

10/18 AMD suggest to connect to GND

5mA

AVDD--H/W monitor
Analog power

2/13 EMI
stuff C375,C366 for SB HW MONITOR

77mA

1mA

Place near ball

PROJECT : BD3G
Quanta Computer Inc.

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	SB700-SATA/IDE/HWM/SPI 3/4	1A
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PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

12/14 del R234 stuff R235 for A2

VDDQ--3.3V I/O power

+3V → R237 0_8 → +3.3V_SB_R, 0.8A

C285 100u/6.3V_3528; C282 10u/6.3V_8; C307 1u/10V_4; C298 1u/10V_4; C320 1u/10V_4; C305 1u/10V_4; C313 1u/10V_4; C291 1u/10V_4

U6C SB700 Part 3 of 5

VDDQ_1 L9, VDDQ_2 M9, VDDQ_3 T15, VDDQ_4 U9, VDDQ_5 U16, VDDQ_6 U17, VDDQ_7 V8, VDDQ_8 W7, VDDQ_9 Y6, VDDQ_10 AA4, VDDQ_11 AB5, VDDQ_12 AB21

PCI/GPIO I/O

1.8V : FLASH MEMORY MODE(DEFAULT)
3.3V: IDE MODE

10/18 change to +1.8V

VDD33_18--3.3V IDE I/O power
1.8V flash memory I/O power

+1.8V → R231 2 1_0_8 → +VDD33_18, 0.45A

C287 *10u/6.3V_8; C288 *1u/10V_4; C297 *1u/10V_4; C293 *1u/10V_4; C294 *1u/10V_4

VDD33_18_1 Y20, VDD33_18_2 AA21, VDD33_18_3 AA22, VDD33_18_4 AE25

IDE/FLSH I/O

4/24 IDE/FLASH not use
,remove
C287,C288,C297,C293,C294

VDD-- S/B CORE power

+1.2V_VCC_SB_R → 604mA → R235 0_8 → +1.2V

C312 1u/10V_4; C314 1u/10V_4; C324 1u/10V_4; C323 1u/10V_4; C281 10u/6.3V_8

VDD_1 L15, VDD_2 M12, VDD_3 M14, VDD_4 N13, VDD_5 P12, VDD_6 P14, VDD_7 R11, VDD_8 R15, VDD_9 T16

CORE S0

CKVDD_1.2V-- Internal clock Generator I/O power

+1.2V_CKVDD → 286mA → L28 0_6 → +1.2V

C332 *2.2u/6.3V_6; C330 *0.1u/50V_6; C327 *0.1u/50V_6; C331 *2.2u/6.3V_6

CKVDD_1.2V_1 L21, CKVDD_1.2V_2 L22, CKVDD_1.2V_3 L24, CKVDD_1.2V_4 L25

CLKGEN I/O

4/24 internal clk not use
remove C332,C330,C327,C331
change L28 to 0 ohm

POWER

PCIE_VDDR--PCIE I/O power

+1.2V → L34 BLM18PG221SN1D(220,1.4A)_6 → +1.2V_PCIE_VDDR, 844mA

C301 10u/6.3V_8; C302 1u/10V_4; C311 1u/10V_4; C303 1u/10V_4; C299 1u/10V_4; C308 1u/10V_4

PCIE_VDDR_1 P18, PCIE_VDDR_2 P19, PCIE_VDDR_3 P20, PCIE_VDDR_4 P21, PCIE_VDDR_5 R22, PCIE_VDDR_6 R24, PCIE_VDDR_7 R25

A-LINK I/O

S5_3.3--3.3v standby power

+3VALW_R → 0.01A → R336 0_6 → +3V_S5

Change to 0603

C487 0.1u/10V_4; C326 0.1u/10V_4; C482 10u/6.3V_8

S5_3.3V_1 A17, S5_3.3V_2 A24, S5_3.3V_3 B17, S5_3.3V_4 J4, S5_3.3V_5 J5, S5_3.3V_6 L1, S5_3.3V_7 L2

3.3V_S5 I/O

AVDD_SATA--SATA phy power

+1.2V → L35 BLM18PG221SN1D(220,1.4A)_6 → +1.2V_AVDD_SATA, 0.2A

C521 10u/6.3V_8; C304 0.1u/10V_4; C295 0.1u/10V_4; C292 1u/10V_4; C284 1u/10V_4

AVDD_SATA_1 AA14, AVDD_SATA_4 AB18, AVDD_SATA_2 AA15, AVDD_SATA_3 AA17, AVDD_SATA_5 AC18, AVDD_SATA_6 AD17, AVDD_SATA_7 AE17

SATA I/O

S5_1.2V--1.2V standby power

+1.2VALW_R → 0.22A → R250 0_6 → +1.2V_S5

C335 0.1u/10V_4; C342 0.1u/10V_4

S5_1.2V_1 G2, S5_1.2V_2 G4

CORE S5

0.2A → +1.2V_USB_PHY_R

USB_PHY_1.2V_1 A10, USB_PHY_1.2V_2 B10

For support USB wakeup-->3V_S5

AVDDTX--USB Phy Analog I/O power

+3V_S5 → L33 BLM18PG221SN1D(220,1.4A)_6 → +3V_AVDD_USB, 0.2A

C477 10u/6.3V_8; C475 10u/6.3V_8; C488 0.1u/10V_4; C484 0.1u/10V_4

C367 1u/10V_4; C334 1u/10V_4; C489 1u/10V_4; C388 0.1u/10V_4; C379 0.1u/10V_4; C483 0.1u/10V_4; C333 0.1u/10V_4

AVDDTX_0 A16, AVDDTX_1 B16, AVDDTX_2 C16, AVDDTX_3 D16, AVDDTX_4 D17, AVDDTX_5 E17, AVDDRX_0 F15, AVDDRX_1 F17, AVDDRX_2 F18, AVDDRX_3 G15, AVDDRX_4 G17, AVDDRX_5 G18

USB I/O

V5_VREF--PCI 5V TOLERANCE

V5_VREF AE7 ← +5V_VREF, 4mA → R436 1K/F_4 → +5V

D31 CH501H-40PT → +3V

AVDDCK_3.3V J16 ← +3V_AVDDCK, 7mA

AVDDCK_1.2V K17 ← +1.2V_AVDDCK, 44mA

AVDDC E9 ← +3V_AVDDC, 16mA

C274 1u/10V_4

PLL

USB_PHY_1.2V--USB Phy digital power

+1.2V_S5 → R334 0_6 → +1.2V_USB_PHY_R

C485 0.1u/10V_4; C481 0.1u/10V_4; C478 10u/6.3V_8

AVDDC--USB Analog PLL power

+3V_S5 → L32 BLM18PG221SN1D(220,1.4A)_6 → +3V_AVDDC

C389 0.1u/10V_4; C413 10u/6.3V_8

AVDDCK_1.2--USB Phy digital power

+1.2V → L29 BLM18PG221SN1D(220,1.4A)_6 → +1.2V_AVDDCK

C336 2.2u/6.3V_6

AVDDCK_3.3--Analog system PLL power

+3V → L30 BLM18PG221SN1D(220,1.4A)_6 → +3V_AVDDCK

C337 2.2u/6.3V_6

U6E SB700 Part 5 of 5

AVSS_SATA_1 T10, AVSS_SATA_2 U10, AVSS_SATA_3 U11, AVSS_SATA_4 U12, AVSS_SATA_5 V11, AVSS_SATA_6 V14, AVSS_SATA_7 W9, AVSS_SATA_8 Y9, AVSS_SATA_9 Y11, AVSS_SATA_10 Y14, AVSS_SATA_11 Y17, AVSS_SATA_12 AA9, AVSS_SATA_13 AB9, AVSS_SATA_14 AB11, AVSS_SATA_15 AB13, AVSS_SATA_16 AB15, AVSS_SATA_17 AB17, AVSS_SATA_18 AC8, AVSS_SATA_19 AD8, AVSS_SATA_20 AE8

AVSS_USB_1 A15, AVSS_USB_2 B15, AVSS_USB_3 C14, AVSS_USB_4 D8, AVSS_USB_5 D9, AVSS_USB_6 D11, AVSS_USB_7 D13, AVSS_USB_8 D14, AVSS_USB_9 D15, AVSS_USB_10 E15, AVSS_USB_11 F12, AVSS_USB_12 F14, AVSS_USB_13 G9, AVSS_USB_14 H9, AVSS_USB_15 H17, AVSS_USB_16 J9, AVSS_USB_17 J11, AVSS_USB_18 J12, AVSS_USB_19 J14, AVSS_USB_20 J15, AVSS_USB_21 K10, AVSS_USB_22 K12, AVSS_USB_23 K14, AVSS_USB_24 K15

PCIE_CK_VSS_1 H18, PCIE_CK_VSS_2 J17, PCIE_CK_VSS_3 J22, PCIE_CK_VSS_4 K25, PCIE_CK_VSS_5 M16, PCIE_CK_VSS_6 M17, PCIE_CK_VSS_7 M21, PCIE_CK_VSS_8 P16

AVSSC F9

VSS_1 A2, VSS_2 A25, VSS_3 B1, VSS_4 D7, VSS_5 F20, VSS_6 G19, VSS_7 H8, VSS_8 K9, VSS_9 K11, VSS_10 K16, VSS_11 L4, VSS_12 L7, VSS_13 L10, VSS_14 L11, VSS_15 L12, VSS_16 L14, VSS_17 L16, VSS_18 M6, VSS_19 M10, VSS_20 M11, VSS_21 M13, VSS_22 M15, VSS_23 N4, VSS_24 N12, VSS_25 N14, VSS_26 P6, VSS_27 P9, VSS_28 P10, VSS_29 P11, VSS_30 P13, VSS_31 P15, VSS_32 R1, VSS_33 R2, VSS_34 R4, VSS_35 R9, VSS_36 R10, VSS_37 R12, VSS_38 R14, VSS_39 T11, VSS_40 T12, VSS_41 T14, VSS_42 U4, VSS_43 U14, VSS_44 V6, VSS_45 V21, VSS_46 AB1, VSS_47 AB19, VSS_48 AB25, VSS_49 AE1, VSS_50 AE24

PCIE_CK_VSS_9 P23, PCIE_CK_VSS_10 R16, PCIE_CK_VSS_11 R19, PCIE_CK_VSS_12 T17, PCIE_CK_VSS_13 U18, PCIE_CK_VSS_14 U20, PCIE_CK_VSS_15 V18, PCIE_CK_VSS_16 V20, PCIE_CK_VSS_17 V21, PCIE_CK_VSS_18 W19, PCIE_CK_VSS_19 W22, PCIE_CK_VSS_20 W24, PCIE_CK_VSS_21 W25

AVSSCK L17

GROUND

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Quanta Computer Inc.

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	SB700-PWR/DECOUPLING 4/4	1A
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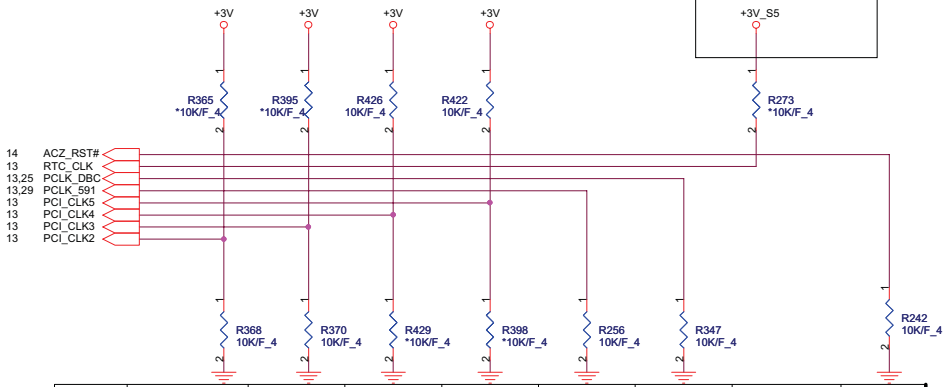
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

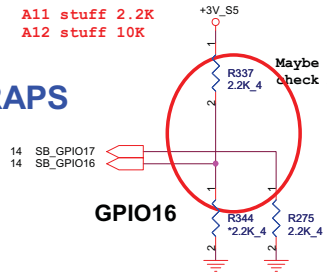
It must ready refore RSMRST#



	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT
					EC ENABLED			ENABLE PCI MEM BOOT

REQUIRED STRAPS

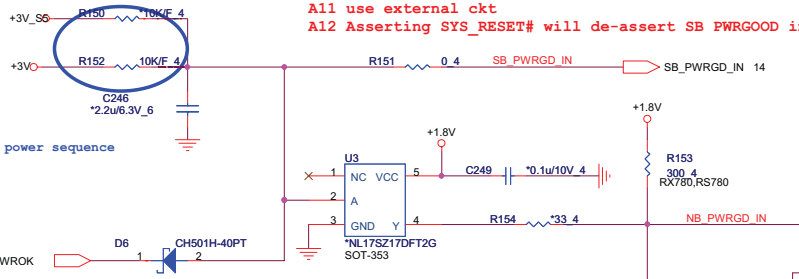
A11 stuff 2.2K
A12 stuff 10K



TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)

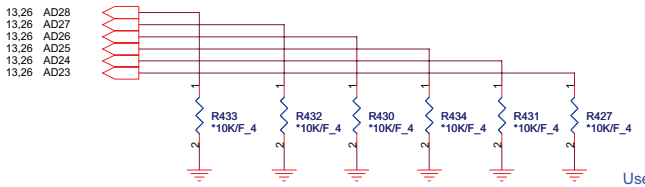
SB_PWRGD
A11 use external ckt
A12 Asserting SYS_RESET# will de-assert SB PWRGOOD internally



4/10 change R150 to R152 for power sequence

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



Use 2.2K PD.

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

NB/SB POWER GOOD CIRCUIT

WD_PWRGD: Push/Pull when A11SB700, OD when A12SB700.

	U11	R230	R229	R245	R234
RX780 RS780M	V	V	V	X	X

AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5

12/18 add cap for NB_PWRGD signal

4/24 stuff C765 10nf to meet power sequence

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	SB700-STRAPS	1A
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TVOUT BTO

5/8 stuff D9,D11 for S-VIDEO

TVOUT

close to NB & VGA connector

12/21 EMI
add 27p for TV_Y/G , TV_C/R

21 EXT_TV_Y/G — R497 EV@0_4 — SYS_TV_Y/G
21 EXT_TV_C/R — R496 EV@0_4 — SYS_TV_C/R
C790 EV@27p/50V_4 — C791 EV@27p/50V_4
11 INT_TV_Y/G — R189 IV@0_4
11 INT_TV_C/R — R190 IV@0_4
C792 IV@27p/50V_4 — C793 IV@27p/50V_4

SYS_TV_C/R — L14 TV@BLM18PG181SN1D — TV-CHROMA — CN22 — TV-LUMA — L20 TV@BLM18PG181SN1D — SYS_TV_Y/G
R105 TV@150/F_4 — C149 TV@6p/50V_4 — C148 TV@6p/50V_4
C214 TV@6p/50V_4 — C215 TV@6p/50V_4 — R158 TV@150/F_4
TV@SUYIN_030018FR004S100FR

A:(10/24) change CN22 from 7PIN to 4PIN CONN

10/24 modify it to 4 pin BOI request
10/30 modify footprint to SV-030018FR004S100FR-RVS-4P-H
12/12 update p/n to DFMD04FR006
4/16 update footprint to sv-030018fr004s100fr-4p-h-b15m

BTO

+3V — D9 TV-CHROMA — TV@DA204U
+3V — D11 TV-LUMA — TV@DA204U

CRT PORT

2/1
RS780M A13 R8 ---> 140 CS11402FB19
MXM R8 ---> 150 CS11502FB21

1/31 EMI Change L4,L5,L6 from CX0HM121008 to CX8BA470003

10/12 fix CRT connect error

2/10 DEL D4,D5 footprint and DEL CRT_SENSE# net

10/25 no use sense

close to NB & VGA connector

21 EXT_VGA_RED — R196 EV@0_4 — CRT_R
21 EXT_VGA_GRN — R195 EV@0_4 — CRT_G
21 EXT_VGA_BLU — R194 EV@0_4 — CRT_B
21 EXT_HSYNC — R198 EV@0_4 — HSYNC
21 EXT_VSYNC — R197 EV@0_4 — VSYNC
21 EXT_CRT_DDCCLK — R193 EV@0_4 — DDCCLK
21 EXT_CRT_DDCDAT — R192 EV@0_4 — DDCDAT

11 INT_CRT_RED — R184 IV@0_4
11 INT_CRT_GRN — R183 IV@0_4
11 INT_CRT_BLU — R182 IV@0_4
11 INT_HSYNC — R187 IV@0_4
11 INT_VSYNC — R186 IV@0_4
11 INT_CRT_DDCCLK — R181 IV@0_4
11 INT_CRT_DDCDAT — R180 IV@0_4

+5V — D30 SSM14 — F4 FUSE/1A6V_POLY-1A-6V — 25 MIL — 5V_CRT2
C433 0.1u/10V_4

CRT_R — L6 BLM18BA470SN1_6 — CRT_R1 — R8 150/F — C11 6.8p_4 — R6 150/F_4
CRT_G — L5 BLM18BA470SN1_6 — CRT_G1 — C8 6.8p_4 — R4 150/F_4
CRT_B — L4 BLM18BA470SN1_6 — CRT_B1 — C5 6.8p_4 — C4 6.8p_4 — C7 6.8p_4 — C10 6.8p_4

A:(8/20) change from 39 to 0 ohm
Because MXM side already be stuff 30ohm

2/13 EMI
C4,C7,C10,C5,C8,C11 change from 10p to 6.8p

CN18 — DSUB-070549FR015SX03CX-15P-V — T172

A:(8/20) Reserve Diode for ESD solution

U4 CM2009
5V_CRT2 — VCC_SYNC SYNC_OUT2 — VSYNC1 — R14 0_4 — VSYNC1_CRT — L8 BLM18BA220SN1D_6 — CRTVSYNC
+5V — C25 0.22u/10V_6 — VCC_DDC BYP — SYNC_OUT1 — HSYNC1 — R13 0_4 — HSYNC1_CRT — L7 BLM18BA220SN1D_6 — CRTHSYNC
+3V — VCC_VIDEO — SYNC_IN2 — VSYNC — HSYNC
CRT_R1 — VIDEO_1 — DDC_IN1 — DDCCLK
CRT_G1 — VIDEO_2 — DDC_IN2 — DDCDAT
CRT_B1 — VIDEO_3
GND — DDC_OUT1 — CRTDCLK
DDC_OUT2 — CRTDDAT

LCD_ON
C14 *10p/50V_4 — C13 *10p/50V_4
A:(10/5) default no stuff
5V_CRT2 — R5 6.8K_4 — R7 6.8K_4
A:(8/28) change from 2.7k to 6.8k
Follow AMD check list
C8 *10p/50V_4 — C9 *10p/50V_4
A:(8/27) default no stuff

H=1.75mm

+5V — C24 0.1u/10V_4
+3V — C18 0.1u/10V_4

DDCCLK — R22 4.7K_4 — +3V
DDCDAT — R21 4.7K_4
A:(8/28) change from 2.2k to 4.7k
Follow AMD check list

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Quanta Computer Inc.

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	SB600 STRAPS/TV/CRT	2A
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BTO (all parts in the page)

Reserve Test Pad for Debug

REV04 Reserve Test Pad for Debug

1/31 DChange U11 from ARBL5SV0000 to ARBL5MV0000

11/01 no stuff U13 to avoid leakage

9/07 Add

To EC

To SB

8/30 Change HDMI HPD circuit

REV02 SWAP net

To EC

REV02 Add C5806

REV02 Add C5807

REV02 Add R5812,R5813

To IV/EV VGA Hot Plug Detect

From HDMI conn Pin 19 (Hot Plug Det)

2/4 reserve C798 PLTRST#

REV02 Modify net to PLTRST#

To HDMI CONN Pin 13

HDMI

close to NB & VGA connector

10/22 add level shift for CEC

10/18 update footpritnt HDMI-C12816-119A5-L-19P-H-BL5

12/4 update footprint to HDMI-C12816-119A5-L-19P-V-BL5-1

12/7 update footprint to HDMI-C12816-119A5-L-19P-H-BD3

1/17 update footprint to HDMI-C12816-119A5-L-19P-H-BL5

1/31 DEL L56,L57,L58,L59,R465,R474,R493,R495,R486,R488,R478,R483,C226,C227 for HDMI circuit

2/13 EMI stuff C808 for HDMI

2/1 change R168,R171,R163,R170 to 4.7K

2/1 change R1,R2 to 6.8K

2/4 let layout smooth to modify ckt

1/01 add stitch cap for HDMI

Close to HDMI Connector

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Quanta Computer Inc.		
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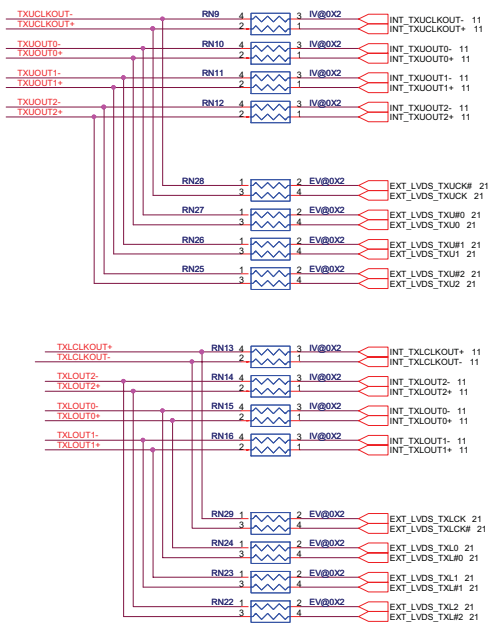
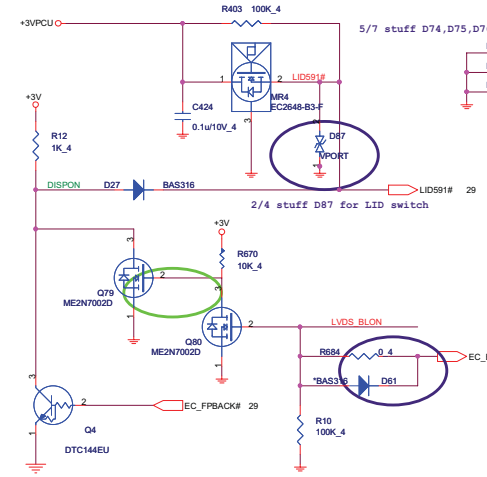
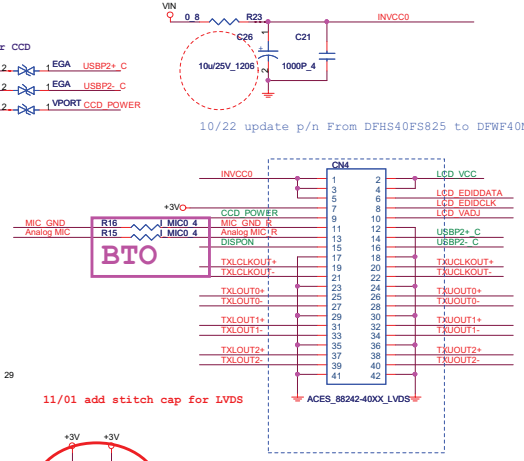
HALL SENSOR

LCD TYPE CONNECTOR

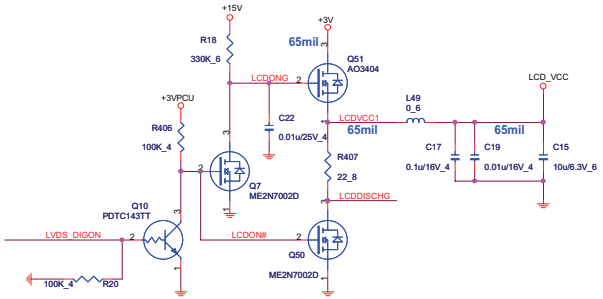




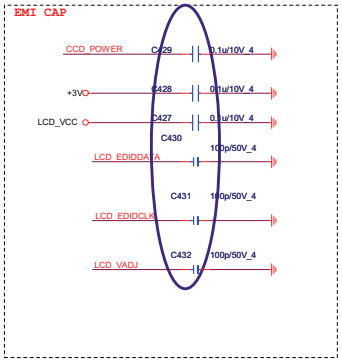
12/4 modify display on ckt to avoid flash when into S3/S4/S5

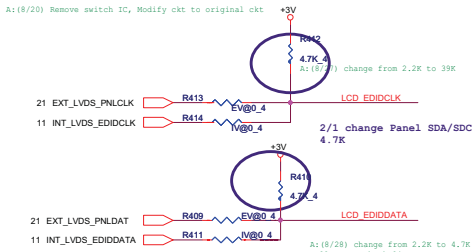


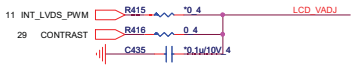
1/17 EnegryStar 4.0 Idle power issue
When BLON= High, Turn ON LCD then turn ON MMB
When BLON= Low, Turn OFF LCD then turn OFF MMB

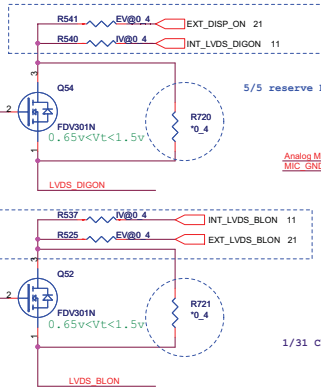


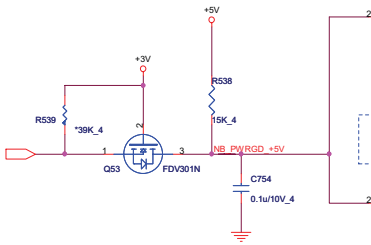
2/13 EMI
stuff C427~C432

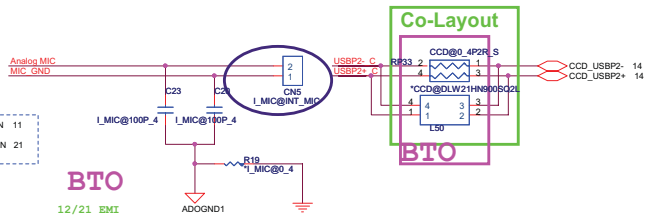






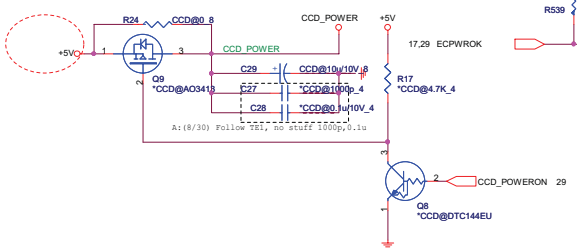






BTO

CAMERA MODULE



A:(8/27) Camera module power +5V or +3V?

A:(8/18) update VGA conn footprint based on Allan information
A:(8/23) update VGA conn pin-define (change pin 1 location)

CN27

PEG_TXN15 PEG_TXP15 PEG_TXN14 PEG_TXP14 PEG_TXN13 PEG_TXP13 PEG_TXN12 PEG_TXP12 PEG_TXN11 PEG_TXP11 PEG_TXN10 PEG_TXP10 PEG_TXN9 PEG_TXP9 PEG_TXN8 PEG_TXP8 PEG_TXN7 PEG_TXP7 PEG_TXN6 PEG_TXP6 PEG_TXN5 PEG_TXP5 PEG_TXN4 PEG_TXP4 PEG_TXN3 PEG_TXP3 PEG_TXN2 PEG_TXP2 PEG_TXN1 PEG_TXP1 PEG_TXN0 PEG_TXP0

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EXT_CRT_DDCCLK EXT_CRT_DDCDAT
EXT_HDMI_DDCCLK EXT_HDMI_DDCDAT
EXT_LVDS_PNLCLK EXT_LVDS_PNLDAT
EXT_VGA_RED EXT_VGA_GRN EXT_VGA_BLU
EXT_LVDS_TXL#2 EXT_LVDS_TXL2 EXT_LVDS_TXL#1 EXT_LVDS_TXL1 EXT_LVDS_TXL#0 EXT_LVDS_TXL0 EXT_LVDS_TXLCK# EXT_LVDS_TXLCK
EXT_TV_C/R EXT_TV_Y/G EXT_TV_COMP
EXT_HDMICLK- EXT_HDMICLK+ EXT_HDMITX2N EXT_HDMITX2P EXT_HDMITX1N EXT_HDMITX1P EXT_HDMITX0N EXT_HDMITX0P

MXM_REFCLKN MXM_REFCLKP
PLTRST# SYSFANON# MAINON GFXPG
VGA_MBDATA VGA_MBCLK
EXT_LVDS_BLON EXT_DISP_ON DVI_HPD
EXT_HSYNC EXT_VSYNC
EXT_LVDS_TXU#2 EXT_LVDS_TXU2 EXT_LVDS_TXU#1 EXT_LVDS_TXU1 EXT_LVDS_TXU#0 EXT_LVDS_TXU0 EXT_LVDS_TXUCK# EXT_LVDS_TXUCK

EV@QT00200A-5120T-9F

+5V 0.5A
+3V 1.5A
A:(9/14) no stuff for A-stage
VIN 4A
A:(9/14) no stuff for A-stage

10/30 modify to +3V

+3V C566 EV@0.1u/10V_4 C565 EV@10u/6.3V_6
+5V C563 EV@0.1u/10V_4 C569 EV@10u/6.3V_6
VIN C568 0.1u/50V_6 C548 0.1u/50V_6
A:(8/29) reserve 100u for VIN
C256 *100u/25V_6X7.7

2/4 reserve C797 PLTRST#

C797 PLTRST# *.1U_4

A:(9/18) don't connect pin 161, 167, 171, 183, 187,188 to ground and reserve test point for A build.

A:(9/19) don't have enough space to put the test point, Remove it for A-test

1/17 Remove R492,R517, Short CN27/Pin189,190 to VIN directly.

12/21 EMI
stuff C568,C548

+3V R208 EV@4.7K_4 Q37 EV@RHU002N06 19,28,29 3ND_MBCLK VGA_MBCLK
+3V R203 EV@4.7K_4 Q34 EV@RHU002N06 19,28,29 3ND_MBDATA VGA_MBDATA

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Quanta Computer Inc.

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	MXM CONNECTOR / TV	2A
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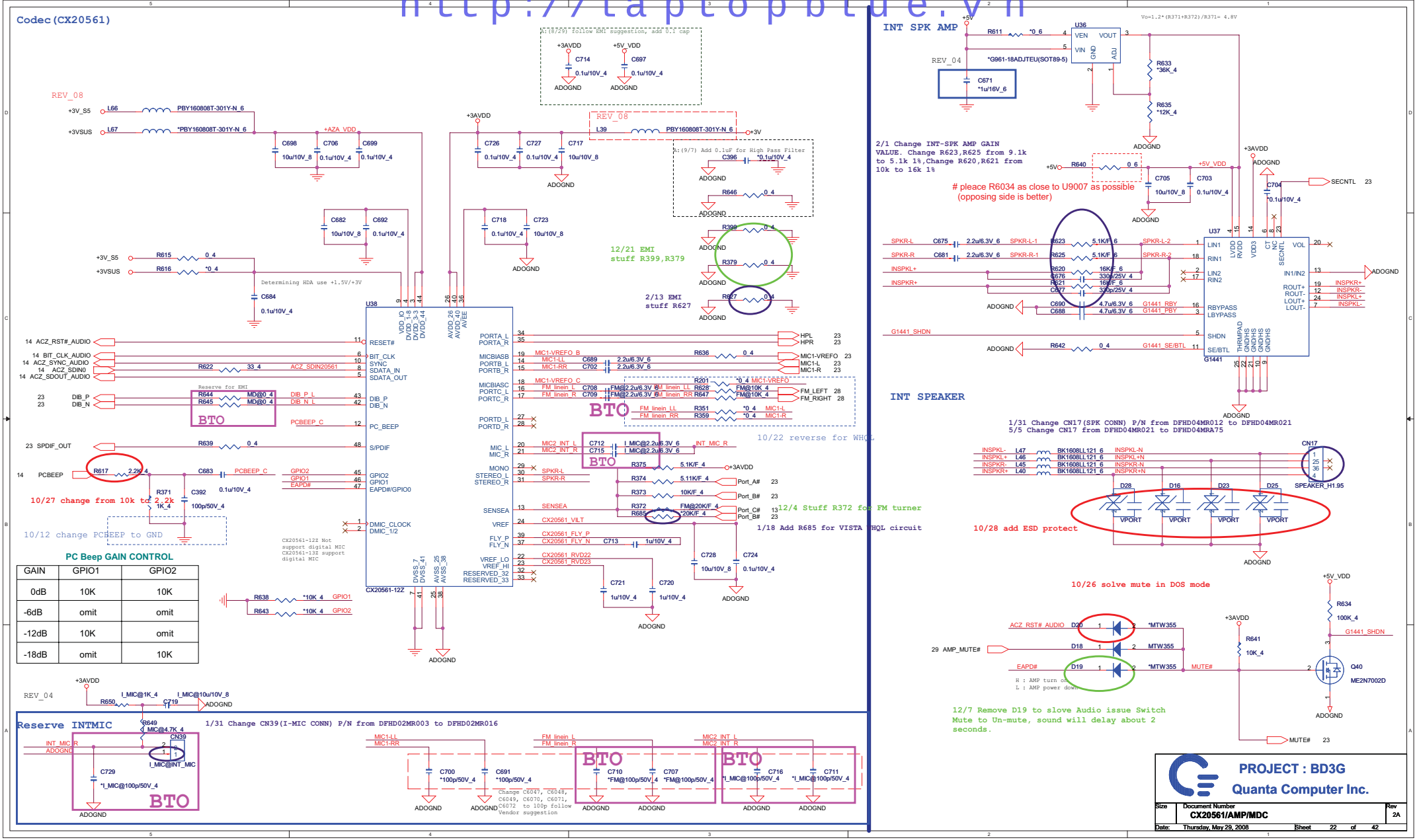
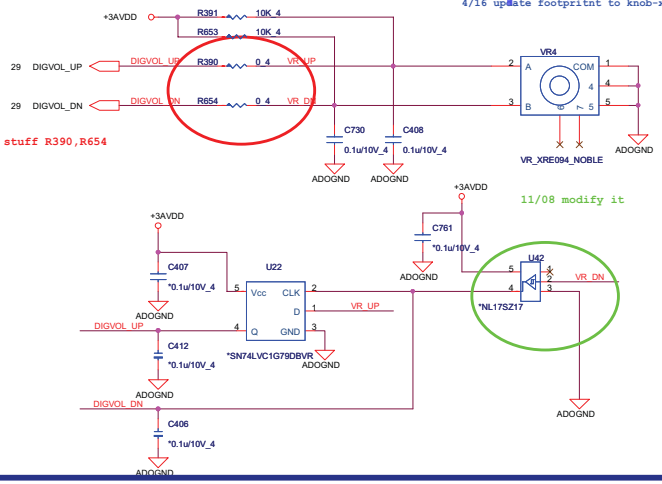
Codec (CX20561)



VR

4/16 update footpritnt to knob-xre094-3p-bl5m

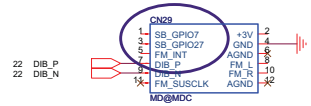


MDC

REV_04

1/18 Change CN43 footprint from MDC-1-179373-2-12P-RUV to MDC-1-179373-2-12P-RUV-BD3A (SMT open issue)

BTO



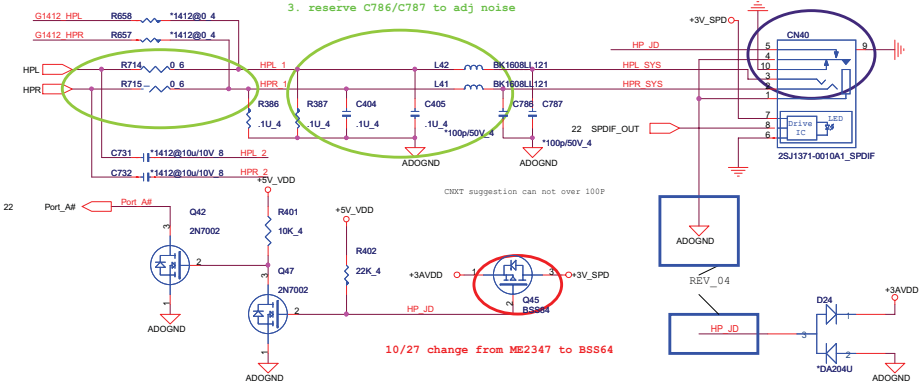
12/07 Slove Audio issue:When plug in-out headphone,headphone has bo sound.
1. Change R652&R651 to C763,C764(10U/6.3V 0603)

2/5 Change R714,R715 from 10uF to 0 ohm (Audio HP circuit)

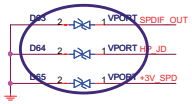
HP

12/20 solve GPRS noise
1. stuff R386/R387/C404/C405 to 0.1U
2. Change L44/41 to BK1608LL121
3. reserve C786/C787 to adj noise

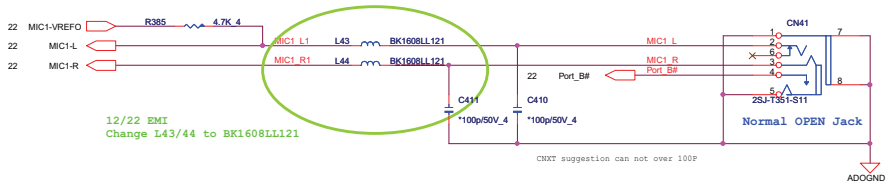
2/4 CN40 pin 9/10 connect to GND



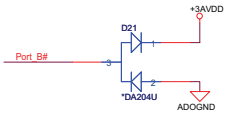
2/4 add Varistor D63,D64,D65 on SPDIF_OUT/HP_JD/+3V_SPD



SYSTEM MIC

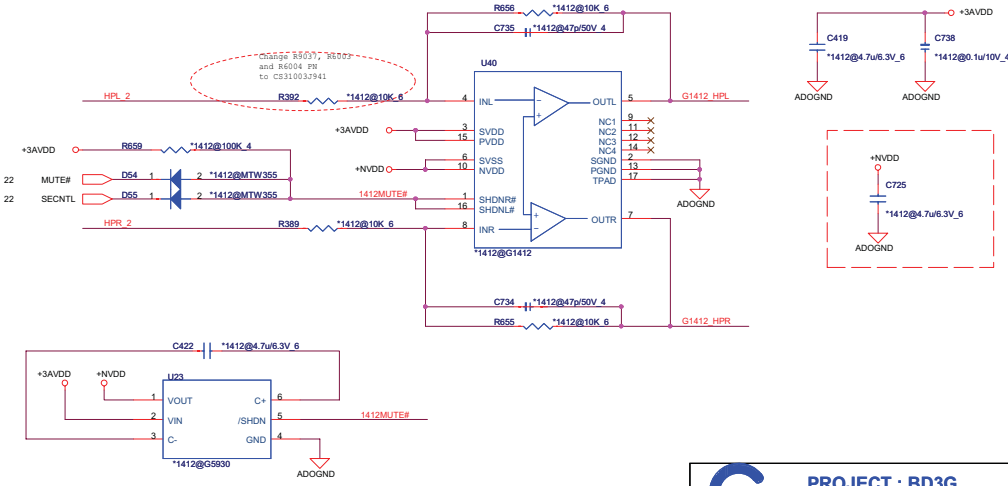


12/22 EMI
Change L43/44 to BK1608LL121



HP Amplifier

REV_05



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Quanta Computer Inc.

Size	Document Number	Rev
	Audio JACK /VR/FM Tuner	2A
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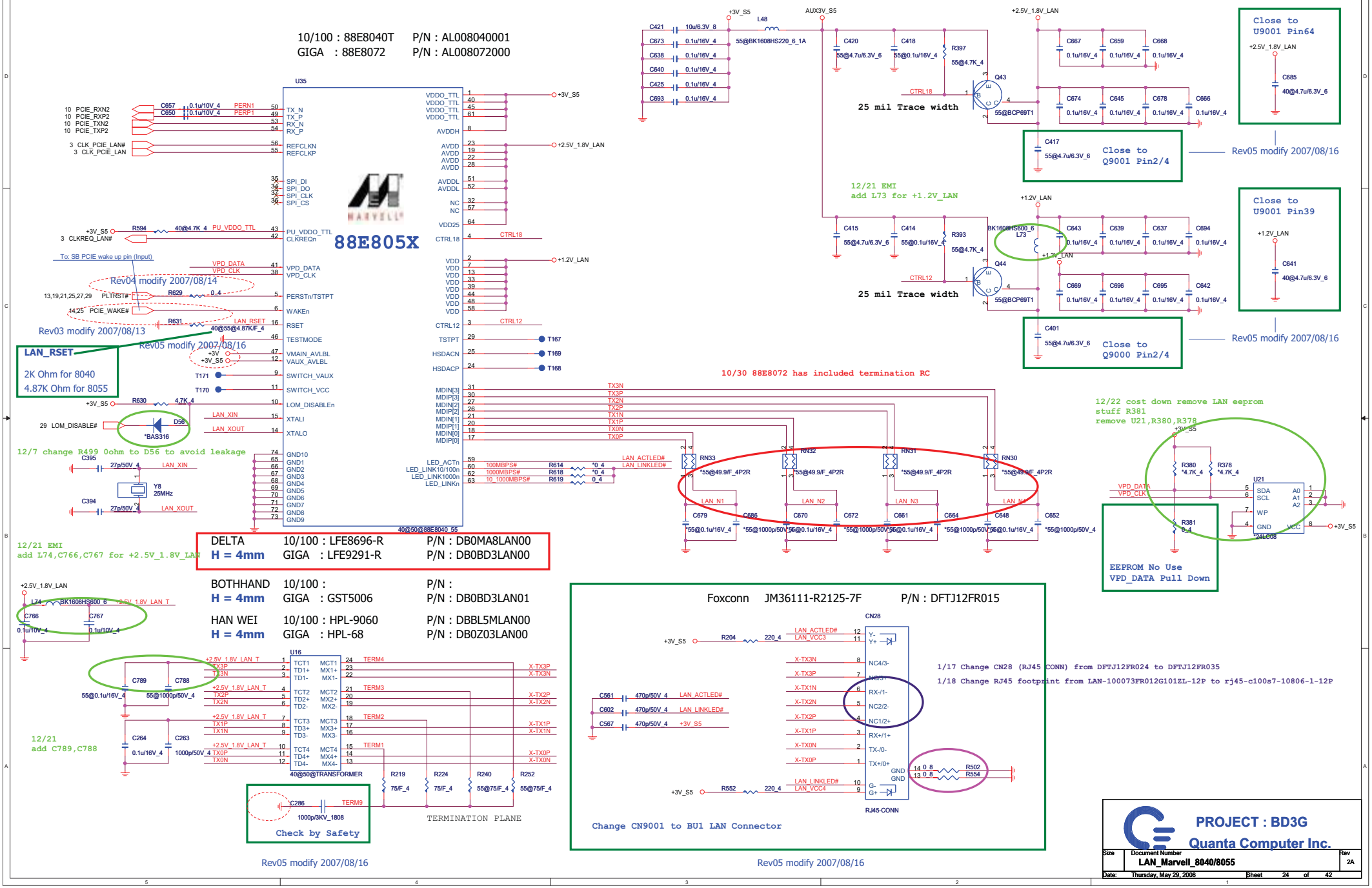
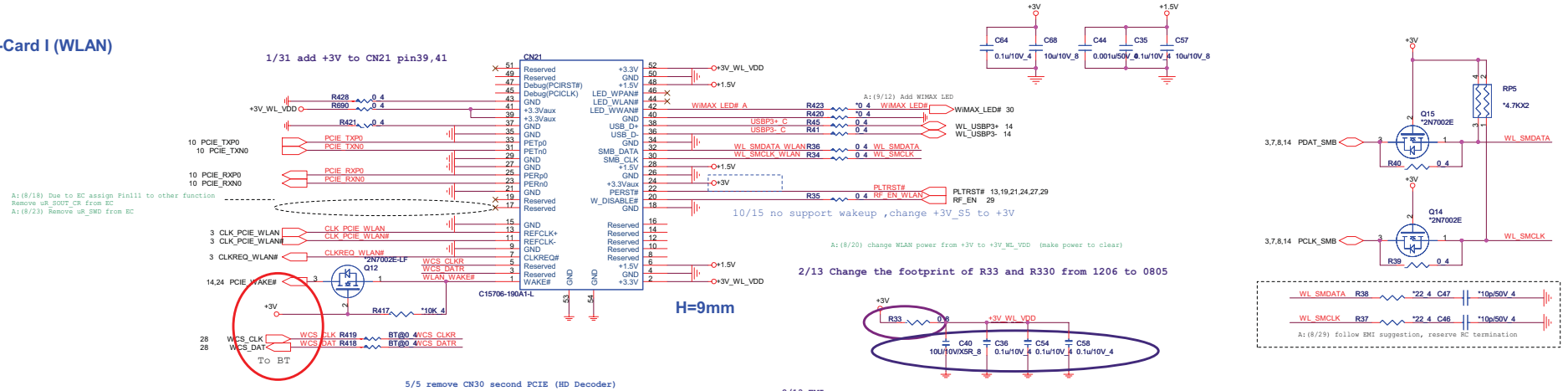
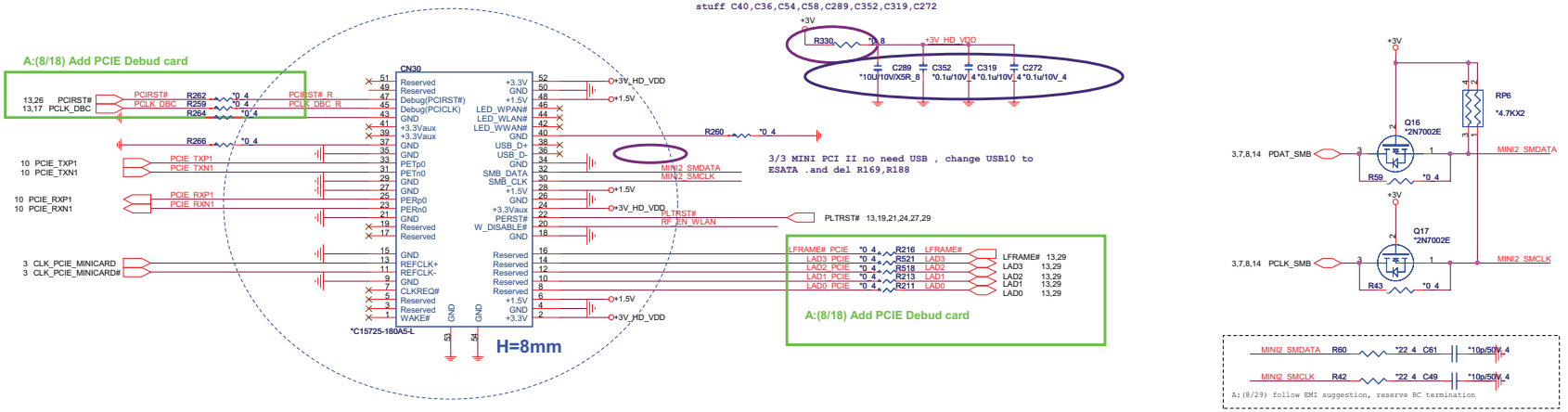
LAN_MARVELL_88E8040/88E8055



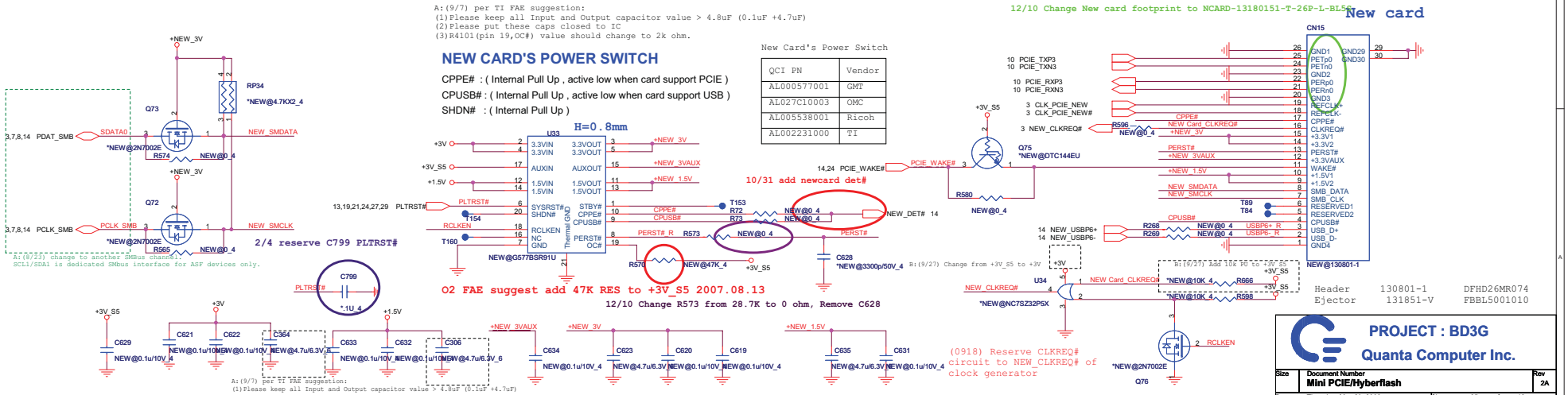
MINI-Card I (WLAN)



MINI-Card II (HD Decoder)



New card



QCI PN	Vendor
AL000577001	GMT
AL027C10003	OMC
AL005538001	Ricoh
AL002231000	TI

PROJECT : BD3G
Quanta Computer Inc.

Size	Document Number	Rev
	Mini PCIE/Hyberflash	2A
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MMC

CARDREADER POWER

30mil

12/21 EMI
R308~R329 0ohm(CS00002JB38) change to 33ohm(CS03302JB29)

1/31 hange CN33(5 in 1 card CONN) P/N from DFHS38FR003 to DFHS38FR005

5/9 for card reader MS DUO adapter short issue
reserve R723,724,722 ,Q82,Q81,Q83,Q84

5 IN 1 CARD READER

MXP038-C0-1015

A:(8/29) change from 33 to 0 ohm
connect the socket and chip by wire directly, and keep same length of these signals.
but if these signal over 15 -cm , please consider to add these damping resistors.

1394

12/21 EMI
Don't stuff RN34,RN35(CJ000042N12)
Add L68,L69(CX0900JT005)

As close as possible to OZ129

These 1394 signals are high speed differential pairs and must be kept equal length with a differential impedance (Zo) of 110ohms.

2/29 del RN34,RN35

2/4 reserve D88~D91 for 1394

4/10 add D88~D91 for 1394 ESD

12/8 change from 22p to 18p

H=1.2mm Better than 50ppm

12/21 add 0 ohm and 22p for SD/MS CLK

1/31 According to customer request, we can't stuff C782(22pF) in SD/MS_CLK
2/13 EMI change R683 from 0 to 33 ohm

A:(8/29) add 100ohm is that reduce the notice form PCI signal.

A:(8/24) Remove 33 ohm serial resister for PCIRST# (22 ohm resister alerady be puted in SB600 side)

A:(8/14)Base on AMD platform, change net name from INTA# to INTE#

A:(9/7)Correct P/N to 1% resister

H=1.6mm

5/27 some 1394 device can't boot normal
change L38 to BK1608HS220_6

Change Pulled-up Resistor on the South Bridge side.

Reserve EMI

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Quanta Computer Inc.	
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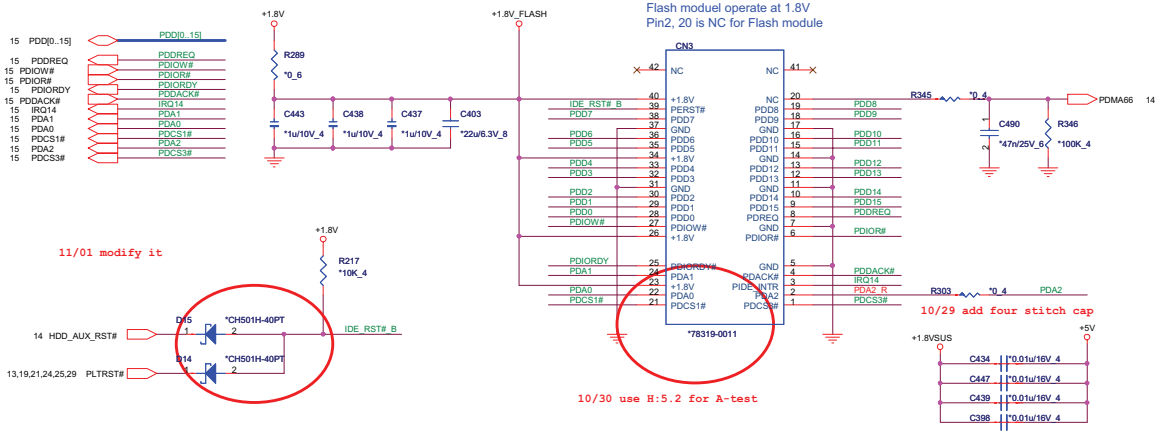
FLASH

4/10 remove Flash Card Cct

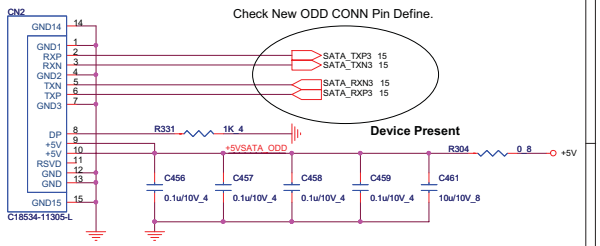
Flash moduel operate at 1.8V
Pin2, 20 is NC for Flash module



SATA ODD

9/28 change to SATA ODD conn to BD3G use

10/22 update footprint to SATA-C18534-11305-13P-R

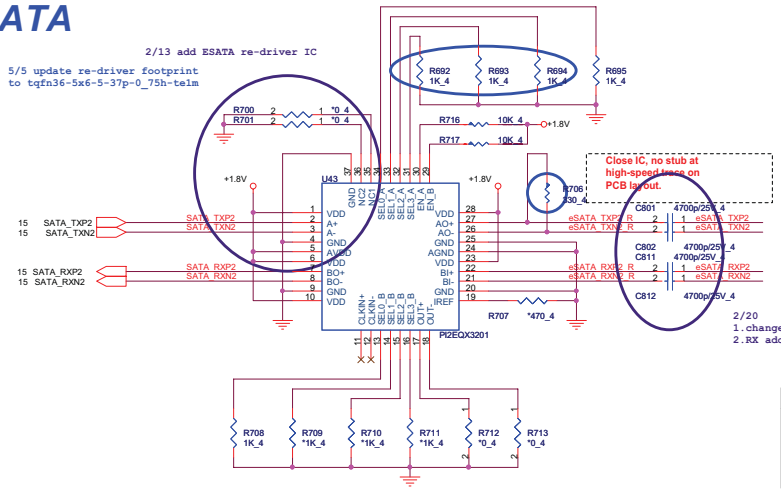


ESATA

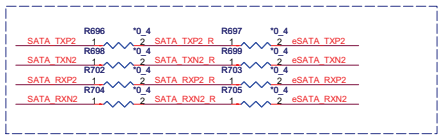
4/14 change R706 from 0 ohm to 330 , stuff R692,R693,R694

2/13 add ESATA re-driver IC

5/5 update re-driver footprint
to tqfn36-5x6-5-37p-0_75h-telm



Option SB to ESATA directly



2/20
1.change C801,C82 from 0.01u to 4.7n
2.RX add C811,C812 4.7n

SEL0_X	SEL1_X	Eq	SEL2_X	Swing	SEL3_X	De-Emphasis
0	0	0dB	0	1.0X	0	0dB
0	1	2.5dB	1	1.2X	1	-3.5dB
1	0	4.5dB				
1	1	6.5dB				

Co-lay ESATA footprint

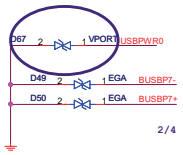
2/29 del R572,R569

2/26 change ESATA conn usb-2006109-11p
update p/n to DFHS11FR021

4/10 change ESATA conn usb-2006109-11p
update p/n to DFHS11FR023

4/10 add D67,D49,D50 for ESATA USB ESD

5/29 change ESATA conn p/n to DFHS11FR027

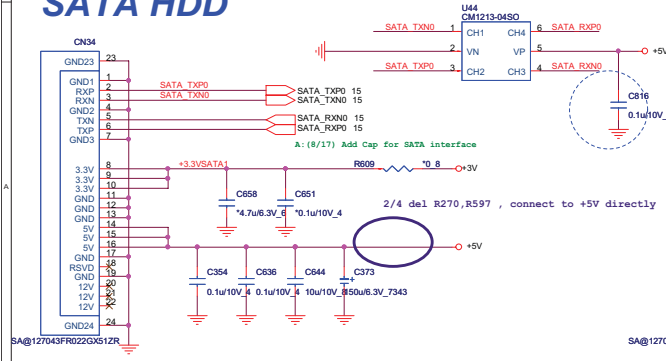


2/4 reserve D67 for CN31

4/17 remove D77~D81 for CN34 , change to U44 CM1213-04SO

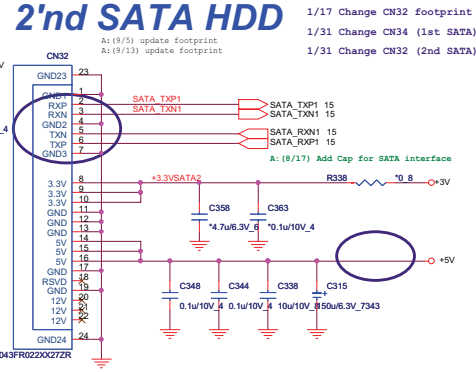
5/5 add C816 0.01u to U44 +5V for ESD

SATA HDD



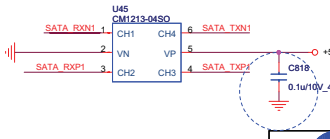
2'nd SATA HDD

A:(9/5) update footprint
A:(9/13) update footprint



1/17 Change CN32(2nd SATA CONN) from DFHS22FR064 to DFHS22FR094
1/17 Change CN32 footprint from SATA-127043FR022XX27ZR-22P-L-H to SATA-127043FR022G285ZR-22P-L
1/31 Change CN34 (1st SATA) P/N from DFHS22FR063 to DFHS22FR082
1/31 Change CN32 (2nd SATA) P/N from DFHS22FR094 to DFHS22FR083

2/4 reserve D82~D86 for CN32(2ND HDD)
4/17 remove D82~D86 for CN32 , change to U45 CM1213-04SO
5/5 add C818 0.01u to U45 +5V for ESD



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	SATA / PATA	2A
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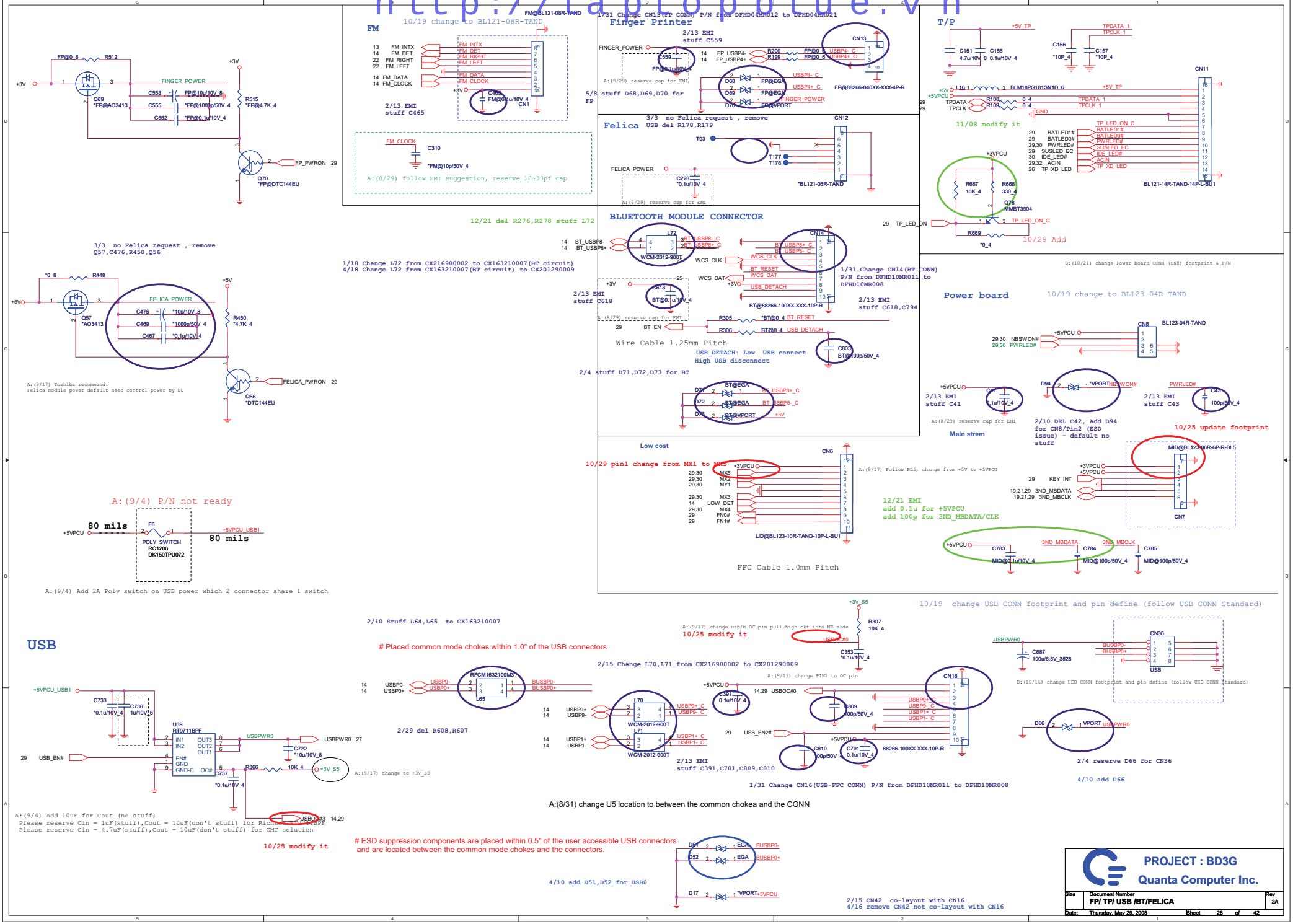
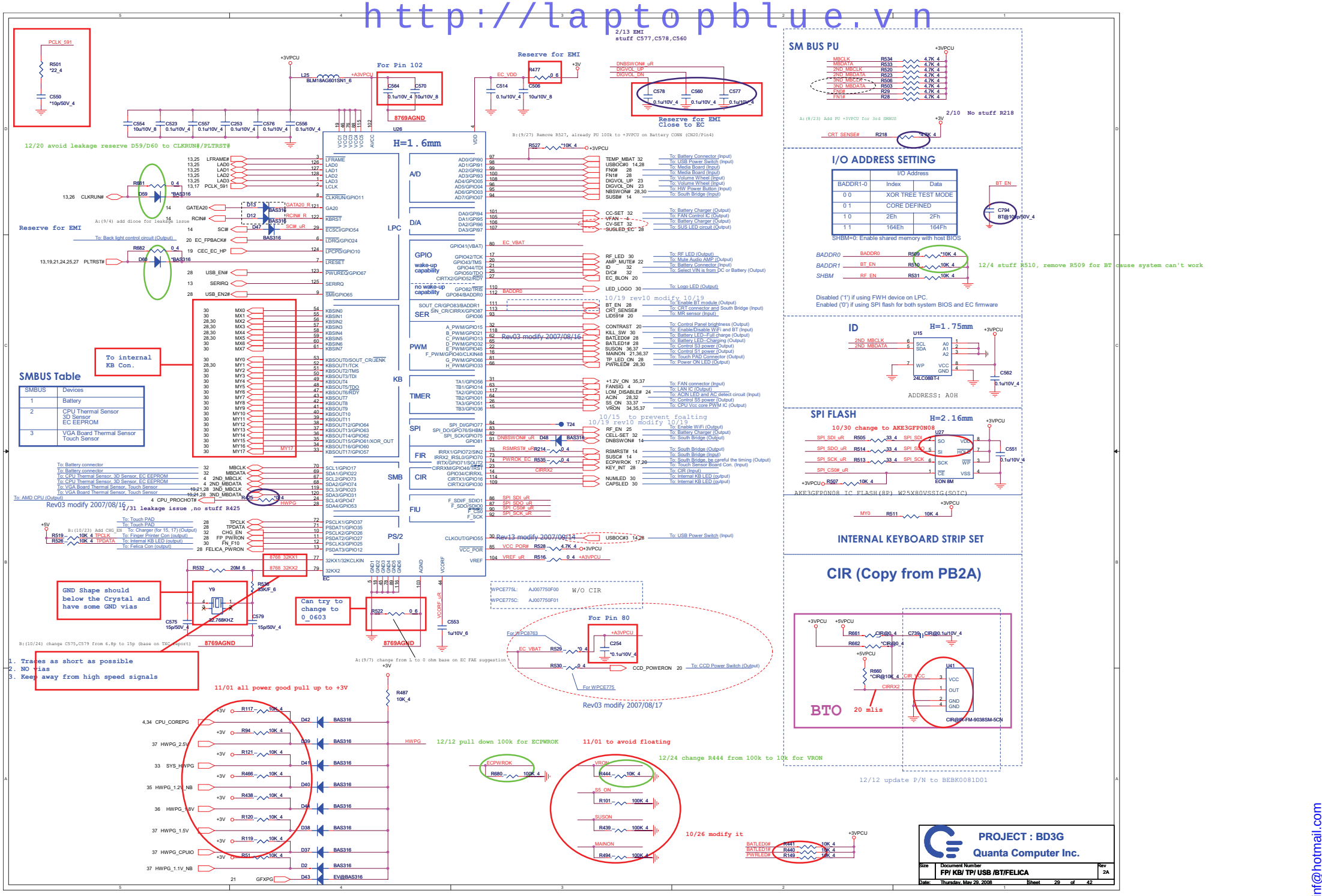
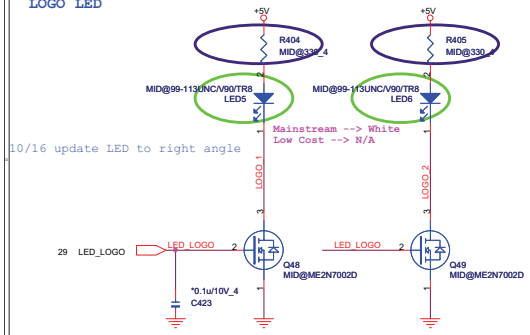




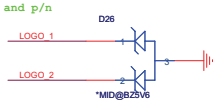
2/1 Change R404,R405 from CS13902JB14 (390 ohm) to CS13302JB21(330 ohm)

LOGO LED



10/16 update LED to right angle

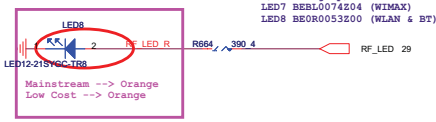
12/7 change LED5,LED6 footprint and p/n



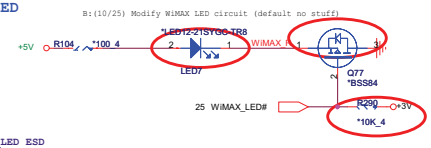
W-LAN&BT

1/18 LED7,8 change footprint from LED12-215YGC-TR8 to LED27-21-BHC-ZL1M2TY-3C

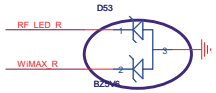
1/18 change p/n
LED7 BEBL0074Z04 (WIMAX)
LED8 BE0R0053Z00 (WLAN & BT)



WiMAX LED

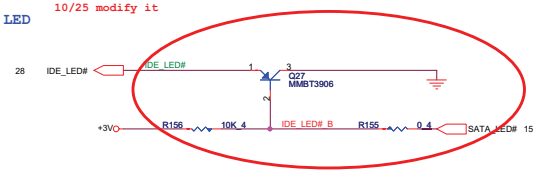


5/8 stuff D53 for RF_LED ESD



IDE LED

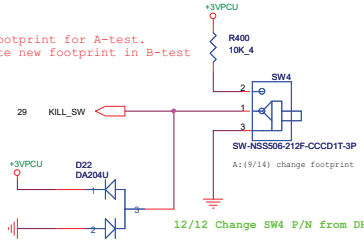
10/25 modify it



Kill SW

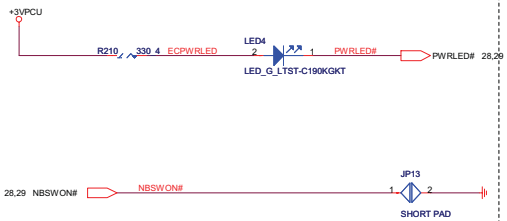
1/18 Change SW4 footprint from SW-NSS506-212F-CCCD1T-3P to SW-NSS506-212F-CCCD1T-3P-BD3A (SMT open issue)

Use old footprint for A-test.
Must update new footprint in B-test

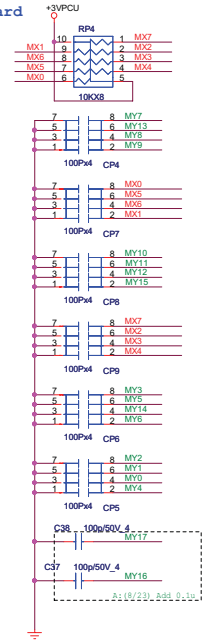


12/12 Change SW4 P/N from DHL00212F05 to DHL00212F07

Jumper & LED (debug use)



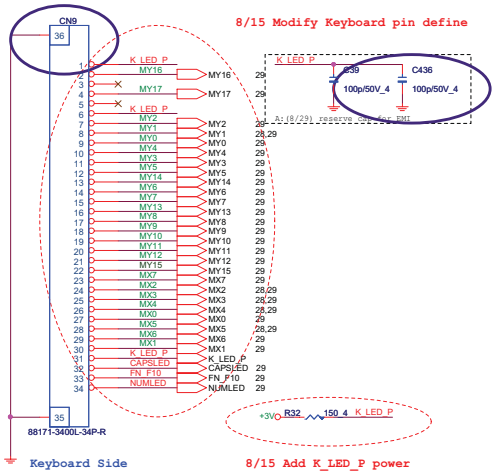
Keyboard



1/18 change footprint from 88171-3400L-34P-L to 91504-340N-34P-L

8/15 Modify Keyboard pin define

2/13 EMI
stuff C39,C436



Keyboard Side

8/15 Add K_LED_P power

1/17 Remove CN10 (Keyboard CONN)

	15"	17"
CAPSLED K_LED_P (Pin 31)	V	V
FN_F10 K_LED_P (Pin 6)	V	
NUMLED K_LED_P (Pin 1)	V	V

A:(8/27) Confirm with EC FAE,
MY no need External PU resister

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Size	Document Number	Rev
	SW/LED/KEYBOARD	2A
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HOLE

Take care NUT P/N base on IV/EV sku

1/18 HOLE 17,18,23 FBBL5004010
change to FBBL5002010

VGA NUT
(BOT)

HOLE15 H-TC315BC236D146P2
HOLE24 H-C236D146P2
HOLE25 H-C236D146P2

10/31 EMI request

2/18 HOLE 15,24,25 FBBD3017010
change to FBBD3021010

MDC NUT
(BOT)

HOLE32 MD@H-C236D146P2

CPU NUT
(BOT)

HOLE17 H-C236D146P2
HOLE18 H-C236D146P2
HOLE23 H-C236D146P2

Mini-PCI-B NUT
(BOT)

HOLE13 H-C236D146P2
HOLE14 H-C236D146P2

2/18 HOLE 13,14 FBBL5008010
change to FBBL5051010

Mini-PCI-A NUT
(BOT)

HOLE28 *H-C236D126P2
HOLE35 *H-C236D126P2

B:(10/17) update footprint

2/18 HOLE 28.35 FBBL5007010
change to FBBL5050010

5/5 remove HOLE28,35 (HD Decoder)

B:(10/17) update footprint

KB NUT
(TOP)

HOLE5 H-C236D146P2
HOLE6 H-C236D146P2

E-SATA NUT
(BOT)

4/21 remove Hole31,37

HOLE30 *H-C236D91P2
HOLE38 *H-C236D91P2
HOLE8 *H-C216D91P2
HOLE9 *H-C216D91P2
HOLE22 *H-C216D91P2
HOLE34 *H-C216D91P2
HOLE39 *H-C216D91P2
HOLE16 *H-CT315

HOLE33 *h-sped110p2
HOLE26 *H-C216D91P2
HOLE40 *H-SPED118P2

A:(9/17) Base ON EMI mail(9/13) Item5

A:(9/12) Base ON EMI mail(9/13) Item1

10/24 update footprint

B:(10/17) update footprint

HOLE44 *H-TS315BC295D118P2-8
HOLE43 *H-TS8C315D118P2-8

HOLE42 *H-C276D118P2-8
HOLE41 *H-C335D118P2-8
HOLE19 *H-C335D118P2-8
HOLE4 *H-C335D118P2-8
HOLE7 *H-C335D146P2-8
HOLE12 *H-C335D118P2-8
HOLE10 *H-C335D118P2-8
HOLE11 *H-C315D118P2-8

B:(10/17) update footprint

HOLE36 *H-C335D118P2-8
HOLE27 *H-C335I248D118P2-8
HOLE29 *H-C335D118P2-8
HOLE21 *H-C335D118P2-8
HOLE20 *H-C335D118P2-8

R85 0_8

10/31 EMI request

RAMP:(1/16) Follow BL5, update Hole footprint (13pcs)

NUT P/N Control Table

	UMA sku	EV sku
HOLE15	FBBL5002010	FBBD3021010
HOLE24	FBBL5002010	FBBD3021010
HOLE25	FBBL5002010	FBBD3021010

Stitch CAP

For fix HyperTransport nets across plane splits

4/17 update HOLE13,14 footprint to H-C236D146P2

CPU_CORE0
C134 0.01u/16V_4
C133 0.01u/16V_4
C130 0.01u/16V_4
C135 0.01u/16V_4

VIN
C768 C769 C770 C771 C772 C773 C774 C775 C776 C777 C778 C779 C780 C781
0.1u/10V_4

EMI CAP.

VIN
C746 C63 0.1u/10V_4
C87 C137 C106 C97 C119 C169 0.1u/10V_4

VIN
C529 C270 C472 C758 C755 C756 C31 C30 C74
0.1u/10V_4

+3V
C244 C243 C204 C202 C162 C138 C749 C112 C742
0.1u/10V_4

+3V
C12 C85 C2 C416 C451 C1 C71 C72 C50 C62
0.1u/10V_4

+3V
C450 C454 C224 C480 C409 C460 C455
0.1u/10V_4

+3VPCU
C240 C549
0.1u/10V_4

+3VSUS
C229 C518 C128
*0.1u/10V_4

+5VPCU
C83 C161 C132 C165 C760 C205
0.1u/10V_4

3/3 EMI request add C813,C814

+5V
C464 C745 C51 C3 C759 C59
0.1u/10V_4

+1.5V
C813 C814
0.1u/10V_4

+3VPCU
C164 C547 C122 C748 C32 C33 C75 C34 C70
0.1u/10V_4

+1.8V
C273 C213 C574 C107 C146
0.1u/10V_4

+1.2V
C528 C163 C127 C585 C584
0.1u/10V_4

+5V
C139 C271 C462 C442 C171
0.1u/10V_4

+5VPCU
C16 C757 C45
0.1u/10V_4

+1.8V
C599 C385 C283 C203 C189 C176 C173 C153
0.1u/10V_4

PROJECT : BD3G
Quanta Computer Inc.

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	HOLE/EMI CAP/ESD PAD	2A
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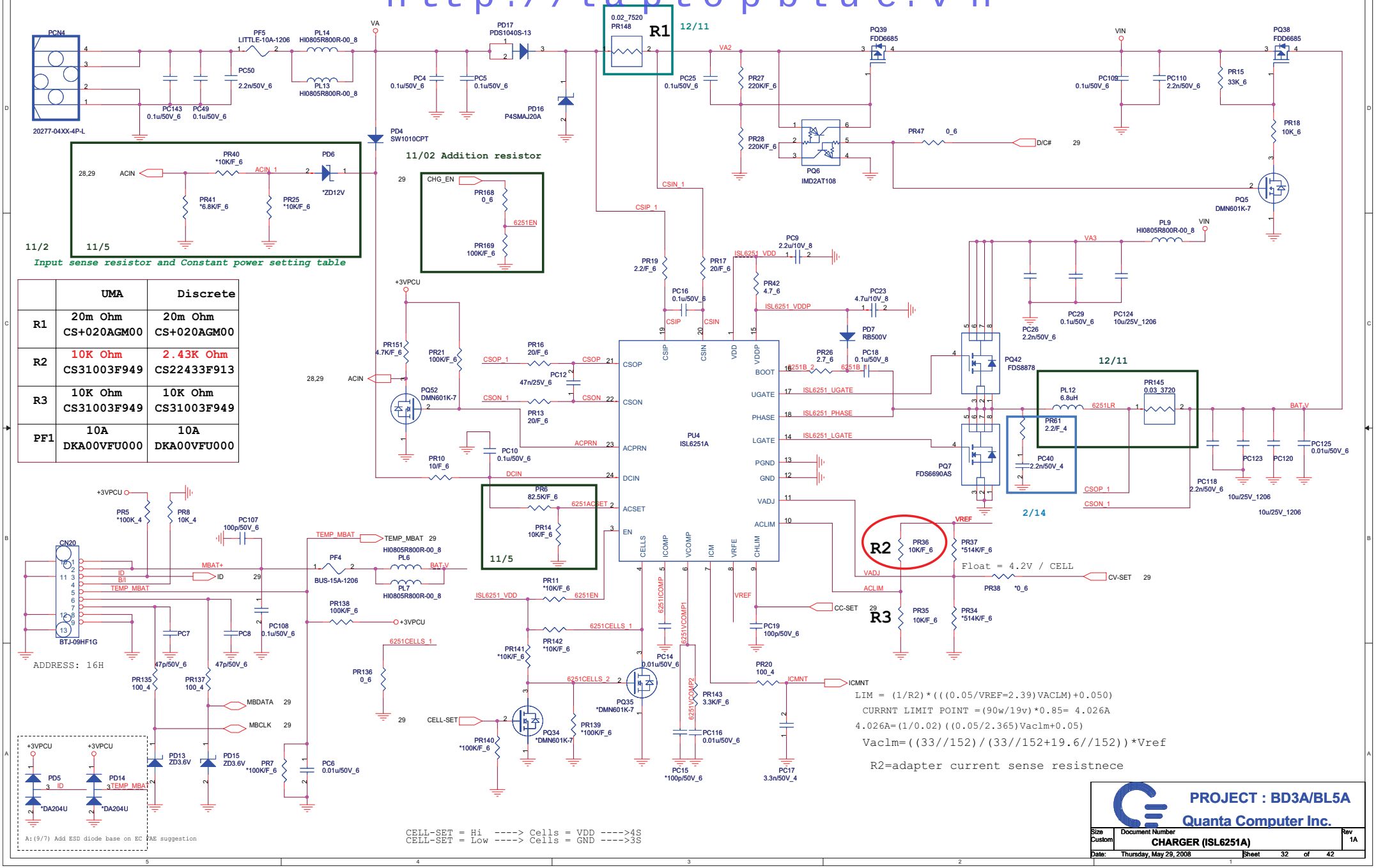
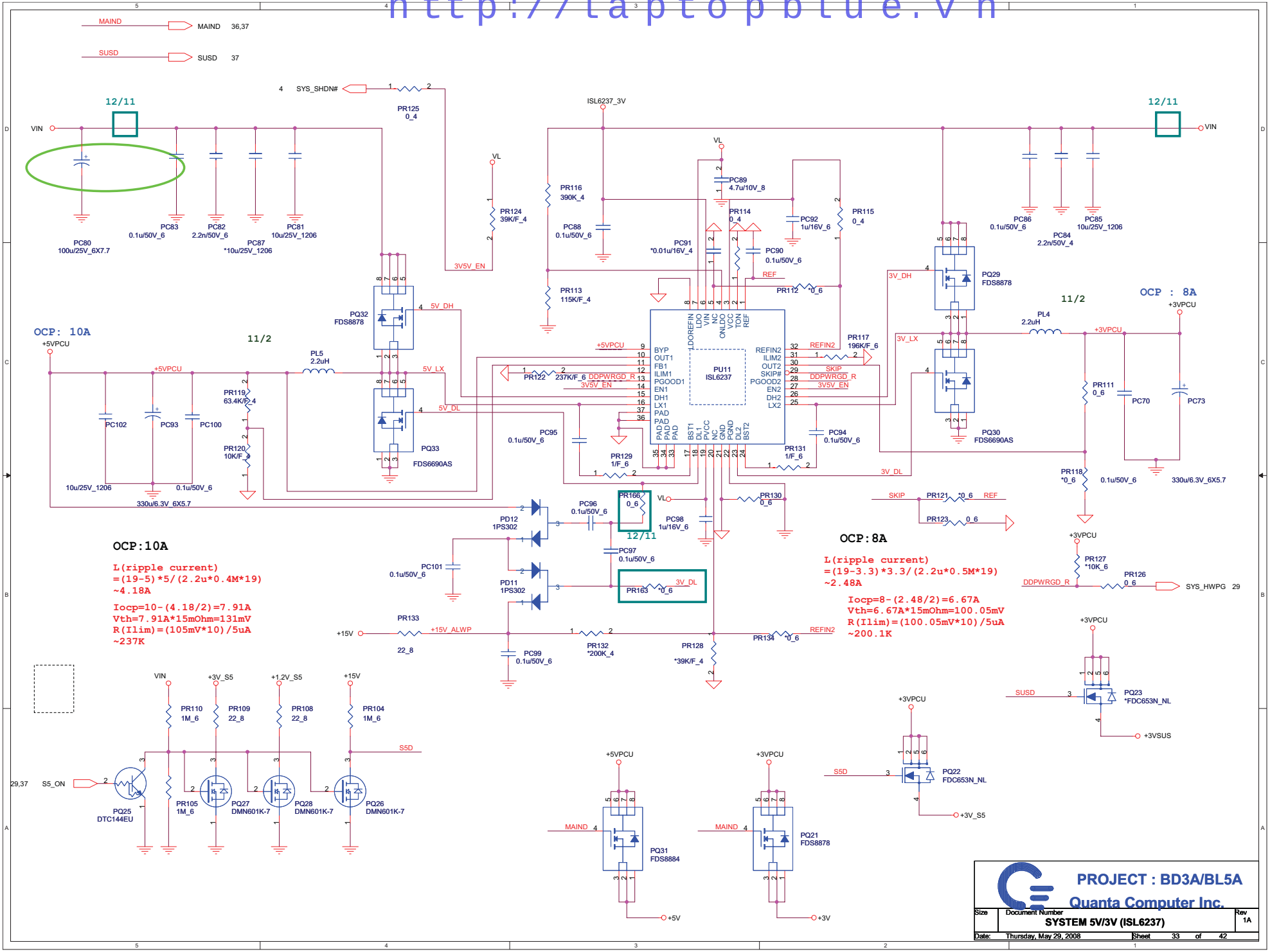


	UMA	Discrete
R1	20m Ohm CS+020AGM00	20m Ohm CS+020AGM00
R2	10K Ohm CS31003F949	2.43K Ohm CS22433F913
R3	10K Ohm CS31003F949	10K Ohm CS31003F949
PF1	10A DKA00VFU000	10A DKA00VFU000



OFS/VFIXEN	Offset & Droop	SVI	VFIX
GND	O	O	X
+3.3V	X	X	O
+5V	X	O	X

Metal VID Codes

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

3A

20A

20A

Pin 49 is GND Pin

PU3
ISL6265

Close to CPU socket

Parallel

Close to CPU socket

4/10 add PC191,PC193

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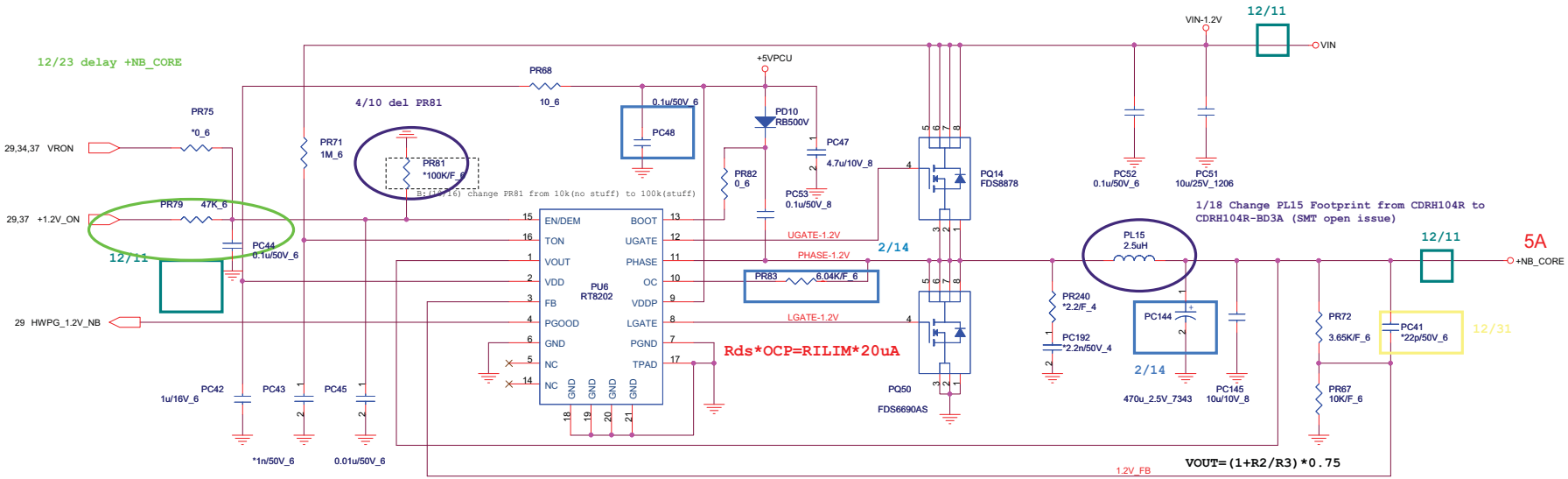
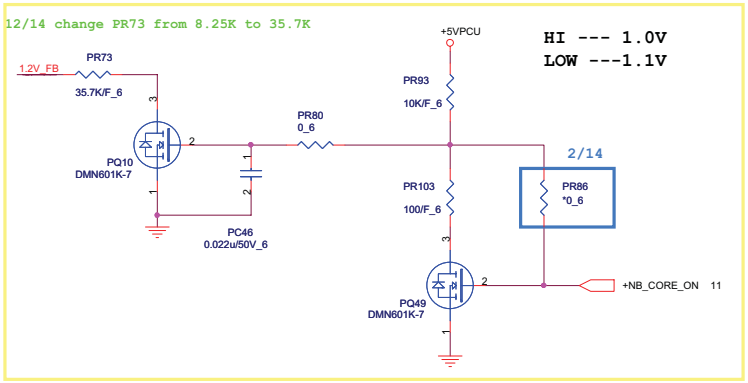


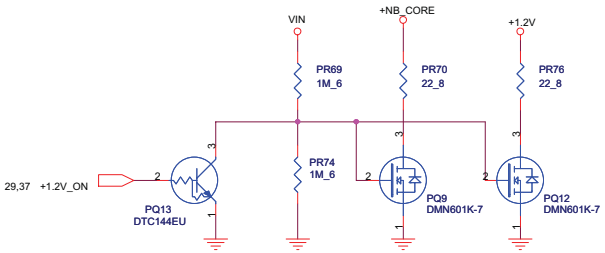
TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

6A OCP --- OC=4.53K
FDS6690AS Rds=15mOhm



12/14 del +1.35V_VDDHTTX
PU15
PC180,PC182,PC179
PR227,PR226,PR225



PROJECT : BD3A/BL5A
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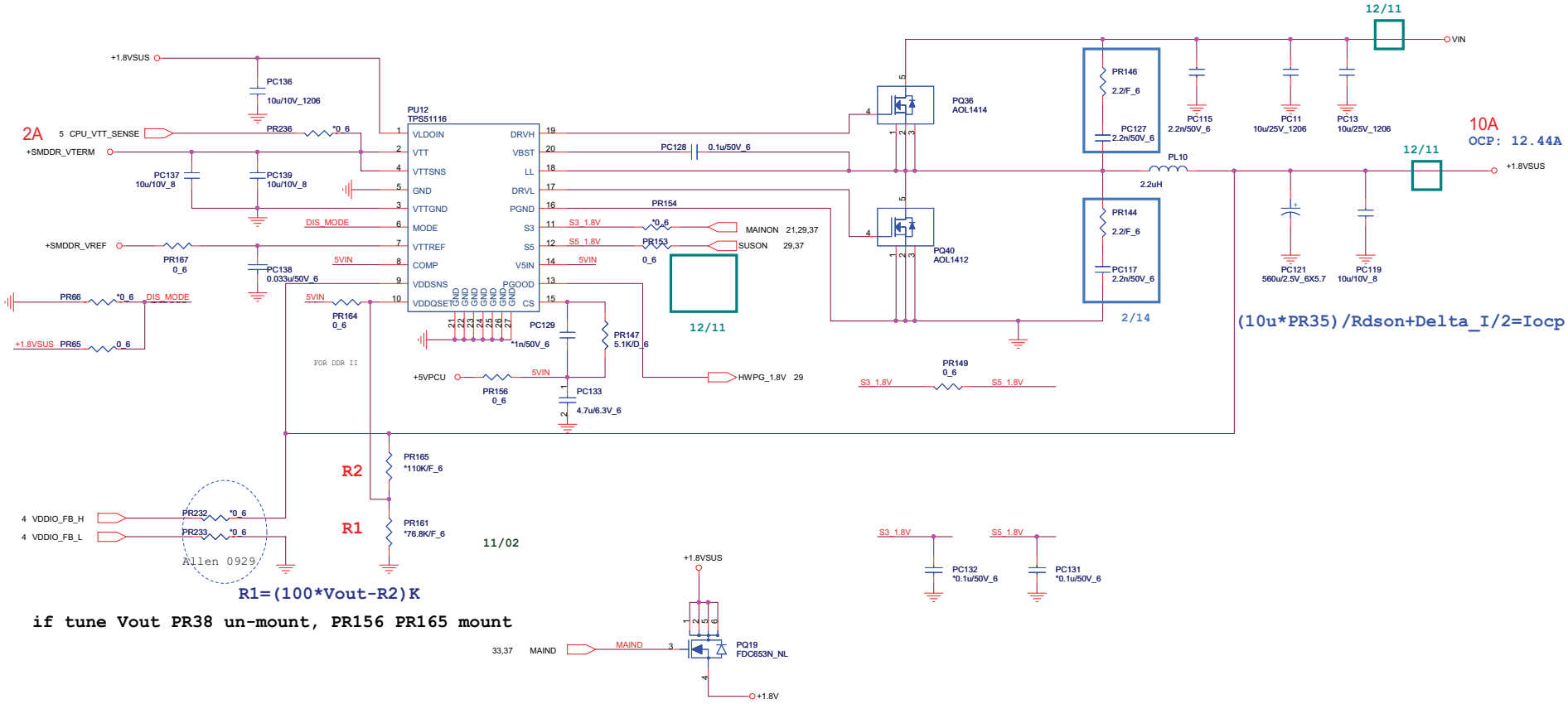
Size	Document Number	Rev
	NB_VCC (RT8202)	1A
Date: Thursday, May 29, 2008	Sheet 35 of 42	



PROJECT : BD3A/BL5A
Quanta Computer Inc.

Size	Document Number	Rev
	DDR 1.8V(TPS51116)	1A
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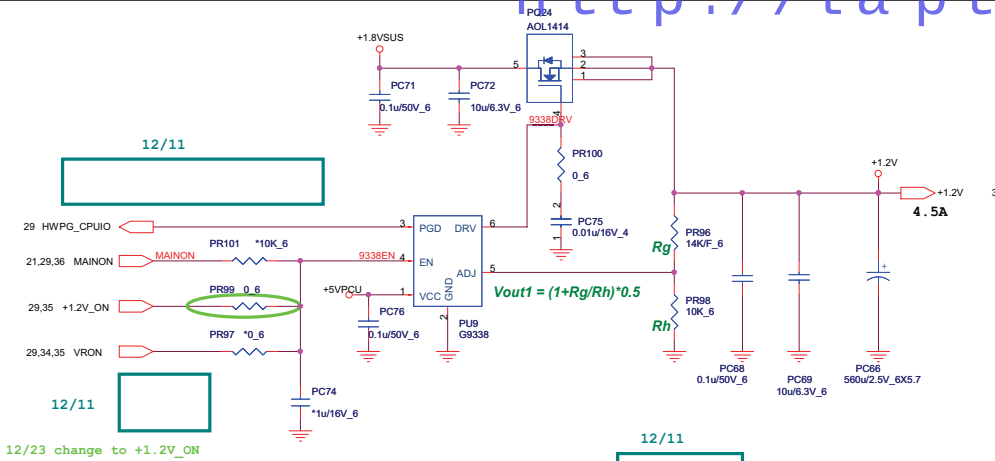

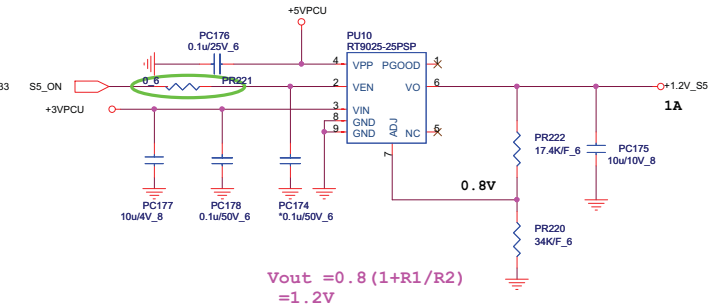

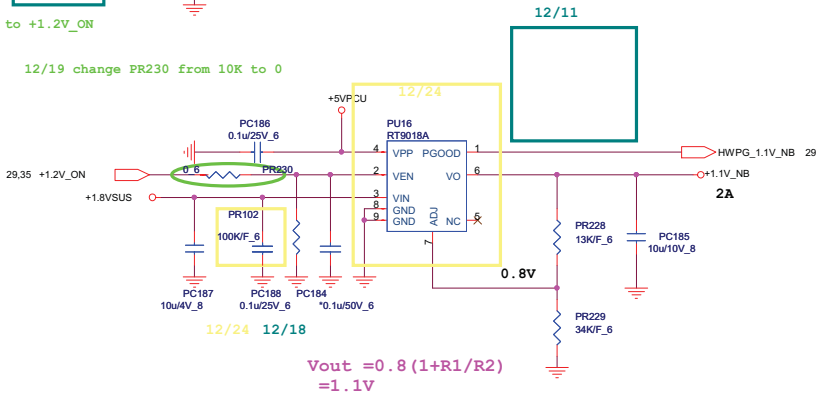

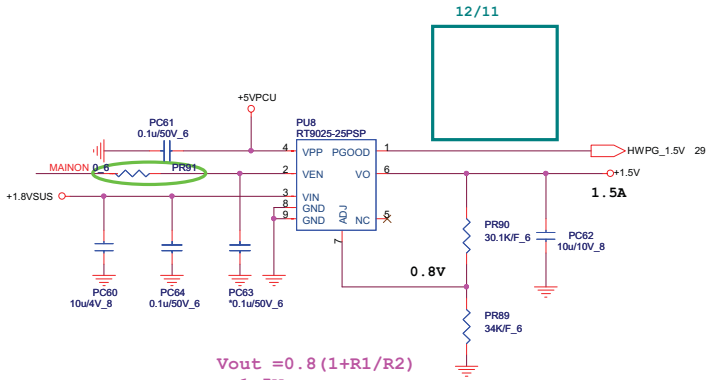

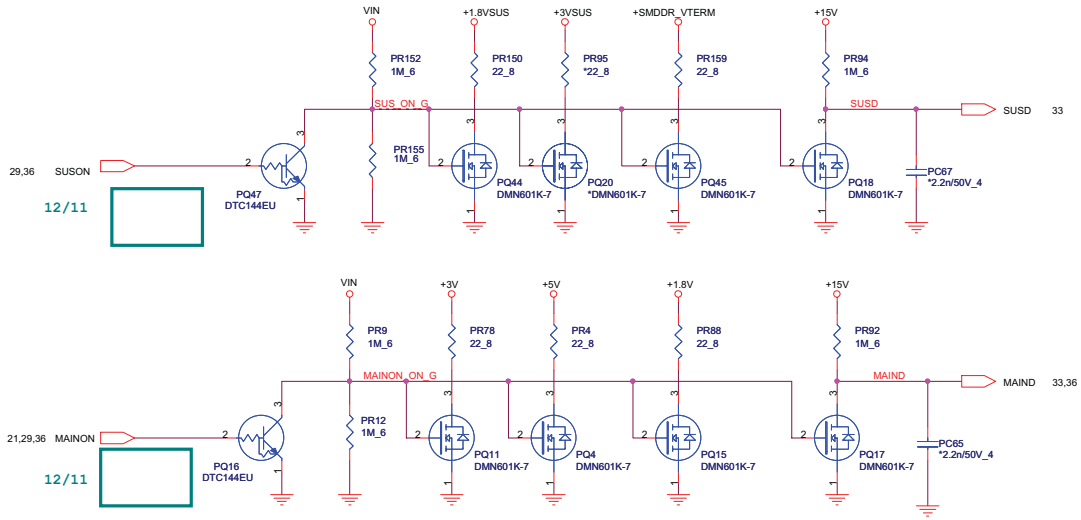

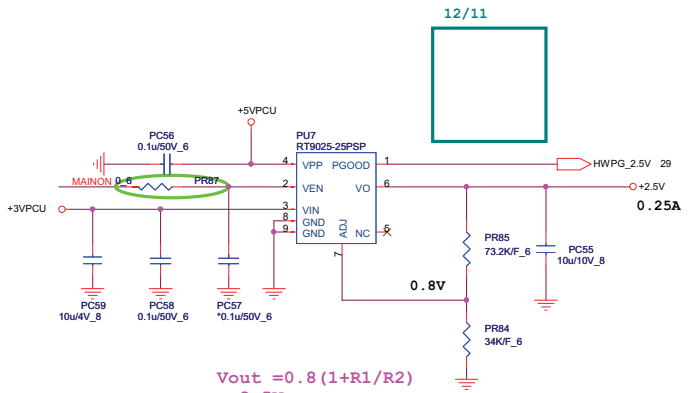

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Quanta Computer Inc.

Size	Document Number	Rev
	Discharge (1.25V/1.5V)	1A
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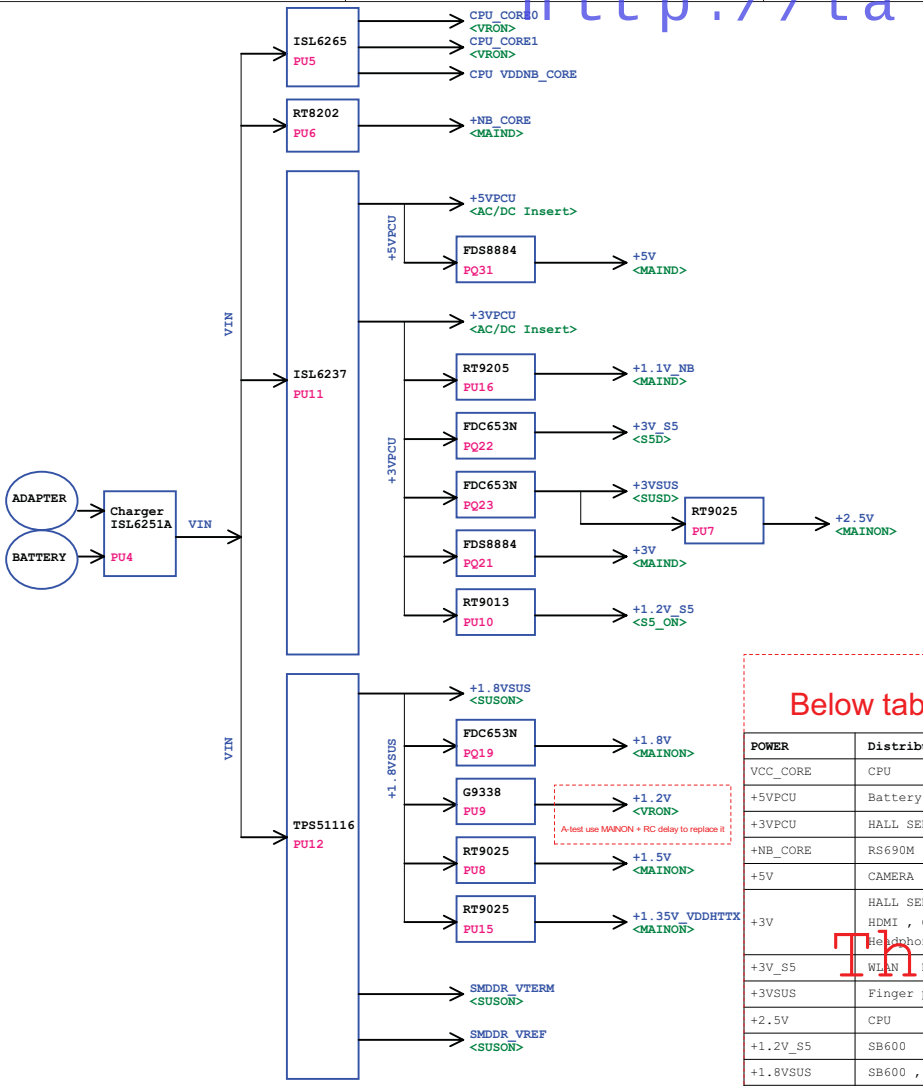

Below table need be modify (waiting other schematic ready)

POWER	Distribution
VCC_CORE	CPU
+5VPCU	Battery LED , Power LED , USB , CIR , RTC
+3VPCU	HALL SENSOR , Battery LED , RF LED , kill SW , Jumper LED , KB , Power Board , EC , ID , SPI Flash , CIR
+NB_CORE	RS690M
+5V	CAMERA , Card Reader LED , ODD/HDD LED , Felica , T/P , T/sensor , CRT , HDMI , SB600 , CPU FAN , MXM , Headphone , EC , INT SPK AMP
+3V	HALL SENSOR , LCD PANEL , LVDS , WLAN , HD Decoder , NEW CARD , KB , KB LED , XD LED , Blue tooth , Touch sensor , Card Reader (OZ129) , ODD/HDD , HDMI , CRT , TVOUT , REQUIRED STRAPS , DEBUG STRAPS , SB600 , RS690M , DDR , CPU Thermal monitor , CPU FAN , CLK , MXM , VR , FM Tuner MDC , Headphone , EC , LAN , Codec(CX 20561)
+3V_S5	WLAN , NEW CARD , SB600 , MXM , LAN
+3VSUS	Finger print , SB600
+2.5V	CPU
+1.2V_S5	SB600
+1.8VSUS	SB600 , DDR , CPU , HDT
+1.8V	SB600 , LCD , LVDS , RS690M
+1.2V	SB600 , RS690M , CPU , WLAN , HD Decoder , NEW CARD
+SMDDR_VTERM	DDR , CPU
+SMDDR_VREF	DDR
+5V_S5	

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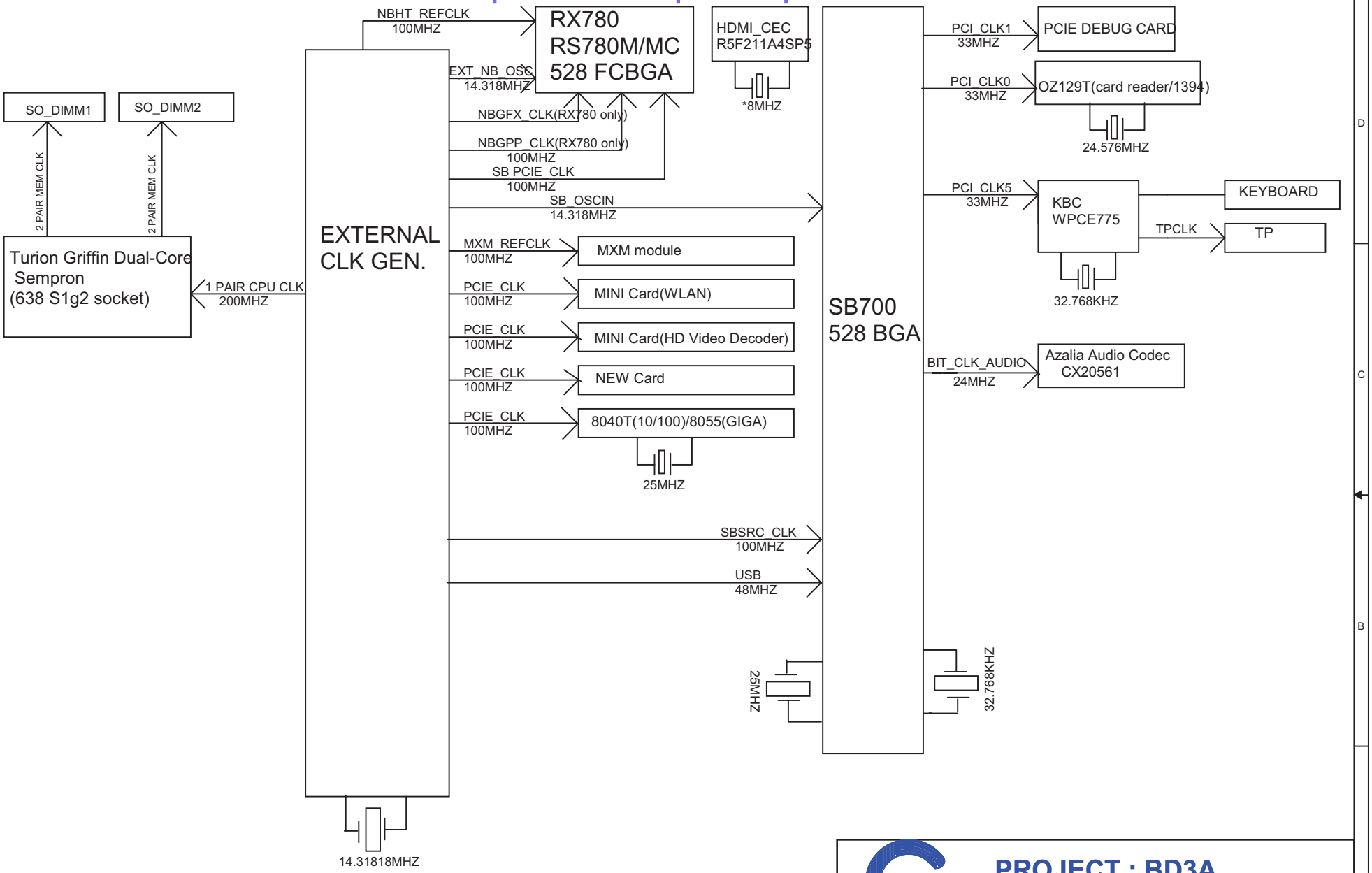

PROJECT : BD3A

Quanta Computer Inc.

Size	Document Number	Rev
	Clock distribution diagram	2A
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Model	REV	DATE	CHANGE LIST	NOTE
BD3G	A1A	2007	FIRST RELEASED : Import BOM ECN	ECN Release
	B2A	20071008	PAGE23:Reverse U42,C761 for VR	Circuit modify
		20071008	PAGE28:Add R667,R668,Q78 for TP_LED	Circuit modify
		20071204	PAGE04:Reverse C762 for AMD engineer CPU use	Circuit modify
		20071204	PAGE19:update CN25 HDMI footprint to HDMI-C12816-119A5-L-19P-V-BL5-1	Circuit modify
		20071204	PAGE15:change BOARD ID3 from GEVENT7 to GPIO48	Circuit modify
		20071204	PAGE14:change BOARD ID PD value from 10K to 1K(R227,R228,R229,R248,R343,R236)	Circuit modify
		20071204	PAGE29:Stuff R510, no-stuff R509 (slove BT module can't bring up issue)	Circuit modify
		20071204	PAGE20: modify display on ckt to avoid flash when into S3/S4/S5 (add Q78,Q80,R670,del Q41,R388)	Circuit modify
		20071207	PAGE19:update CN25 HDMI footprint to HDMI-C12816-119A5-L-19P-H-BD3	Circuit modify
		20071207	PAGE32:update ACIN design	Circuit modify
		20071207	PAGE24:Change R449(0 ohm) to D56(Diode) for leakage issue (3VPCU to 3V_S5)	Circuit modify
		20071207	PAGE23: Slove Audio issue:When plug in-out headphone, headphone has bo sound. 1. Change R652&R651 to C763,C764(10U/6.3V 0603)	Circuit modify Circuit modify Circuit modify
		20071207	PAGE22: Remove D19 to slove Audio issue Switch Mute to Un-mute, sound will delay about 2 seconds.	Circuit modify
		20071207	PAGE14: add D57,D58 to avoid voltage leakage	Circuit modify
		20071207	PAGE30:update LED5,LED6 footprint and PN	Circuit modify
		20071207	PAGE04:add R671~R679 for AMD request	Circuit modify
		20071208	PAGE03:change C223 C225 from 10p to 33p PAGE15:change C257 C258 from 10p to 27p PAGE26:change C380 C381 from 22p to 18p	
		20071210	PAGE25:Change New card footprint to NCARD-13180151-T-26P-L-BL5S	
		20071210	PAGE22:stuff R372 for FM	
		20071211	update power	
		20071212	PAGE29: Change U41(CIR) from BEBK0081D00 to BEBK0081D01	
		20071212	PAGE18: Change CN22(S-Video) from DFMD04FR296(Yellow Color) to DFMD04FR006(Black Color)	
		20071212	PAGE30: Change SW4 P/N from DHL00212F05 to DHL00212F07	
		20071212	PAGE31: Update Hole43 H-TSBC315D118P2, Hole 44 H-TS315BC295D118P2	
		20071212	PAGE29: pull down 100k R680 for ECPWROK	
		20071212	A11 to A12 implemen PAGE12: Del L15 stuff L36 PAGE16: Del R234 stuff R235 PAGE35: Del PU15,PC180,PC182,PC179PR227,PR226,PR225, Change PR73 from 8.25K to 35.7K	
		20071220	PAGE23: Slove GPRS noise 1. stuff R386/R387/C404/C405 to 0.1U 2. Change L44/41 to BK1608LL121	
		20071220	PAGE29: avoid leakage reserve D59/D60 to CLKRUN#/PLTRST#	
		20071221	PAGE18:add 27p(C790~C793) for TV_Y/G , TV_C/R	
		EMI	PAGE21:stuff C568,C548 PAGE22:stuff R399,R379 PAGE23:Change L43/44 to BK1608LL121 PAGE24:add L74,C766,C767,C789,C788 for +2.5V_1.8V_LAN,add L73 for +1.2V_LAN PAGE26:add 0 ohm and 22p for SD/MS CLK , R308~R329 0ohm(CS00002JB38) change to 33ohm(CS03302JB29), remove RN34,RN35, stuff L68,L69 for 1394 PAGE28:del R276,R278 stuff L72 , del R613,R612,R624,R626 stuff L70,L71 , add 0.1u for +5VPCU add 100p for 3ND_MBDATA/CLK PAGE31:stuff all 0.1 cap	
		20071221	update power	
		20071222	PAGE11: stuff R48 2.2K for power play	
		20071222	PAGE24: Per cost down remove LAN eeprom,stuff R381,remove U21,R380,R378	
	C3A	20080102	PAGE14: NEW_DET# change from Geven3# to GPM1#	
		20080117	Update RX781	
		20080117	PAGE13:Modify RTC circuit. R301,R302 change from 8.66k to 2k. R332 change from 4.7K to 6.8K	
		20080117	PAGE13:Change RTC Battery from VARTA (AHL03001441) to MATSUSHITA (AHL03002005)	
		20080117	PAGE19:Change back HDMI connector(CN25) footprint from HDMI-C12816-119A5-L-19P-H-BD3 to HDMI-C12816-119A5-L-19P-H-BL5(SMT open issue)	
		20080117	PAGE20:for engery star add R684 connect to EC pin27	
		20080117	PAGE24:Change CN28 (RJ45 CONN) from DFTJ12FR024 to DFTJ12FR035	
		20080117	PAGE27:Change CN32(2nd SATA CONN) from DFHS22FR064 to DFHS22FR094	
		20080117	PAGE27:Change CN32 footprint from SATA-127043FR022XX27ZR-22P-L-H to SATA-127043FR022G285ZR-22P-L	
		20080117	PAGE30:Remove CN10 (Keyboard CONN)	
		20080117	PAGE21:Remove R492,R517, Short CN27/Pin189,190 to VIN directly.	
		20080118	PAGE28:Change L72 from CX216900002 to CX163210007(BT circuit)	
		20080118	PAGE08:Change CN19 footprint from DDR-C-292564-200P to DDR-C-292564-200P-BD3A (SMT open issue)	
		20080118	PAGE08:Change CN23 footprint from DDR-C-1734071-200P to DDR-C-1734071-200P-BD3A (SMT open issue)	
		20080118	PAGE30:Change SW4 footprint from SW-NSS506-212F-CCCD1T-3P to SW-NSS506-212F-CCCD1T-3P-BD3A (SMT open issue)	
		20080118	PAGE23:Change CN43 footprint from MDC-1-179373-2-12P-RUV to MDC-1-179373-2-12P-RUV-BD3A (SMT open issue)	
		20080118	PAGE35:Change PL15 Footprint from CDRH104R to CDRH104R-BD3A (SMT open issue)	
		20080118	PAGE22:Add R685 for VISTA WHQL circuit	
		20080118	PAGE24: Change RJ45 footprint from LAN-100073FR012G101ZL-12P to rj45-c100s7-10806-l-12P	
		20080118	PAGE31:HOLE 17,18.23 FBBL5004010 change to FBBL5002010	

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	Change list	2A

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Model	REV	DATE	CHANGE LIST	NOTE
BD3G	C3A	20080118	PAGE30:change footprint from 88171-3400L-34P-L to 91504-340N-34P-L	Circuit modify
		20080118	PAGE30:LED7,8 change footprint from LED12-21SYGC-TR8 to LED27-21-BHC-ZL1M2TY-3C	Circuit modify
		20080118	PAGE30:change p/n LED7 BEBL0074Z04 (WIMAX),LED8 BE0R0053Z00 (WLAN & BT)	Circuit modify
		20080131	PAGE31:update HOLE42,41,19,4,7,12,10,11,36,27,29,21,20,43,44	Circuit modify
		20080131	voltage leakage issue	Circuit modify
			PAGE04:modify CPU_PROCHOT# ckt (add R687, no stuff R686,R425), CPU_LDT_REQ#_CPU ,CPU_PWRGD connect to +1.8V	Circuit modify
			PAGE11:remove Q5,Q3,R83,R80,R97,stuff R88,R77	Circuit modify
			PAGE14:BOARD_ID4 change from GPIO66 to GPIO3	Circuit modify
		20080131	PAGE14:NEW CARD hot plug issue ,NEW_DET# change from GEVEN5# to GPM1# (SB700 A12 Errata)	Circuit modify
		20080131	PAGE19: DEL L56,L57,L58,L59,R465,R474,R493,R495,R486,R488,R478,R483,C226,C227 for HDMI circuit	Circuit modify
		20080131	PAGE25: add +3V to CN21 pin39,41	Circuit modify
		20080131	PAGE18: Change L4,L5,L6 to CX8BA470003 to meet CRT spec	Circuit modify
		20080131	PAGE19: Change U11 from ARBL5SV0000 to ARBL5MV0000	Circuit modify
		20080131	PAGE26:According to customer request, we can't stuff C782 (22pF) in SD/MS_CLK.	Circuit modify
		20080131	PAGE25: Change R573 from 28.7K to 0 ohm, Remove C628 for NEW card some device can't work normal	Circuit modify
		20080131	PAGE14: Change R350 from 1K to 0 ohm (Slove VCCRTC can't reach 0V when clear CMOS.)	Circuit modify
		20080131	PAGE26: Change CN33(5 in 1 card CONN) P/N from DFHS38FR003 to DFHS38FR005	Circuit modify
		20080131	PAGE27: Change CN34 (1st SATA) P/N from DFHS22FR063 to DFHS22FR082	Circuit modify
		20080131	PAGE27: Change CN32 (2nd SATA) P/N from DFHS22FR094 to DFHS22FR083	Circuit modify
		20080131	PAGE20: Change CN5 (I-MIC)P/N from DFHD02MR003 to DFHD02MR016	Circuit modify
		20080131	PAGE22: Change CN39(I-MIC CONN) P/N from DFHD02MR003 to DFHD02MR016	Circuit modify
		20080131	PAGE22: Change CN17(SPK CONN) P/N from DFHD04MR012 to DFHD04MR021	Circuit modify
		20080131	PAGE28: Change CN16(USB-FFC CONN) P/N from DFHD10MR011 to DFHD10MR008	Circuit modify
		20080131	PAGE28: Change CN13(FP CONN) P/N from DFHD04MR012 to DFHD04MR021	Circuit modify
		20080131	PAGE28: Change CN14(BT CONN) P/N from DFHD10MR011 to DFHD10MR008	Circuit modify
		20080201	PAGE22: Change INT-SPK AMP GAIN VALUE. Change R623,R625 from 9.1k to 5.1k 1%,Change R620,R621 from 10k to 16k 1%	Circuit modify
		20080201	PAGE30: Change R404,R405 from CS13902JB14 (390 ohm) to CS13302JB21(330 ohm)	Circuit modify
		20080201	RS780M A13 Errata	Circuit modify
			PAGE11:change R103 from 150 to 140 CS11402FB01	Circuit modify
			PAGE18:RS780M A13 R8 ---> 140 CS11402FB19,MXM R8 ---> 150 CS11502FB21	Circuit modify
		20080201	PAGE19: change HDMI SCL/SDA pull res R168,R171,R163,R170 to 4.7K ,change R1,R2 to 6.8K	Circuit modify
		20080201	PAGE20: change Panel SDA/SDC pull res R412,R410 from 39K to 4.7K	Circuit modify
		20080204	ESD solution	Circuit modify
			PAGE23: add Varistor D63,D64,D65 on SPDIF_OUT/HP_JD/+3V_SPD	Circuit modify
			PAGE28: reserve D66 for CN36 , reserve D68,D69,D70 for FP , stuff D71,D72,D73 for BT	Circuit modify
			PAGE20:reserve D74,D75,D76 for CCD ,stuff D87 for LID switch	Circuit modify
			PAGE27:del R270,R597 , connect to +5V directly ,reserve D77~D81 for CN34(1ND HDD) ,reserve D82~D86 for CN32(2ND HDD) ,reserve D67 for CN31	Circuit modify
			PAGE26:reserve D88~D91 for 1394	Circuit modify
			PAGE04:reserve D92,D93 for FAN , reserve C795,C796 change R122 to 0 0603	Circuit modify
			PAGE13,19,21,25:reserve C797~800 for PLTRST#	Circuit modify
		20080204	PAGE04: pull up R691 CPU_BDREQ# to avoid noise cause system shut down	Circuit modify
		20080205	PAGE23:Change R714,R715 from 10uF to 0 ohm (Audio HP circuit)	Circuit modify
		20080210	PAGE18,29: DEL D4,D5 footprint and DEL CRT_SENSE# net, No stuff R218	Circuit modify
		20080210	PAGE28: DEL C42, Add D94 for CN8/Pin2 (ESD issue) - default no stuff	Circuit modify
		20080210	PAGE28: Change L70,L71 from CX216900002 to CX163210007	Circuit modify
		20080210	PAGE28: Stuff L64,L65 to CX163210007	Circuit modify
		20080213	PAGE27: Add ESATA re-driver IC	Circuit modify
		20080213	PAGE25: Change the footprint of R33 and R330 from 1206 to 0805	Circuit modify
		20080213	EMI solution	Circuit modify
			PAGE18: C4,C7,C10,C5,C8,C11 change from 10p to 6.8p	Circuit modify
			PAGE28: stuff C391,C701, C559 ,C228,C465,C618,C41,C43, C618,C794,C809,C810	Circuit modify
			PAGE20: stuff C427~C432	Circuit modify
			PAGE30: stuff C39,C346	Circuit modify
			PAGE29: stuff C577,C578,C560	Circuit modify
			PAGE12: stuff C804~C807 for +NB_CORE	Circuit modify
			PAGE25: stuff C40,C36,C54,C58,C289,C352,C319,C272 for WL	Circuit modify
			PAGE19: stuff C808 for HDMI	Circuit modify
			PAGE15: stuff C375,C366 for SB HW MONITOR	Circuit modify
			PAGE22: stuff R627	Circuit modify
			PAGE26: change R683 from 0 to 33 ohm	Circuit modify
		20080214	UPDATE POWER	Circuit modify
		20080215	PAGE28: CN42 co-layout with CN16	Circuit modify
		20080215	PAGE31: Remove R98,R145,R118 Hole15,17,18	Circuit modify
		20080215	PAGE28: Change L70,L71 from CX216900002 to CX201290009	Circuit modify
		20080218	PAGE31: HOLE 15,24.25 FBBD3017010 change to FBBD3021010	Circuit modify
		20080218	PAGE31: HOLE 28.35 FBBL5007010 change to FBBL5050010 , HOLE 13,14 FBBL5008010 change to FBBL5051010	

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	Change List02	3C

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Model	REV	DATE	CHANGE LIST	NOTE
BD3G	C3A	20080218	PAGE04: G781 reverse R718 0 ohm for Griffin CPU	Circuit modify
		20080219	PAGE04: change G781 to G786P81U	Circuit modify
		20080220	PAGE27:1.change C801,C82 from 0.01u to 4.7n, 2.RX add C811,C812 4.7n	Circuit modify
		20080222	PAGE15:change SATA ODD from port3 to port4 (solve ODD post detect fail)	Circuit modify
		20080226	PAGE27:change ESATA conn usb-2006109-11p,update p/n to DFHS11FR021	Circuit modify
		20080227	update power include EMI	Circuit modify
		20080229	del co-layout parts	Circuit modify
			RN34,RN35,R608,R607,R572,R569	Circuit modify
		20080303	PAGE14: del Mini card USB10,Felica USB5 , change BT to port5 , ESATA to port 10	Circuit modify
		20080303	PAGE25: MINI PCI II no need USB , change USB10 to ESATA .and del R169,R188	Circuit modify
		20080303	PAGE28: no Felica request , remove USB del R178,R179,remove Q57,C476,R450,Q56	Circuit modify
		20080303	PAGE31: EMI request add C813,C814	Circuit modify
		20080410	PAGE17: change R150 to R152 for power sequence	Circuit modify
		20080410	PAGE26: add D88~D91 for 1394 ESD	Circuit modify
		20080410	PAGE27: change ESATA conn usb-2006109-11p update p/n to DFHS11FR023	Circuit modify
		20080410	PAGE27: add D67,D49,D50 for ESATA USB ESD	Circuit modify
		20080410	PAGE28: add D51,D52, D66 for USB0	Circuit modify
		20080410	PAGE34: add PC191,PC193 for CPU core	Circuit modify
		20080410	PAGE35: del PR81	Circuit modify
		20080410	PAGE27: remove Flash card ckt	Circuit modify
		20080416	PAGE13: change RTC pad location to G1	Circuit modify
		20080416	PAGE14: pull up USB_OC5# R719	Circuit modify
		20080416	PAGE18: update footprint to sv-030018fr004s100fr-4p-h-bl5m	Circuit modify
		20080416	PAGE23: update footpritnt to knob-xre094-3p-bl5m	Circuit modify
		20080416	PAGE28: remove CN42 not co-layout with CN16	Circuit modify
		20080416	PAGE31: update HOLE13,14 footprint to H-C236D146P2	Circuit modify
		20080417	PAGE27: remove D77~D81 for CN34 , change to U44 CM1213-04SO(AL001213001) ,remove D82~D86 for CN32 , change to U45 CM1213-04SO	Circuit modify
		20080418	PAGE28: Change L72 from CX163210007(BT circuit) to CX201290009	Circuit modify
		20080421	PAGE31: remove Hole31,37	Circuit modify
		20080421	no stuff +3VSUS component	Circuit modify
			PAGE31: no stuff C229,C518,C128	Circuit modify
			PAGE33: no stuff PQ23	Circuit modify
			PAGE37: no stuff PR95,PQ20	Circuit modify
		20080424	PAGE16: IDE/FLASH not use ,remove C287,C288,C297,C293,C294	Circuit modify
		20080424	PAGE16: internal clk not use ,remove C332,C330,C327,C331, change L28 to 0 ohm	Circuit modify
		20080424	To meet ESATA SI	Circuit modify
			PAGE27: change R706 from 0 ohm to 330 , stuff R692,R693,R694	Circuit modify
				Circuit modify
		20080424	PAGE16: remove C762 to meet PWRGD timing spec	Circuit modify
		20080424	PAGE9: stuff R480,R479 to meet AMD spec	Circuit modify
		20080424	PAGE17: stuff C765 10nf to meet power sequence	Circuit modify
		20080505	PAGE34: intersil recommand to set OCP to 30A	Circuit modify
			Change PR218 from CS32052FB21 to CS41072FB11,Change PR157 from CS41002FB28 to CS31002FB26,Change PR160 PR216 from	Circuit modify
			CS31622FB27 to CS23652FB08	Circuit modify
		20080505	PAGE22: Change CN17 from DFHD04MR021 to DFHD04MRA75	Circuit modify
		20080505	PAGE27: update re-driver footprint to tqfn36-5x6-5-37p-0_75h-te1m	Circuit modify
		20080505	PAGE20: reserve R720,R721 for cost down	Circuit modify
		20080505	PAGE27: add C816 0.1u to U44 +5V for ESD , add C818 0.1u to U45 +5V for ESD	Circuit modify
		20080505	PAGE25: remove CN30 second PCIE (HD Decoder)	Circuit modify
		20080505	PAGE31: remove HOLE28,35 (HD Decoder)	Circuit modify
		20080507	PAGE20: stuff D74,D75,D76 for CCD	Circuit modify
		20080508	PAGE20: reserve CM1293 U46,C819 for CCD ESD protect	Circuit modify
		20080508	PAGE28: stuff D68,D69,D70 for FP	Circuit modify
		20080508	PAGE30: stuff D53 for RF_LED ESD	Circuit modify
		20080509	PAGE26: 5/9 for card reader MS DUO adapter short issue	Circuit modify
			reserve R723,724,722 ,Q82,Q81,Q83,Q84	Circuit modify
		20080513	PAGE4: follow AMD design guide 1.03 stuff R675	Circuit modify
		20080527	PAGE26: some 1394 device can't boot normal	Circuit modify
			change L38 to BK1608HS220_6	Circuit modify
		20080527	PAGE34: CPU core adj	Circuit modify
			1.PR160,PR216 change to 3.92K/F_4	Circuit modify
			2.PR213,PR215 change to 18.2K/F_4	Circuit modify
		20080527	PAGE33: solve system hang up , when plug adp quickly	Circuit modify
			change PR113 from 150K_4 to 115K/F_4	Circuit modify
		20080527	PAGE33: avoid right side USB voltage drop	Circuit modify
			change PR119 to 63.4K , PR120 to 10K	Circuit modify
		20080528	PAGE12: del C805,C807	
		20080529	PAGE27: change ESATA conn p/n to DFHS11FR027	

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