

# ***KSKAA***

## ***Bradford 10M/10MG***

# **LA-4993P REV 1.0 Schematic**

Intel Penryn/ Cantiga/ ICH9M  
2009-07-23 Rev. 1.0

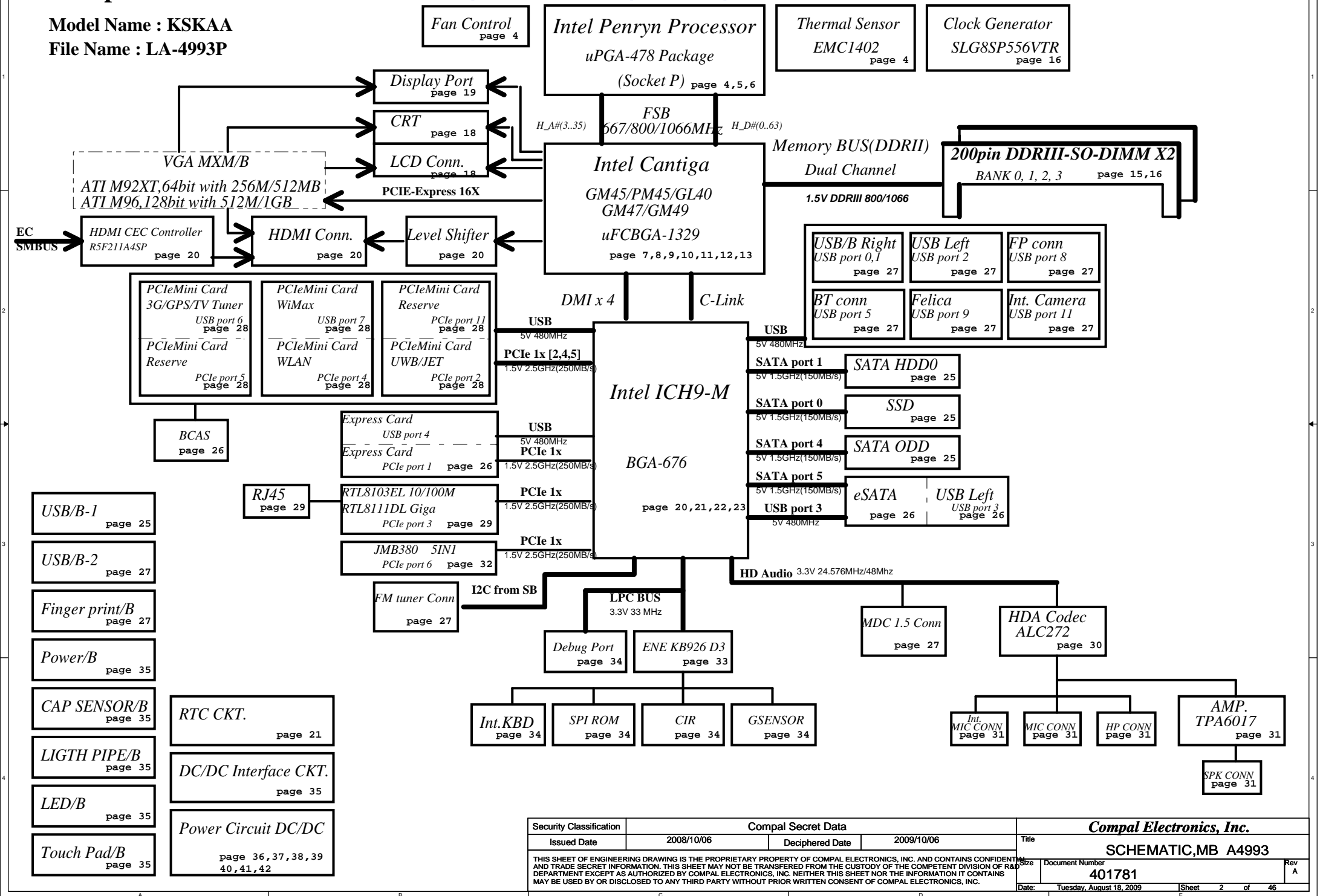
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# Compal Confidential

Model Name : KSKAA

File Name : LA-4993P

http://laptopblue.vn



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## Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
+3VL	3.3V always on power rail	ON	ON	ON	ON
+3V_SB	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_WLAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	OFF
+5VL	5V always on power rail	ON	ON	ON	ON
+5V_SB	5V power rail for SB	ON	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	ON
+CPU_CORE	Core voltage for VGA chip	ON	ON	OFF	OFF
+VGA_PCIE_1.1VS	1.1V switched power rail for VGA PCIE	ON	ON	OFF	OFF
+1.8VS	1.8V power rail for VRAM	ON	ON	OFF	OFF

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#		
Full ON	HIGH	HIGH	HIGH	HIGH		
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH		
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH		
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH		
S5 (Soft OFF)	LOW	LOW	LOW	LOW		
G3	LOW	LOW	LOW	LOW		

## BTO Option Table

Function	HDMI			CRT	Display	LAN		
description	(Y)			(Q)	(Z)	(E)	(C)	
explain	Intel(UMA)	ATI MXM/B	COMMON			10/100M	Giga	
BTO	IHDMI@	NIHDMI@	HDMI@	H@	CRT@	DP@	8103EL@	8111DL@

Function	3G SIM slot	Mini card	Felica	Finger printer	CIR	CAMERA & MIC		BLUE TOOTH
description	(3)	(D2)	(J)	(F)	(I)	(X)		(B)
explain		Two Cards				CAMERA	MIC	
BTO	3G@	3G@	FLICA@	FP@	CIR@	CAM@	MIC@	BT@

## External PCI Devices

## EC SM Bus1 address

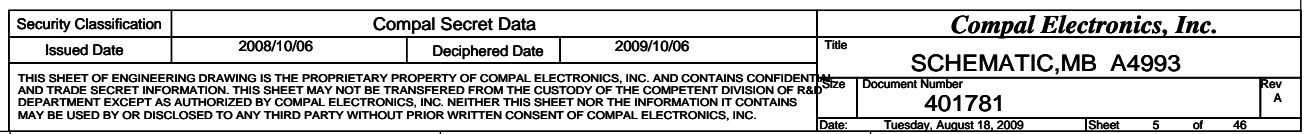
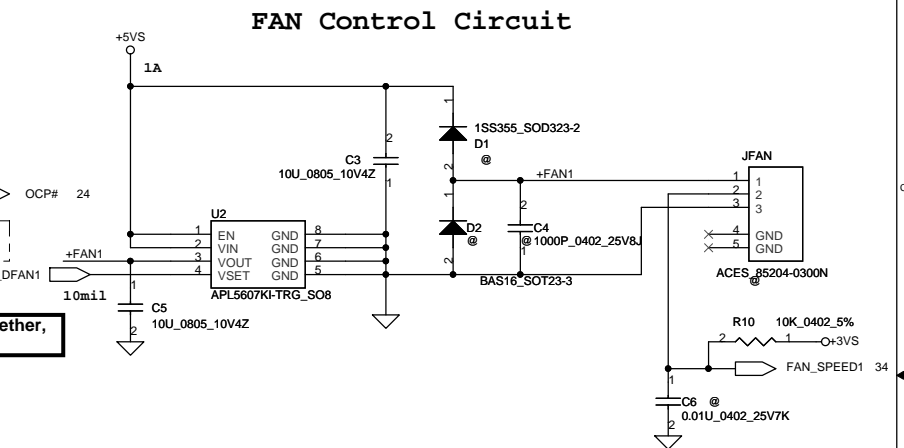
## EC SM Bus2 address

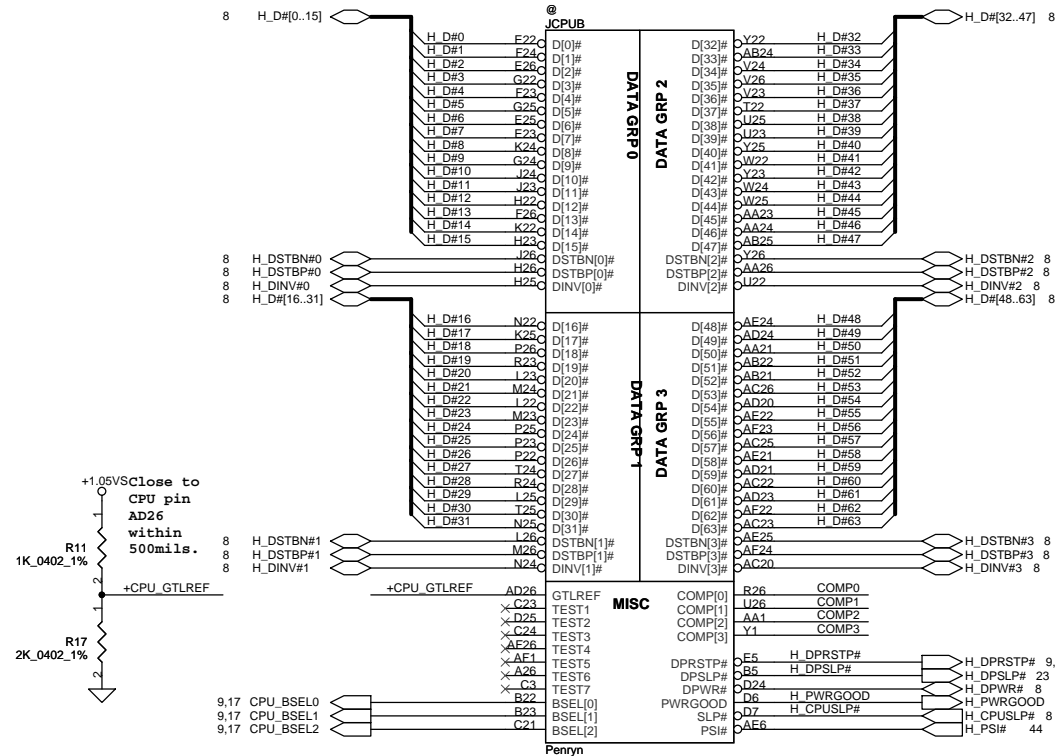
Power	Device	Address	Power	Device	Address
+3VL	EC KB926 D3		+3VS	EC KB926 D3	
+5VL	Smart Battery	0001 01X b		CPU THM Sen	
+5VL	HDMI-CEC	0011 010x b	+3VS	SMSC SMC1402	0100 110x b
+3VL	FUN/B (CAP Sensor)				

## ICH9M SM Bus address

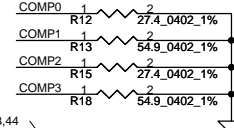
Power	Device	Address
+3V_SB	ICH9M	
	Clock Generator (SLG8SP556V)	1101 001Xb
+3VS	DDR DIMM0	1001 000Xb
+3VS	DDR DIMM1	1001 010Xb
+3VS	Express	
+3VS	FM Module	

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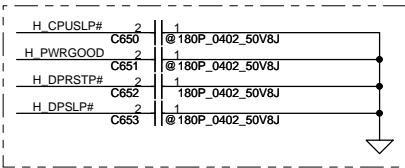
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



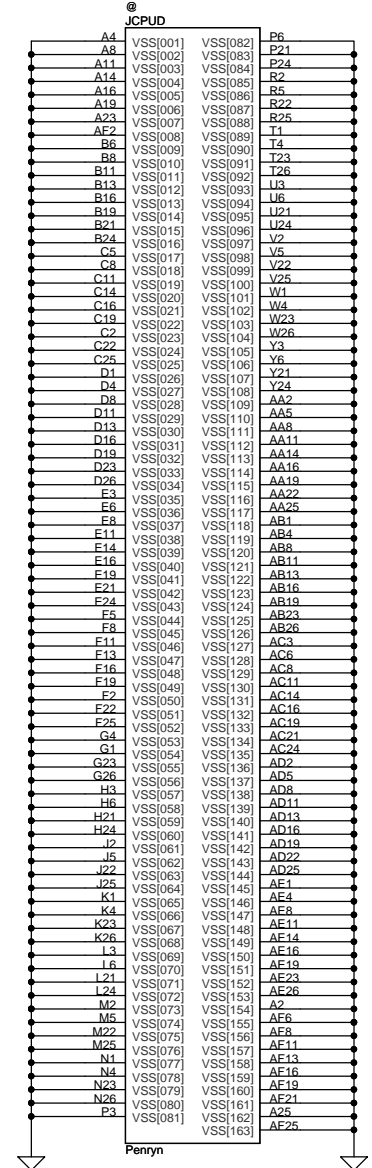
layout note: Please use "Daisy Chain" to layout and the signal (H\_DPRSTP#) is routed from ICH9 to power IC, then to NB and CPU

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

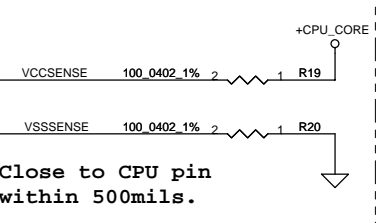
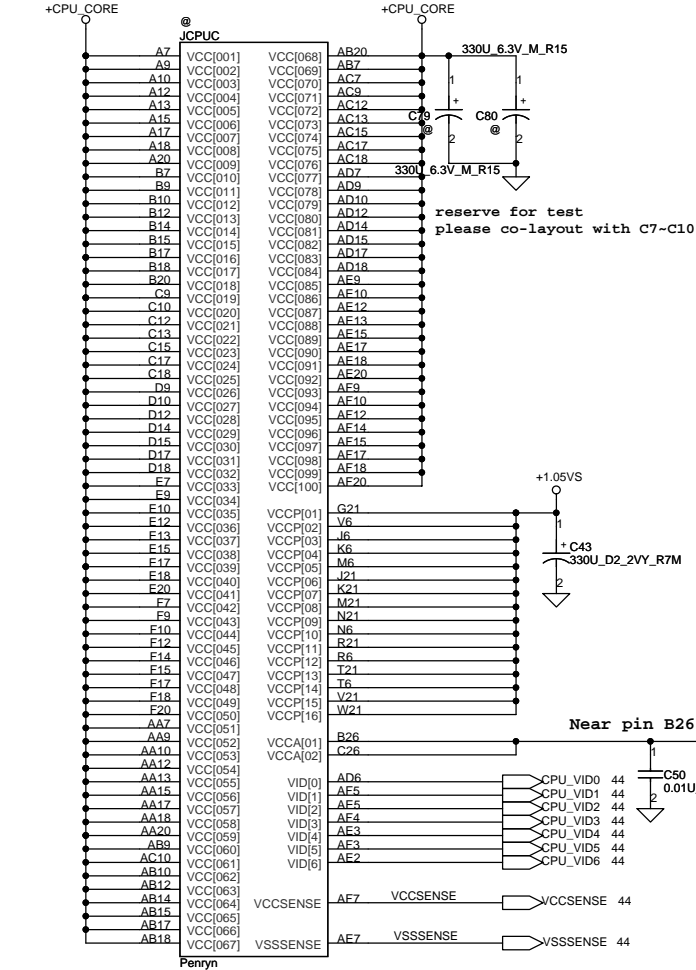
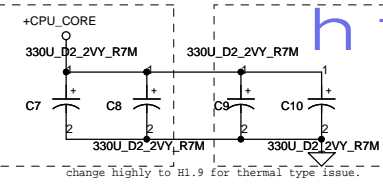


Reserve for debug close to CPU

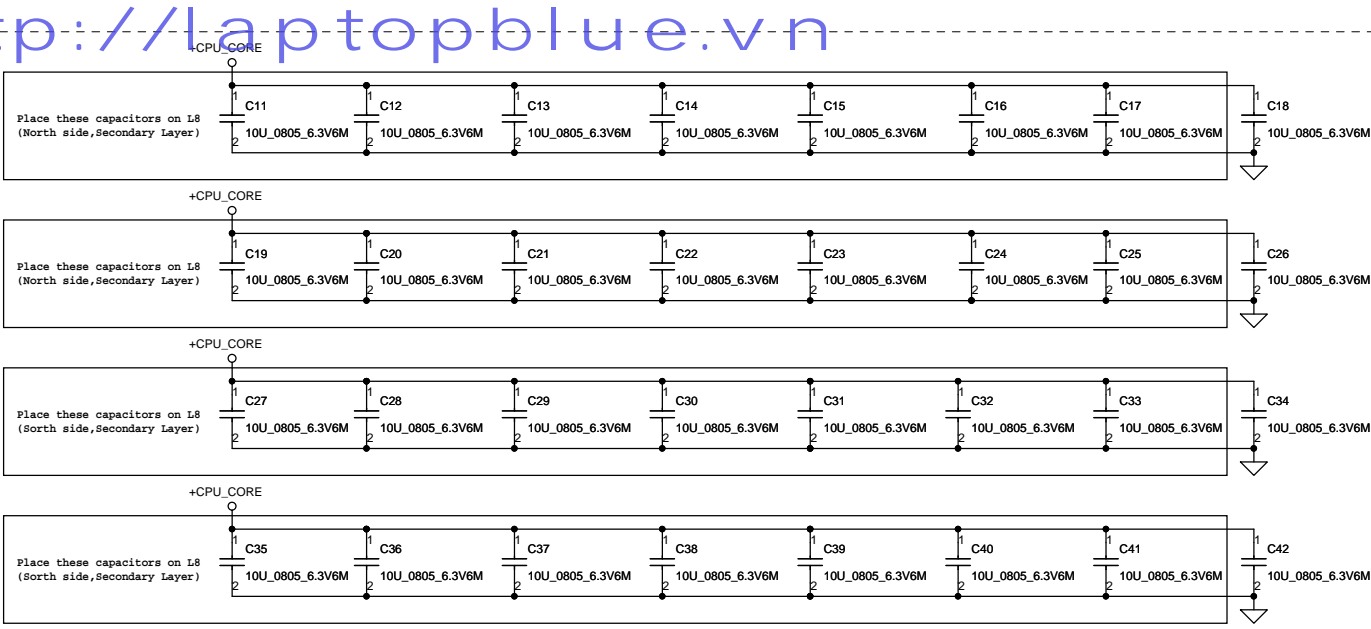


Near CPU CORE regulator

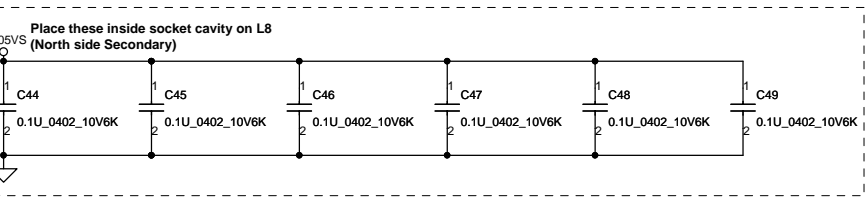
ESR <= 1.5m ohm  
Capacitor > 1980uF



Length match within 25 mils.  
The trace width/space/other is 14/7/25.

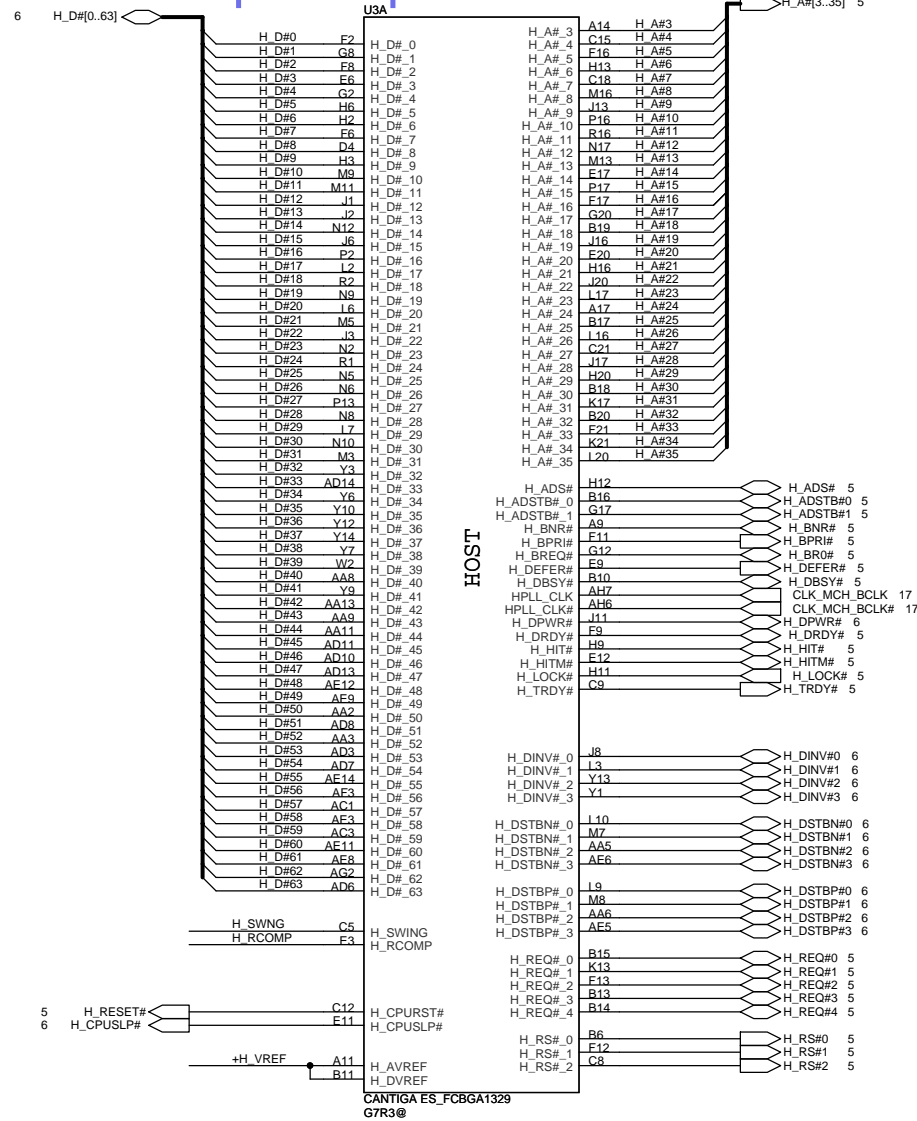
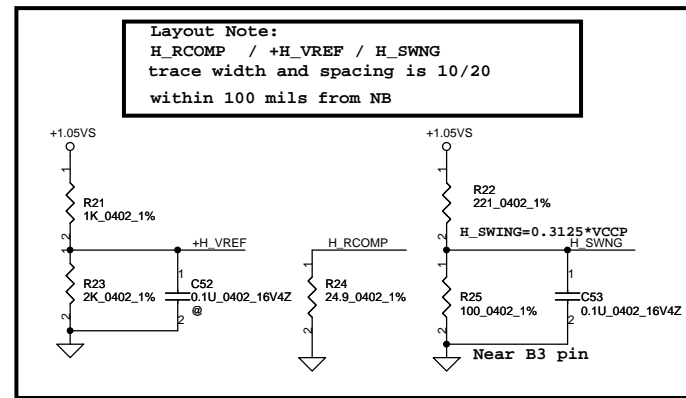


Mid Frequency Decoupling



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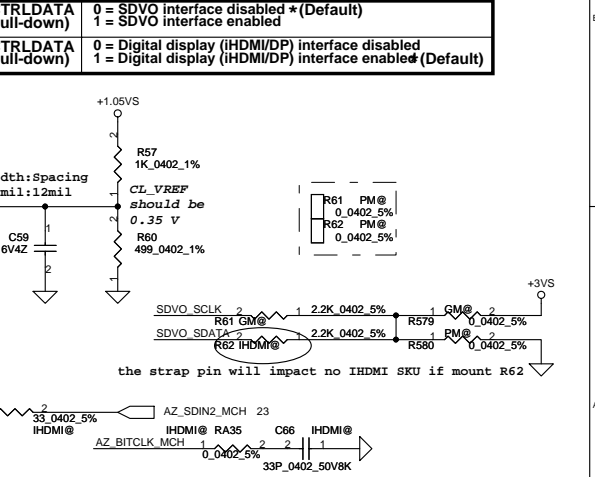
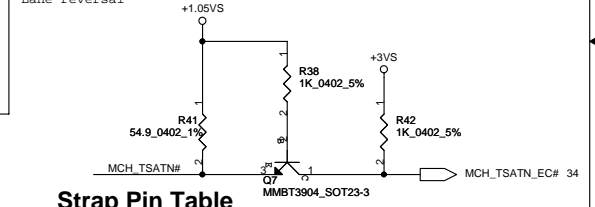
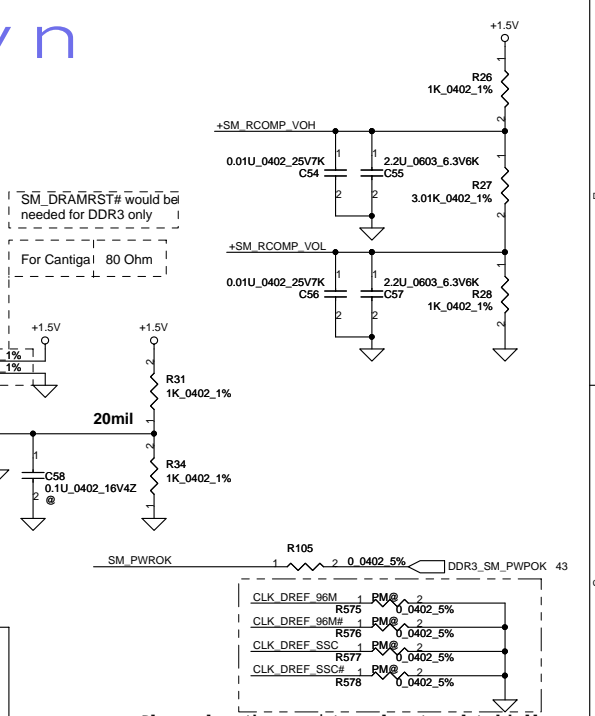
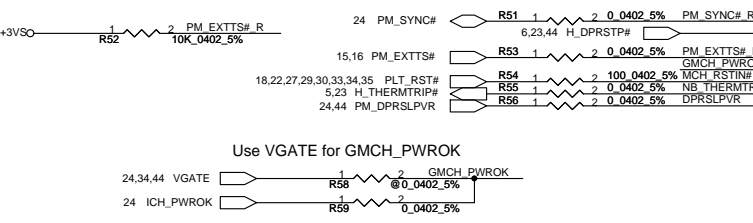
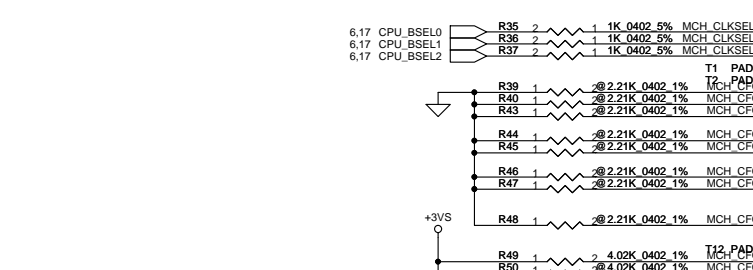


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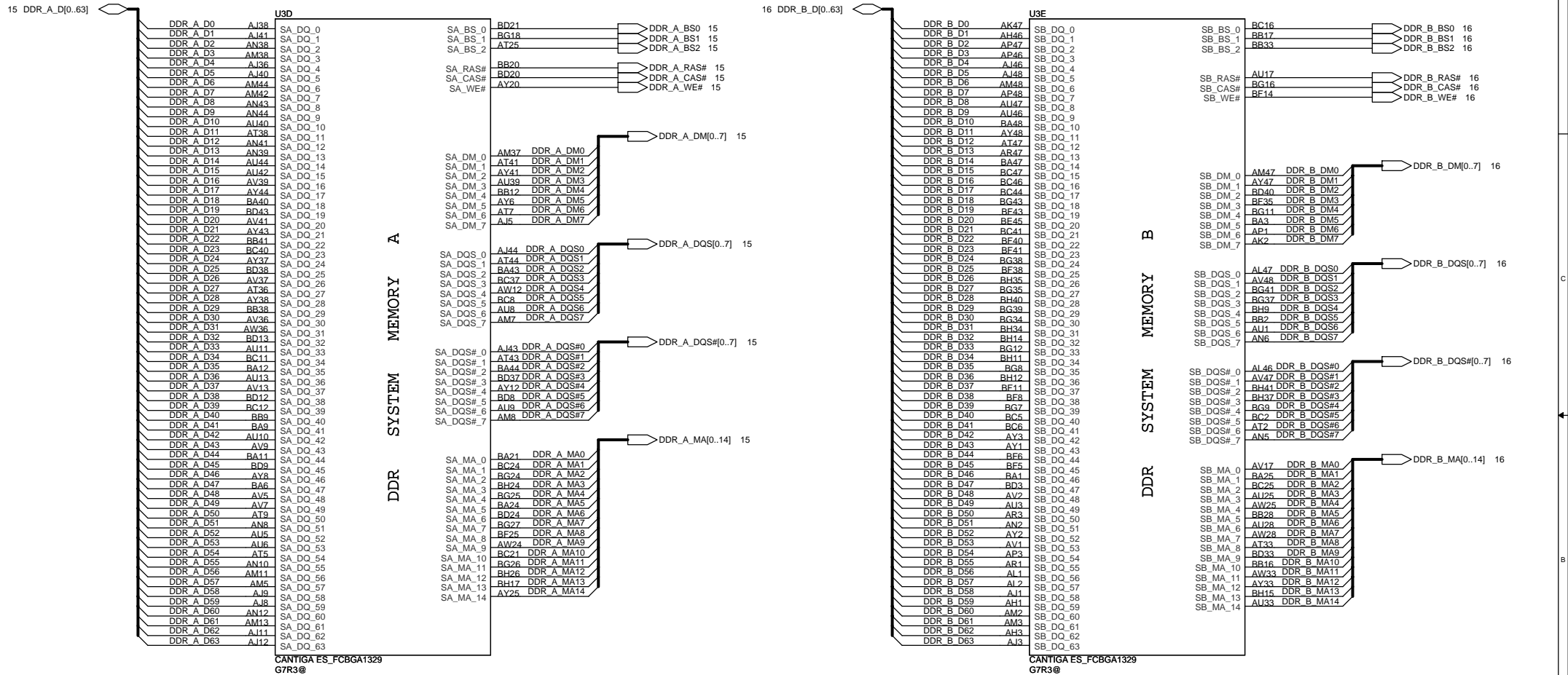
Strap Pin Table

CFG[2:0]	011 = FSB667 010 = FSB800 000 = FSB1067
CFG5 Internal pull-up	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG6 Internal pull-up	0 = iTPM Host Interface is enabled can support disable by SW. 1 = iTPM Host Interface is Disabled *(Default)
CFG7 Internal pull-up	0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel Management Engine Crypto TLS cipher suite with confidentiality *(Default)
CFG9 Internal pull-up	0 = Lane Reversal Enable 1 = Normal Operation *(Default)
CFG10 Internal pull-up	0 = PCIe Loopback Enable 1 = Disable*(Default)
CFG[13:12] Internal pull-up	01 = All Z Mode Enabled 00 = Reserved 10 = XOR Mode Enabled 11 = Normal Operation*(Default)
CFG16 Internal pull-up	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG19 Internal pull-down	0 = Normal Operation 1 = DMI Lane Reversal Enable *(Default)
CFG20 Internal pull-down (PCIe/SDVO select)	0 = Only PCIe or [SDVO/DP/HDMI] is operational. * (Default) 1 = PCIe/[SDVO/DP/HDMI] are operating simu.

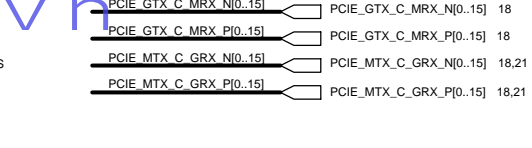


CANTIGA ES\_FC8GA1329  
G7R3@

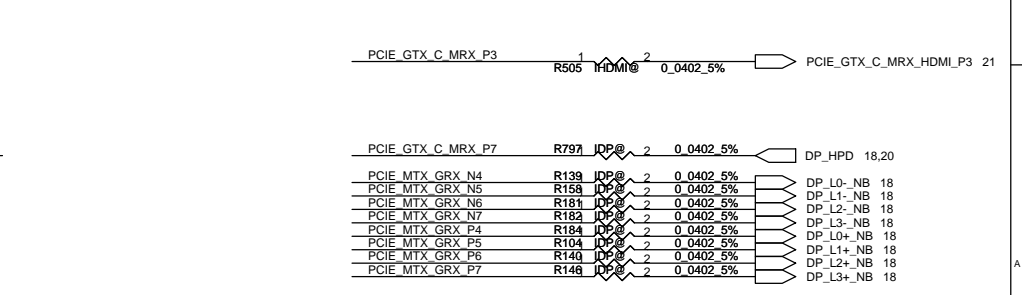
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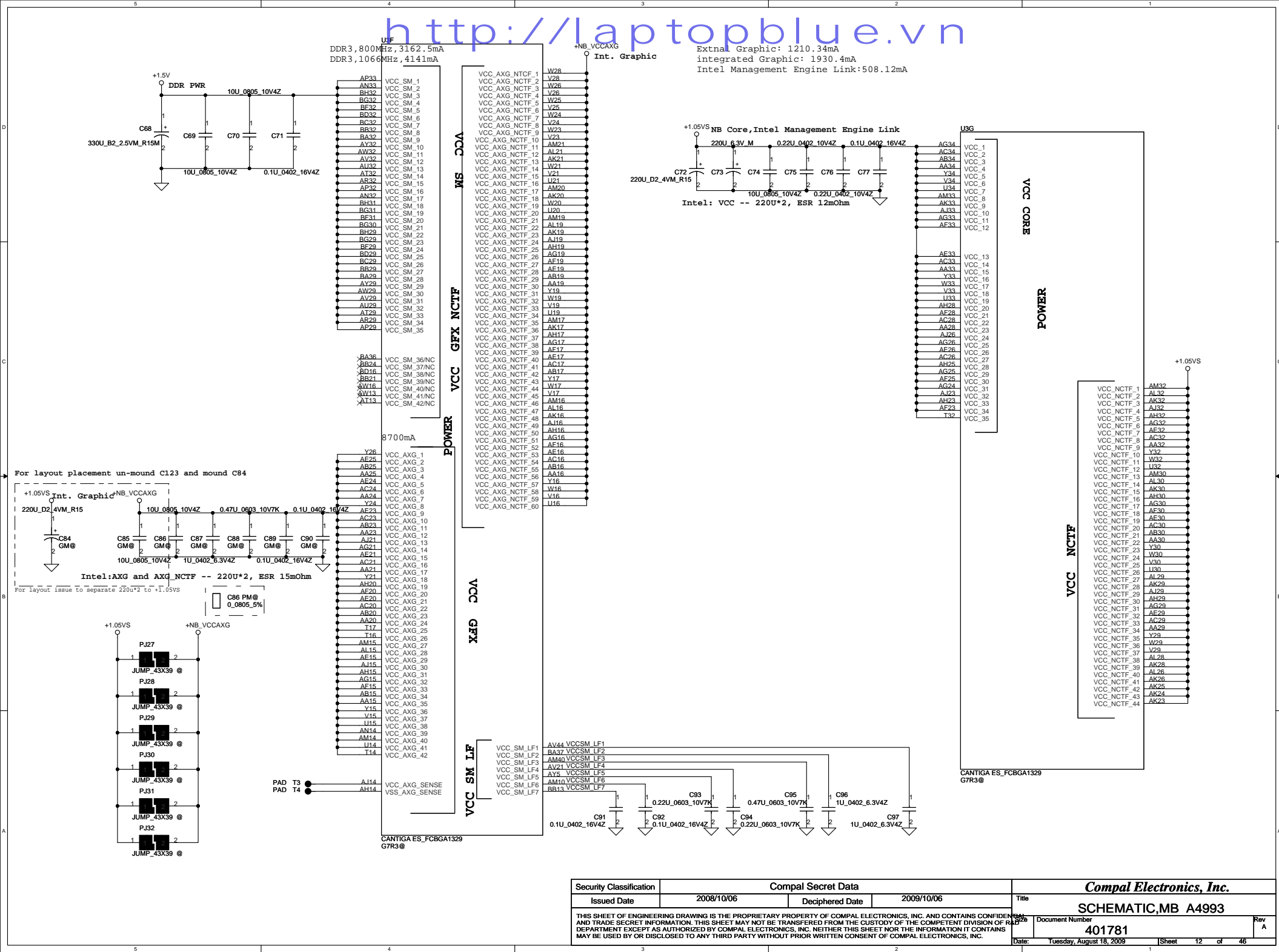
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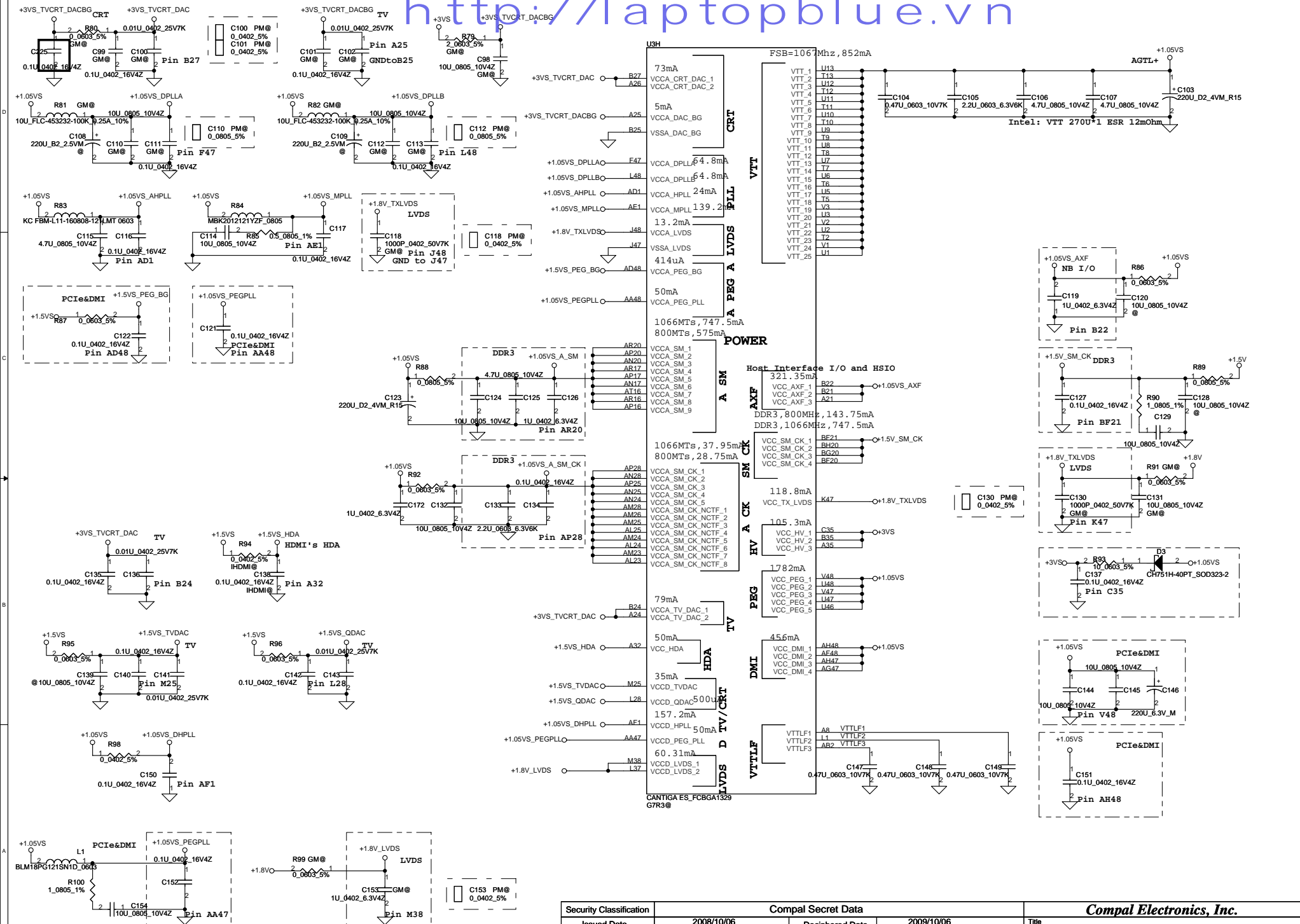
0.1U_0402_16V7K				PCIE	MTX	C	GRX	P13
C641_1	2	PM@	0.1U_0402_16V7K	PCIE	MTX	C	GRX	P14
0.1U_0402_16V7K				PCIE	MTX	C	GRX	P15



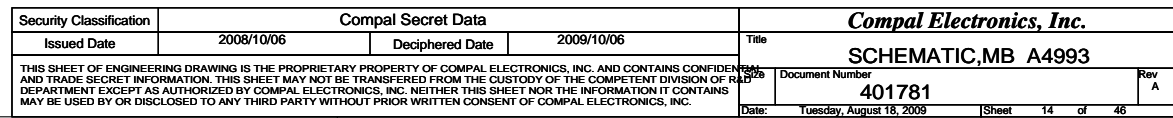
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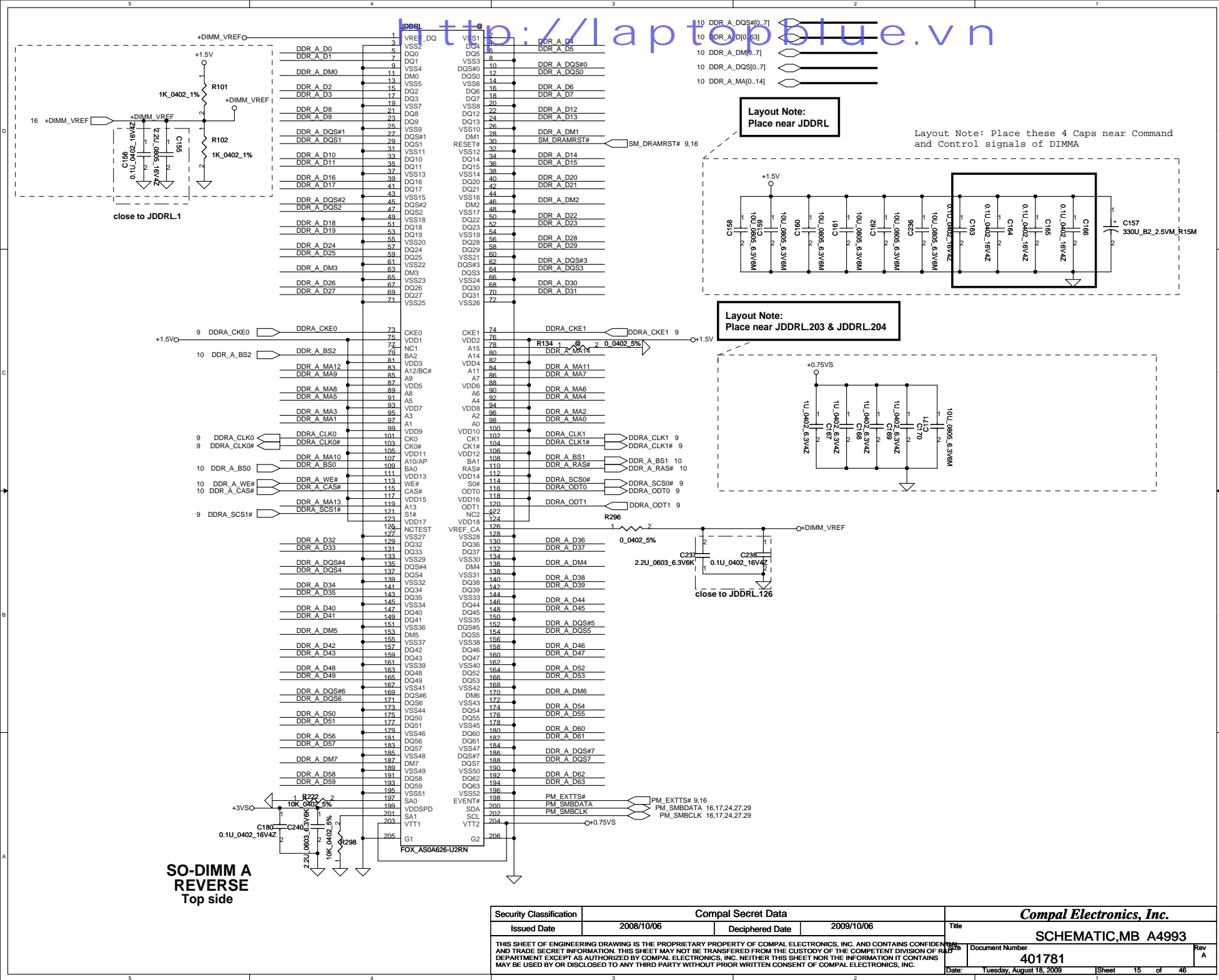




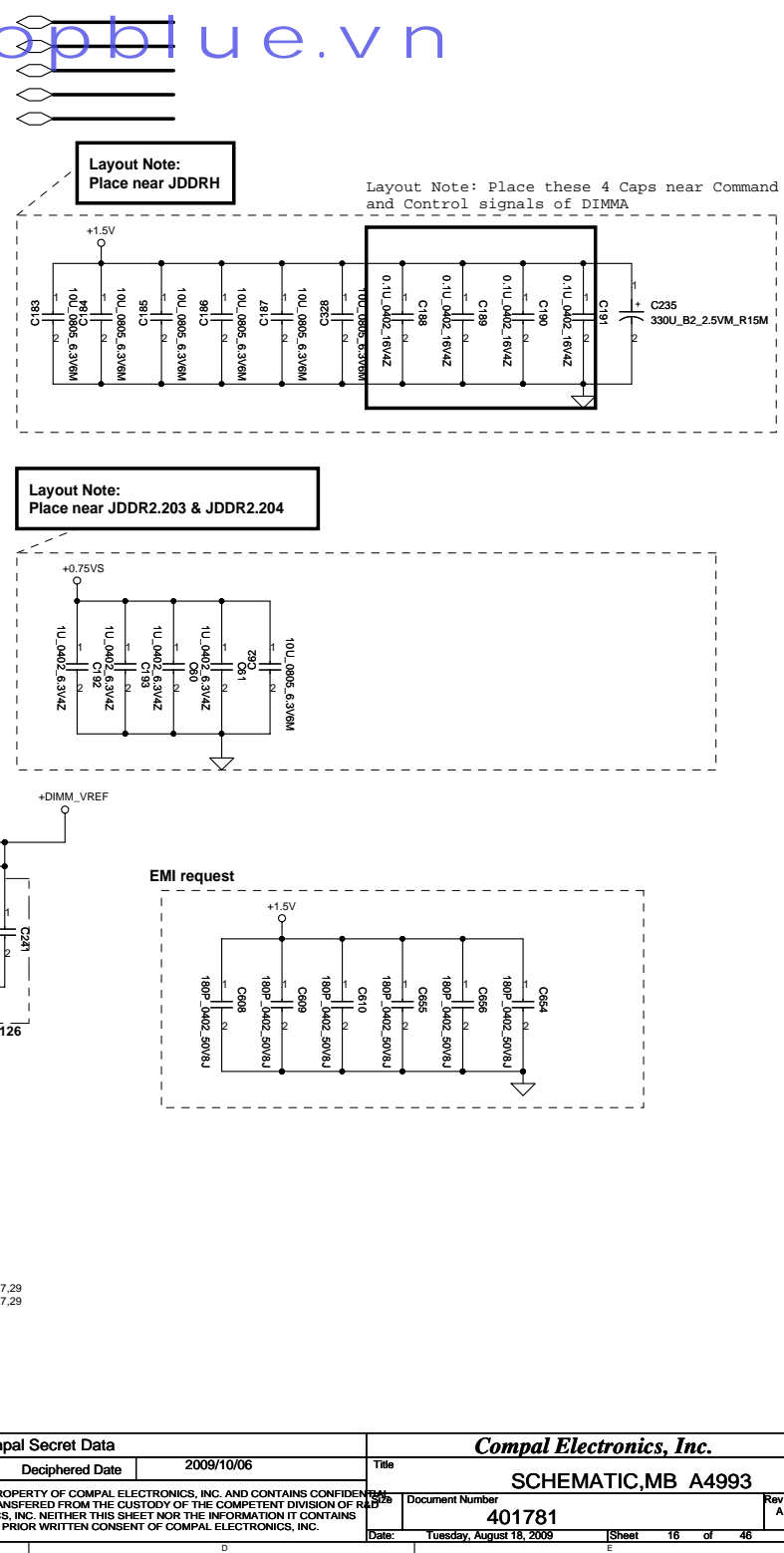
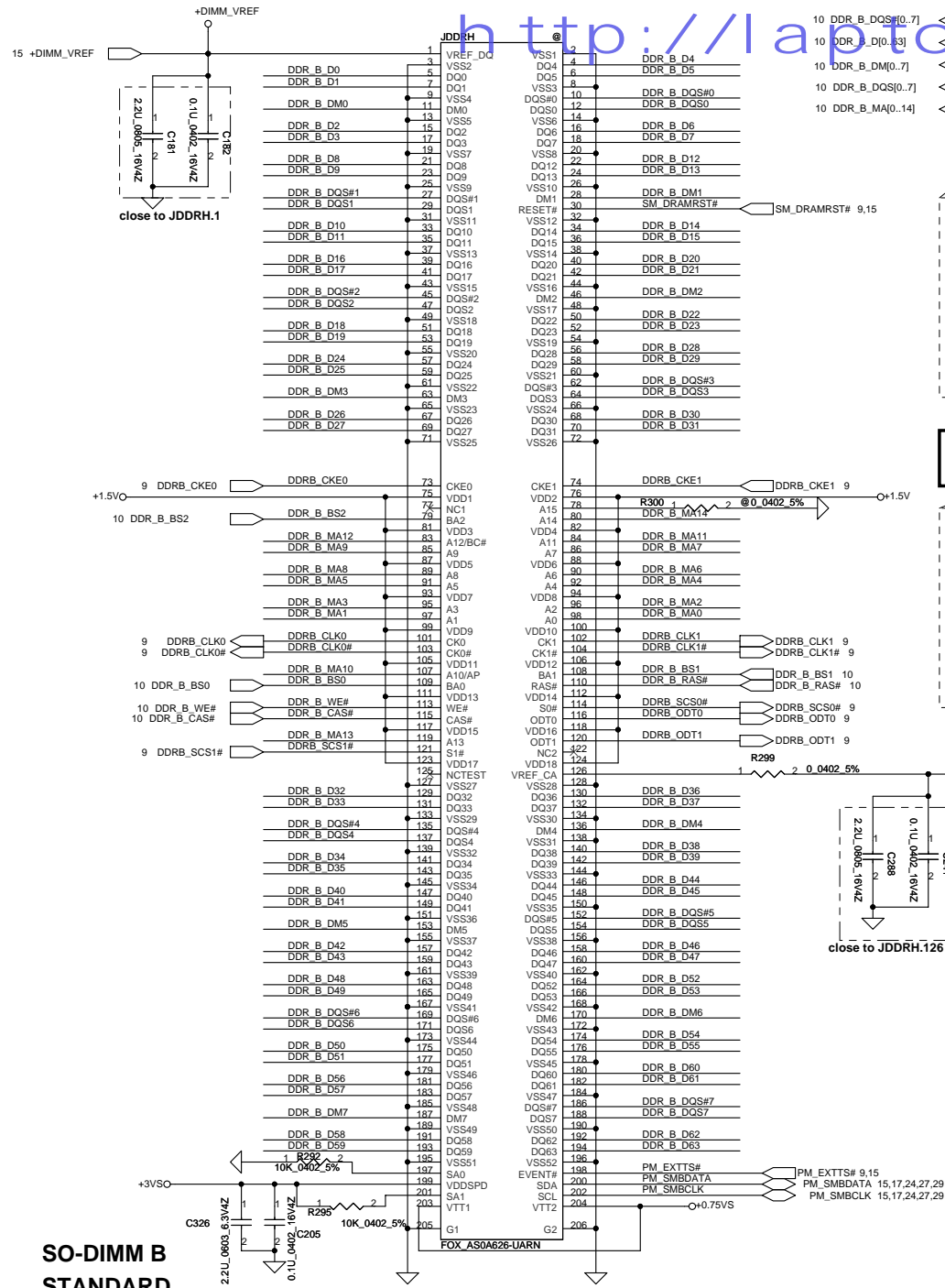


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11,21 PCIE\_MTX\_C\_GRX\_N0..15]
11,21 PCIE\_MTX\_C\_GRX\_P0..15]

11 PCIE GTX\_C\_MRX\_N0..15]
11 PCIE GTX\_C\_MRX\_P0..15]

PCIE GTX\_C\_MRX\_N0..15]
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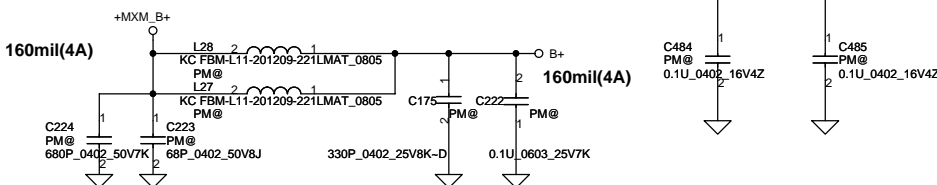
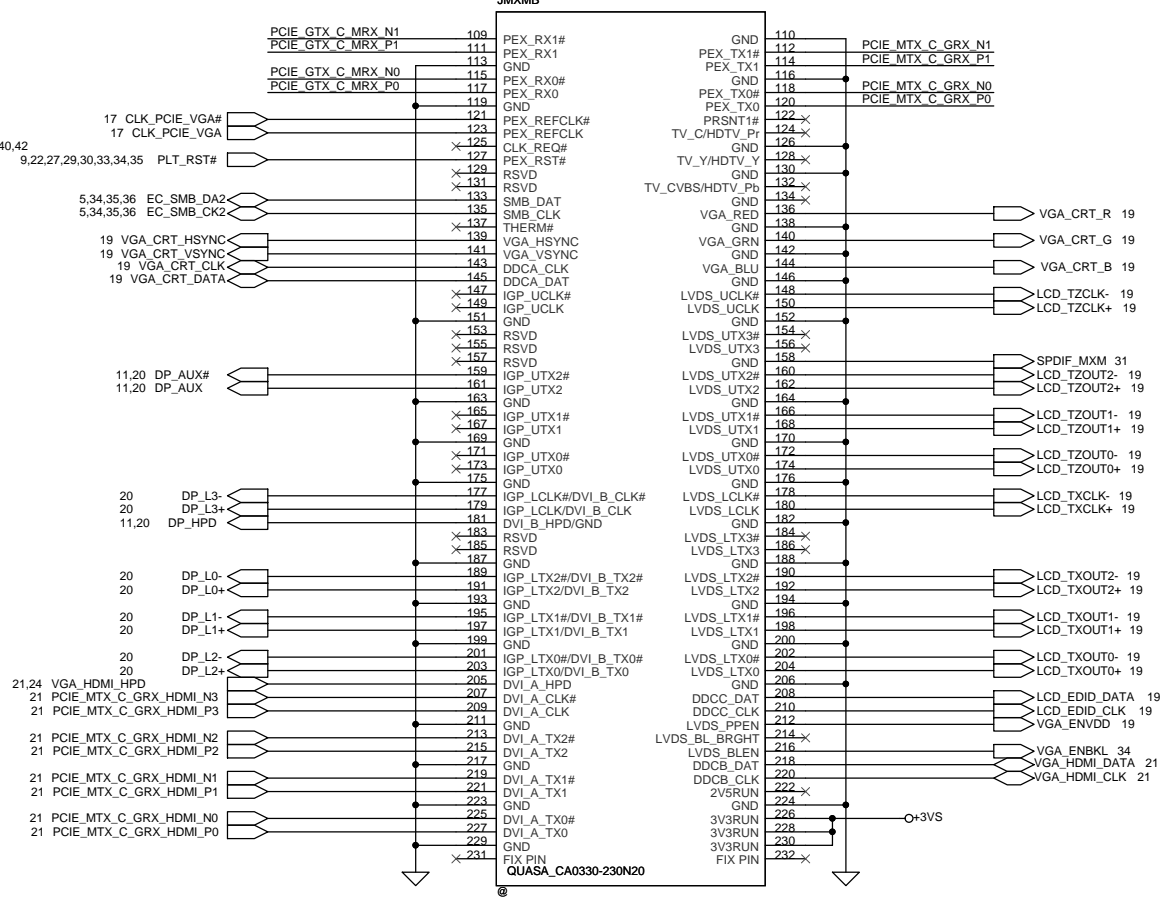
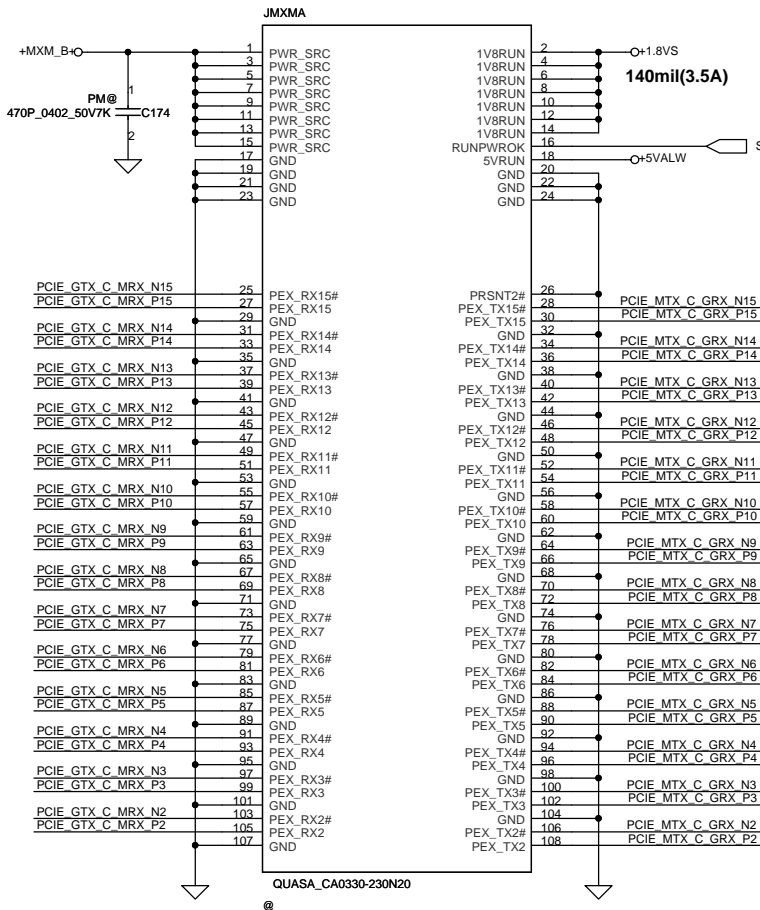
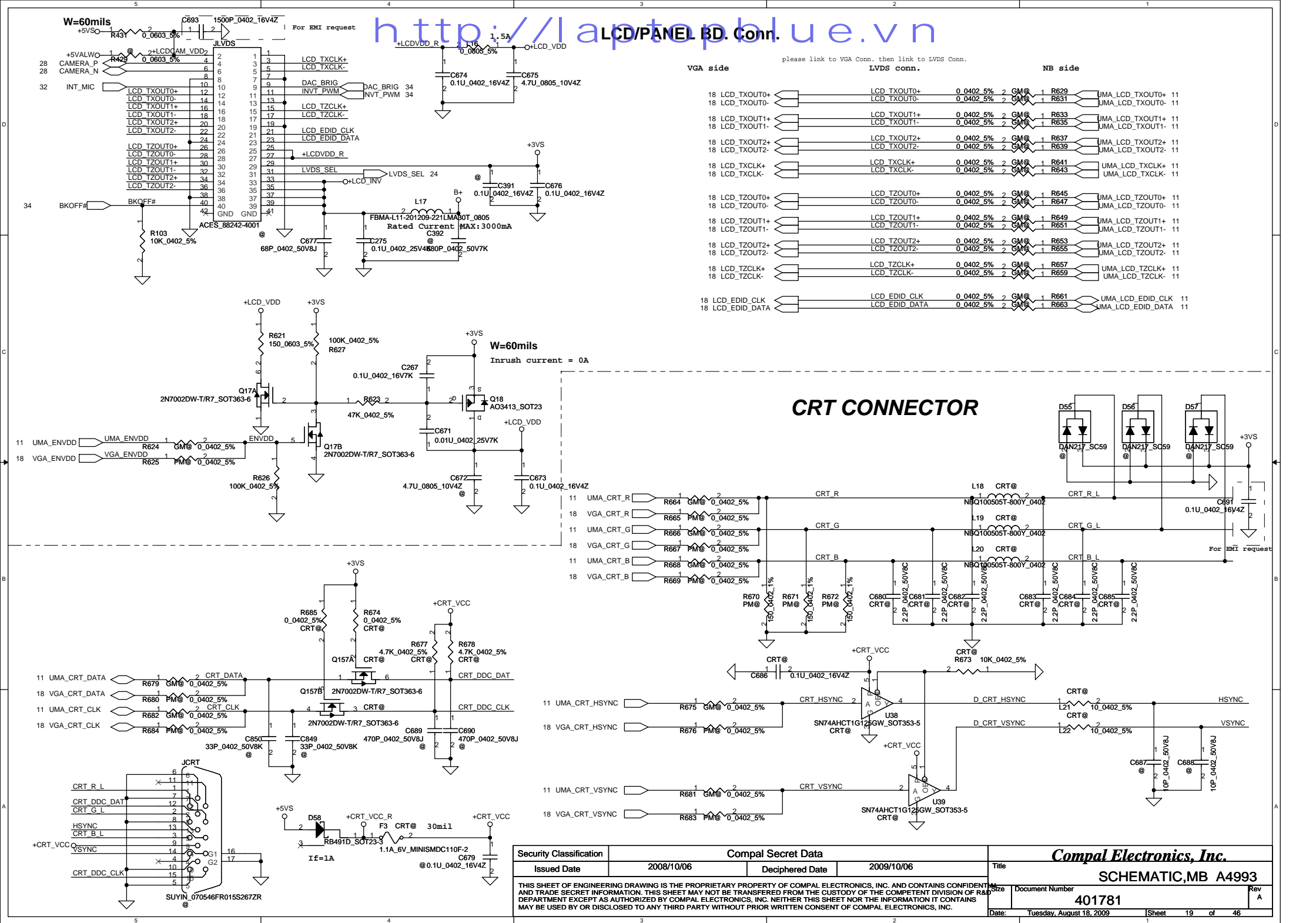


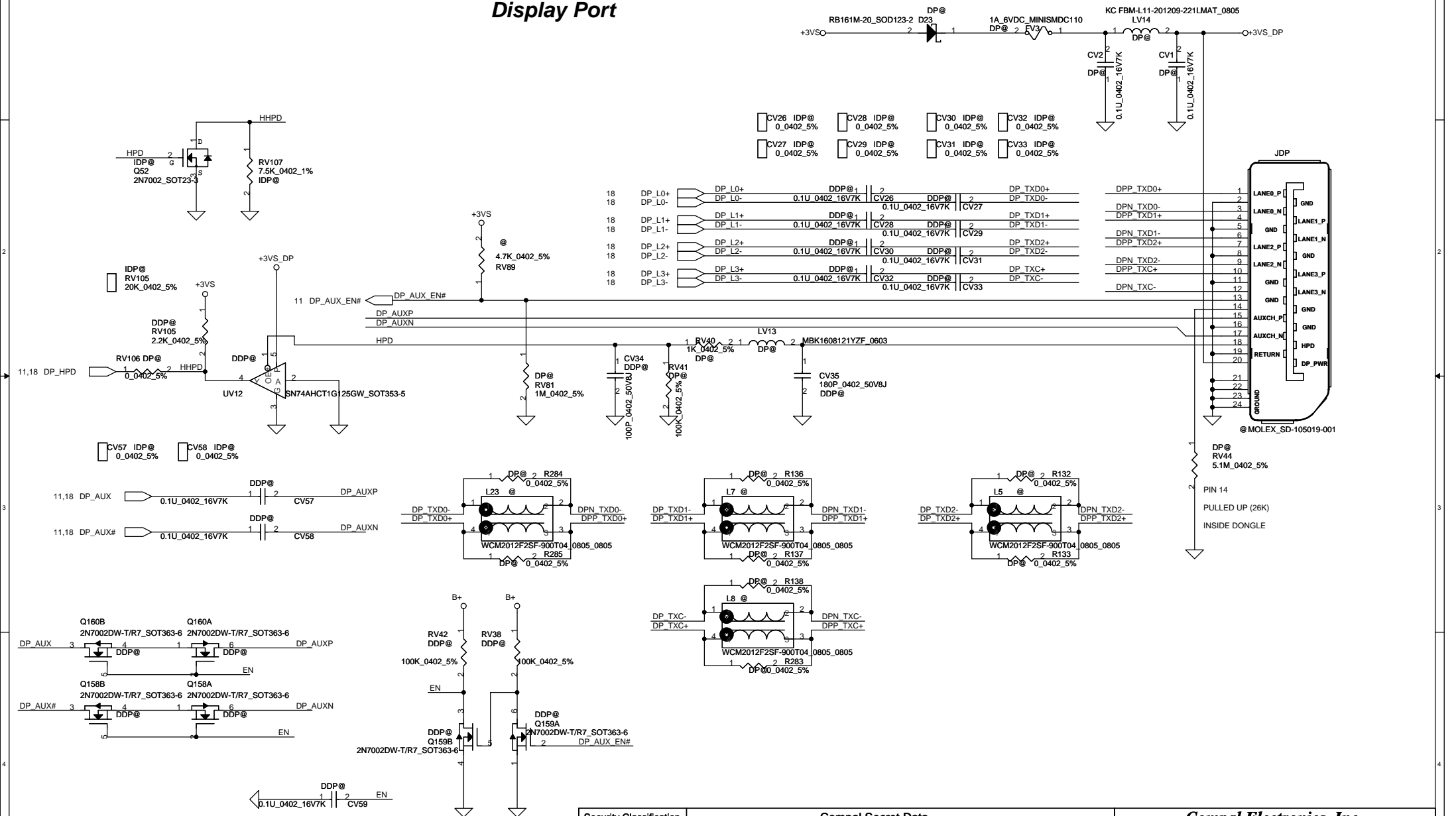
Table with 4 columns: Pin Number, Signal Name, Component Value, and Pin Name. It lists connections for DP\_L0- through DP\_L3+.

Close to MXM Connector

Table with 4 columns: Security Classification, Issued Date, Deciphered Date, and Title. It contains information about the document's security and date.

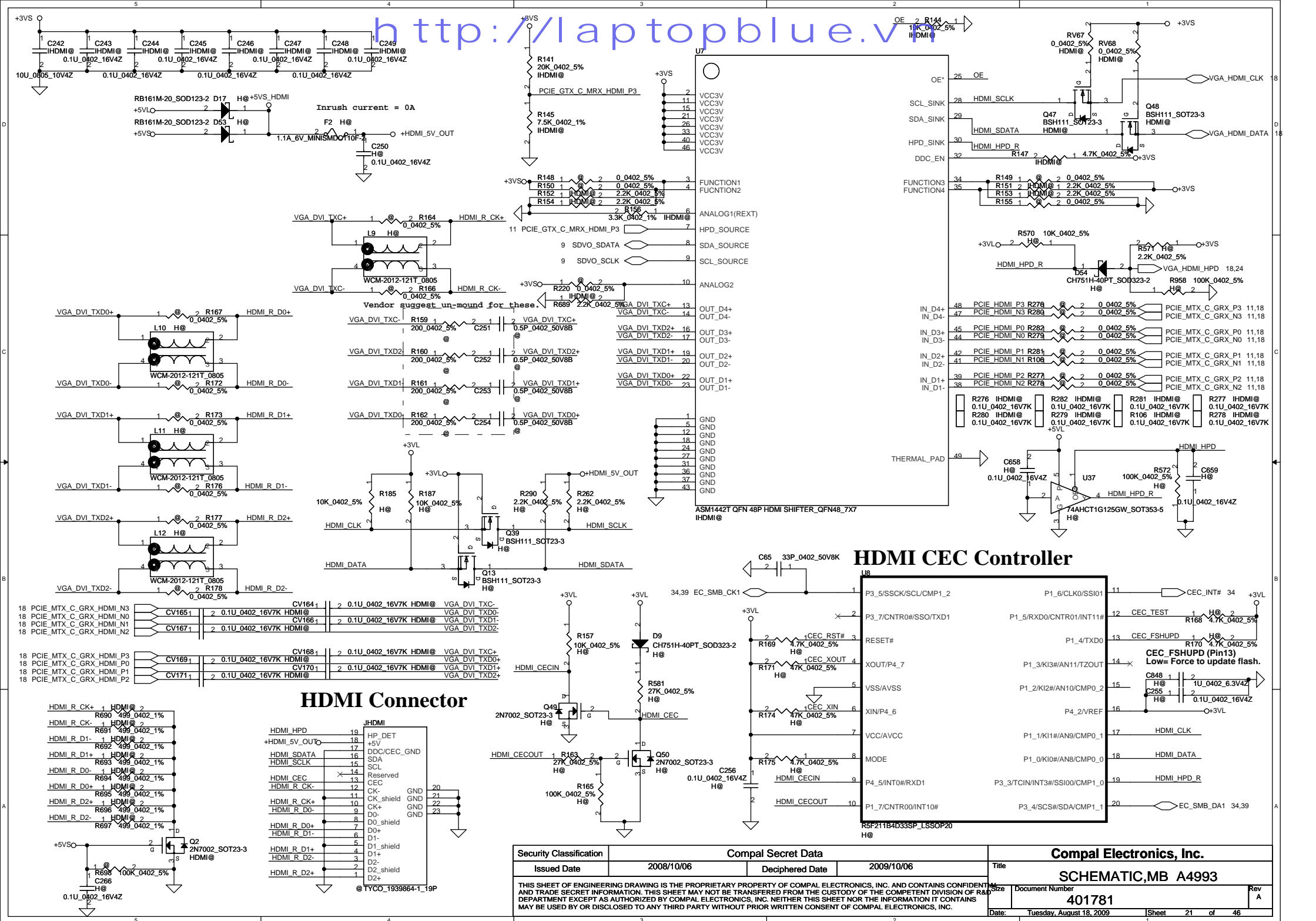


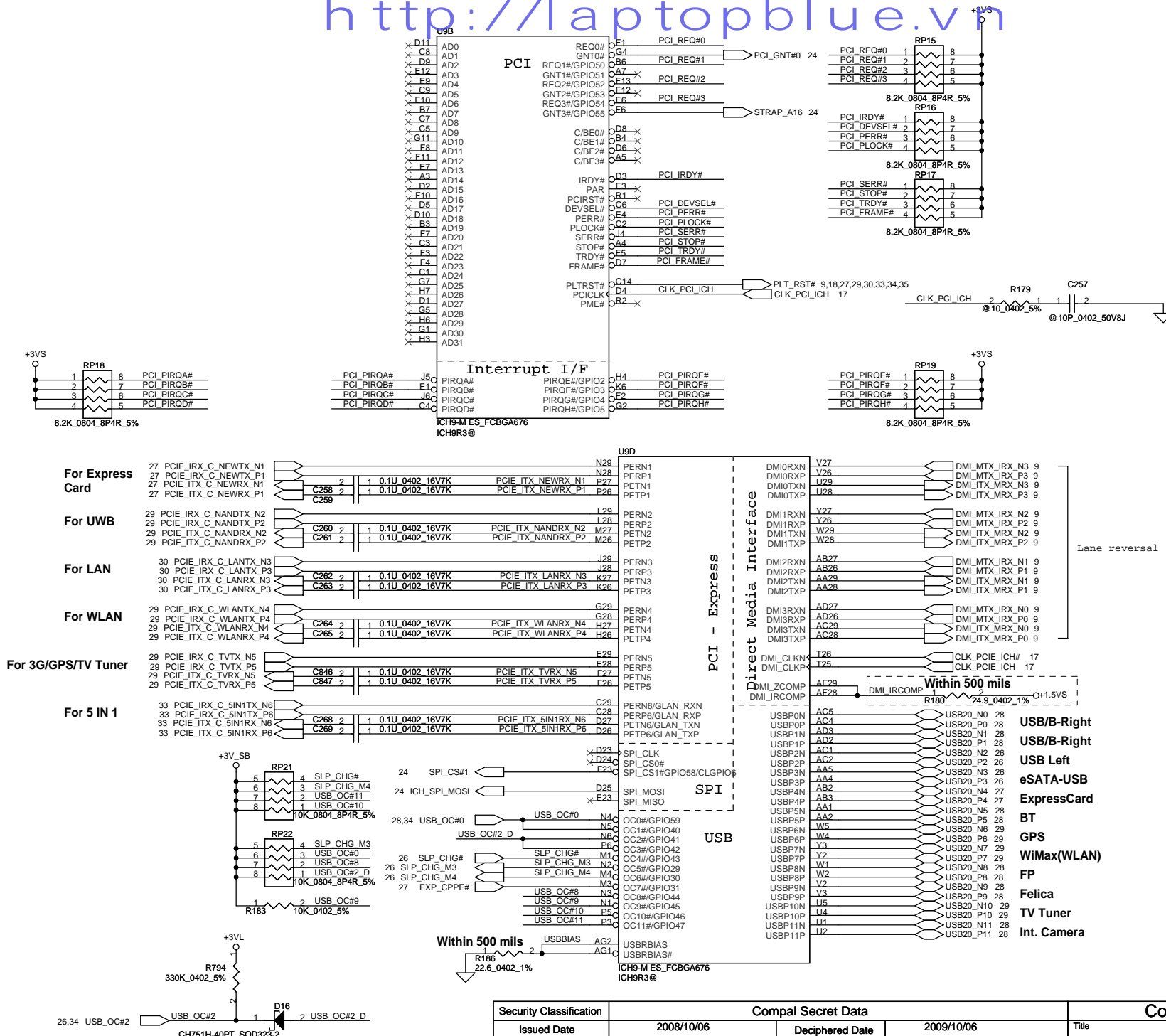
# Display Port



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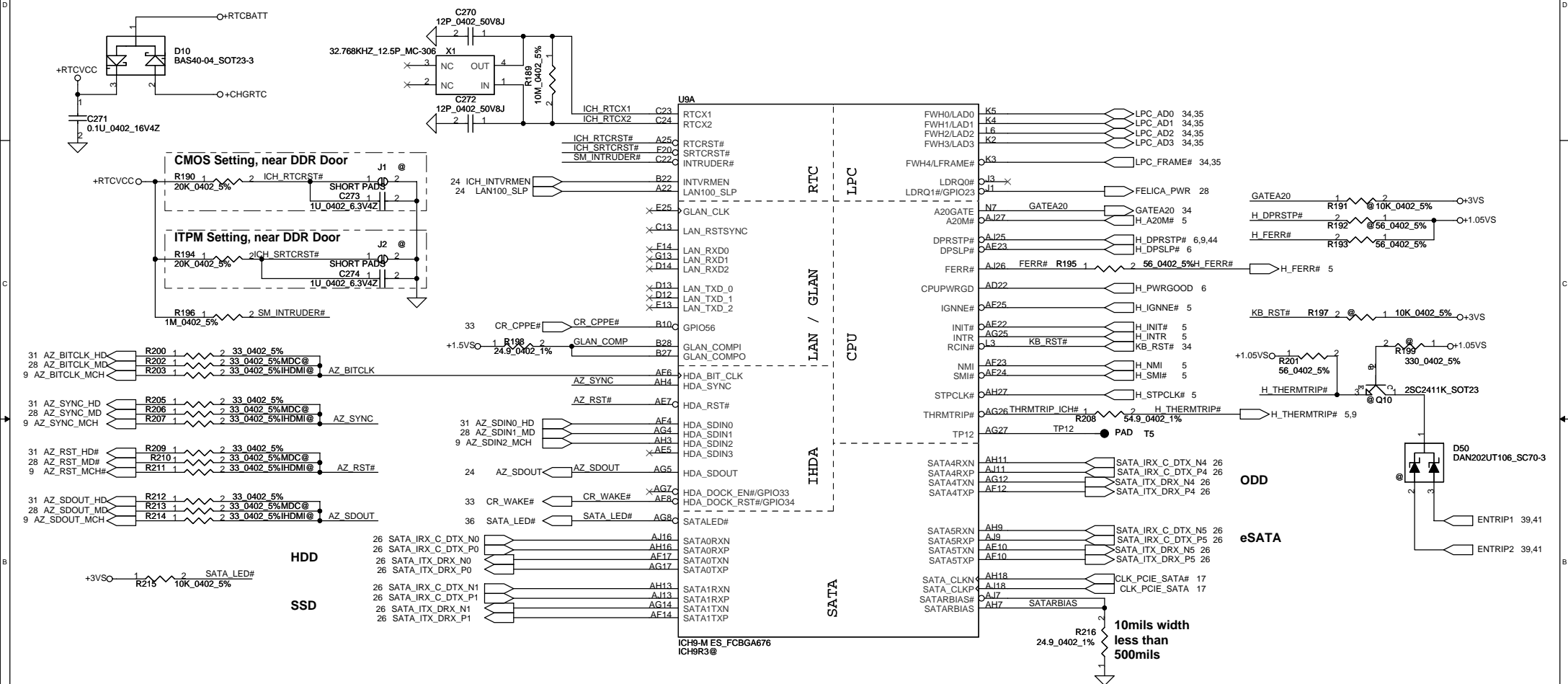




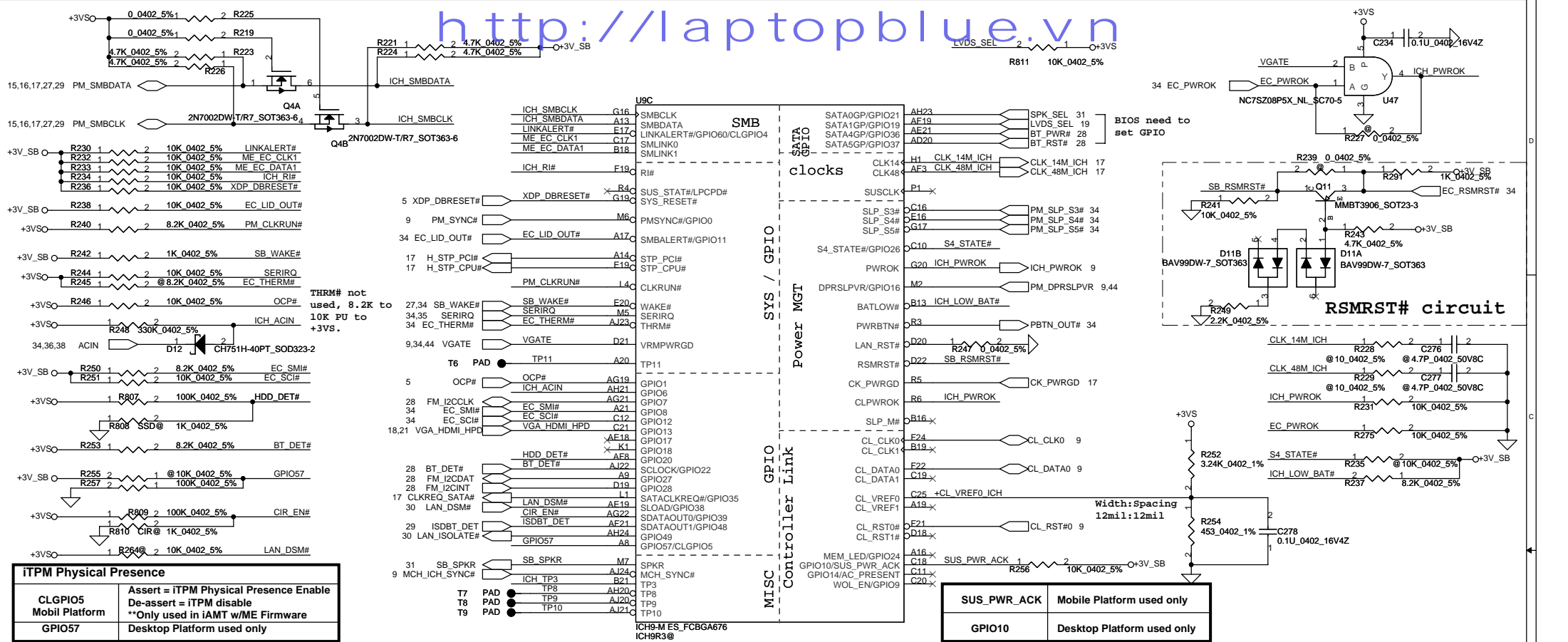


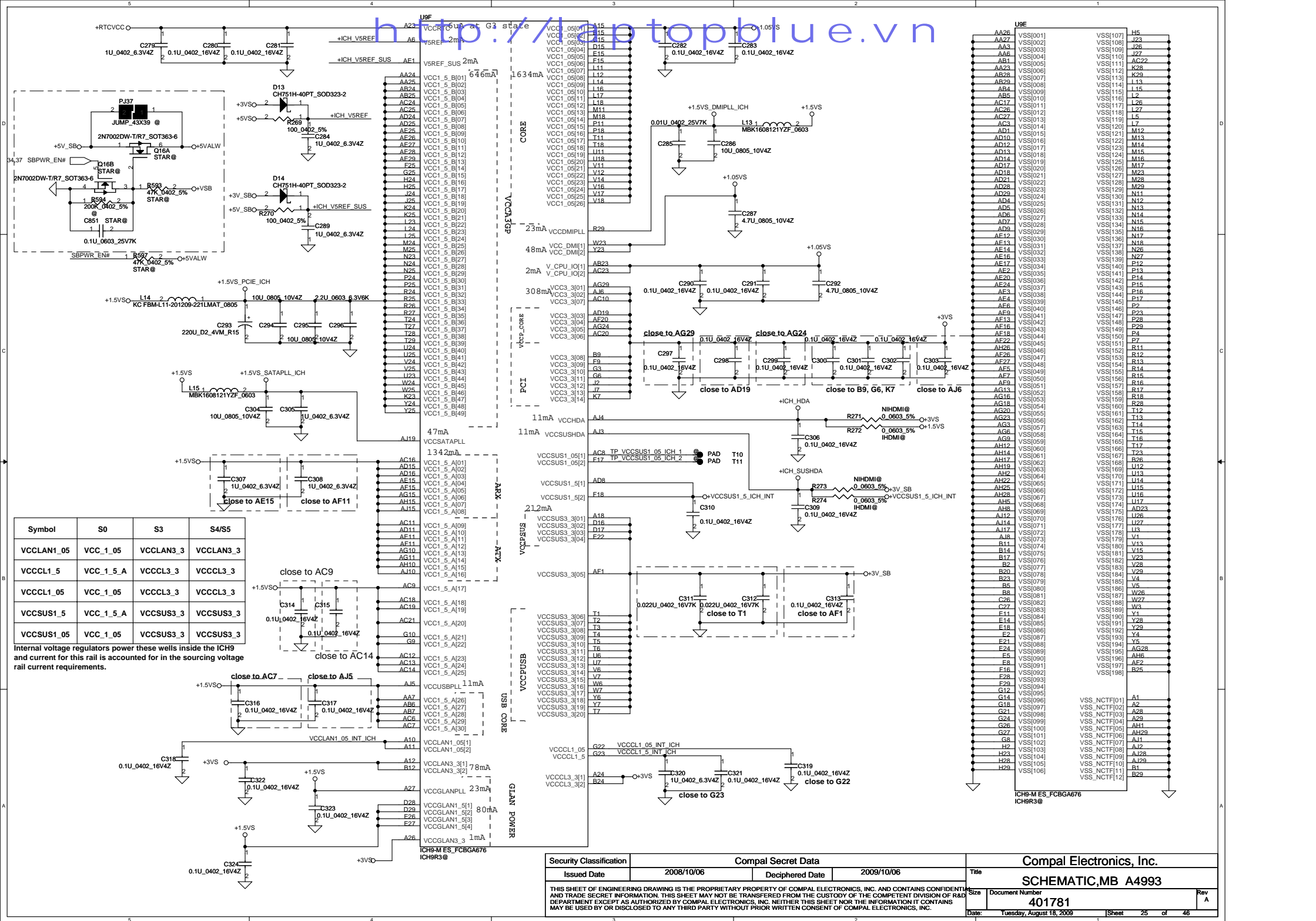
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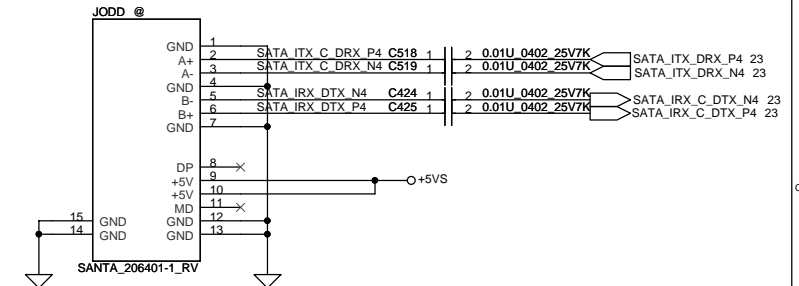
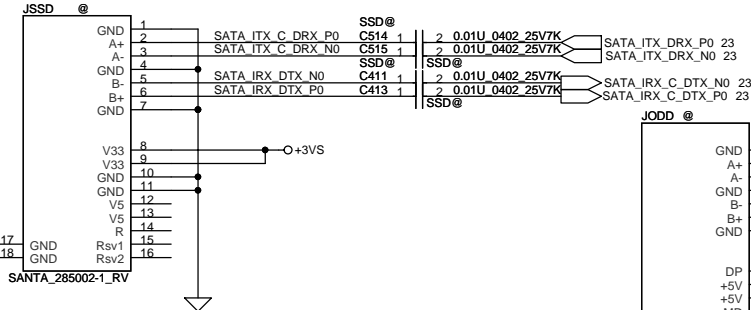
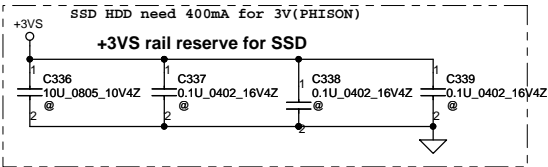
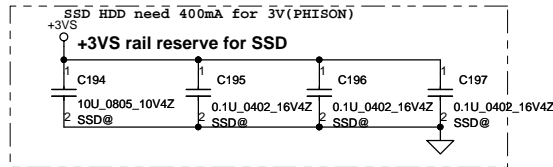


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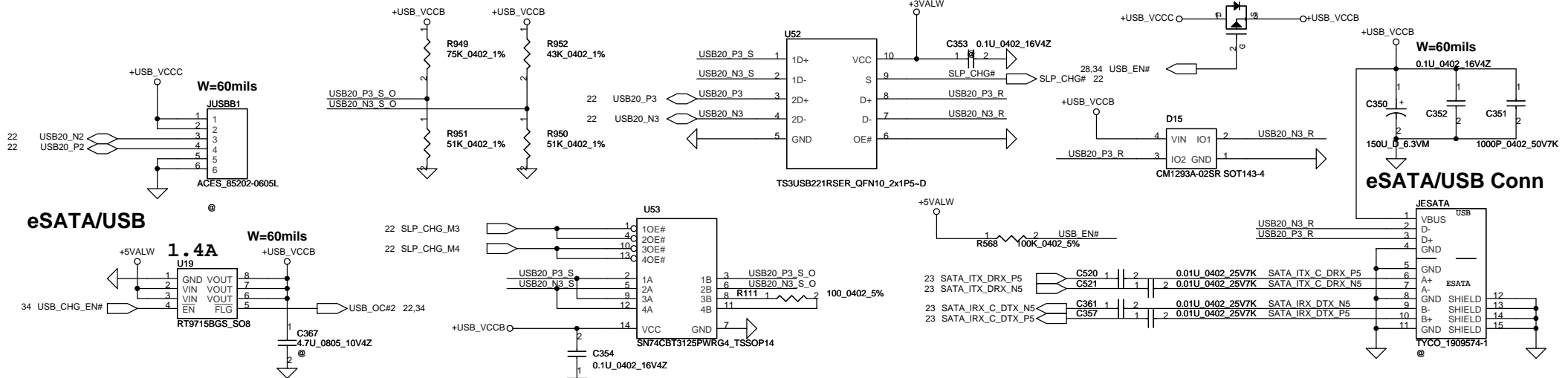




http://laptopblue.vn

~~SSD Conn.~~

## eSATA/USB



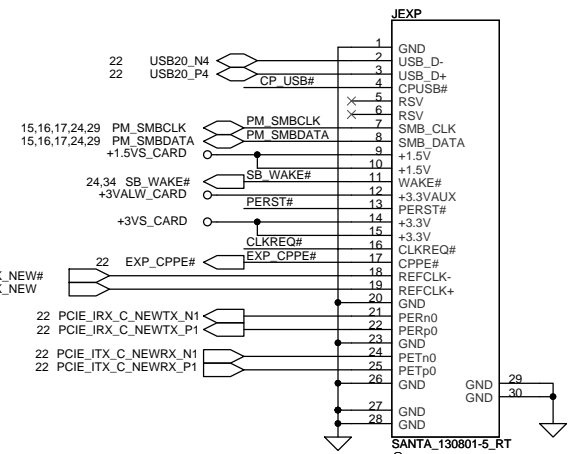
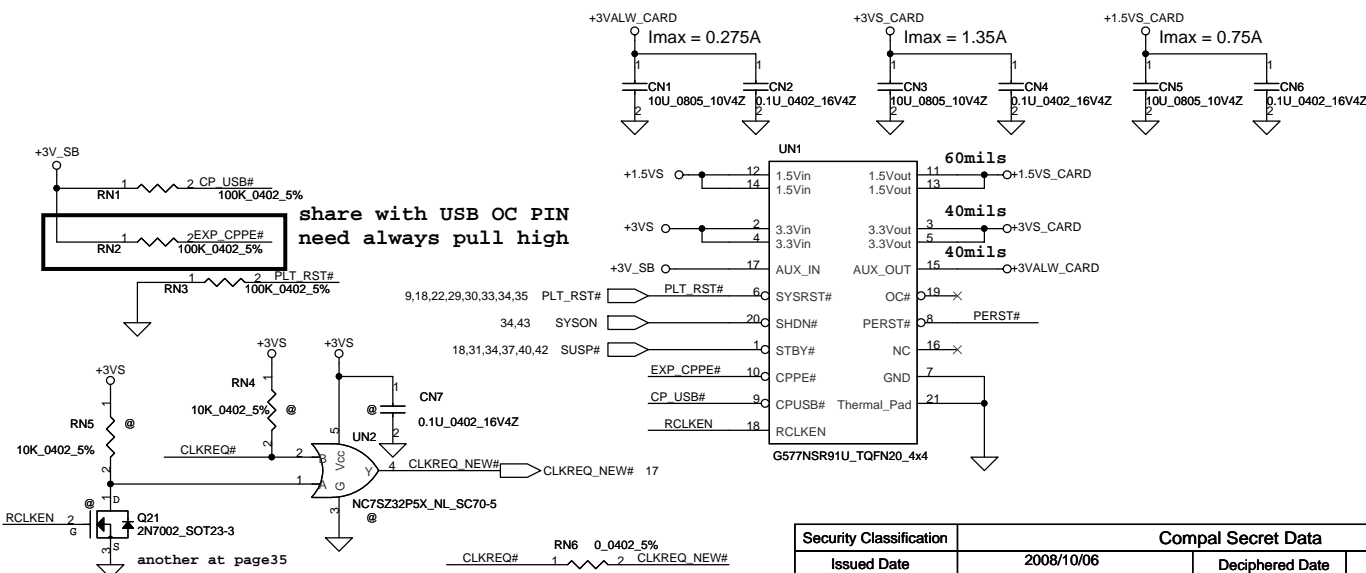
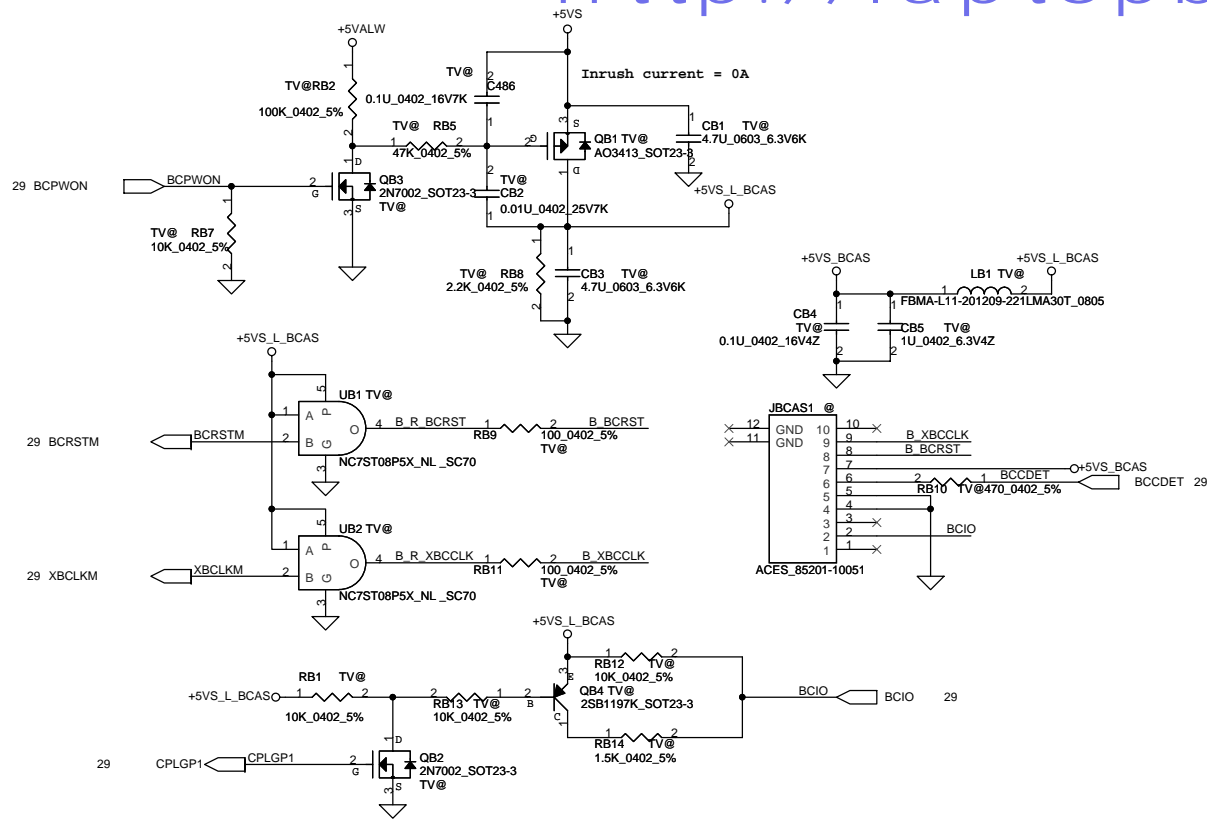
SLP_CHG	FUNCTION
LOW	D=1D
HIGH	D=2D

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Title	SCHEMATIC MD-A1822

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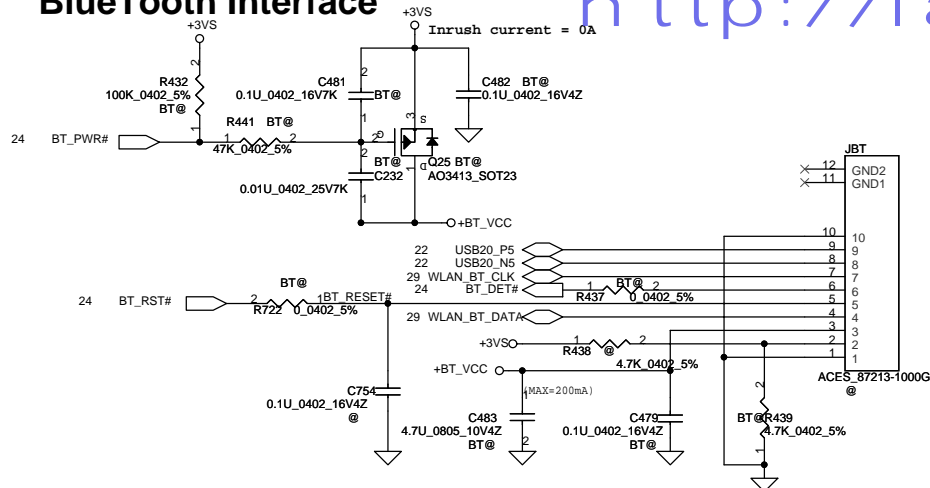
# B-CAS Circuit



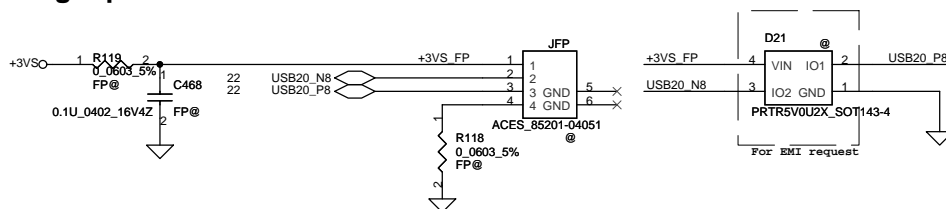
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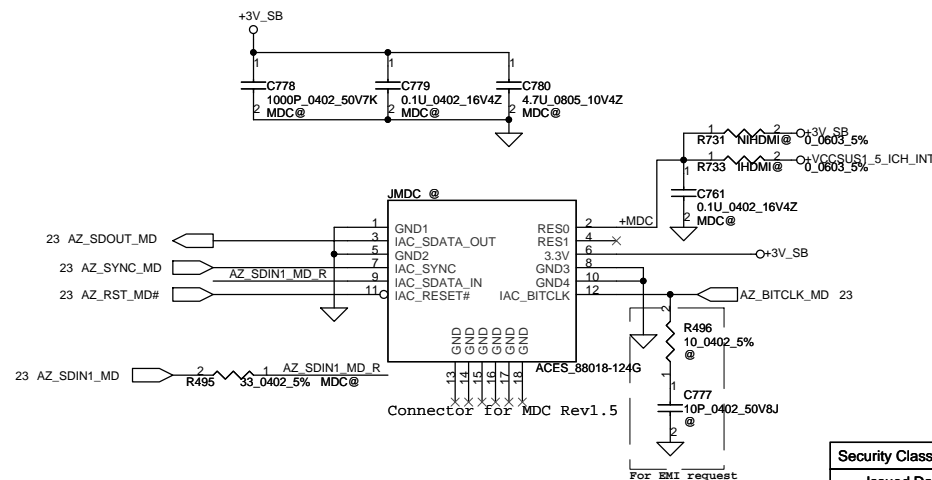
## Bluetooth Interface



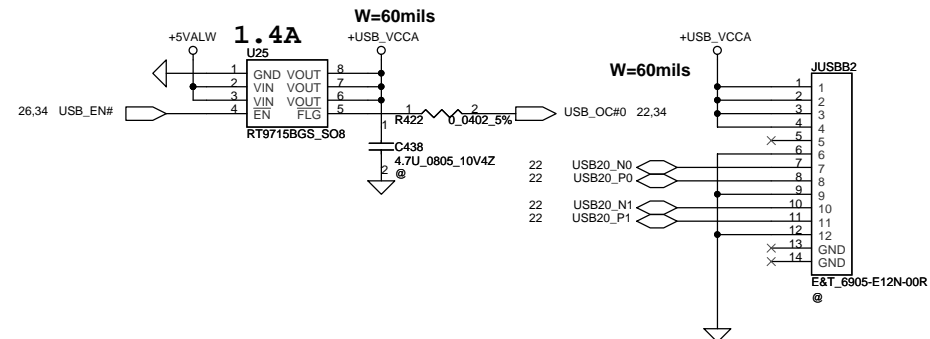
## Finger printer



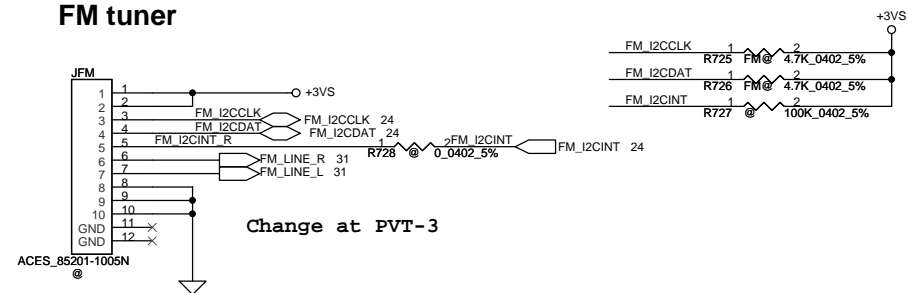
**MDC 1.5 Conn.**



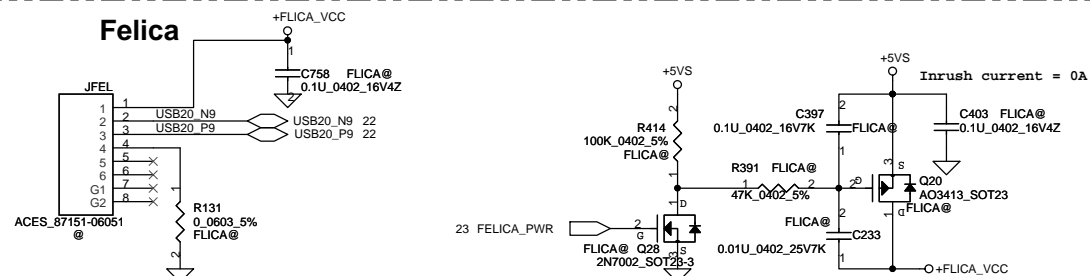
# Right USB Board



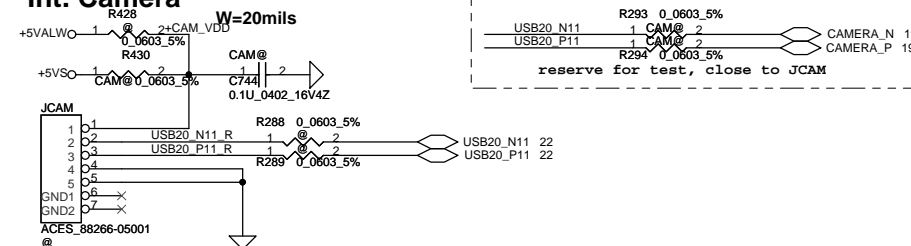
## FM tuner



## Felica

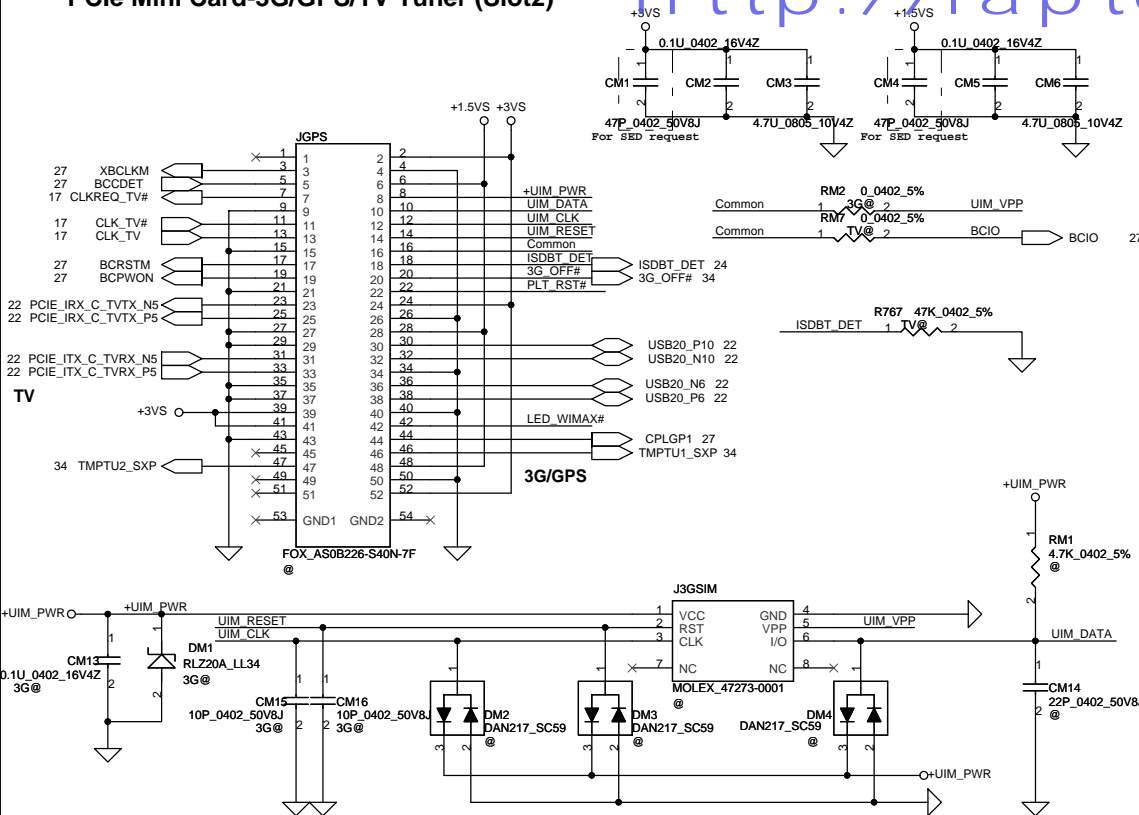


### Int. Camera

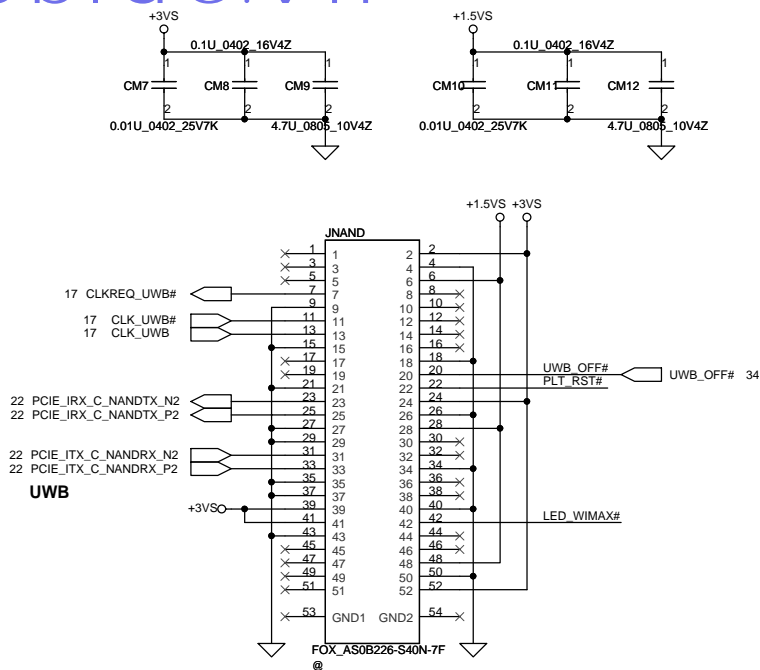


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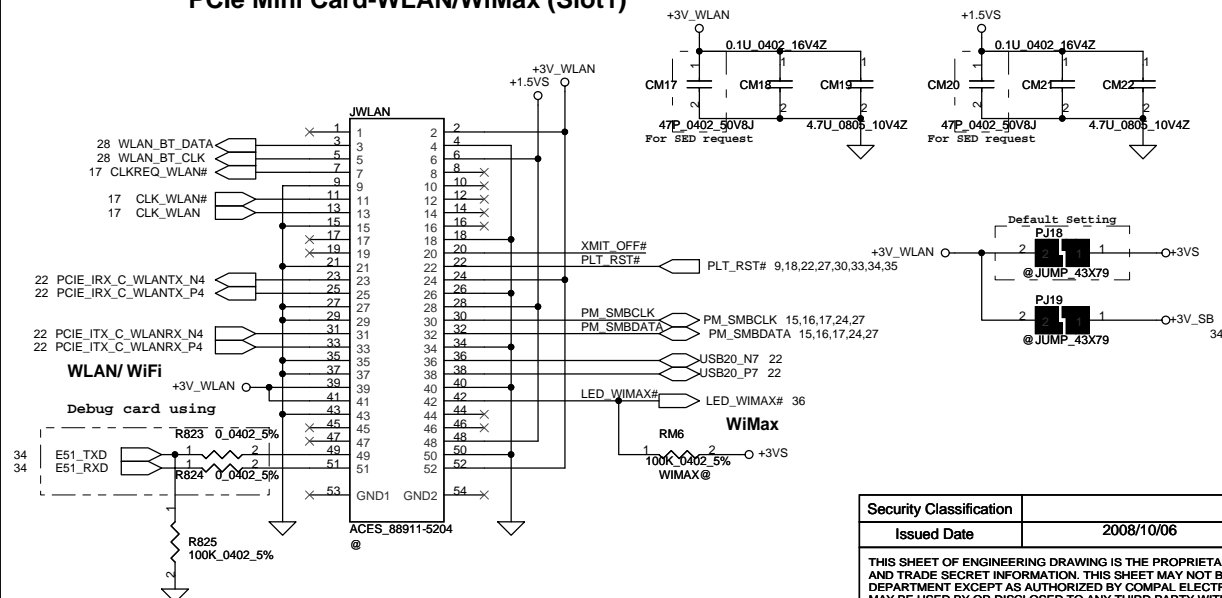
## PCIe Mini Card-3G/GPS/TV Tuner (Slot2)



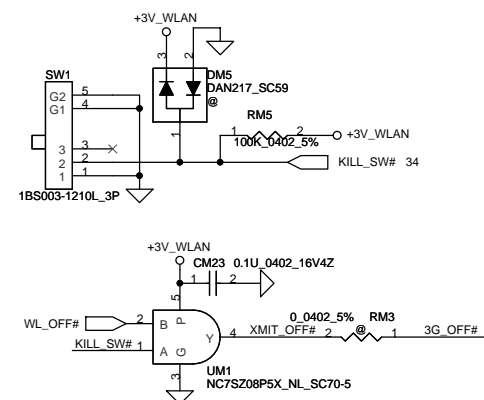
## UWB/JET (Slot3)



## PCIe Mini Card-WLAN/WiMax (Slot1)

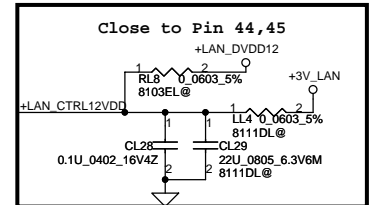
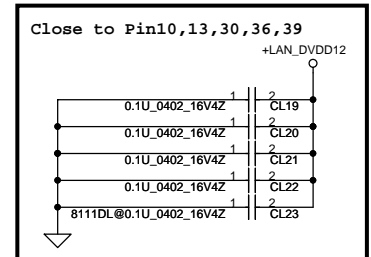
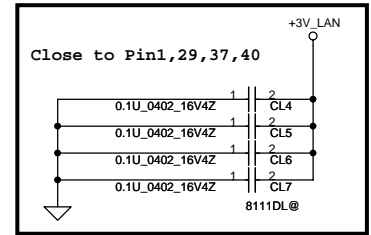
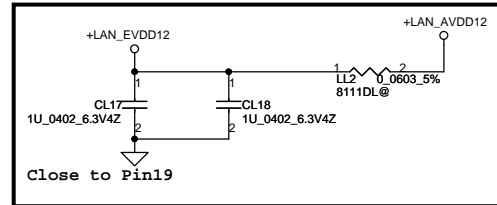
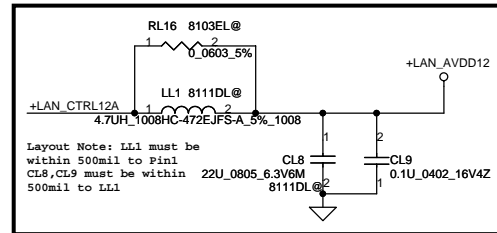
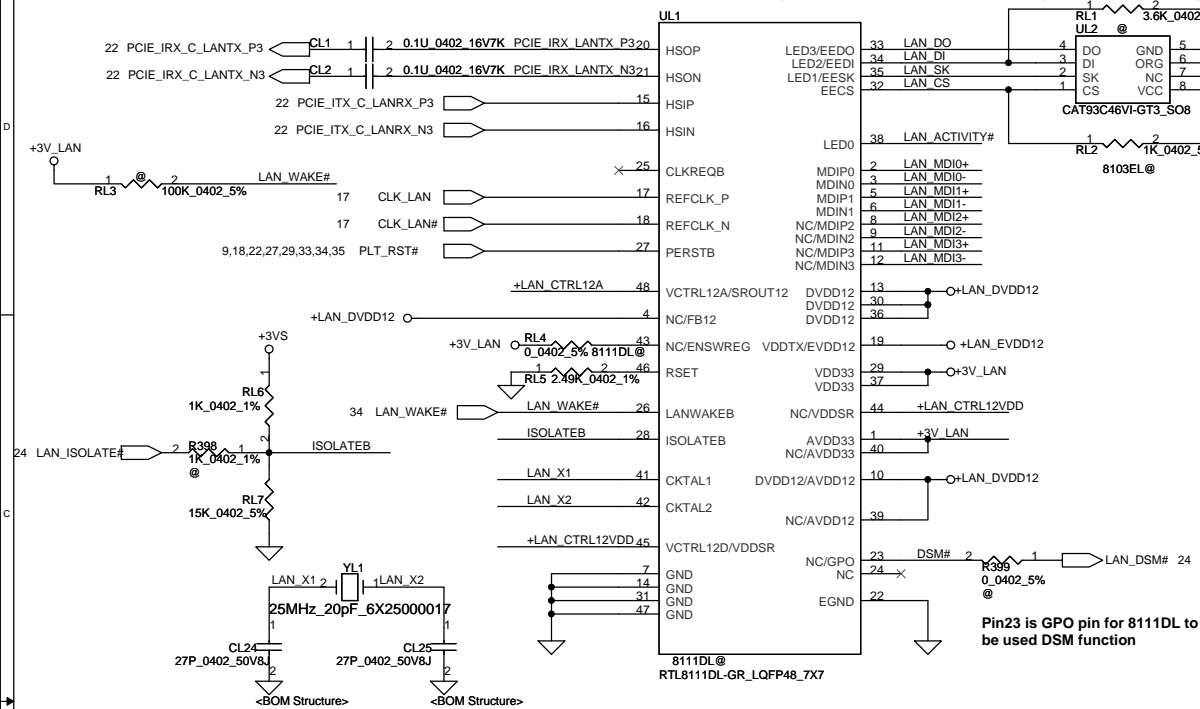


## Kill SWITCH



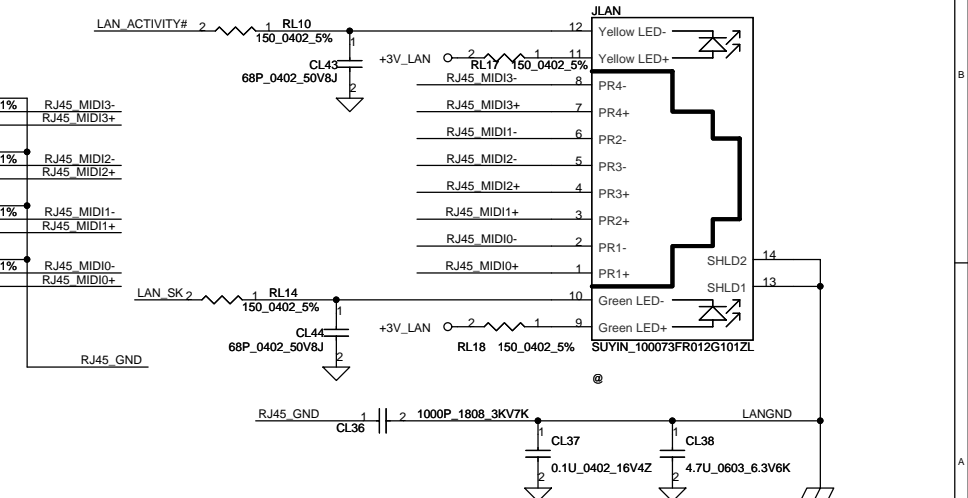
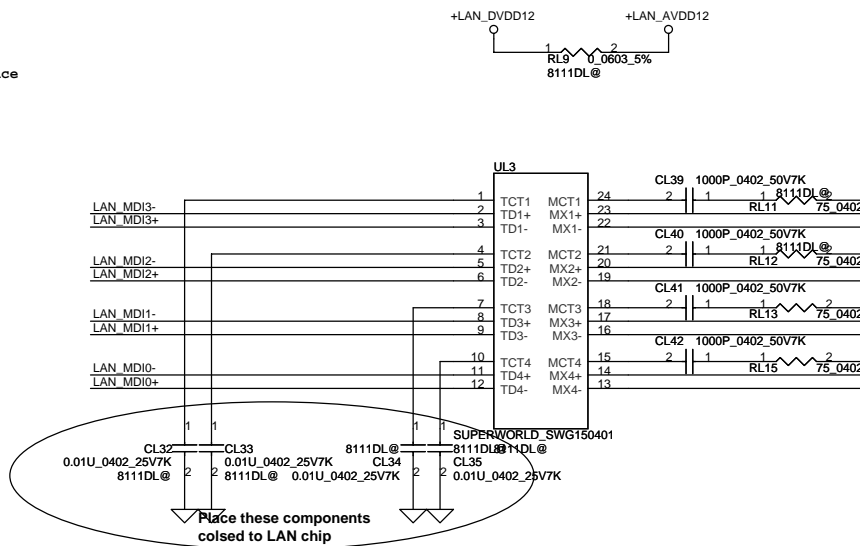
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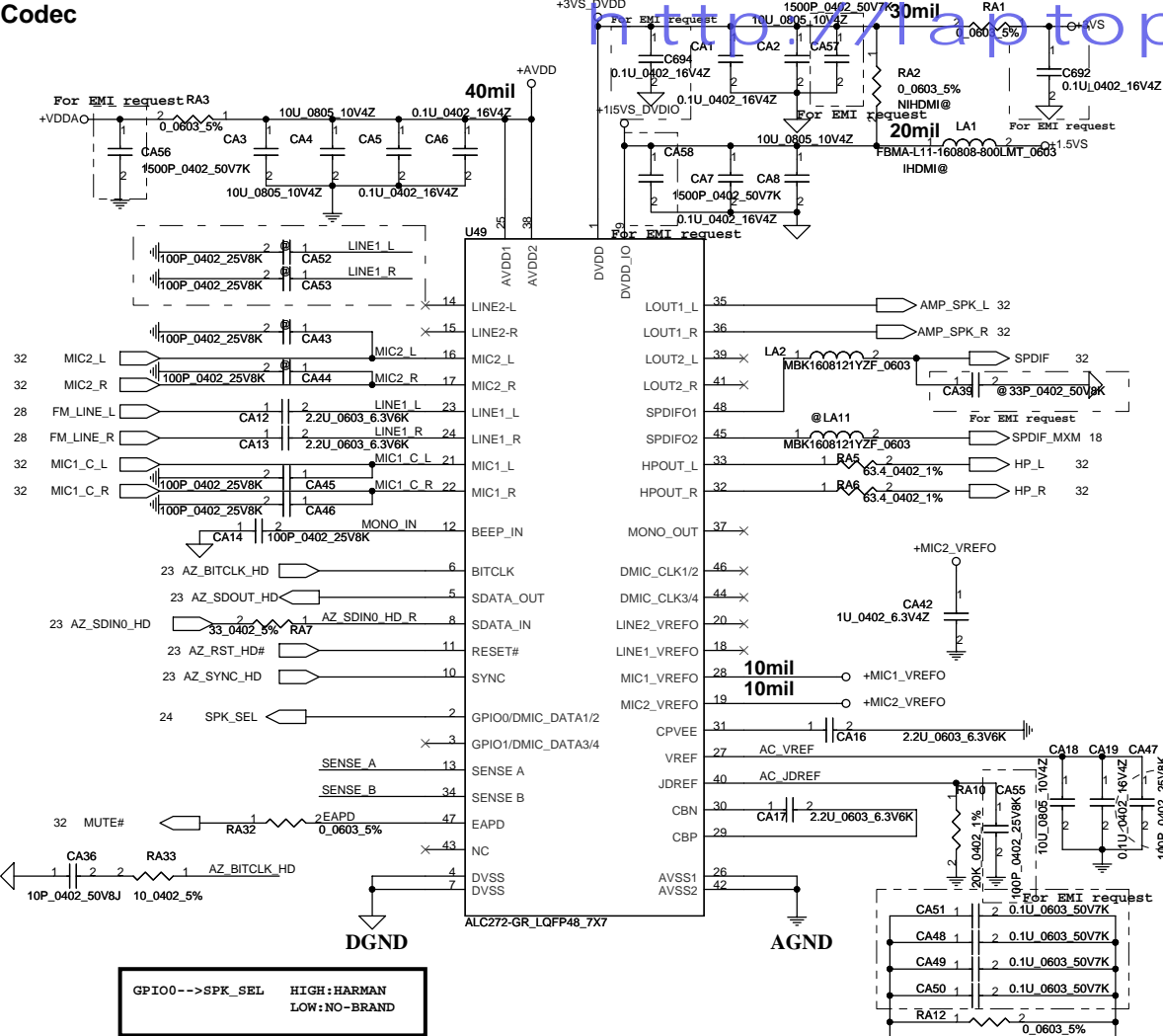


pin assignments table for difference

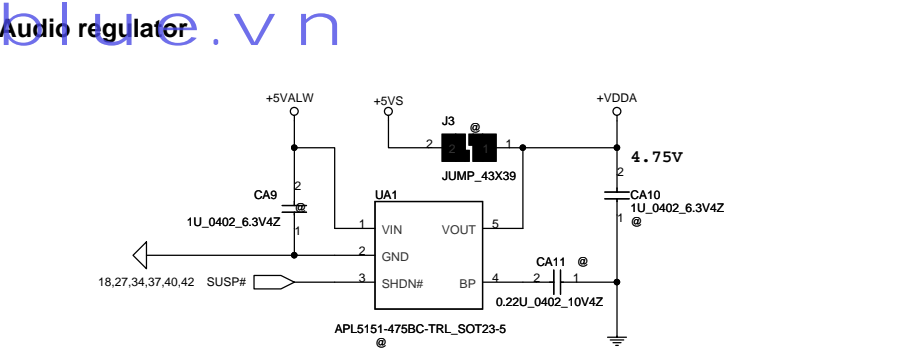
Pin	8111DL	8103EL
4	FB12	NC
8	MDIP2	NC
9	MDIN2	NC
10	AVDD12	DVDD12
11	MDIP3	NC
12	MDIN3	NC
19	EVDD12	VDDTX
23	GPO	NC
33	EEDO	LED3
34	EEDI	LED2
35	EESK	LED1
39	AVDD12	NC
40	AVDD33	NC
43	ENSR	NC
44	VDDSR	NC
45	VDDSR	NC
48	SR0UT12	NC



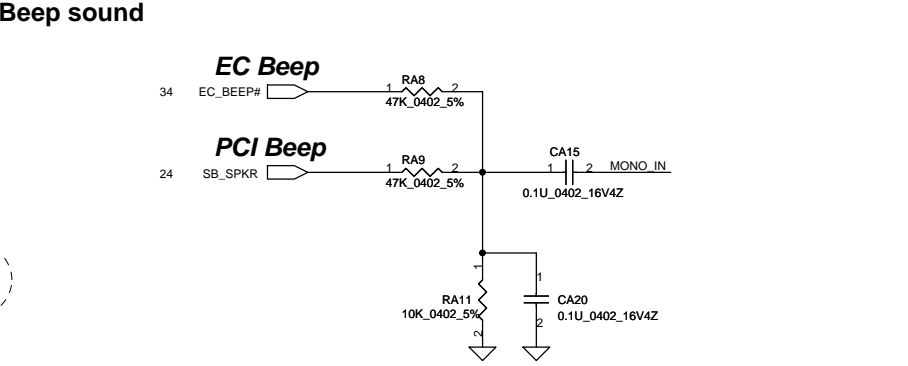
Codec



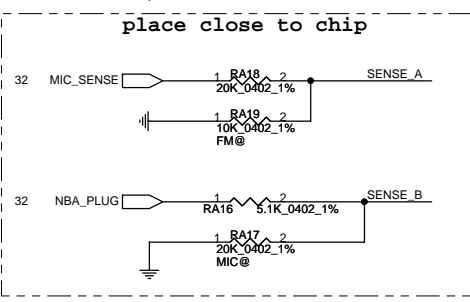
Audio regulator



BEEP sound



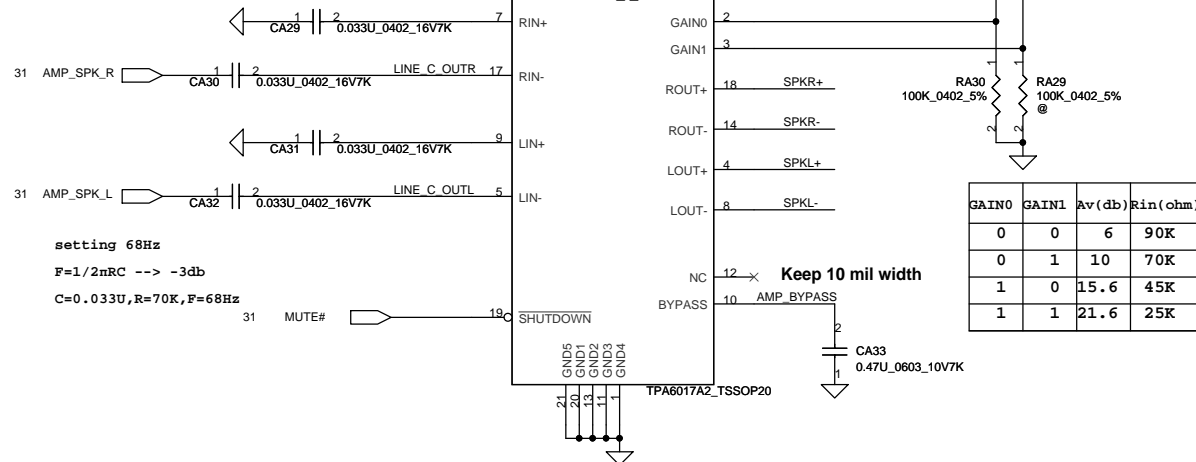
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	FM tuner
SENSE B	5.1K	PORT-D (PIN 35, 36)	SPK out
	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	Headphone out



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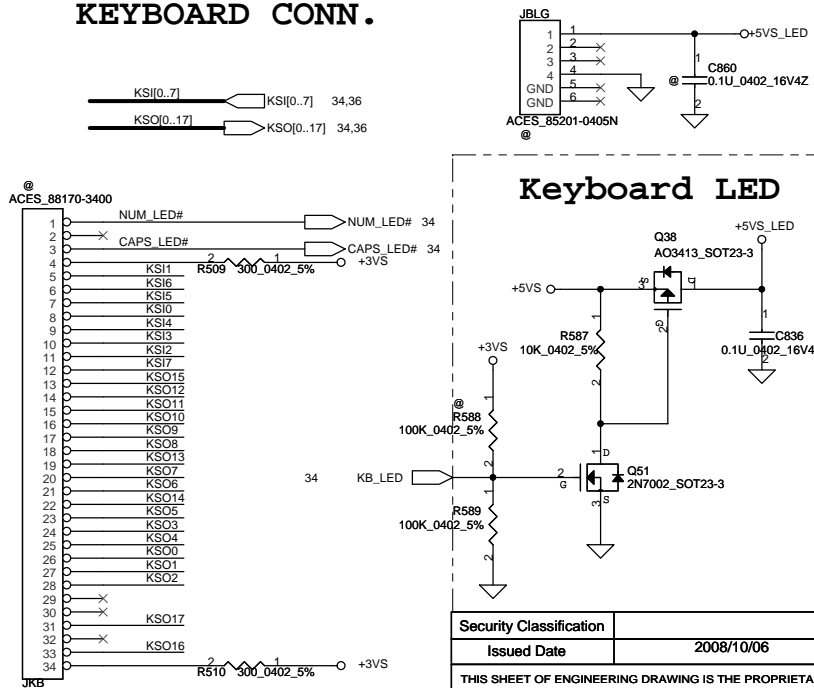
# TPA6017 Medium Range Amplifier

Rin = 70Kohm

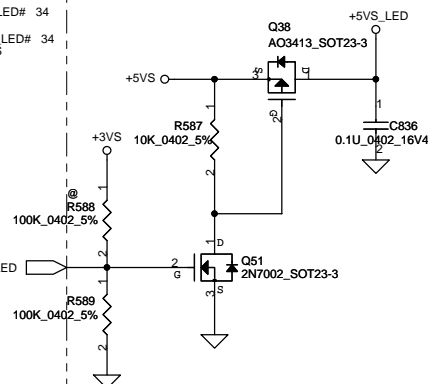


KSO10	C803	100P_0402_25V8K
KSO11	C804	100P_0402_25V8K
KSO12	C805	100P_0402_25V8K
KSO15	C807	100P_0402_25V8K
KSI7	C808	100P_0402_25V8K
KSI2	C810	100P_0402_25V8K
KSI3	C811	100P_0402_25V8K
KSI4	C812	100P_0402_25V8K
KSI0	C813	100P_0402_25V8K
KSI5	C814	100P_0402_25V8K
KSI6	C815	100P_0402_25V8K
KSI1	C816	100P_0402_25V8K
CAPS_LED#	C817	100P_0402_25V8K
NUM_LED#	C819	100P_0402_25V8K
KSO16	C809	100P_0402_25V8K
KSO17	C806	100P_0402_25V8K
KSO2	C793	100P_0402_25V8K
KSO1	C790	100P_0402_25V8K
KSO0	C791	100P_0402_25V8K
KSO4	C792	100P_0402_25V8K
KSO3	C795	100P_0402_25V8K
KSO5	C796	100P_0402_25V8K
KSO14	C797	100P_0402_25V8K
KSO6	C798	100P_0402_25V8K
KSO7	C799	100P_0402_25V8K
KSO13	C800	100P_0402_25V8K
KSO8	C801	100P_0402_25V8K
KSO9	C802	100P_0402_25V8K

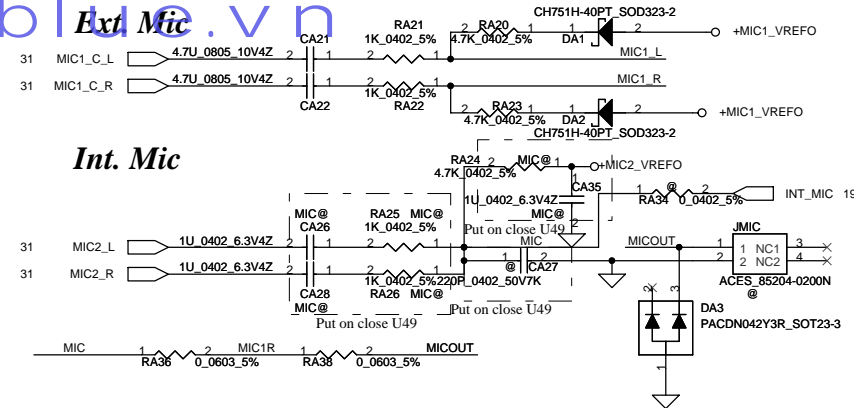
## KEYBOARD CONN.



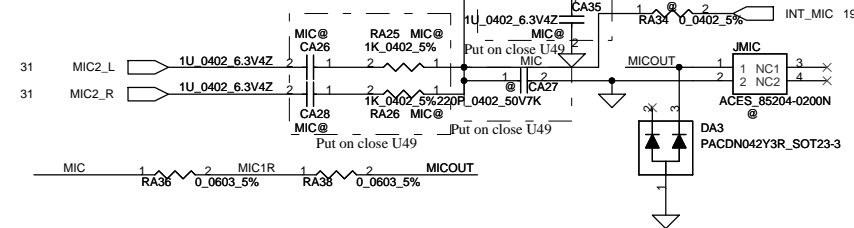
## Keyboard LED



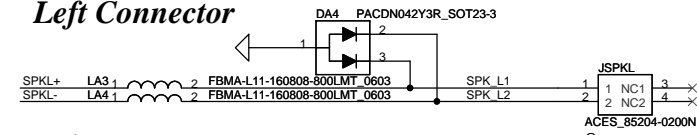
# Ext Mic



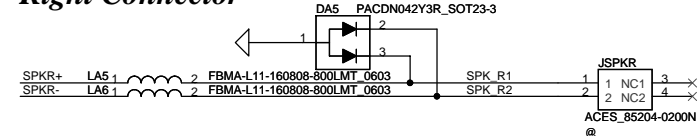
## Int. Mic



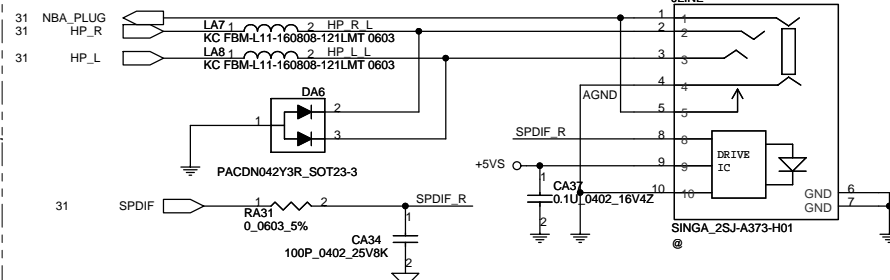
## Left Connector



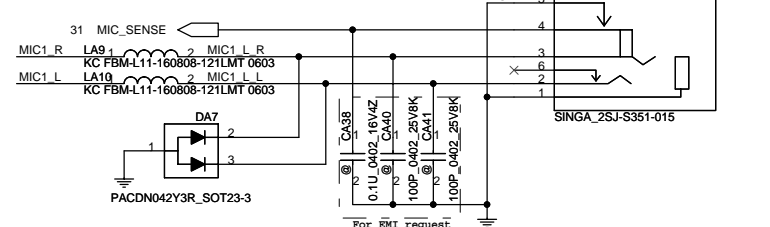
## Right Connector



## HeadPhone/LINE Out JACK

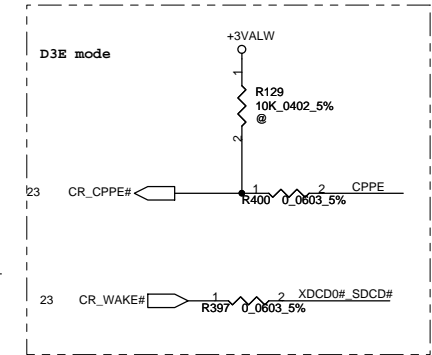
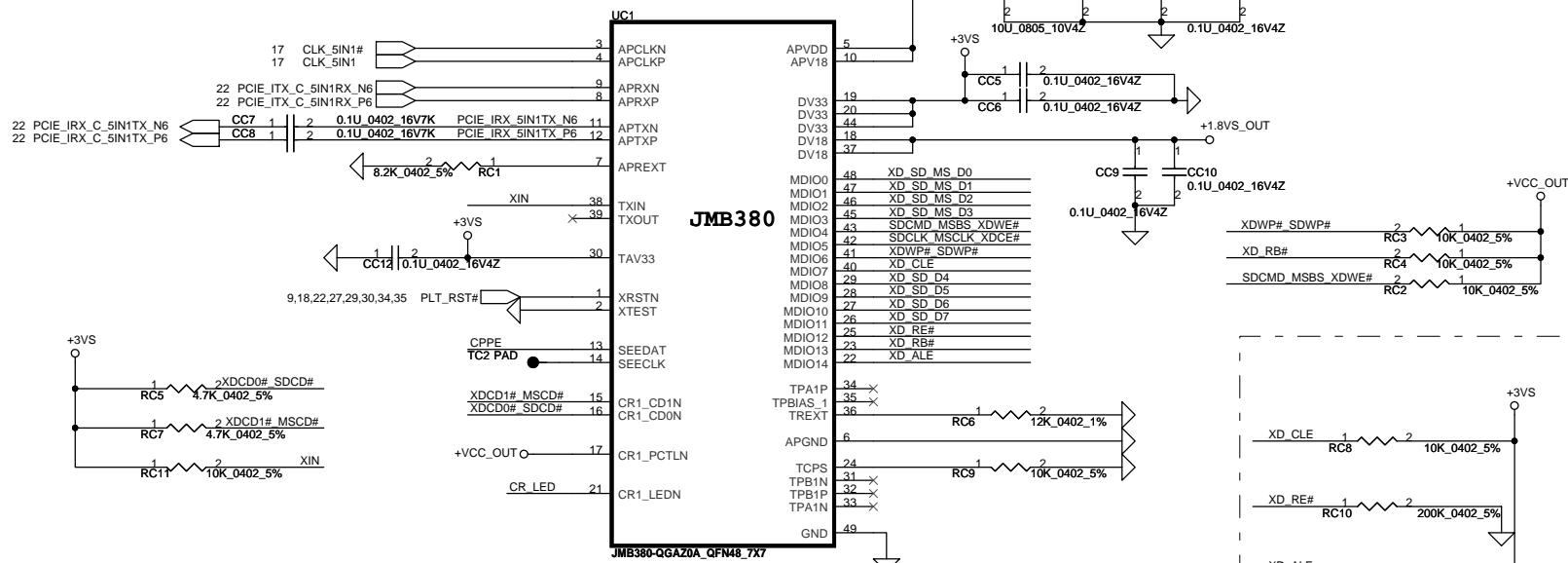


## Ext.MIC/LINE IN JACK



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## Power Circuit

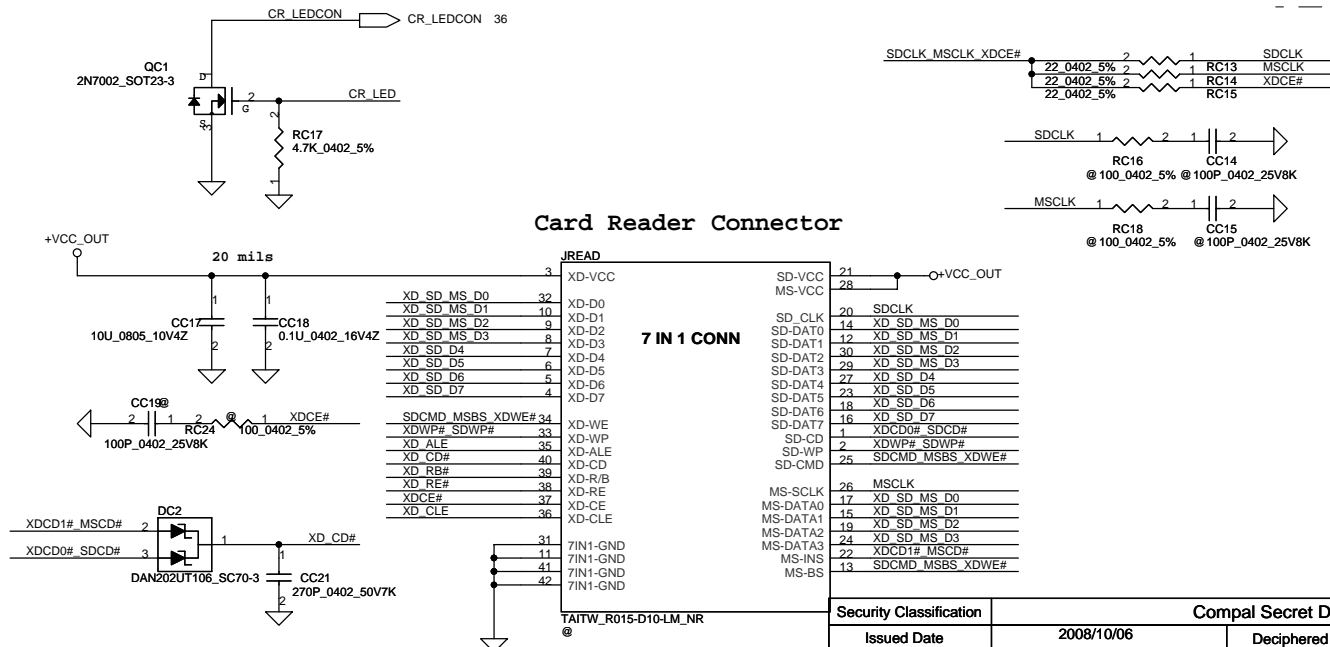


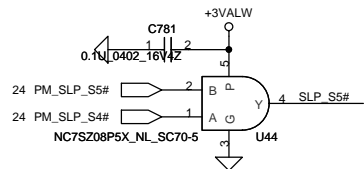
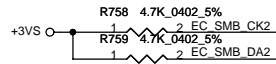
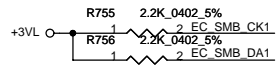
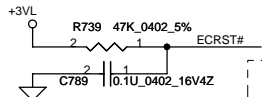
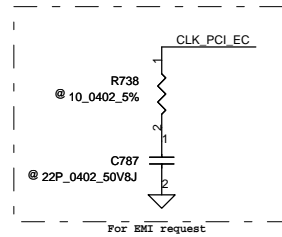
## Strapping setting

Pin name	Description	
	High	low
MDIO7	on-board	add-in card
MDIO12	+VCC_OUT high active	+VCC_OUT low active
MDIO14	CR_LED high active	CR_LED low active

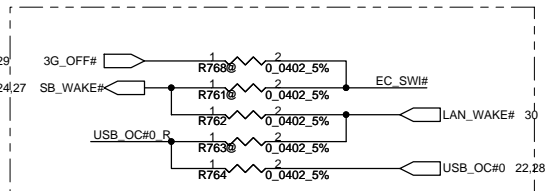
P.S CR1\_PCTLN aslo can out 3V with 250mA for 5IN1 using.(MDIO12 can't be seted after MP IC)

## Card Reader Connector

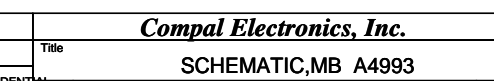
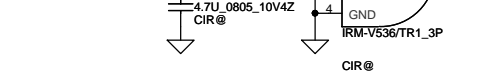
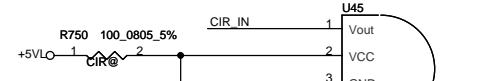
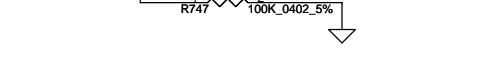
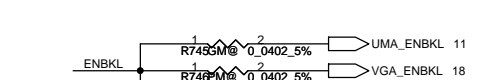
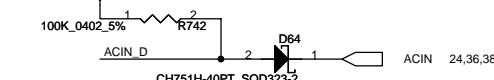
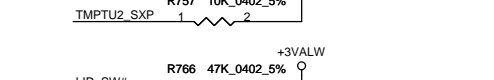
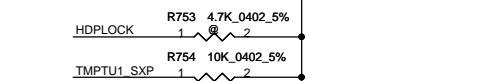
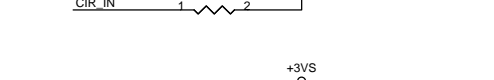
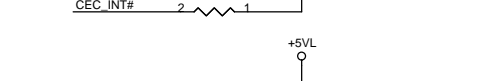
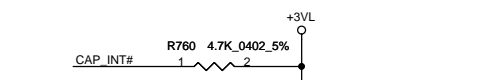
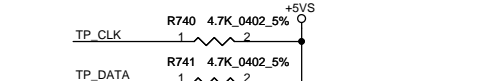
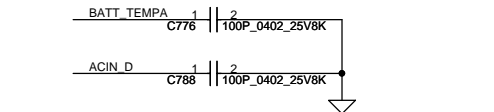
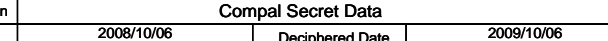
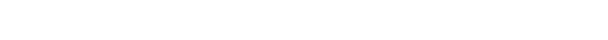
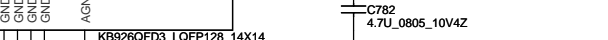
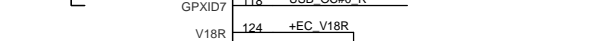
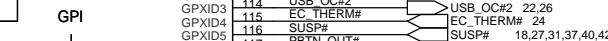
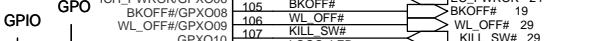
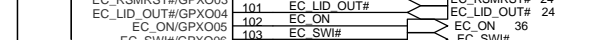
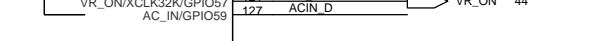
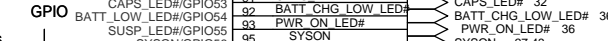
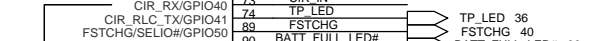
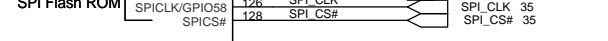
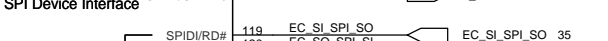
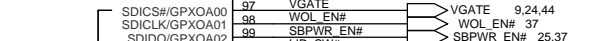
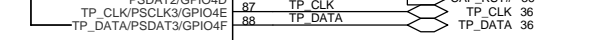
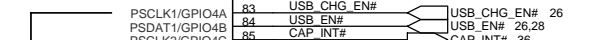
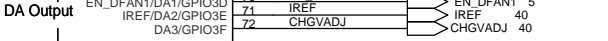
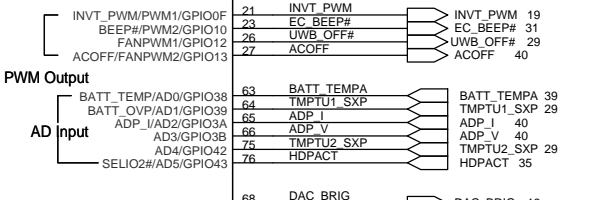
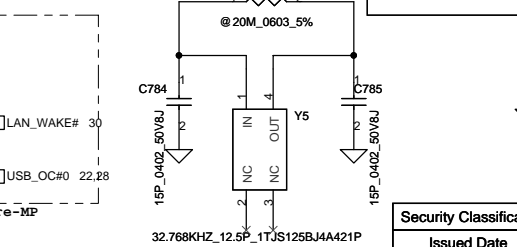
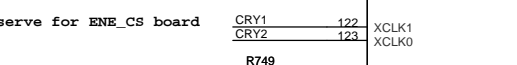
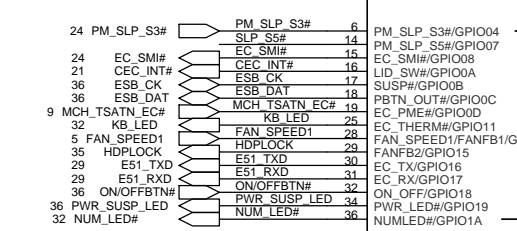
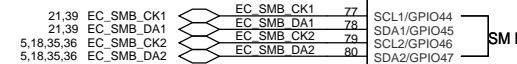
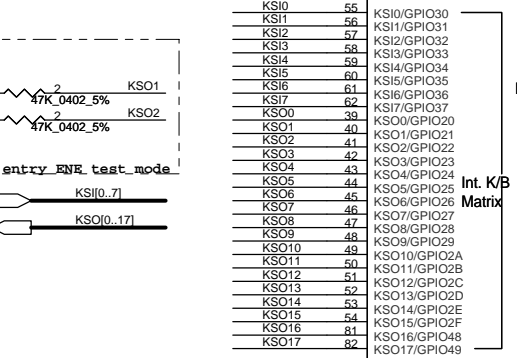
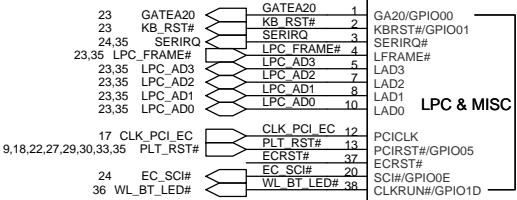
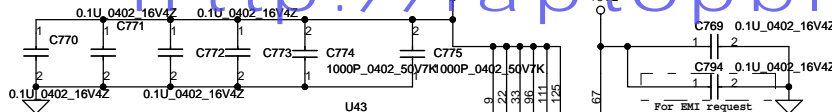




reserve for ENE\_CS board

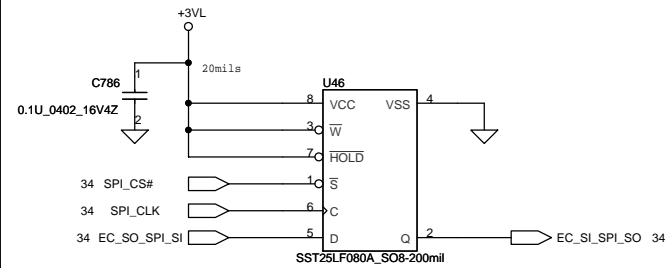


The circuit is reserve for new design for pre-MP

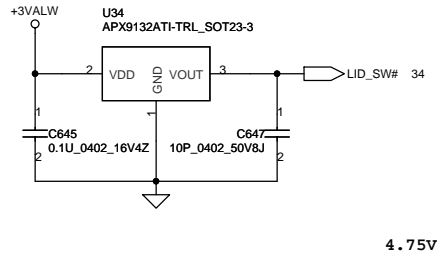


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## SPI Flash (16Mb\*1)

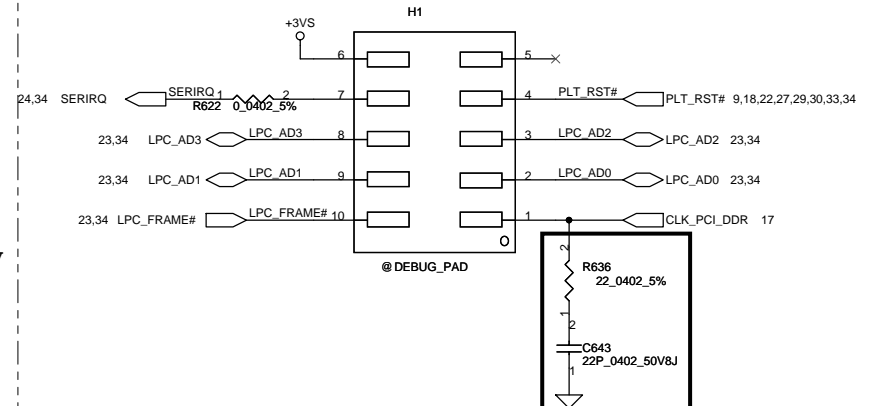


## Lid SW

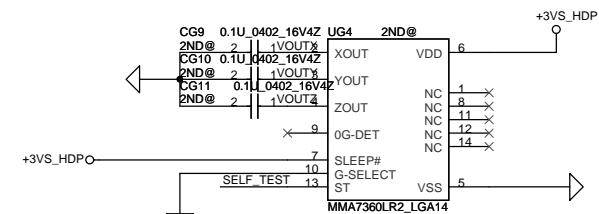
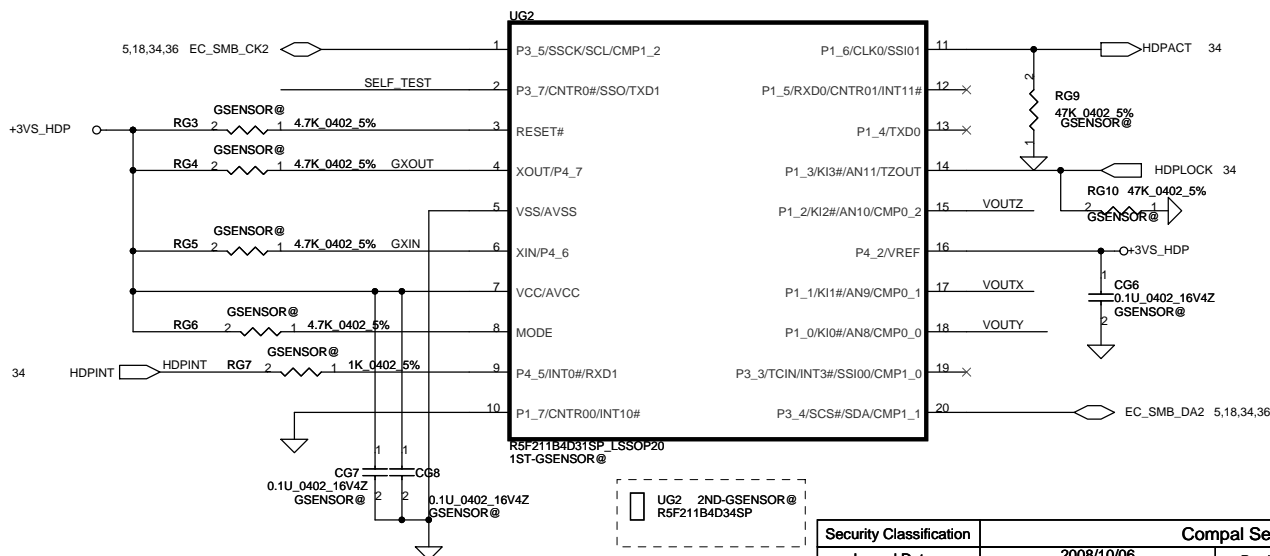
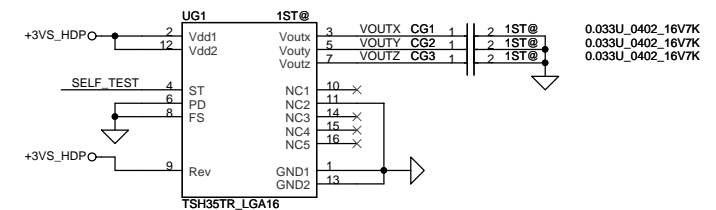
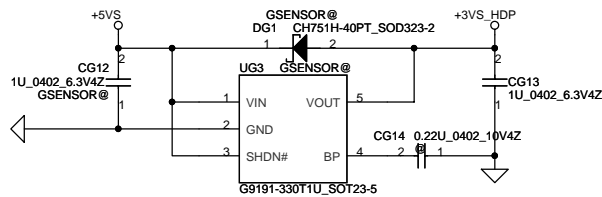


## LPC Debug Port

Please place the PAD under DDR DIMM.



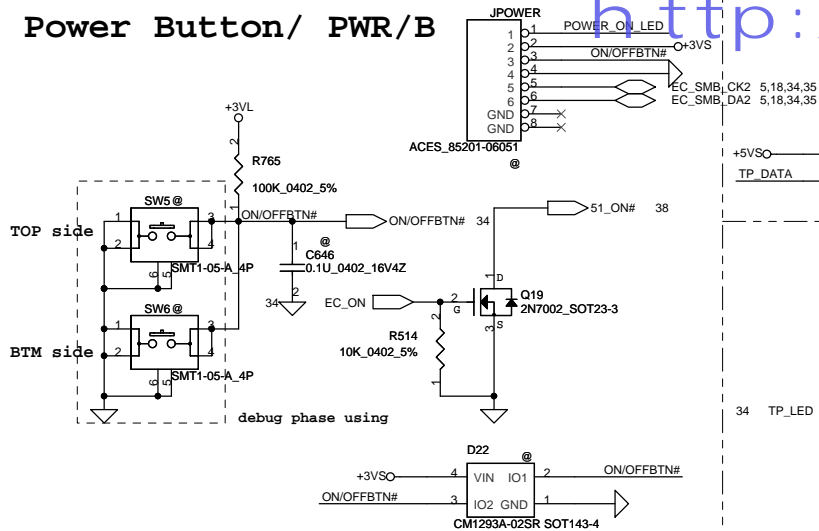
## G-Sensor



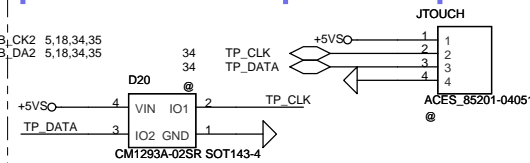
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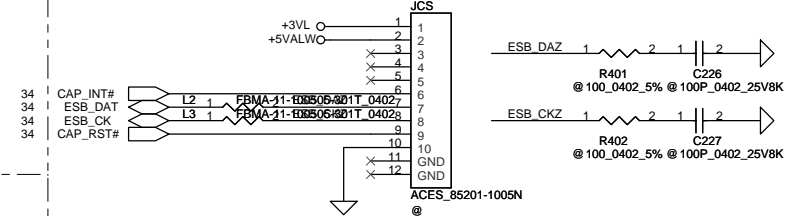
## Power Button/ PWR/B



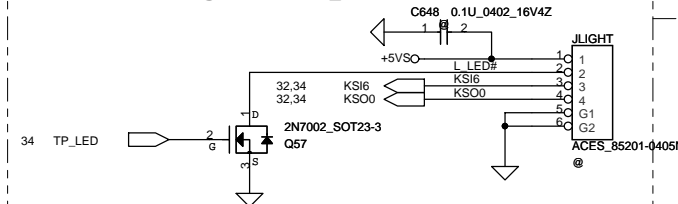
## Touch/B Connector



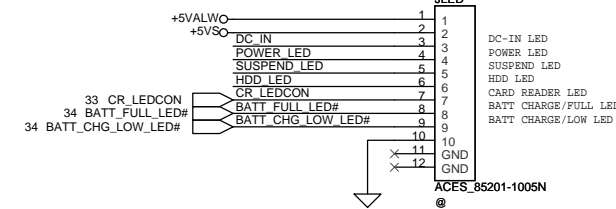
## Caps Sensor Connector



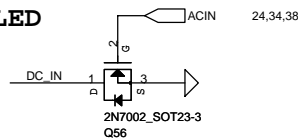
## Light Pipe Connector



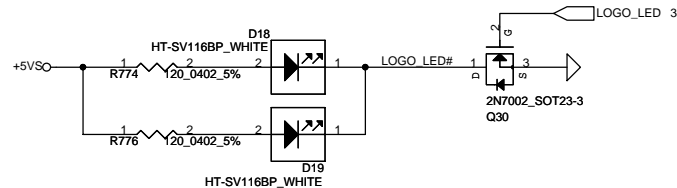
## LED/B Connector



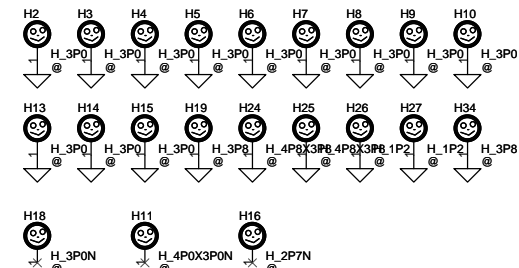
## DC-IN LED



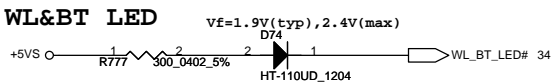
## Satellite LED



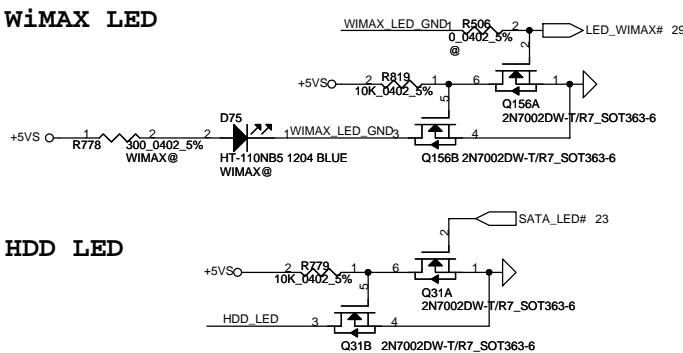
## Screw Hole



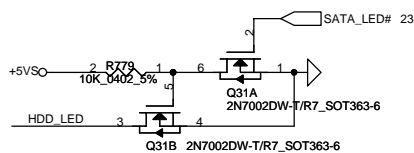
## WL&BT LED



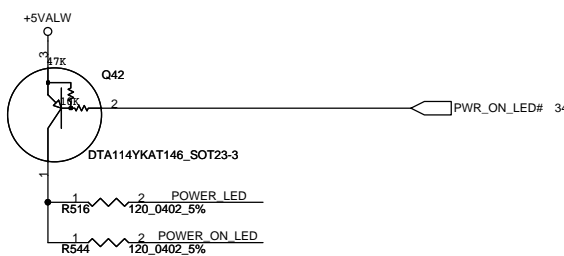
## WiMAX LED



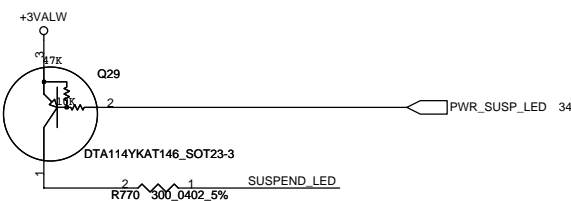
## HDD LED



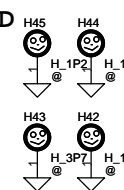
## POWER LED



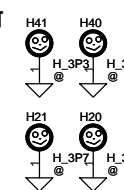
## SUSPEND LED



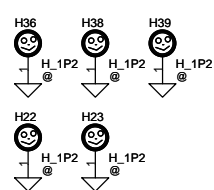
## JNAND



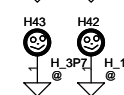
## JWLAN



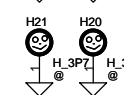
## SSD



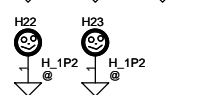
## JGPS



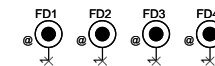
## VGA



## MDC



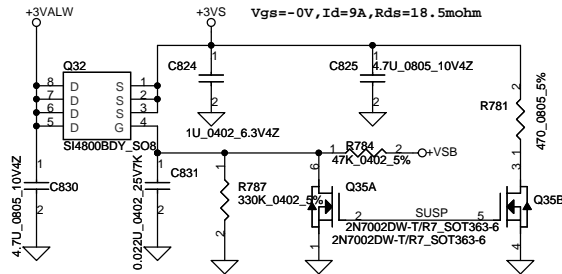
## PCB Federal Mark PAD



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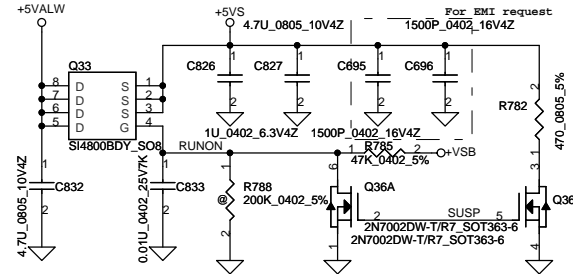
### +3VALW TO +3VS

Inrush current = 0A  
Vgs=-0V, Id=9A, Rds=18.5mohm



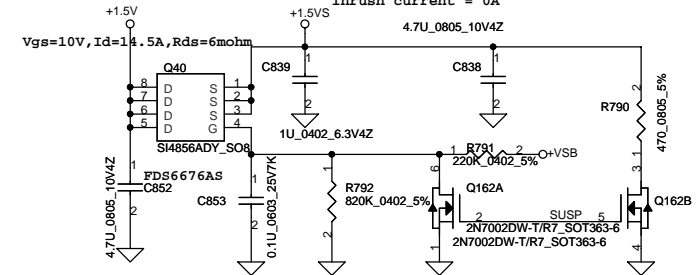
### +5VALW TO +5VS

Inrush current = 0A



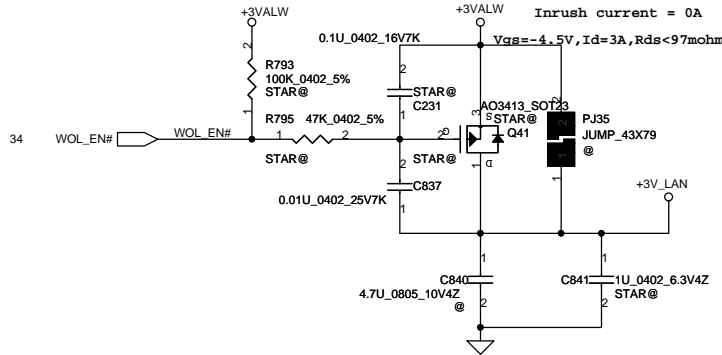
### +1.5V to +1.5VS

Inrush current = 0A



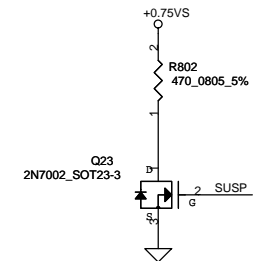
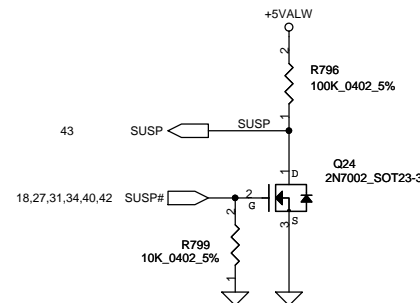
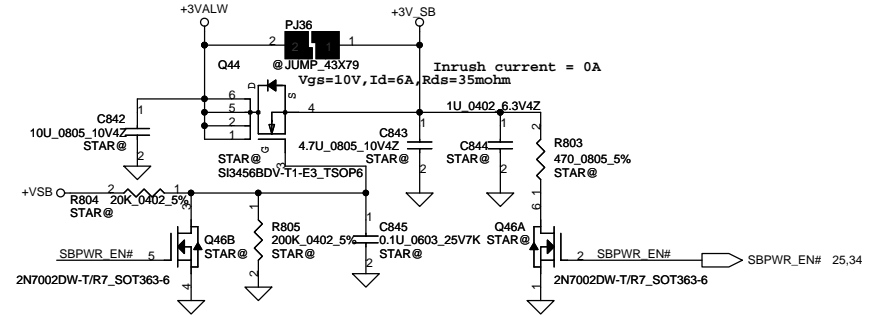
### +3VALW TO +3V\_LAN

Inrush current = 0A



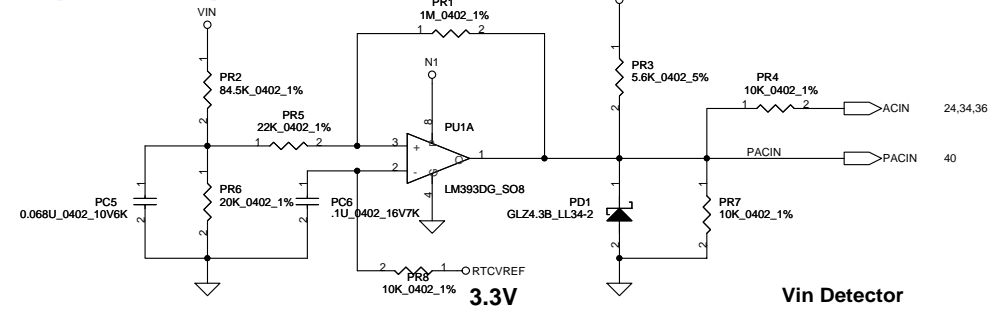
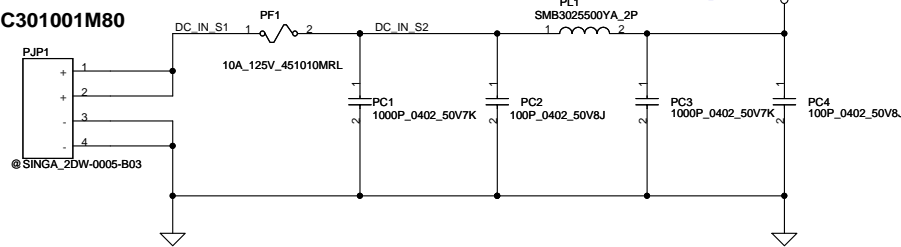
### +3VALW TO +3V\_SB

Inrush current = 0A



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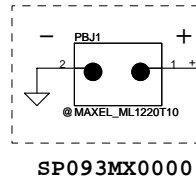
# DC301001M80



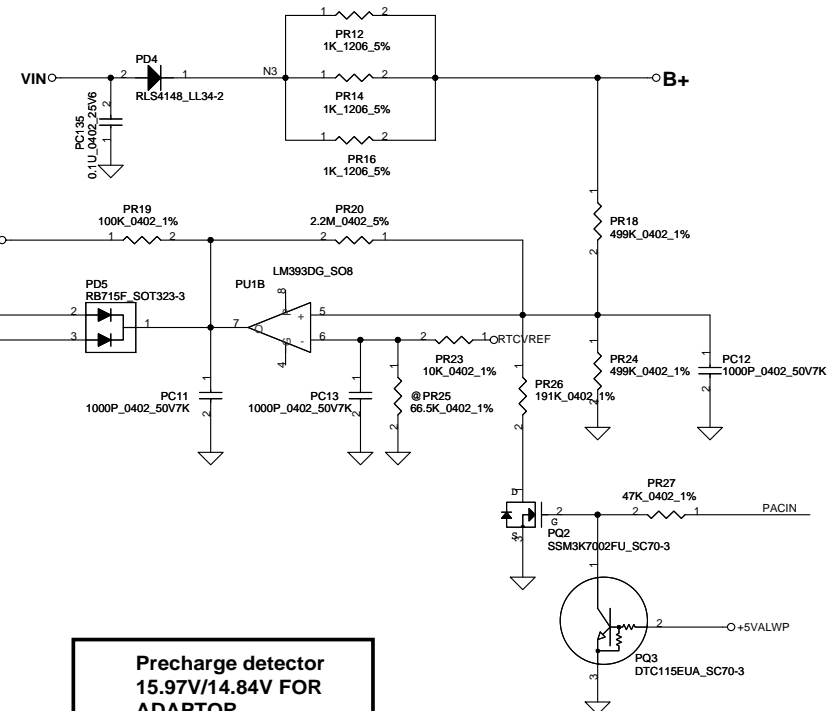
## Vin Detector

High 18.384 17.901 17.430  
Low 17.728 17.257 16.976

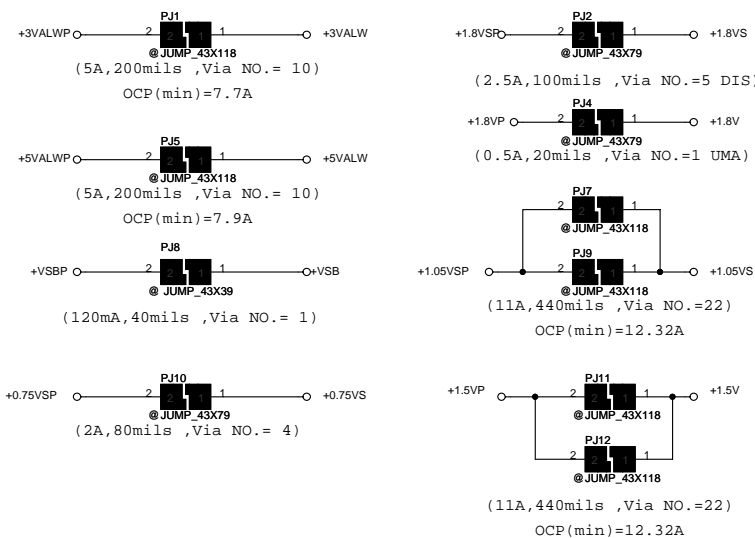
## RTC Battery



41 EN0  
40 ACON



Precharge detector  
15.97V/14.84V FOR  
ADAPTOR

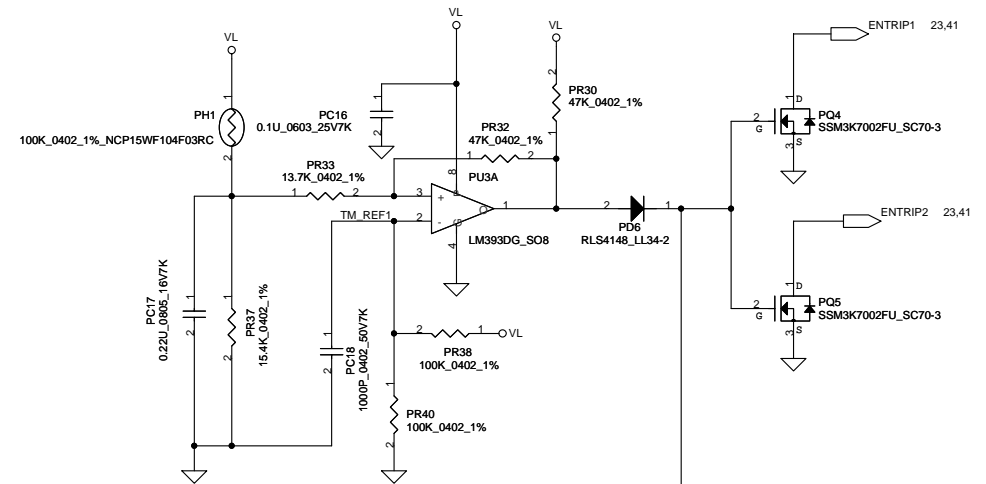


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PH1 under CPU botten side :

CPU thermal protection at 92 degree C

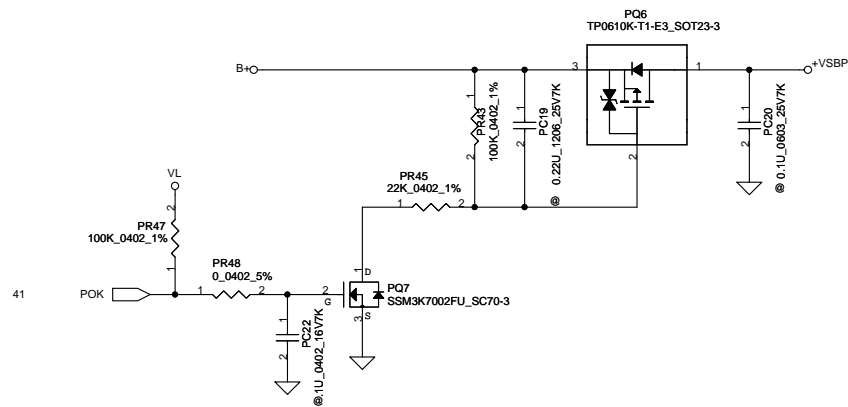
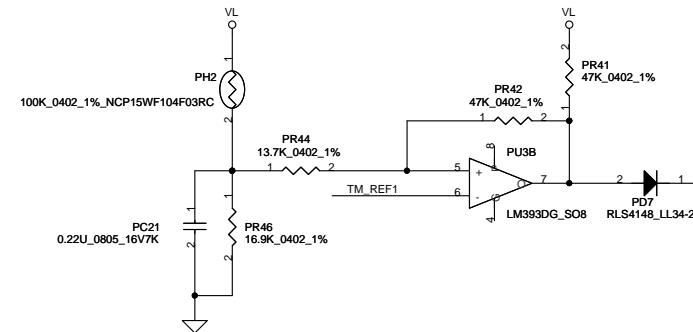
Recovery at 56 degree C



PH2 near main Battery CONN :

BAT. thermal protection at 90 degree C

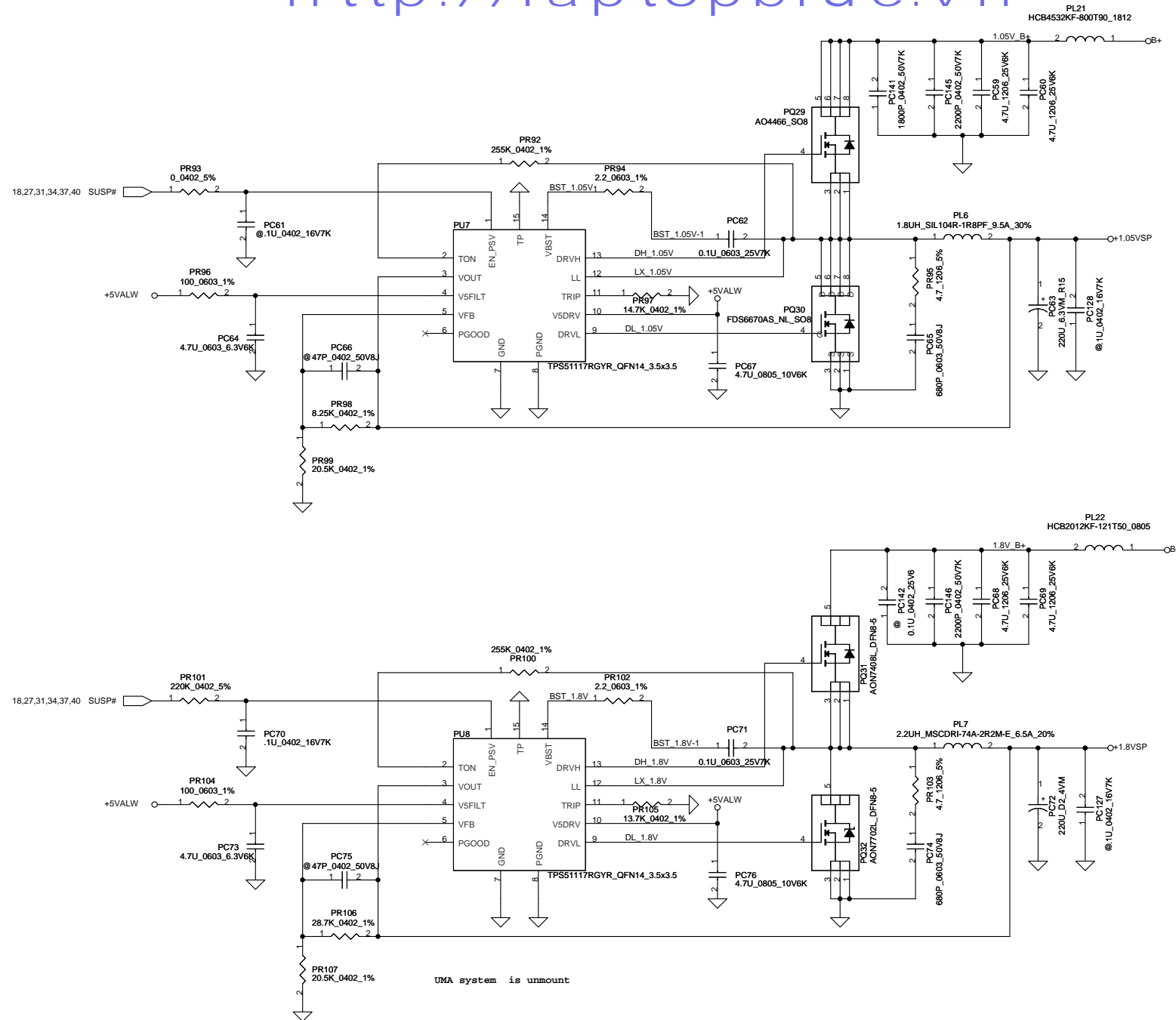
Recovery at 53 degree C

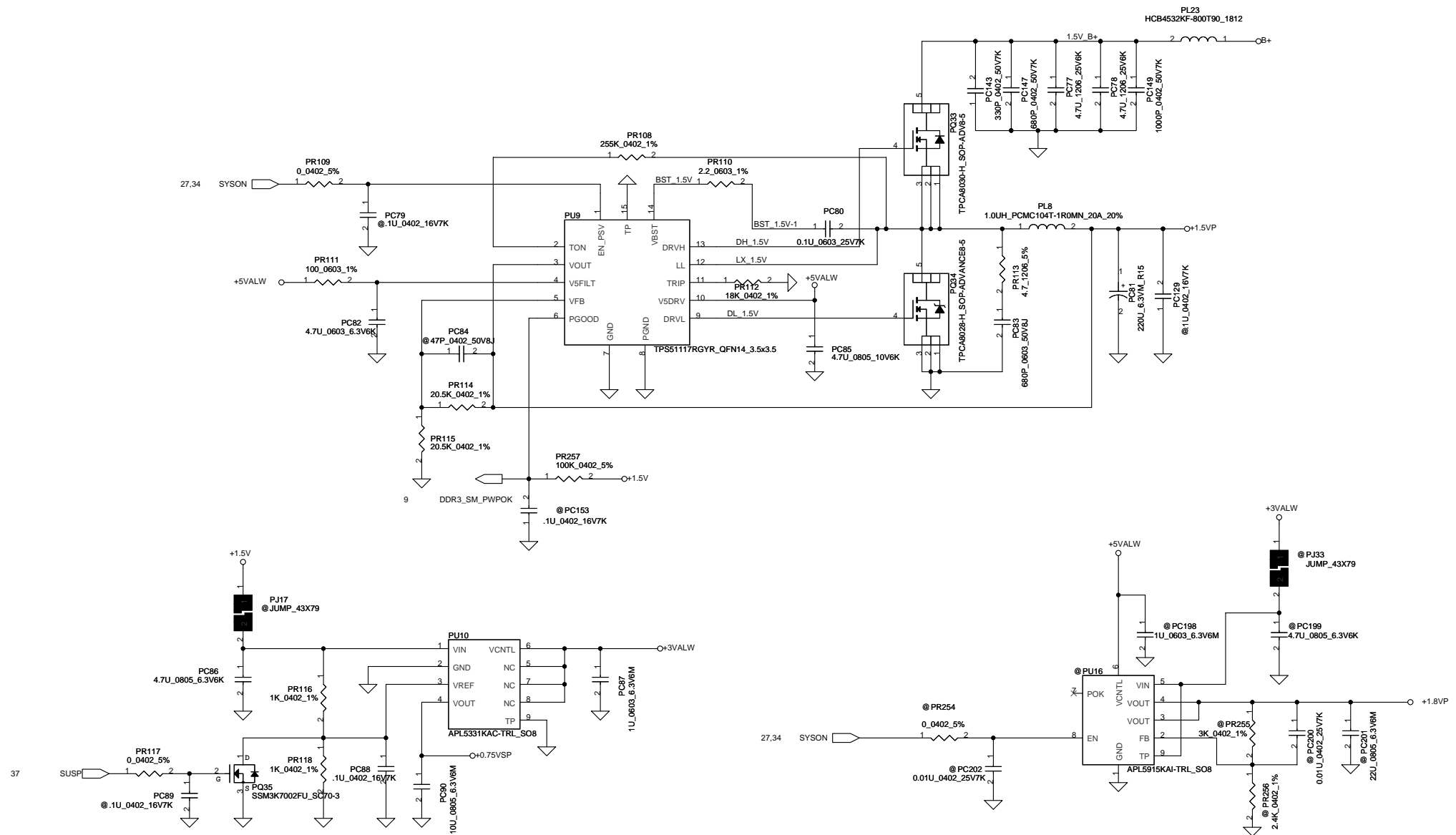






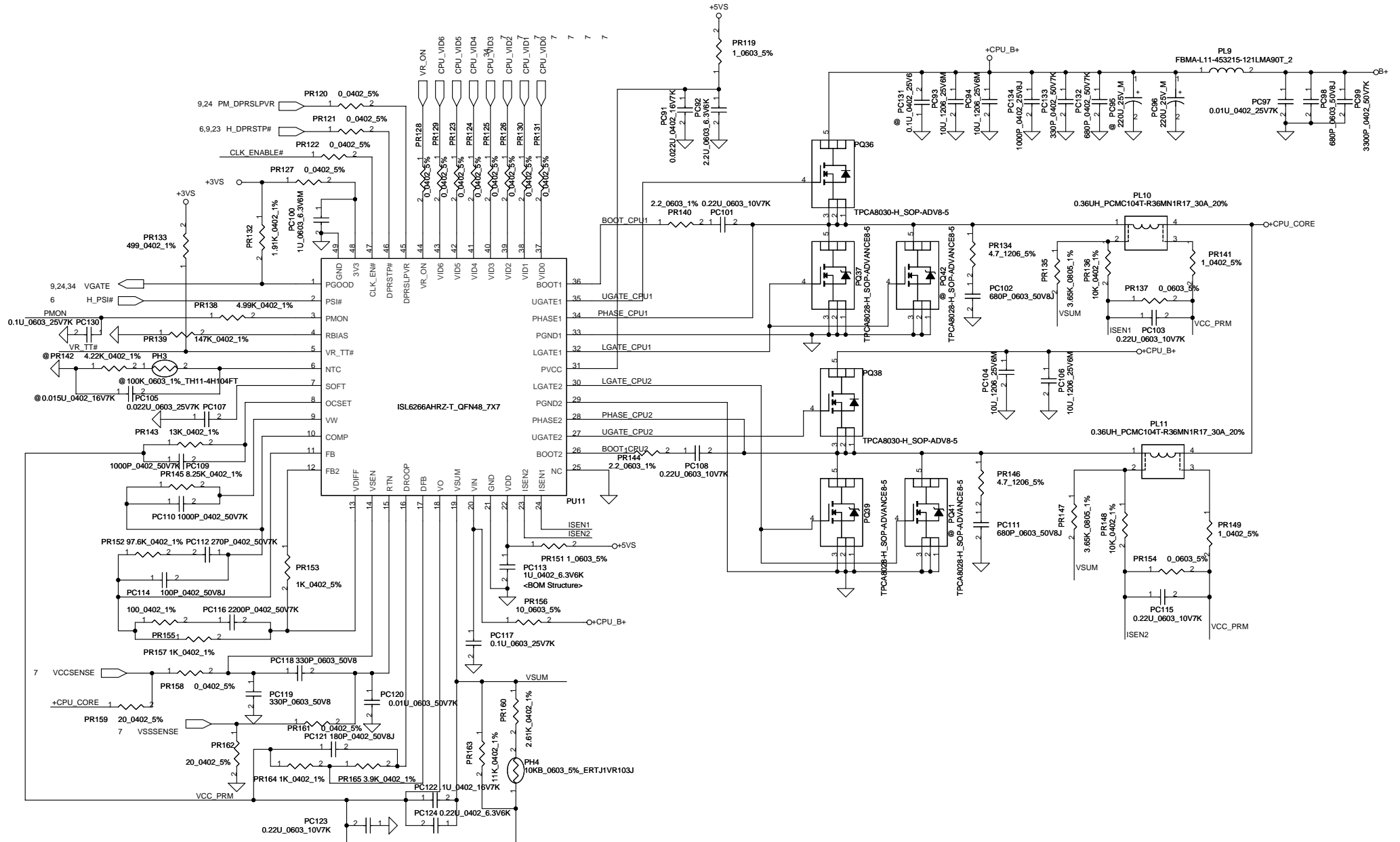






Discrete system is unmount @

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38-44	DVT Release	2009/06/03			
42	Change PQ31,PQ32,PC72,PL7	2009/06/10	POWER		Change to small size
43	Change PC81	2009/06/10	POWER		Change to POSCAP

# ISPD

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