

# Compal confidential

## *Bradford 10AT*

### NSKAE LA-5381P REV 0.2 Schematics Document

Mobile AMD SIG3/RS880M&RS880MC/SB710

2009-04-10 Rev. 0.2

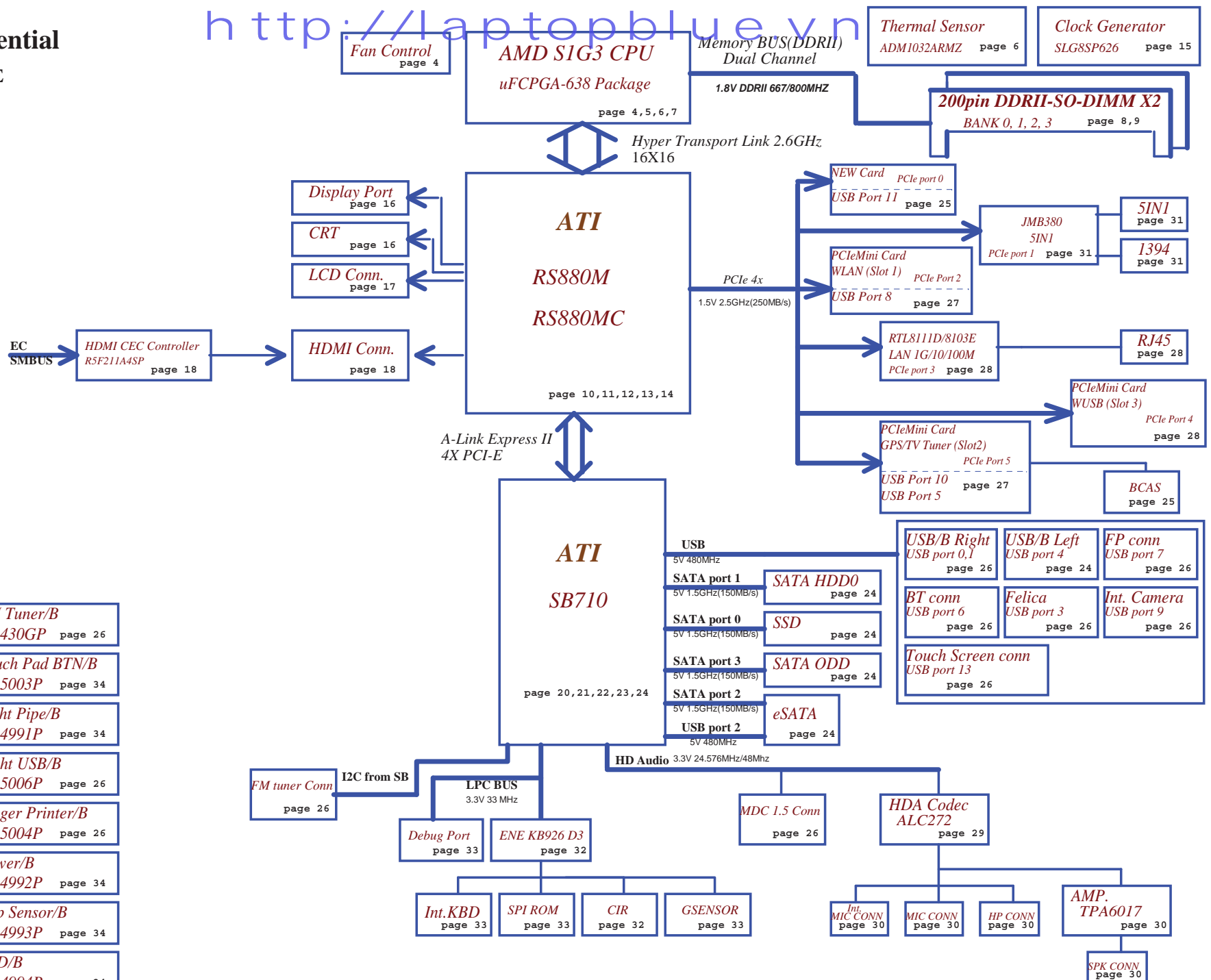
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Model Name : NSKAE

File Name : LA-5381P

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## Block Diagram

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## Voltage Rails

O MEANS ON X MEANS OFF

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Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build

Item	CPU	NB	VGA	SB
	S1G3	RS880MC	NA	SB710
	S1G3	RS880M	NA	SB710

## BTO Option Table

Function	HDMI		DIPLAY PORT	Side Port			
description				Memory			
explain	HDMI	CEC	DIPLAY PORT	Side Port	Samsung	Hynix	No Side Port
BTO	HDMI@	H@	DP@	SIDE@	SAMSIDE@	HYNSIDE@	NOSIDE@

Function	MINI PCI-E SLOT			LAN	Felica	BLUETOOTH	CRT
description							
explain	3G	B-CAS	WIMAX	10/100M	Giga	FELICA	BLUE TOOTH
BTO	3G@	TV@	WIMAX@	8103EL@	8111DL@	FEL@	BT@

Function	G-SENSOR	Modem	FM TUNER	Fingerprint	SSD	CIR
description						
explain	HDD PROTECT	Modem	FM TUNER	Fingerprint		
BTO	GSENSOR@	RJ11@	FM@	FP@	SSD@	CIR@

SMBUS Control Table

	SOURCE	New Card	BATT	CEC	THERMAL SENSOR CPU & ADM1032	SODIMM I / II	CLK	3G/TV	LCD	HDMI	Display Port	G-Sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	X	X	V
I2C_CLK I2C_DATA	RS780M	X	X	X	X	X	X	X	V	X	X	X
DDC_CLK0 DDC_DATA0	RS780M	X	X	X	X	X	X	X	X	V	X	X
DDC_CLK1 DDC_DATA1	RS780M	X	X	X	X	X	X	X	X	X	V	X
SCL0 SDA0	SB700	V	X	X	X	V	V	X	X	X	X	X
SCL1 SDA1	SB700	X	X	X	X	X	X	V	X	X	X	X
SCL2 SDA2	SB700	X	X	X	X	X	X	X	X	X	X	X
SCL3 SDA3	SB700	X	X	X	X	X	X	X	X	X	X	X

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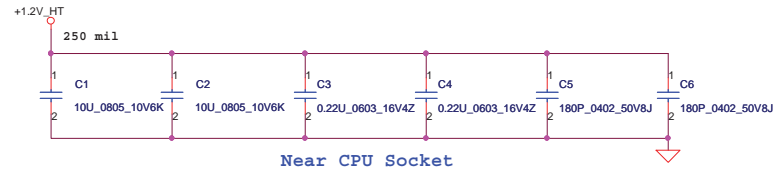
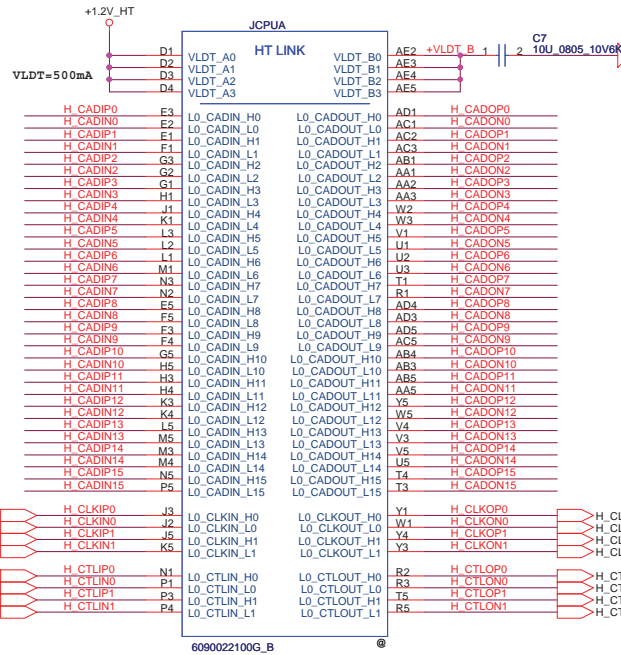
power plane	State	B+ +3VL +5VL +RTCVCC	+5VALW +3VALW +1.2VALW +3V_LAN	+1.8V +0.9V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +VGA_CORE +1.2V_HT +VDDNB +CPU_CORE_0 +CPU_CORE_1
S0		O	O	O	O
S1		O	O	O	O
S3		O	O	O	X
S5 S4/AC		O	O	X	X
S5 S4/ Battery only		O	X	X	X
S5 S4/AC & Battery don't exist		X	X	X	X

SB SM Bus1 Address				SB SM Bus2 Address			
Power	Device	HEX	Address	Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b	+3VALW	WLAN/WIMAX		
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b				
+3VS	Clock Generator	D2 H	1101 0010 b				
+3VS	New Card			Power	Device	HEX	Address
				+3VS	FM Tuner		Virtual I2C

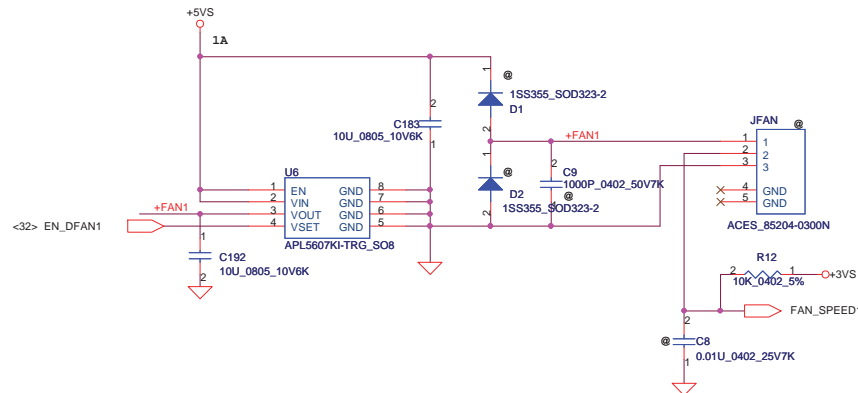
EC SM Bus1 Address				EC SM Bus2 Address			
Power	Device	HEX	Address	Power	Device	HEX	Address
+5VL	Smart Battery	16 H	0001 011X b	+3VS	CPU_ADM1032-1	98 H	1001 100X b
+5VL	HDMI-CEC	34 H	0011 010X b	+3VS	VGA_ADM1032-2	9A H	1001 101X b
				+3VS	G-Sensor		
				+3VS	Light Sensor		
Power	Device	HEX	Address				
+3VL	Cap. Sensor		Virtual I2C				

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<10> H\_CADIP[0..15] H\_CADIP[0..15]  
<10> H\_CADIN[0..15] H\_CADIN[0..15]  
<10> H\_CADOP[0..15] H\_CADOP[0..15]  
<10> H\_CADON[0..15] H\_CADON[0..15]

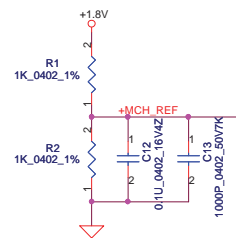


### FAN Control Circuit

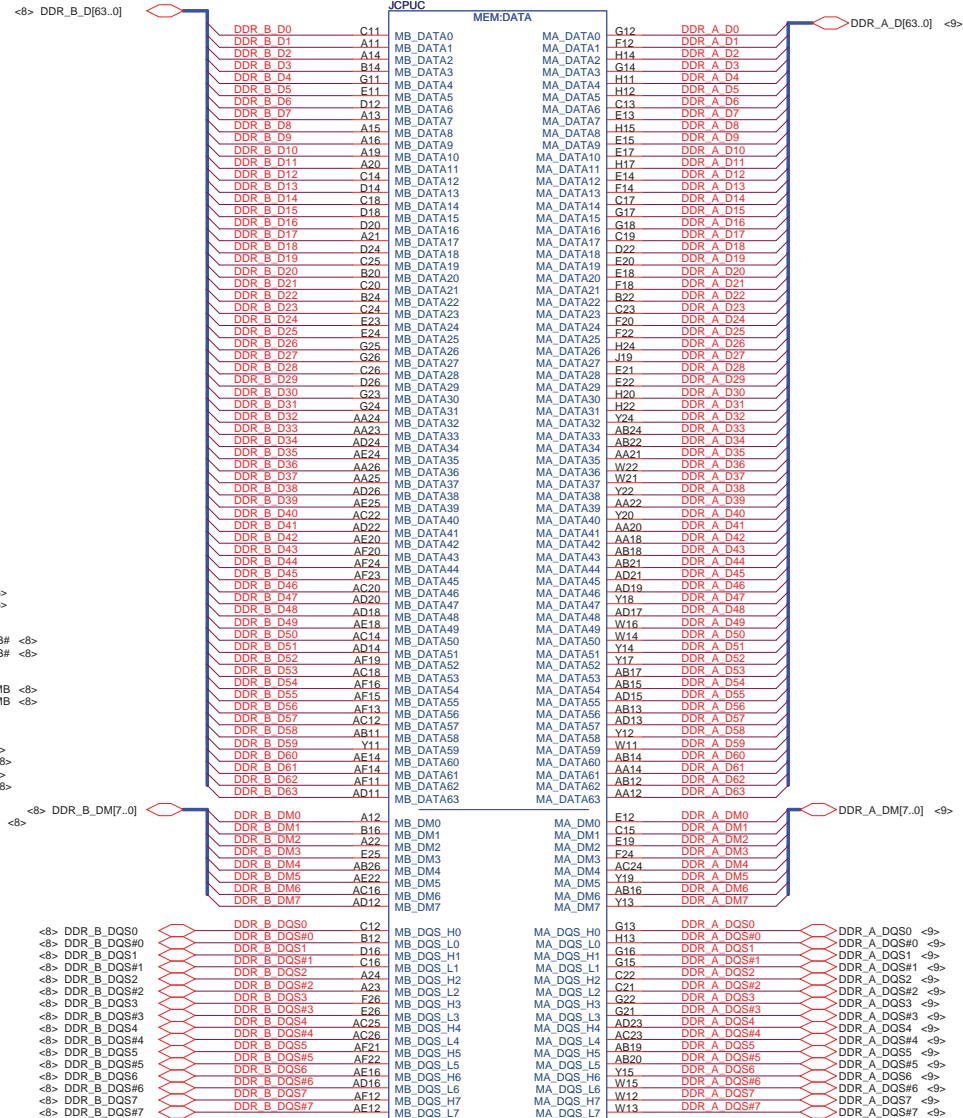
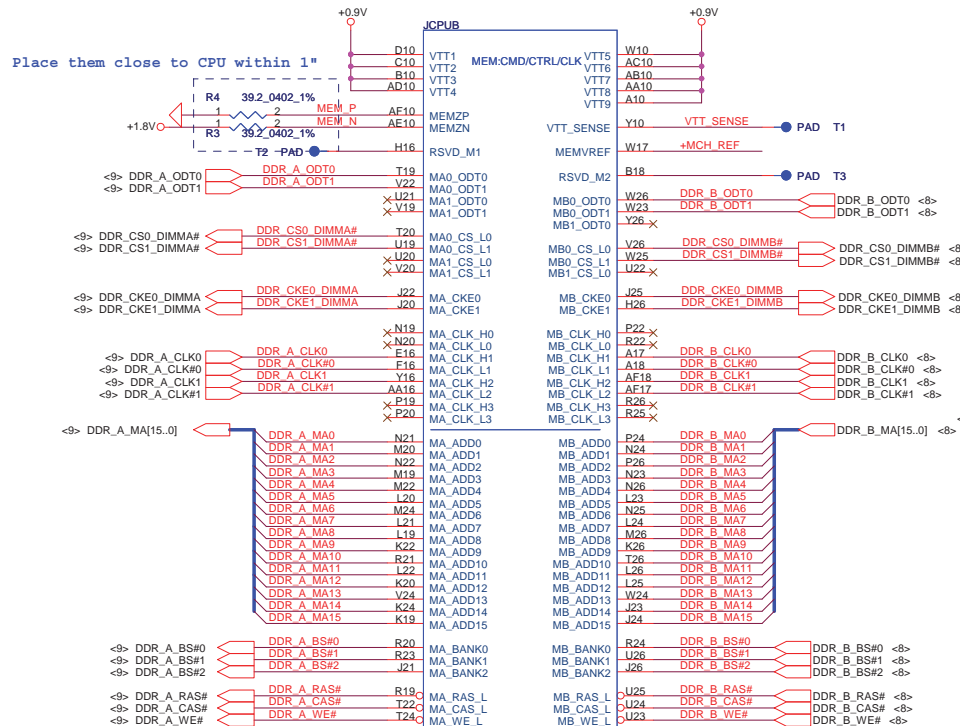
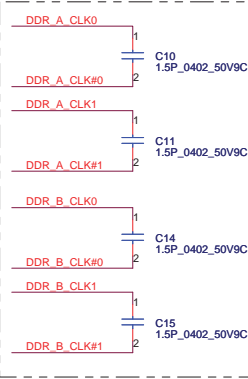


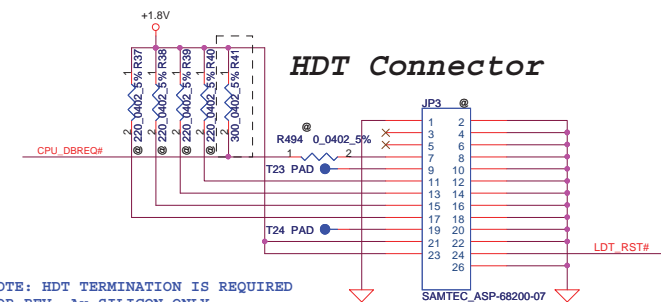
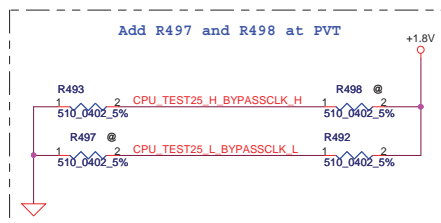
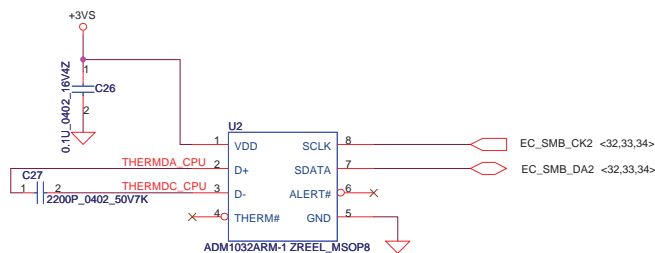
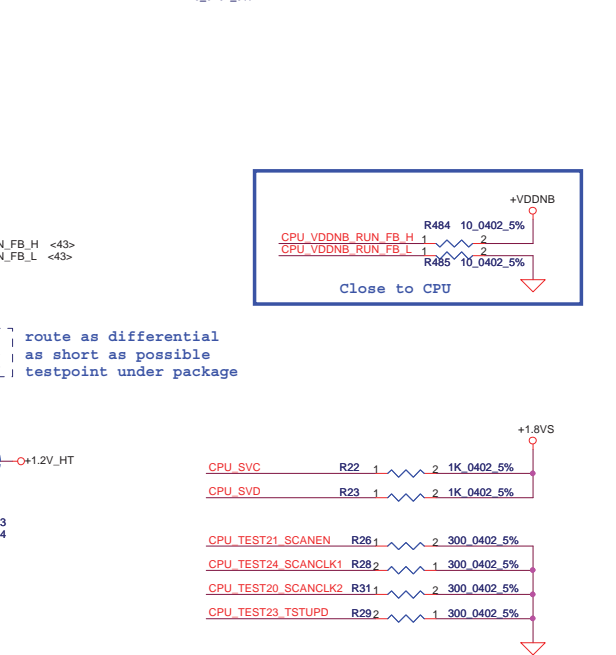
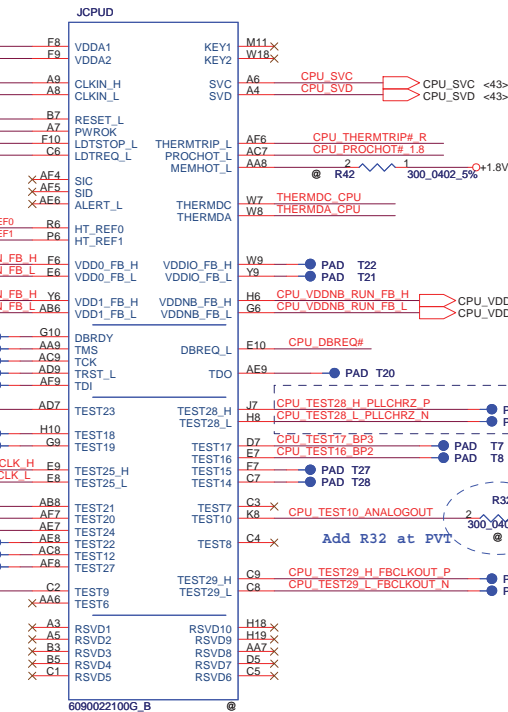
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Issued Date				2008/04/14				AMD CPU SIG2 HT I/F			
Deciphered Date				2009/04/14				LA-5381P			
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# Processor DDR2 Memory Interface



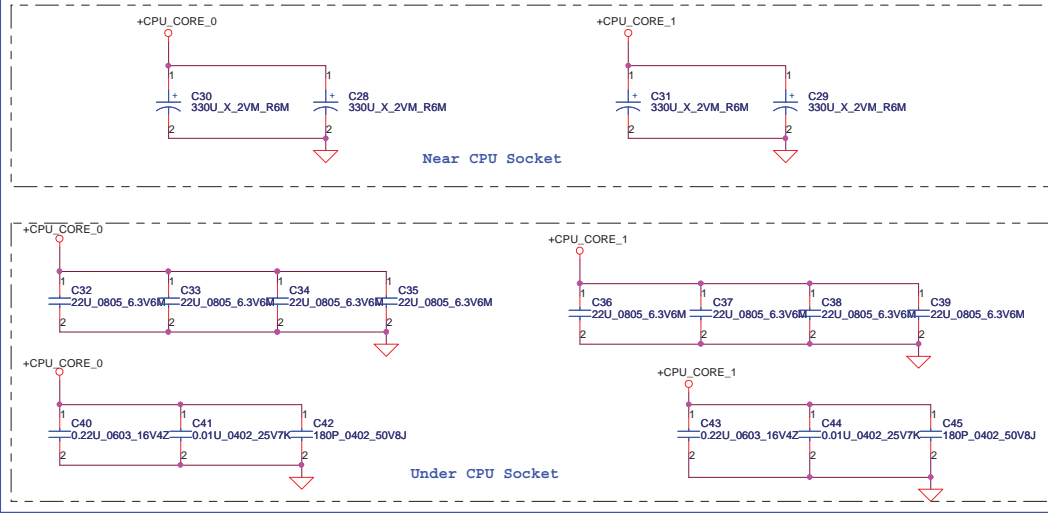
PLACE CLOSE TO PROCESSOR  
WITHIN 1.5 INCH



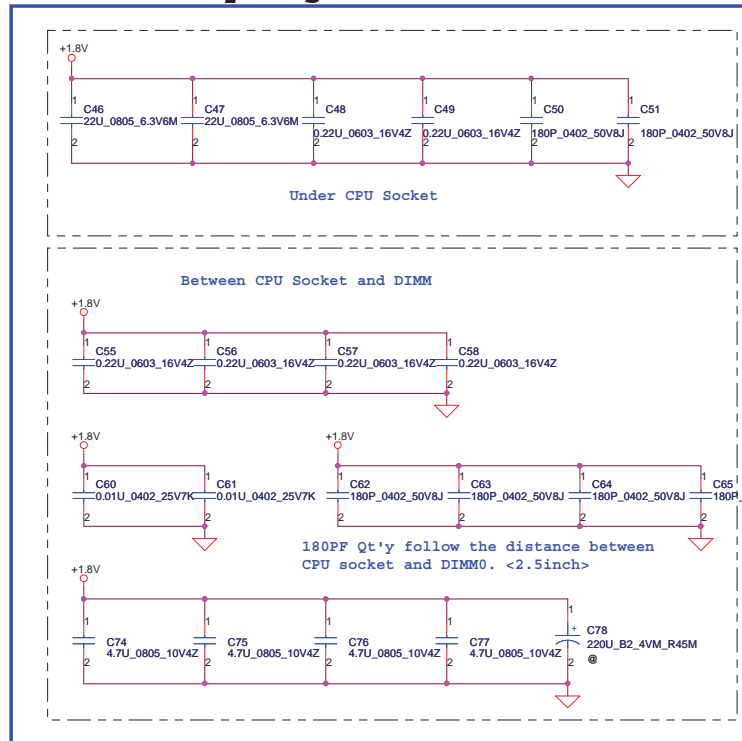


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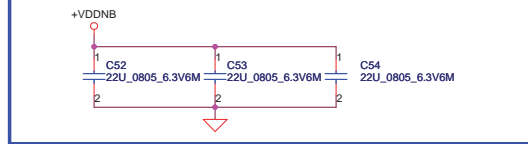
## VDD(+CPU\_CORE) decoupling.



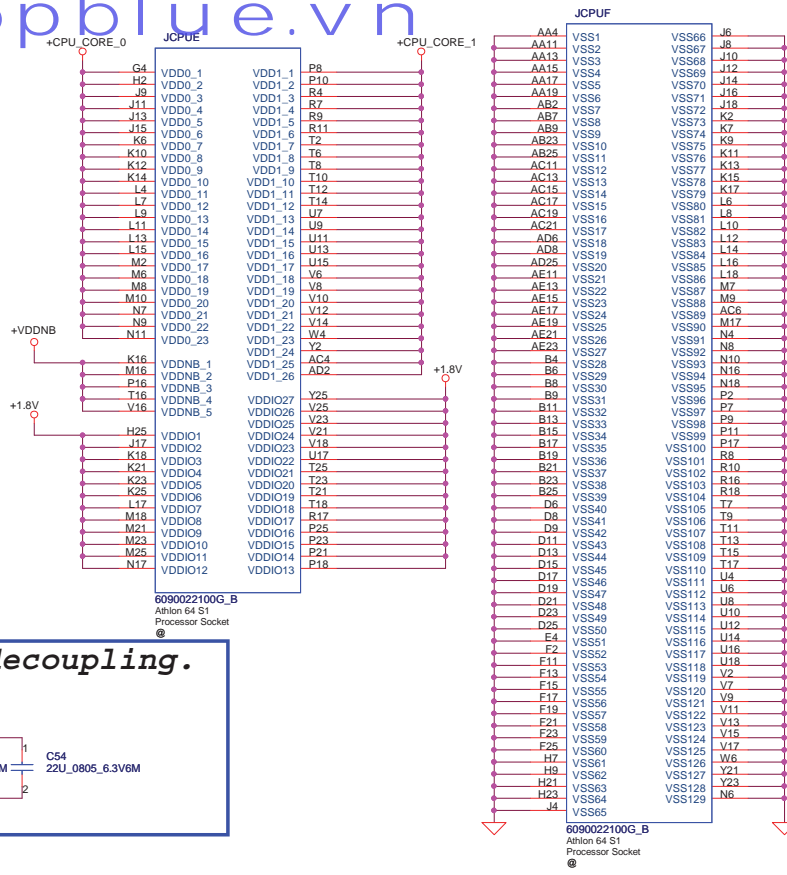
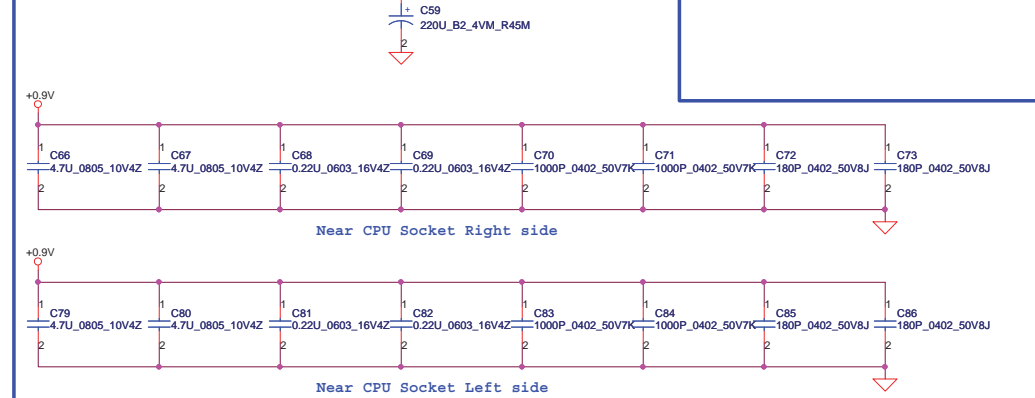
## VDDIO decoupling.



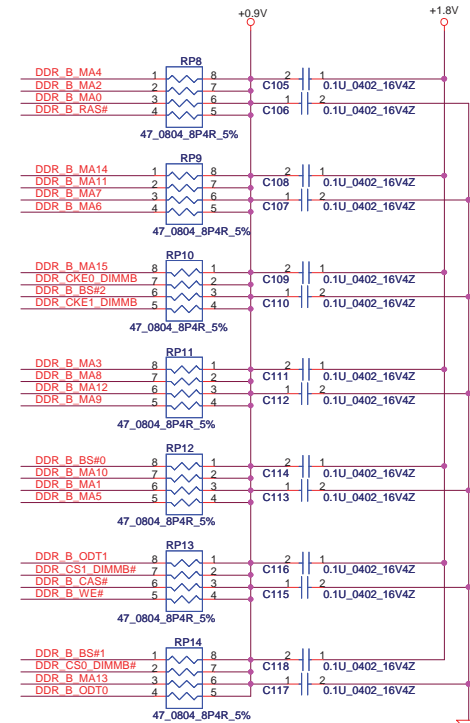
## +CPU\_CORE\_NB decoupling.



## VTT decoupling.





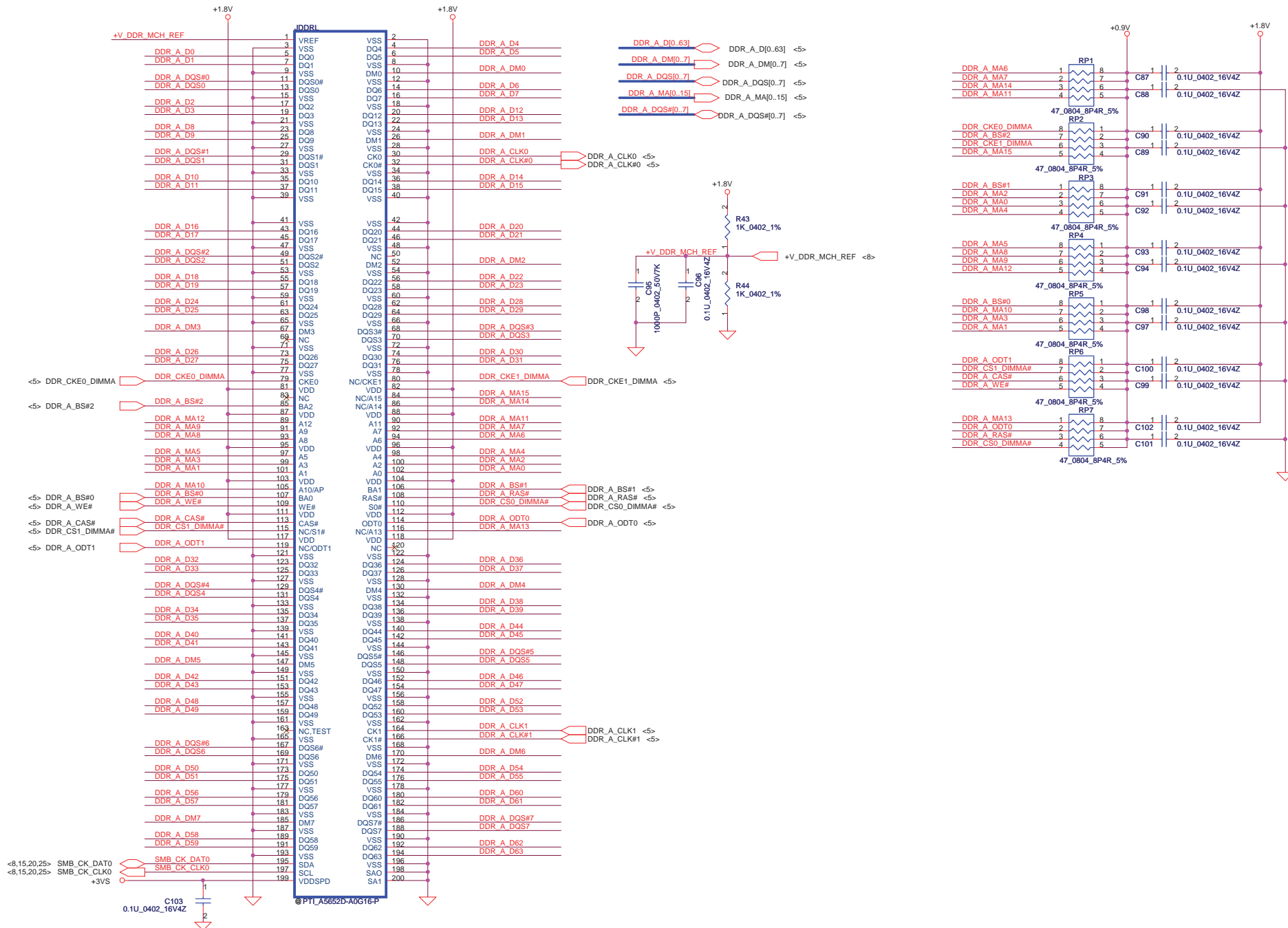


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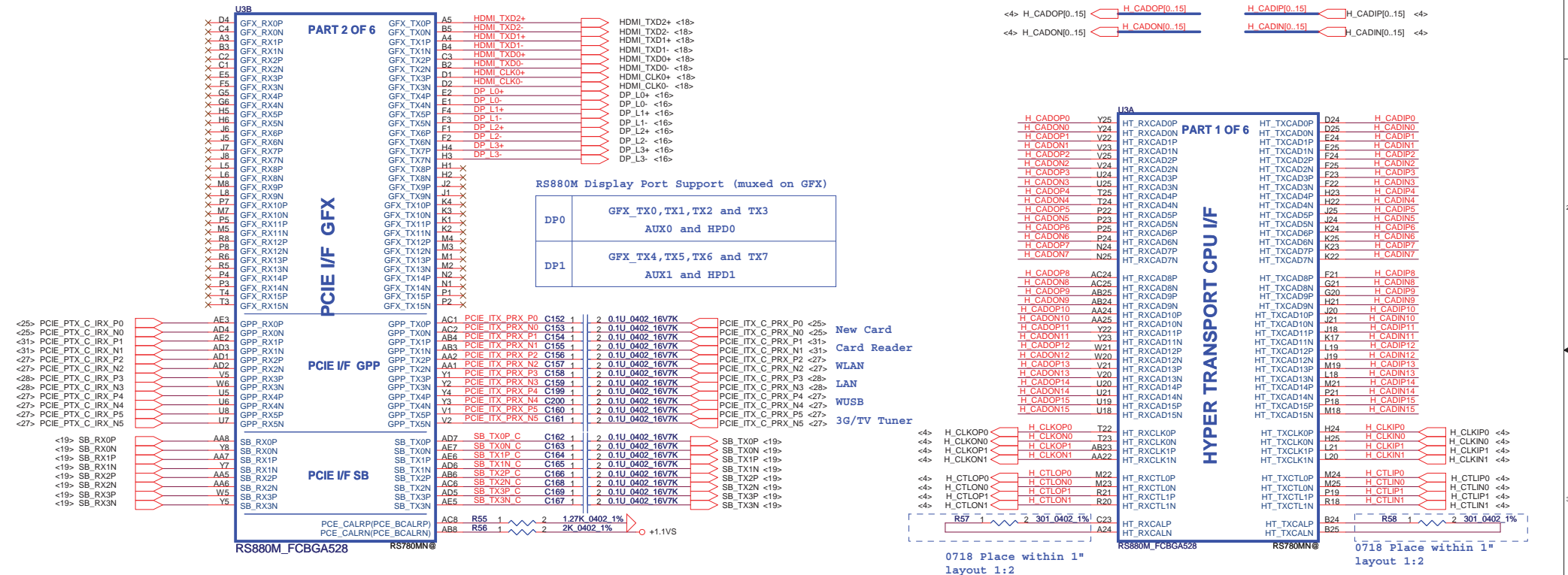
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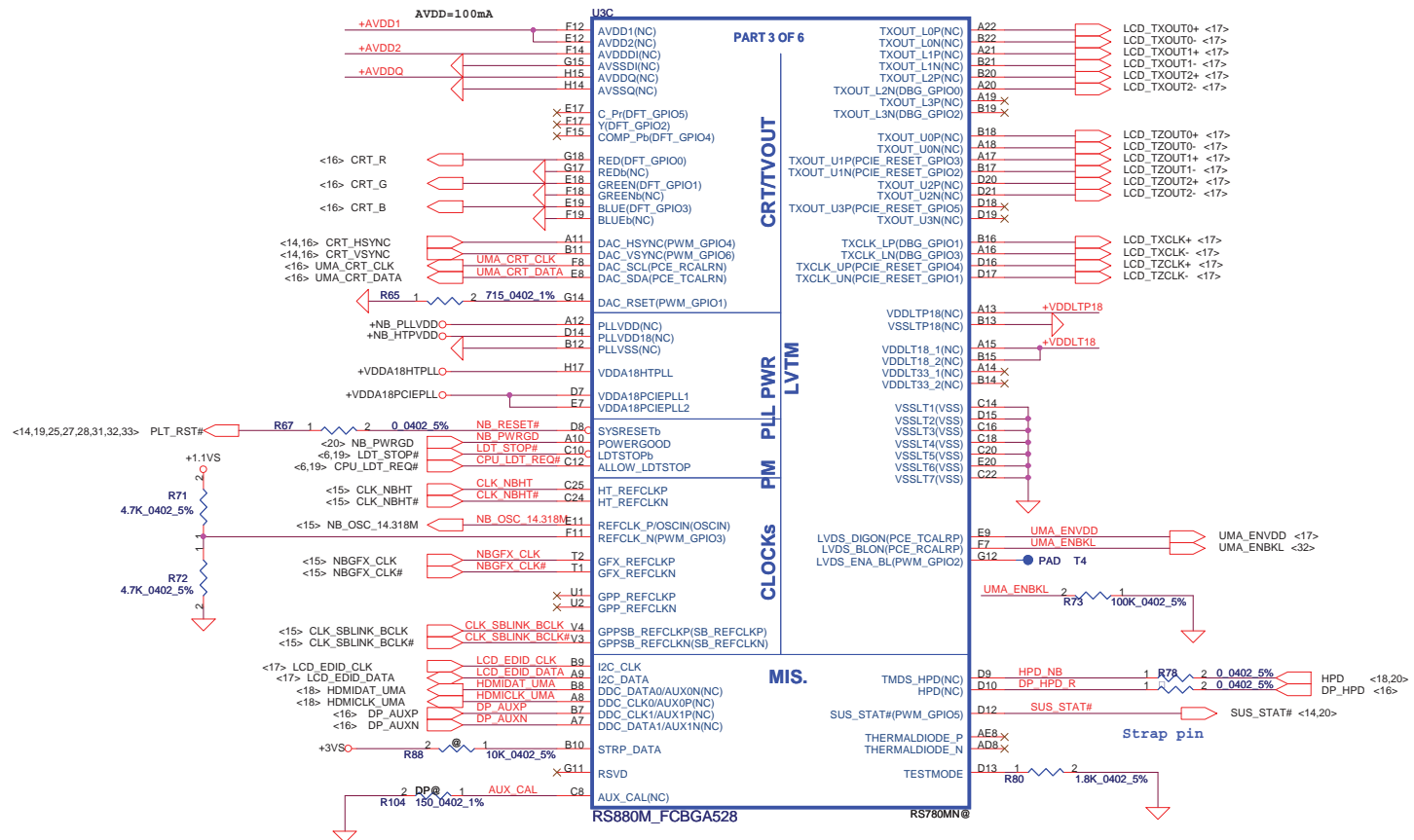
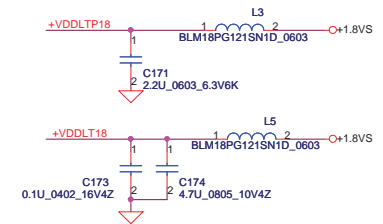
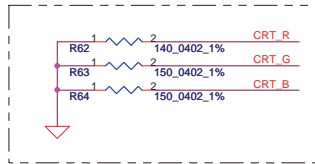
DIMM0 STD H:5.2mm (Bot)

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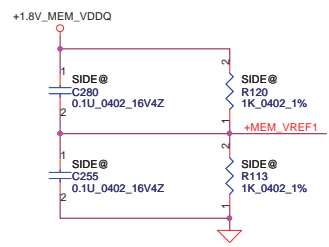
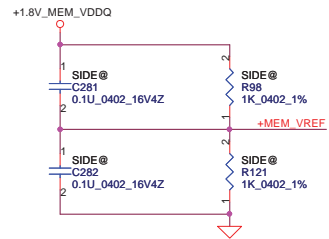
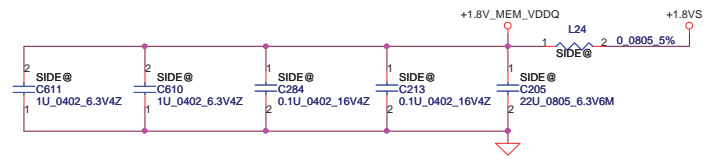


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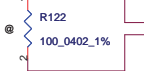
220 ohm @ 100MHz 2A



MEM\_COMP\_P and MEM\_COMP\_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions

PAR 4 OF 6					
MEM_A0	AB12	MEM_A0(NC)	MEM_DQ0	AA18	MEM_DQ0
MEM_A1	AE16	MEM_A1(NC)	MEM_DQ1	AA20	MEM_DQ1
MEM_A2	V11	MEM_A2(NC)	MEM_DQ2	AA19	MEM_DQ2
MEM_A3	AE15	MEM_A3(NC)	MEM_DQ3	Y19	MEM_DQ3
MEM_A4	AA12	MEM_A4(NC)	MEM_DQ4	V17	MEM_DQ4
MEM_A5	AB16	MEM_A5(NC)	MEM_DQ5	AA17	MEM_DQ5
MEM_A6	AB14	MEM_A6(NC)	MEM_DQ6	AA15	MEM_DQ6
MEM_A7	AD14	MEM_A7(NC)	MEM_DQ7	Y15	MEM_DQ7
MEM_A8	AD13	MEM_A8(NC)	MEM_DQ8	AC20	MEM_DQ8
MEM_A9	AD15	MEM_A9(NC)	MEM_DQ9	AD19	MEM_DQ9
MEM_A10	AC16	MEM_A10(NC)	MEM_DQ10	AE22	MEM_DQ10
MEM_A11	AE13	MEM_A11(NC)	MEM_DQ11	AC18	MEM_DQ11
MEM_A12	AC14	MEM_A12(NC)	MEM_DQ12	AB20	MEM_DQ12
MEM_A13	AD14	MEM_A13(NC)	MEM_DQ13	AC22	MEM_DQ13
MEM_BA0	AD16	MEM_BA0(NC)	MEM_DQ14	AD21	MEM_DQ14
MEM_BA1	AE17	MEM_BA1(NC)	MEM_DQ15	Y17	MEM_DQ15
MEM_BA2	AD17	MEM_BA2(NC)	MEM_DQS_P0	W18	MEM_DQS_P0
MEM_RAS#	W12C	MEM_RASb(NC)	MEM_DQS_N0	AD20	MEM_DQS_P1
MEM_WE#	V12C	MEM_CASb(NC)	MEM_DQS_P1	AE21	MEM_DQS_N1
MEM_CS#	AD18C	MEM_CASb(NC)	MEM_DM0	W17	MEM_DM0
MEM_CKE	AB13C	MEM_CKE(NC)	MEM_DM1	AE19	MEM_DM1
MEM_ODT	V14	MEM_ODT(NC)	MEM_DQS_P0	AE23	MEM_DQS_P0
MEM_CLKP	V15	MEM_CLKP(NC)	MEM_DQS_N0	AE24	MEM_DQS_N0
MEM_CLKN	W14	MEM_CLKN(NC)	MEM_DQS_P1	AE21	MEM_DQS_N1
MEM_COMP_P	AE12	MEM_COMP(NC)	MEM_DM0	W17	MEM_DM0
MEM_COMP_N	AD12	MEM_COMP(NC)	MEM_DM1	AE19	MEM_DM1

U61					
MEM_BA0	L2	BA0	DQ15	B1	MEM_DQ15
MEM_BA1	L3	BA1	DQ14	D9	MEM_DQ11
MEM_A12	R2	A12	DQ13	D1	MEM_DQ12
MEM_A11	P7	A11	DQ12	D3	MEM_DQ13
MEM_A10	M2	A10	DQ11	D7	MEM_DQ10
MEM_A9	P3	A9	DQ10	C2	MEM_DQ9
MEM_A8	P8	A8	DQ9	C8	MEM_DQ14
MEM_A7	P2	A7	DQ8	F9	MEM_DQ3
MEM_A6	N7	A6	DQ7	F1	MEM_DQ7
MEM_A5	N3	A5	DQ6	H8	MEM_DQ1
MEM_A4	N8	A4	DQ5	H1	MEM_DQ6
MEM_A3	N2	A3	DQ4	H3	MEM_DQ5
MEM_A2	N7	A2	DQ3	H7	MEM_DQ0
MEM_A1	M3	A1	DQ2	G2	MEM_DQ4
MEM_A0	M8	A0	DQ1	G8	MEM_DQ2



MEM_CLKP	K8	CK	VDDQ	A9	1.8V MEM_VDDQ
MEM_CLKN	J8	CK	VDDQ	C1	
MEM_CKE	K2	CKE	VDDQ	C3	
MEM_CS#	L8	CS	VDDQ	C7	
MEM_WE#	K3	WE	VDDQ	C9	
MEM_RAS#	K7	RAS	VDDQ	E9	
MEM_CAS#	L7	CAS	VDDQ	G1	
MEM_DM0	F3	LDM	VDDQ	G3	
MEM_DM1	B3	UDM	VDDQ	G7	
MEM_ODT	K9	ODT	VDDQ	G9	
MEM_DQS_P0	F7	LDQS	VDDQ	A1	
MEM_DQS_N0	E8	LDQS	VDDQ	E1	
MEM_DQS_P1	B7	UDQS	VDDQ	J9	
MEM_DQS_N1	A8	UDQS	VDDQ	M9	
+MEM_VREF	J2	VREF	VDDQ	R1	
MEM_BA2	X A2	NC	VDDQ	J1	
	X E2	NC	VDDQ	J7	
	X R3	NC	VDDQ	C283	
	X R7	NC	VDDQ	1U_0603_10V6K	
	X B8	NC	VDDQ		

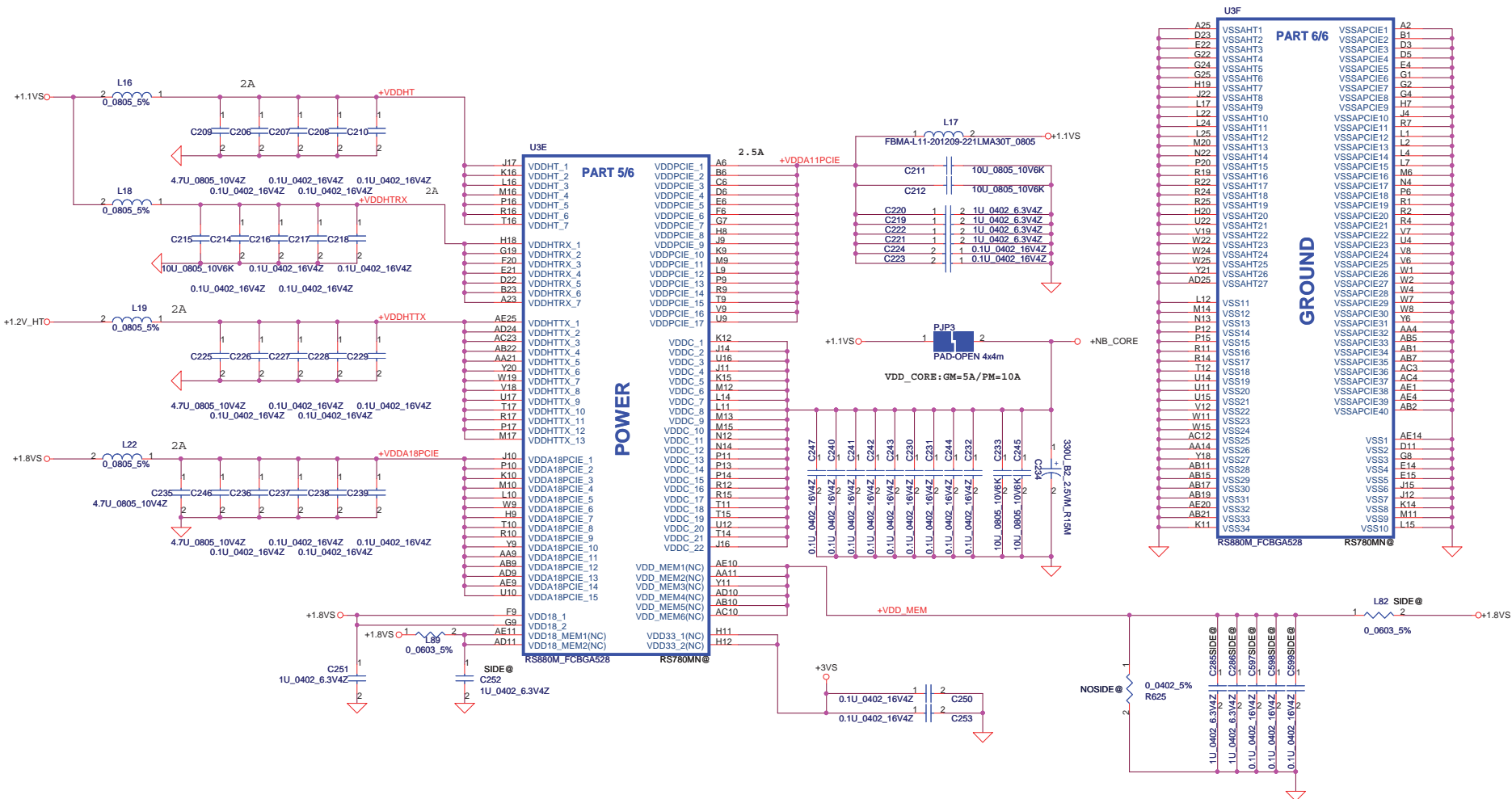
Layout Note: 50 mil for VSSDL

U61 SAMSIDE@ K4N1G164QE-HC20

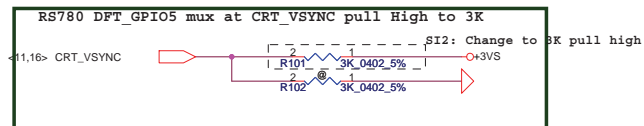
SA00002UH00 : Hynix  
SA000031O00 : Samsung

64M\*16 DDR2 400MHZ

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## DFT\_GPIO5:STRAP\_DEBUG\_BUS\_GPIO\_ENABLEb

Enables the Test Debug Bus using GPIO.  
 1 : Enable (RX780, RS780)  
 0 : Disable (RX780, RS780)  
 PIN: RS740-->RS780\_AUX\_CAL; RX780-->NB\_TV\_C; RS780--> VSYNC#

RS780 use register to control PCI-E configure

## DFT\_GPIO[4:2]: STRAP\_PCIE\_GPP\_CFG[2:0]

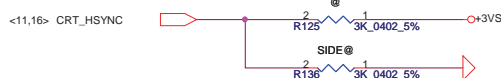
These pin straps are used to configure PCI-E GPP mode.  
 000 : 00001  
 001 : 00010  
 010 : 01011  
 011 : 00100  
 100 : 01010  
 101 : 01100  
 111 : 01011



## DFT\_GPIO1: LOAD\_EEPROM\_STRAPS

Selects Loading of STRAPS from EPROM  
 1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected  
 RS740/RX780: DFT\_GPIO1 RS780:SUS\_STAT

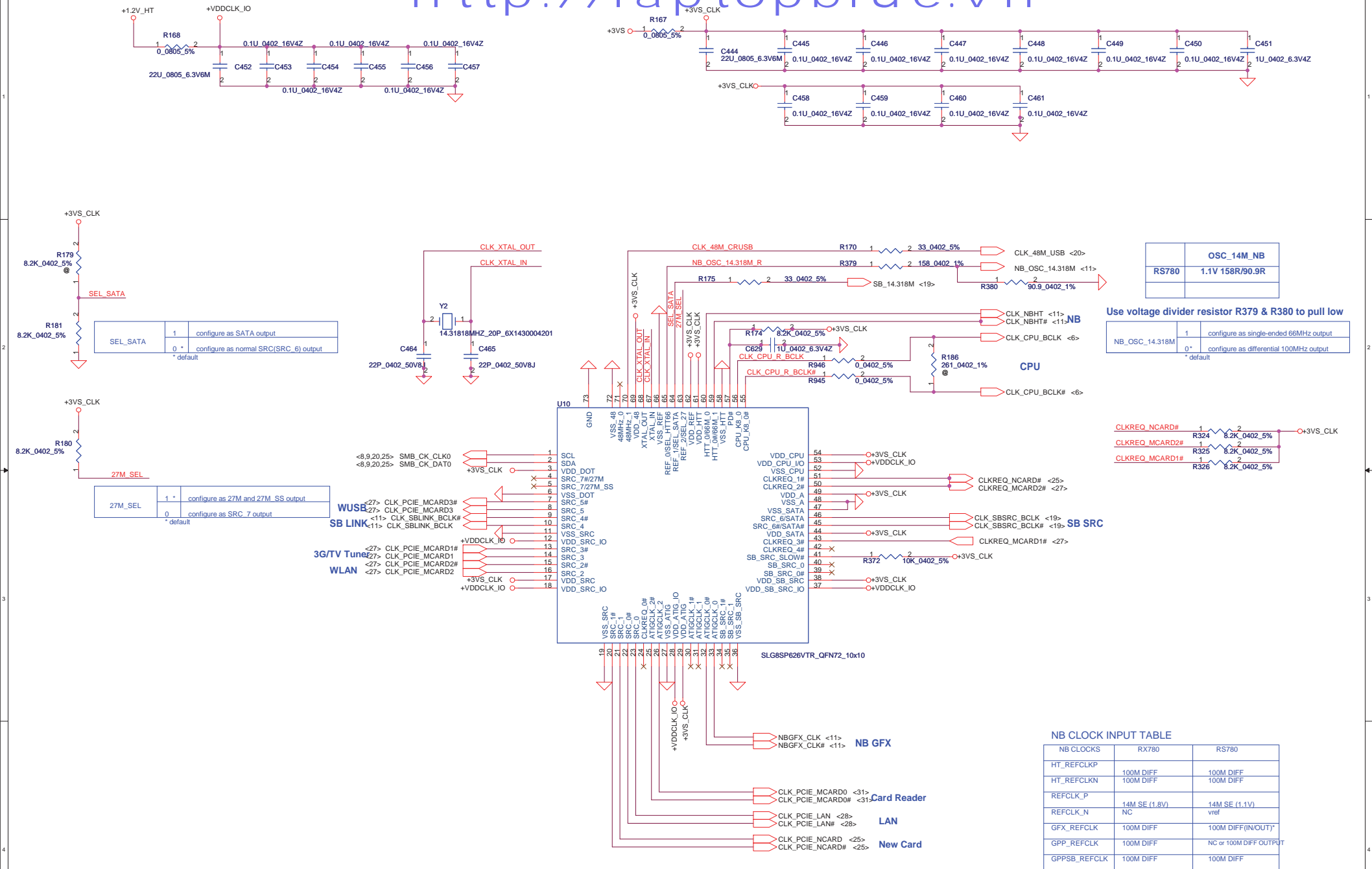
RS780 use HSYNC to enable SIDE PORT (internal pull high)



## DFT\_GPIO0: STRAP\_DEBUG\_BUS\_PCIE\_ENABLEb

RX780: Enables the Test Debug Bus using PCIE bus  
 1 : Disable ( Can still be enabled using nbcfg register access )  
 0 : Enable  
 RS780: Enables Side port memory ( RS780 use HSYNC#)  
 1. Disable (RS780)  
 0 : Enable (RS780)

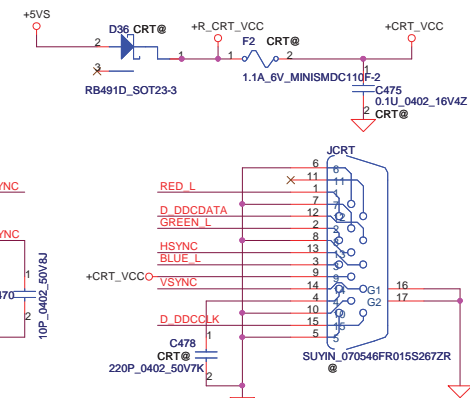
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Issued Date	2008/04/14	Deciphered Date	2009/04/14	Title	
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				Date: Friday, April 10, 2009	Sheet 14 of 46



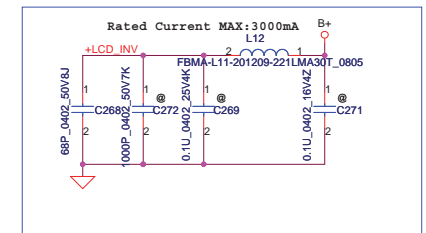
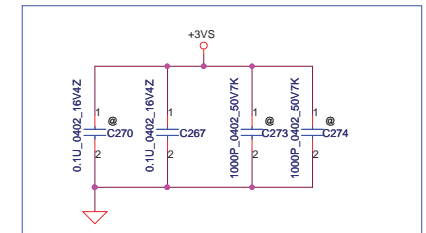
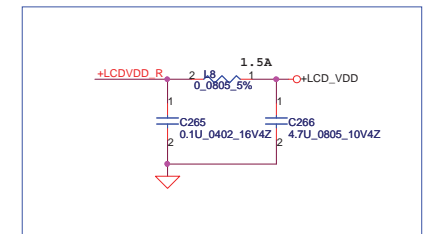
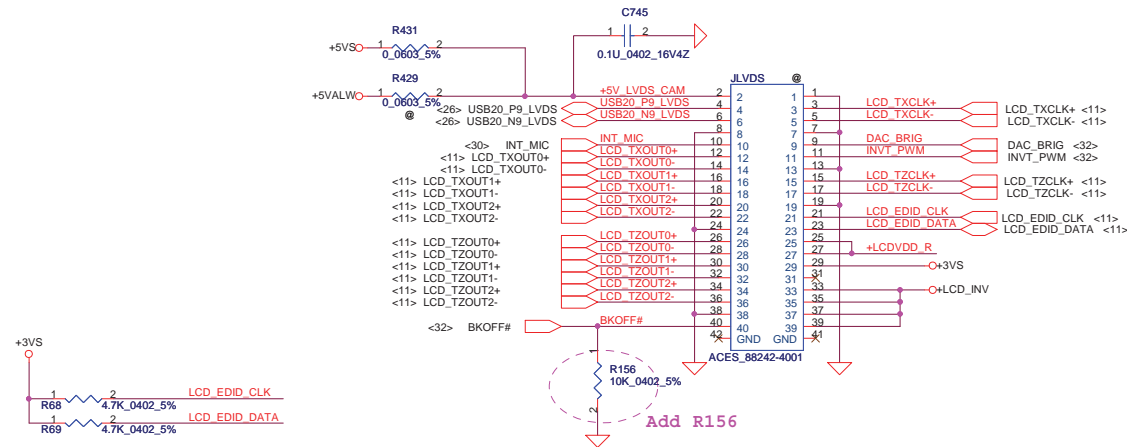
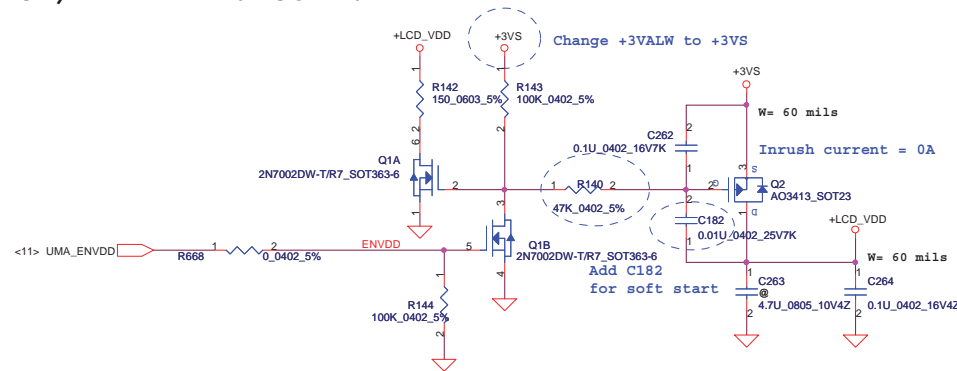
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Issued Date	2008/04/14	Deciphered Date	2009/04/14	Title	<b>Clock Generator</b>
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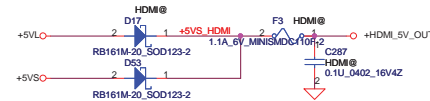
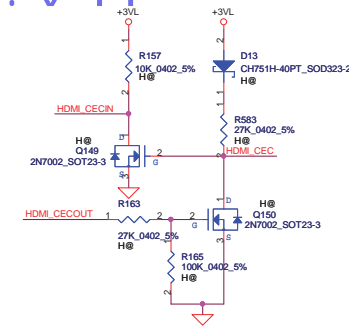
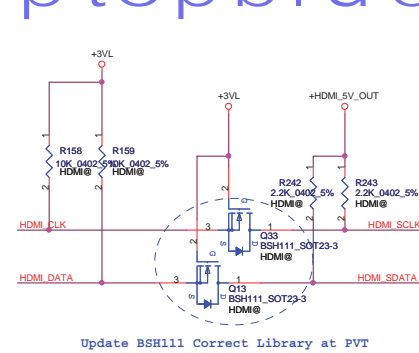


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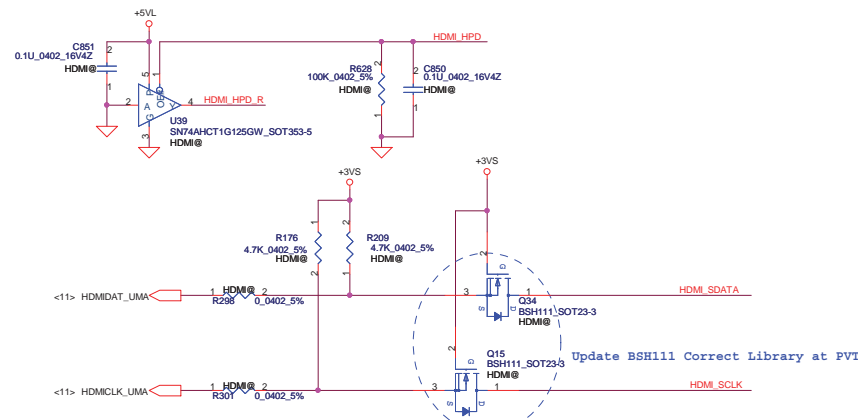
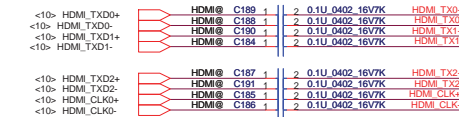
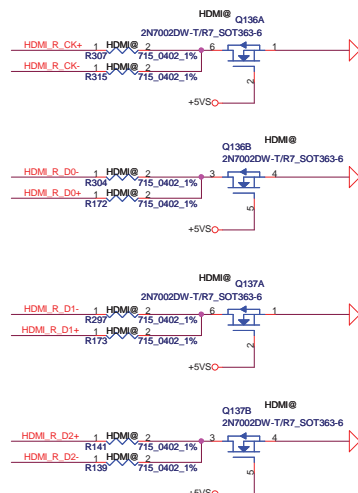


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				Friday, April 10, 2009	Sheet 17 of 46

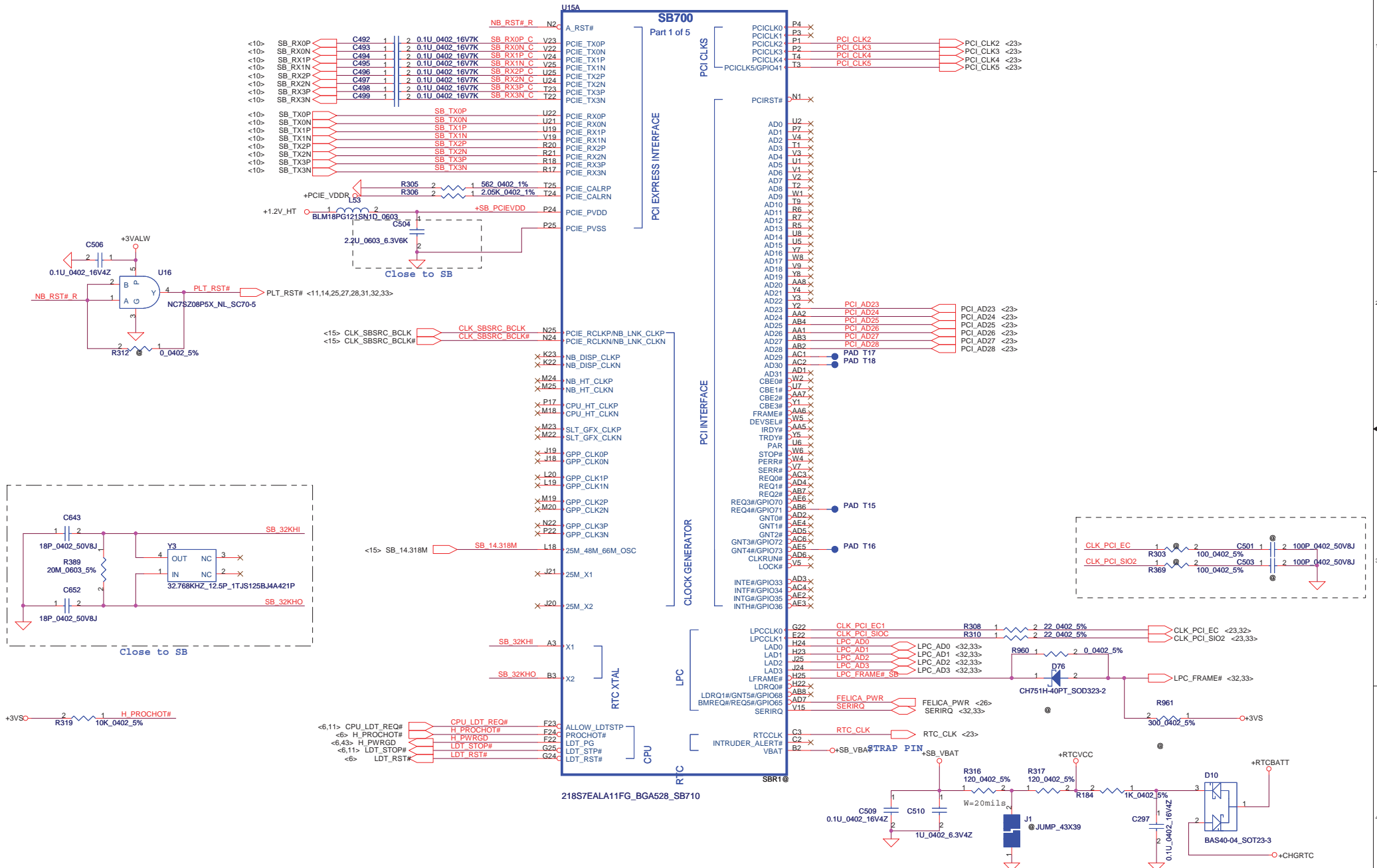
http://laptopblue.vn<sup>+3VL</sup>

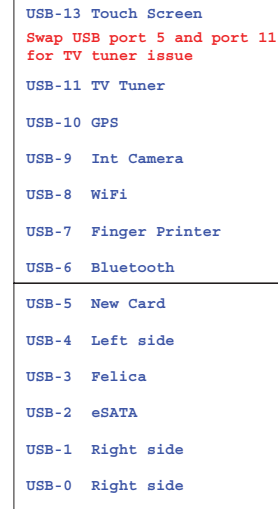


Pinout diagram for the HY626560P memory module. The diagram shows two rows of pins. The top row (pins 1-19) is labeled with signals: HDM1\_HPD (18), +HDM1\_5V\_OUT (19), HDM1\_SDAT4 (16), HDM1\_SCLK (17), HDM1\_CEC (14), HDM1\_RN\_CK (15), HDM1\_RN\_CK+ (11), HDM1\_RN\_D0 (10), HDM1\_RN\_D0+ (7), HDM1\_RN\_D1 (6), HDM1\_RN\_D1+ (5), HDM1\_RN\_D2 (3), and HDM1\_RN\_D2+ (2). The bottom row (pins 20-23) is labeled with signals: JHDM1\_HPD\_DET (+5V) (20), DDC/CEC\_GND (21), SDA\_SCL (22), and Reserved (23). A note indicates that pins 14 and 15 are crossed. A ground symbol is shown at the bottom right.

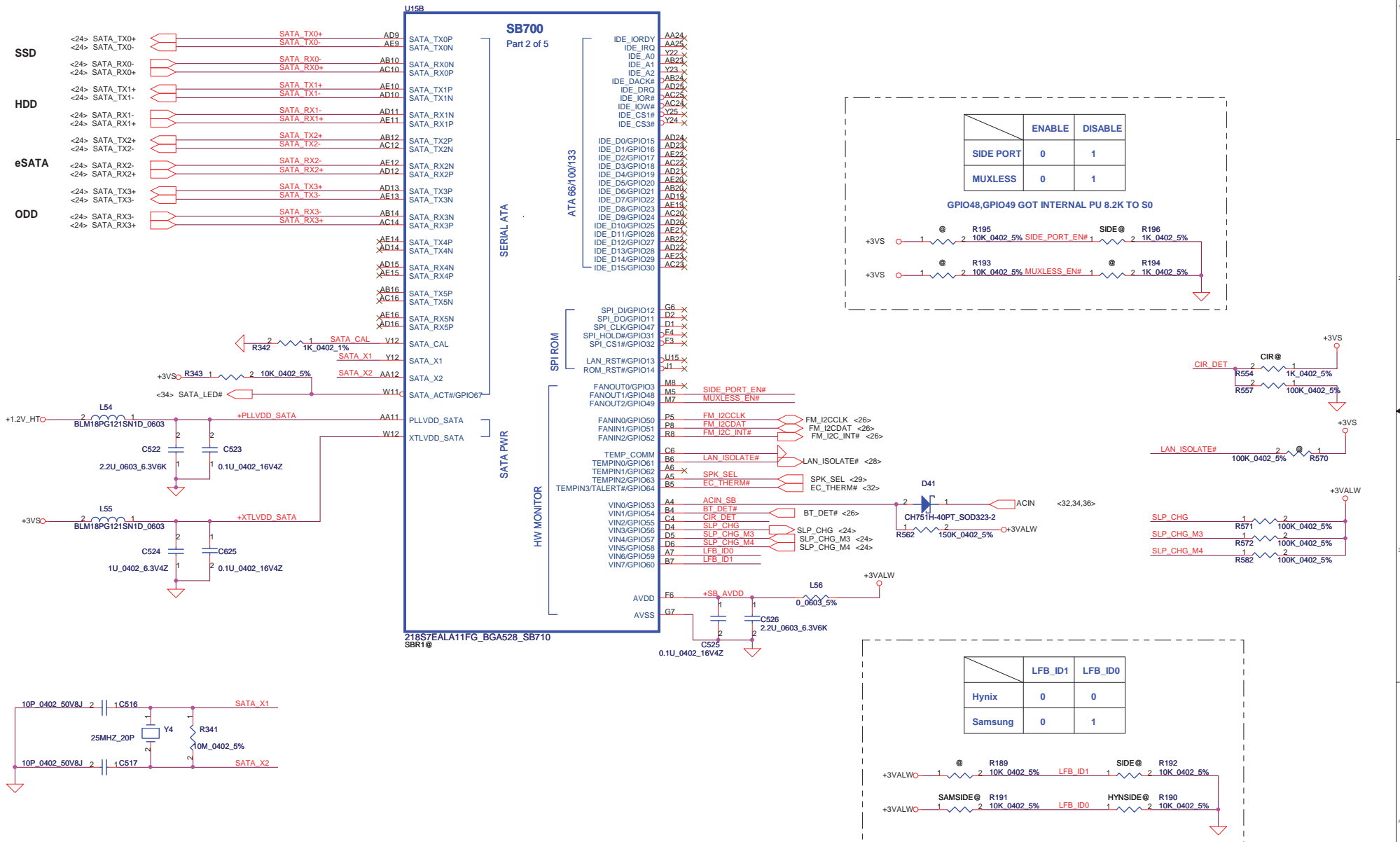


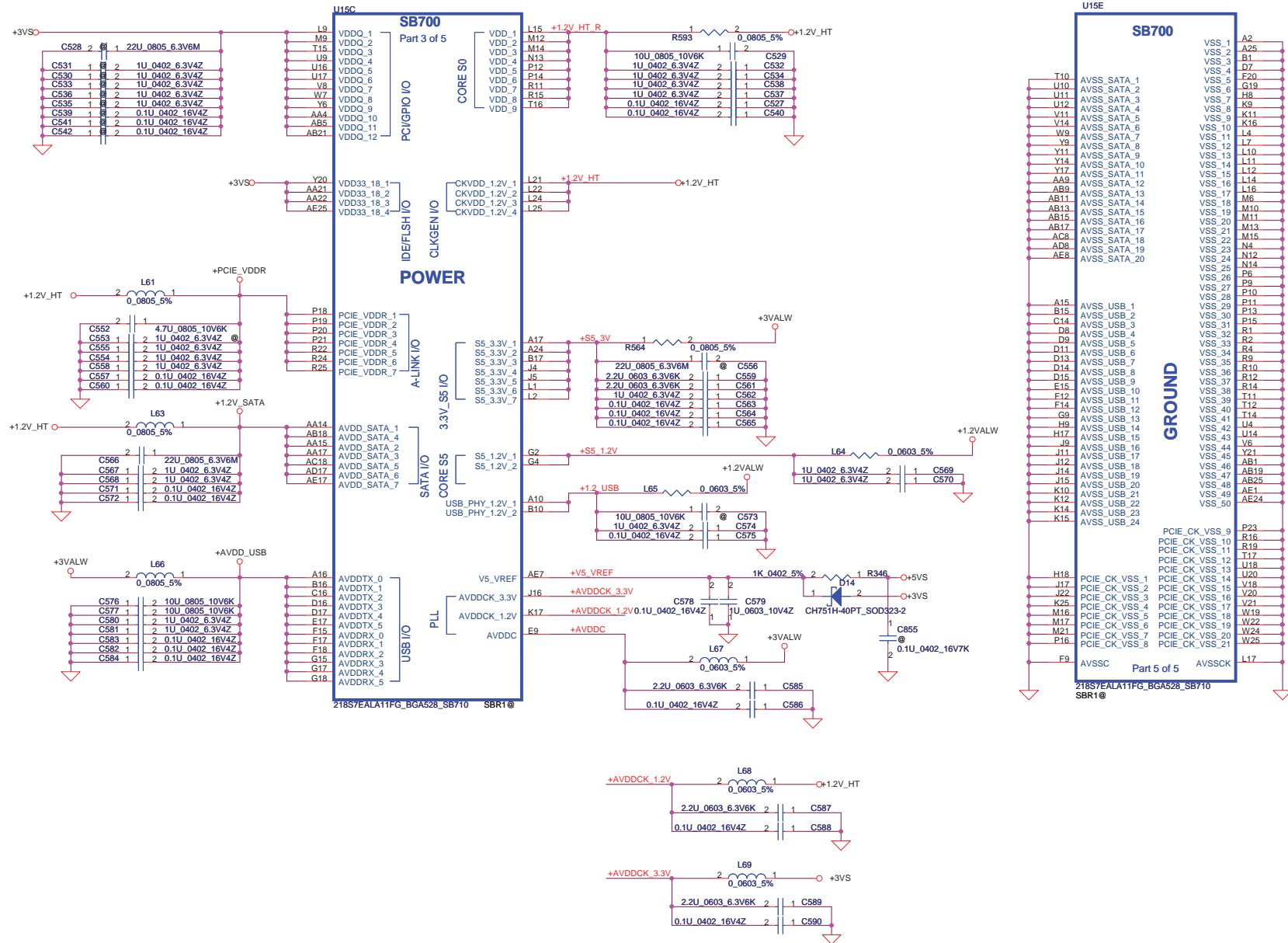
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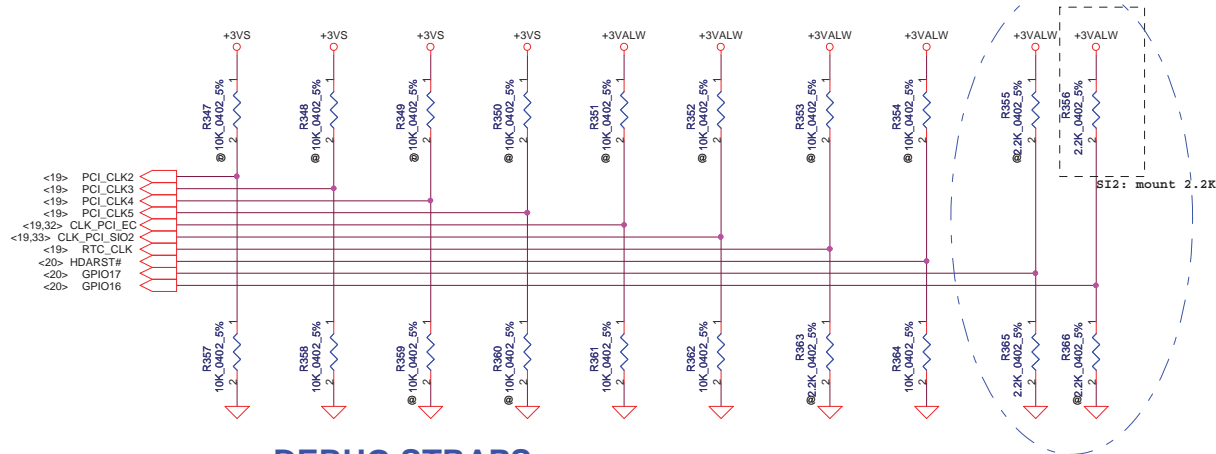


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Date: Friday, April 10, 2009		Sheet 22 of 46			



NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC\_CLK

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC  DEFAULT	EC ENABLED	Internal pull up H,H = Reserved  H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT  DEFAULT	CLKGEN DISABLED  DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED  DEFAULT		

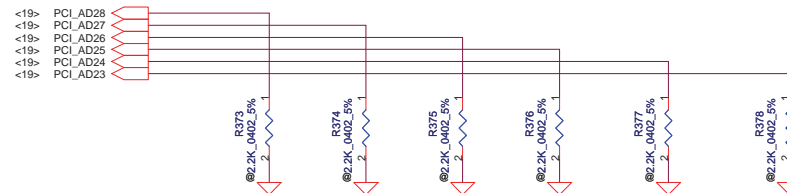


## DEBUG STRAPS

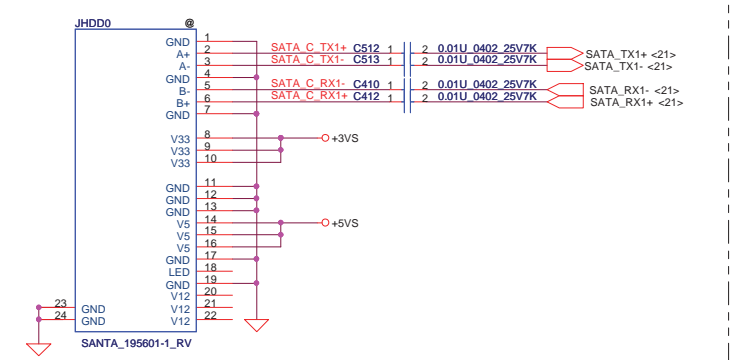
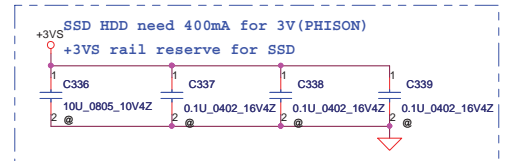
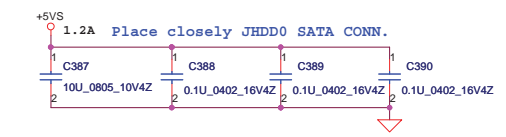
SB700 HAS 15K INTERNAL PU FOR PCI\_AD[28:23]

Need to confirm if SB SPI ROM will mount

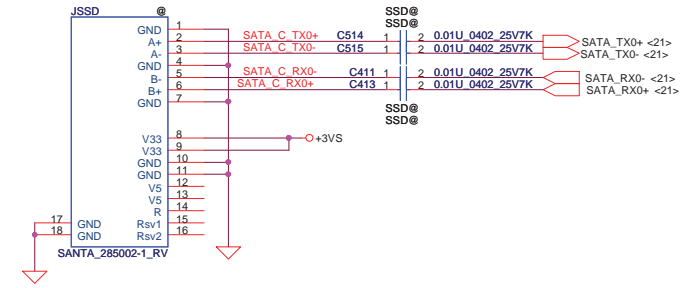
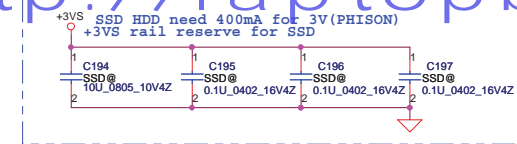
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



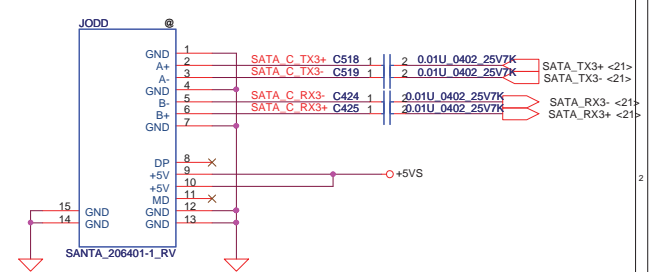
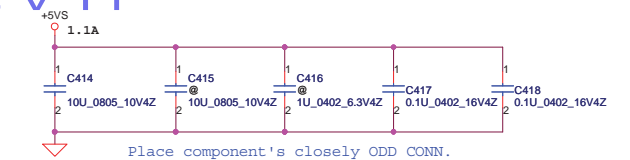
SATA HDD0 Conn.



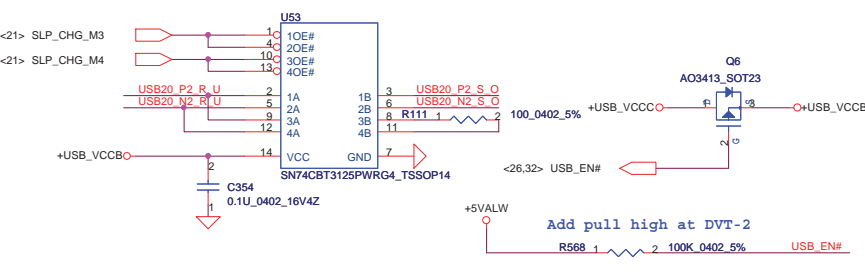
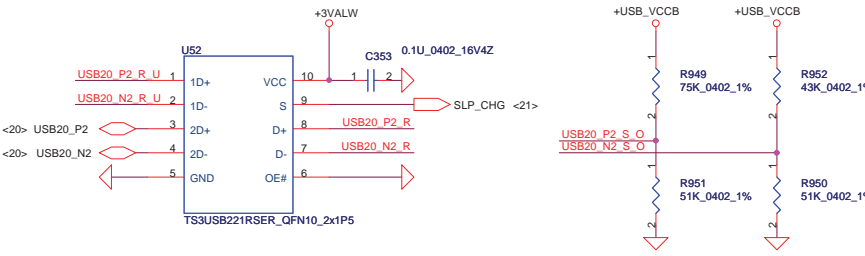
SSD Conn.



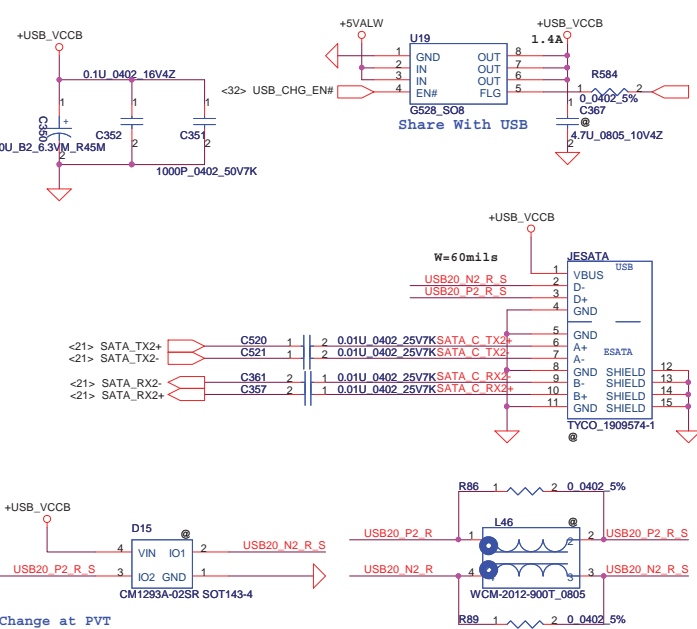
SATA ODD Conn



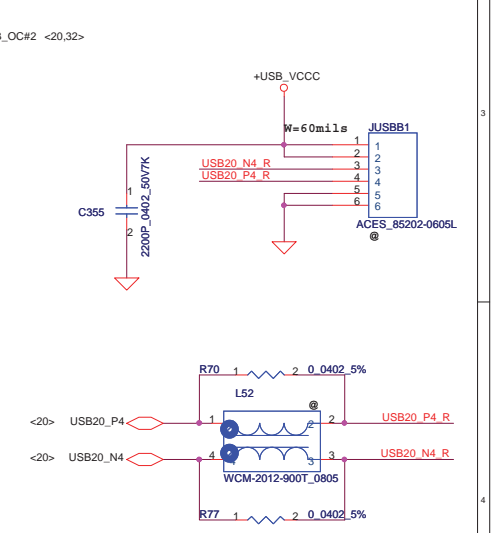
E-SATA/USB



	SLP_CHG_M3	SLP_CHG_M4	SLP_CHG	FUNCTION
Mode 3	HIGH	LOW	LOW	D=1D
Mode 4	LOW	HIGH	HIGH	D=2D



LEFT USB



Security Classification

Compal Secret Data

Issued Date

2008/04/14

Deciphered Date

2009/04/14

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Rev 0.2

Compal Electronics, Inc.

SATA HDD/ODD

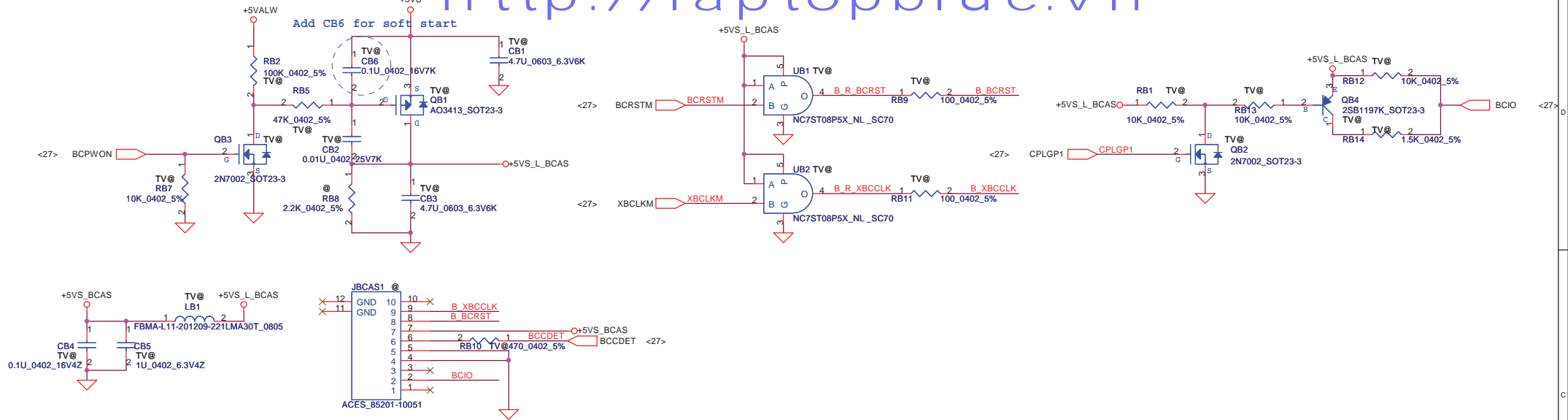
LA-5381P

Friday, April 10, 2008

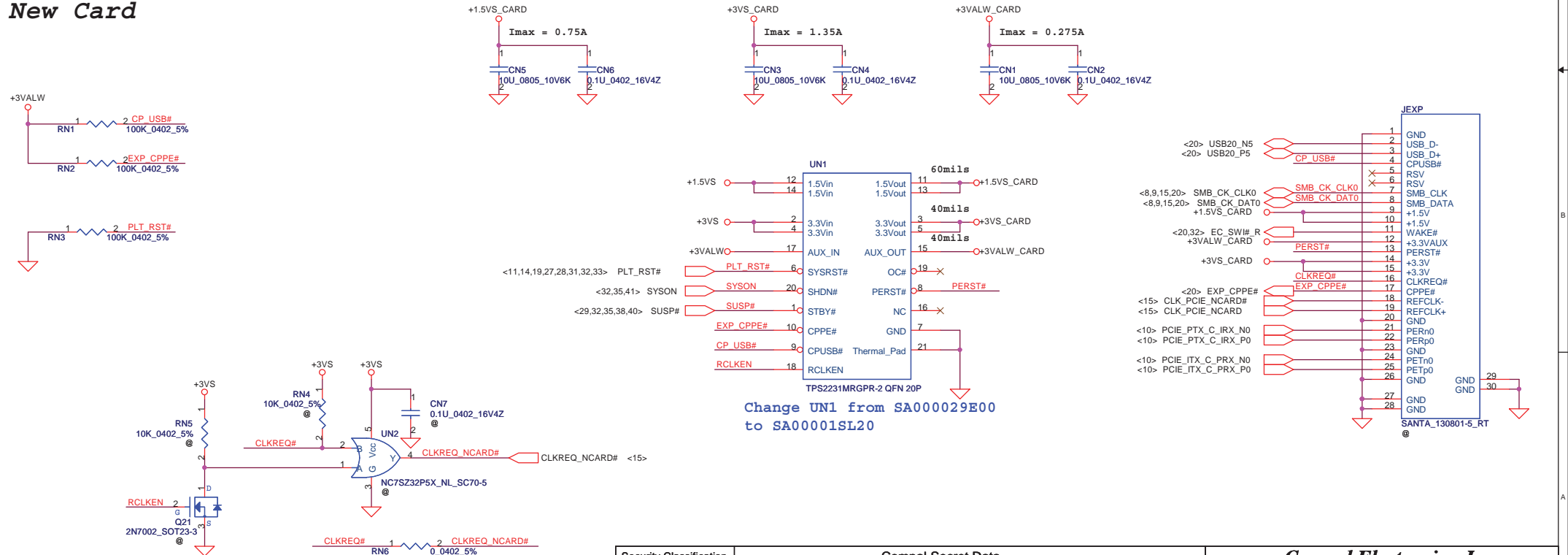
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# B-CAS Circuit

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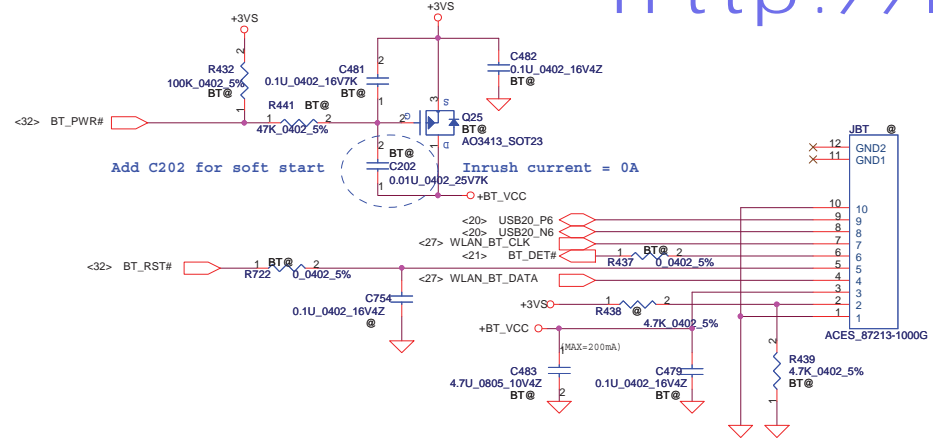


## New Card

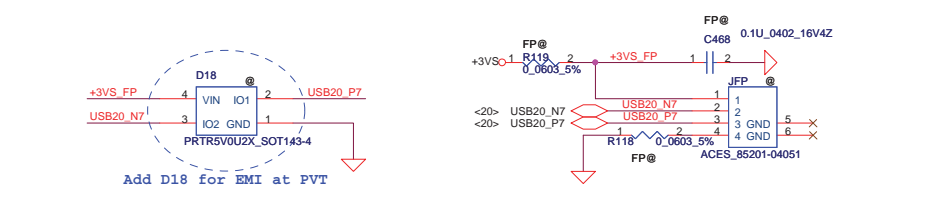


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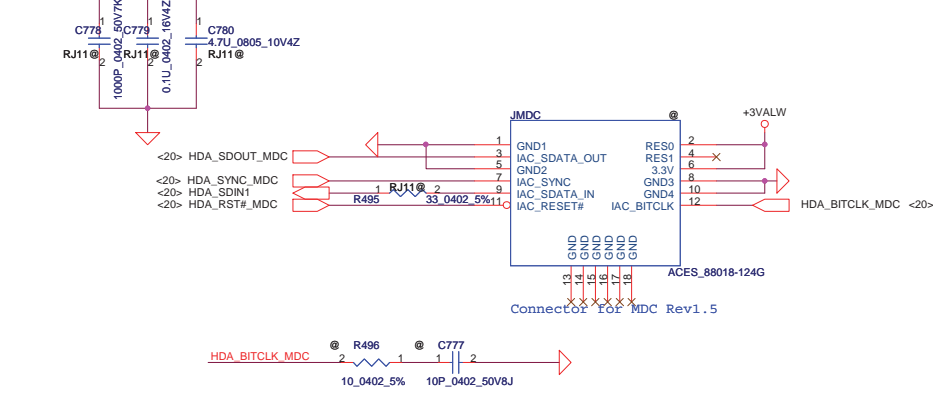
BlueTooth Interface



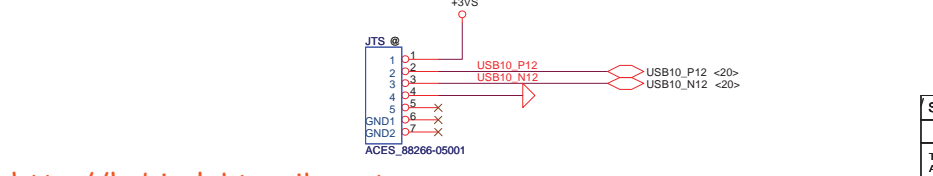
Finger printer



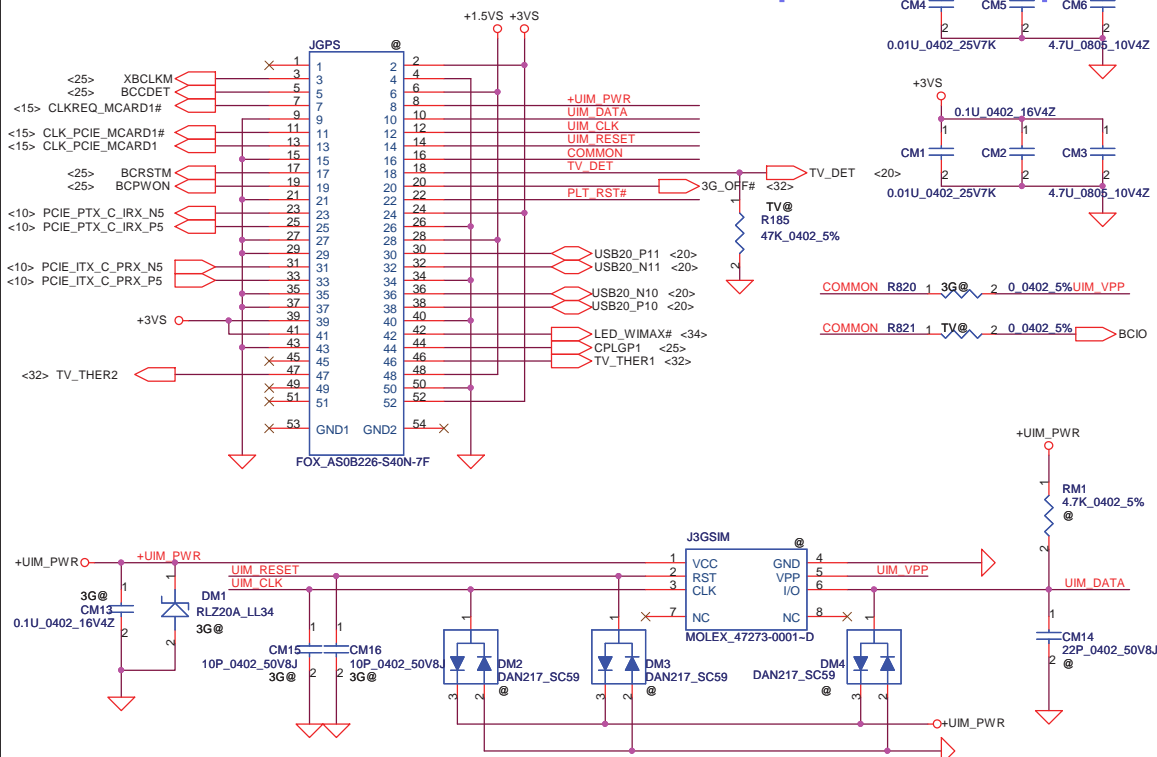
MDC 1.5 Conn.



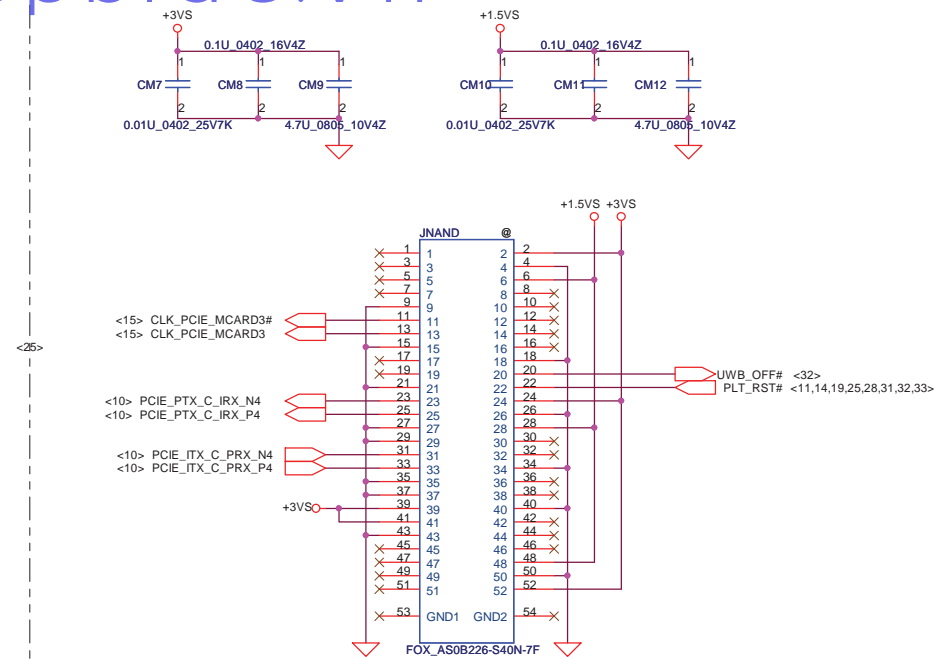
Touch Screen



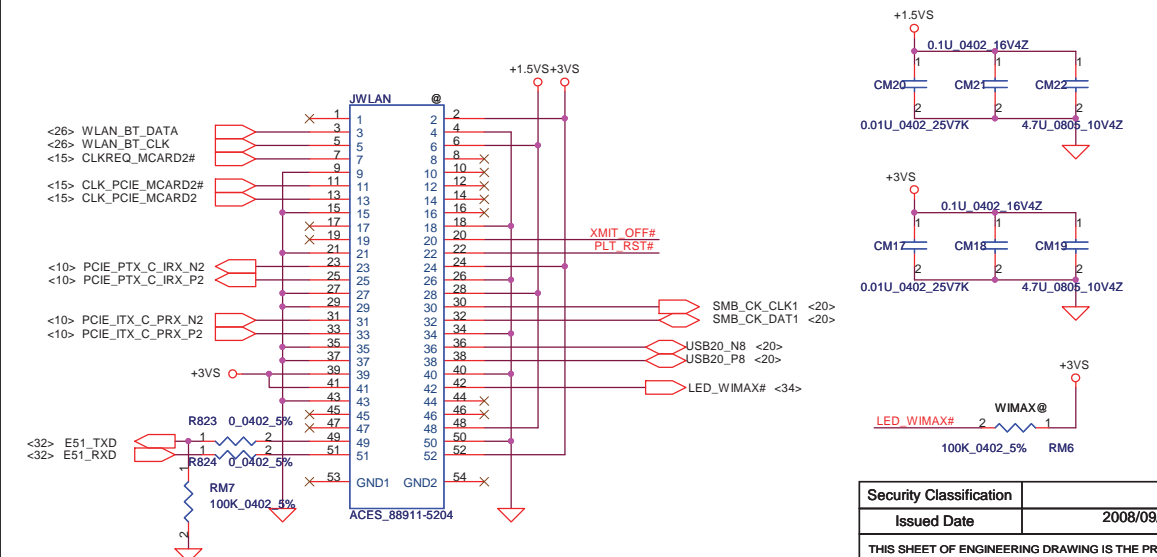
# PCiE Mini Card-3G/GPS/TV Tuner (Slot 2)



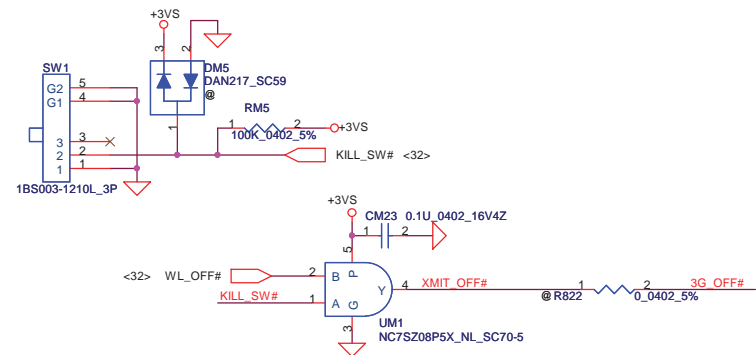
# WUSB or Upconvert (Slot 3)



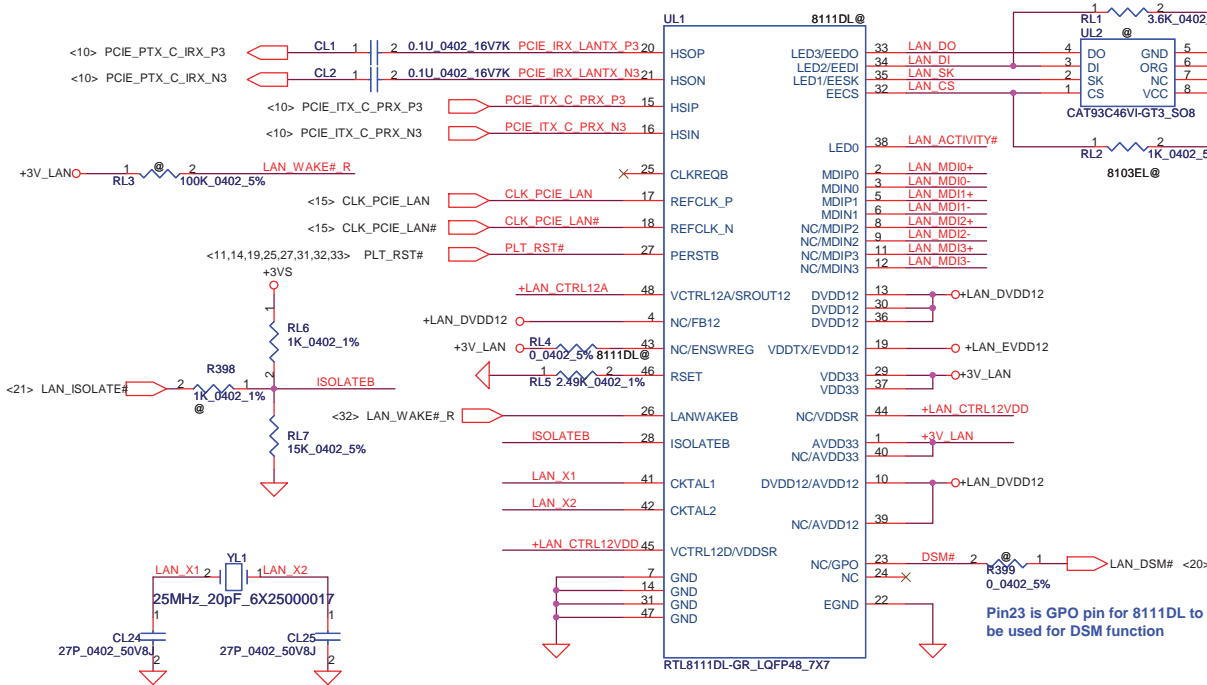
# PCiE Mini Card-WLAN/WiMax (Slot 1)



# Kill SWITCH

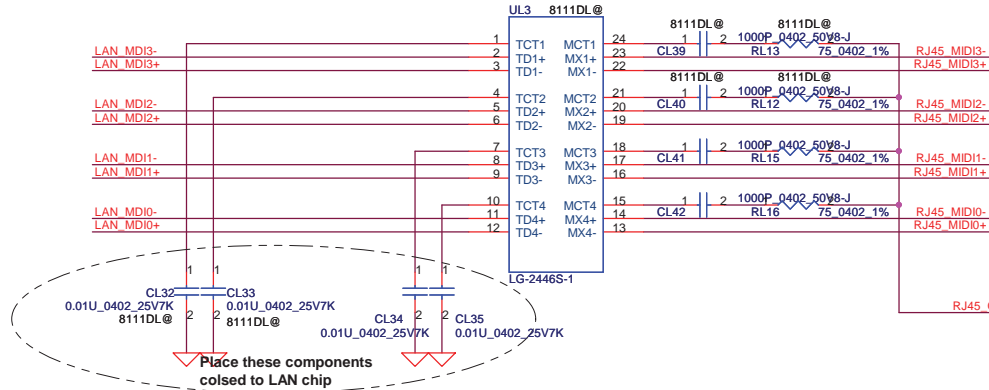


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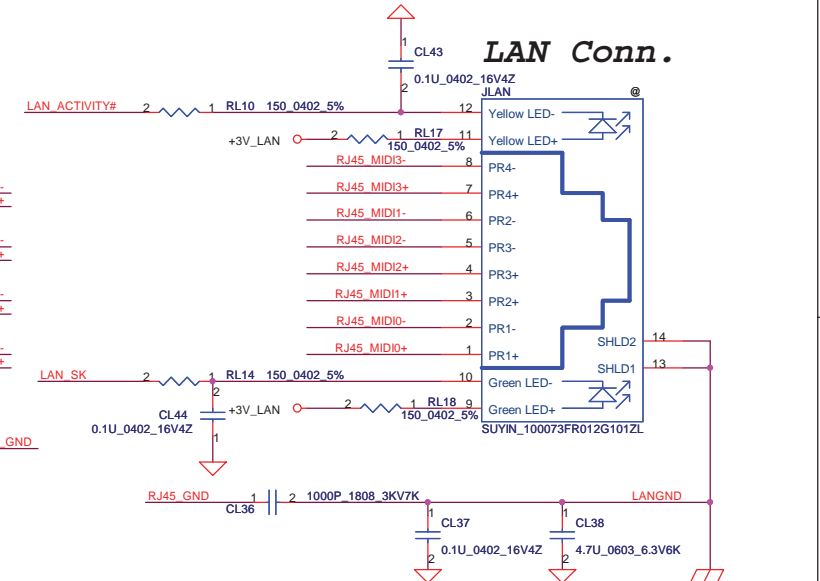
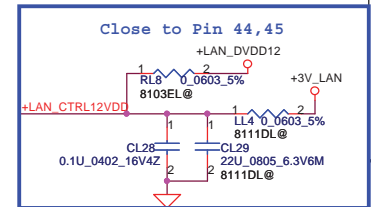
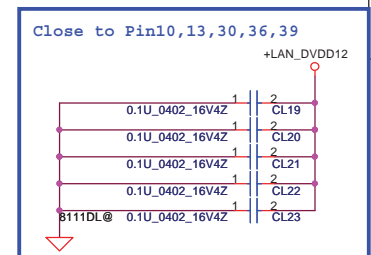
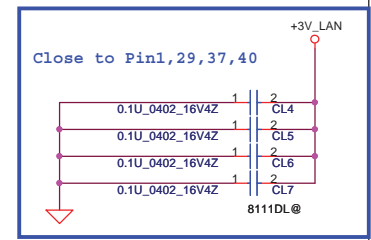
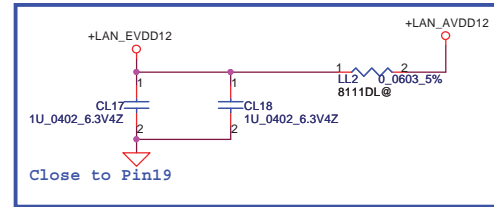
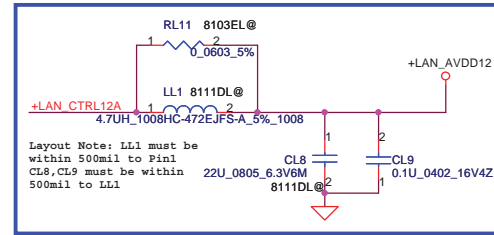


pin assignments table for difference

Pin	8111DL	8103EL
4	FB12	NC
8	MDIP2	NC
9	MDIN2	NC
10	AVDD12	DVDD12
11	MDIP3	NC
12	MDIN3	NC
13	EVDD12	VDDTX
23	GPO	NC
33	EEDO	LED3
34	EEDI	LED2
35	ESK	LED1
39	AVDD12	NC
40	AVDD33	NC
43	ENSR	NC
44	VDDSR	NC
45	VDDSR	VCTRL12D
48	SROUT12	VCTRL12A

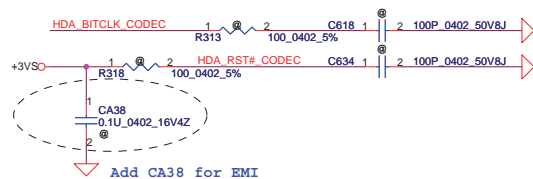
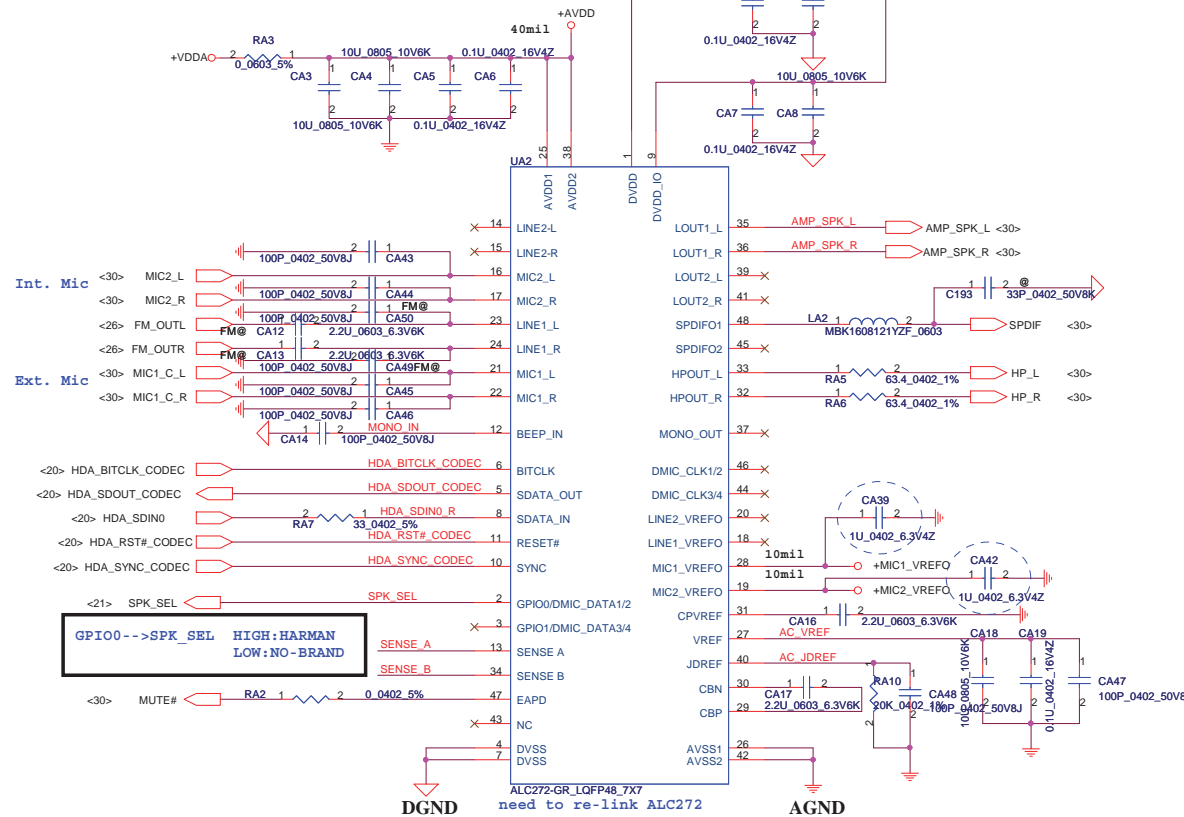


Place these components  
closed to LAN chip

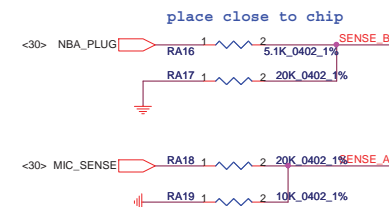
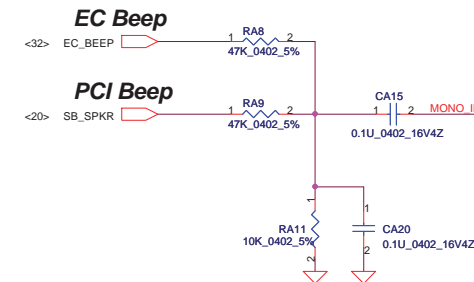
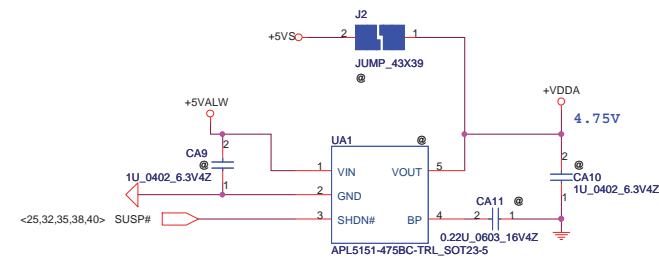
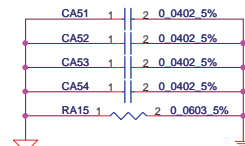


## LAN Conn.

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Change CA51-CA54 to 0 ohm for PC-Beep noise issue



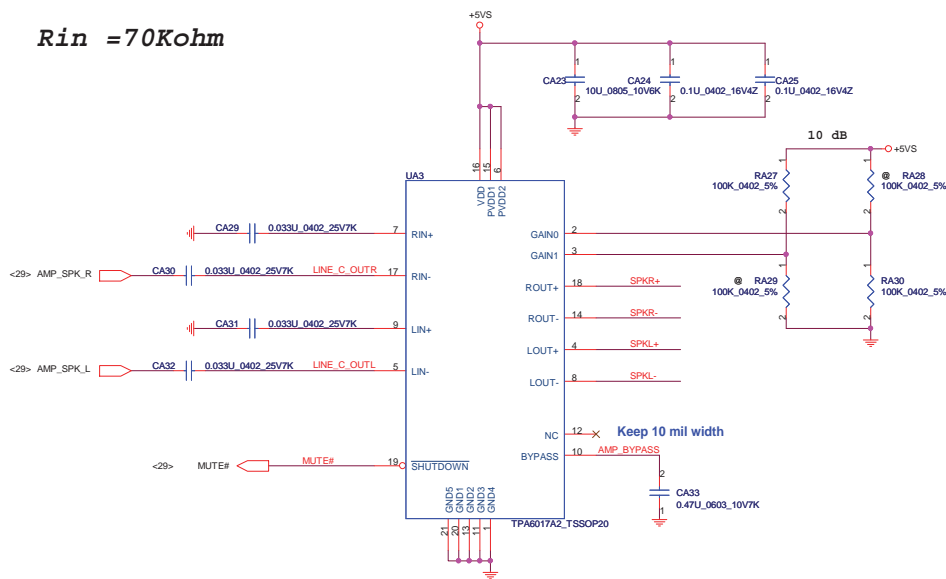
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	FM tuner
	5.1K	PORT-D (PIN 35, 36)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	Headphone out



# TPA6017 Medium Range Amplifier

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Rin = 70Kohm

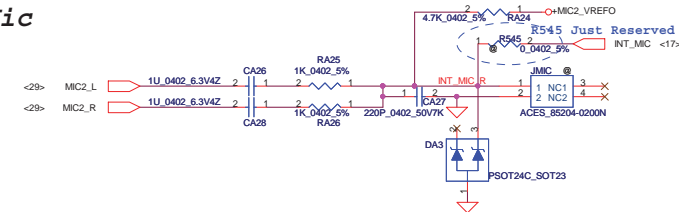


GAIN0	GAIN1	Av (db)	Rin (ohm)
0	0	6	90K
0	1	10	70K
1	0	15.6	45K
1	1	21.6	25K

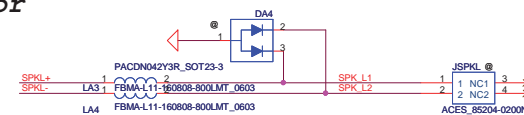
## Ext. Mic



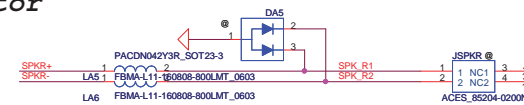
## Int. Mic



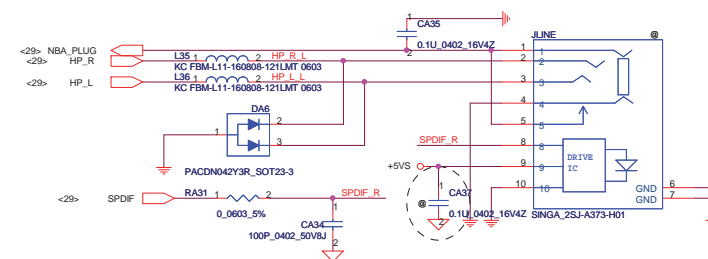
## Left Connector



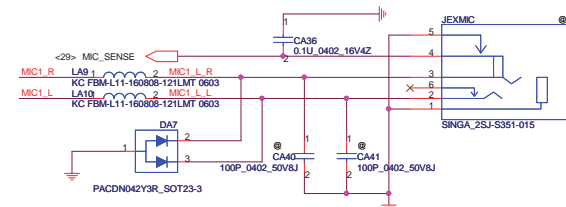
## Right Connector



## HeadPhone/LINE Out JACK



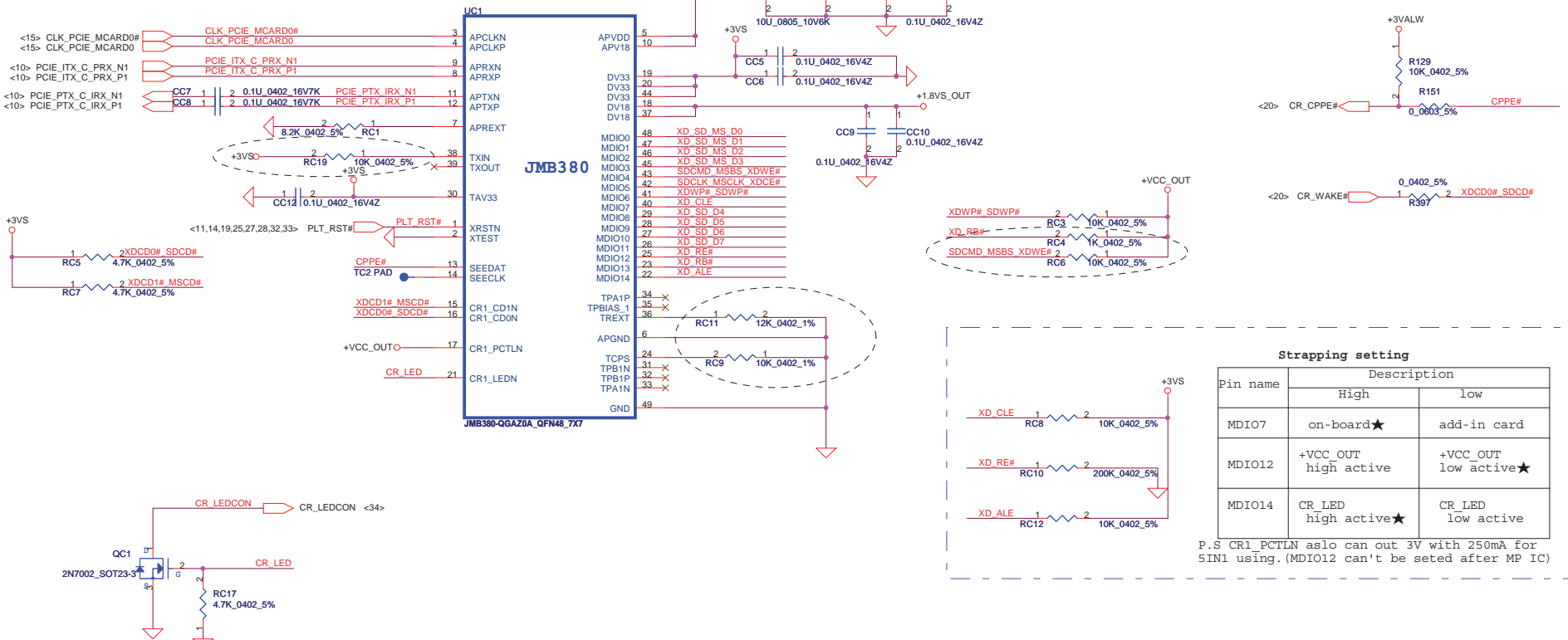
## Ext.MIC/LINE IN JACK



http://hobi-elektronika.net

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				Sheet	30 of 46

### Power Circuit

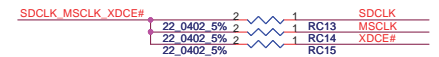
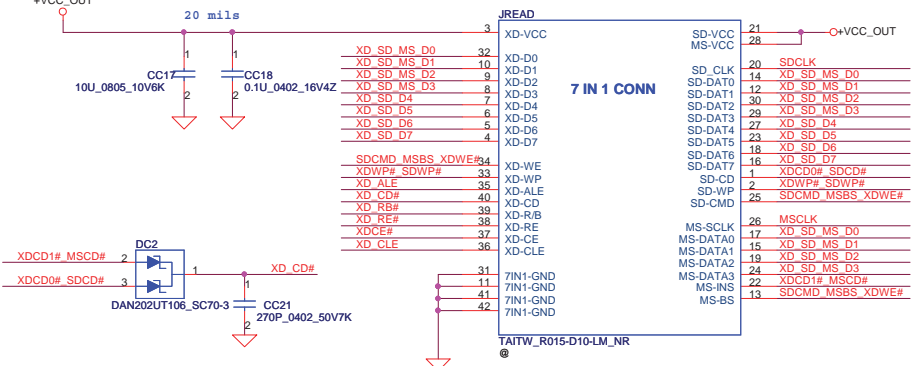


### Strapping setting

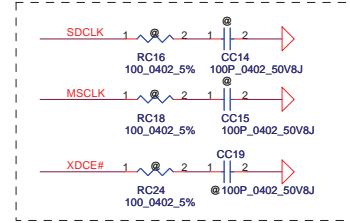
Pin name	Description	
	High	low
MDIO7	on-board★	add-in card
MDIO12	+VCC_OUT high active	+VCC_OUT low active★
MDIO14	CR_LED high active★	CR_LED low active

P.S CR1\_PCTLN also can out 3V with 250mA for 5IN1 using. (MDIO12 can't be seted after MP IC)

### Card Reader Connector

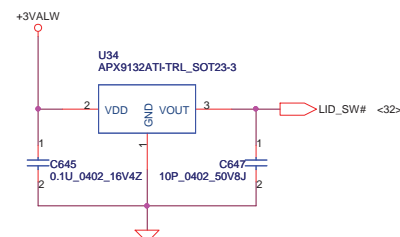
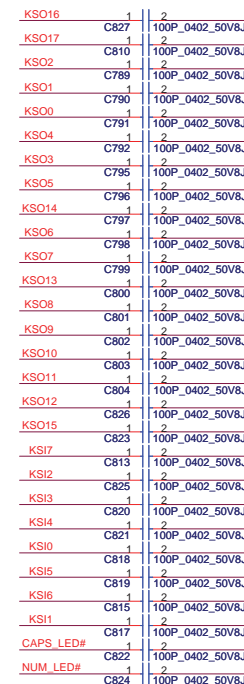
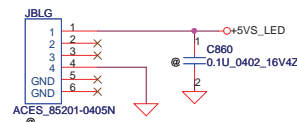


### For EMI

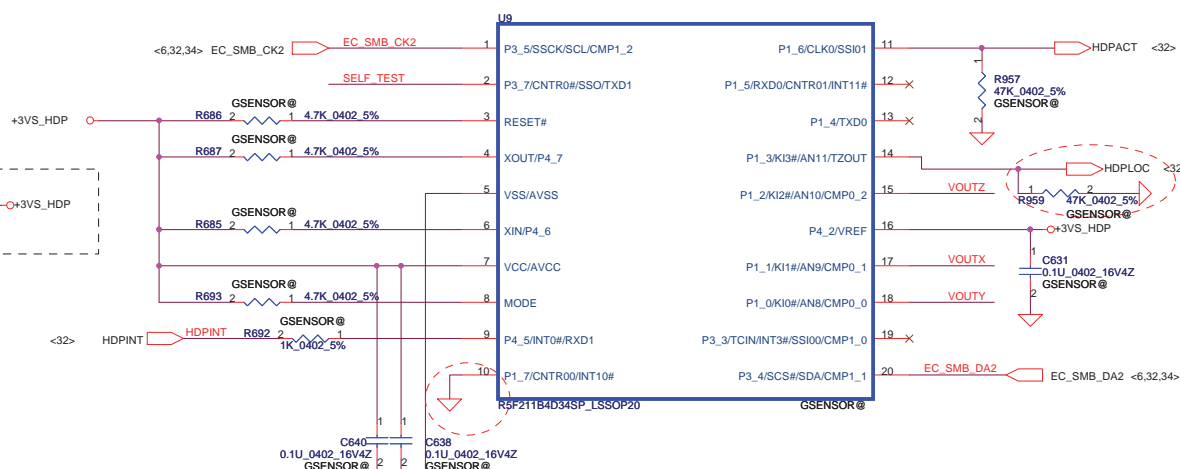
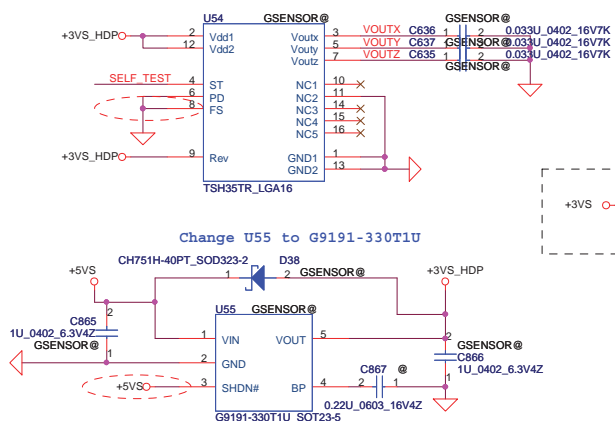


32.768KHZ\_12.5P\_1TJS125B4A421P  
<http://hobi-elektronika.net>

h t t p : *Lid* / l a p t o p b l u e

[illegible][illegible]

### G-Sensor

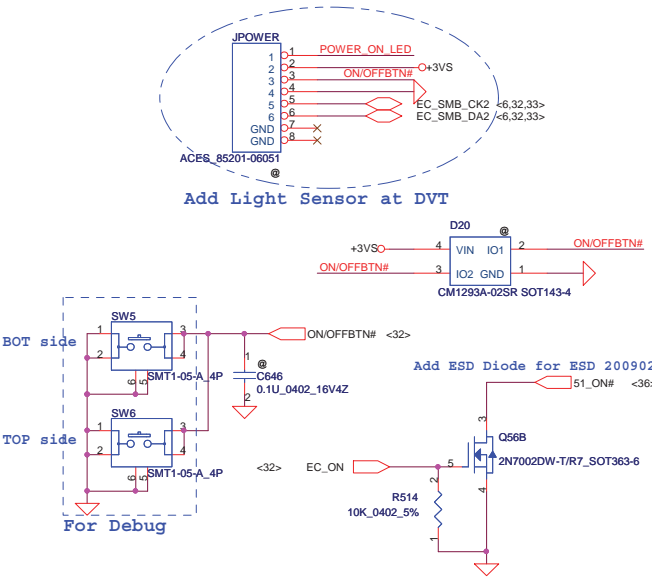


Pin configuration diagram for MMA7360LR2\_LGA14. The diagram shows the chip with pins 1-14. Pin 1 is labeled 'XOUT' and is connected to 'VDD'. Pin 2 is labeled 'YOUT' and is connected to 'VDD'. Pin 3 is labeled 'ZOUT' and is connected to 'VDD'. Pin 4 is labeled 'OG-DET' and is connected to 'VDD'. Pin 5 is labeled 'SLEEP# G-SELECT' and is connected to 'VSS'. Pin 6 is labeled 'ST' and is connected to 'VSS'. Pin 7 is labeled 'SELF TEST' and is connected to 'VDD'. Pin 8 is labeled 'VDD' and is connected to '+3VS\_HDP'. Pin 9 is labeled 'VSS' and is connected to 'VSS'. Pin 10 is labeled 'VDD' and is connected to 'VDD'. Pin 11 is labeled 'VSS' and is connected to 'VSS'. Pin 12 is labeled 'VDD' and is connected to 'VDD'. Pin 13 is labeled 'VSS' and is connected to 'VSS'. Pin 14 is labeled 'VDD' and is connected to 'VDD'. The chip is labeled 'MMA7360LR2\_LGA14'.

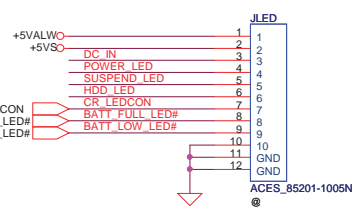
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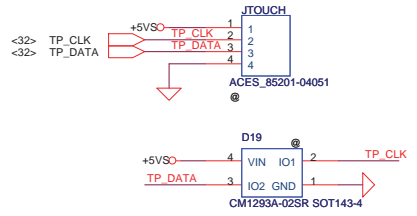
Power Button & PWR/B



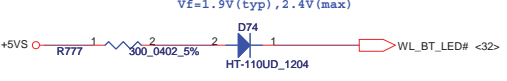
LED/B Connector



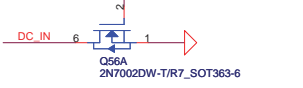
Touch/B Connector



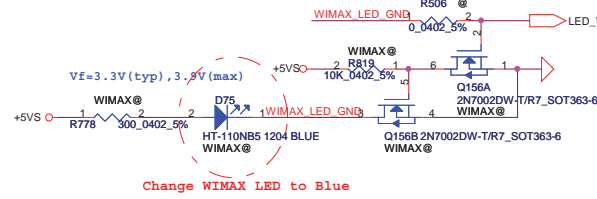
WL&BT LED



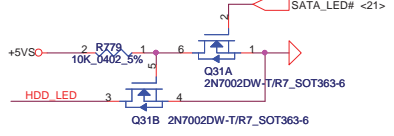
DC-IN LED



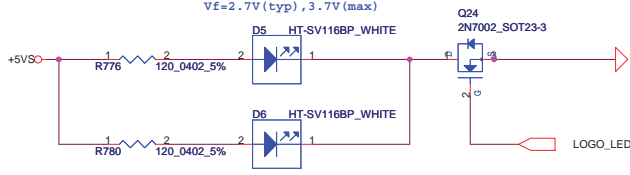
WiMAX LED



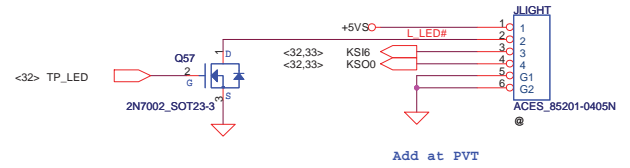
HDD LED



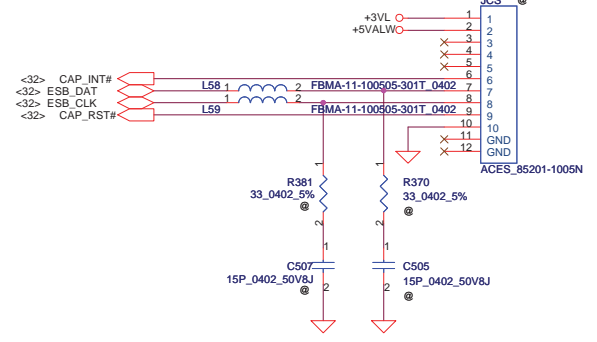
Satellite LED



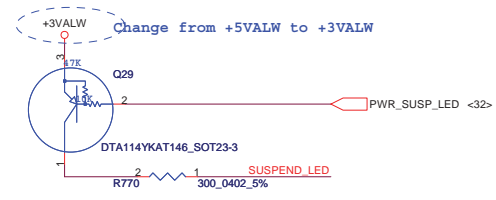
Light Pipe Connector



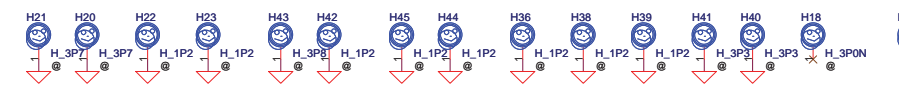
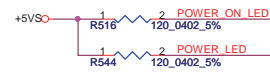
Caps Sensor Connector



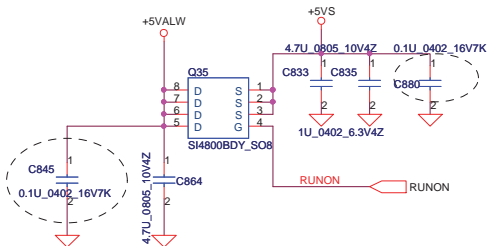
SUSPEND LED



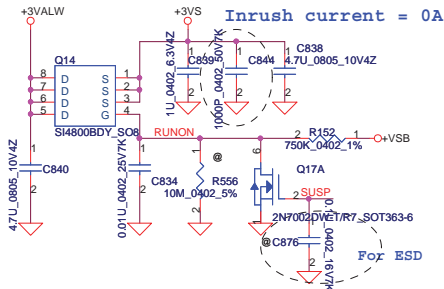
POWER LED



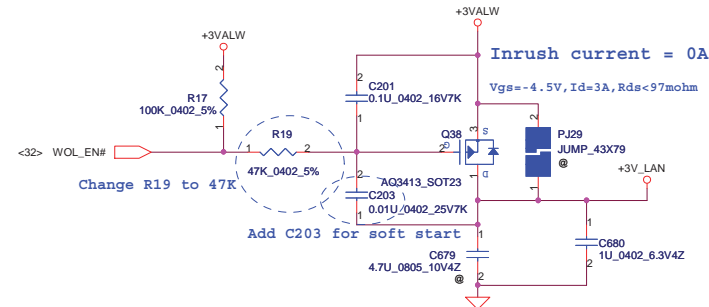
### +5VALW TO +5VS



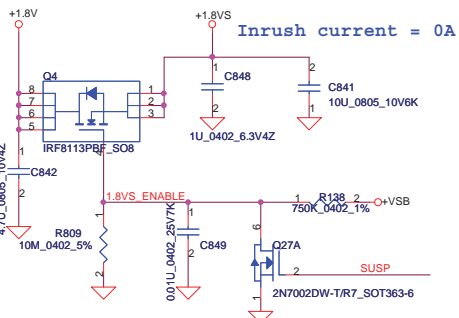
### +3VALW TO +3VS



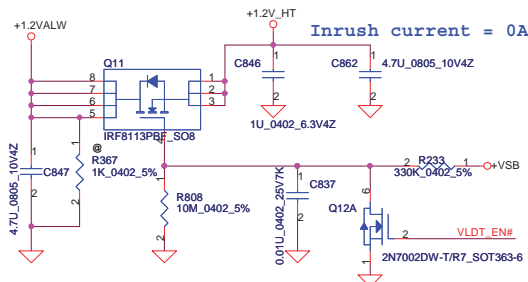
### +3VALW TO +3V\_LAN



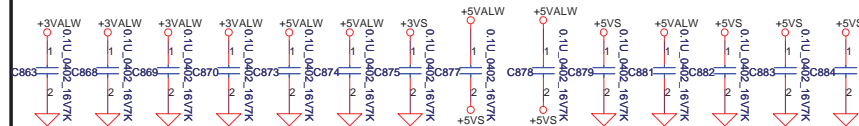
### +1.8V TO +1.8VS



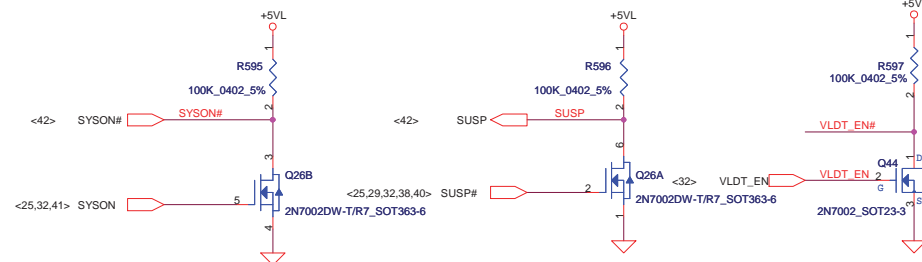
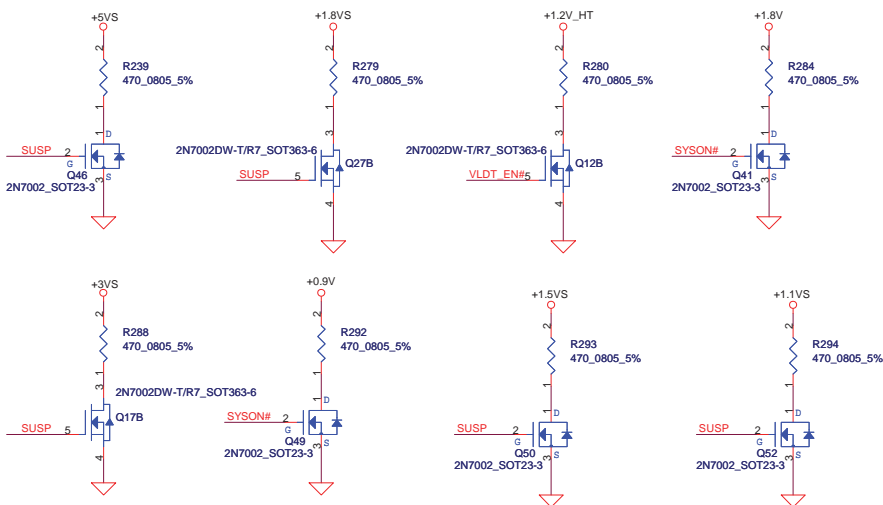
### +1.2VALW TO +1.2V\_HT



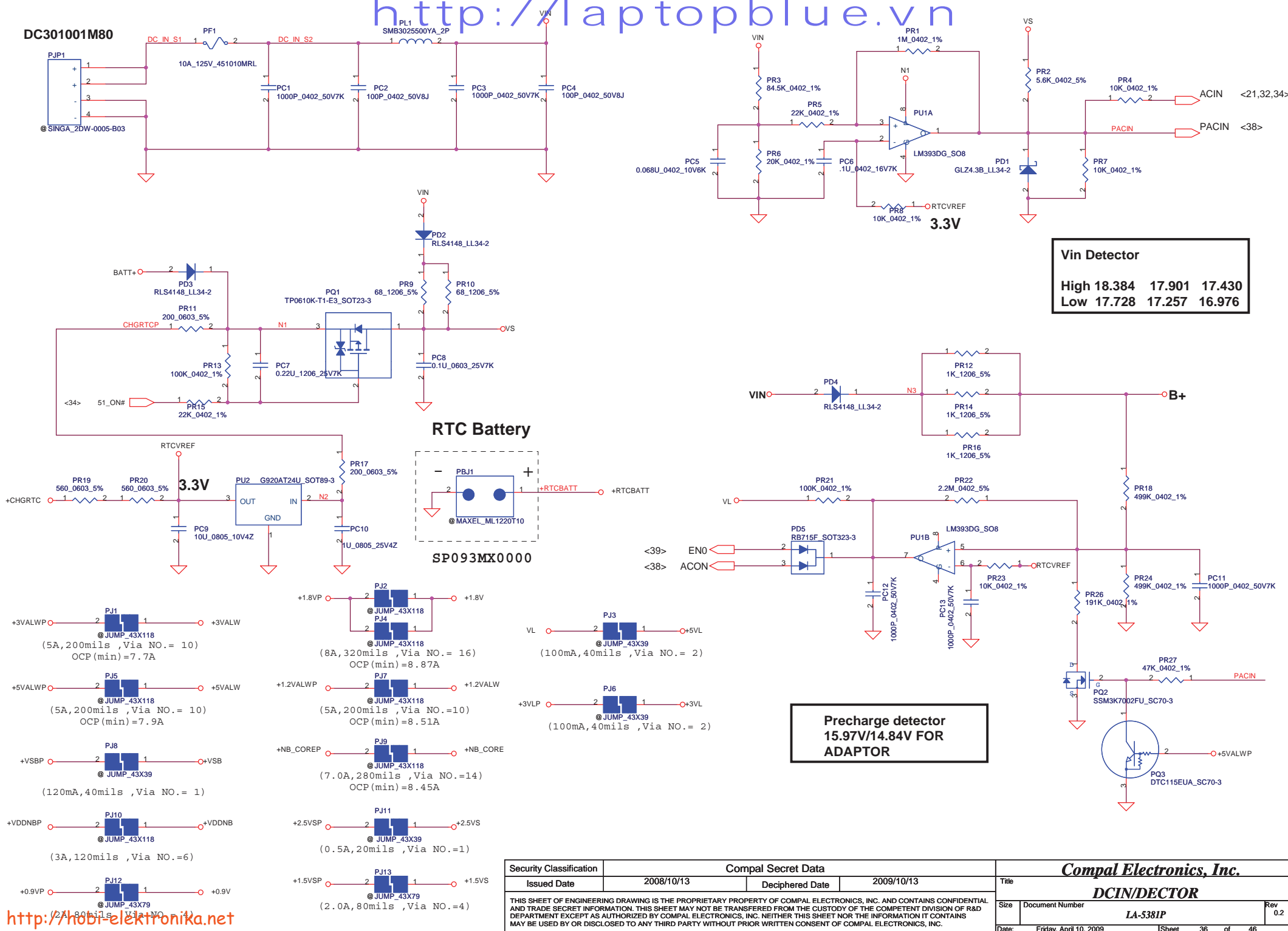
### Reserve for ESD



### Discharge circuit



# DC301001M80



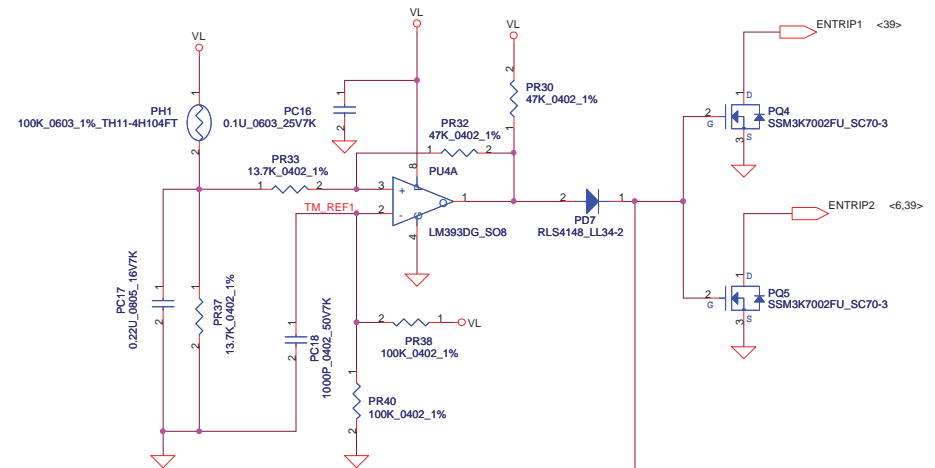
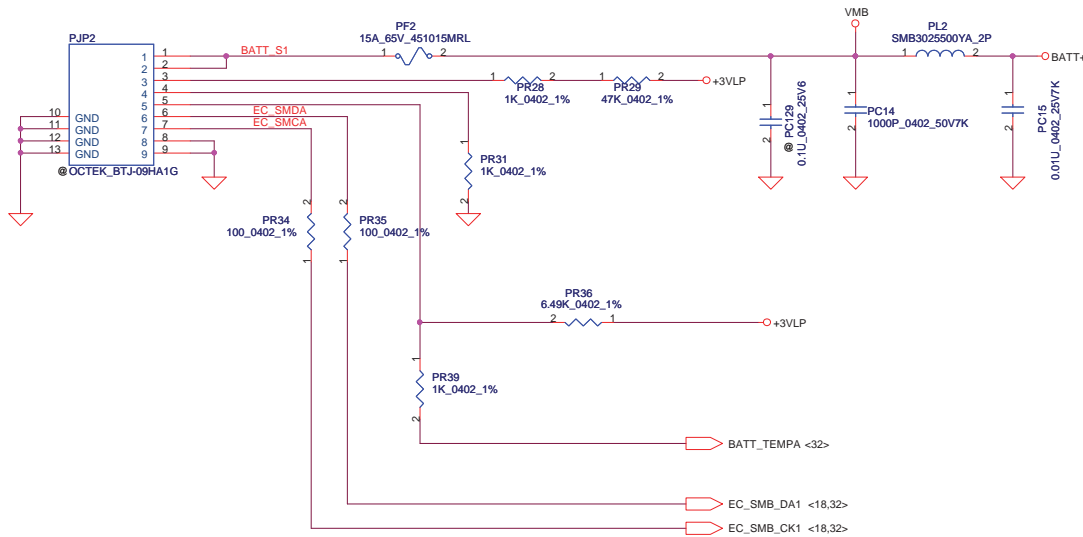
Vin Detector			
High	18.384	17.901	17.430
Low	17.728	17.257	16.976

**Precharge detector  
15.97V/14.84V FOR  
ADAPTOR**

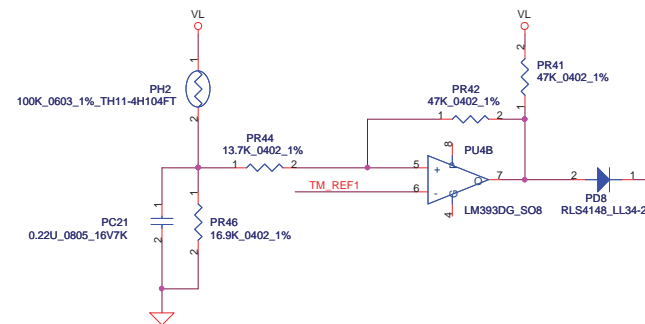
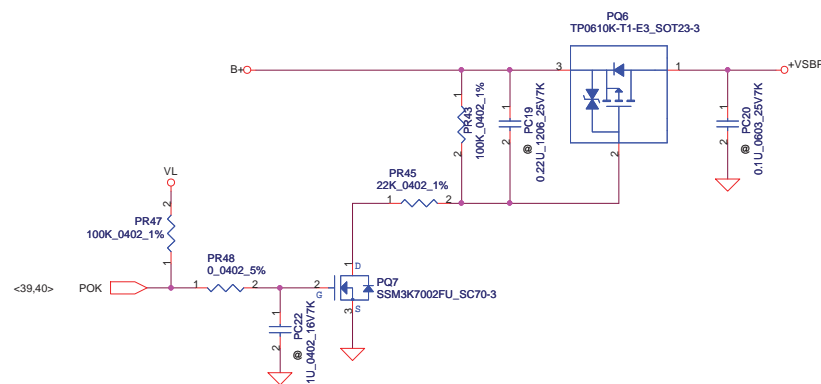
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Deciphered Date				2009/10/13				DCIN/DECTOR			
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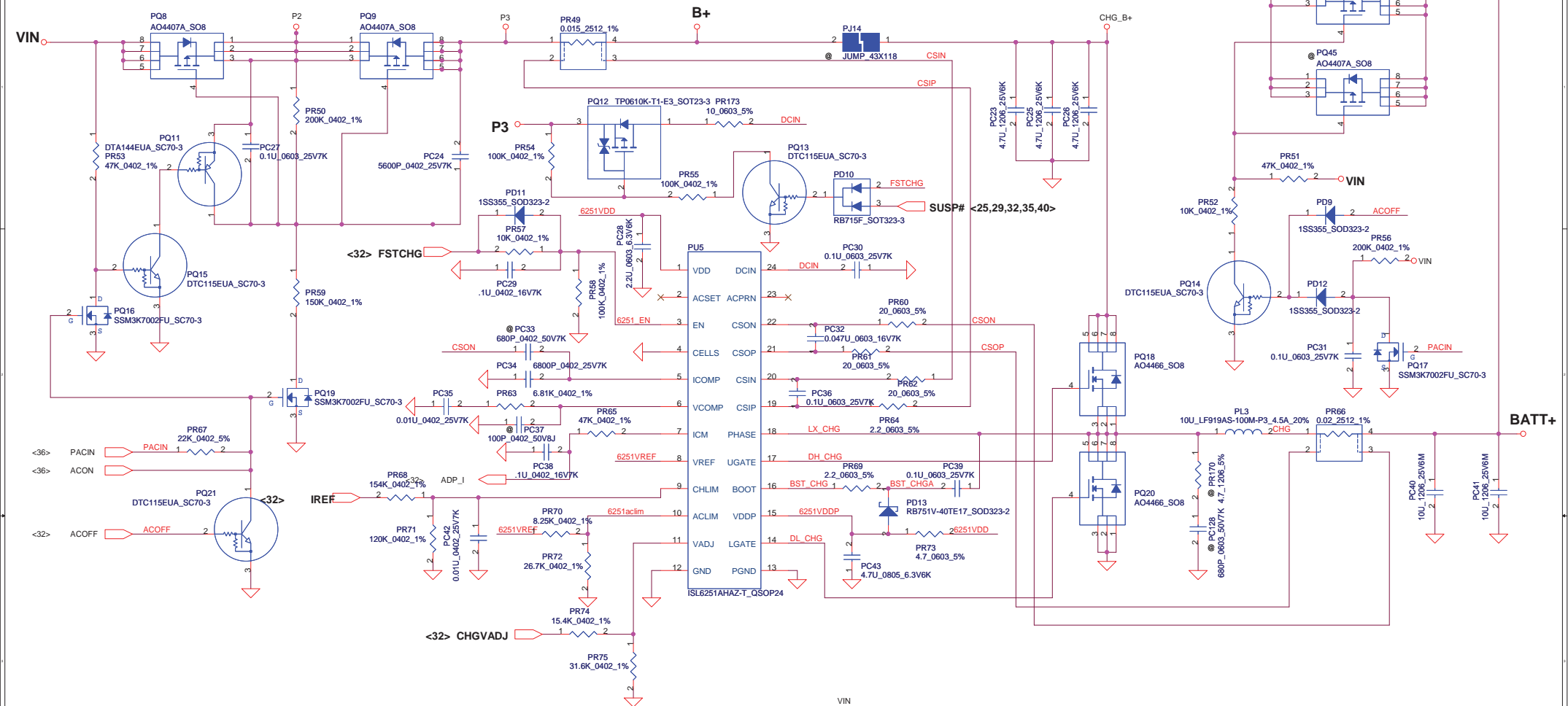


PH1 under CPU bottom side :  
CPU thermal protection at 96 degree C  
Recovery at 60 degree C



PH2 near main Battery CONN :  
BAT. thermal protection at 90 degree C  
Recovery at 53 degree C





CC=0.25A~3A  
IREF=1.016\*Icharge  
IREF=0.254V~3.048V  
VCHLIM need over 95mV

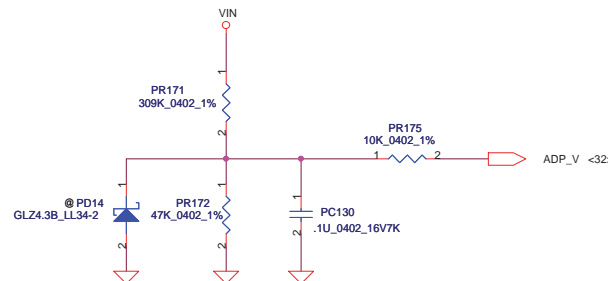
CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

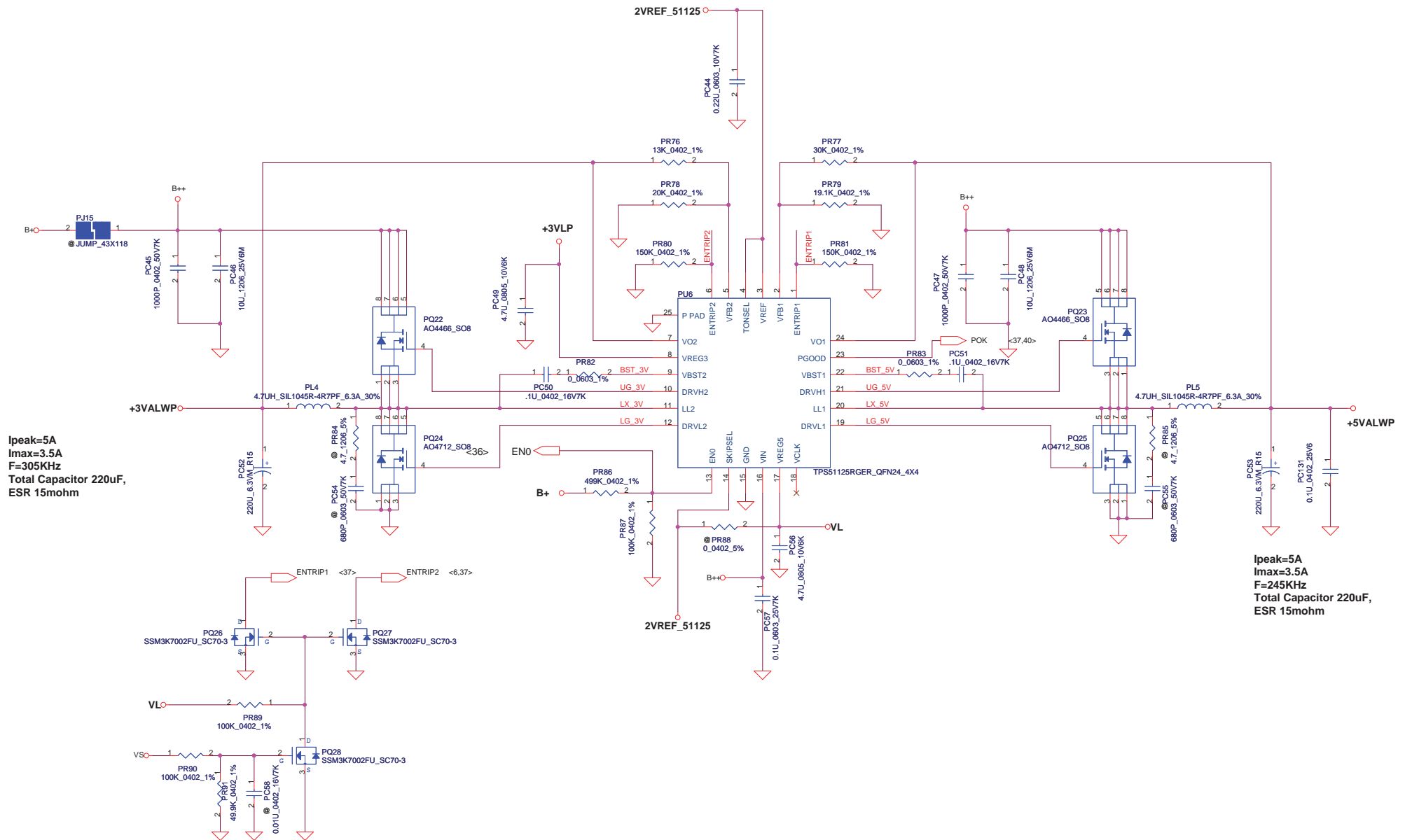
Iada=0~3.947A(75W) CP= 92%\*Iada; CP=3.65A

CP mode  
Vaclim=2.39\*(20K/(152K/(20K/(152K+24K/(152K)))=1.09986V  
Iinput=(1/0.02)\*((0.05\*Vaclim)/2.39+0.05)  
where Vaclim=1.09986V, Iinput=3.65A

CELLS	VDD	GND	Float
CELL number	4	3	2

90W Iadapter=0~4.74A PR49=0.015 ohm CP=4.357A PR70=53.6K PR72=20K  
120W Iadapter=0~6.32A PR49=0.015 ohm CP=5.81A PR70=8.25K PR72=26.7K

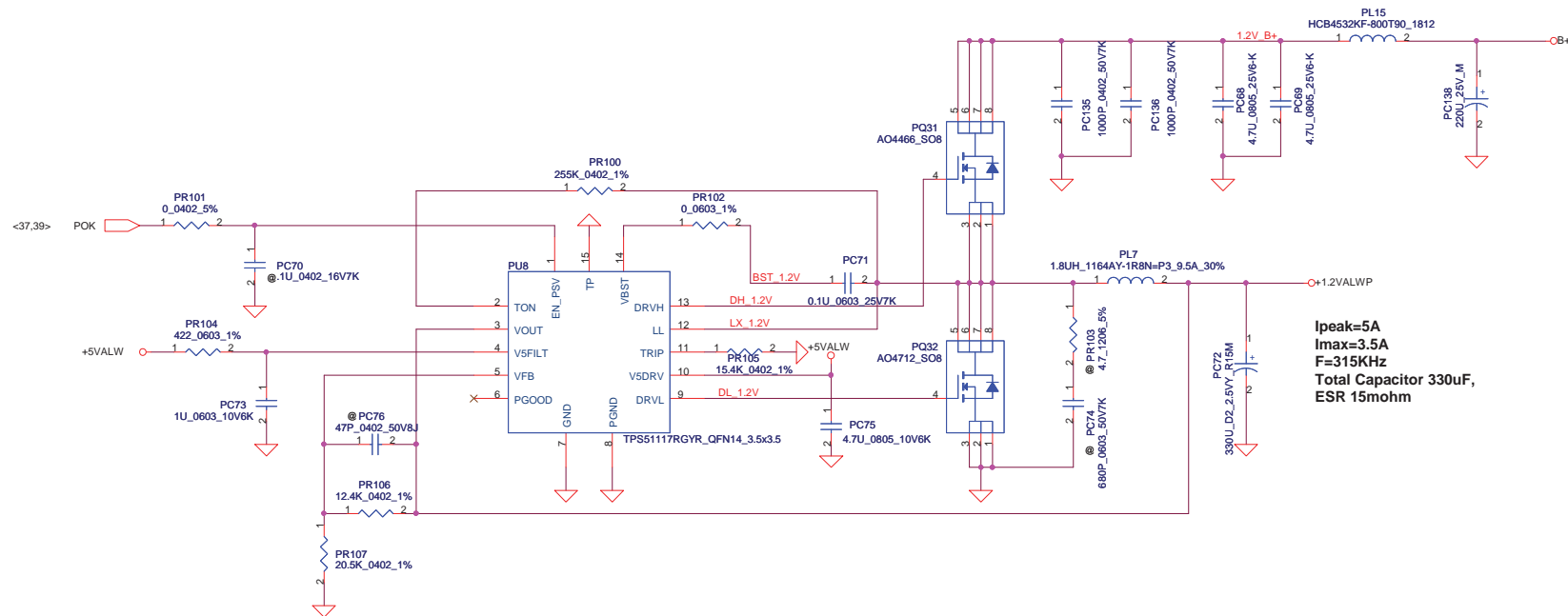
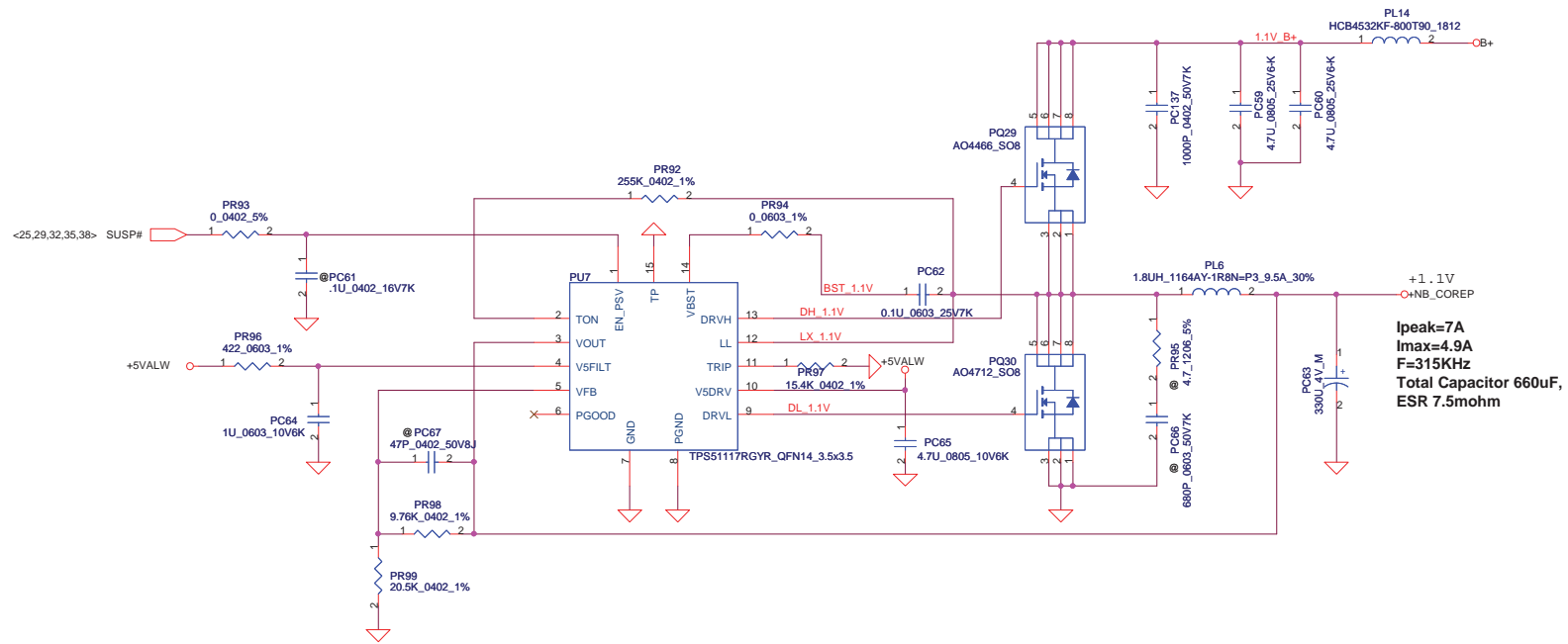




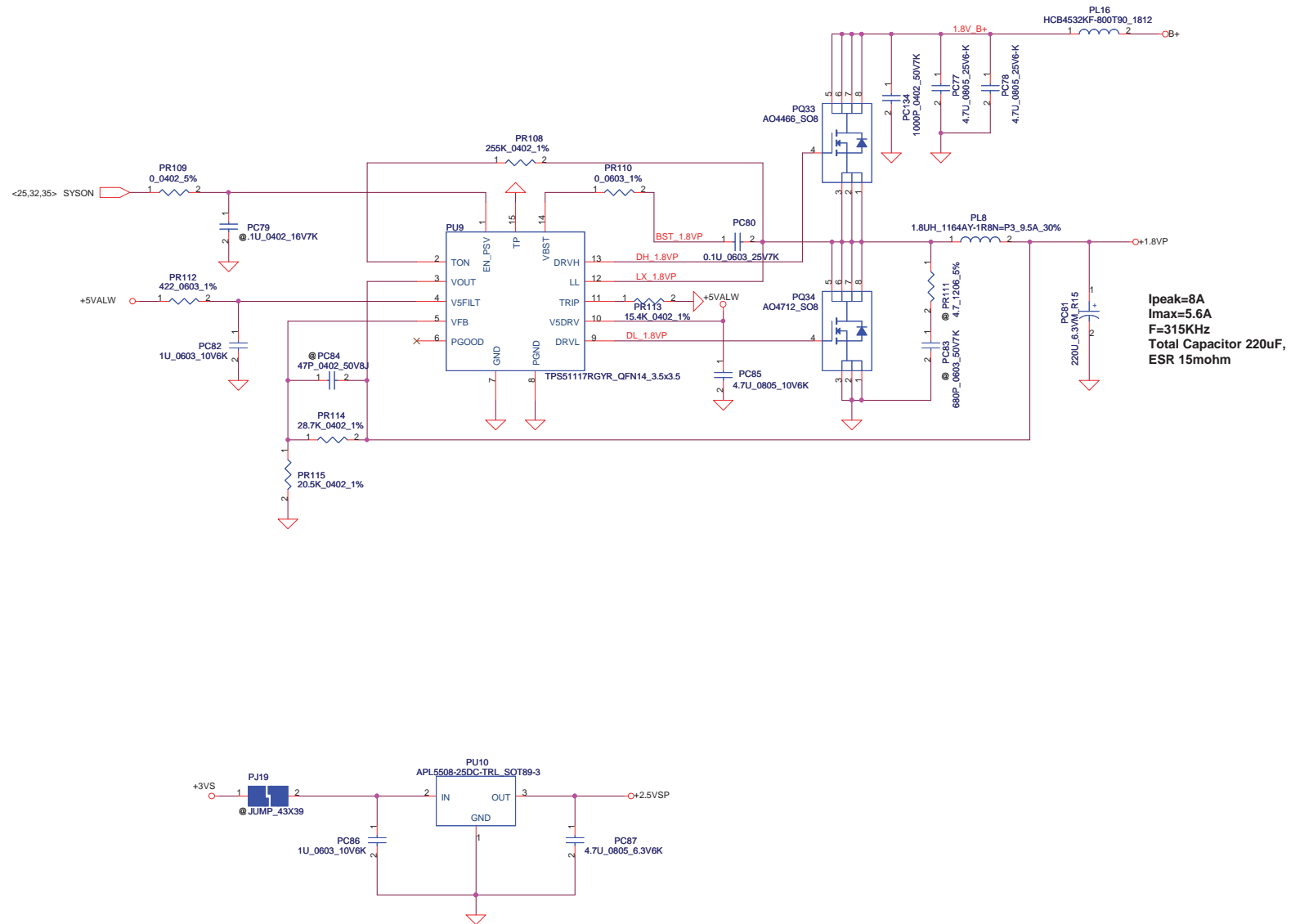
Ipeak=5A  
Imax=3.5A  
F=305KHz  
Total Capacitor 220uF,  
ESR 15mohm

Ipeak=5A  
Imax=3.5A  
F=245KHz  
Total Capacitor 220uF,  
ESR 15mohm

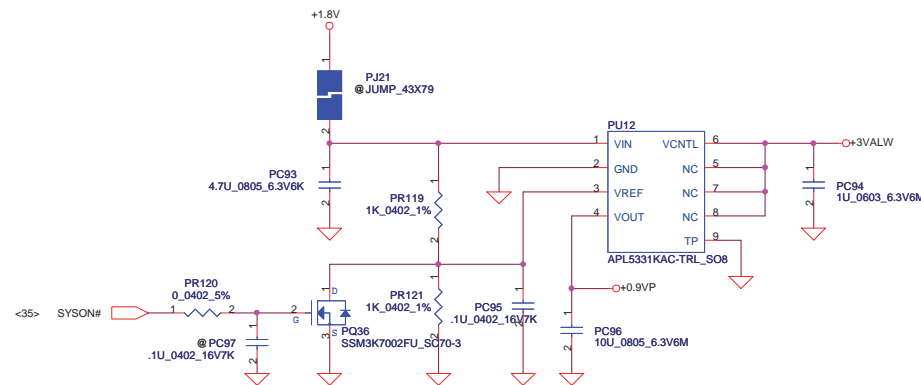
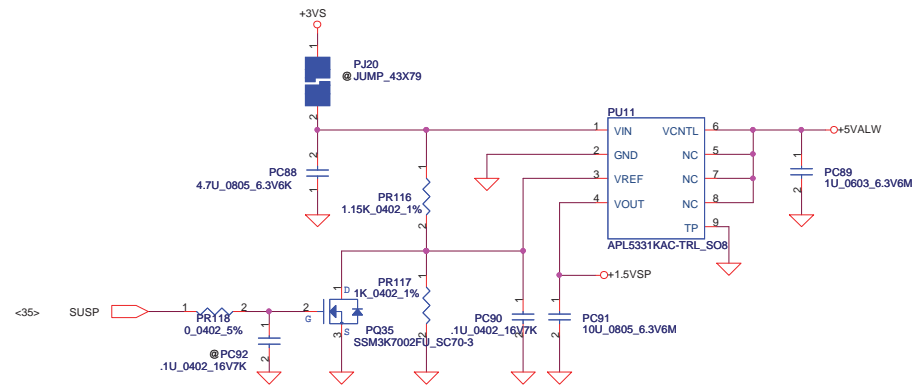
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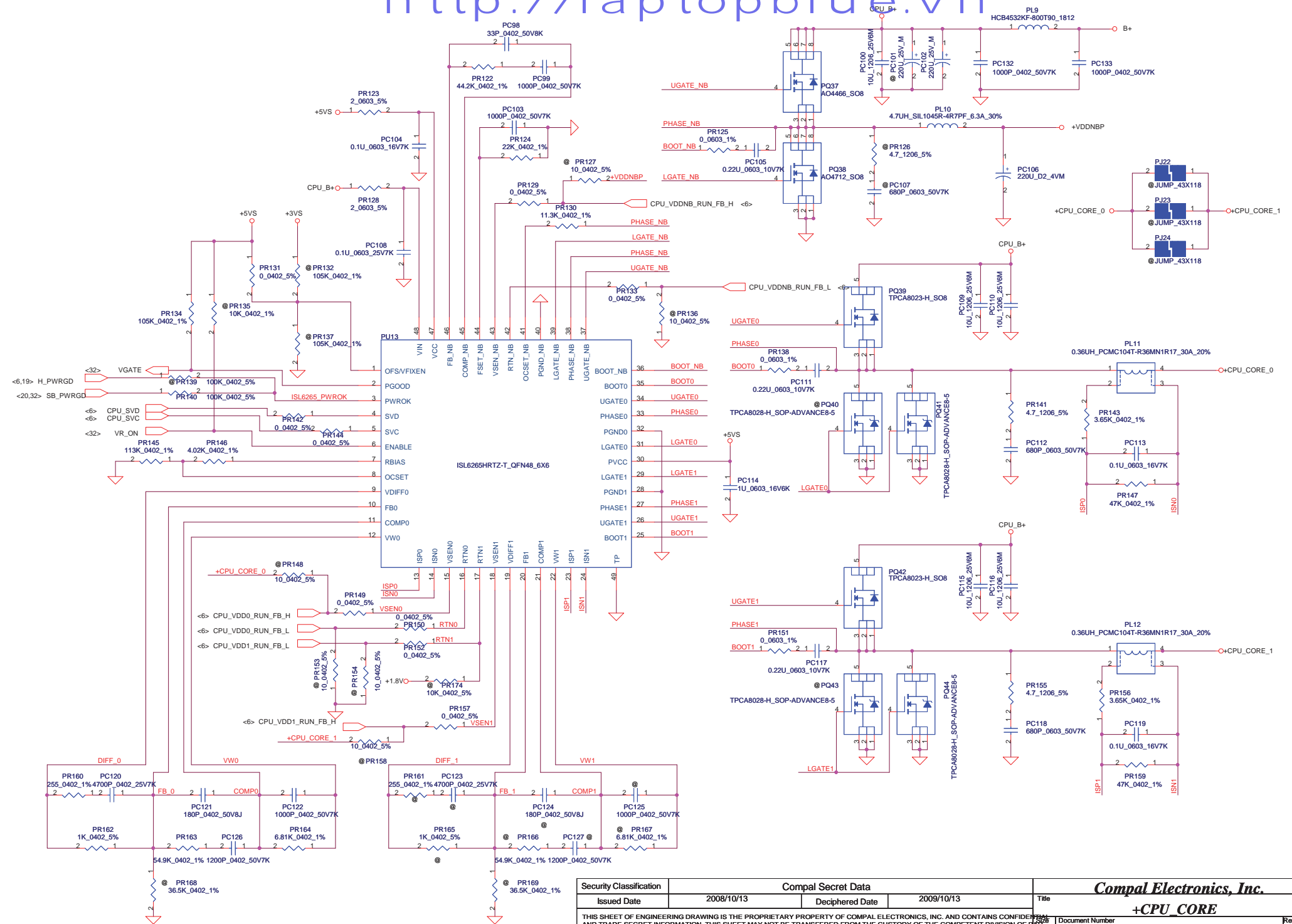
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						Document Number		LA-538IP	
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				LA-538IP				Rev			
				0.2				Date			
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				46							

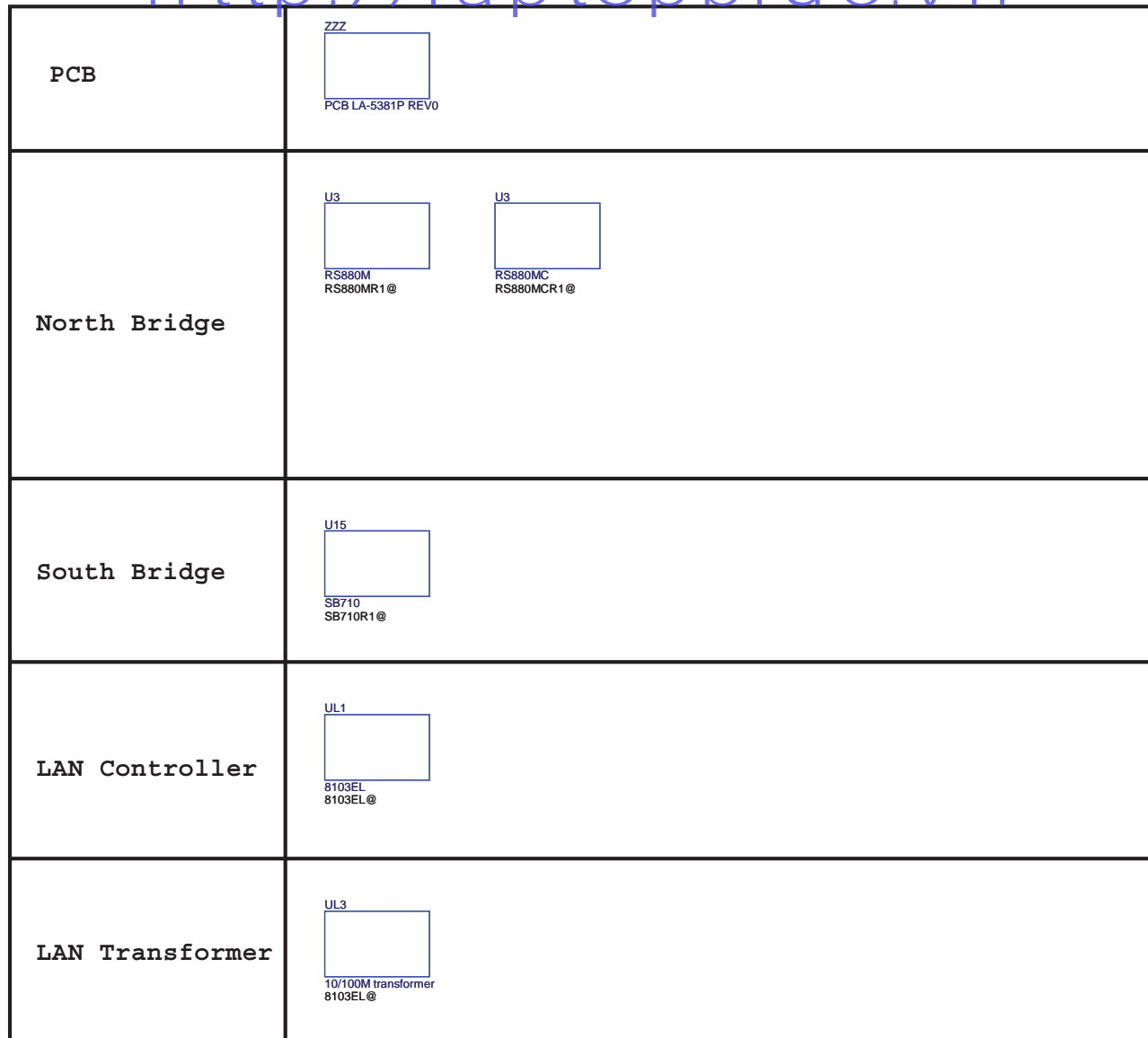


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				Date	Rev
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# HW4 Product Improvement Record (P.I.R.)

NSKAR LA-5381P SCHEMATIC CHANGE LIST  
REVISION CHANGE: 0.1 TO 0.2  
GERBER-OUT DATE: 2009/04/06

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	3/10	17	Change R156 to 10K pull down	Special LCD issue
2	3/10	30	Change RA16 to 1% tolerance	Codec requirement
3	3/10	33	Add R962-R965	Reserve GPIO to EC
4	3/13	22	Add R193-R196	Strap pin for SW
5	3/23	16	Add R540	Common Design
6	3/24	30	Add CA49,CA50	GPS issue
7	3/24	30	Add CA51-CA54	Common design
8	3/24	27	Add R722 and C754	Common design
9	3/25	27	Add R423	Common design
10	3/25	28	Add RM7 for Wimax module	Wimax issue
11	3/25	28	Add R822	Customer Request
12	4/9	31	Change UC1 from JMB385 to JMB380	For ME height limit
13	4/9	35	Add C863 to C884	For EMI request
14	4/9	18	Delete Q161 and add D53	For customer request
15	4/9	16	Delete Q162 and add D21	For customer request

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for Power Circuit

<i>Page#</i>	<i>Title</i>	<i>Date</i>	<i>Request Owner</i>	<i>Issue Description</i>	<i>Solution Description</i>
44	EVT	2009/02/25	POWER		NSKAE for Tigirs(UMA)
39	EVT	2009/03/16	POWER		For CHGVADJ (memo)
41	EVT	2008/12/30	HW		meet AMD RS780 SPEC (memo)
41	EVT	2009/02/10	POWER		Noise (memo)
41-42	DVT	2009/03/31	POWER		Noise
40	DVT	2009/03/31	HW		For HDMI
41	DVT	2009/03/31	POWER		Noise
41-42	DVT	2009/03/31	POWER		Noise
41-42	DVT	2009/03/31	POWER		For EMI
	Add PL13,PL14,PL15,PL16				
39	DVT	2009/03/31	POWER		For ADP_I
40	DVT	2009/03/31	POWER		For common circuit
39	DVT	2009/03/31	POWER		For 12 Cell charge 3.6A
41	DVT	2009/03/31	HW		Change to 12.1K and 19.6K
44	PVT	2009/03/31	POWER	No issue	Change to common parts

Security Classification		Compal Secret Data		<div>Compal Electronics, Inc.</div>		
Issued Date	2008/10/13	Deciphered Date	2009/10/13	Title	Power PIR	
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