


MODEL		REV	CHANGE LIST				Model	TW3A M/B	
							Page	From	To
TW3A M/B	3A	First Release 31T3MB0033 (E200601-0720) 2006/1/10					1	3A	
	3B	E200601-5311 2006/2/8					2	3A	
							3	3A	
							4	3A	
							5	3A	
							6	3A	
							7	3A	
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							10	3A	
							11	3A	
							12	3A	
							13	3A	
							14	3A	3B
							15	3A	
							16	3A	
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							19	3A	3B
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							23	3A	3B
							24	3A	
							25	3A	
							26	3A	3B
							27	3A	3B
							28	3A	
							29	3A	3B
							30	3A	
							31	3A	
							32	3A	3B
							33	3A	3B
							34	3A	
							35	3A	3B
							36	3A	3B
							37	3A	
							38	3A	
							39	3A	
							40	3A	
							41	3A	3B
							42	3A	
							43	3A	3B
							44	3A	
							45	3A	
							46	3A	
							47	3A	
							48	3A	
 PROJECT : TW3A Quanta Computer Inc.		PROJECT: TW3A		ASSY P/N:31TW3MB0033		TITLE:		DOC NO:204	
		APPROVED BY : Johnson Hsu		DRAWING BY : Tony Huang		VER:3B		DATE :02/08/2006	
								SHEET 1	

# TW3A- DESIGN

31TW3MB00XX

**Yonah/Merom**  
31W/35W  
(478 Micro-FCPGA)

PG 4,5

**CPU VR**

PG 37

DC/DC  
+3VSUS  
+5VSUS  
PG43

DC/DC  
+3VPCU  
+5VPCU  
PG38

DC/DC  
+1.05V  
+1.5V  
PG37

**CLOCKS**  
ICS954206  
PG 3

**RUN POWER SW**  
PG 43

**AC/BATT CONNECTOR**  
PG 40

**BATT CHARGER**  
PG 40

## PCB STACK UP

LAYER 1 : TOP  
LAYER 2 : SGND1  
LAYER 3 : IN1  
LAYER 4 : IN2  
LAYER 5 : VCC  
LAYER 6 : IN3  
LAYER 7 : SGND2  
LAYER 8 : BOT

**DDRII SODIMM1**  
PG 16,17

DDRII 667mhz

**DDRII SODIMM2**  
PG 16,17

DDRII 667mhz

**FSB**  
133MHZ

**Calistoga PM**  
945PM

**Integrated VGA Function**  
1466 BGA  
PG 6,7,8,9,10,11

**DMI interface**

**ICH7-M**

652 BGA

PG 12,13,14,15

**LPC**

**KBC**  
PC87541V  
PG 36

**X-Bus**

Key Matrix  
PG 34

Touch Pad  
PG 34

Flash  
PG 36

**Internal ODD CD-ROM**  
PG 29

Azalia

**Conexant Audio**  
CX20549-12  
PG 30

**AUDIO Amplifier**  
PG 31

Jack to Speaker  
PG 31

Audio Jacks  
PG 30

**MDC DAA**  
CX20548-A  
PG 32

MODEM RJ 11  
PG 32

**SATA - HDD**  
PG 29

SATA0

**PATA - HDD**  
PG 29

PATA 100

USB2.0 (P0-P7)

USB2.0 (P5)

USB2.0 (P0-P1,P4)

PCI-E, 1X

PCI-E, 1X

PCI-E, 1X

**PCI Bus 33MHz**

**TI PC7402**  
PG 27

IEEE1394 CONN  
3 in 1 Card reader  
PG28

PCI-Express 16X

**nVIDIA**  
NV72M/MV  
(64 Bit B/W)

DDRII  
16M\*16(128MB)  
32M\*16(256MB)  
(Bank\*4)

PG 18-21

**Panel Connector**  
PG 22

**S-Video**  
PG 35

**VGA,DVI**  
PG 23

**Bluetooth**  
PG 33

**USB2.0 I/O Ports**  
PG 26

**LAN**  
88E8038/88E8055  
PG 24

**Mini PCI-E Card**  
PCI Express Mini Card  
PG 33

**Express Card x1 NEW CARD**  
PG 33

**Magnetics**  
PG 25

**Power On**  
Power Input  
LPT PORT  
COM PORT  
LAN  
VGA  
Headphone  
1394  
USB X 2

**RQ6**

**Replicator Daughter Board**

USB

PG 35



**PROJECT : TW3**  
**Quanta Computer Inc.**

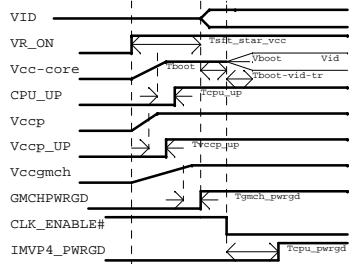
Size Document Number Rev 3A  
Block Diagram  
Date: Thursday, June 15, 2006 Sheet 1 of 48

## Board Stack up Description

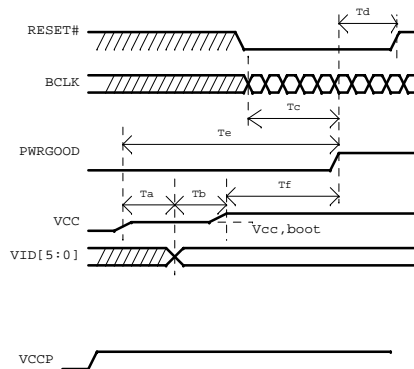
## PCB Layers

Layer 1		TOP(Component,Other)
Layer 2		Ground Plane
Layer 3		IN1
Layer 4		IN2
Layer 5		Power Plane
Layer 6		IN3
Layer 7		Ground Plane
Layer 8		BOTTOM

Power On Sequencing Timing Diagram



Dothan Power-up Timing Specifications

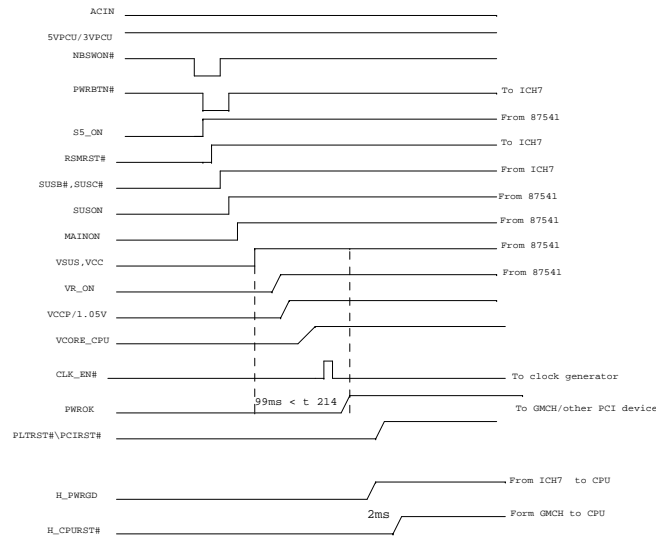


Ta=VCC and VCCP assertion to VID[5:0] valid  
 Tb=VID[5:0] stable to VCC valid  
 Tc=BCLK stable to PWRGOOD assertion  
 Td=PWRGOOD to RESET# de-assertion time  
 Te=Vcc,boot valid to PWRGOOD assertion time

## Voltage Rails

Voltage Rails	ON S0-S2	ON S3	ON S4	ON S5	Control signal
VCC CORE Core voltage for Processor	X				VR_ON 0.726V~0.94V
VCCP Core voltage for CPU / NB	X				VR_ON
SMDDR_VTERM0.9V for DDR2 Termination voltage	X				MAINON
RVCC1.5	X	X	X		RVCC_ON
RVCC3	X	X	X		RVCCD
VCC1.5	X				MAIND
VCC2.5	X				MAINON
VCC3	X				MAIND
VCC5	X				MAIND
1.8VSUS	X	X			SUSON
3VSUS	X	X			SUSD
5VSUS	X	X			SUSD
3VPCU	X	X	X	X	VL
5VPCU	X	X	X	X	VL
9VPCU	X	X	X	X	5VPCU

ACIN POWER ON TIMING

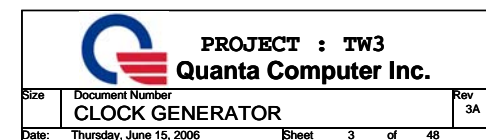


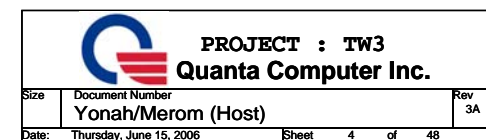
Voltage Rails	ON S0-S1	ON S3	ON S4	ON S5	Control signal
VCC CORE Core voltage for Processor	X				VRON
GMCH_VTT Core voltage for GMCH 1.05V	X				MAINON
SMDDR_VTERM 0.9V for DDR 2 Termination voltage	X				MAINON
SMDDR_VREF 0.9V for DDR 2 Reference Voltage	X				MAINON
GMCH 1.5V	X				MAINON
1.8VSUS 1.8V for DDR 2 voltage	X	X			SUSON
2.5V	X				MAINON
3VPCU	X	X	X	X	VL
5VSUS	X	X			MAINON
2.5V	X	X	X	X	MAINON
3VPCU	X	X	X	X	VL
5VSUS	X	X			MAINON
2.5V	X	X	X	X	MAINON
VR	POWER SOURCE	X	X	X	

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
PCI#402	AD17	REQ2# / GNT2#	PRQ C/D

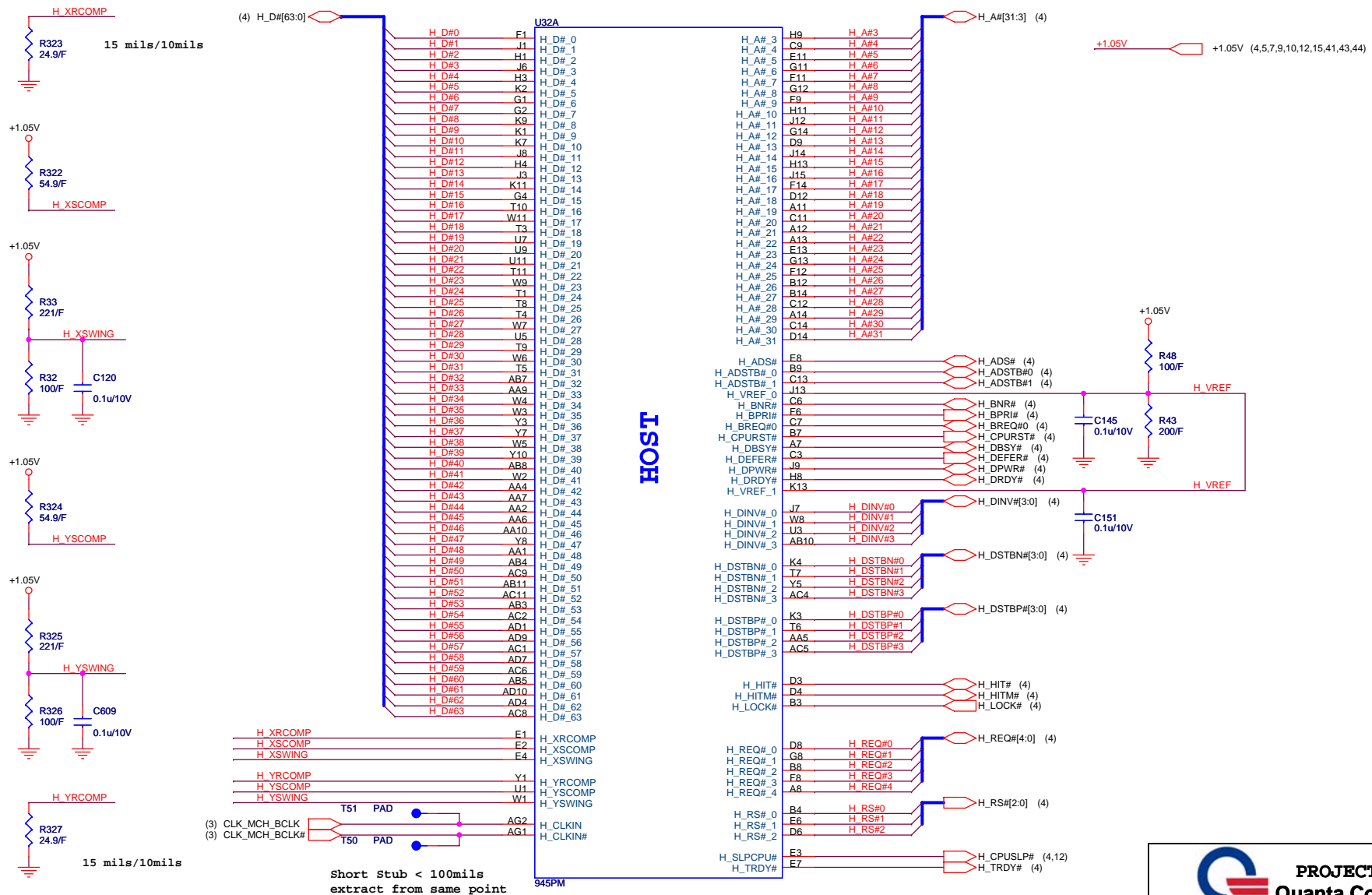
http://laptopblue.vn

3

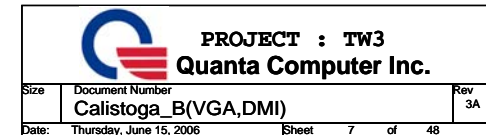




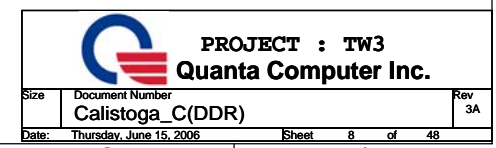


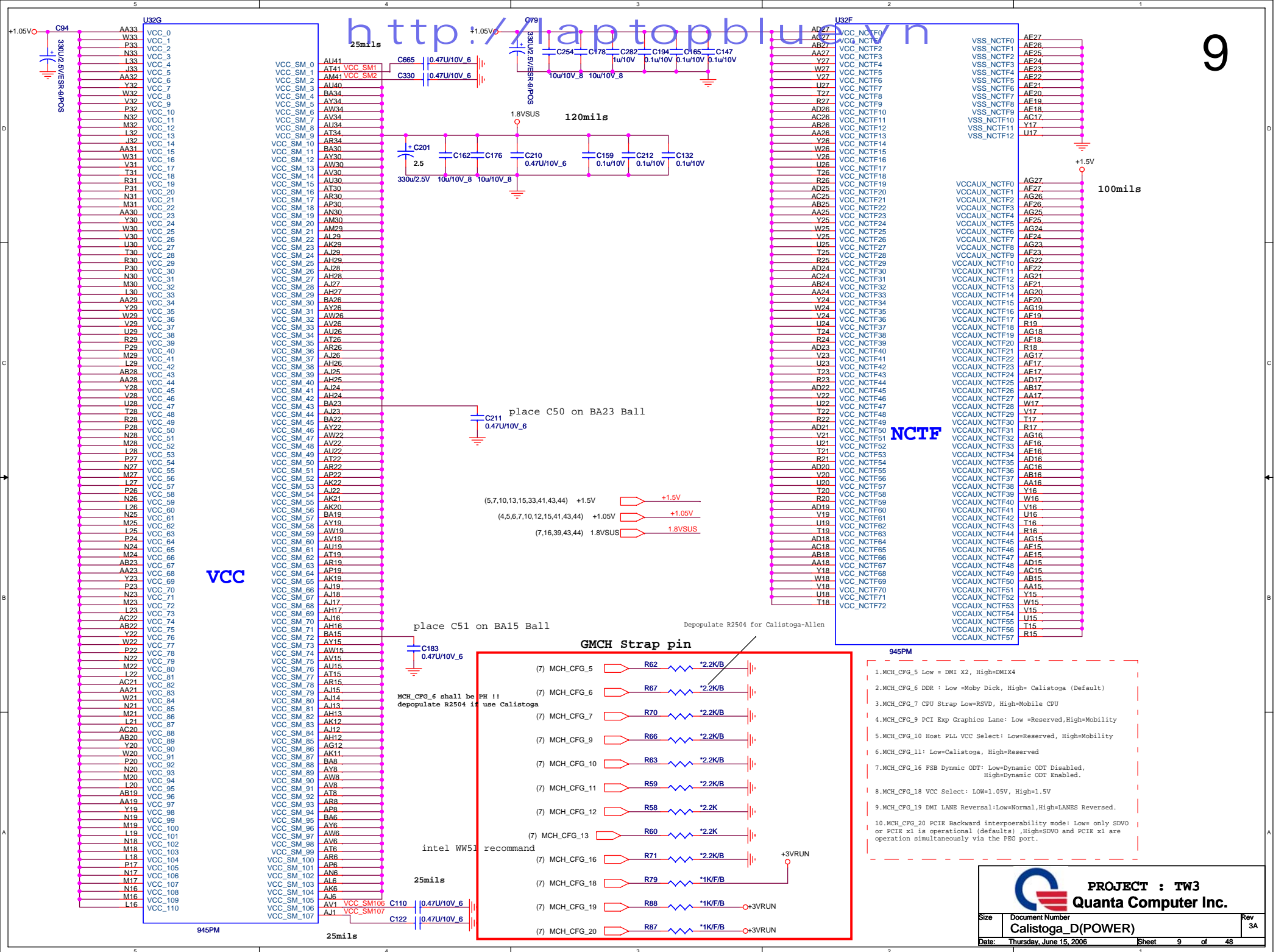


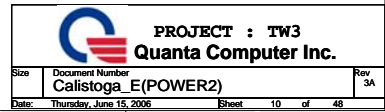


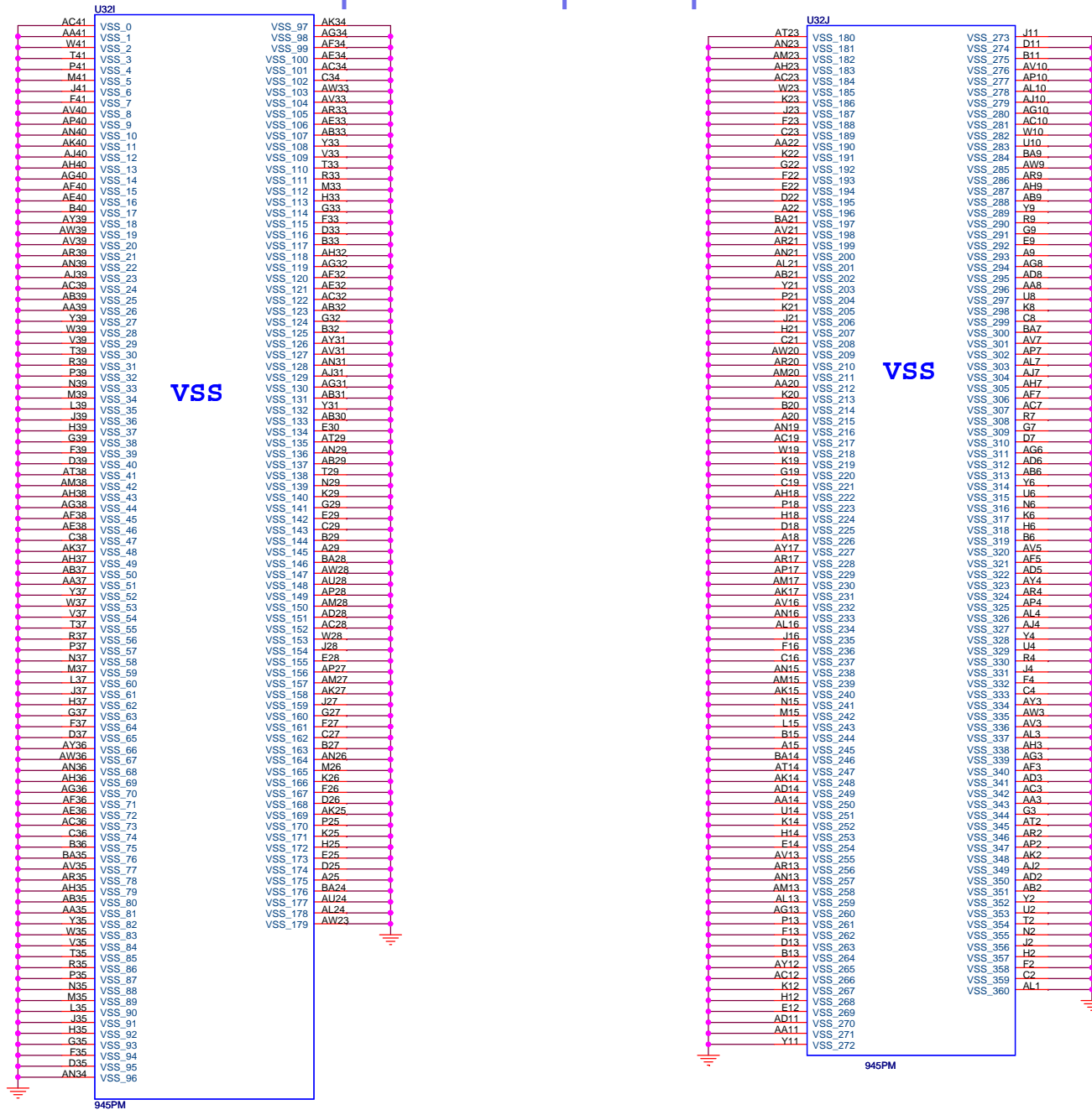


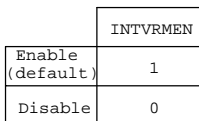


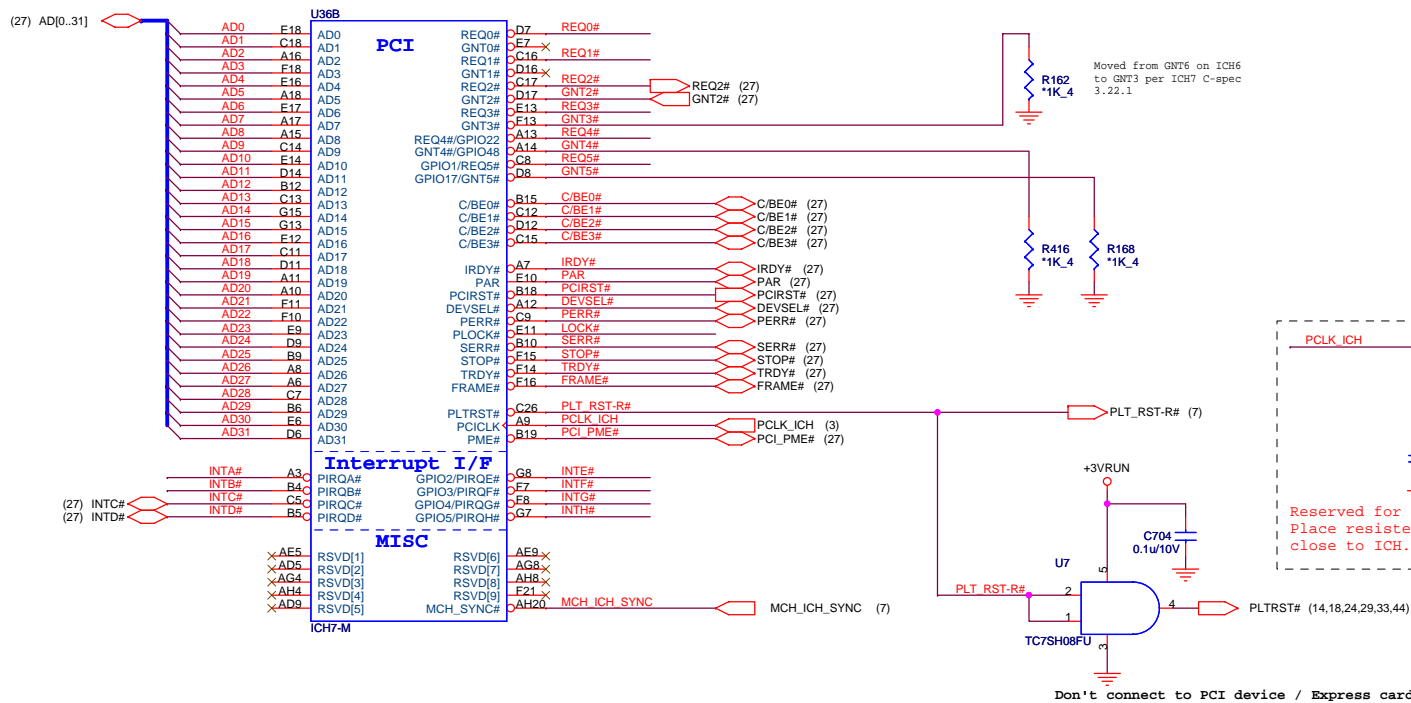
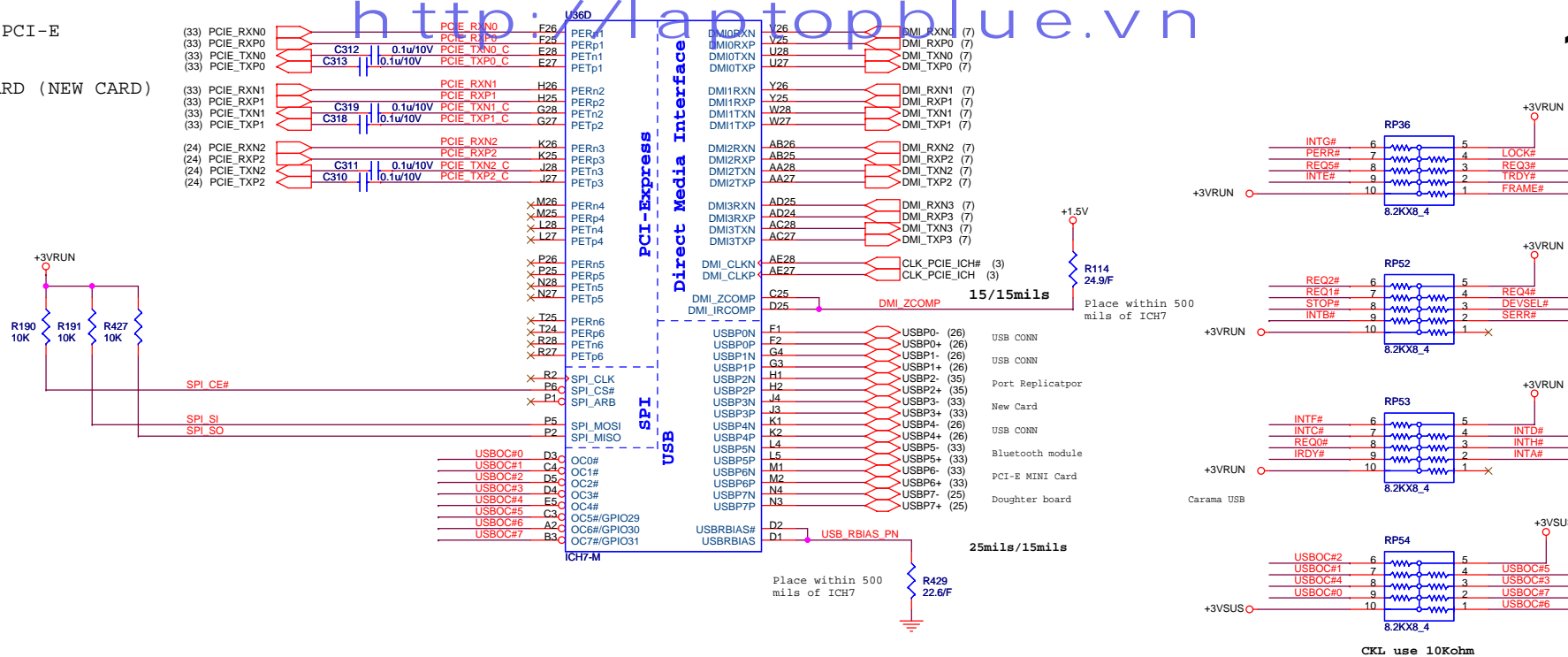












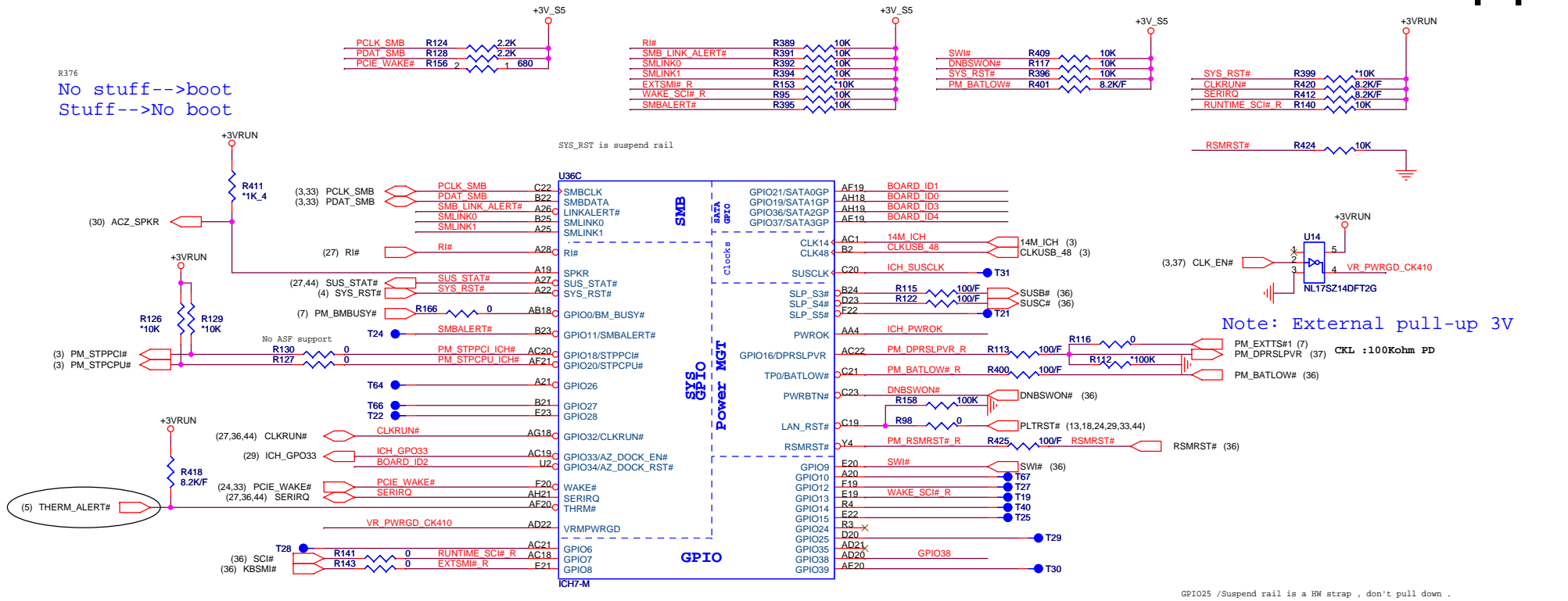
ICH7 Boot BIOS select			
	STRAP	GNT5# R1	GNT4# R2
LPC (default)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

Reserved for EMI.  
Place resistor and cap  
close to ICH.



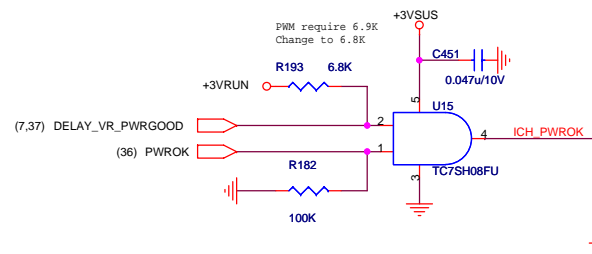
R376

No stuff-->boot  
Stuff-->No boot



Note: External pull-up 3V

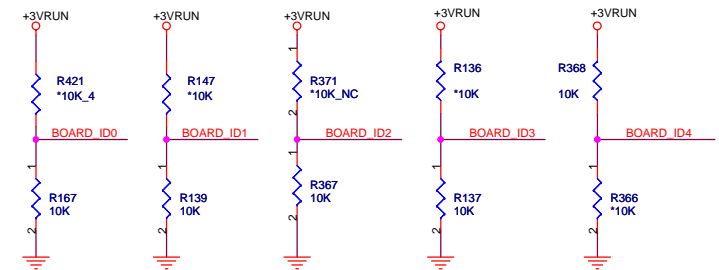
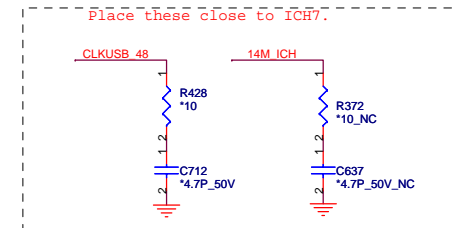
GPIO25 /Suspend rail is a HW strap , don't pull down .



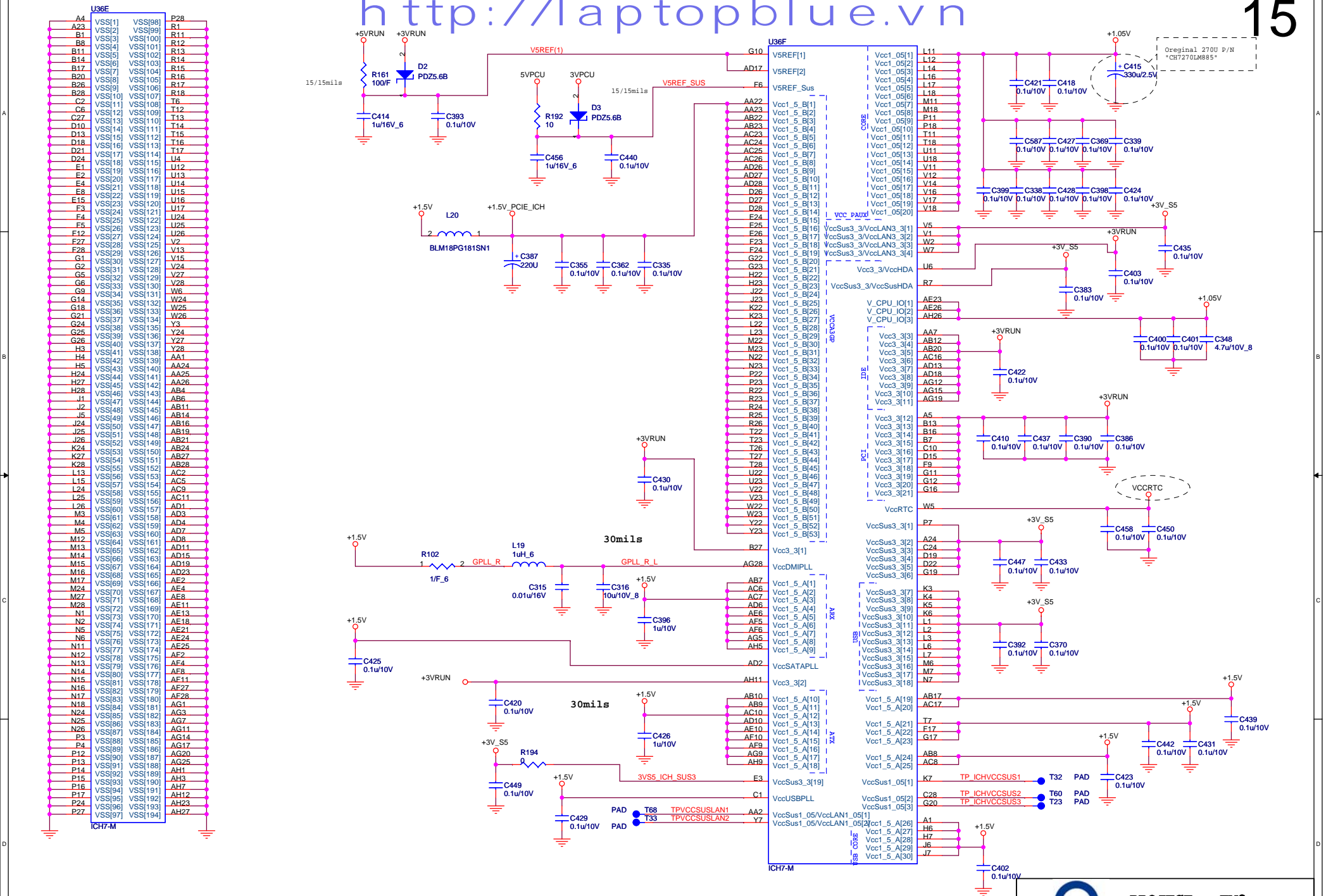
Level is incorrect !!

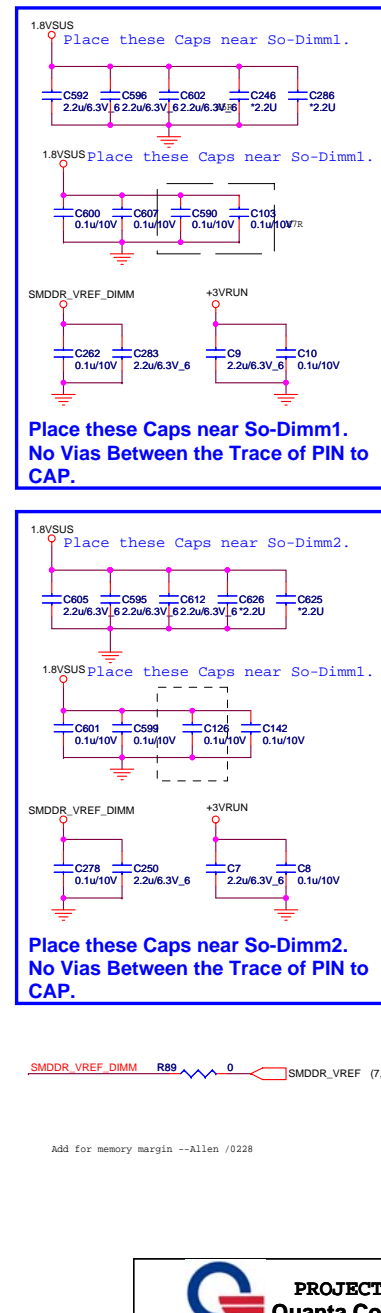
GPIO38	Function
High	CRT
Low	DVI

Board ID	Function
ID [1:0]	00: TW3 01: DW1
ID2	0: SATA HDD 1: PATA HDD
ID3	Reserve
ID4	0: No docking. 1: w/ docking



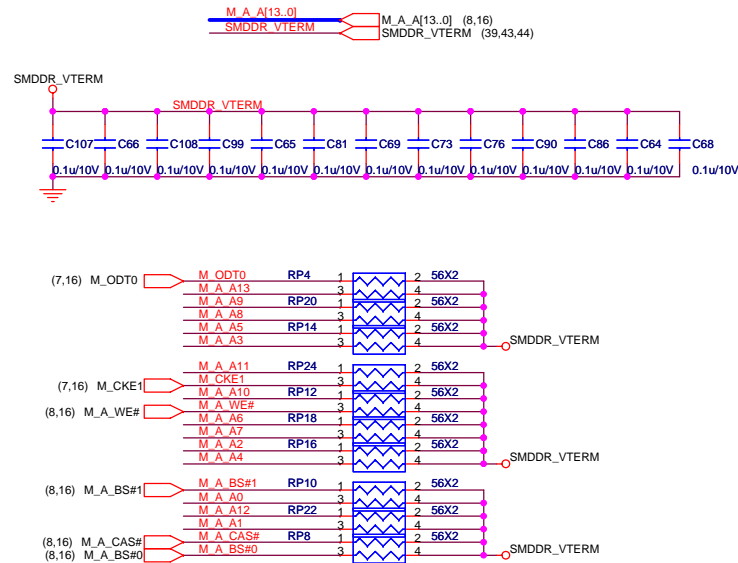




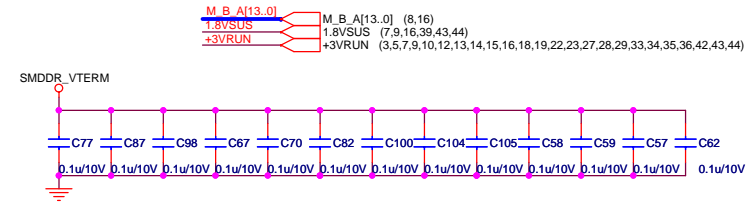


# DDRII DUAL CHANNEL A,B.

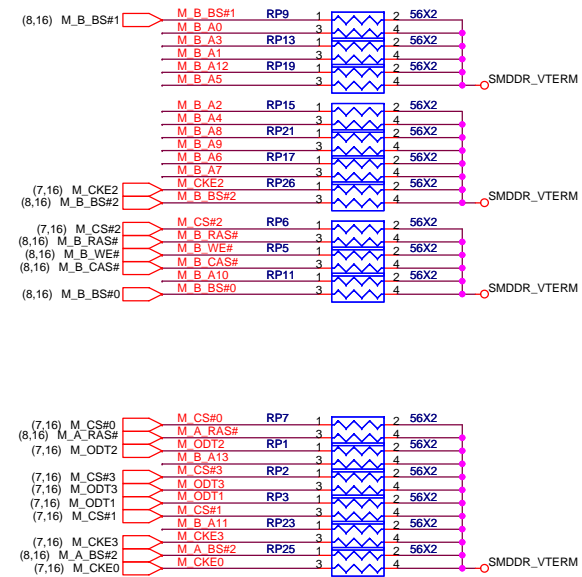
## DDRII A CHANNEL



## DDRII B CHANNEL



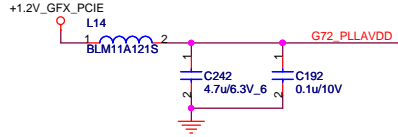
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR\_VTERM



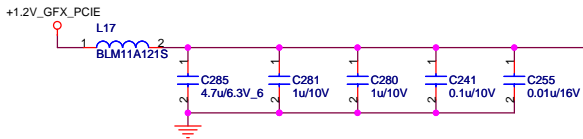
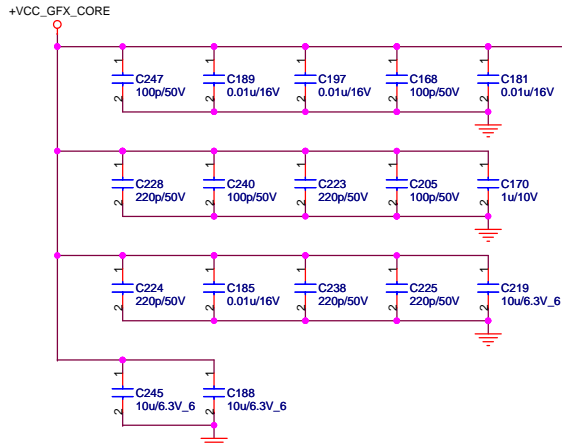
(7) PEG\_RXP[15:0]  
(7) PEG\_RXN[15:0]

(7) PEG\_TXP[15:0]  
(7) PEG\_TXN[15:0]

PEG_RXP0	0.1u/10V	1	C304	V_GMCHEXP_RXP0
PEG_RXP1	0.1u/10V	2	C656	V_GMCHEXP_RXP1
PEG_RXP2	0.1u/10V	1	C314	V_GMCHEXP_RXP2
PEG_RXP3	0.1u/10V	2	C664	V_GMCHEXP_RXP3
PEG_RXP4	0.1u/10V	2	C326	V_GMCHEXP_RXP4
PEG_RXP5	0.1u/10V	2	C684	V_GMCHEXP_RXP5
PEG_RXP6	0.1u/10V	2	C368	V_GMCHEXP_RXP6
PEG_RXP7	0.1u/10V	2	C688	V_GMCHEXP_RXP7
PEG_RXP8	0.1u/10V	2	C385	V_GMCHEXP_RXP8
PEG_RXP9	0.1u/10V	2	C690	V_GMCHEXP_RXP9
PEG_RXP10	0.1u/10V	2	C353	V_GMCHEXP_RXP10
PEG_RXP11	0.1u/10V	2	C693	V_GMCHEXP_RXP11
PEG_RXP12	0.1u/10V	2	C361	V_GMCHEXP_RXP12
PEG_RXP13	0.1u/10V	2	C696	V_GMCHEXP_RXP13
PEG_RXP14	0.1u/10V	2	C364	V_GMCHEXP_RXP14
PEG_RXP15	0.1u/10V	2	C699	V_GMCHEXP_RXP15



(3) CLK\_PCIE\_VGA  
(3) CLK\_PCIE\_VGA#



PEG_TXP0	AF1	PEG_RX0P	AD5	V_GMCHEXP_RXP0
PEG_TXN0	AG2	PEG_RX0N	AD6	V_GMCHEXP_RXN0
PEG_TXP1	AG3	PEG_RX1P	AE6	V_GMCHEXP_RXP1
PEG_TXN1	AG4	PEG_RX1N	AE7	V_GMCHEXP_RXN1
PEG_TXP2	AE4	PEG_RX2P	AD7	V_GMCHEXP_RXP2
PEG_TXN2	AE5	PEG_RX2N	AC7	V_GMCHEXP_RXN2
PEG_TXP3	AG6	PEG_RX3P	AE9	V_GMCHEXP_RXP3
PEG_TXN3	AG7	PEG_RX3N	AE10	V_GMCHEXP_RXN3
PEG_TXP4	AE7	PEG_RX4P	AD10	V_GMCHEXP_RXP4
PEG_TXN4	AE8	PEG_RX4N	AC10	V_GMCHEXP_RXN4
PEG_TXP5	AG9	PEG_RX5P	AE12	V_GMCHEXP_RXP5
PEG_TXN5	AG10	PEG_RX5N	AE13	V_GMCHEXP_RXN5
PEG_TXP6	AE10	PEG_RX6P	AD13	V_GMCHEXP_RXP6
PEG_TXN6	AE11	PEG_RX6N	AC13	V_GMCHEXP_RXN6
PEG_TXP7	AG12	PEG_RX7P	AE15	V_GMCHEXP_RXP7
PEG_TXN7	AG13	PEG_RX7N	AE16	V_GMCHEXP_RXN7
PEG_TXP8	AG15	PEG_RX8P	AC18	V_GMCHEXP_RXP8
PEG_TXN8	AG16	PEG_RX8N	AD18	V_GMCHEXP_RXN8
PEG_TXP9	AE16	PEG_RX9P	AE18	V_GMCHEXP_RXP9
PEG_TXN9	AE17	PEG_RX9N	AE19	V_GMCHEXP_RXN9
PEG_TXP10	AG18	PEG_RX10P	AD19	V_GMCHEXP_RXP10
PEG_TXN10	AG19	PEG_RX10N	AC19	V_GMCHEXP_RXN10
PEG_TXP11	AE19	PEG_RX11P	AE21	V_GMCHEXP_RXP11
PEG_TXN11	AE20	PEG_RX11N	AD21	V_GMCHEXP_RXN11
PEG_TXP12	AG21	PEG_RX12P	AE22	V_GMCHEXP_RXP12
PEG_TXN12	AG22	PEG_RX12N	AD22	V_GMCHEXP_RXP13
PEG_TXP13	AE22	PEG_RX13P	AD23	V_GMCHEXP_RXN13
PEG_TXN13	AE23	PEG_RX13N	AE25	V_GMCHEXP_RXP14
PEG_TXP14	AG24	PEG_RX14P	AE26	V_GMCHEXP_RXN14
PEG_TXN14	AG25	PEG_RX14N	AE24	V_GMCHEXP_RXP15
PEG_TXP15	AG26	PEG_RX15P	AD24	V_GMCHEXP_RXN15
PEG_TXN15	AE27	PEG_RX15N		

P  
C  
I  
-  
E  
X  
P  
R  
E  
S  
S  
  
I  
N  
T  
E  
R  
F  
A  
C  
E

PEX\_RST#  
PEX\_TSTCLK\_OUT#  
PEX\_TSTCLK\_OUT#

PEX\_I0VDD0\_01  
PEX\_I0VDD0\_02  
PEX\_I0VDD0\_03  
PEX\_I0VDD0\_04  
PEX\_I0VDD0\_05  
PEX\_I0VDD0\_06  
PEX\_I0VDD0\_07  
PEX\_I0VDD0\_08

PEX\_I0VDDQ\_01  
PEX\_I0VDDQ\_02  
PEX\_I0VDDQ\_03  
PEX\_I0VDDQ\_04  
PEX\_I0VDDQ\_05  
PEX\_I0VDDQ\_06  
PEX\_I0VDDQ\_07  
PEX\_I0VDDQ\_08  
PEX\_I0VDDQ\_09  
PEX\_I0VDDQ\_10  
PEX\_I0VDDQ\_11  
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VDD\_LP\_01  
VDD\_LP\_02  
VDD\_LP\_03  
VDD\_LP\_04

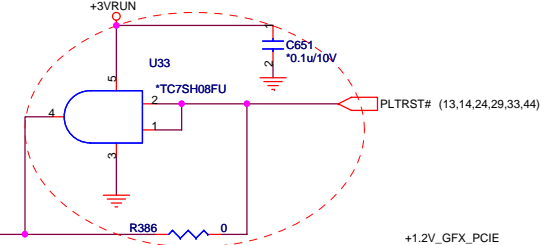
VDD33\_01  
VDD33\_02  
VDD33\_03  
VDD33\_04  
VDD33\_05  
VDD33\_06

NC\_01  
NC\_02  
NC\_03  
NC\_04

PEX\_PLLAVDD  
PEX\_PLLDVDD  
PEX\_PLLGND

G72M

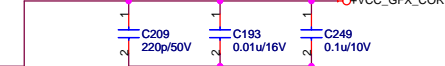
PEG_RXN0	0.1u/10V	2	C309	V_GMCHEXP_RXN0
PEG_RXN1	0.1u/10V	2	C657	V_GMCHEXP_RXN1
PEG_RXN2	0.1u/10V	2	C323	V_GMCHEXP_RXN2
PEG_RXN3	0.1u/10V	2	C663	V_GMCHEXP_RXN3
PEG_RXN4	0.1u/10V	2	C332	V_GMCHEXP_RXN4
PEG_RXN5	0.1u/10V	2	C685	V_GMCHEXP_RXN5
PEG_RXN6	0.1u/10V	2	C367	V_GMCHEXP_RXN6
PEG_RXN7	0.1u/10V	2	C687	V_GMCHEXP_RXN7
PEG_RXN8	0.1u/10V	2	C384	V_GMCHEXP_RXN8
PEG_RXN9	0.1u/10V	2	C689	V_GMCHEXP_RXN9
PEG_RXN10	0.1u/10V	2	C352	V_GMCHEXP_RXN10
PEG_RXN11	0.1u/10V	2	C692	V_GMCHEXP_RXN11
PEG_RXN12	0.1u/10V	2	C360	V_GMCHEXP_RXN12
PEG_RXN13	0.1u/10V	2	C695	V_GMCHEXP_RXN13
PEG_RXN14	0.1u/10V	2	C363	V_GMCHEXP_RXN14
PEG_RXN15	0.1u/10V	2	C698	V_GMCHEXP_RXN15



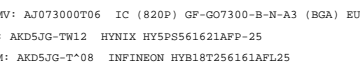
PLACE NEAR BALLS

PLACE NEAR GPU

PLACE NEAR BALLS



PLACE NEAR BALLS



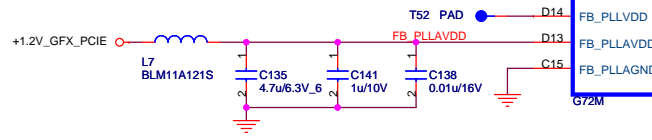
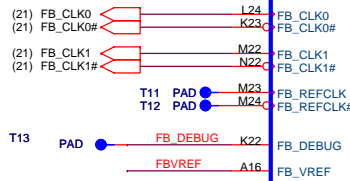
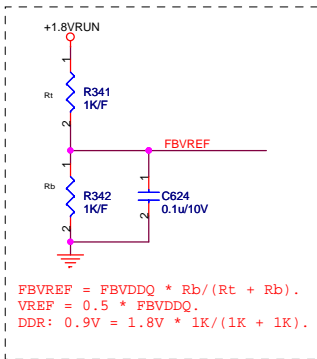
SLAVE ADDRESS: 90

FB\_CMD[0..26] (21)  
FBD[0..63] (21)  
FBDQM[0..7] (21)  
FBDQS[0..7] (21)

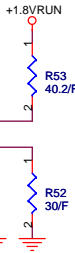
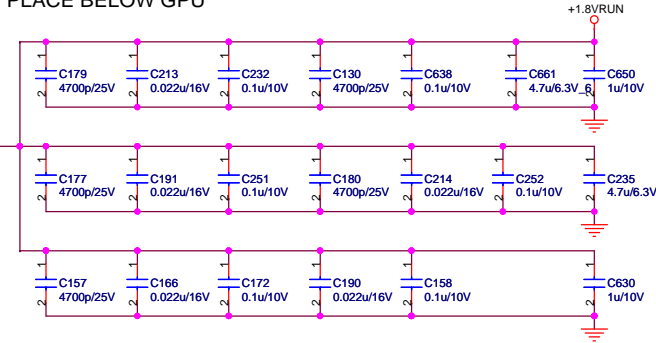
http://laptopblue.vn

20

MEMORY INTERFACE



PLACE BELOW GPU



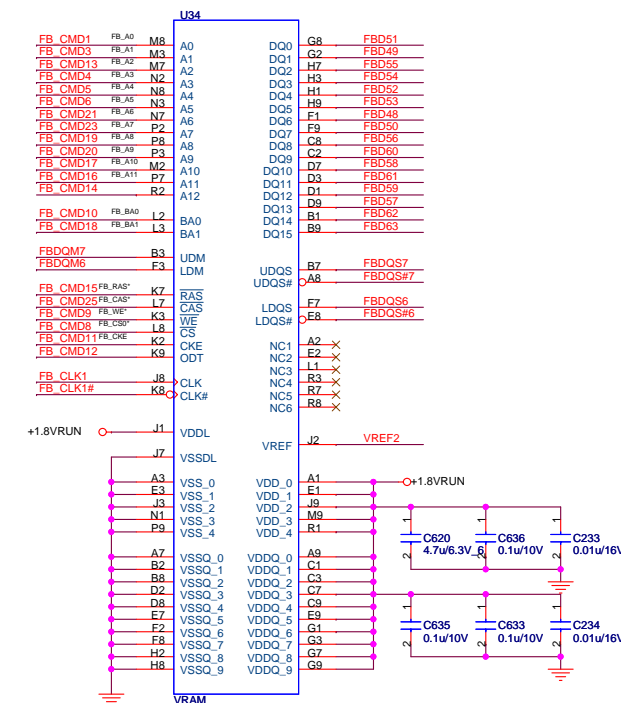
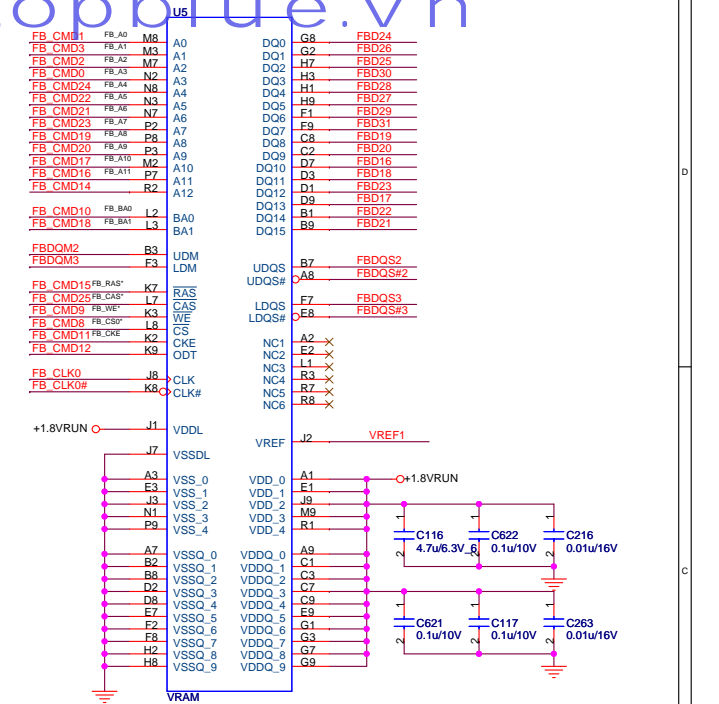
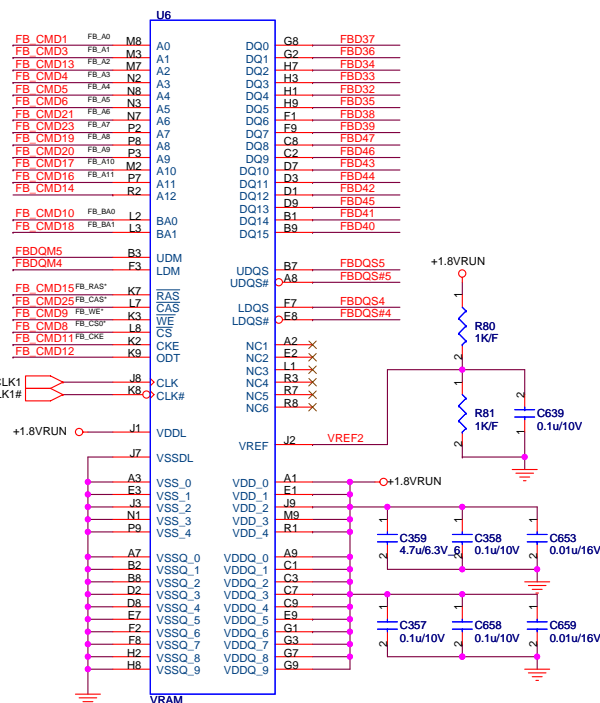
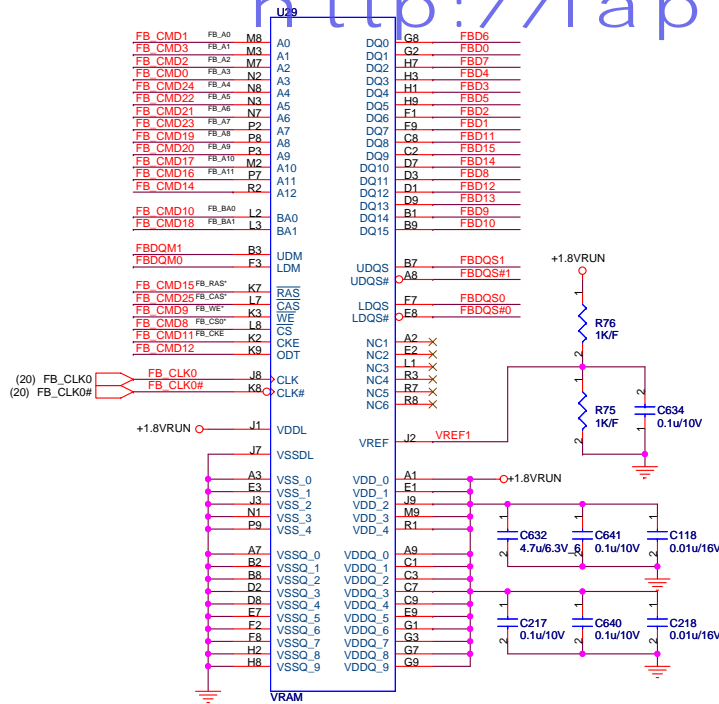
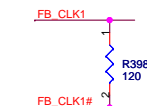
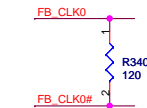
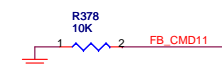
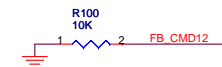
PROJECT : TW3  
Quanta Computer Inc.

Size Document Number NV72M-3 Rev 3A

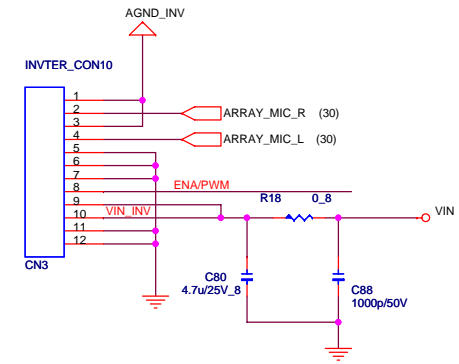
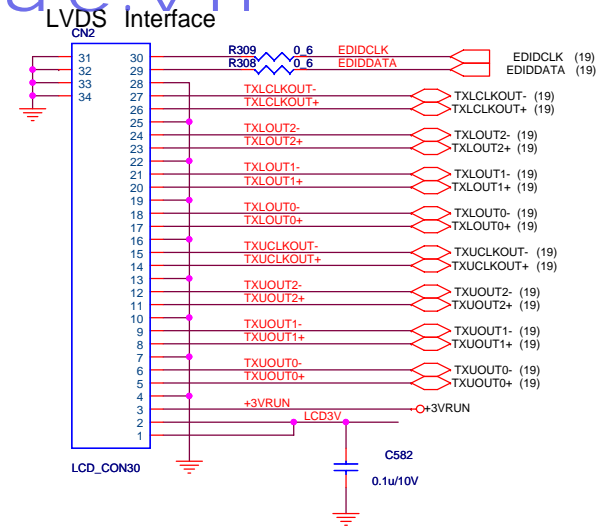
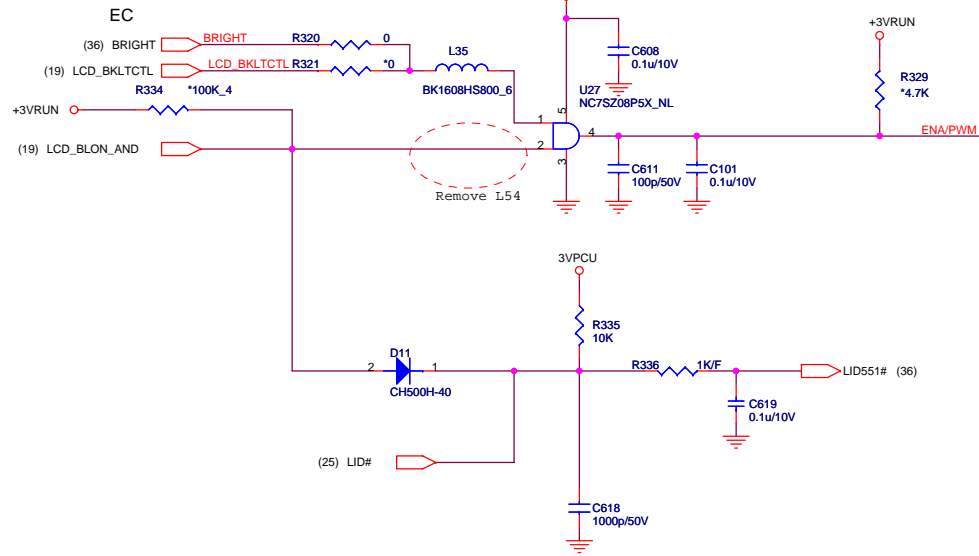
Date: Thursday, June 15, 2006 Sheet 20 of 48



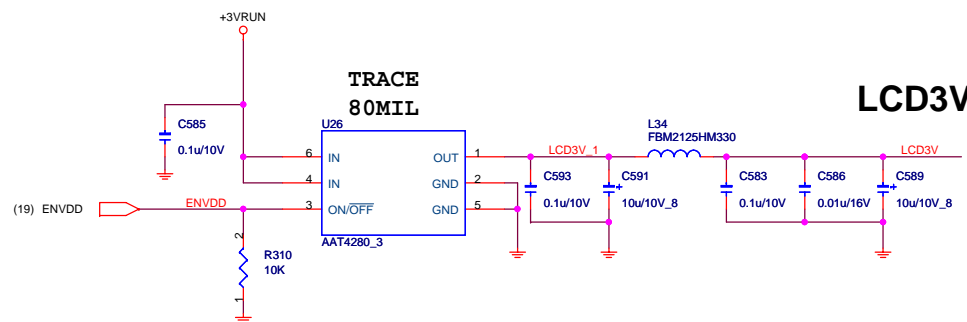
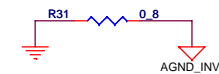
FB\_CMD0[0..26] (20)  
FBD[0..63] (20)  
FBDQM[0..7] (20)  
FBDQS[0..7] (20)  
FBDQS# [0..7] (20)



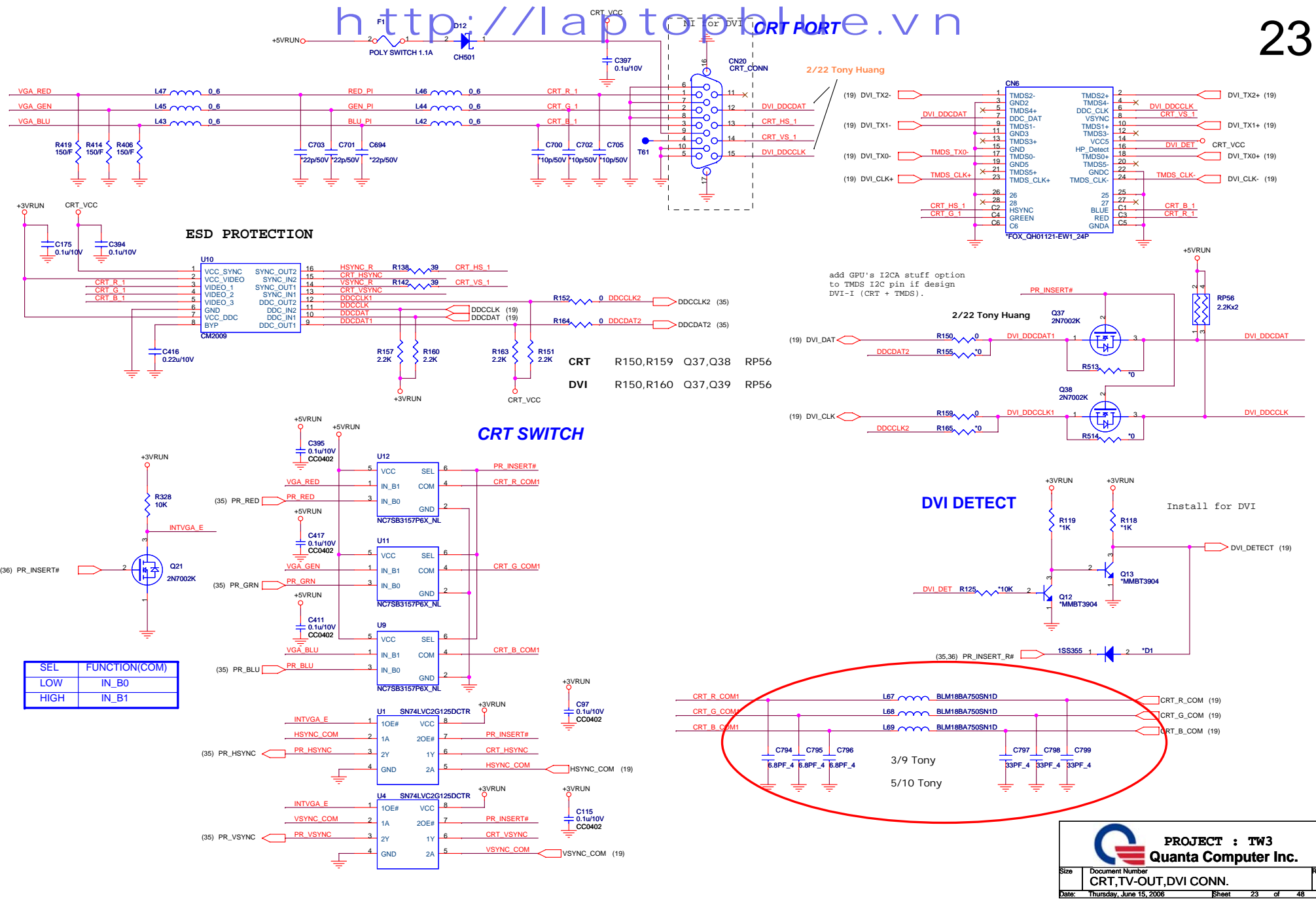




Inverter Interface



LCD3V



1Mbits

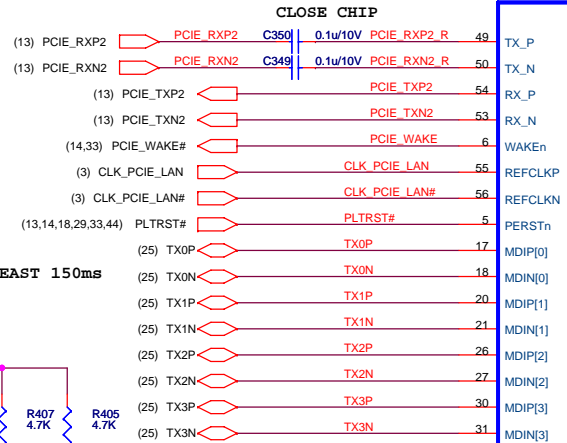
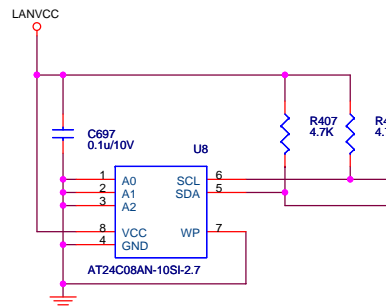
C: Add 9 X GND Pad for LAN controller.  
(20050411)

C: Add these GND pin for via hole to GND Plane.

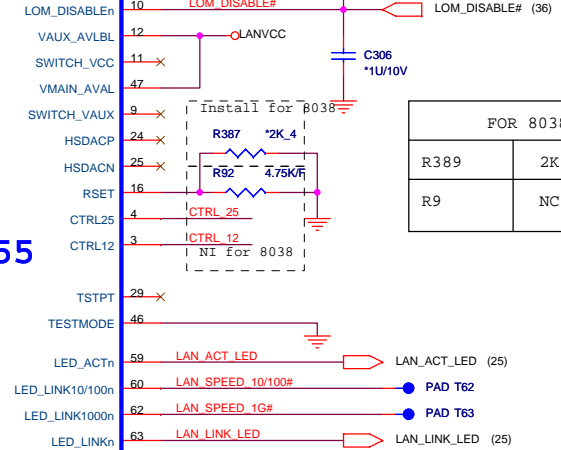
C: Add RC (R37 change to 200K, Add C101) delay to  
control LOM\_DISABLE#. (20050411)

C: Reserve R36. Change  
LANRST# to PCIRST# source  
from MB option  
modify. (2005/04/11)

DELAY PIN10 AT LEAST 150ms

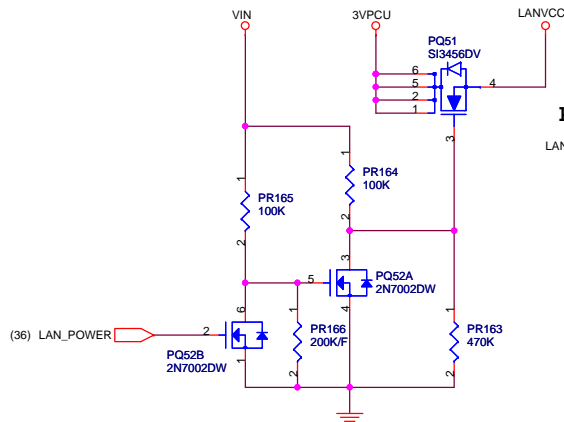


88E8038/88E8055

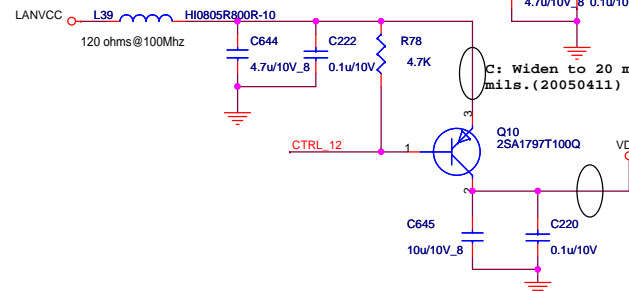


FOR 8038	
R389	2K
R9	NC

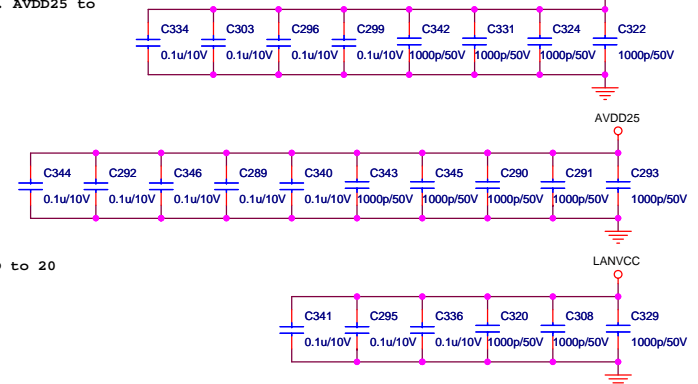
LANVCC

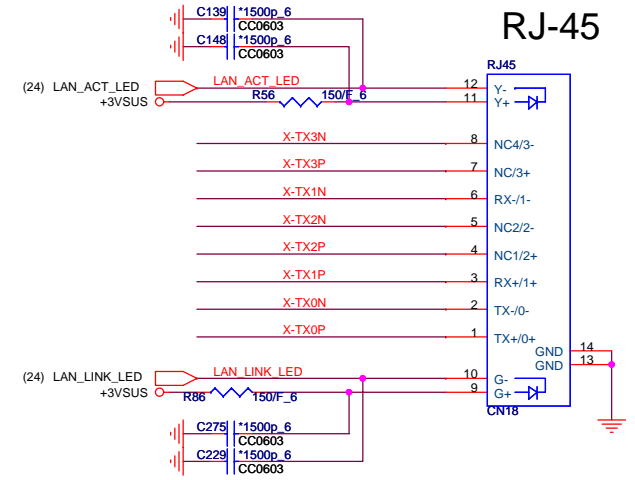
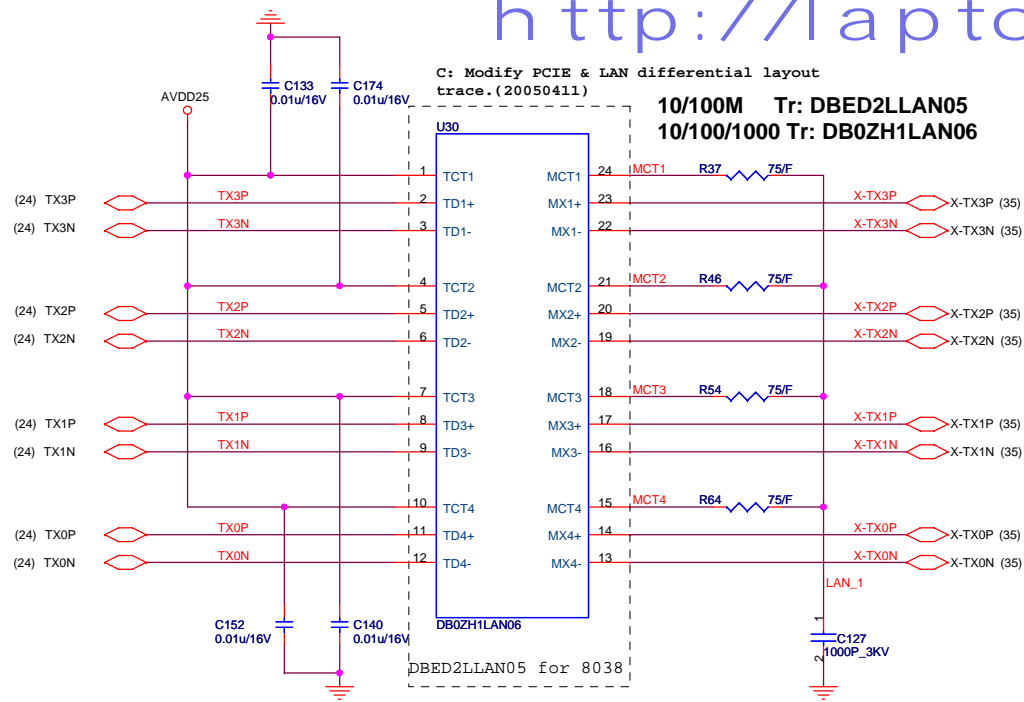


PLACEMENT CLOSE TO EACH OTHER

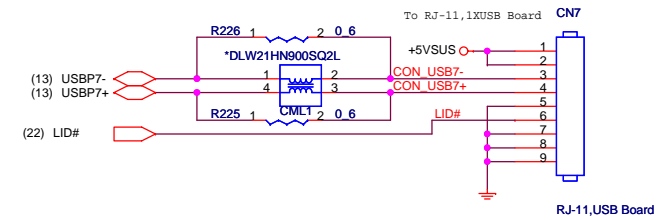
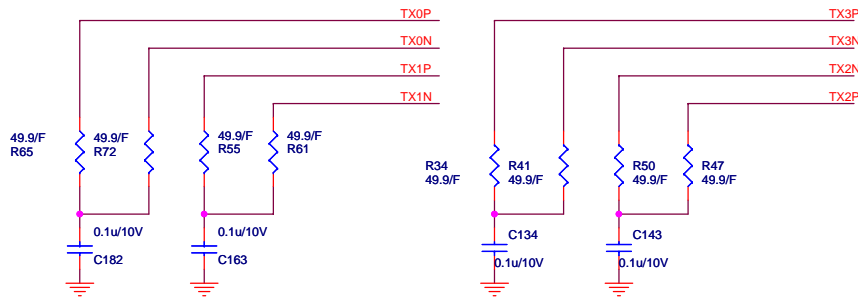


0804 REDUCING THE LANVCC NOISE



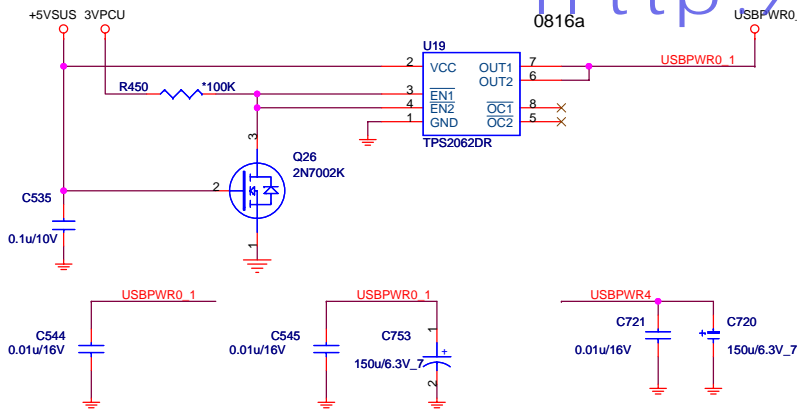


GigaLAN transformer

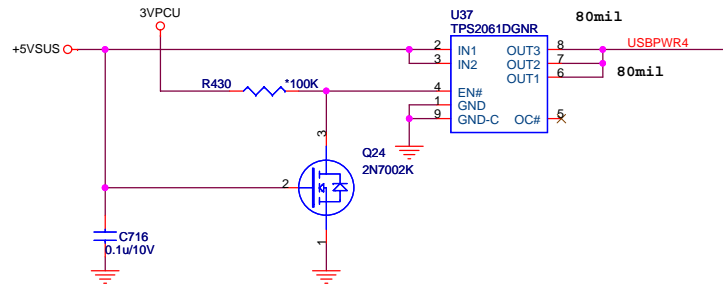


**PROJECT : TW3**  
**Quanta Computer Inc.**

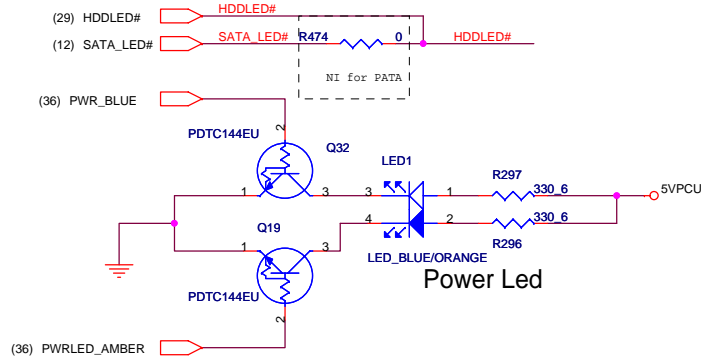
Size	Document Number	Rev
	LAN SW CONN& MDC CONN	3A
Date:	Thursday, June 15, 2006	Sheet 25 of 48



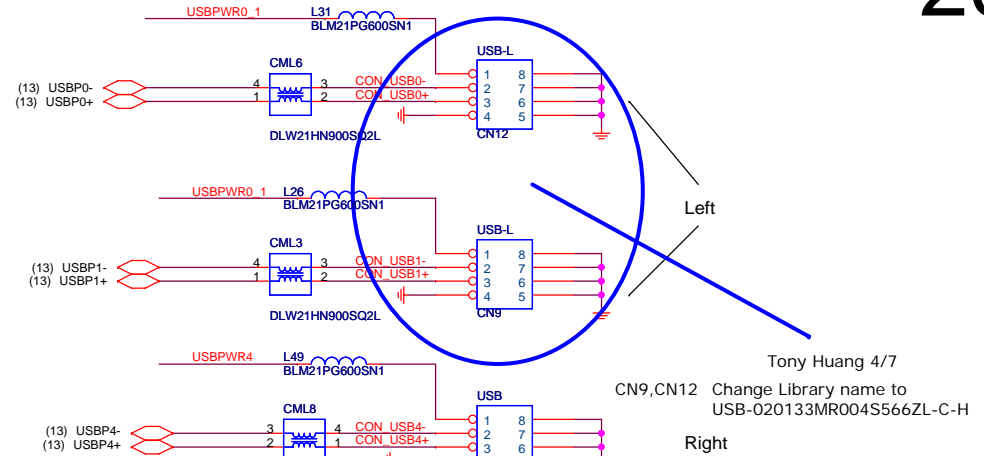
C:Change U1 from G528 to TPS2061



### HDD,SATA Led

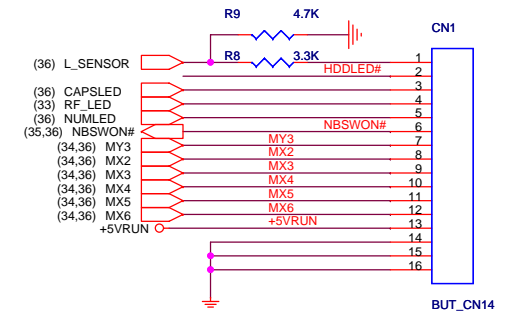
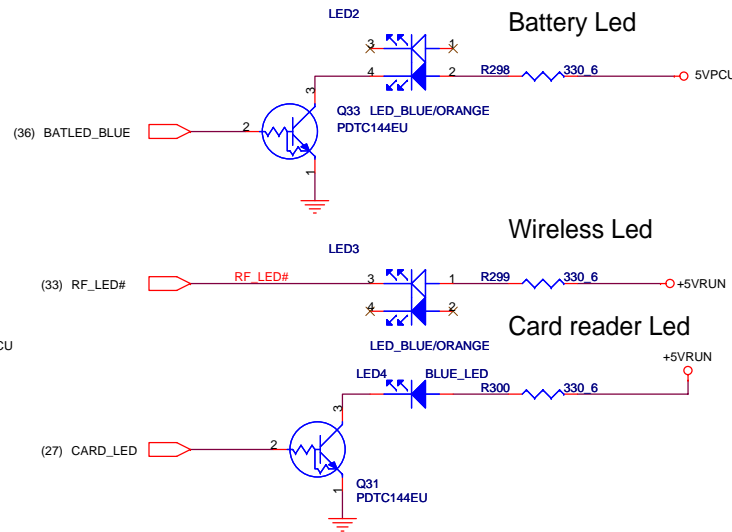


### Power Led

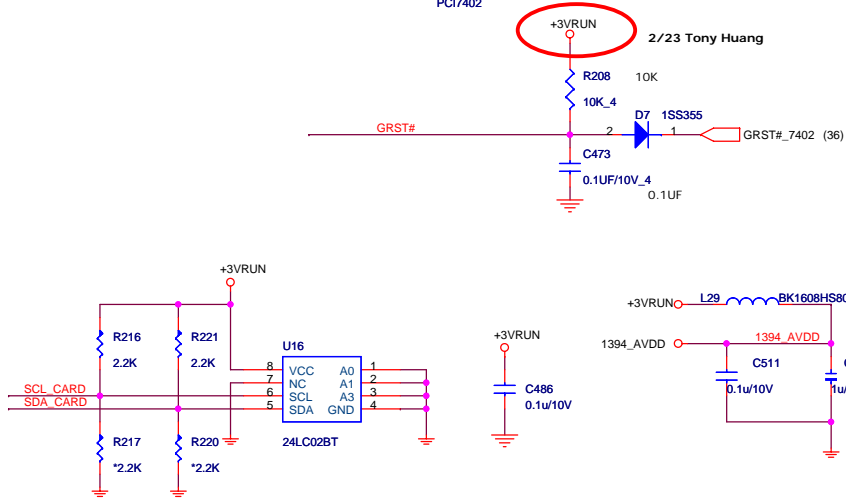
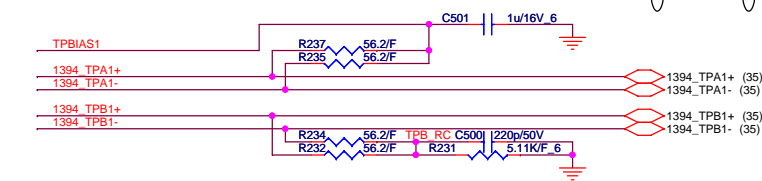
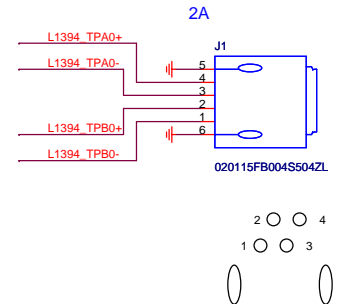
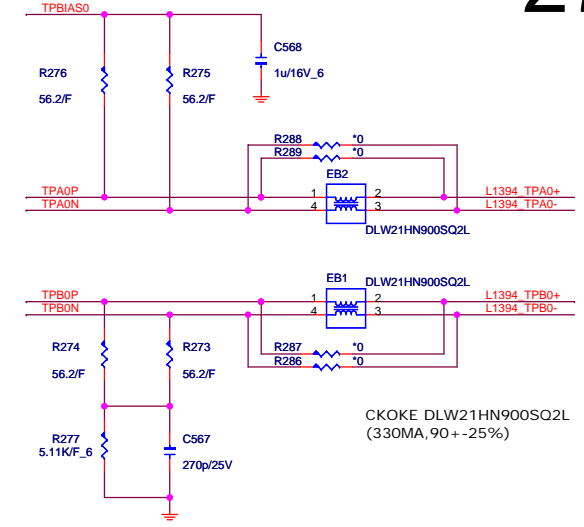
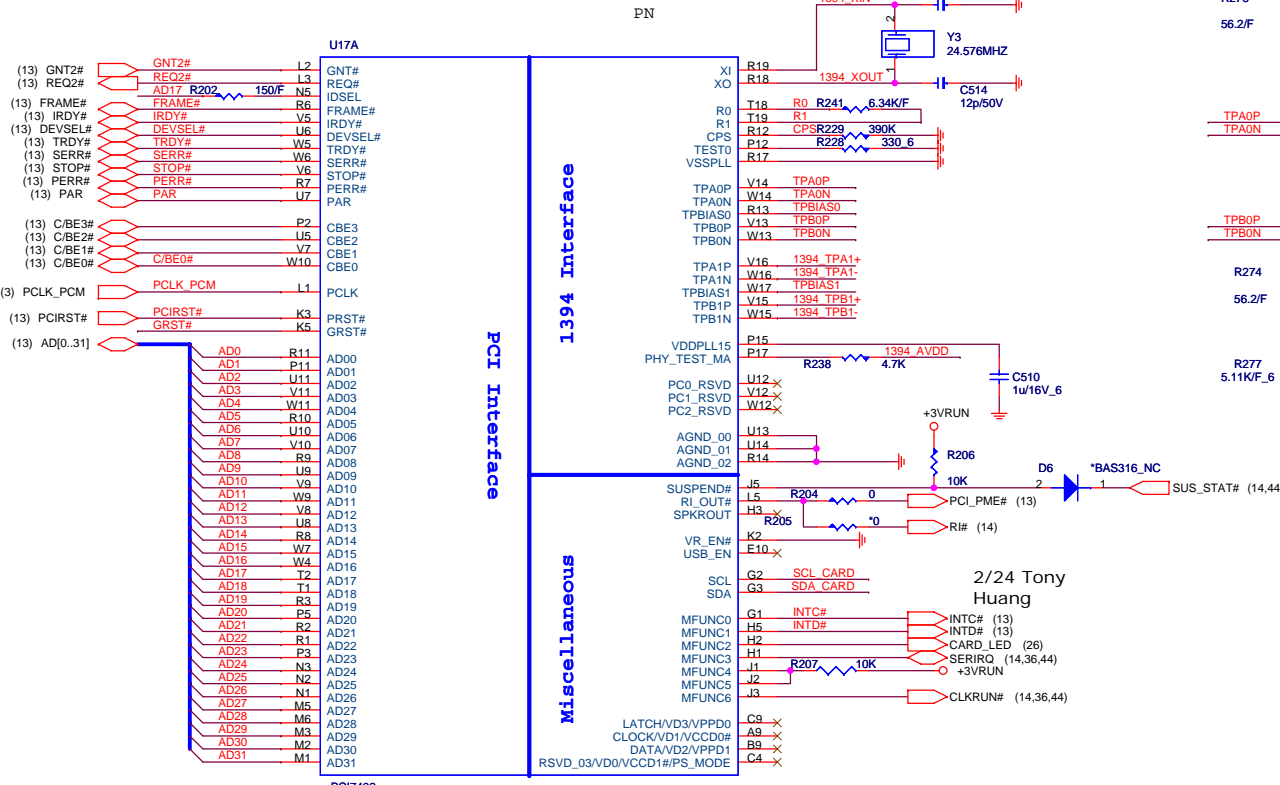


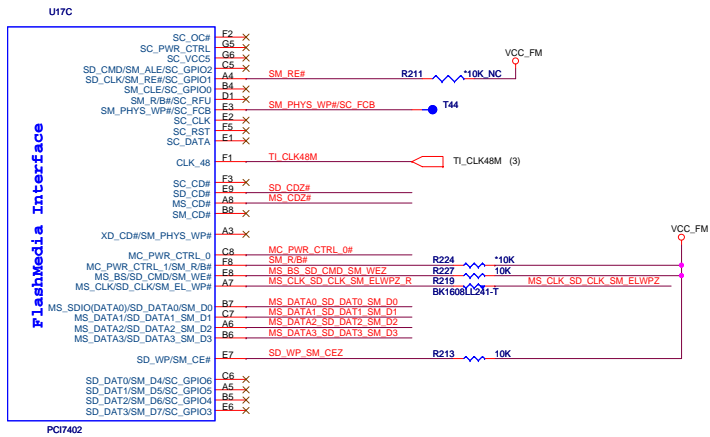
Tony Huang 4/7  
CN9,CN12 Change Library name to  
USB-020133MR004S566ZL-C-H

### For Bottom Board

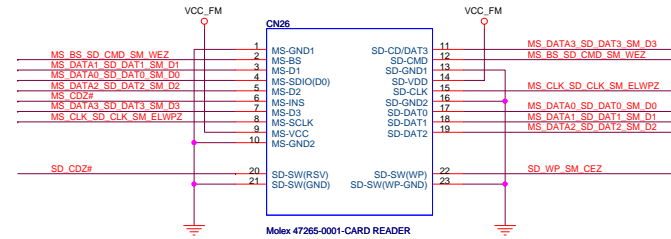


<b>PROJECT : TW3</b> <b>Quanta Computer Inc.</b>		
Size	Document Number	Rev
	USB_LED,Bottom/B	3B
Date:	Thursday, June 15, 2006	Sheet 26 of 48

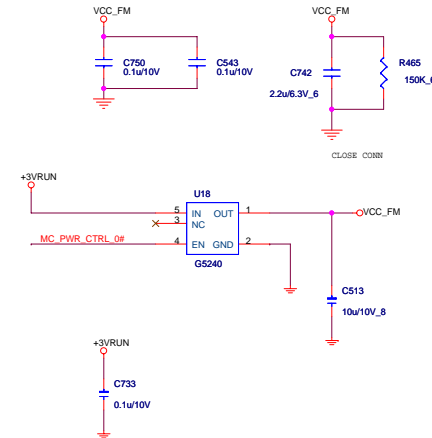
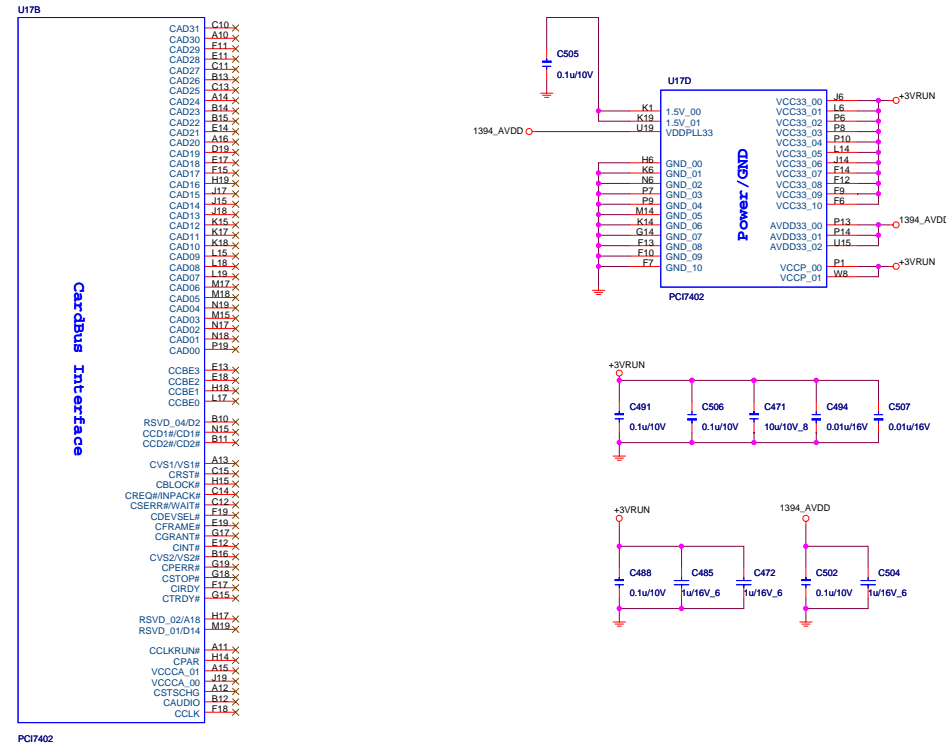




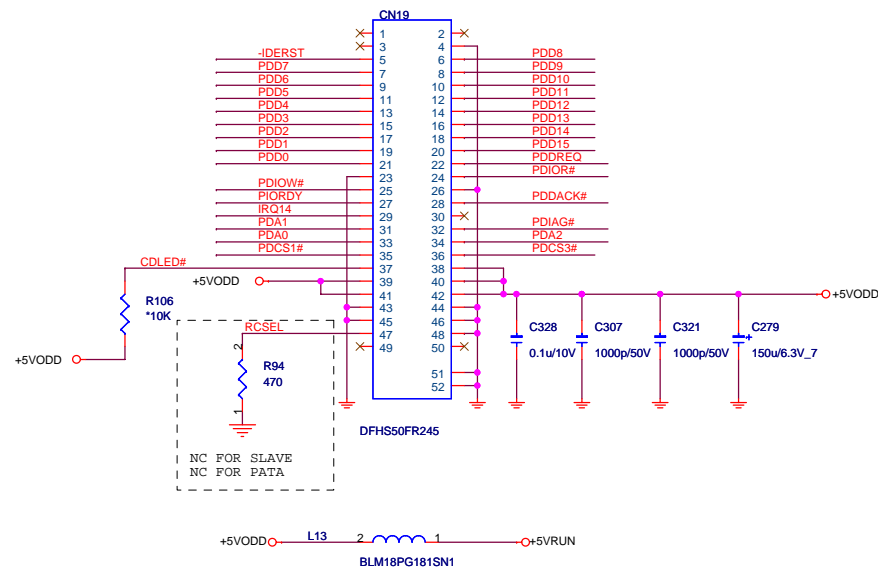
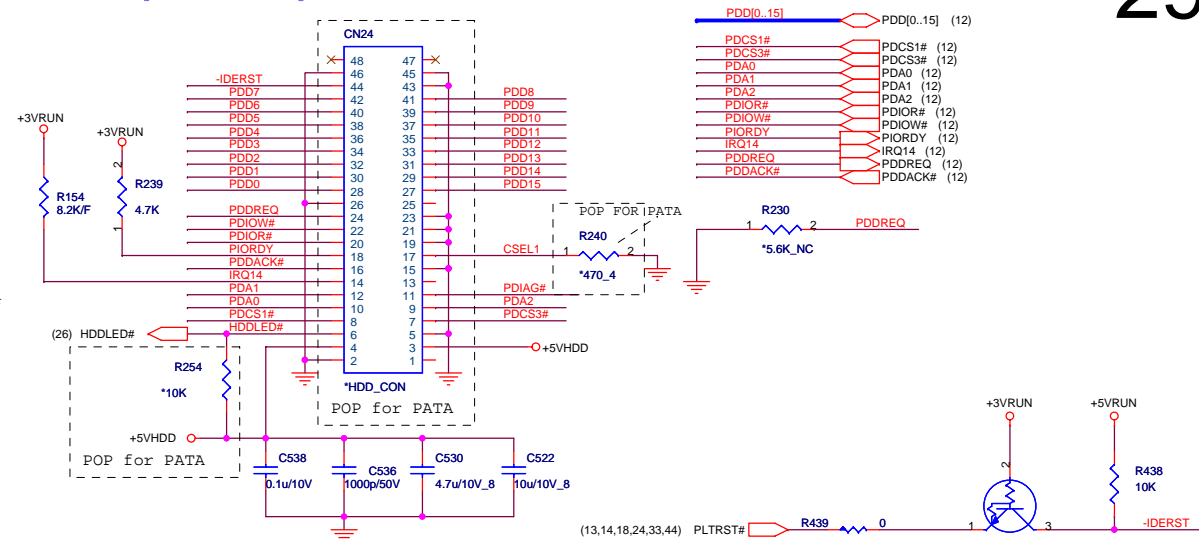
### 3 IN1 CARD READER (push-push)



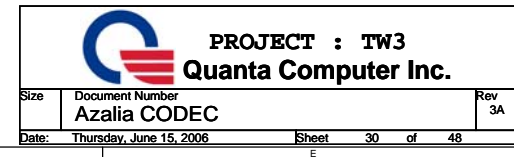
Supporting MMC/SD/MS Cards  
Molex P/N: DFHD23MS0B6

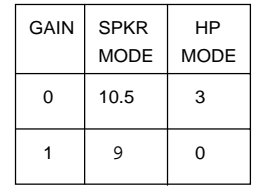







CN19	NI
C730	NI
C729	NI
CN18	HDD CON
R517	NI
Q25	2N7002
Q26	2N7002
R513	10K
R512	0
R168	470





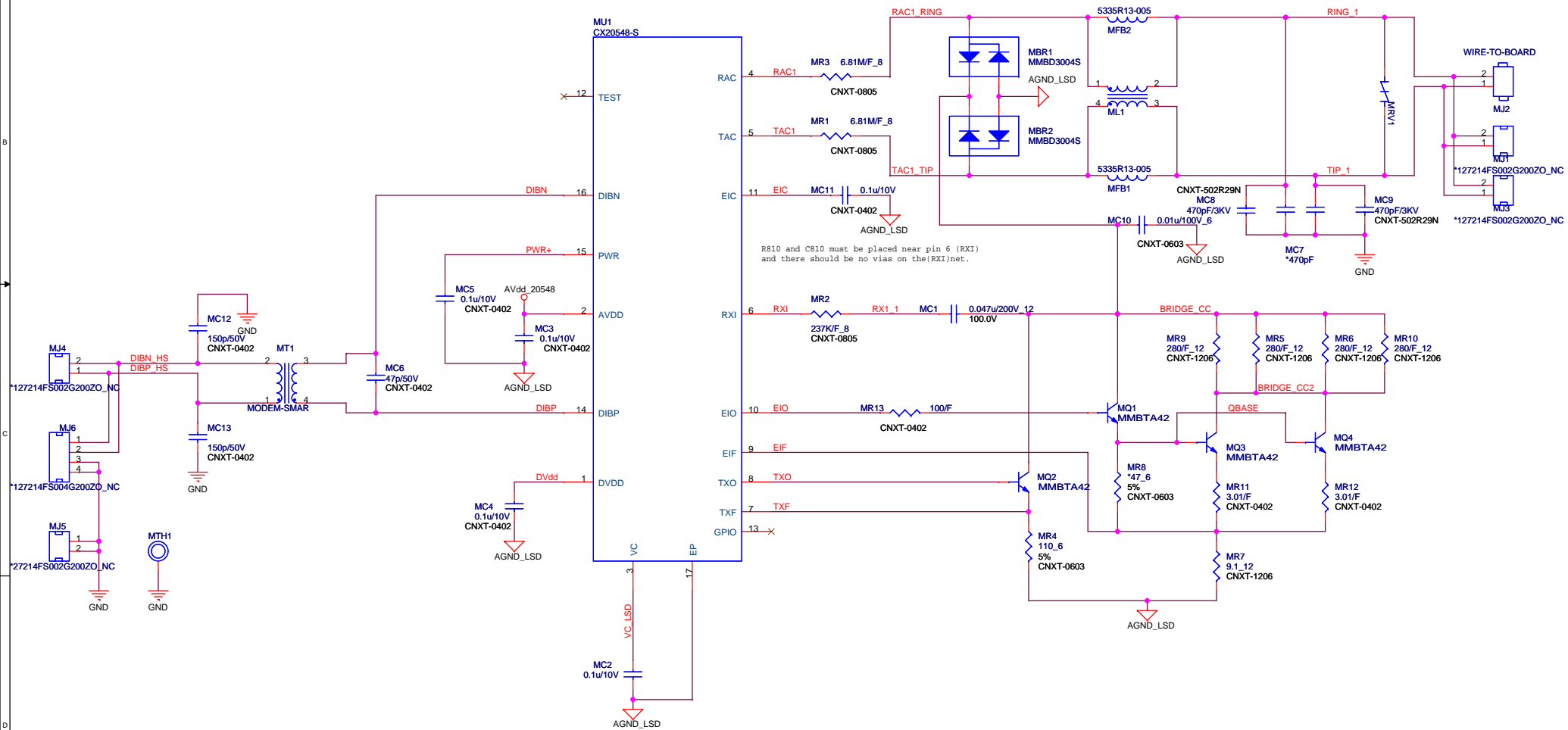
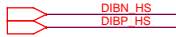
		<b>PROJECT : TW3</b> <b>Quanta Computer Inc.</b>	
Size	Document Number	Rev	
	<b>AUDIO AMPLIFIER</b>	<b>3A</b>	
Date:	Thursday, June 15, 2006	Sheet	31 of 48

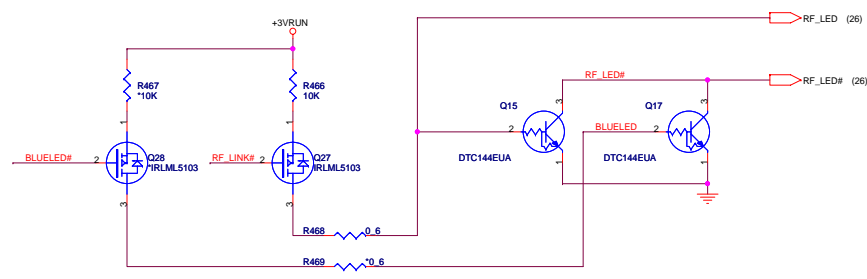
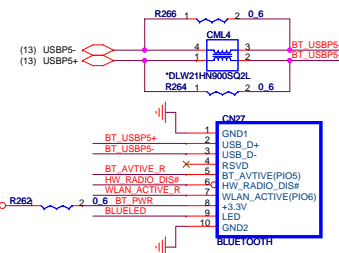
Revision History		
REV	Description	Date
0	Initial Release	April 26, 2005

http://laptopblue.vn

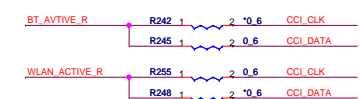
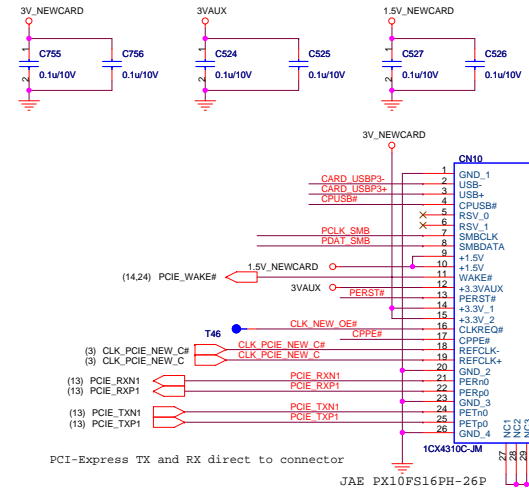
32

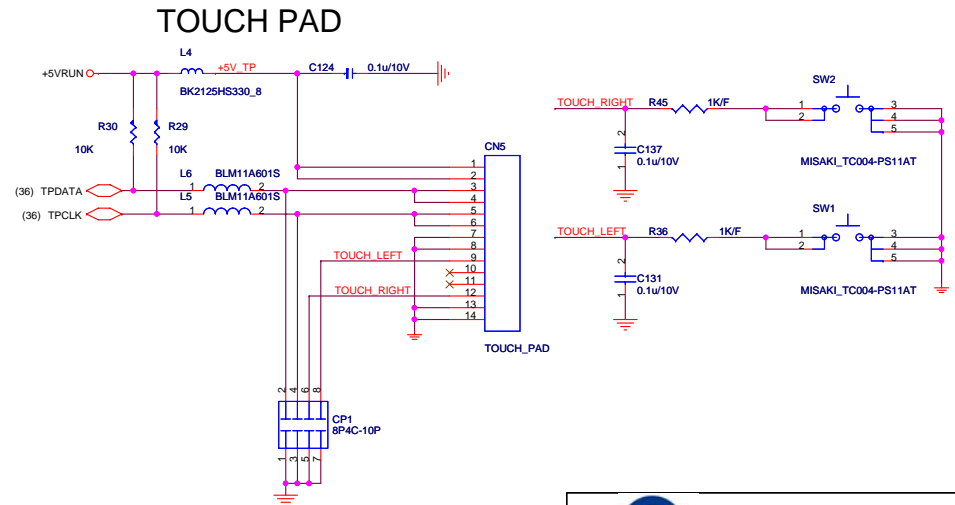
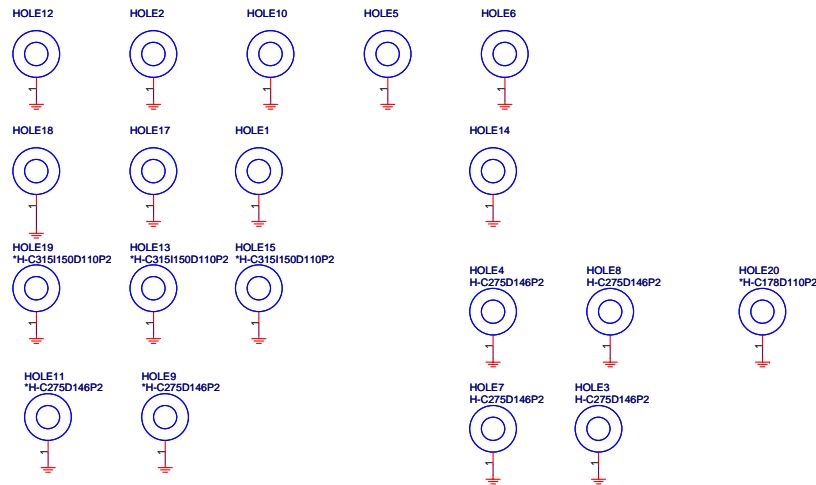
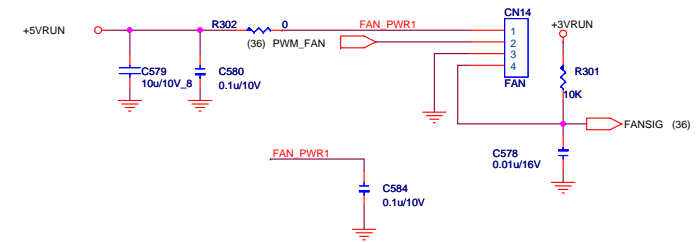
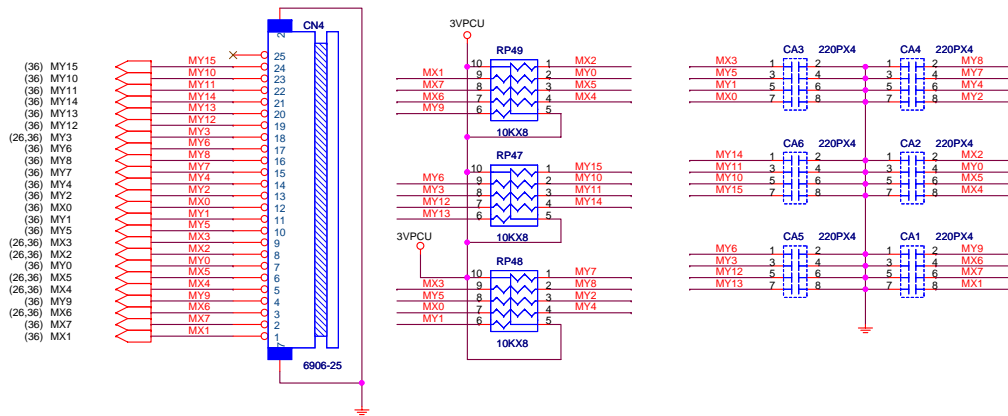
(30) DIBN\_HS  
(30) DIBP\_HS

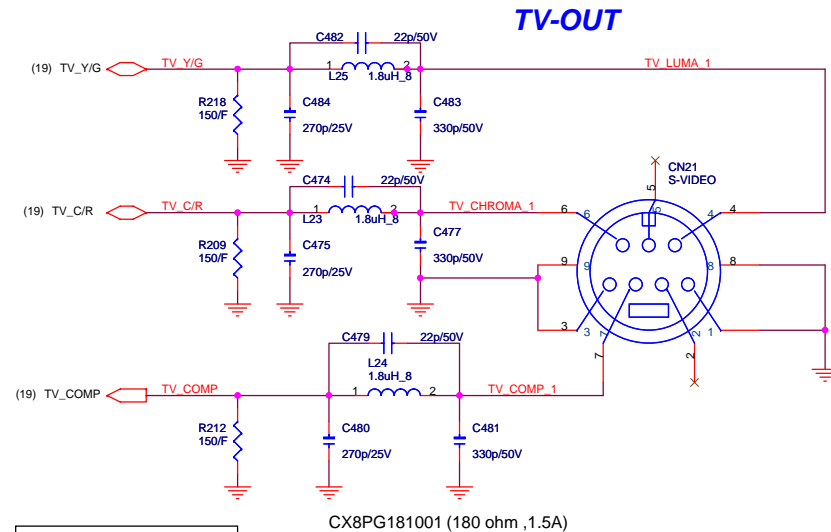
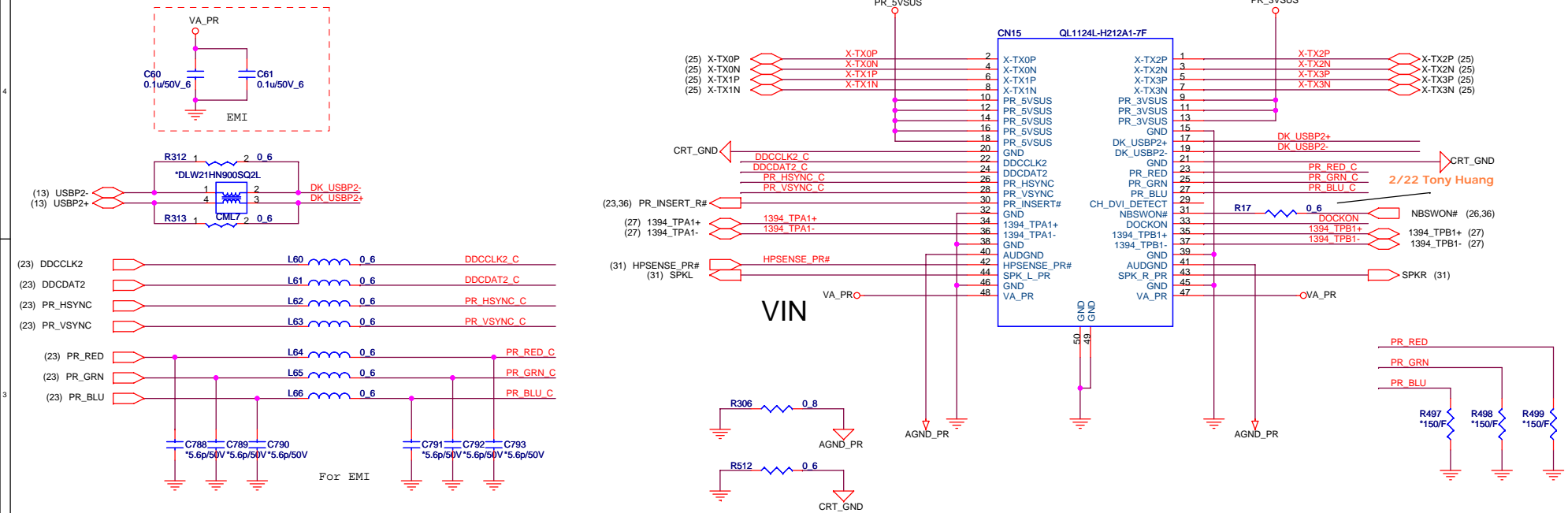




The diagram shows the connection of USB3+ and USB3- signals to the CML5 pin of the UTLN21H90S02L component. The component has pins labeled R267, CML5, R265, and UTLN21H90S02L. The USB3+ signal is connected to pin R267 (pin 1) and the USB3- signal is connected to pin R265 (pin 1). Both signals are also connected to the CML5 pin (pin 4). The component is connected to a +3V/RUN supply.







CX8PG181001 (180 ohm, 1.5A)

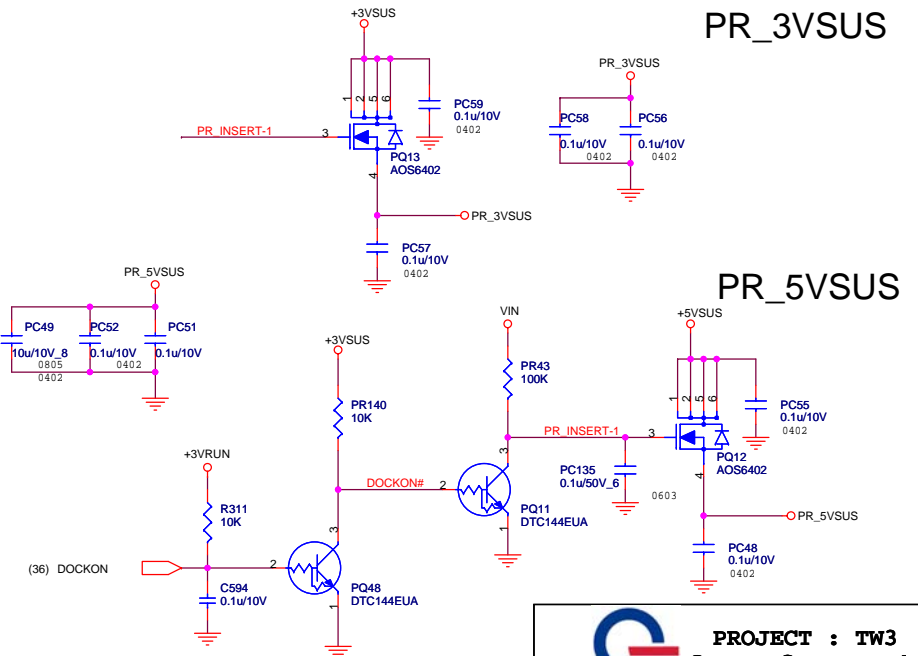
CH00606TB04 CH00606TB04

Intel CRB

150 ohm @ 100MHz  
(100mA)

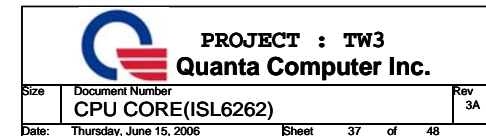
6pf  
16V

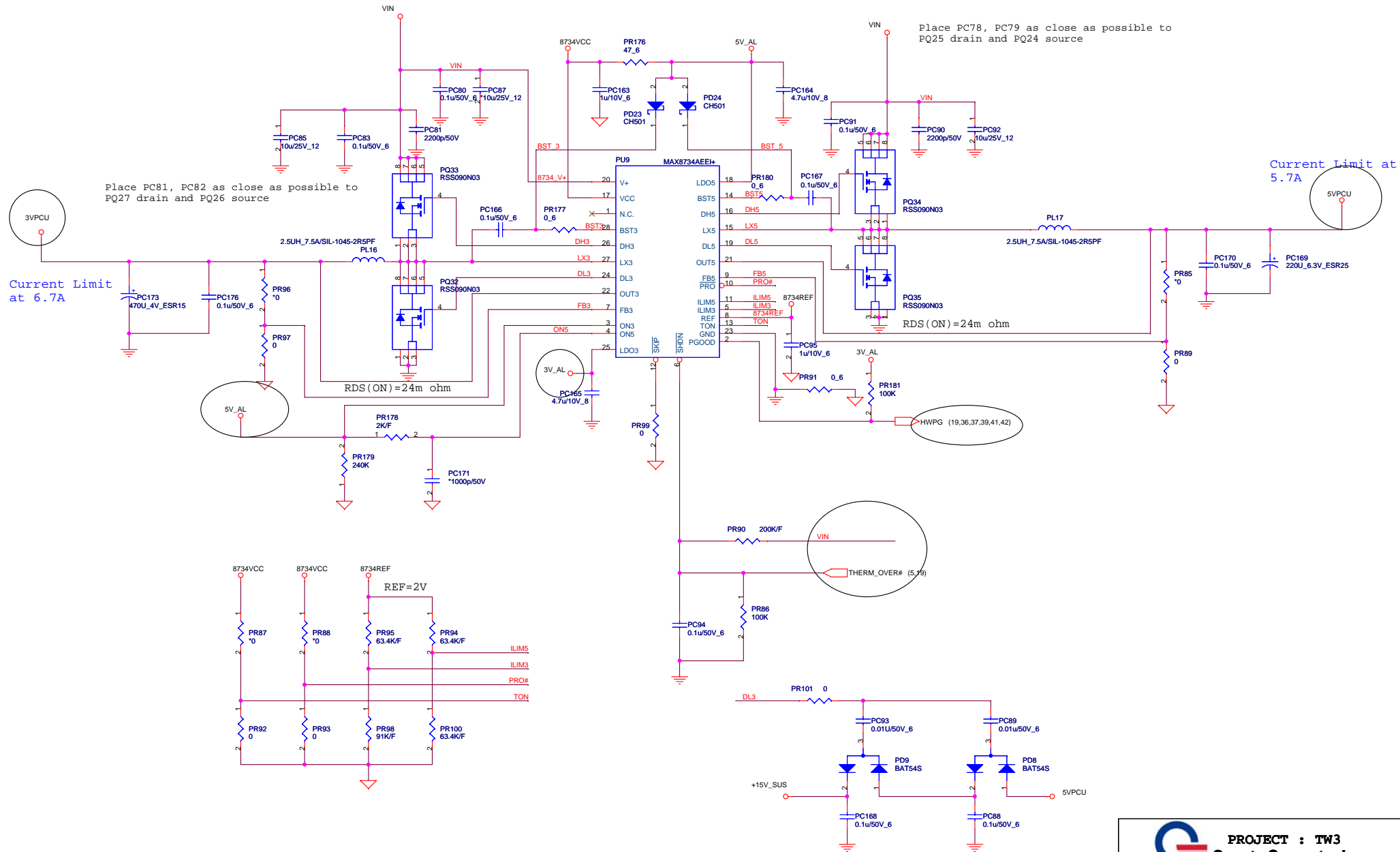
6pf  
16V

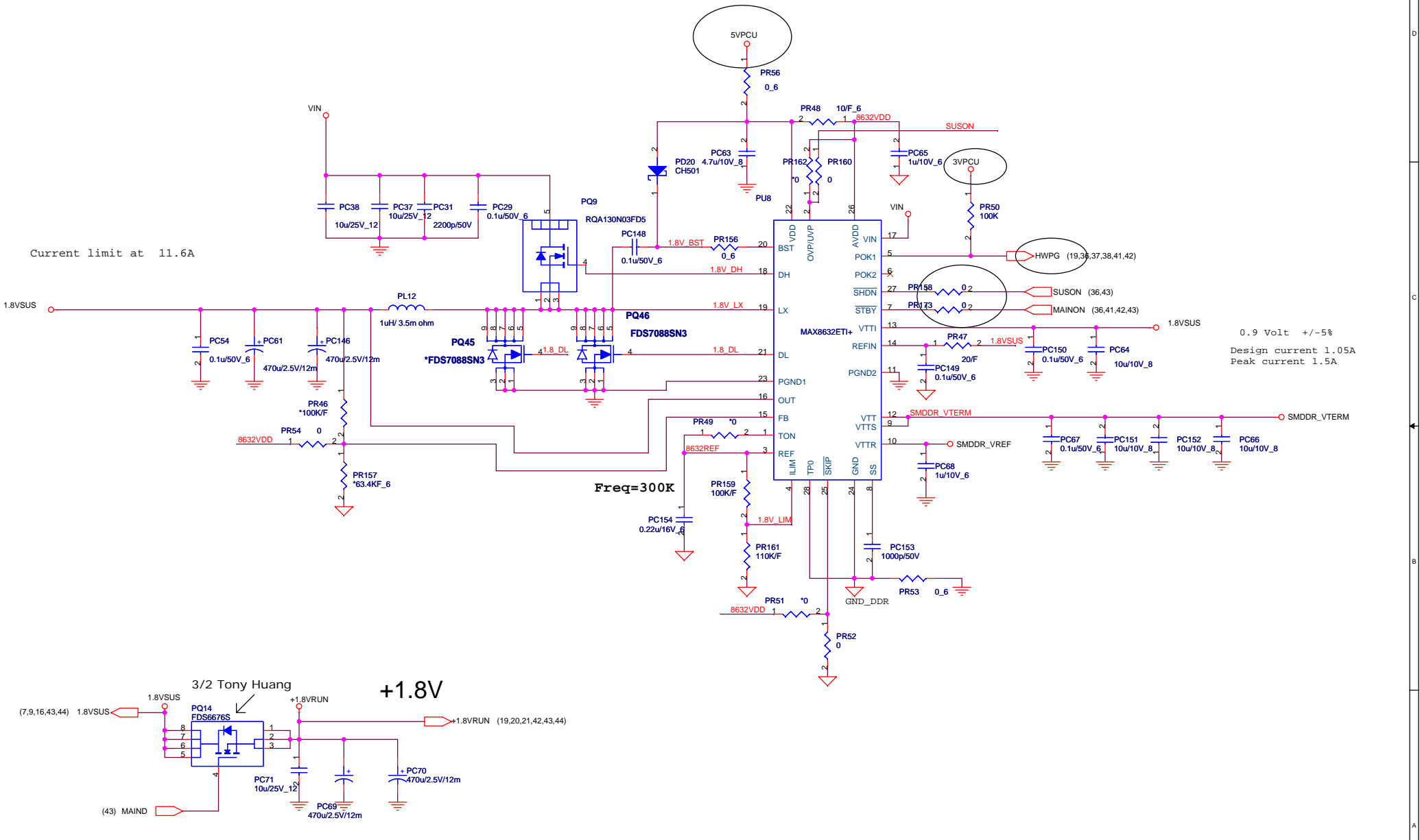


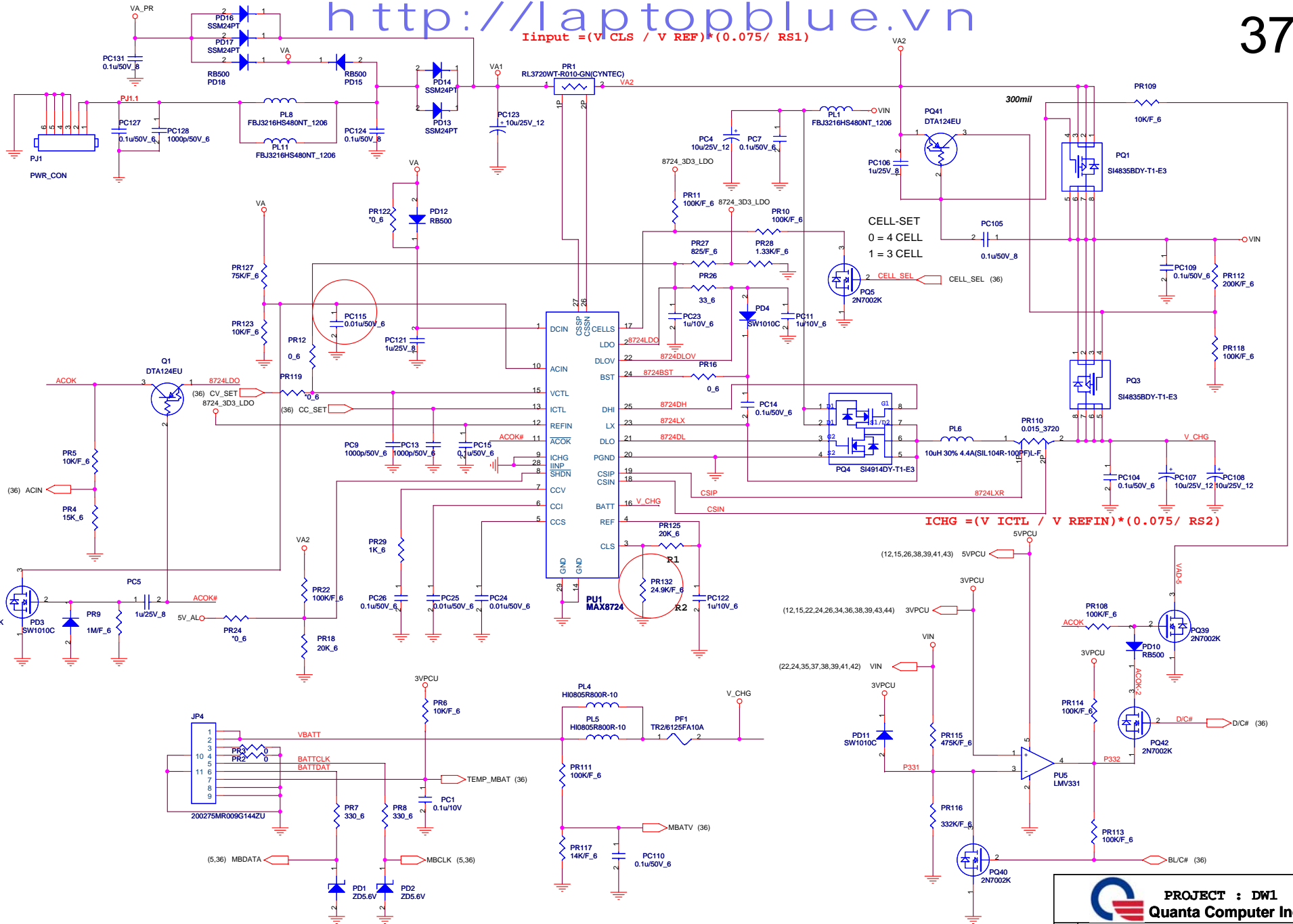








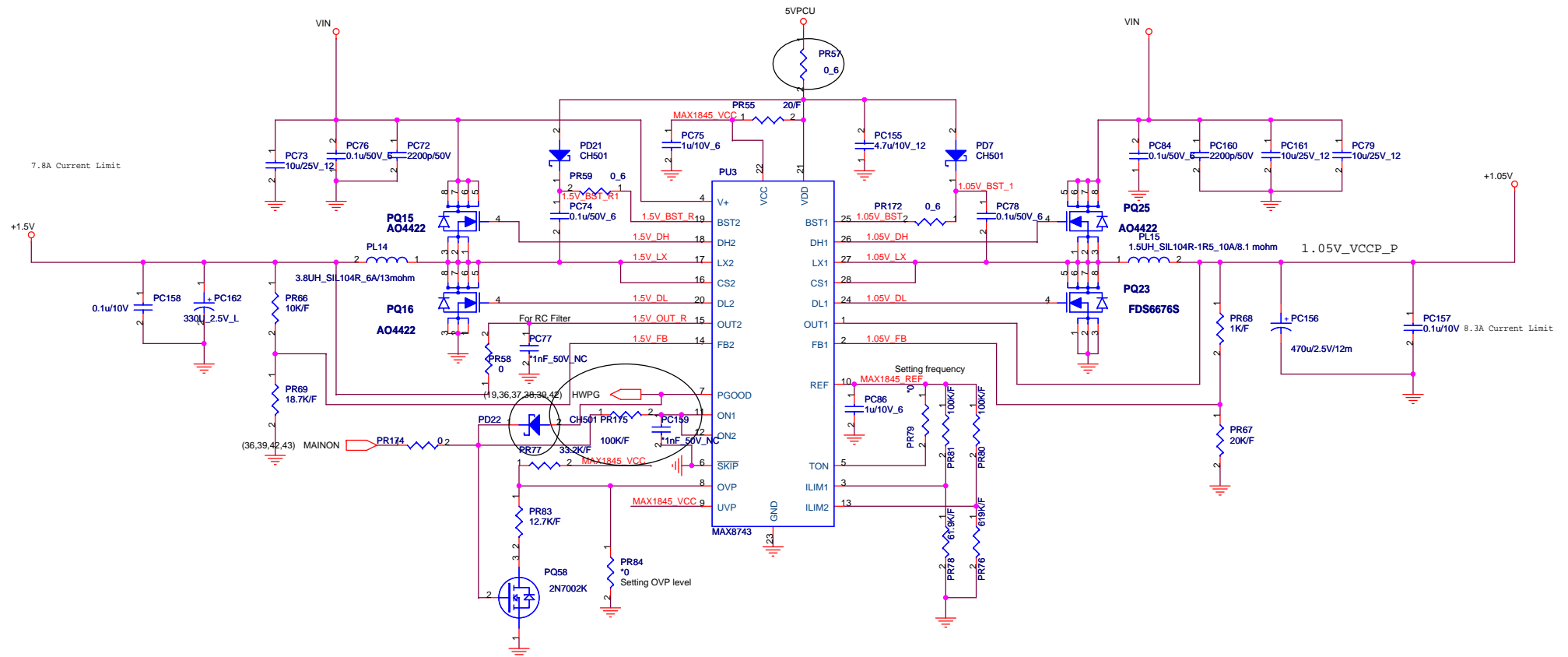




PROJECT : DW1  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CHARGER	3A
Date:	Thursday, June 15, 2006	Sheet 40 of 48

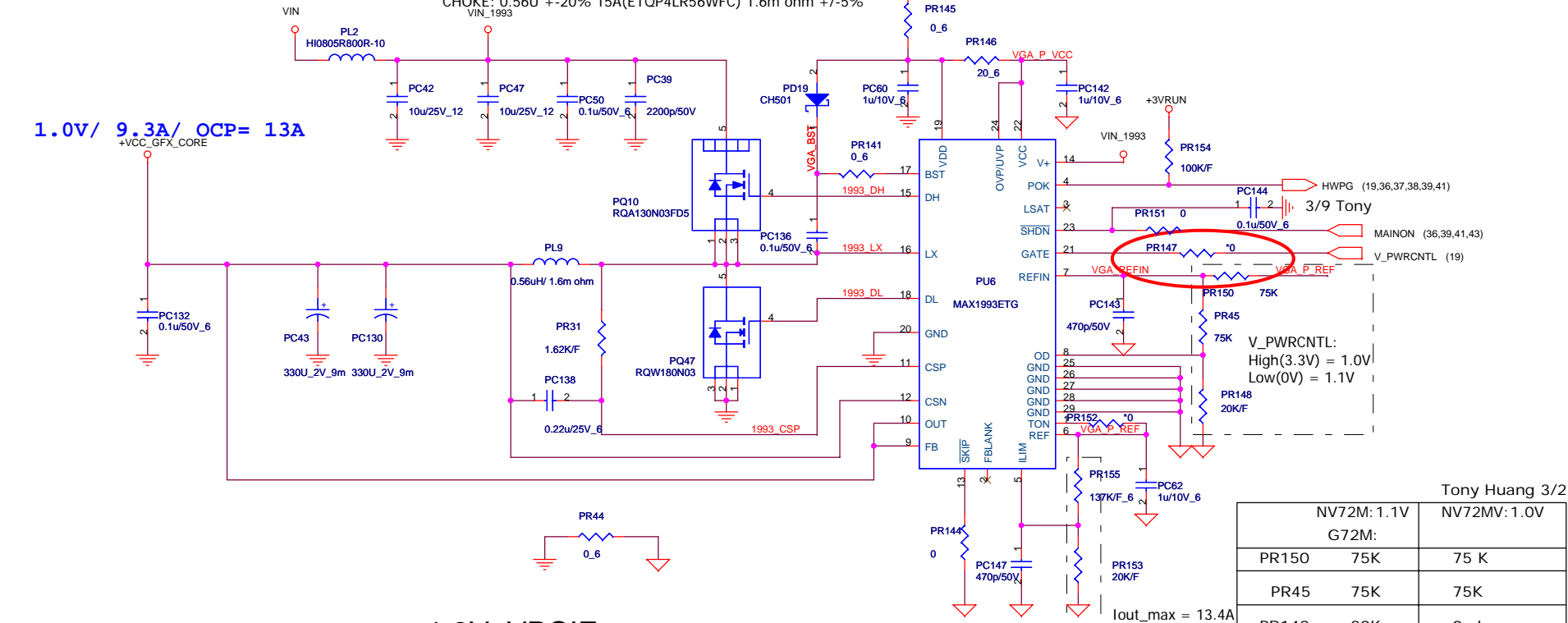
AO4422: Id= 11A, Rdson= 24m ohm, Qg= 19.8nC  
FDS6676S: Id= 14.5A, Rdson= 7.25m ohm, Qg= 43 nC



1.0V/ 9.3A/ OCP= 13A

RQW130N03: Id= 13A, Rdson= 17.1m ohm, Qg= 12.6nC  
RQW200N03: Id= 20A, Rdson= 5.6m ohm, Qg= 40 nC  
CHOKE: 0.56U +/-20% 15A(ETOP4LR56WFC) 1.6m ohm +/-5%

(13,14,25,31,33,35,43,44) +3VSUS  
(25,26,35,37,43,44) +5VSUS  
(22,24,35,37,38,39,40,41) VIN

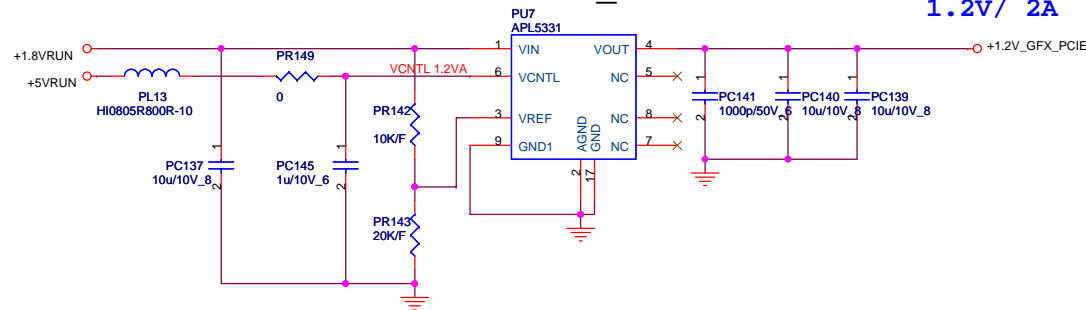


Tony Huang 3/2

NV72M: 1.1V	NV72MV: 1.0V
G72M:	
PR150	75K
PR45	75K
PR148	20K
PR147	NC

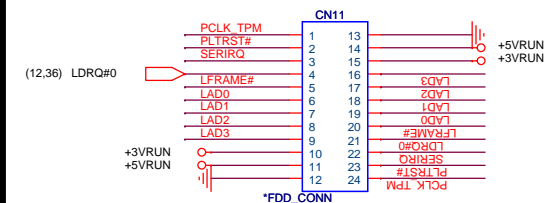
+1.2V\_VPCIE


1.2V/ 2A










 <div style="display: inline-block; vertical-align: middle;"> <b>PROJECT : TW3</b>  <b>Quanta Computer Inc.</b> </div>		
Size	Document Number	Rev
	<b>EMI &amp; TPM &amp; Debug Conn</b>	<b>3A</b>
Date:	Thursday, June 15, 2006	Sheet 44 of 48

MODEL		DATE	http://laptopblue.vn	
TW3A			Page	Description
B to 1223			Page 29	Change R472 to NI for SATA,install for PATA to solve sometimes ODD can't be detected and slow boot..
			Page 33	Add R481,R480 to solve WLAN LED light leakage.
			Page 3	Change R177 to install and pull low to set VGA clock to 100MHz.
			Page 19	Change R345 to install to solve back light can't enable.
			Page 29	Change R245 to NI for SATA,install for PATA.
			Page 14	Add R482,R483 for CRT/DVI option.
			Page 24	Change C645 to 10uF for LAN 1.2V per Marvell recommendation.
			Page 19	R377 to install,R362,R364,R365 to NI. (Set default to G72M)
			Page 30	3V_DVDD connect to +3VSUS to solve WOR.
1223 to 1224			Page 32	Change MQ1,MQ2,MQ3,MQ4 to BA000420Z07 to solve MODEM low performance.
			Page 37	Delete short pad.
			Page 38	Delete short pad.PC92 change to install.
			Page 39	Delete short pad.
			Page 41	Delete short pad.
			Page 42	Delete short pad.PR45,PR150 change to 75K(CS37502FB04).
			Page 43	Delete short pad.
			Page 5	R19 change to NI for solving power-on shutdown.
			Page 34	HOLE,3,HOLE4,HOLE7,HOLE8 change to MBRW1003011.
			Page 40	PR110 change to CS+0158JL11.PR132 change to 24.9K.
			Page 37	PC34,PC113,PC114,PC129 change to CH733RM8831.
			Page 23	F1 change to DK100TPU028.
			Page 33	Q17 change to install for BT LED control.
			Page 34	Change CN4 footprint to "afn250-a2g1t-25p-l" for SMT issue.
			Page 26	Change CN1.4 connection to RF_LED.
			Page 33	Add NET RF_LED.
			Page 36	Delete NET TUCHLED.
			Page 31	Change C541,C546 to X7R for audio precision.
1223 to 1226			Page 38	Change PC93,PD9,PC168 to install. Delete NET 10V.
			Page 41	Change NET 10V to +15V_SUS.
			Page 26	LED2,LED3 change to dual color type(cost down and unify brightness and color).
			Page 12	Reserve C784 on THERMTRIP for ESD.
			Page 35	Reserve R497,R498,R499 for TW2 PR.
			Page 33	Delete RP45,RP46,R210 for layout problem.
1226 to 1227			Page 33	Change CN23 to Molex (same as SW1). Add CN31 PCIE latch.
			Page 44	Add EMI spring B1,B2,B3.
			Page 32	Install MC8,MC9 for EMI.
			Page 12	Change C459 TO 22pF for EMI.
			Page 31	R479,R281,R295 change to install for EMI.
1227 to 1228			Page 44	Add B4,C785,C786,C787 for EMI.
			Page 19	Reserve R504,R505,R506,R507 for DVI EMI.
			Page 3	Change Y1 P/N to BG614318081(CL=20pF) for solving system time delay issue.
			Page 23	Change C694,C701,C703 to NI for signal quality.
			Page 36	RN2 change to 4.7K for IIC signal quality.
			Page 30	C528,C529 change to 1uF/10V X5R for audio precision.
			Page 35	Add L60-L66,C788-C793 for EMI.
1227 to 1230			Page 26	Change CN9,CN12 P/N to DFHS04FRE80.
			Page 36	Delete D13, add R508,R509,Q34 for PR leakage current. R454 change to 100K.



PROJECT : TW3  
Quanta Computer Inc.

Size	Document Number	Rev
Change Note		3A
Date: Thursday, June 15, 2006	Sheet 45 of 48	

MODEL	REV			
TW3A		Page	Description	
TW3A	1230 to 0102	Page 38	PC173 change to 470uF.	
		Page 39	PC66 change to install.	
		Page 42	PR153 change to 20K.	
		Page 41	PD7,PD21,PD22 change to CH501.	
		Page 37	PD6,PD5 change to CH501.	
		Page 42	PQ47 change to RQW180N03.	
	0102 to 0103	Page 26	CN12,CN9 USB connector change to DIP type.	
		Page 29	CN25 pin25,26 and CN24 pin47,48 disconnect to GND.	
		Page 23	CN6 pin27,28 disconnect to GND.	
		Page 34	SW1,SW2 P/N change to DHP00FC1G16.	
		Page 36	Change R454 to 100K,R508,R509 to 10K.	
		Page 4	R101,R97,Q11 change to install.	
	0103 to 0105	Page 6,7,8,9,10,11	Change U32 P/N to AJSL8Z40T26.(945PM)	
		Page 12,13,14,15	Change U36 P/N to AJSL8YB0T12.(ICH7M)	
		Page 37	PR128 change to 3.9K.	
		Page 45,46	Update change list.	
		Page 27	Change J1 P/N to DFHS04FRE47.	
		Page 35	Change CN15 to install and P/N to DFHS48FR001	
	0105 to 0111	Page 44	Change B1,B2,B4 P/N to FDTW3002018.	
		Page 36	U38 P/N change to AKE35ZAKK17.	
		Page 42	PR45,PR150 P/N change to CS37502FB12.	
		Page 30	Change C528,C529 to 2.2uF/6.3V for audio precision.	
C1 TO C2	0111 to 0119	Page 19	Change R26 to 0 ohm and change connection to THERM_OVER#.	
		Page 23	Q21 mirror vertical.	
		Page 23	Add C794~C799, L67~L69 for EMI.	
		Page 23	L46,L44,L42 change to 0 ohm. C700,C702,C705 change to NI for EMI.	
		Page 32	Change MR5,MR6,MR,MR10 to 280ohm. Add MR11,MR12,MR13. Change MR8 to NI.	
		Page 35	R17 change to install.	
	0119 to 0120	Page 35	CN15.21,22 change to CRT_GND. Add R512 for EMI.	
		Page 35	Change D1 to page23 and its connection and to NI.	
		Page 41	PL14 P/N change to DC-38600001.	
		Page 43	PQ59,PQ61,PQ36 P/N change to BAM44220002.	
		Page 36	RN2 P/N change to CJ247084N25.	
		Page 26	LED4 P/N change to BEBL0002Z62. LED1~3 P/N change to BEAB0013ZA1.	
	0120 to 0209A	Page 33	CN10 P/N change to DFHS26FR489.	
		Page 14	Change R368 to install,R366 to NI to set w/ docking.	
		Page 27	Change D7 to install to solve 7402 does not work.	
		Page 19	Delete R410,R413,R417 for EMI layout.	
		Page 23	Correct CN6 C1~C4 pin define.	
		Page 23	Reserve Q37,Q38,RP56,R513,R514 for DVI disable when docking attach.	
C2 TO C3	0120 to 0209A	Page 29	CN25 footprint change to "SATA-C16647-122A4-B-22P-R-V" for SMT issue.	
		Page 25	LAN active/link LED change to +3VSUS.	

MODEL	DATE	Change Note	
TW3A	0209 to 0222A	Page	Description
C2 to C3	0209 to 0222A	Page 23	(1) CN20 pin 12,15 change connect to DVI_DDCDAT,DVI_DDCCLK (In C1 was connect to DDCCLK2,DDCDAT2) (2) R150,R159,Q37,Q38,RP56 Change to install for DVI,CRT I2C,D1 change to NI (3) Change L67,L68,L69 P/N from CX8BB121002 to CX8BB470007 (4) Change C794,C795,C796,C797,C798,C799 P/N from CH01806JB07 to CH01006JB08
		Page 27	(1) Change R208 pin1 contact to +3VRUN Change R208 P/N to CS31002JB28,C473 change to CH4102K1B03 ,D7 change to NI.
		Page 34	(1) RP47,RP48,RP49 change to CJ3100A8N21 (meet Rohs)
		Page 42	(1) Change PR147 to NI
Production	0222A to 0407A	Page 26	(1) Change CN9,CN12 layout footprint to usb-020133mr004s566zl-c-h
	0407A to 0510	Page 31	(1) Change U21 layout footprint to QFN28-5X5-5-33P(add thermal Pad)
		Page 23	(1) Change C794~C796 to 6.8PF(CH-6816TB05) (2) Change C797~C799 to 33PF(CH03306JB04) (3) Change L67,L68,L69 to BLM18BA750SN1D,75 0.3A(CX8BA750006)
	0510 to 0523	Page 12	(1) Change R186 from CS03902JB21 to CX5LL241002 , C459 from CH02206GB02 to NI
		Page 19	(1) Change R504~R507 from CS11502FB21 to CH01006JB08
		Page 27	(1) Change EB1,EB2 from NI to DC09004A014 ,R286~R289 from CS00002JB38 to NI
		Page 30	(1) Change R477,R478 from CS03902JB21 to CX8LL241008R279,R285 from CS00003J951 to CX8LL241008, L33 from CX221T05009 to CX8LL241008
		Page 31	(2) Change R256 to CS02202JB22,C539 to CH02206GB02* R256 from NI to CS02202JB22,C539 from NI to CH02206GB02 (1) Change R268,R278 from CS03303J941 to CX8LL241008 (2) Change C564 from NI to CH11006F909

PROJECT : TW3

Quanta Computer Inc.

Size

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Rev

Change Note

3A

Date: Thursday, June 15, 2006

Sheet 47 of 48

A. G72M to G72MV

1. change P/N to G72MV (AJ073000T14)
2. Set VGA core to 1.0V fix.
3. Change PCI\_DEVID.

B. VRAM 128MB to 64MB

- 1.follow config table to set RAM\_CFG.
- 2.Change VRAM P/N to HYNIX.
- 3.VRAMx2

C. LAN GIGA to 10/100.

- 1.Change LAN chip to 8038(AJ080380000).
- 2.Change Rset resistor.
- 3.Change transformer.

D. SATA to PATA

- 1.Set ODD to slave.
- 2.Set HDD to master.
3. Remove SATA conn.
4. Add PATA conn.
5. Change board ID to PATA.
6. Install resistor to connect ODD and HDD LED.
7. NI resistor of SATA LED.

E. docking to no docking.

- 1.Set board ID4 to low.