

# NWQAA

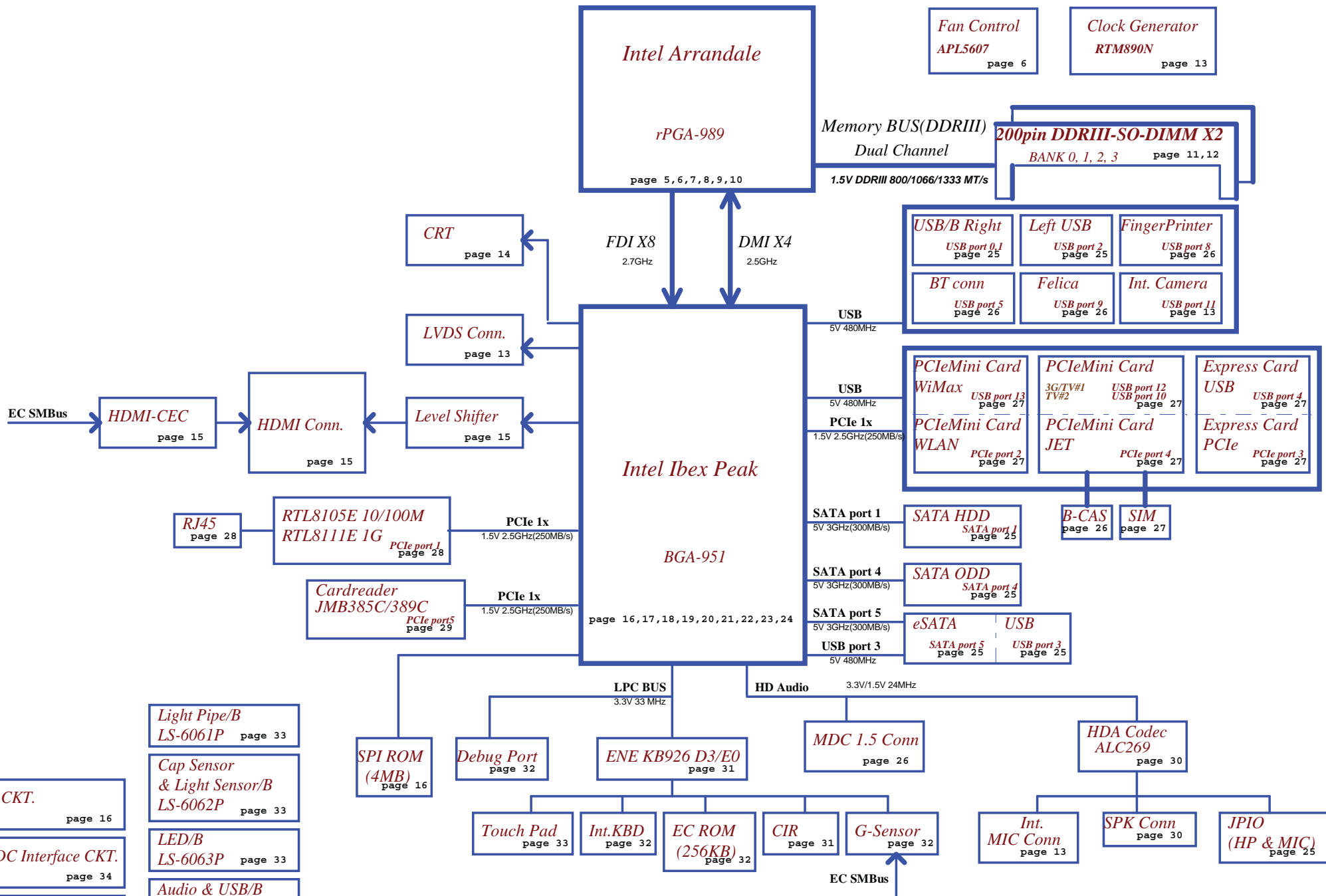
## *Marseille 10*

# LA-6061P REV 2.0 Schematic

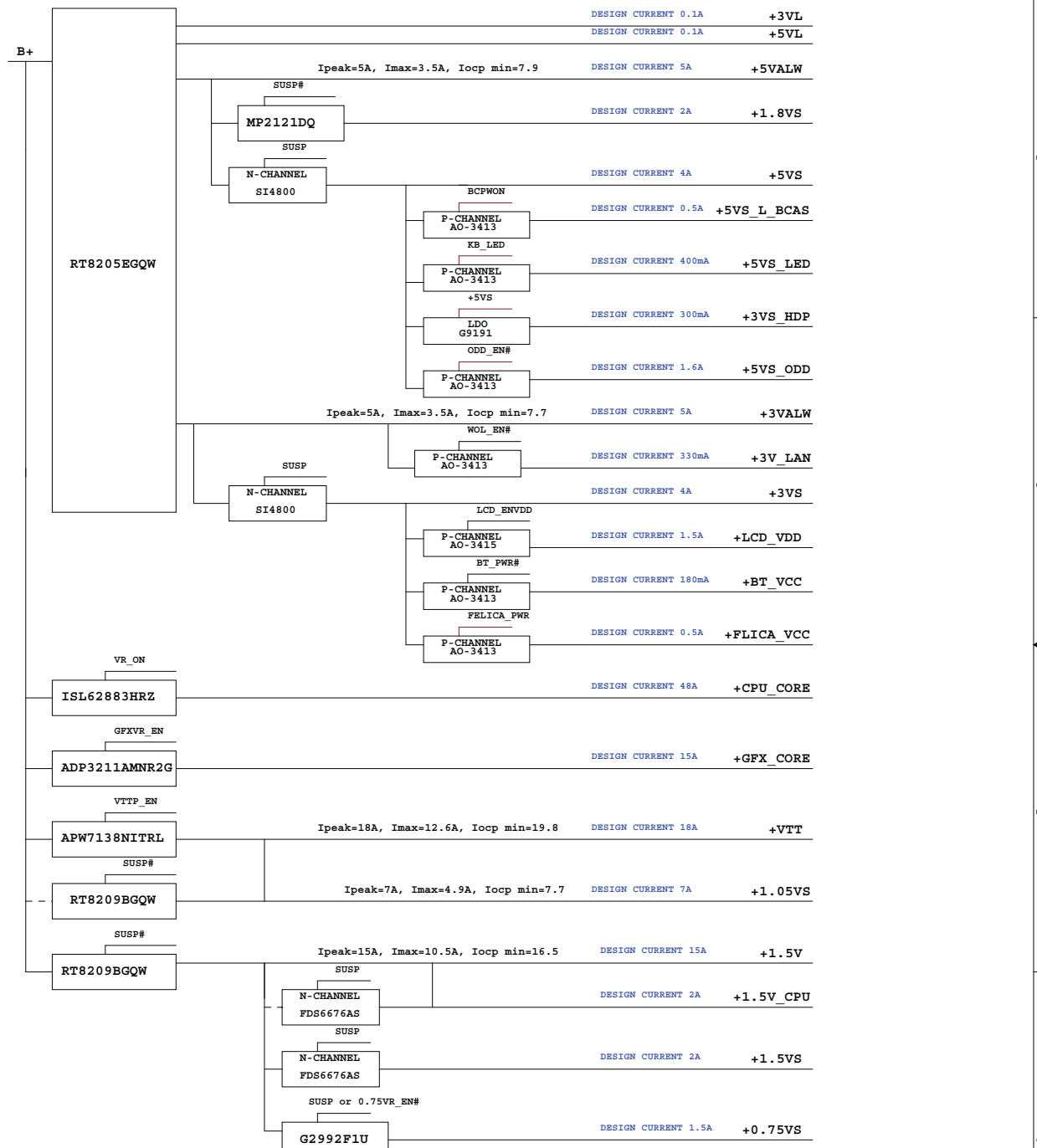
Intel Processor (ARD) / PCH (HM55)

2010-03-24 Rev 2.0

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/10/05	Deciphered Date	2010/01/23	Title	
				Cover Page	
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# Voltage Rails ( O MEANS ON X MEANS OFF )

<div> <div>power plane</div> <div>State</div> </div>	+RTCVCC	+B	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.5VS +VGA_CORE +CPU_CORE +VTT +1.05VS +1.8VS +1.1VS +0.75VS
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

## PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	New Card		
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		
+3VS	3G		

## EC SM Bus1 Address

## EC SM Bus2 Address

Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b	+3VS	PCH	96 H	1001 0110 b
+3VL	HDMI-CEC	34 H	0011 0100 b	+3VS	G-Sensor	40 H	0100 0000 b
				+3VS	Light Sensor	52 H	0101 0010 b
Power	Device	HEX	Address				
+3VL	Cap. Sensor		Virtual I2C				

## BTO Option Table

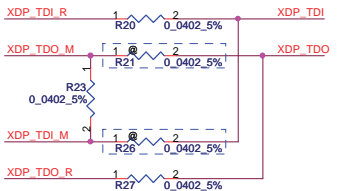
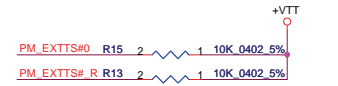
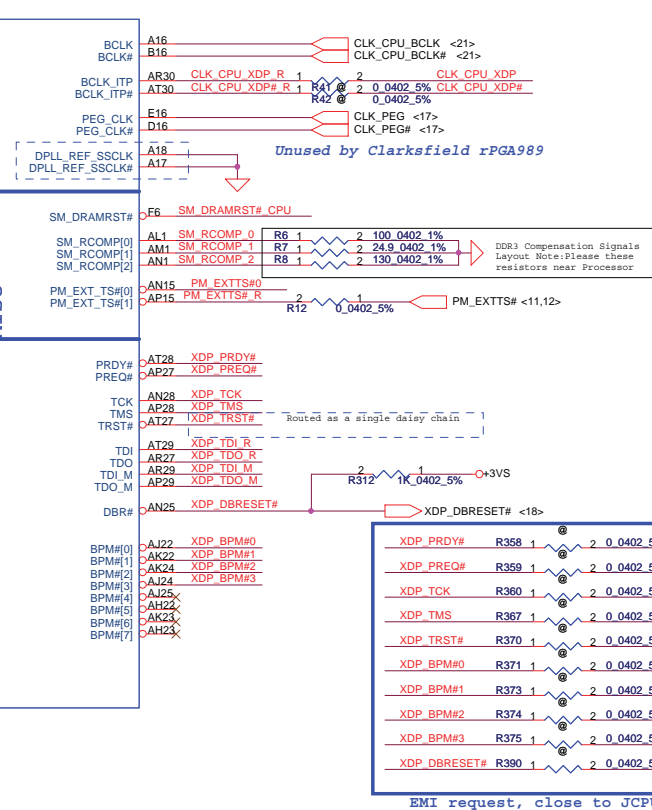
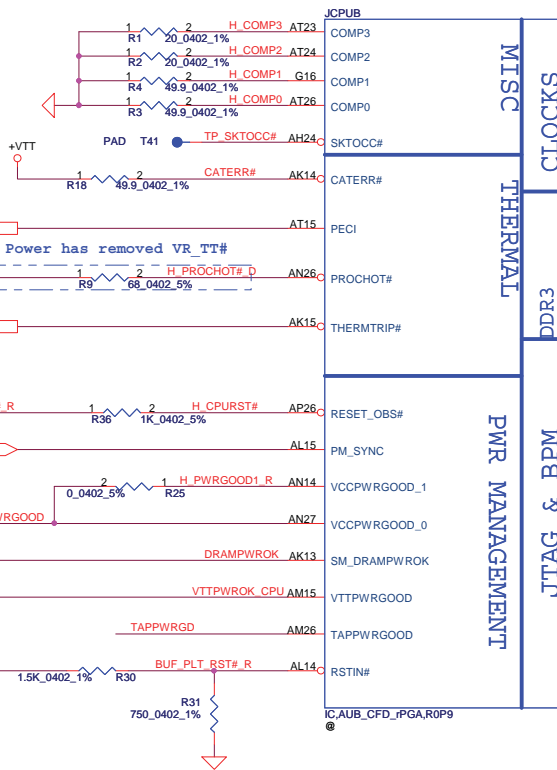
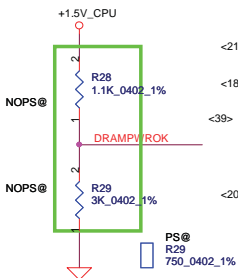
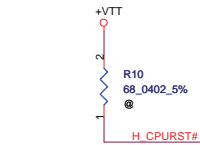
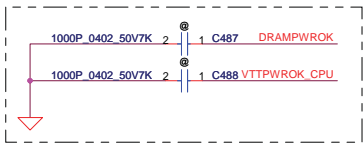
Function	MINI PCI-E SLOT			LAN		Fingerprint	Modem	CIR	KB Light
description	SLOT2		SLOT1	LAN		Fingerprint	Modem	CIR	KB Light
explain	3G	TV Tuner	WIMAX	10/100M	Giga	Fingerprint	Modem	CIR	KB Light
BTO	3G@	TV@	WIMAX@	8105E@	8111E@	FPE@	MDC@	CIR@	KBL@

Function	Felica	BLUE TOOTH	G-SENSOR	Camera & Mic	HDMI		Card reader	
description	Felica	BLUE TOOTH	G-SENSOR	Camera & Mic	HDMI		JMB385C/389C	
explain	Felica	BLUE TOOTH	G-SENSOR	Camera & Mic	UMA	CEC	JMB385C	JMB389C
BTO	FELICA@	BT@	GSENSOR@	CAM@	IHDMI@	CEC@	JMB385@	JMB389@

Function	S3 Power Saving		New Card
description	S3 Power Saving		New Card
explain	No Power Saving	Power Saving	New Card
BTO	NOPS@	PS@	NEW@

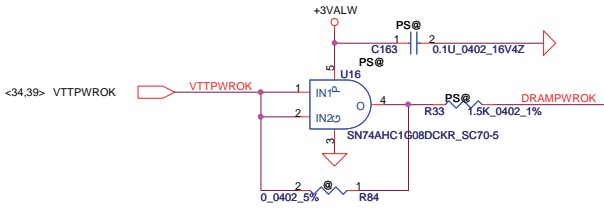
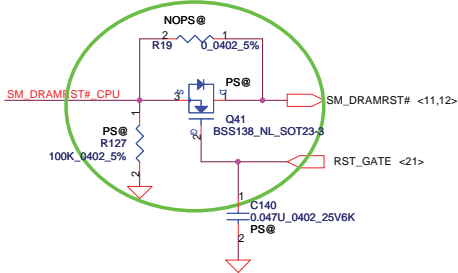
STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON		HIGH	HIGH	HIGH
S1 (Power On Suspend)		HIGH	HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH	HIGH
S4 (Suspend to Disk)		LOW	LOW	HIGH
S5 (Soft OFF)		LOW	LOW	LOW
G3		LOW	LOW	LOW

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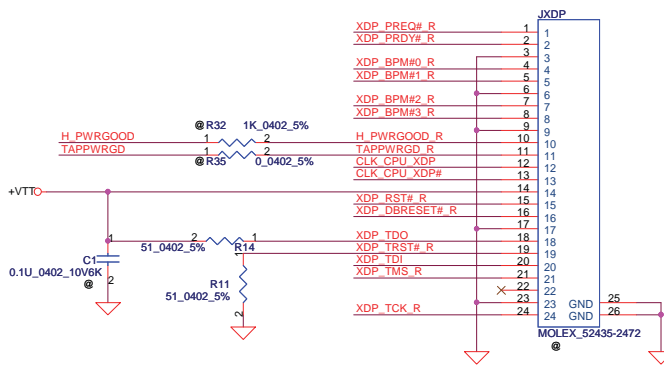


JTAG MAPPING	
Scan Chain (Default)	STUFF -> R20, R23, R27 NO STUFF -> R21, R26
CPU Only	STUFF -> R20, R21 NO STUFF -> R23, R26, R27
GMCH Only	STUFF -> R26, R27 NO STUFF -> R20, R21, R23

## For S3 CPU Power Saving



## XDP Connector

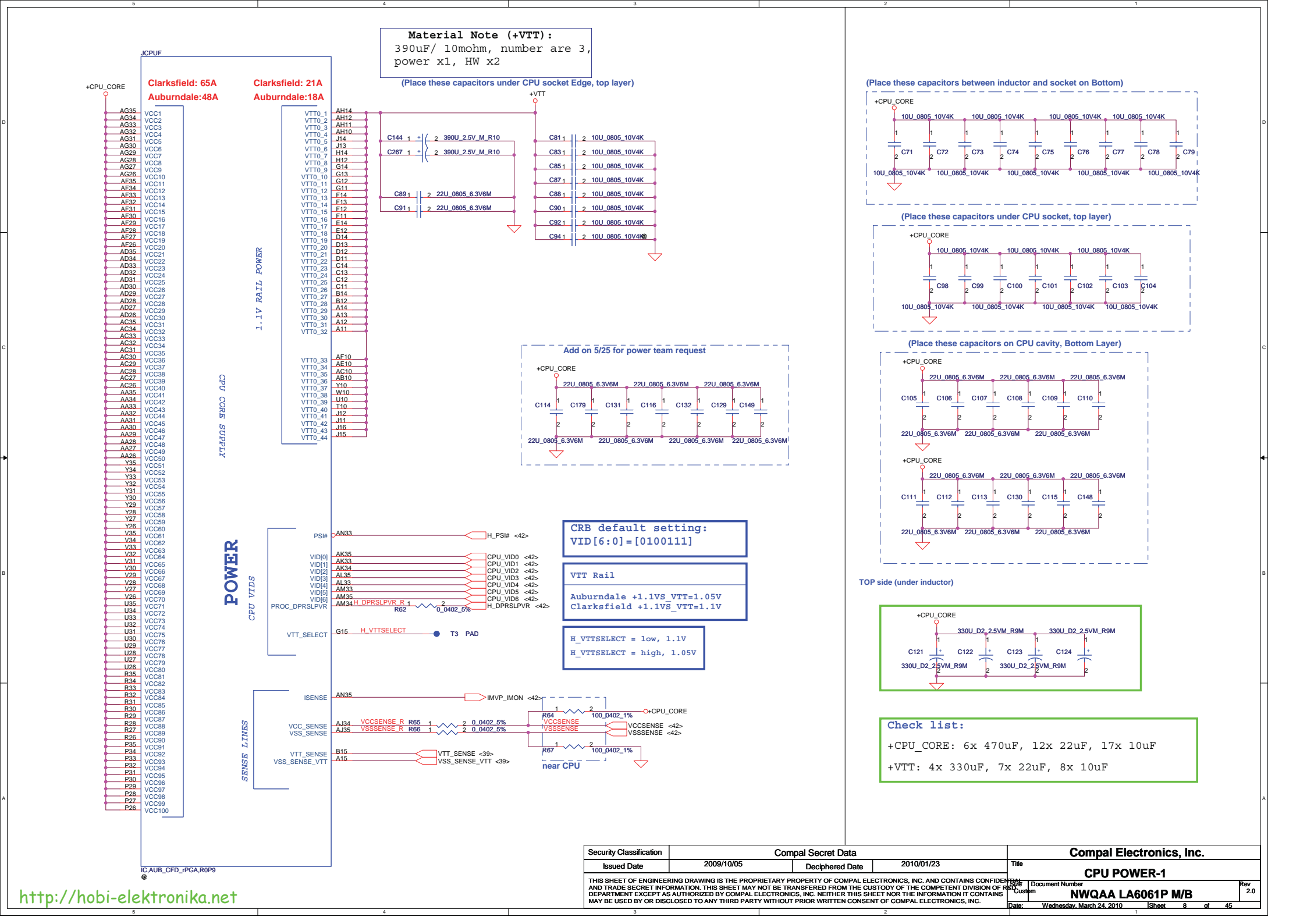


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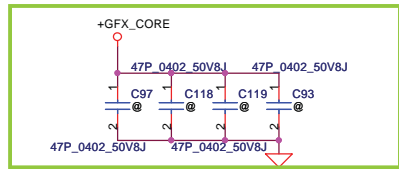


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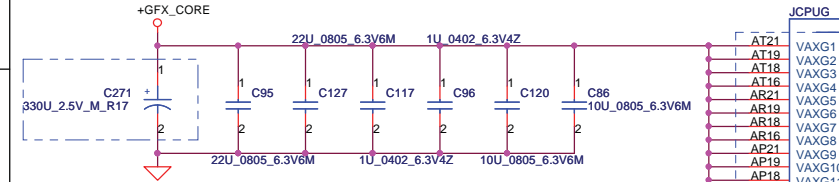




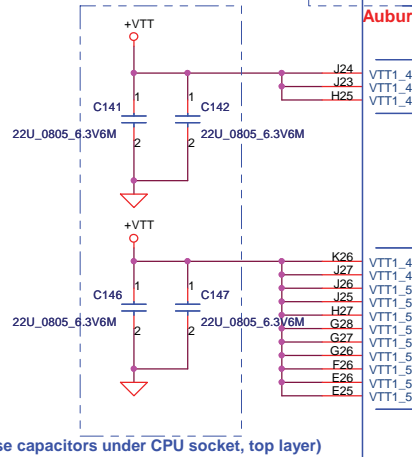
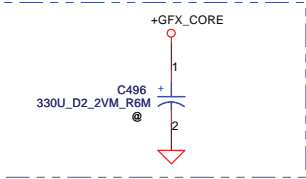
For EMI request



Change C271 to 4.5mm height OS-CON at PVT



Add C496 Co-Layout with C271



(Place these capacitors under CPU socket, top layer)

JCPUG

AT21 VAXG1  
AT19 VAXG2  
AT18 VAXG3  
AT16 VAXG4  
AR21 VAXG5  
AR19 VAXG6  
AR18 VAXG7  
AR16 VAXG8  
AP21 VAXG9  
AP19 VAXG10  
AP18 VAXG11  
AP16 VAXG12  
AN21 VAXG13  
AN19 VAXG14  
AN18 VAXG15  
AN16 VAXG16  
AM21 VAXG17  
AM19 VAXG18  
AM18 VAXG19  
AM16 VAXG20  
AL21 VAXG21  
AL19 VAXG22  
AL18 VAXG23  
AK19 VAXG24  
AK18 VAXG25  
AK16 VAXG26  
AJ21 VAXG27  
AJ19 VAXG28  
AJ18 VAXG29  
AJ16 VAXG30  
AH21 VAXG31  
AH19 VAXG32  
AH18 VAXG33  
AH16 VAXG34  
VAXG35  
VAXG36

Auburndale:22A

VTT1\_45  
VTT1\_46  
VTT1\_47

Clarksfield: 21A  
Auburndale:18A

VTT1\_48  
VTT1\_49  
VTT1\_50  
VTT1\_51  
VTT1\_52  
VTT1\_53  
VTT1\_54  
VTT1\_55  
VTT1\_56  
VTT1\_57  
VTT1\_58

IC:AUB\_CFD\_rPGA,R0P9

GRAPHICS

SENSE LINES

VAXG\_VID[0]  
VAXG\_VID[1]  
VAXG\_VID[2]  
VAXG\_VID[3]  
VAXG\_VID[4]  
VAXG\_VID[5]  
VAXG\_VID[6]  
GFX\_VR\_EN  
GFX\_DPRSLPVR  
GFX\_IMON

Clarksfield: 5A  
Auburndale:3A

POWER

DDR3 - 1.5V RAILS

VDDQ01  
VDDQ02  
VDDQ03  
VDDQ04  
VDDQ05  
VDDQ06  
VDDQ07  
VDDQ08  
VDDQ09  
VDDQ10  
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VDDQ14  
VDDQ15  
VDDQ16  
VDDQ17  
VDDQ18

1.1V

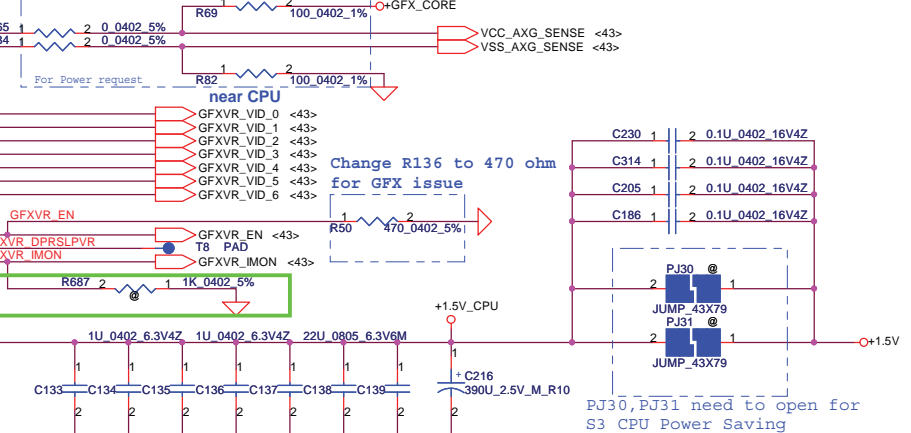
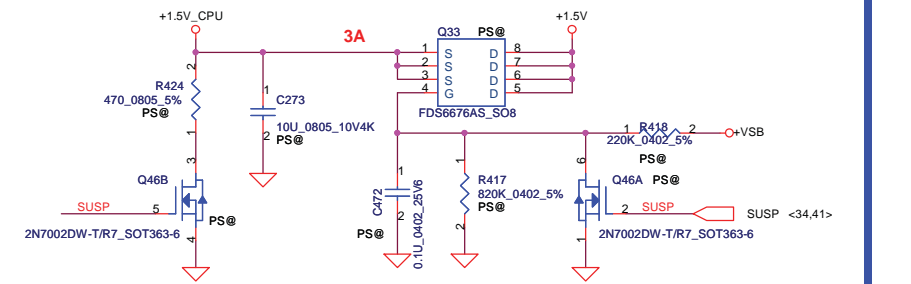
VTT0\_59  
VTT0\_60  
VTT0\_61  
VTT0\_62  
VTT1\_63  
VTT1\_64  
VTT1\_65  
VTT1\_66  
VTT1\_67  
VTT1\_68

1.8V

VCCPLL1  
VCCPLL2  
VCCPLL3

Clarksfield: 0.6A  
Auburndale:1.35A

For S3 CPU Power Saving



PJ30, PJ31 need to open for S3 CPU Power Saving

(Place these capacitors under CPU socket Edge, top layer)






(Place these capacitors under CPU socket, top layer)

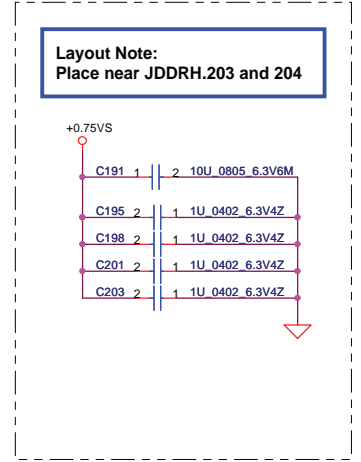
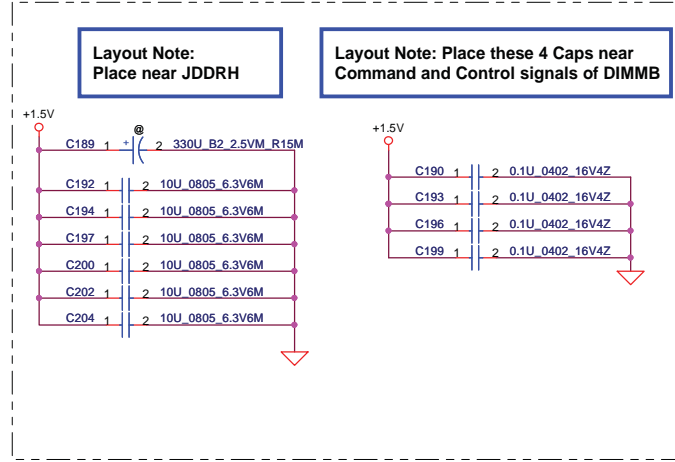
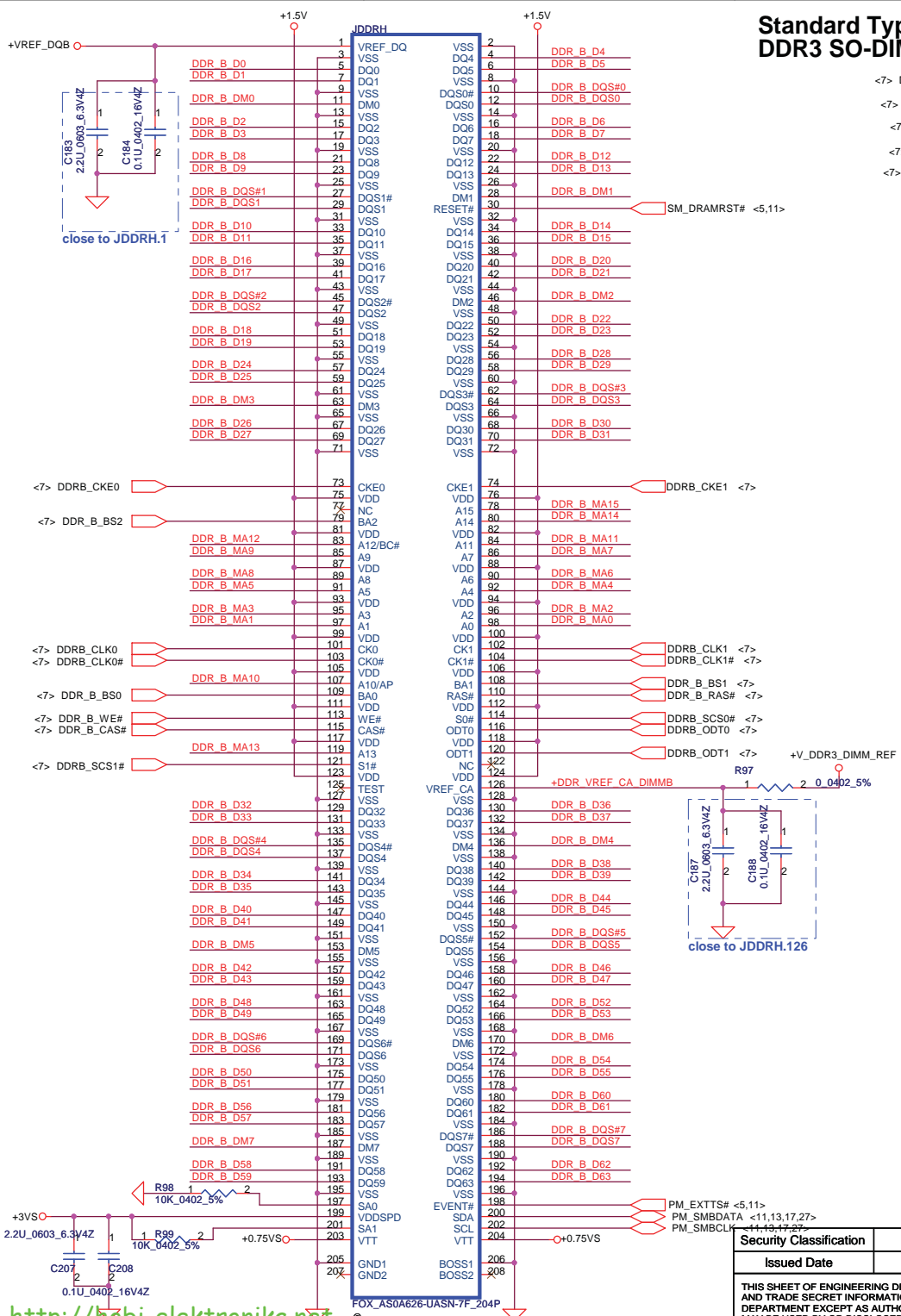
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# Standard Type DDR3 SO-DIMM B

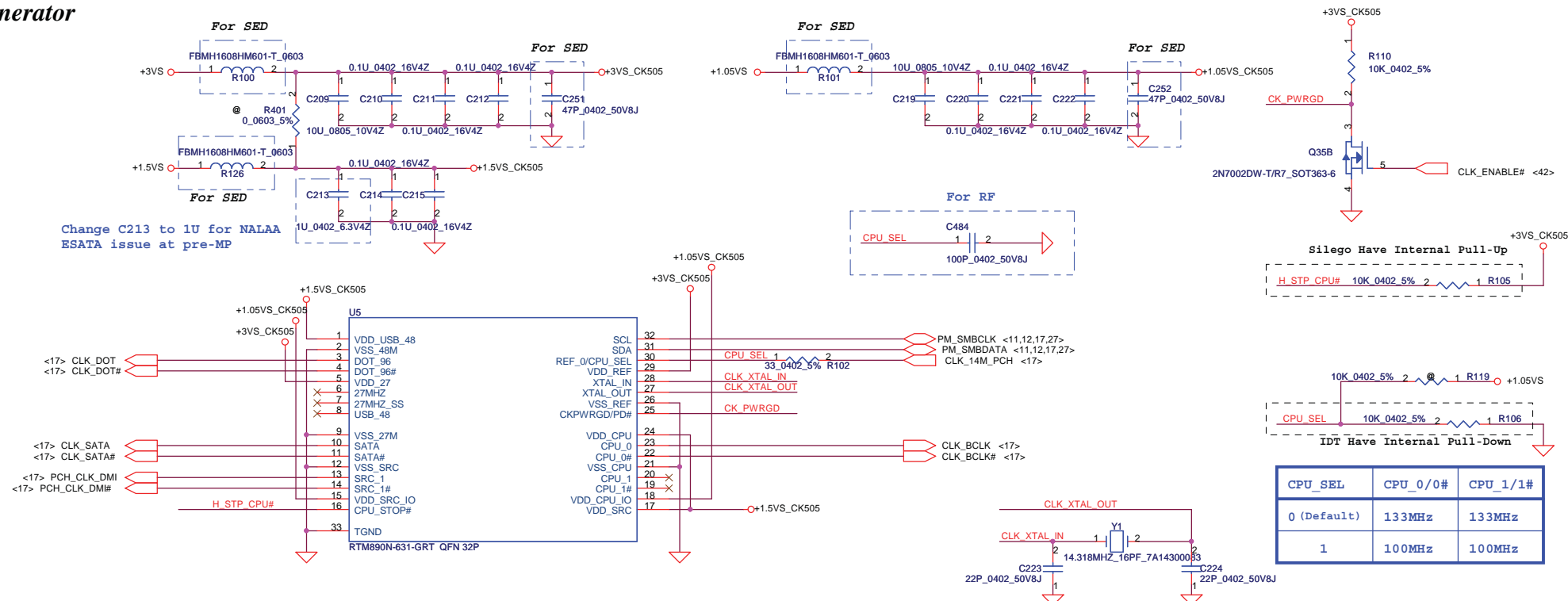
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 <7> DDR\_B\_D[0..63]   
 <7> DDR\_B\_DM[0..7]   
 <7> DDR\_B\_MA[0..15] 



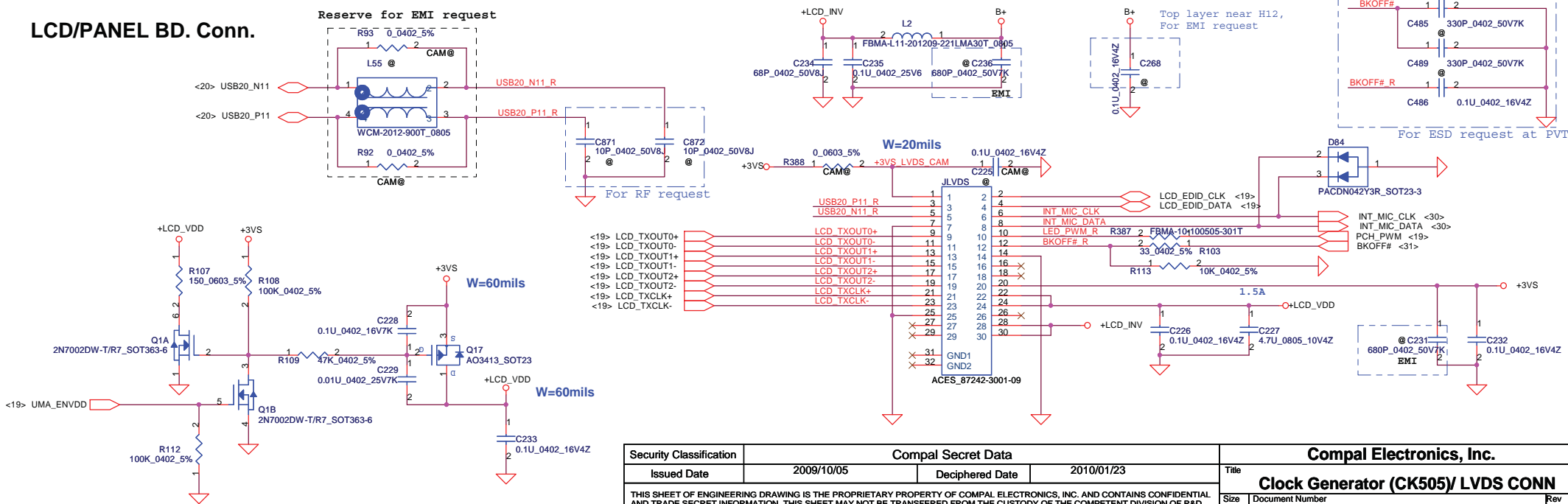
41.43.17.27

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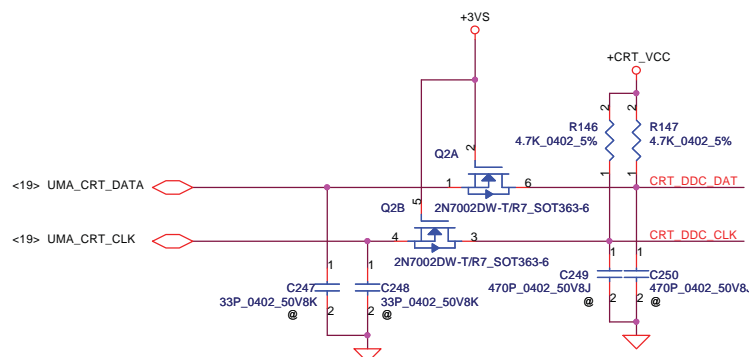
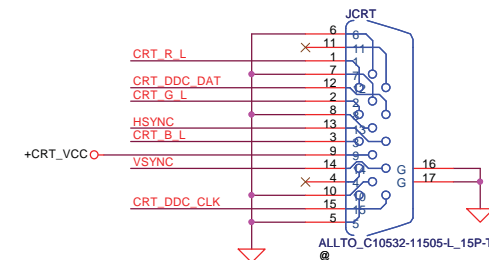
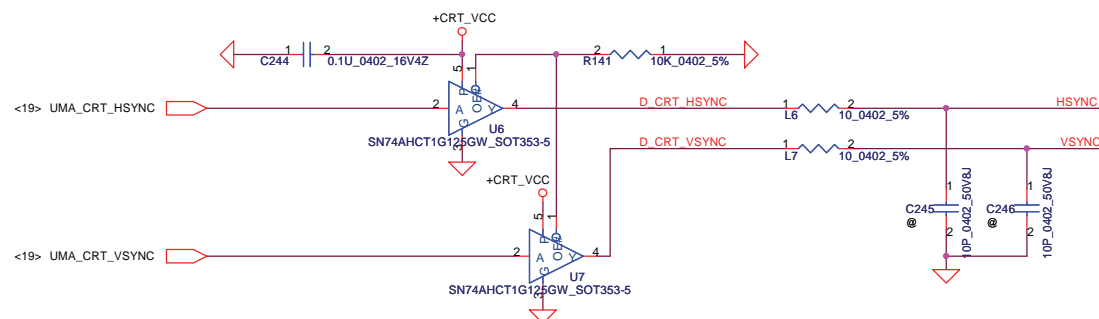
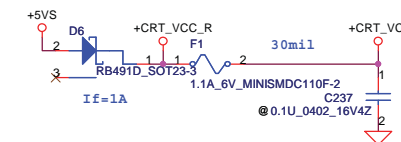
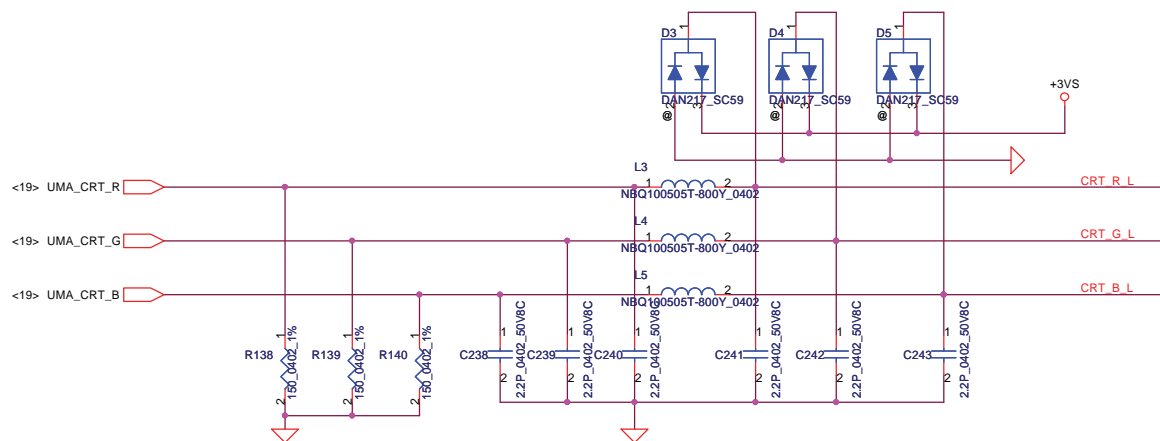
## Clock Generator



**LCD/PANEL BD. Conn.**



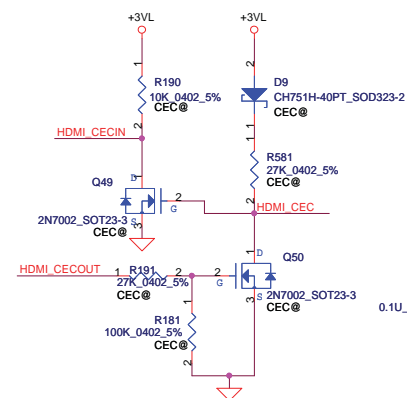
# CRT CONNECTOR



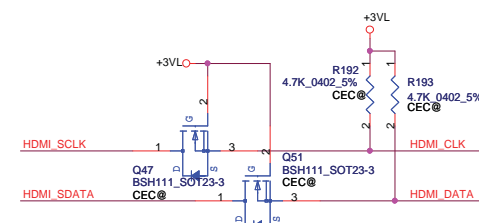
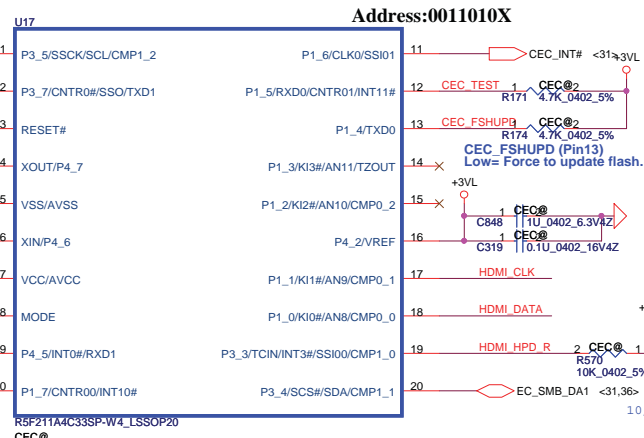
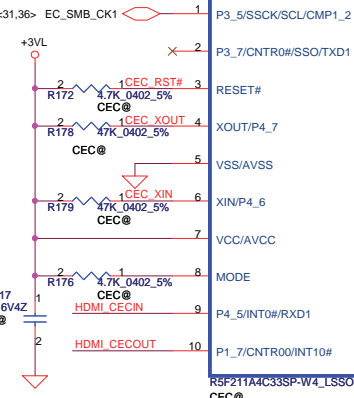
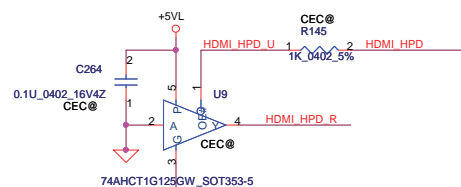
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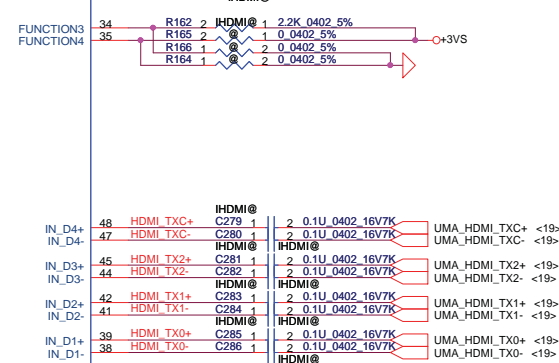
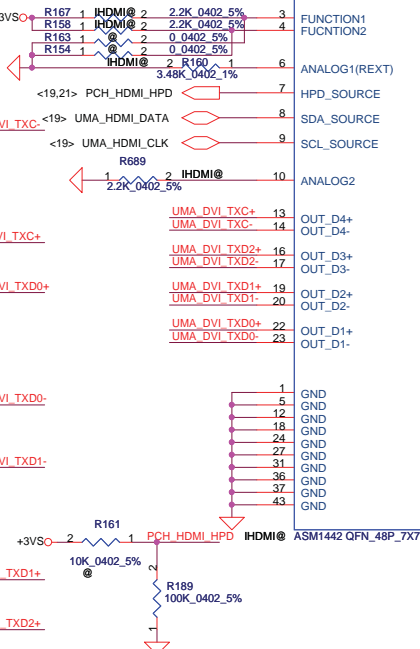
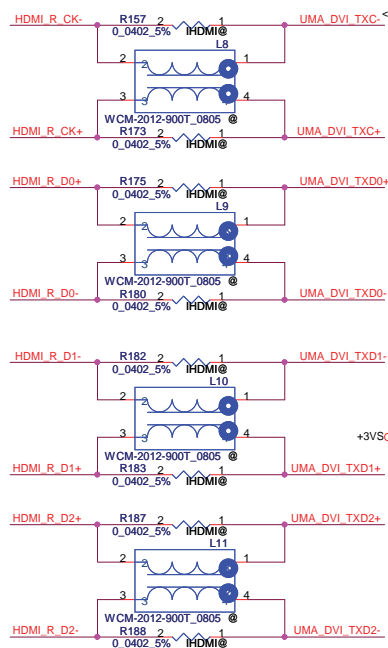
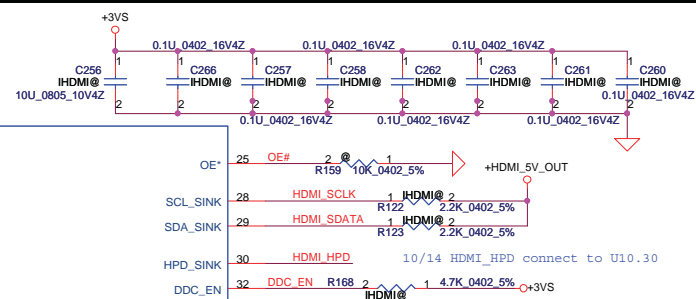
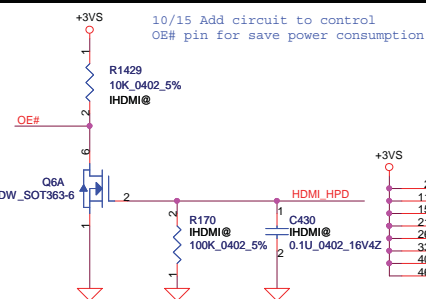
## HDMI CEC Controller



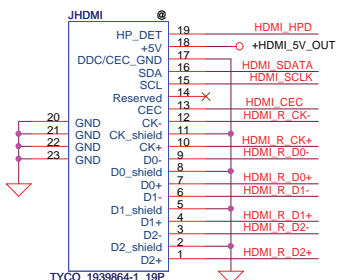
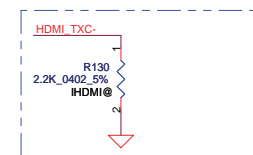
10/14 Remove R691 and change BOM Structure to CEC®



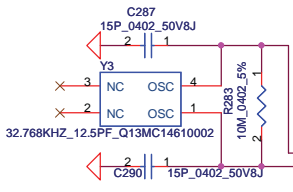
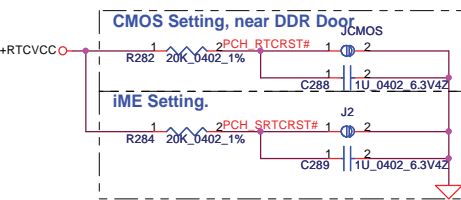
10/14 HDMI HPD R pull-up to +3VL



Add R130 for AOC monitor  
issue at PVT



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**Integrated SUS 1.05V VRM Enable**

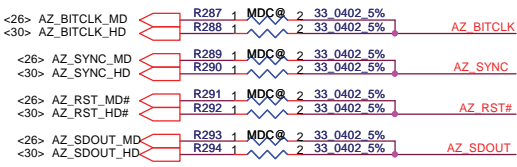
PCH\_INTVRMEN High - Enable Internal VRs (must be always pulled high)

**HDA\_SYNC**  
This signal has a weak internal pull down.  
H=>On Die PLL is supplied by 1.5V  
L=>On Die PLL is supplied by 1.8V

**HDA\_SDO**  
This signal has a weak internal pull down.  
This signal can't PU

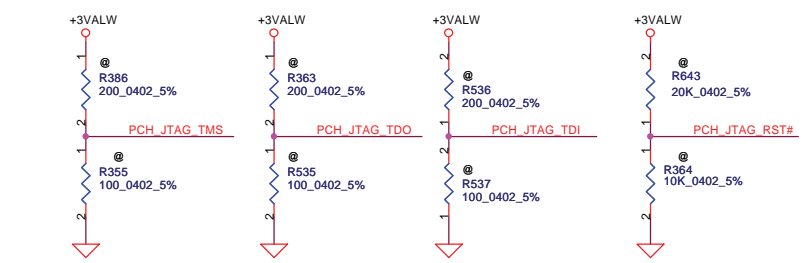
**Flash Descriptor Security Override**

HDA\_DOCK\_EN# Low = Enabled  
High = Disabled \*



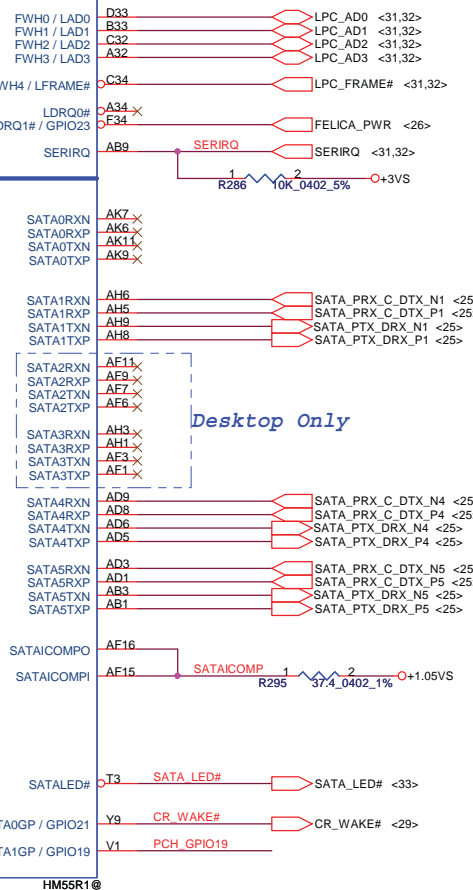
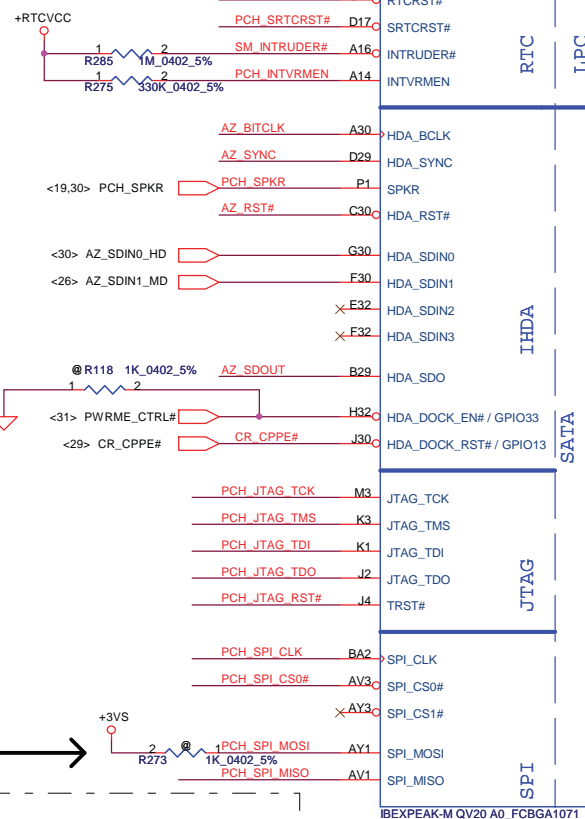
**ITPM Enabled Internal: Pull down 20k**

SPI\_MOSI High = Enabled  
Low = Disabled (Default)



06/01 change R125 from 4.7K to 51 ohm

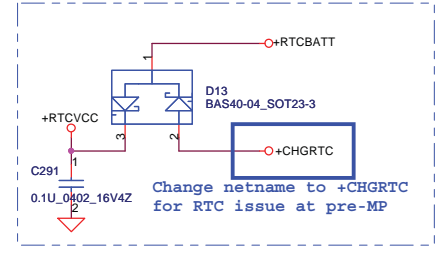
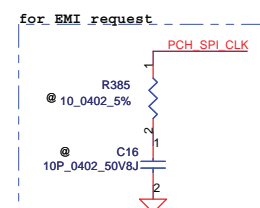
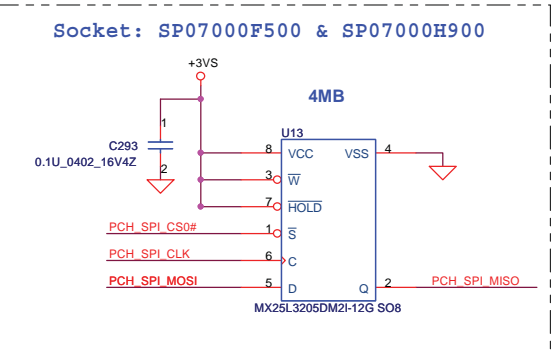
PCH Pin	RefDes	PCH JTAG Enable		PCH JTAG Disable (Default)	
		ES1	ES2	ES1	ES2
PCH_JTAG_TDO	R358	No Install	200ohm	No Install	No Install
PCH_JTAG_TMS	R355	No Install	100ohm	No Install	No Install
PCH_JTAG_TDI	R354	100ohm	100ohm	No Install	No Install
PCH_JTAG_RST#	R536	200ohm	200ohm	20Kohm	No Install
PCH_JTAG_TCK	R156	51ohm	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R643	20Kohm	20Kohm	No Install	No Install
PCH_JTAG_TDO	R355	No Install	100ohm	No Install	No Install



1ST HDD

SATA ODD

eSATA



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								PCH-SPI/SATA/LPC/RTC/HDA			
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Date		Wednesday, March 24, 2010		Sheet		16		of 45			



For LAN

<28> PCIE\_PRX\_C\_LANTX\_N1  
<28> PCIE\_PRX\_C\_LANTX\_P1  
<28> PCIE\_PTX\_C\_LANRX\_N2  
<28> PCIE\_PTX\_C\_LANRX\_P1

For WLAN

<27> PCIE\_PRX\_WLANTX\_N2  
<27> PCIE\_PRX\_WLANTX\_P2  
<27> PCIE\_PTX\_C\_WLANRX\_N2  
<27> PCIE\_PTX\_C\_WLANRX\_P2

For NewCard

<27> PCIE\_PRX\_NEWTX\_N3  
<27> PCIE\_PRX\_NEWTX\_P3  
<27> PCIE\_PTX\_C\_NEWRX\_N3  
<27> PCIE\_PTX\_C\_NEWRX\_P3

For JET

<27> PCIE\_PRX\_JETTX\_N4  
<27> PCIE\_PRX\_JETTX\_P4  
<27> PCIE\_PTX\_C\_JETRX\_N4  
<27> PCIE\_PTX\_C\_JETRX\_P4

For Card Reader

<29> PCIE\_PRX\_C\_CRTX\_N5  
<29> PCIE\_PRX\_C\_CRTX\_P5  
<29> PCIE\_PTX\_C\_CRRX\_N5  
<29> PCIE\_PTX\_C\_CRRX\_P5

LAN

<28> CLK\_LAN#  
<28> CLK\_LAN

WLAN

<27> CLK\_WLAN#  
<27> CLK\_WLAN

NewCard

<27> CLK\_NEW#  
<27> CLK\_NEW

JET

<27> CLK\_JET#  
<27> CLK\_JET

Card Reader

<29> CLK\_CR#  
<29> CLK\_CR

U11B

PCIE\_PRX\_C\_LANTX\_N1 BG30  
PCIE\_PRX\_C\_LANTX\_P1 BJ30  
PCIE\_PTX\_C\_LANRX\_N1 BF29  
PCIE\_PTX\_C\_LANRX\_P1 BH29

AW30  
PCIE\_PRX\_WLANTX\_N2 BA30  
PCIE\_PTX\_C\_WLANRX\_N2 BC30  
PCIE\_PTX\_C\_WLANRX\_P2 BD30

NEW@  
PCIE\_PRX\_NEWTX\_N3 AU30  
PCIE\_PRX\_NEWTX\_P3 AT30  
PCIE\_PTX\_C\_NEWRX\_N3 AU32  
PCIE\_PTX\_C\_NEWRX\_P3 AV32

NEW@  
PCIE\_PRX\_JETTX\_N4 BA32  
PCIE\_PRX\_JETTX\_P4 BB32  
PCIE\_PTX\_C\_JETRX\_N4 BD32  
PCIE\_PTX\_C\_JETRX\_P4 BE32

BF33  
PCIE\_PRX\_C\_CRTX\_N5 BH33  
PCIE\_PTX\_C\_CRRX\_N5 BG32  
PCIE\_PTX\_C\_CRRX\_P5 BJ32

BA34  
AW34  
BC34  
BD34

AT34  
AU34  
AV36  
AV36

BG34  
BJ34  
BG36  
BJ36

AK48  
AK47  
CLKOUT\_PCIE0N  
CLKOUT\_PCIE0P

CLKREQ\_LAN# P9  
PCIECLKRQ0# / GPIO73

AM43  
AM45  
CLKOUT\_PCIE1N  
CLKOUT\_PCIE1P

CLKREQ\_WLAN# U4  
PCIECLKRQ1# / GPIO18

AM47  
AM48  
CLKOUT\_PCIE2N  
CLKOUT\_PCIE2P

CLKREQ\_NEW# N4  
PCIECLKRQ2# / GPIO20

AH42  
AH41  
CLKOUT\_PCIE3N  
CLKOUT\_PCIE3P

CLKREQ\_JET# A8  
PCIECLKRQ3# / GPIO25

AM51  
AM53  
CLKOUT\_PCIE4N  
CLKOUT\_PCIE4P

CLKREQ\_CR# M9  
PCIECLKRQ4# / GPIO26

AJ50  
AJ52  
CLKOUT\_PCIE5N  
CLKOUT\_PCIE5P

AK53  
AK51  
CLKOUT\_PEG\_B\_N  
CLKOUT\_PEG\_B\_P

PCH\_GPIO44 H6  
PCH\_GPIO56 P13

PCIECLKRQ5# / GPIO44

CLKOUT\_PEG\_B\_N  
CLKOUT\_PEG\_B\_P

PEG\_B\_CLKRQ# / GPIO56

PCIECLKRQ6# / GPIO45

CLKOUT\_PEG\_C\_N  
CLKOUT\_PEG\_C\_P

PEG\_C\_CLKRQ# / GPIO57

PCIECLKRQ7# / GPIO46

CLKOUT\_PEG\_D\_N  
CLKOUT\_PEG\_D\_P

PEG\_D\_CLKRQ# / GPIO58

PCIECLKRQ8# / GPIO47

CLKOUT\_PEG\_E\_N  
CLKOUT\_PEG\_E\_P

PEG\_E\_CLKRQ# / GPIO59

PCIECLKRQ9# / GPIO48

CLKOUT\_PEG\_F\_N  
CLKOUT\_PEG\_F\_P

PEG\_F\_CLKRQ# / GPIO60

PCIECLKRQ10# / GPIO49

CLKOUT\_PEG\_G\_N  
CLKOUT\_PEG\_G\_P

PEG\_G\_CLKRQ# / GPIO61

PCIECLKRQ11# / GPIO50

CLKOUT\_PEG\_H\_N  
CLKOUT\_PEG\_H\_P

PEG\_H\_CLKRQ# / GPIO62

PCIECLKRQ12# / GPIO51

CLKOUT\_PEG\_I\_N  
CLKOUT\_PEG\_I\_P

PEG\_I\_CLKRQ# / GPIO63

PCIECLKRQ13# / GPIO52

CLKOUT\_PEG\_J\_N  
CLKOUT\_PEG\_J\_P

PEG\_J\_CLKRQ# / GPIO64

PCIECLKRQ14# / GPIO53

CLKOUT\_PEG\_K\_N  
CLKOUT\_PEG\_K\_P

PEG\_K\_CLKRQ# / GPIO65

PCIECLKRQ15# / GPIO54

CLKOUT\_PEG\_L\_N  
CLKOUT\_PEG\_L\_P

PEG\_L\_CLKRQ# / GPIO66

PCIECLKRQ16# / GPIO55

CLKOUT\_PEG\_M\_N  
CLKOUT\_PEG\_M\_P

PEG\_M\_CLKRQ# / GPIO67

PCIECLKRQ17# / GPIO56

CLKOUT\_PEG\_N\_N  
CLKOUT\_PEG\_N\_P

PEG\_N\_CLKRQ# / GPIO68

PCIECLKRQ18# / GPIO57

CLKOUT\_PEG\_O\_N  
CLKOUT\_PEG\_O\_P

PEG\_O\_CLKRQ# / GPIO69

PCIECLKRQ19# / GPIO58

CLKOUT\_PEG\_P\_N  
CLKOUT\_PEG\_P\_P

PEG\_P\_CLKRQ# / GPIO70

PCIECLKRQ20# / GPIO59

CLKOUT\_PEG\_Q\_N  
CLKOUT\_PEG\_Q\_P

PEG\_Q\_CLKRQ# / GPIO71

PCIECLKRQ21# / GPIO60

CLKOUT\_PEG\_R\_N  
CLKOUT\_PEG\_R\_P

PEG\_R\_CLKRQ# / GPIO72

PCIECLKRQ22# / GPIO61

CLKOUT\_PEG\_S\_N  
CLKOUT\_PEG\_S\_P

PEG\_S\_CLKRQ# / GPIO73

PCIECLKRQ23# / GPIO62

CLKOUT\_PEG\_T\_N  
CLKOUT\_PEG\_T\_P

PEG\_T\_CLKRQ# / GPIO74

PCIECLKRQ24# / GPIO63

CLKOUT\_PEG\_U\_N  
CLKOUT\_PEG\_U\_P

PEG\_U\_CLKRQ# / GPIO75

PCIECLKRQ25# / GPIO64

CLKOUT\_PEG\_V\_N  
CLKOUT\_PEG\_V\_P

PEG\_V\_CLKRQ# / GPIO76

PCIECLKRQ26# / GPIO65

CLKOUT\_PEG\_W\_N  
CLKOUT\_PEG\_W\_P

PEG\_W\_CLKRQ# / GPIO77

PCIECLKRQ27# / GPIO66

CLKOUT\_PEG\_X\_N  
CLKOUT\_PEG\_X\_P

PEG\_X\_CLKRQ# / GPIO78

PCIECLKRQ28# / GPIO67

CLKOUT\_PEG\_Y\_N  
CLKOUT\_PEG\_Y\_P

PEG\_Y\_CLKRQ# / GPIO79

PCIECLKRQ29# / GPIO68

CLKOUT\_PEG\_Z\_N  
CLKOUT\_PEG\_Z\_P

PEG\_Z\_CLKRQ# / GPIO80

PCIECLKRQ30# / GPIO69

CLKOUT\_PEG\_AA\_N  
CLKOUT\_PEG\_AA\_P

PEG\_AA\_CLKRQ# / GPIO81

PCIECLKRQ31# / GPIO70

CLKOUT\_PEG\_AB\_N  
CLKOUT\_PEG\_AB\_P

PEG\_AB\_CLKRQ# / GPIO82

PCIECLKRQ32# / GPIO71

CLKOUT\_PEG\_AC\_N  
CLKOUT\_PEG\_AC\_P

PEG\_AC\_CLKRQ# / GPIO83

PCIECLKRQ33# / GPIO72

CLKOUT\_PEG\_AD\_N  
CLKOUT\_PEG\_AD\_P

PEG\_AD\_CLKRQ# / GPIO84

PCIECLKRQ34# / GPIO73

CLKOUT\_PEG\_AE\_N  
CLKOUT\_PEG\_AE\_P

PEG\_AE\_CLKRQ# / GPIO85

PCIECLKRQ35# / GPIO74

CLKOUT\_PEG\_AF\_N  
CLKOUT\_PEG\_AF\_P

PEG\_AF\_CLKRQ# / GPIO86

PCIECLKRQ36# / GPIO75

CLKOUT\_PEG\_AG\_N  
CLKOUT\_PEG\_AG\_P

PEG\_AG\_CLKRQ# / GPIO87

PCIECLKRQ37# / GPIO76

CLKOUT\_PEG\_AH\_N  
CLKOUT\_PEG\_AH\_P

PEG\_AH\_CLKRQ# / GPIO88

PCIECLKRQ38# / GPIO77

CLKOUT\_PEG\_AI\_N  
CLKOUT\_PEG\_AI\_P

PEG\_AI\_CLKRQ# / GPIO89

PCIECLKRQ39# / GPIO78

CLKOUT\_PEG\_AJ\_N  
CLKOUT\_PEG\_AJ\_P

PEG\_AJ\_CLKRQ# / GPIO90

PCIECLKRQ40# / GPIO79

CLKOUT\_PEG\_AK\_N  
CLKOUT\_PEG\_AK\_P

PEG\_AK\_CLKRQ# / GPIO91

PCIECLKRQ41# / GPIO80

CLKOUT\_PEG\_AL\_N  
CLKOUT\_PEG\_AL\_P

PEG\_AL\_CLKRQ# / GPIO92

PCIECLKRQ42# / GPIO81

CLKOUT\_PEG\_AM\_N  
CLKOUT\_PEG\_AM\_P

PEG\_AM\_CLKRQ# / GPIO93

PCIECLKRQ43# / GPIO82

CLKOUT\_PEG\_AN\_N  
CLKOUT\_PEG\_AN\_P

PEG\_AN\_CLKRQ# / GPIO94

PCIECLKRQ44# / GPIO83

CLKOUT\_PEG\_AO\_N  
CLKOUT\_PEG\_AO\_P

PEG\_AO\_CLKRQ# / GPIO95

PCIECLKRQ45# / GPIO84

CLKOUT\_PEG\_AP\_N  
CLKOUT\_PEG\_AP\_P

PEG\_AP\_CLKRQ# / GPIO96

PCIECLKRQ46# / GPIO85

CLKOUT\_PEG\_AQ\_N  
CLKOUT\_PEG\_AQ\_P

PEG\_AQ\_CLKRQ# / GPIO97

PCIECLKRQ47# / GPIO86

CLKOUT\_PEG\_AR\_N  
CLKOUT\_PEG\_AR\_P

PEG\_AR\_CLKRQ# / GPIO98

PCIECLKRQ48# / GPIO87

CLKOUT\_PEG\_AS\_N  
CLKOUT\_PEG\_AS\_P

PEG\_AS\_CLKRQ# / GPIO99

PCIECLKRQ49# / GPIO88

CLKOUT\_PEG\_AT\_N  
CLKOUT\_PEG\_AT\_P

PEG\_AT\_CLKRQ# / GPIO100

PCIECLKRQ50# / GPIO89

CLKOUT\_PEG\_AU\_N  
CLKOUT\_PEG\_AU\_P

PEG\_AU\_CLKRQ# / GPIO101

PCIECLKRQ51# / GPIO90

CLKOUT\_PEG\_AV\_N  
CLKOUT\_PEG\_AV\_P

PEG\_AV\_CLKRQ# / GPIO102

PCIECLKRQ52# / GPIO91

CLKOUT\_PEG\_AW\_N  
CLKOUT\_PEG\_AW\_P

PEG\_AW\_CLKRQ# / GPIO103

PCIECLKRQ53# / GPIO92

CLKOUT\_PEG\_AX\_N  
CLKOUT\_PEG\_AX\_P

PEG\_AX\_CLKRQ# / GPIO104

PCIECLKRQ54# / GPIO93

CLKOUT\_PEG\_AY\_N  
CLKOUT\_PEG\_AY\_P

PEG\_AY\_CLKRQ# / GPIO105

PCIECLKRQ55# / GPIO94

CLKOUT\_PEG\_AZ\_N  
CLKOUT\_PEG\_AZ\_P

PEG\_AZ\_CLKRQ# / GPIO106

PCIECLKRQ56# / GPIO95

CLKOUT\_PEG\_BA\_N  
CLKOUT\_PEG\_BA\_P

PEG\_BA\_CLKRQ# / GPIO107

PCIECLKRQ57# / GPIO96

CLKOUT\_PEG\_BB\_N  
CLKOUT\_PEG\_BB\_P

PEG\_BB\_CLKRQ# / GPIO108

PCIECLKRQ58# / GPIO97

CLKOUT\_PEG\_BC\_N  
CLKOUT\_PEG\_BC\_P

PEG\_BC\_CLKRQ# / GPIO109

PCIECLKRQ59# / GPIO98

CLKOUT\_PEG\_BD\_N  
CLKOUT\_PEG\_BD\_P

PEG\_BD\_CLKRQ# / GPIO110

PCIECLKRQ60# / GPIO99

CLKOUT\_PEG\_BE\_N  
CLKOUT\_PEG\_BE\_P

PEG\_BE\_CLKRQ# / GPIO111

PCIECLKRQ61# / GPIO100

CLKOUT\_PEG\_BF\_N  
CLKOUT\_PEG\_BF\_P

PEG\_BF\_CLKRQ# / GPIO112

PCIECLKRQ62# / GPIO101

CLKOUT\_PEG\_BG\_N  
CLKOUT\_PEG\_BG\_P

PEG\_BG\_CLKRQ# / GPIO113

PCIECLKRQ63# / GPIO102

CLKOUT\_PEG\_BH\_N  
CLKOUT\_PEG\_BH\_P

PEG\_BH\_CLKRQ# / GPIO114

PCIECLKRQ64# / GPIO103

CLKOUT\_PEG\_BI\_N  
CLKOUT\_PEG\_BI\_P

PEG\_BI\_CLKRQ# / GPIO115

PCIECLKRQ65# / GPIO104

CLKOUT\_PEG\_BJ\_N  
CLKOUT\_PEG\_BJ\_P

PEG\_BJ\_CLKRQ# / GPIO116

PCIECLKRQ66# / GPIO105

CLKOUT\_PEG\_BK\_N  
CLKOUT\_PEG\_BK\_P

PEG\_BK\_CLKRQ# / GPIO117

PCIECLKRQ67# / GPIO106

CLKOUT\_PEG\_BL\_N  
CLKOUT\_PEG\_BL\_P

PEG\_BL\_CLKRQ# / GPIO118

PCIECLKRQ68# / GPIO107

CLKOUT\_PEG\_BM\_N  
CLKOUT\_PEG\_BM\_P

PEG\_BM\_CLKRQ# / GPIO119

PCIECLKRQ69# / GPIO108

CLKOUT\_PEG\_BN\_N  
CLKOUT\_PEG\_BN\_P

PEG\_BN\_CLKRQ# / GPIO120

PCIECLKRQ70# / GPIO109

CLKOUT\_PEG\_BO\_N  
CLKOUT\_PEG\_BO\_P

PEG\_BO\_CLKRQ# / GPIO121

PCIECLKRQ71# / GPIO110

CLKOUT\_PEG\_BP\_N  
CLKOUT\_PEG\_BP\_P

PEG\_BP\_CLKRQ# / GPIO122

PCIECLKRQ72# / GPIO111

CLKOUT\_PEG\_BQ\_N  
CLKOUT\_PEG\_BQ\_P

PEG\_BQ\_CLKRQ# / GPIO123

PCIECLKRQ73# / GPIO112

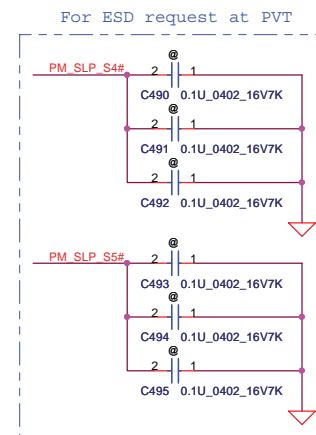
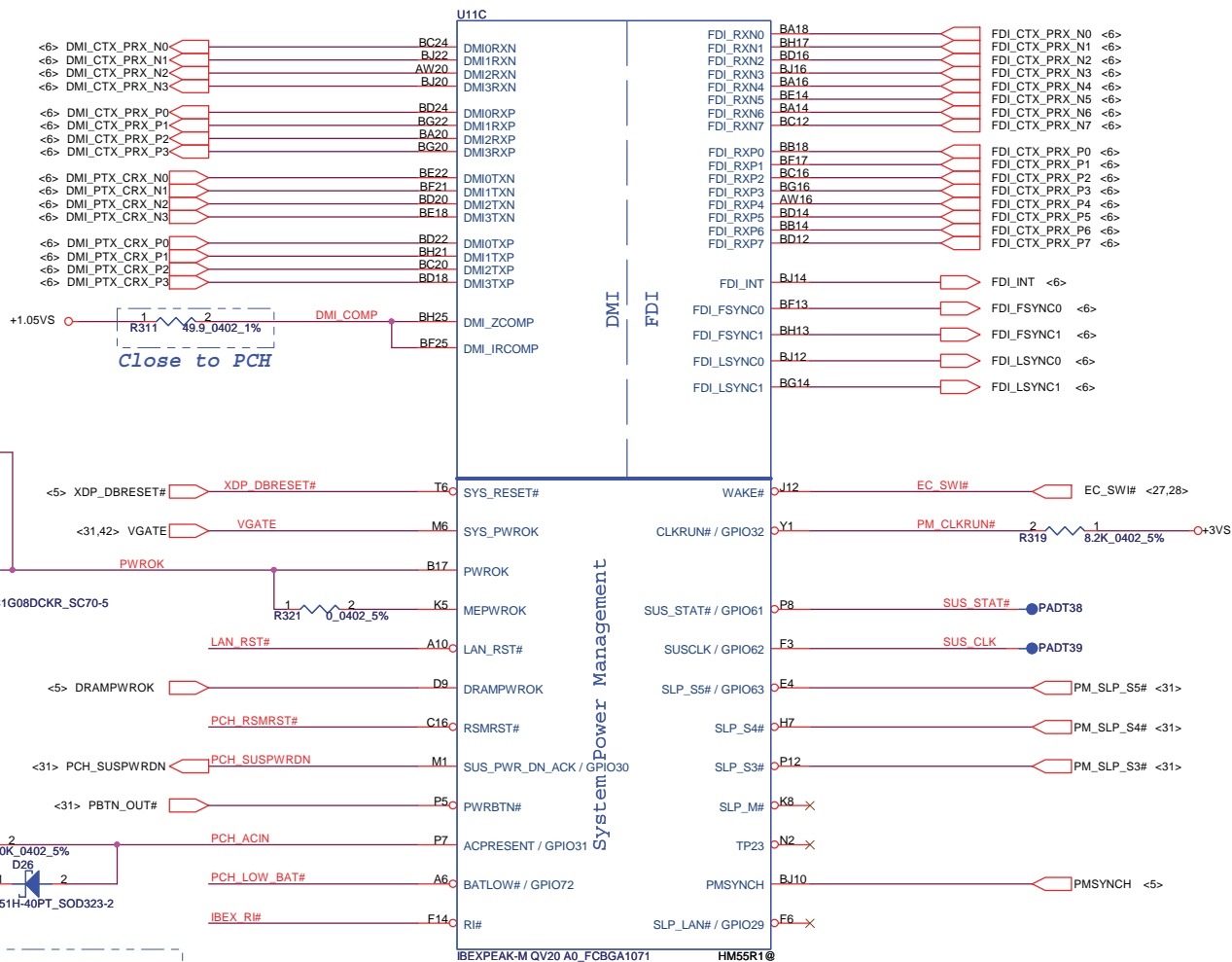
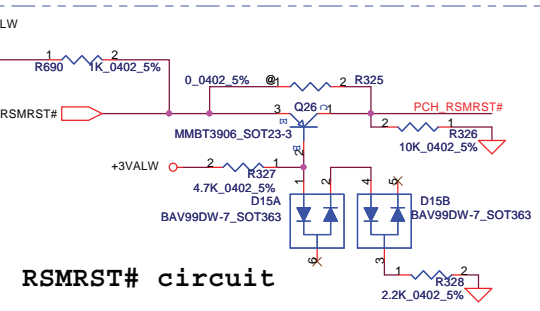
CLKOUT\_PEG\_BR\_N  
CLKOUT\_PEG\_BR\_P

PEG\_BR\_CLKRQ# / GPIO124

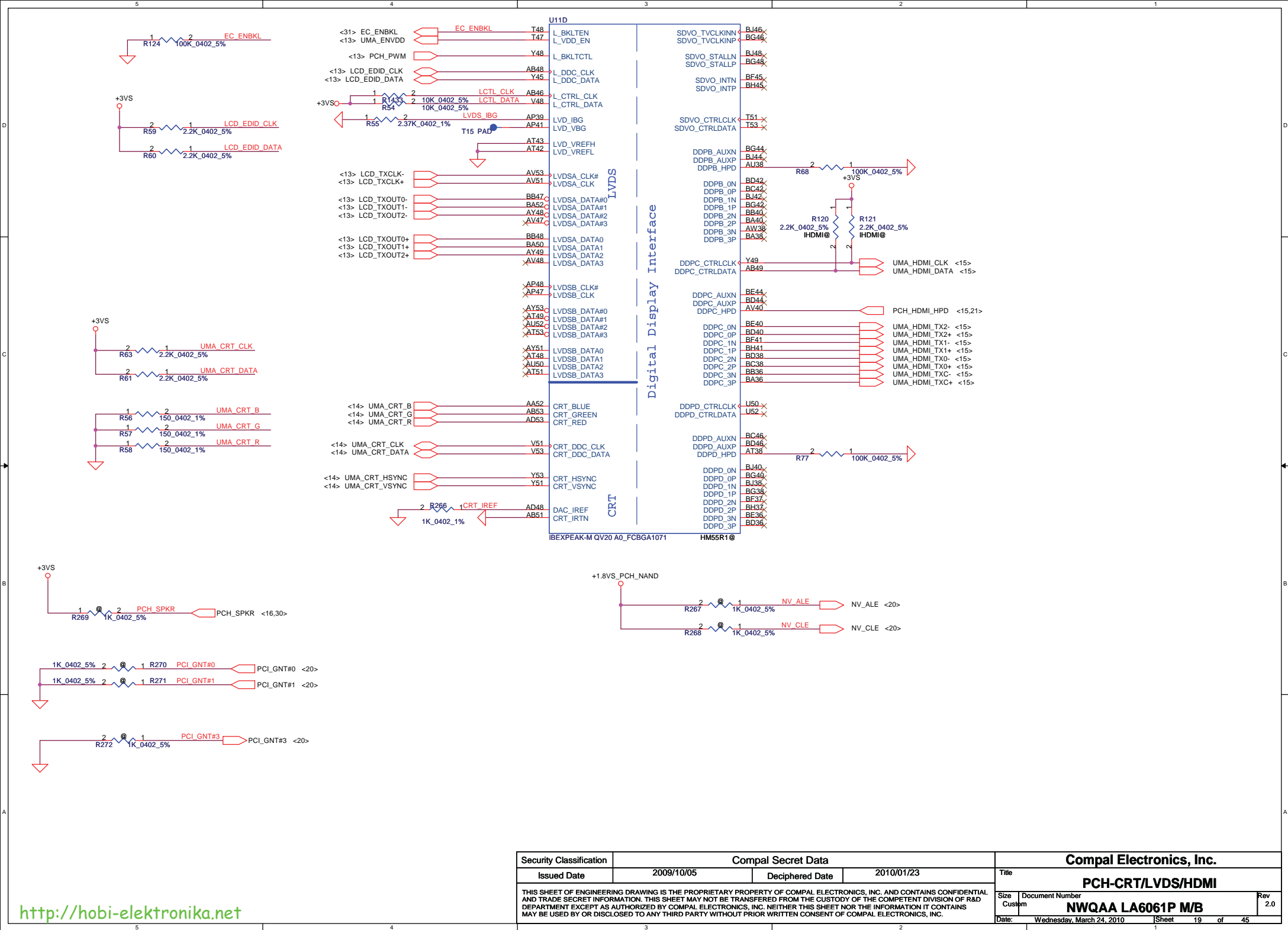
PCIECLKRQ74# / GPIO113

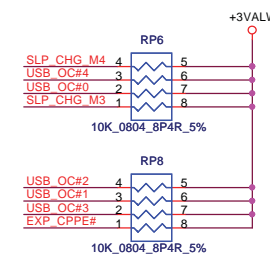
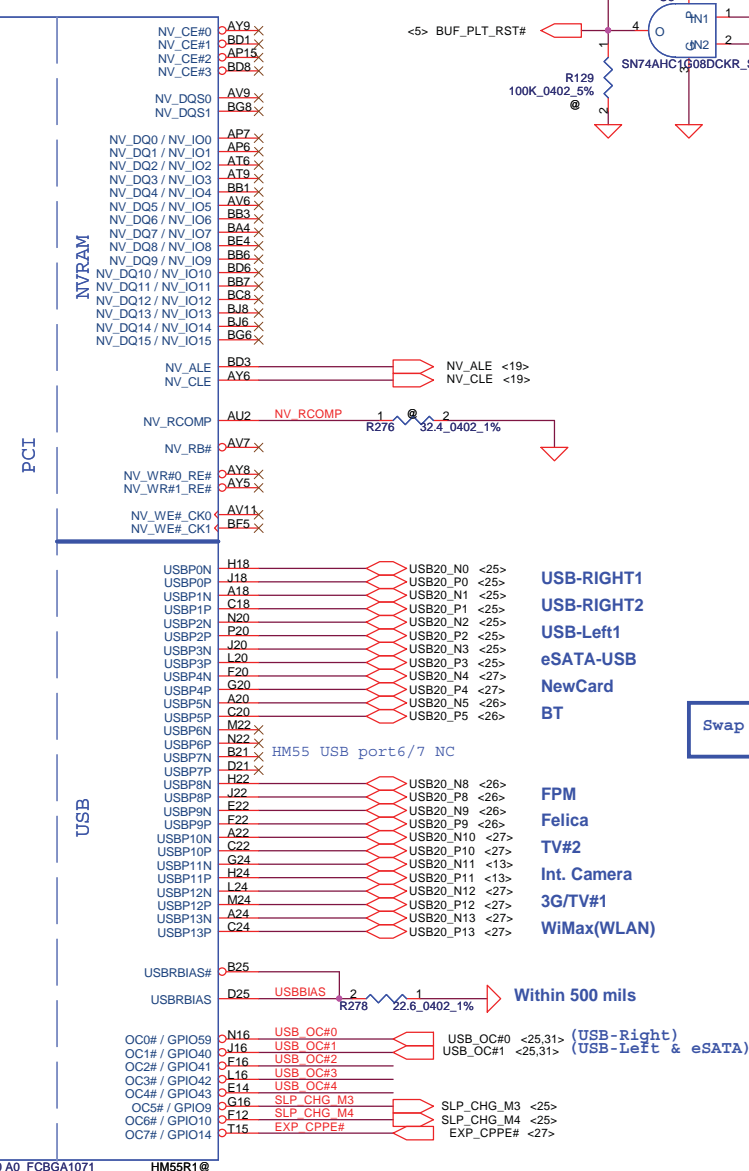
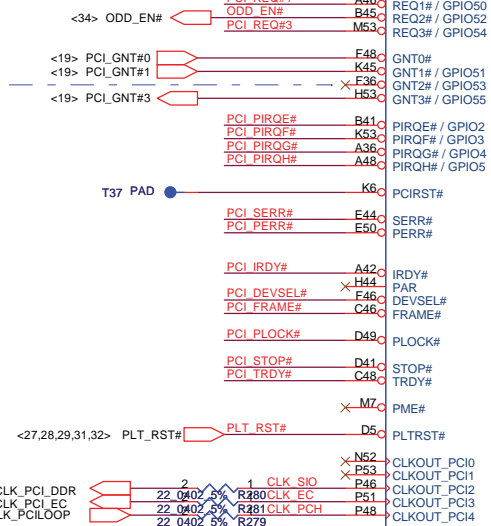
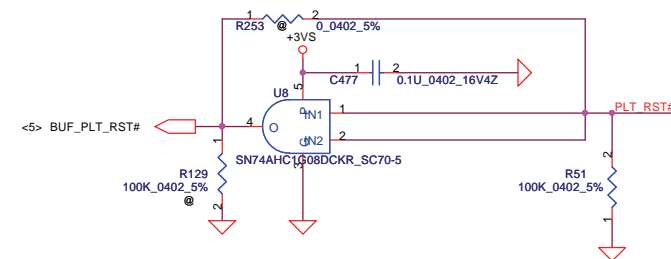
CLKOUT\_PEG\_BS\_N  
CLKOUT\_PEG\_BS\_P

PEG\_BS\_CLKRQ# / GPIO125



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				Size B	Document Number	Rev 2.0
				NWQAA LA6061P M/B		
				Date	Wednesday, March 24, 2010	Sheet 18 of 45





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				Size B	Document Number	Rev 2.0
				<b>NWQAA LA6061P M/B</b>		
Date: Wednesday, March 24, 2010				Sheet 20 of 45		

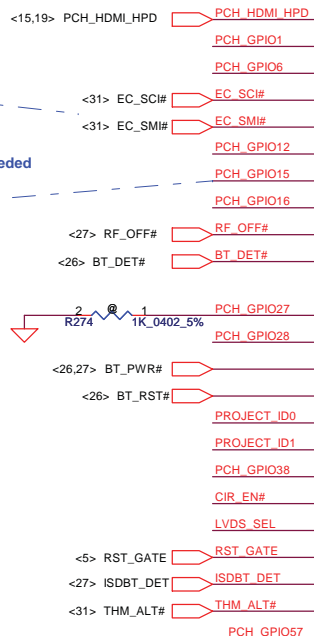
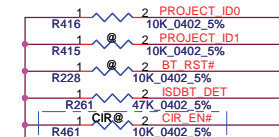
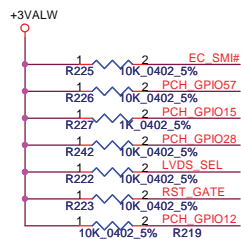
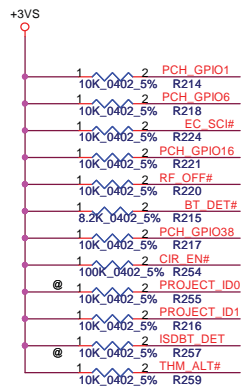
# GPIO8 Not pull down

Internal: Pull up 20k  
During Reset: High  
Initial: High

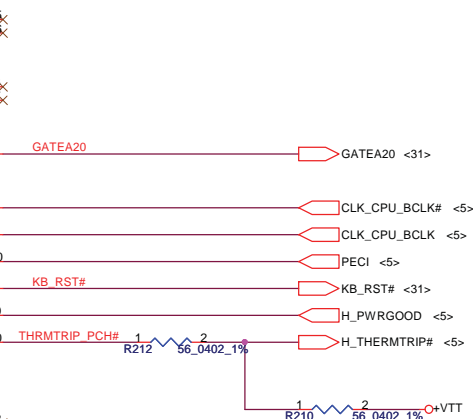
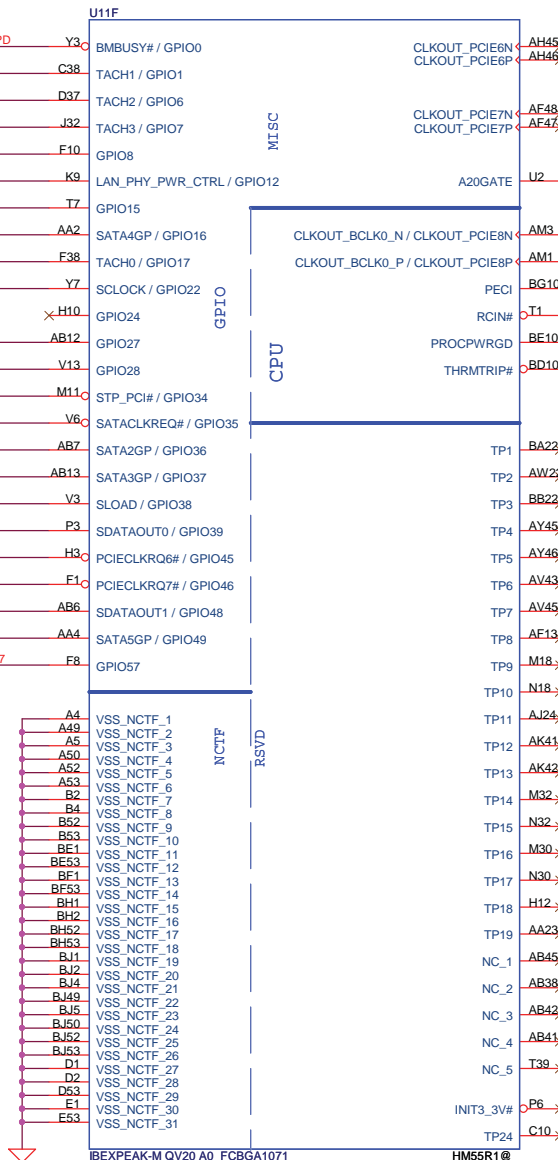
GPIO15  
a Strong pull up may be needed  
for GPIO Functionality  
Internal: Pull down 20k  
During Reset: Low  
Initial: Low

## On-Die PLL VR

PCH\_GPIO27 High = Enabled (Default)  
Low = Disabled



LVDS\_SEL=H  
for Single Channel LVDS



TP1

TP2

TP3

TP4

TP5

TP6

TP7

TP8

TP9

TP10

TP11

TP12

TP13

TP14

TP15

TP16

TP17

TP18

TP19

NC\_1

NC\_2

NC\_3

NC\_4

NC\_5

INIT3\_3V#

TP24

HM55R1@

TP25

TP26

TP27

TP28

TP29

TP30

TP31

TP32

TP33

TP34

TP35

TP36

TP37

TP38

TP39

TP40

TP41

TP42

TP43

TP44

TP45

TP46

TP47

TP48

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TP106

TP107

TP108

TP109

TP110

TP111

TP112

TP113

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TP115

TP116

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TP202

TP203

TP204

TP205

TP206

TP207

TP208

TP209

TP210

TP211

TP212

TP213

TP214

TP215

TP216

TP217

TP218

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TP220

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TP240

TP241

TP242

TP243

TP244

TP245

TP246

TP247

TP248

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TP252

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TP254

TP255

TP256

TP257

TP258

TP259

TP260

TP261

TP262

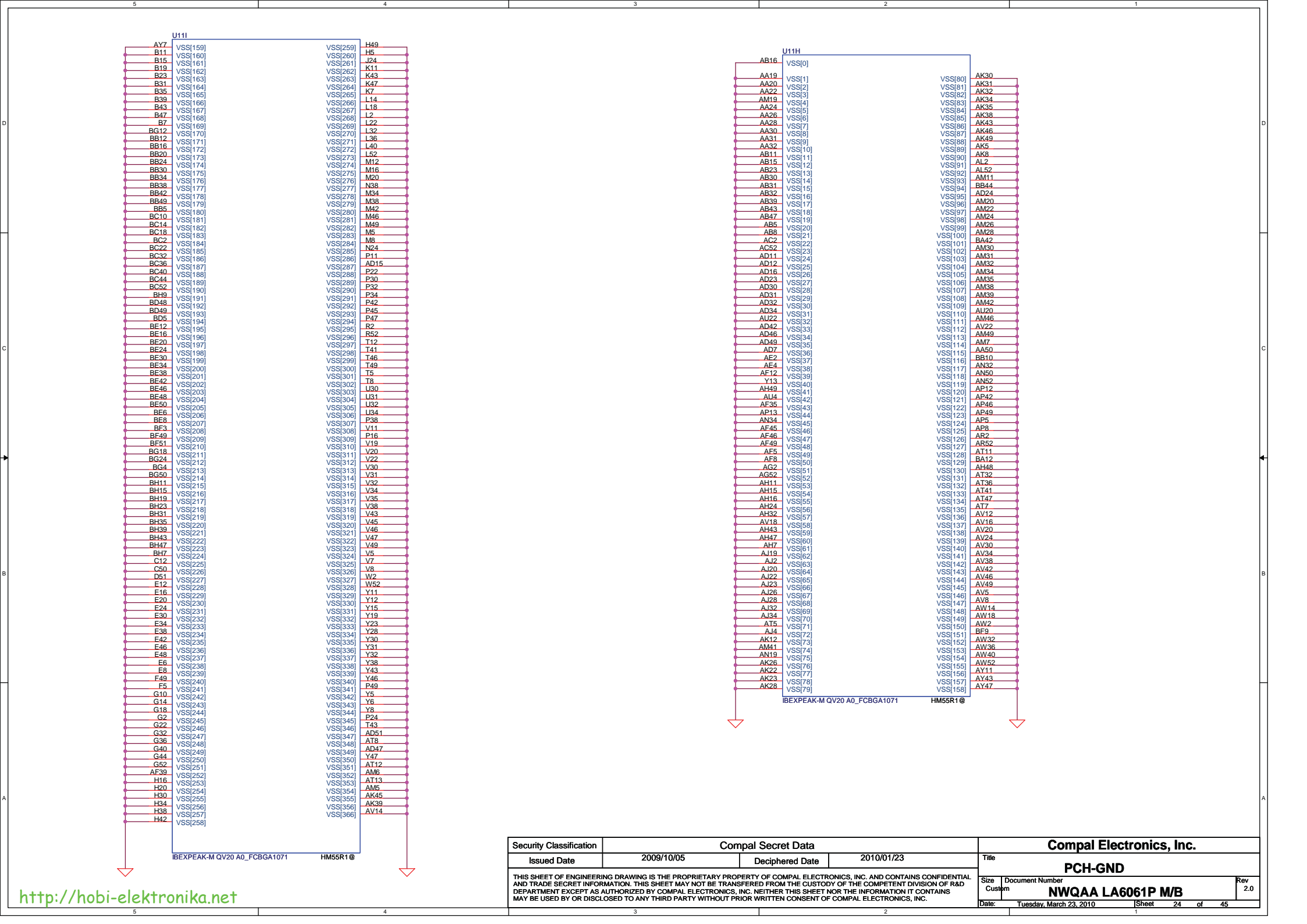
TP263

TP264







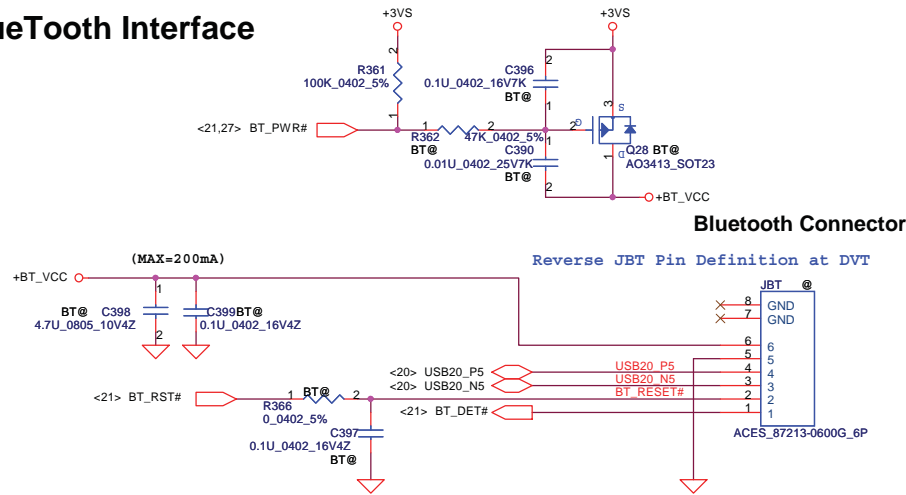


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Size	Document Number	Rev		2.0	
Custom	NWQAA LA6061P M/B	Date:		Tuesday, March 23, 2010	
Sheet		24		of 45	

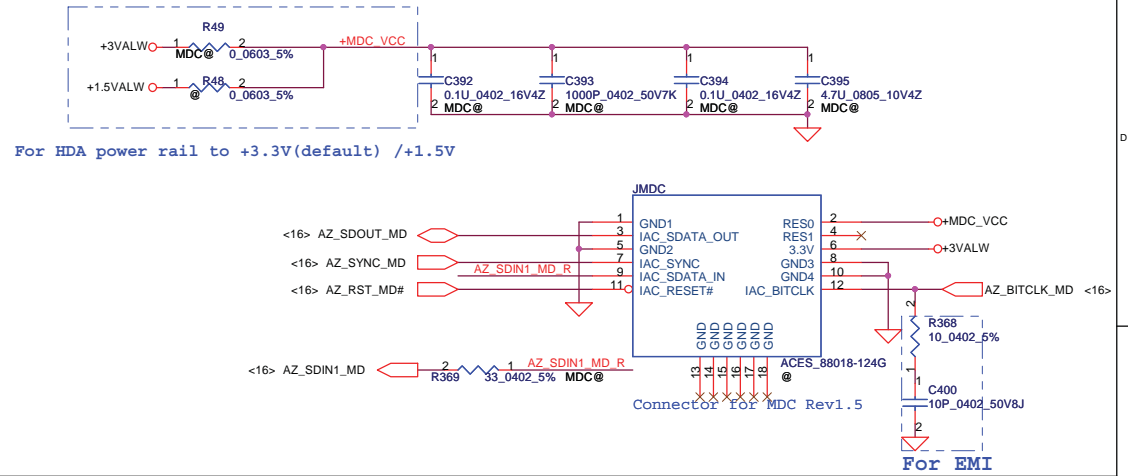




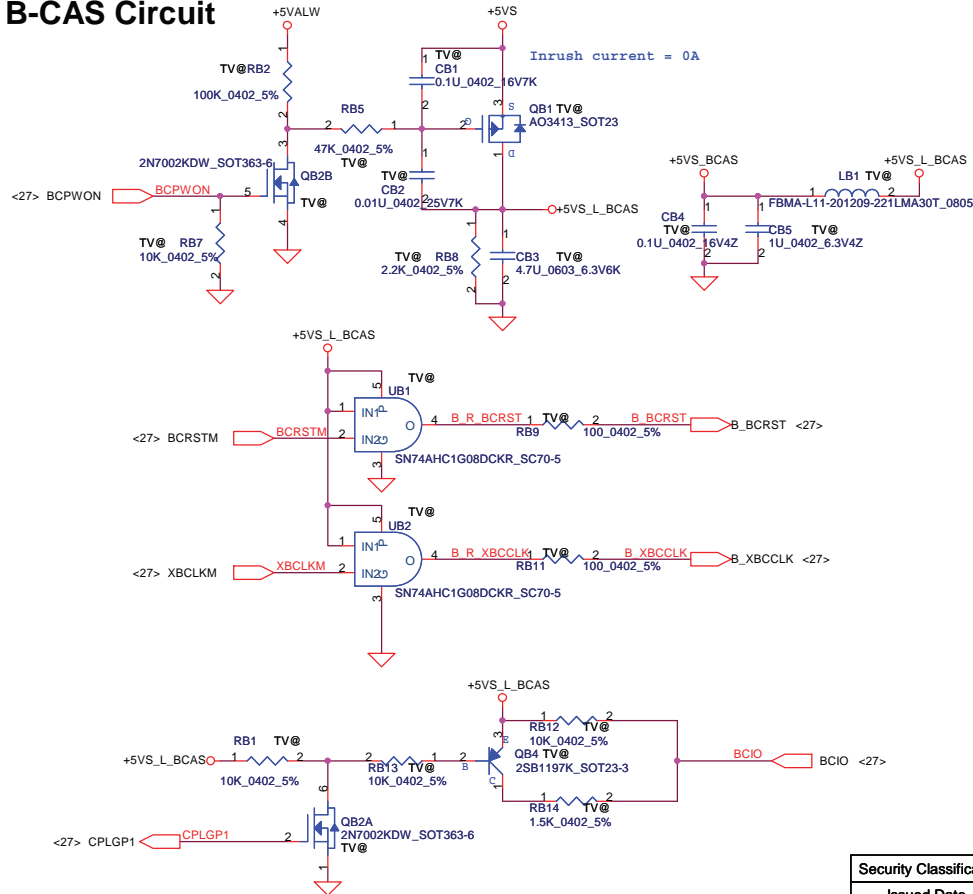
## BlueTooth Interface



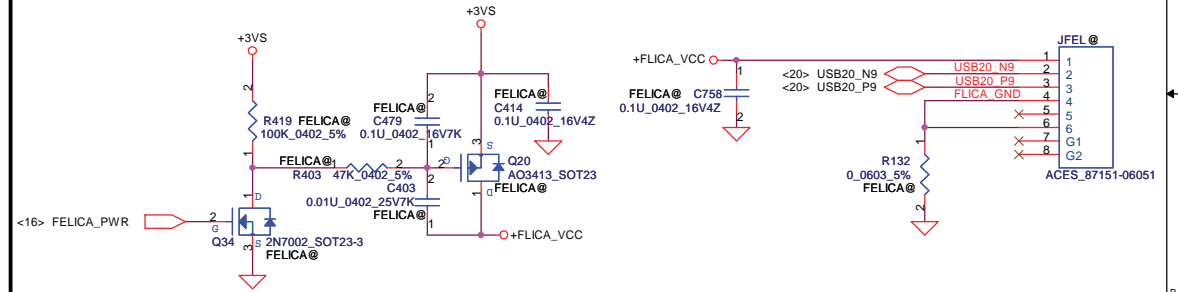
## MDC 1.5 Conn.



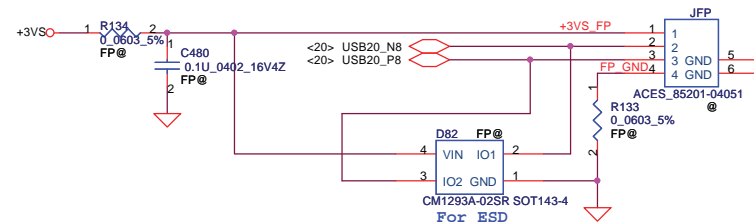
## B-CAS Circuit



## Felica

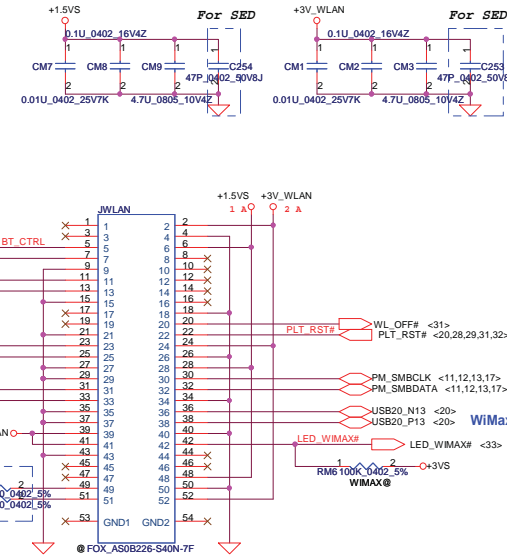
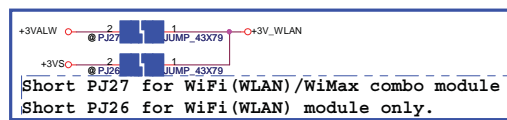
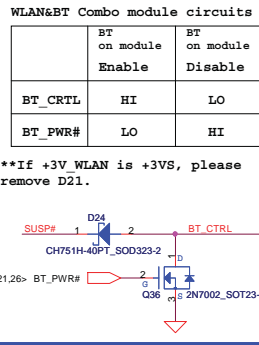


## Finger printer

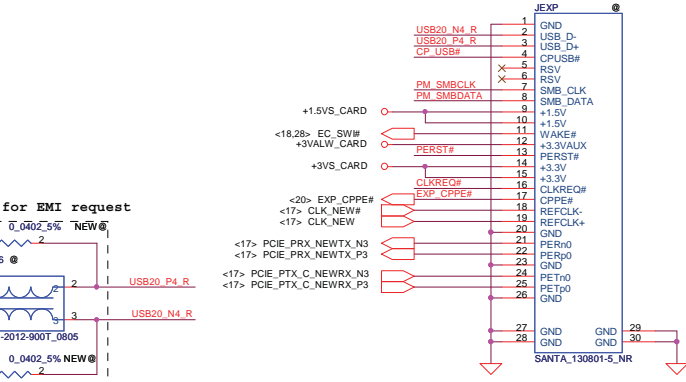
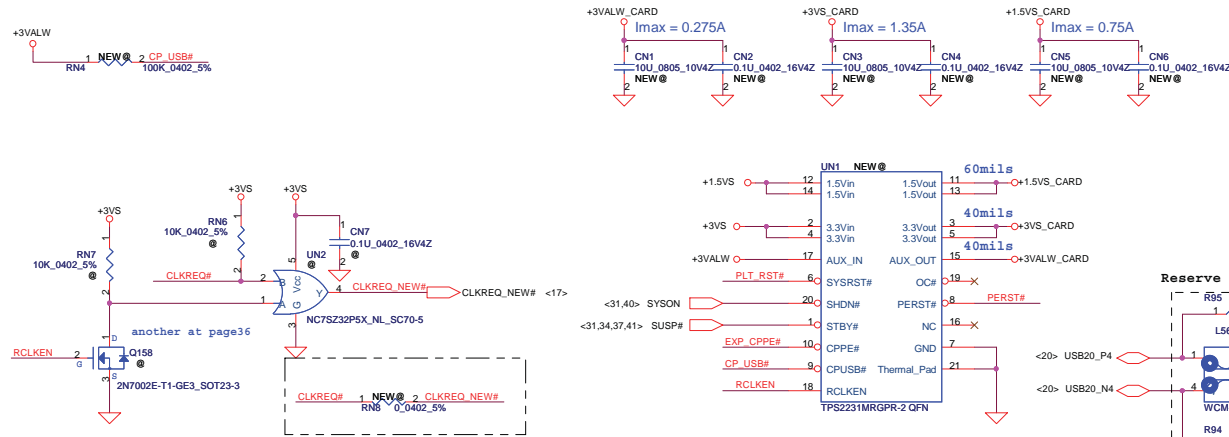
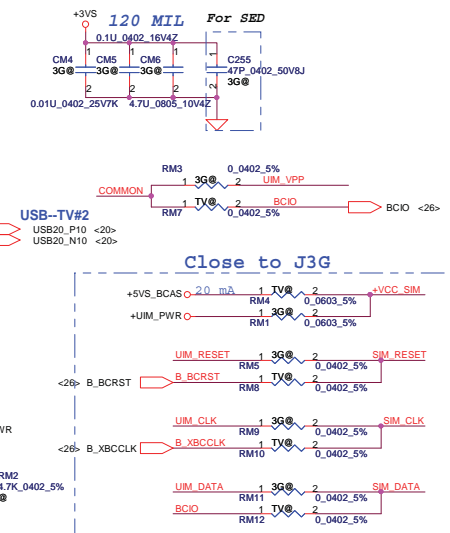
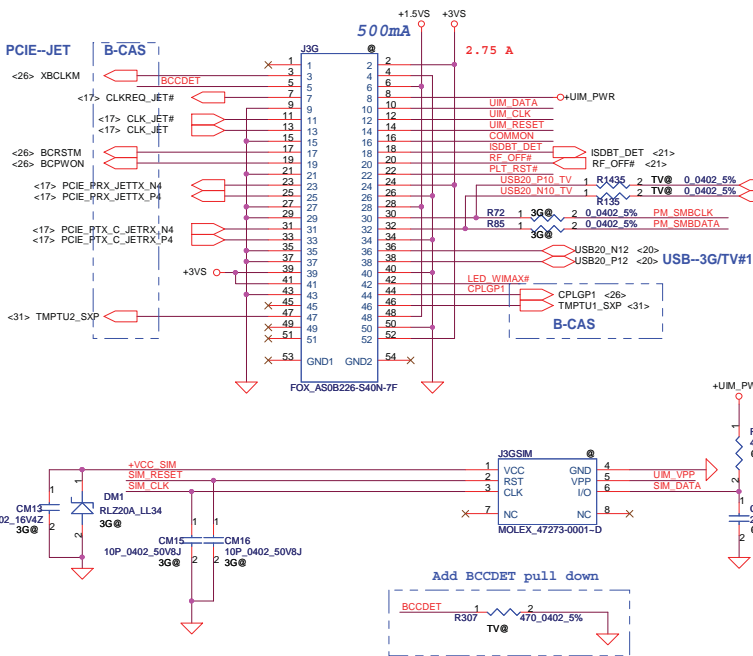


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						Size		Document Number		Rev	
								NWQAA LA6061P M/B		2.0	
						Date:		Wednesday, March 24, 2010		Sheet 26 of 45	

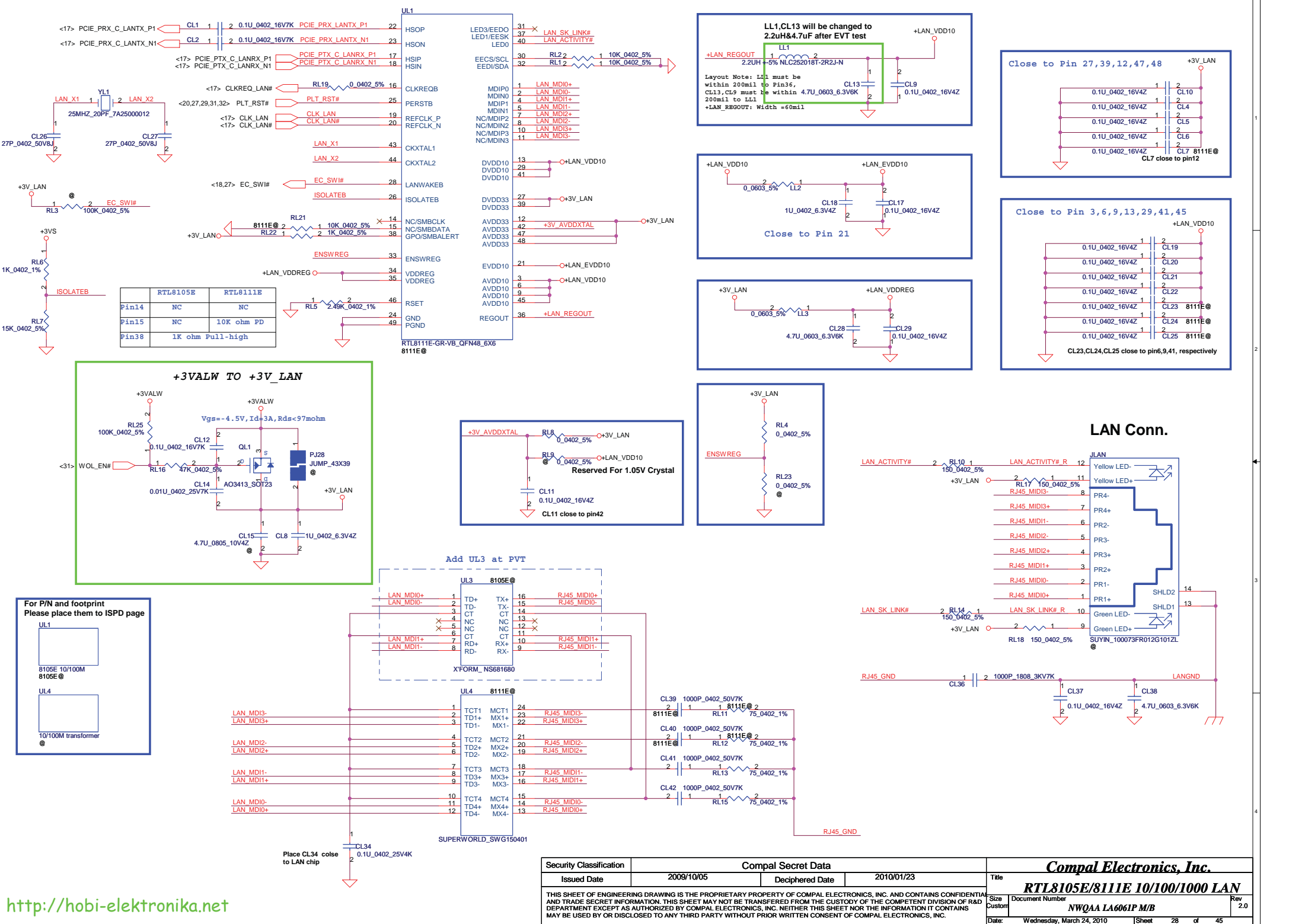
# Slot#1 Half PCIe Mini Card-WLAN/WiMax



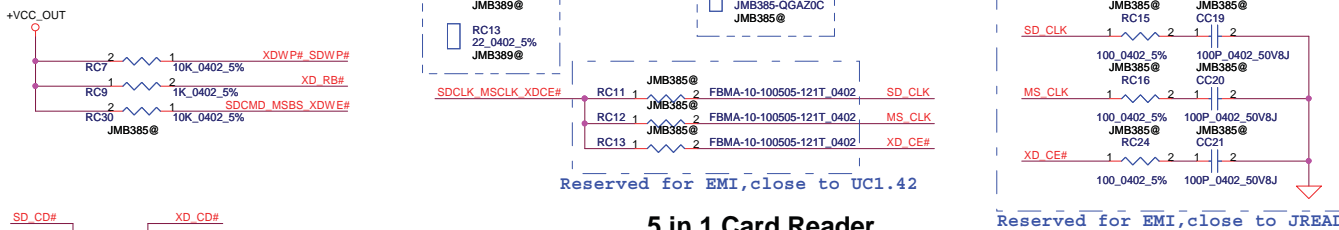
# Slot 2 Half & Full PCIe Mini Card- 3G/ JET/ TV Tuner



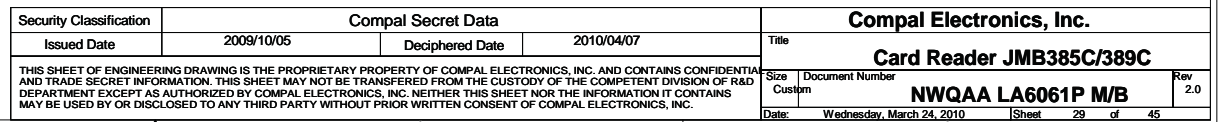
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				2.0
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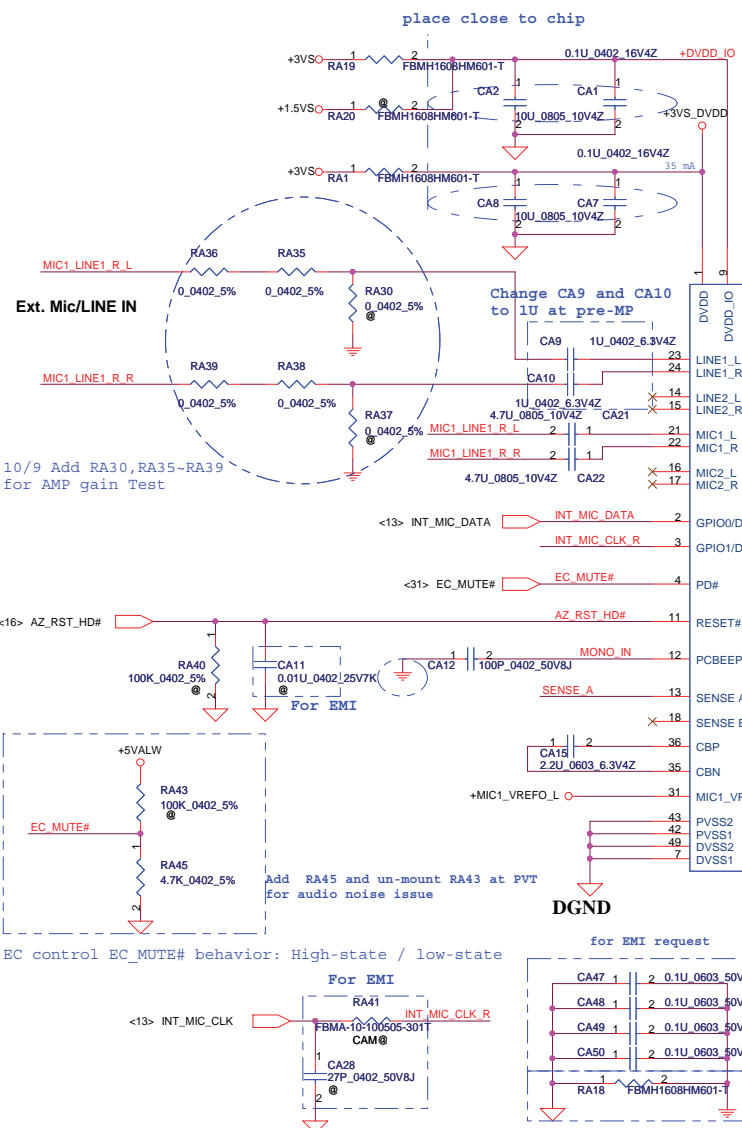


UC2 JMB389©



## MS



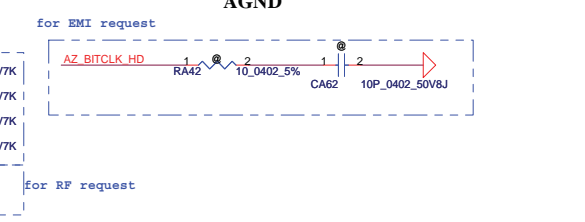
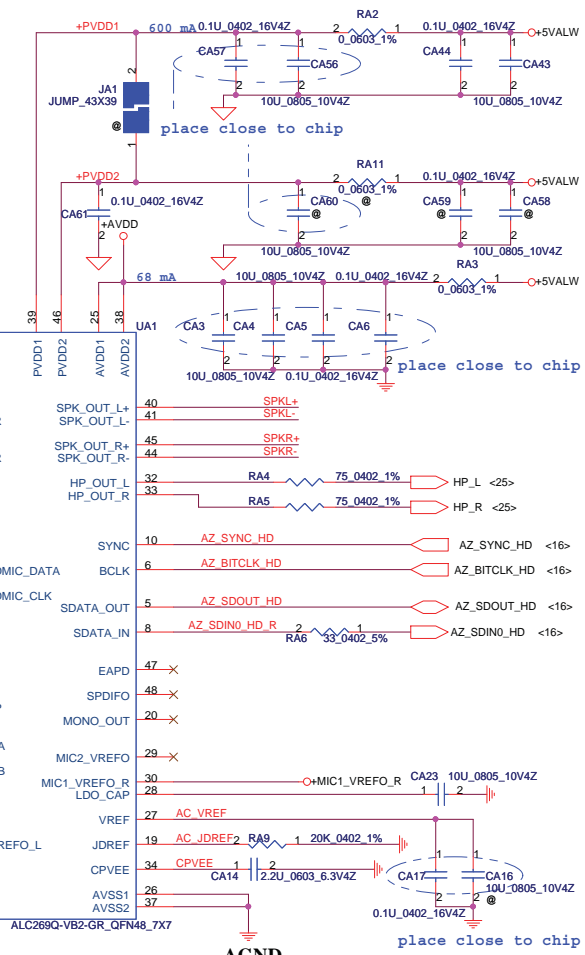
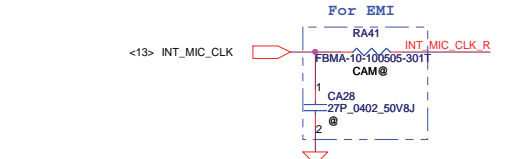


Ext. Mic/LINE IN

10/9 Add RA30, RA35-RA39 for AMP gain Test

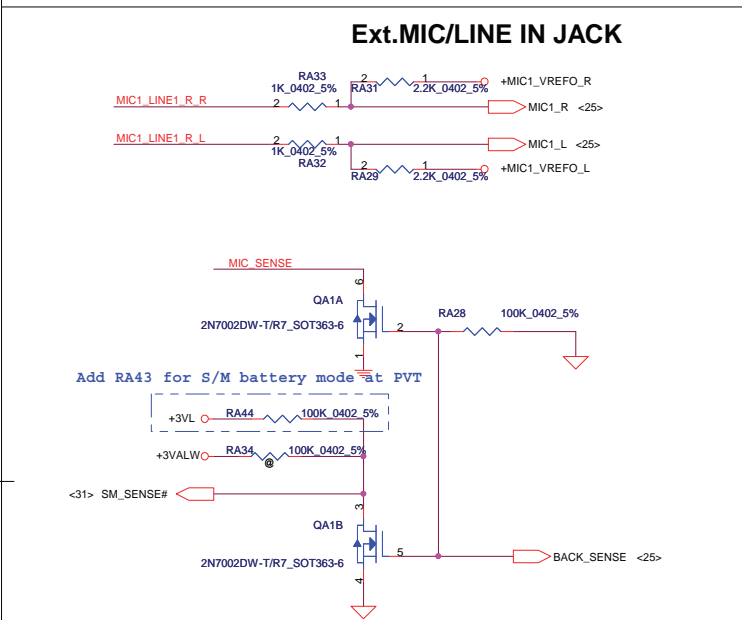
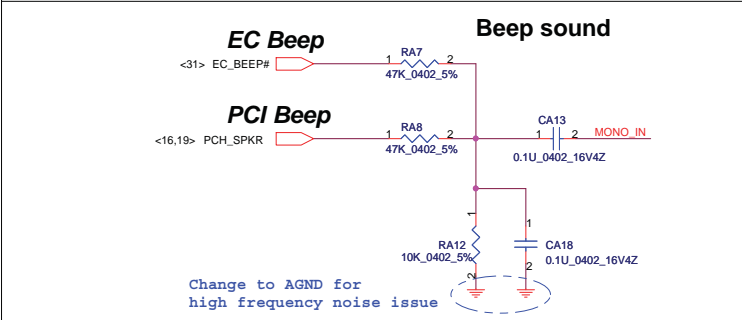
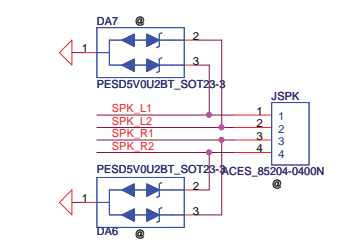
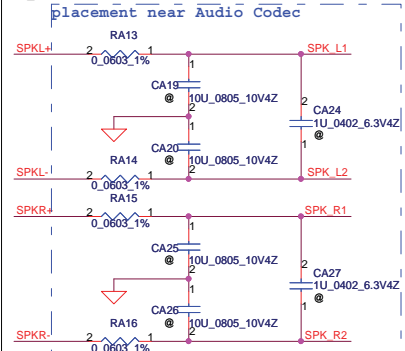
EC\_MUTE#

EC control EC\_MUTE# behavior: High-state / low-state

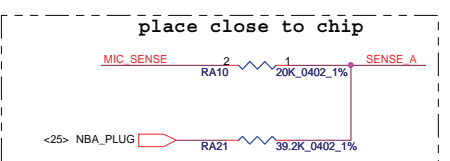


## Speaker Connector

10/20 Change LA6-LA9 to 0 ohm resistor

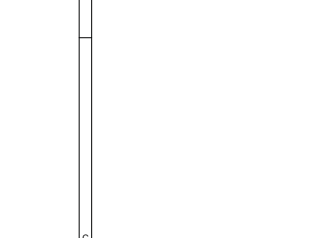
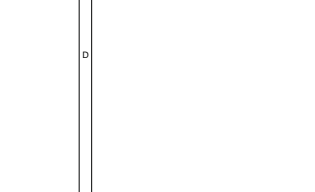
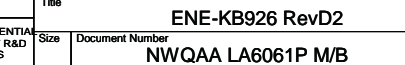
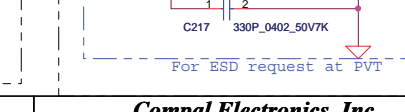
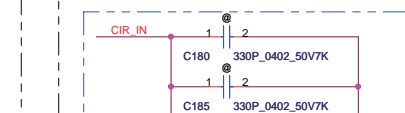
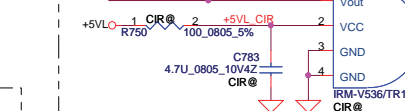
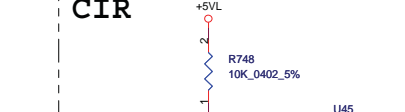
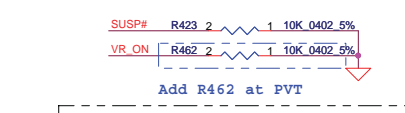
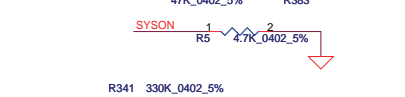
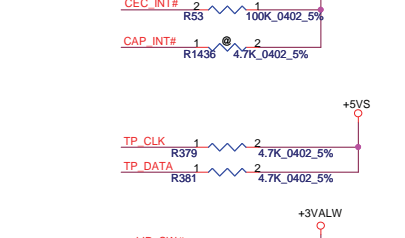
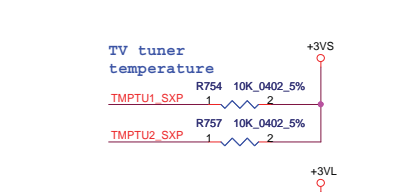
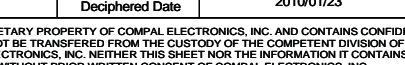
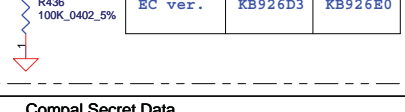
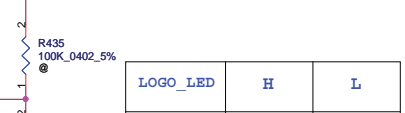
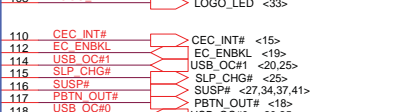
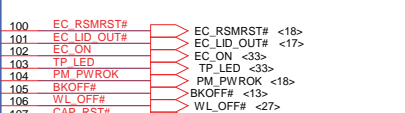
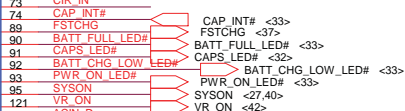
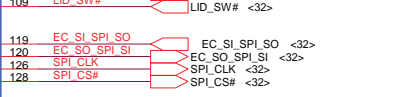
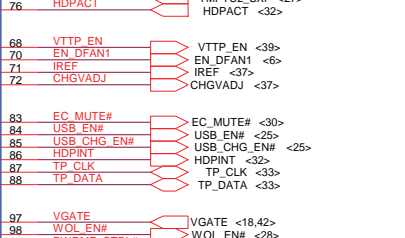
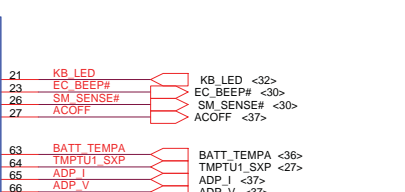
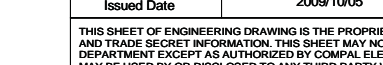
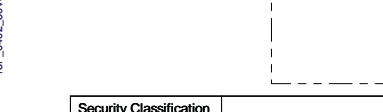
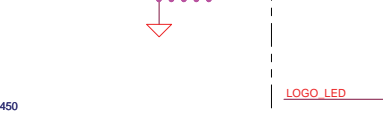
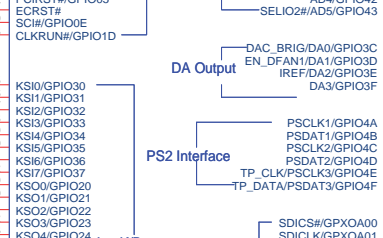
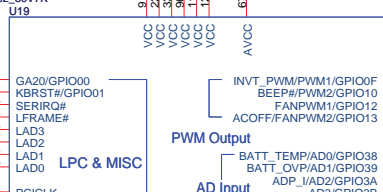
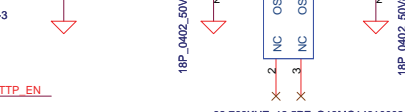
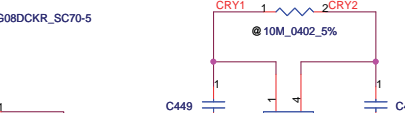
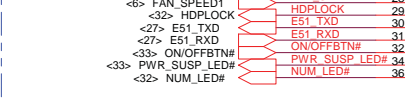
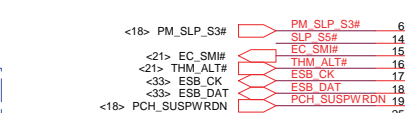
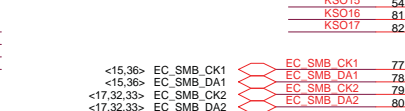
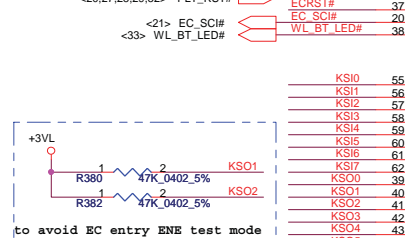
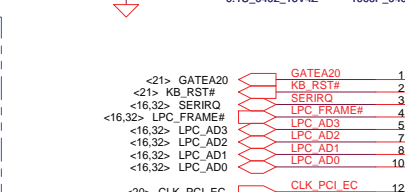
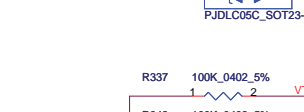
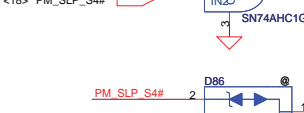
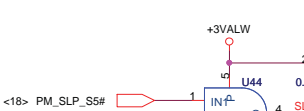
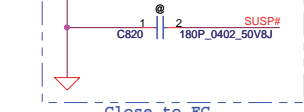
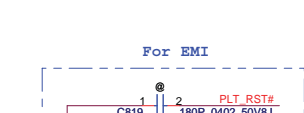
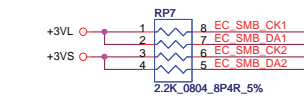
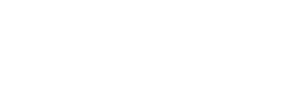
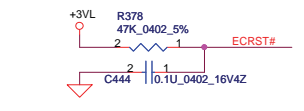
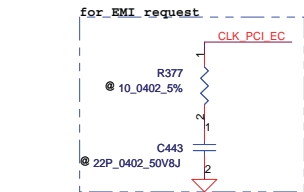


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	



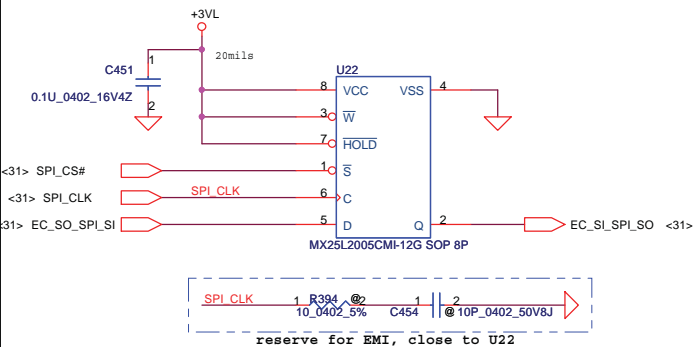
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Size	Document Number	NWQAA LA6061P M/B		Rev 2.0
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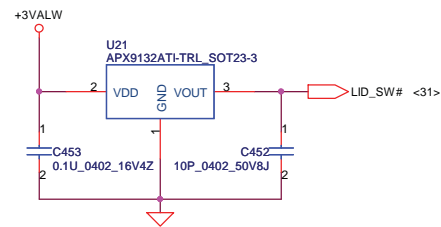


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2009/10/05		2010/01/23		Size	
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				NWQAA LA6061P M/B	
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				2.0	
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				of	
				45	

## SPI Flash (256KB)

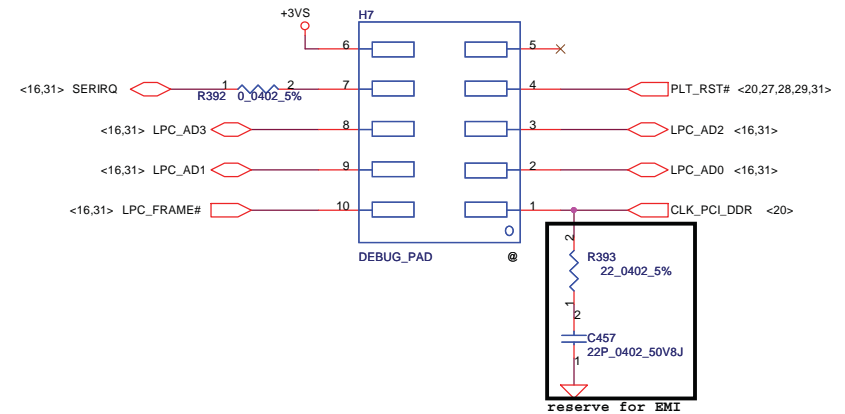


## Lid SW

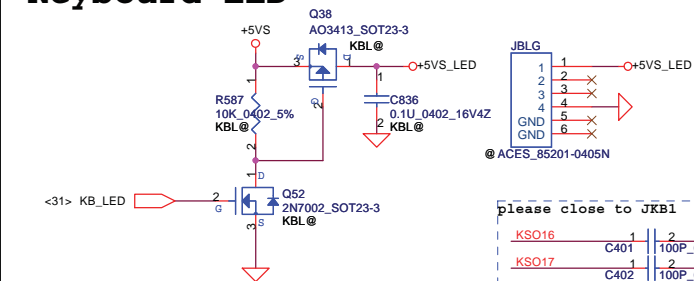


## LPC Debug Port

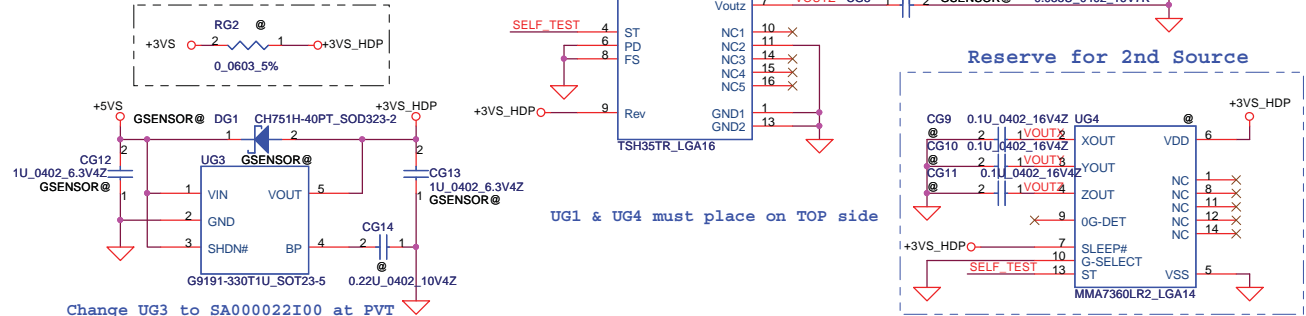
Please place the PAD under DDR DIMM.



## Keyboard LED



## G-Sensor



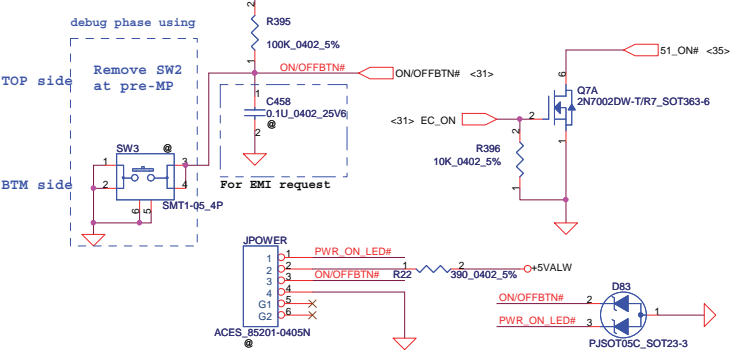
## KEYBOARD CONN.



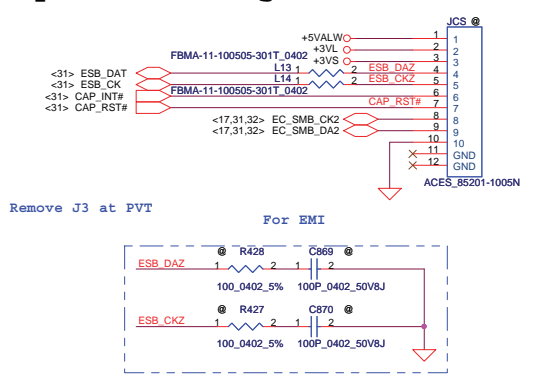
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Issued Date	2009/10/05	Deciphered Date	2010/01/23	Title	SPI ROM/TP/KB/Debug	
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				Date:	Wednesday, March 24, 2010	Sheet 32 of 45



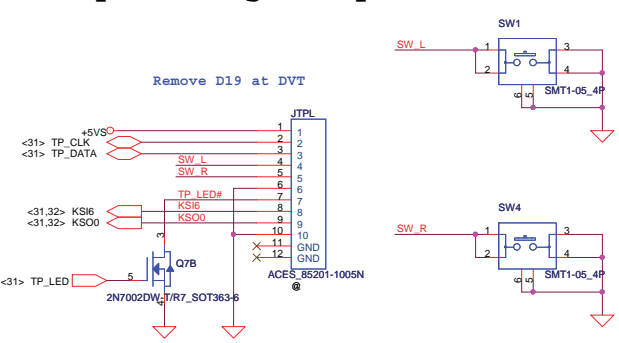
Power Button



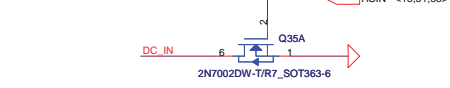
Caps Sensor/Light Sensor Conn.



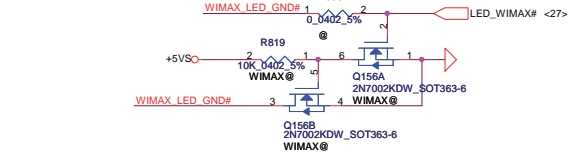
Touchpad & Light Pipe Connector



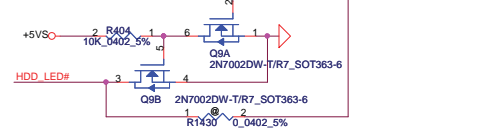
DC-IN LED



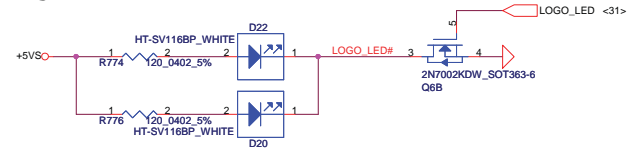
WiMAX LED



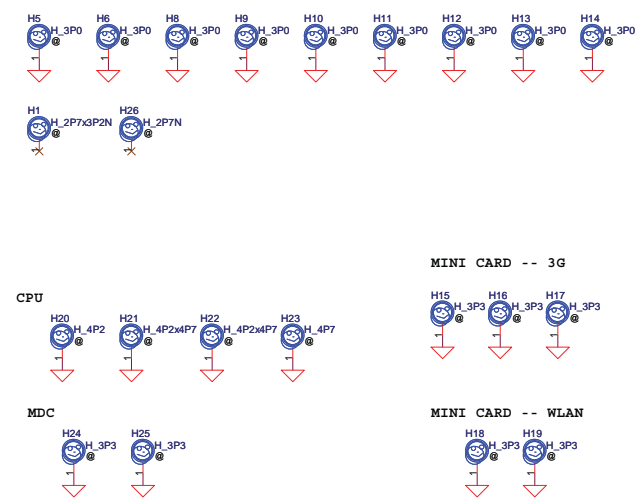
HDD LED



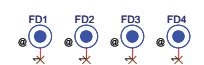
Logo LED



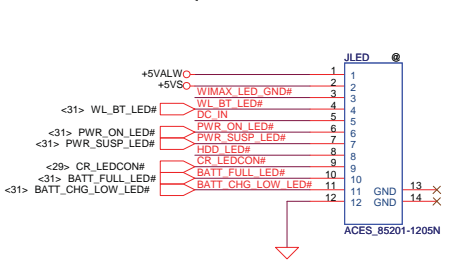
Screw Hole



PCB Fedical Mark PAD



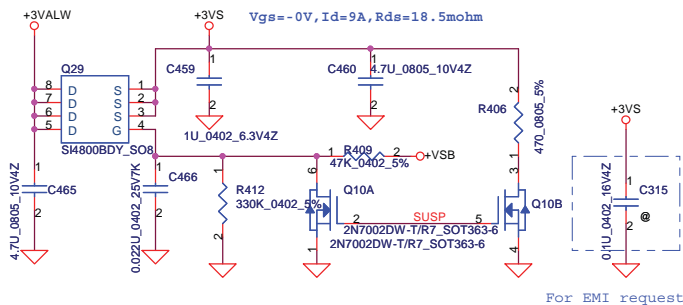
LED/B Connector



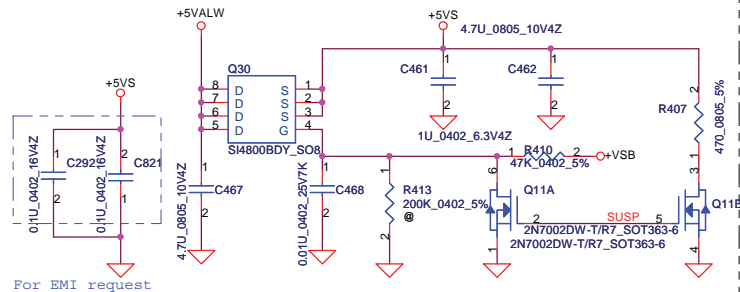
ISPD



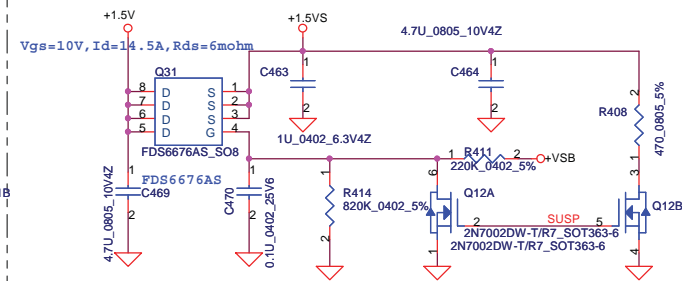
### +3VALW TO +3VS



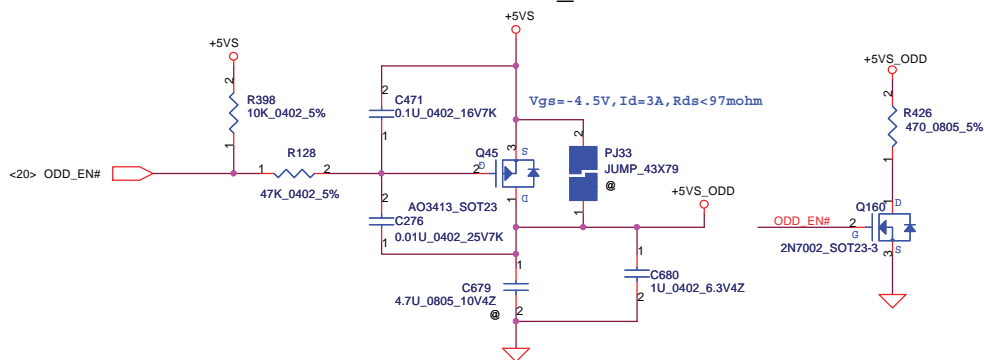
### +5VALW TO +5VS



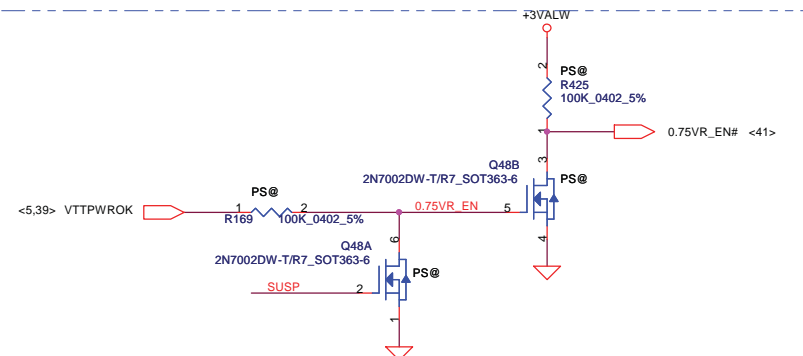
### +1.5V to +1.5VS



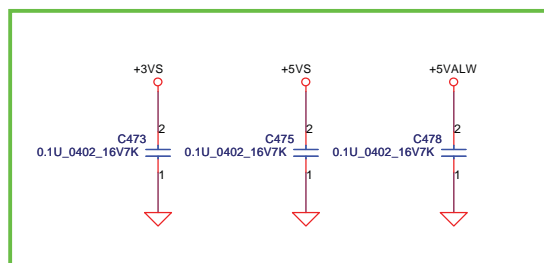
### +5VS TO +5VS\_ODD



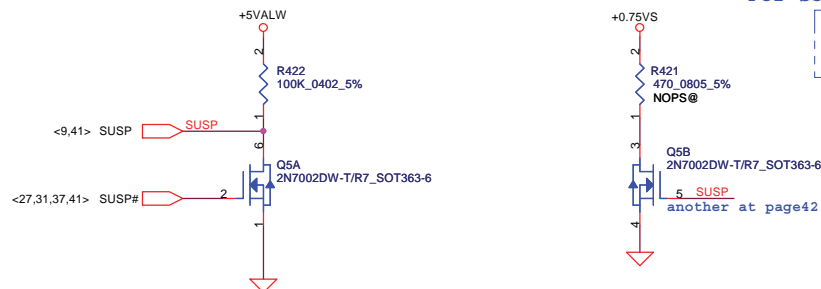
### For S3 CPU Power Saving



### Reserve for EMI test

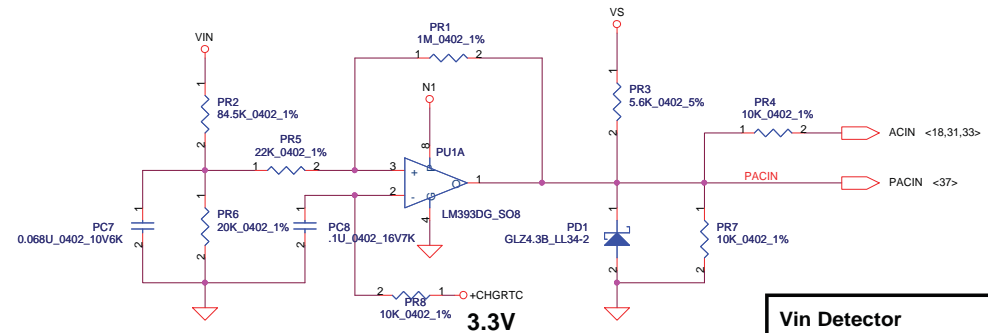
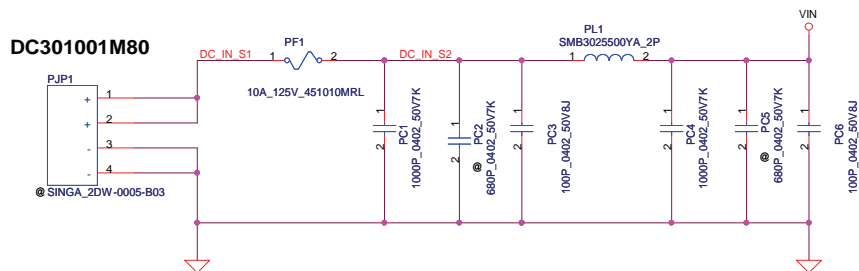


### For S3 CPU Power Saving



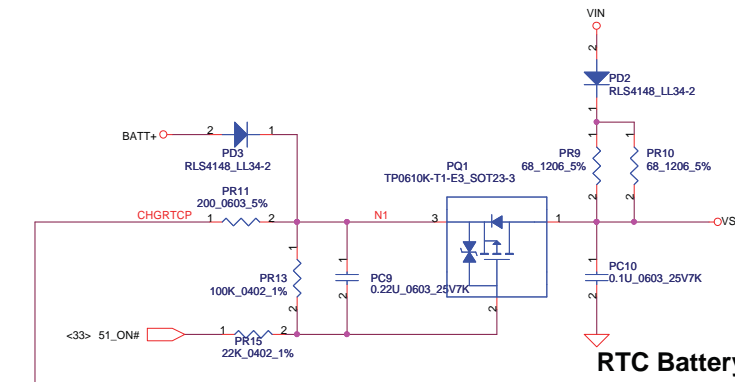
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/10/05	Deciphered Date	2010/01/23	Title	
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Size	Document Number	Rev			2.0
Date	Wednesday, March 24, 2010	Sheet	34	of	45

# DC301001M80



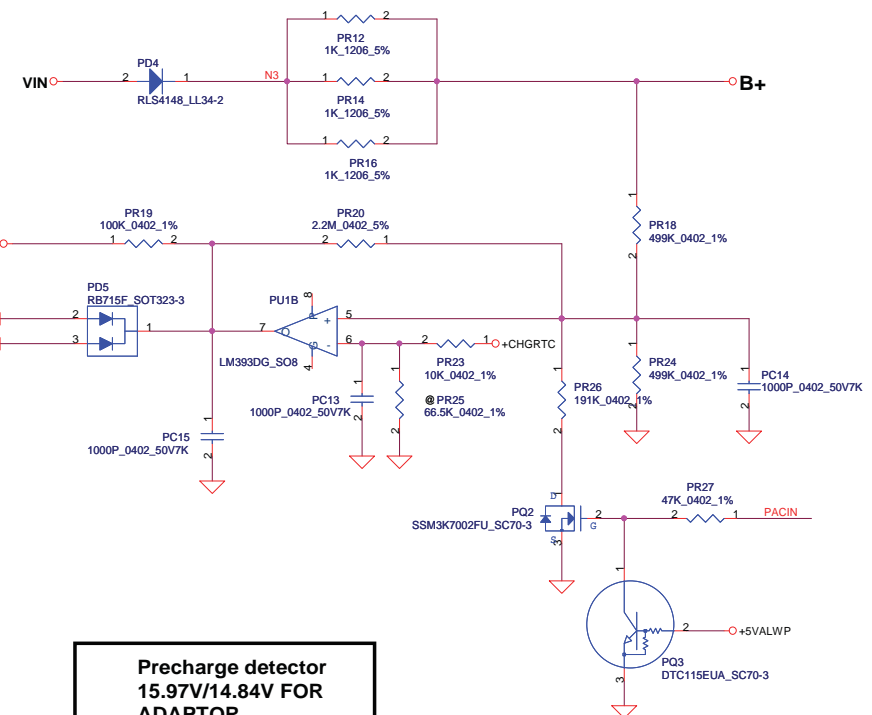
## Vin Detector

High 18.384 17.901 17.430  
Low 17.728 17.257 16.976

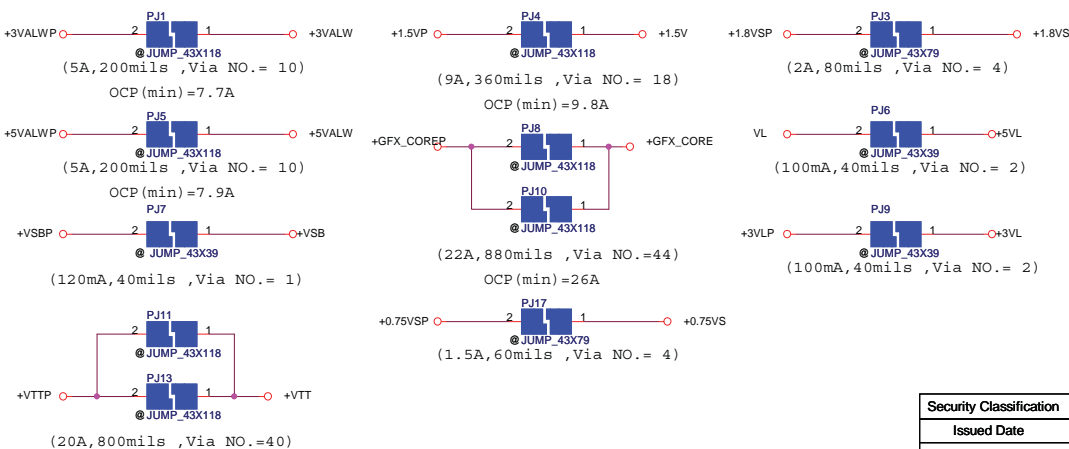


## RTC Battery

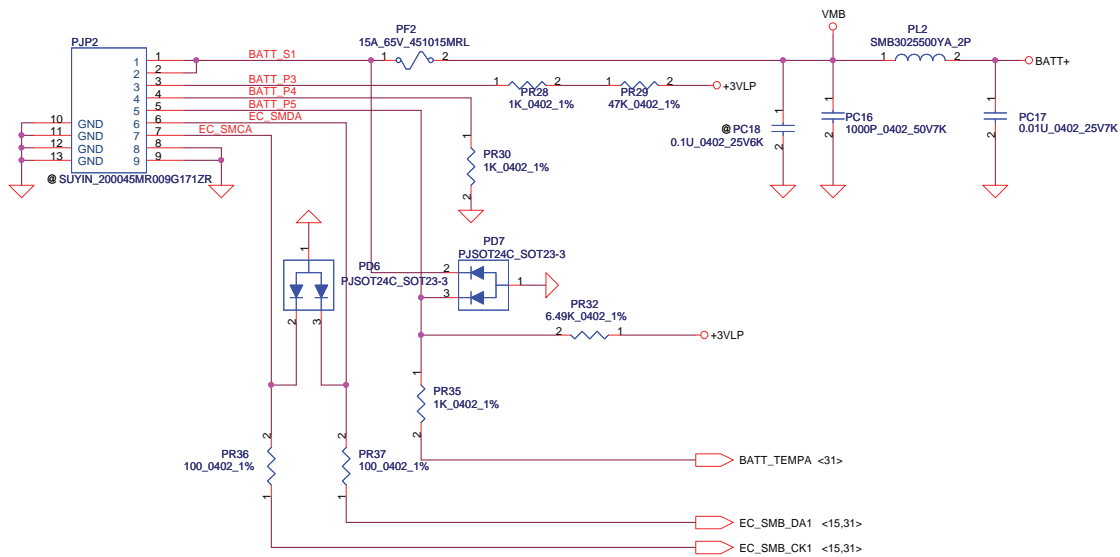
## SP093MX0000



## Precharge detector 15.97V/14.84V FOR ADAPTOR



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Issued Date				2009/01/23		Deciphered Date		2010/01/23		Title	
										DCIN / DETECTOR	
										Size	
										Document Number	
										NWQAA LA6061P M/B	
										Rev	
										2.0	
										Date	
										Wednesday, March 24, 2010	
										Sheet	
										35 of 45	

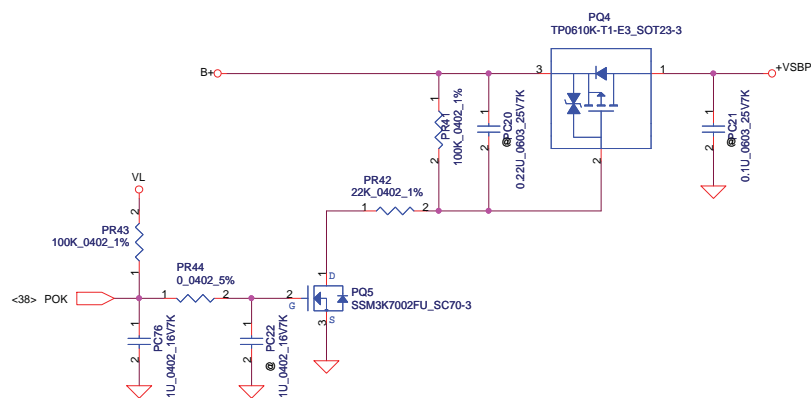
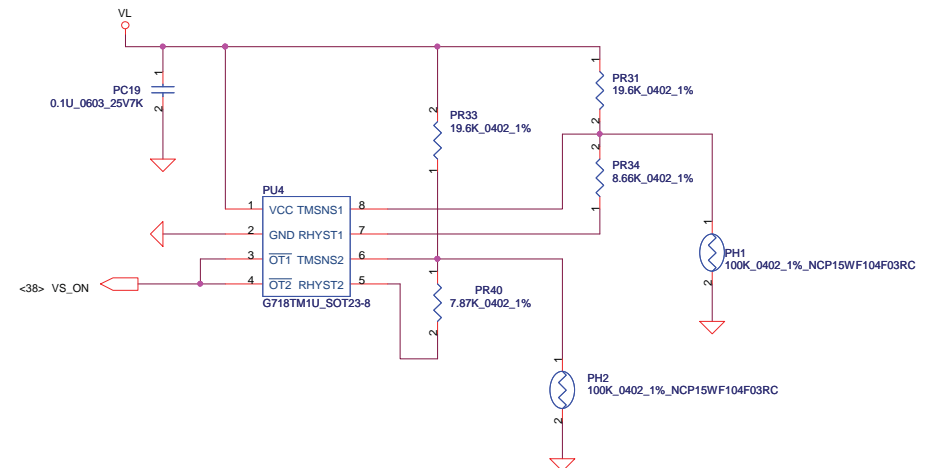


**PH1 under CPU botten side :**

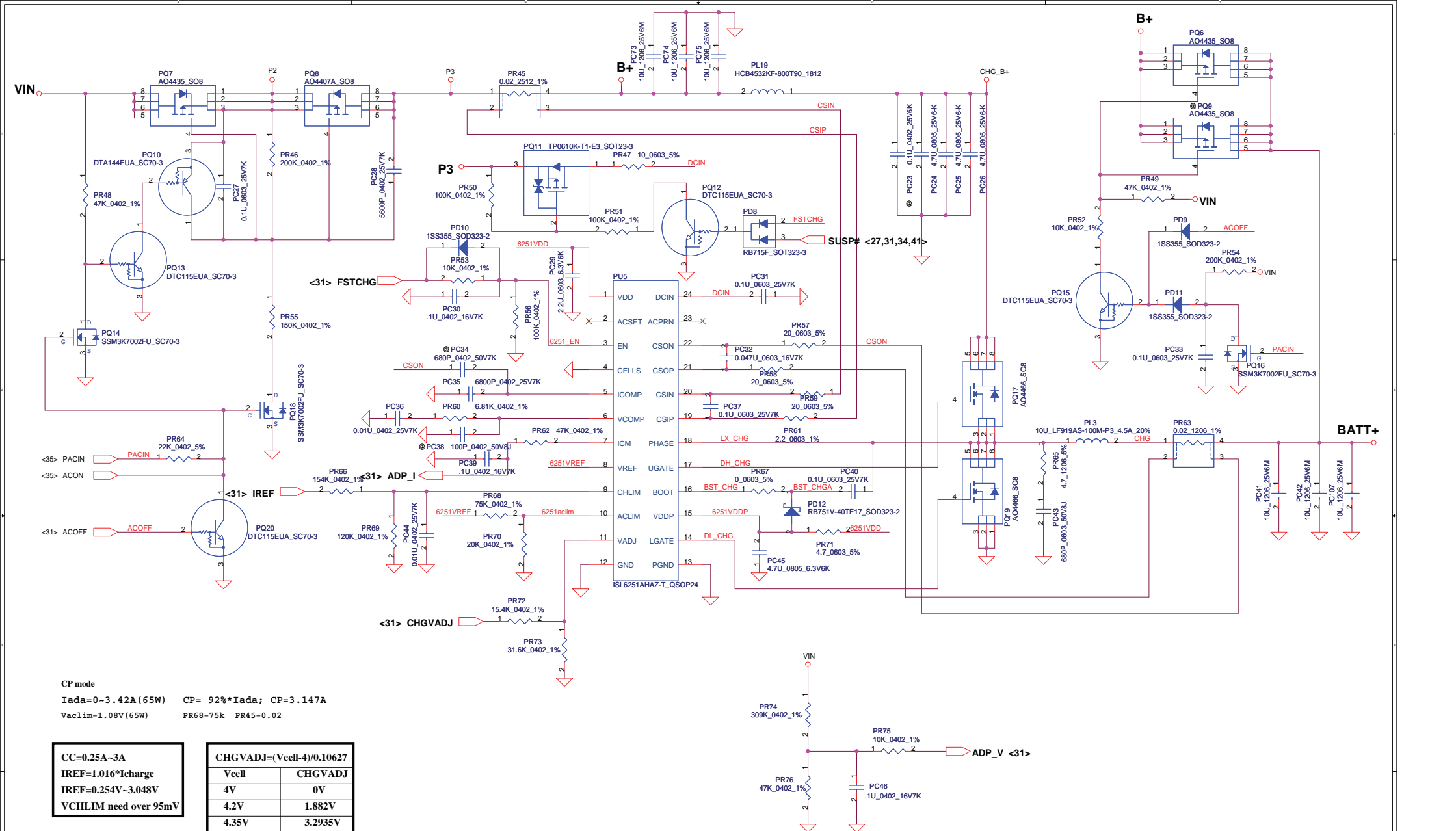
CPU thermal protection at 95degree C  
Recovery at 56 degree C

**PH2 near main Battery CONN :**

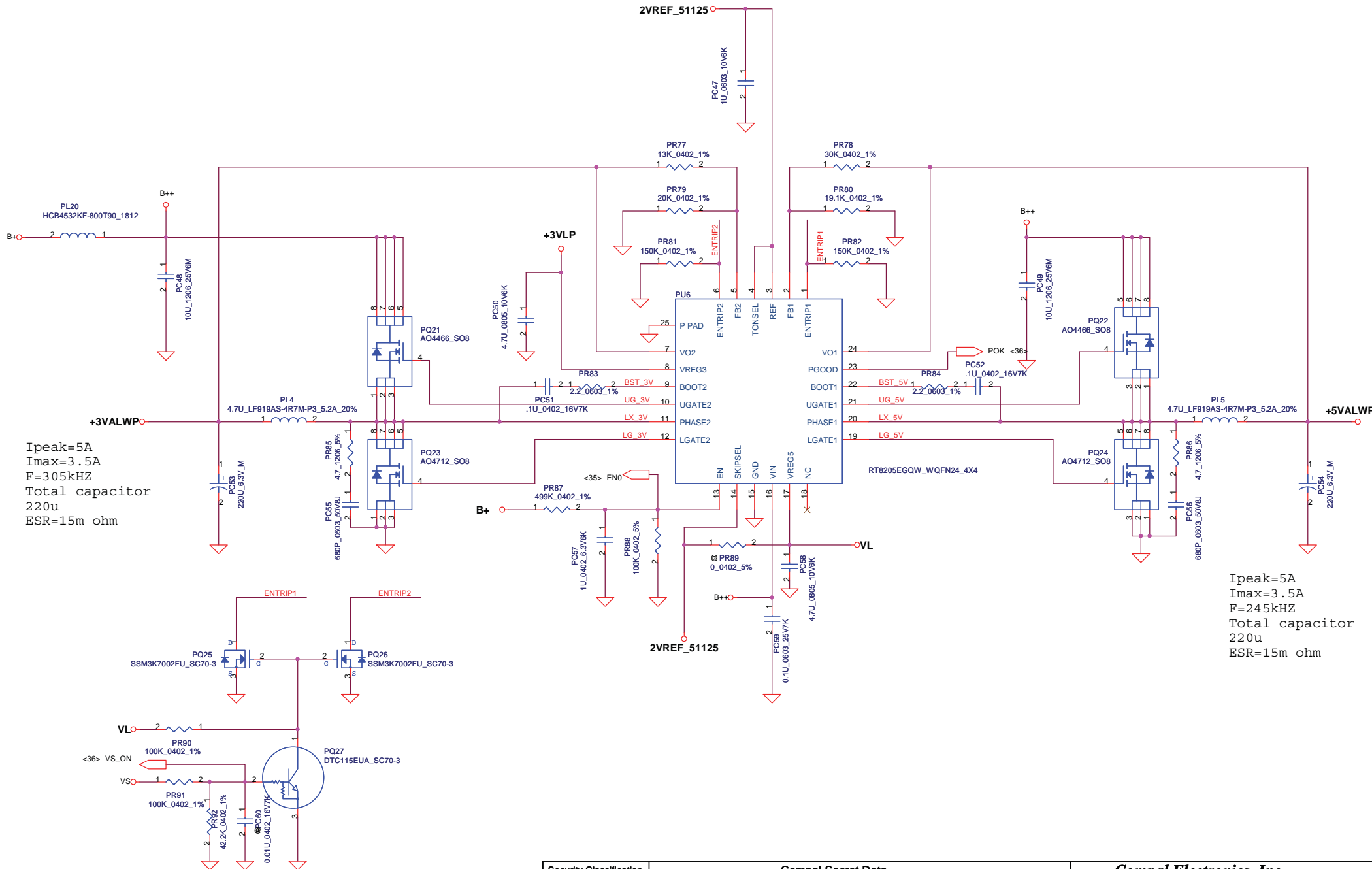
BAT. thermal protection at 95 degree C  
Recovery at 48 degree C



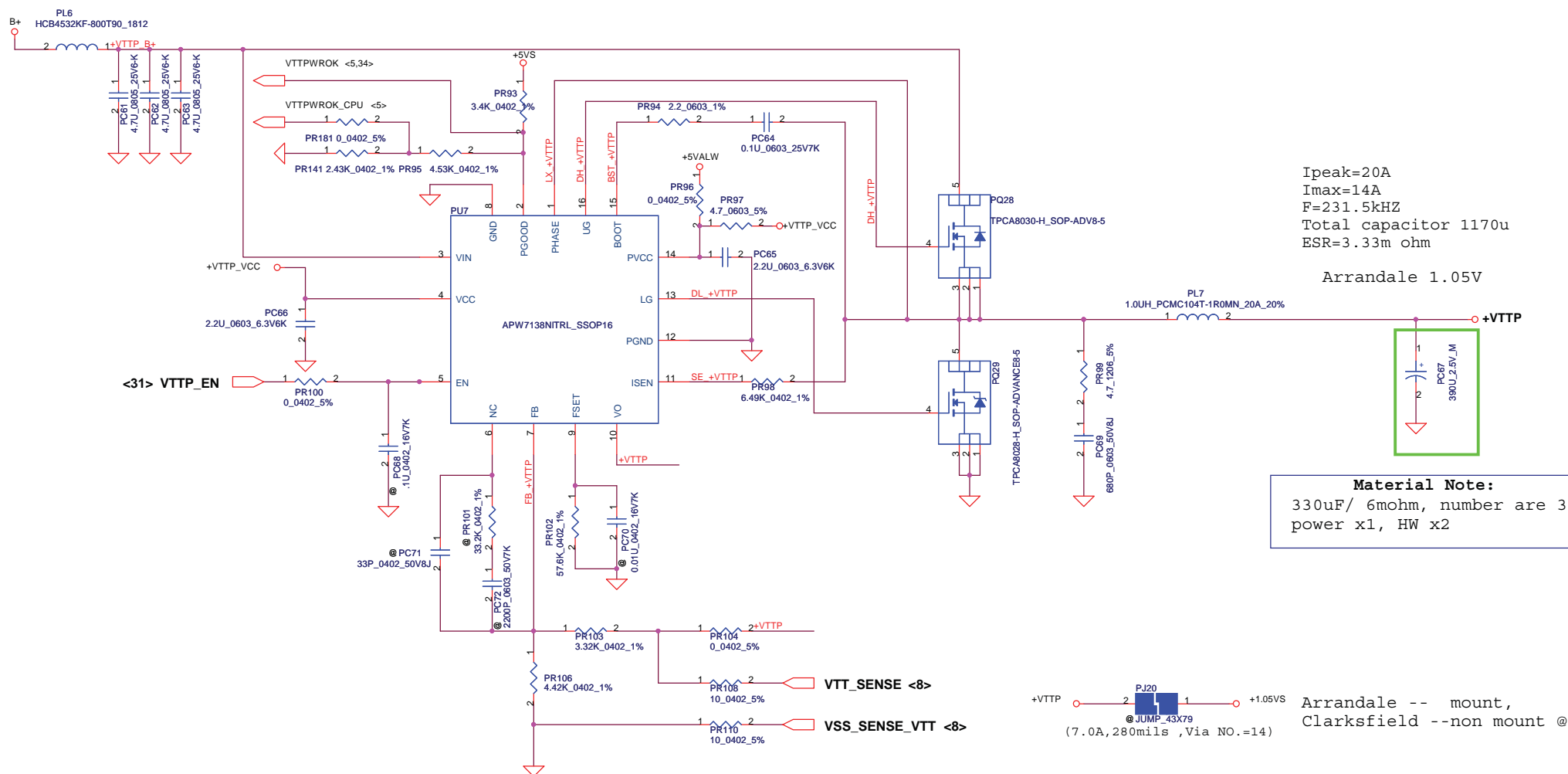
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title	
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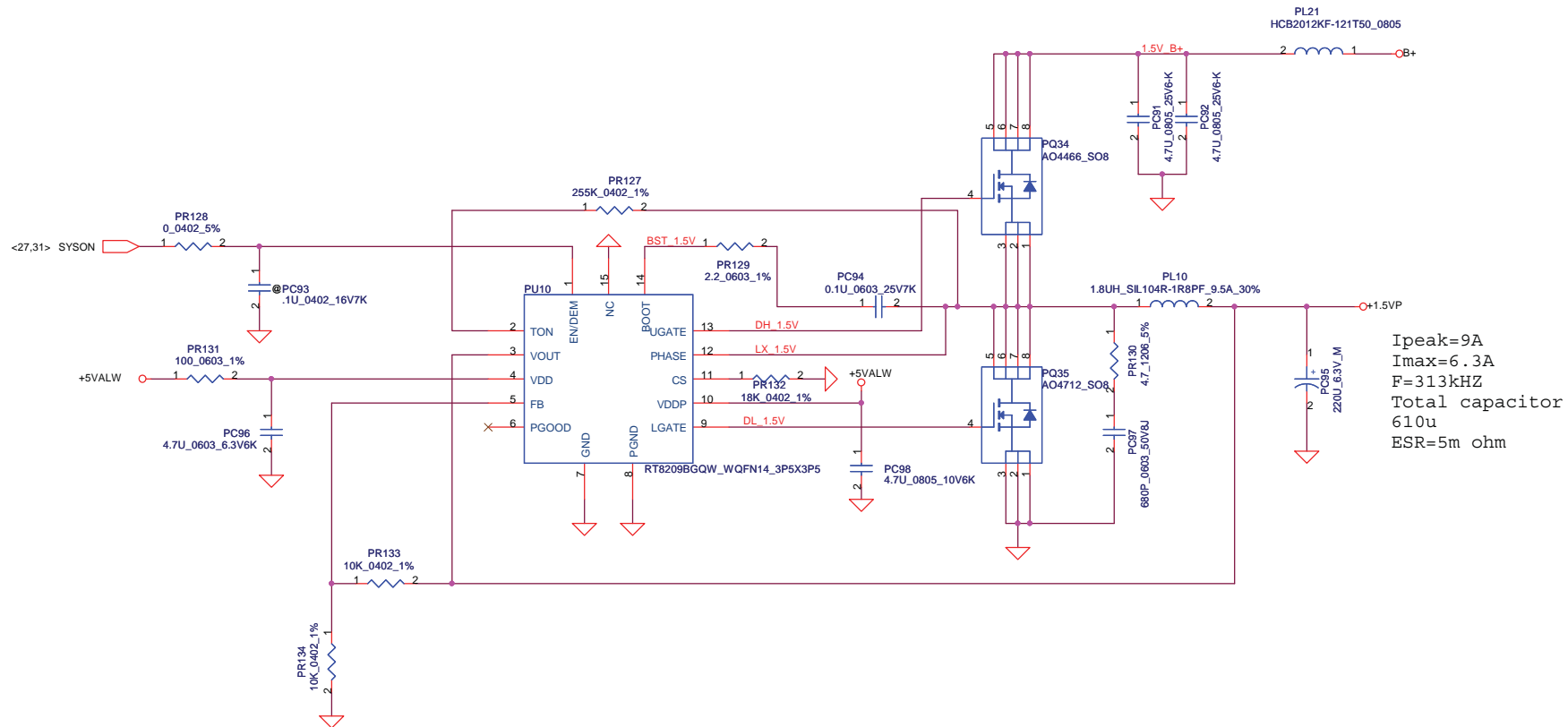


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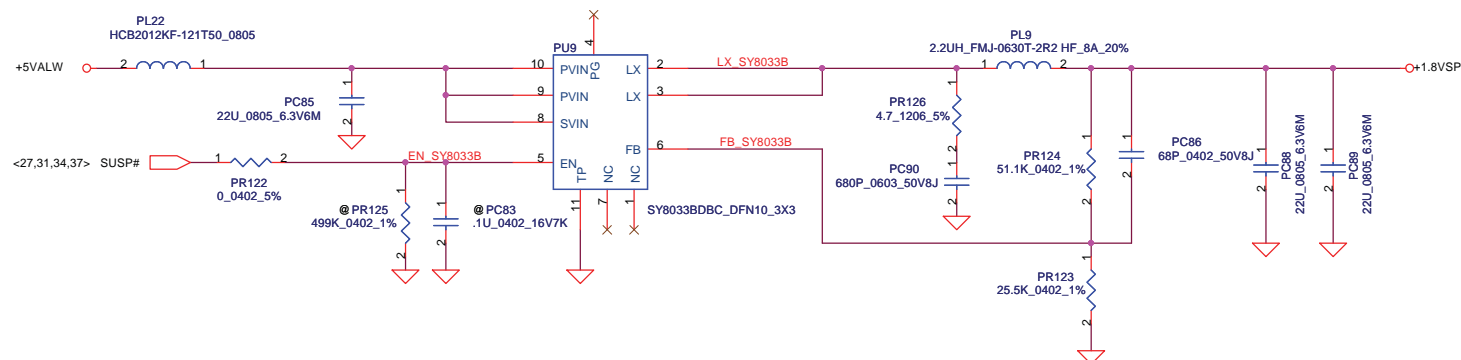
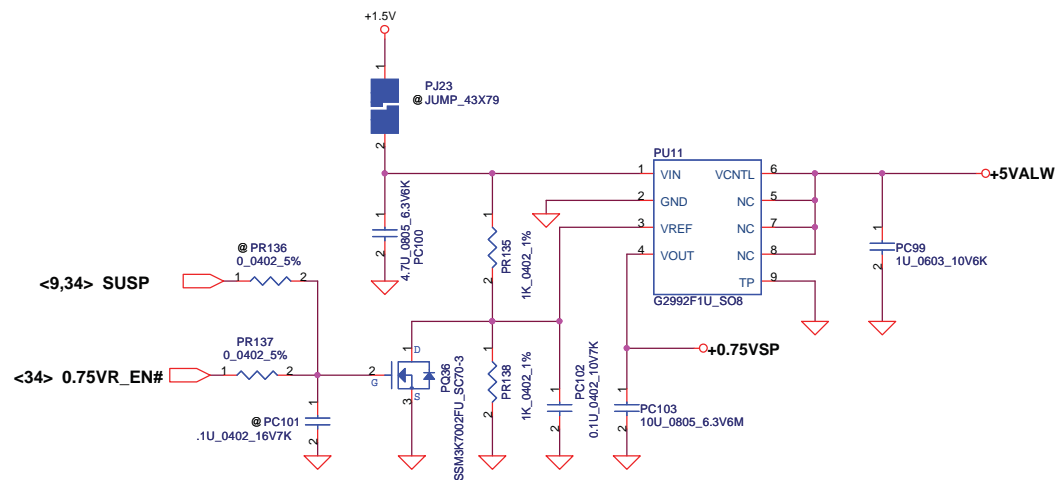
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Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title	
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Size	Document Number	NWQAA LA6061P M/B		2.0	Rev
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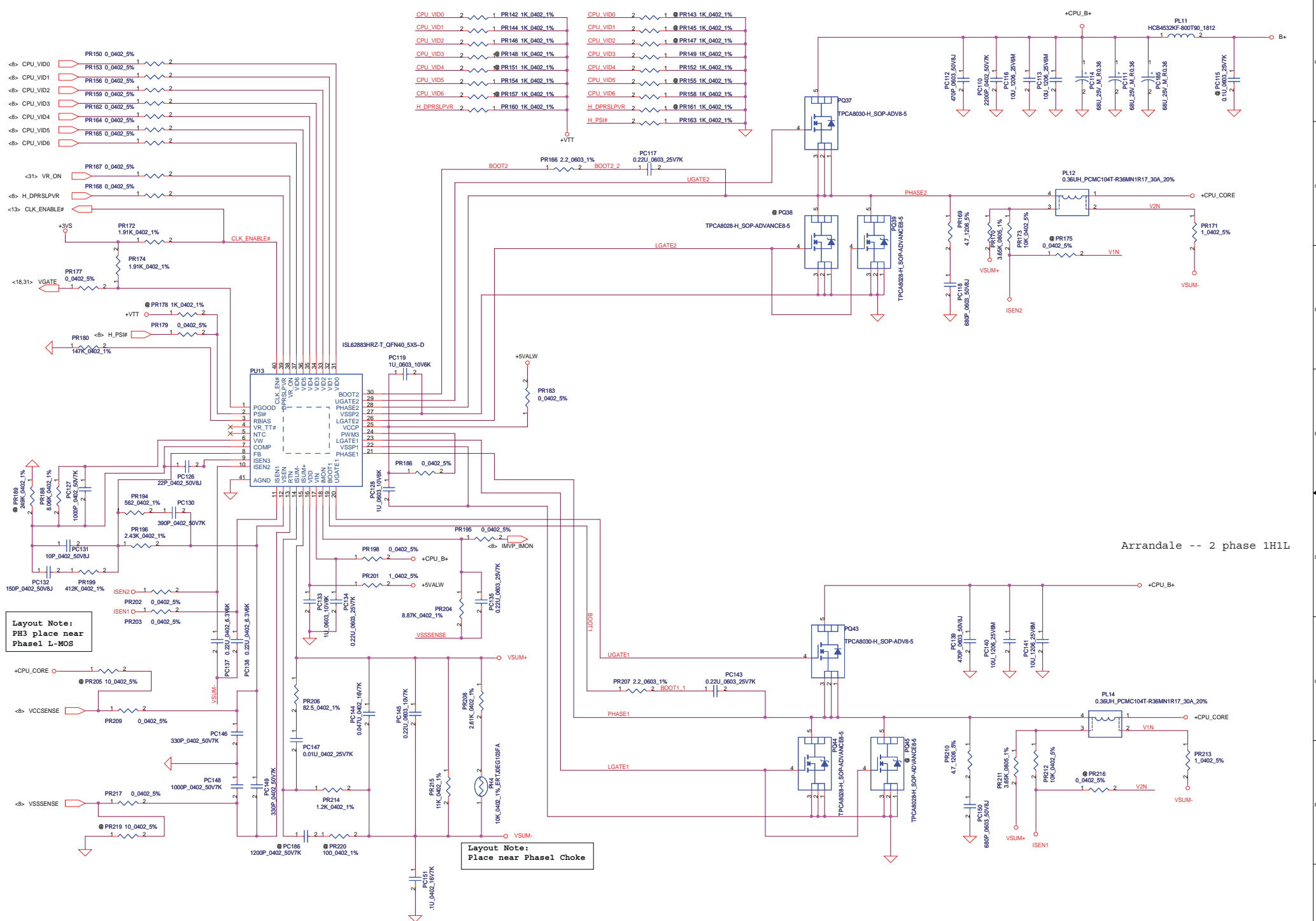


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Issued Date		2009/01/23		Deciphered Date		2010/01/23		Title	
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						Custom	NWQAA LA6061P M/B		2.0
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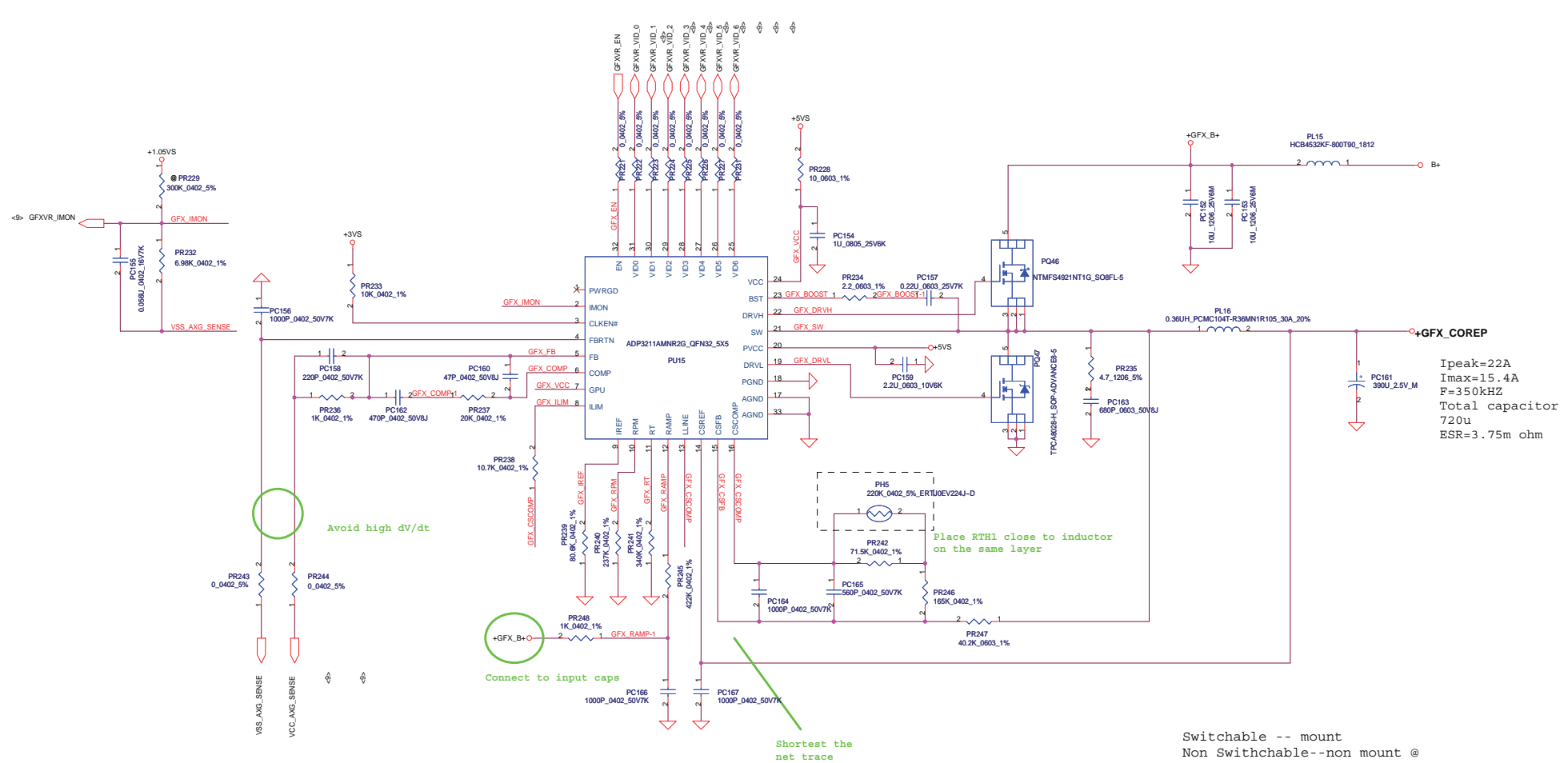
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title	0.75VSP/+1.8VSP
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				Sheet	41 of 45
				Rev	2.0



Layout Note:  
PH3 place near  
Phasel L-MOS

Layout Note:  
Place near Phasel Choke

Arrandale -- 2 phase 1H1L



Ipeak=22A  
I<sub>max</sub>=15.4A  
F=350kHz  
Total capacitor  
720u  
ESR=3.75m ohm

NO DATE	PAGE	MODIFICATION LIST		PURPOSE
EVT	P39-PWR_+VTTP	Change	PR141 2.26k to 2.43k	Modify VTTPPWROK voltage (2009/11/25)
EVT	P39-PWR_+VTTP	Remove	PC71 33P, PC72 2200P, PR101 33.2k	APW7138 not use this function (2009/11/25)
EVT	P38-PWR_3VALWP/5VALWP	Change	PR92 49.9k to 42.2k	Modify VS divider voltage to drive MOS (2009/11/25)
EVT	P42-PWR_CPU_CORE	Change	PL12,PL14 SH000005680 to SH00000IK00	Use 5% DCR choke (2009/11/25)
EVT	P43-PWR_GM VGA_CORE	Change	PH5 SL20000058L to SL200000500	Use Compal PN (2009/11/25)
DVT	P48-PWR_BATTERY CONN / OTP	Add	PD6, PD7 ESD diode	For ESD solution(2009/12/28)
DVT	P43-PWR_GM VGA_CORE	Change	PL16 SH00000HK00 to SH00000IK00	Use same PN choke (2009/12/28)
DVT	P42-PWR_CPU_CORE	Change	PC114, PC111, PC185 from SF000000F80 to SF000000W00	Cost down (2009/12/28)
DVT	P43-PWR_GM VGA_CORE	Change	PC161 to SGA00002680	For DVT budding(thermal issue), it will change to original type for PVT (2009/12/28)
DVT	P50-PWR_3VALWP/5VALWP	Change	PR83,PR84 0 to 2.2	Add boost resistor(For EMI solution)(2009/12/28)
		Add	PR85,PR86 4.7 and PC55,PC56 680P	Add snubber(For EMI solution)(2009/12/28)
DVT	P42-PWR_CPU_CORE	Change	PR166,PR207 0 to 2.2	
		Add	PR169,PR210 4.7 and PC118,PC150 680P	
DVT	P55-PWR_GM VGA_CORE	Change	PR234 0 to 2.2	Add boost resistor(For EMI solution)(2009/12/28)
		Add	PR235 4.7 and PC163 680P	Add snubber(For EMI solution)(2009/12/28)
DVT	P48-PWR_BATTERY CONN / OTP	Change	PR33 10k,PR31 21k to 19.6k, PR34 9.53k to 8.66k, PR40 47k to 7.87k	Adjust OTP setting point(2009/12/28)
DVT	P39-PWR_+VTTP	Change	PR98 4.99k to 6.49k	Adjust VTT_DIS OCP to 27.49A (2009/12/31)
DVT	P49-PWR_CHARGER	Add	PC73,PC74,PC75 10U	Reserve for EMI solution(2009/12/28)
DVT	P42-PWR_CPU_CORE	Change	PR204 8.25k to 8.87k	Adjust resistor for Imon (2009/12/31)
DVT	P55-PWR_GM VGA_CORE	Change	PR247 34.8k to 40.2k	Adjust GFX load line (2009/12/31)
DVT	P41-PWR_0.75VSP/1.8VSP	Change	PC90 SE025681K80 to SE024681J80	Use same PN (2009/12/31)
PVT	P41-PWR_0.75VSP/1.8VSP	Remove	PR136, Add PR137 0 Ohm	For S3 power saving function (2010/02/03)
PVT	P43-PWR_GM VGA_CORE	Change	PC161 to SF000002000	Change to original type for PVT (2010/02/03)
PVT	P49-PWR_CHARGER	Change	PC24,PC25,PC26 4.7U to 10U	For EMI solution(ISN test) (2010/02/03)
PVT	P49-PWR_CHARGER	Add	PC107 10U	For EMI solution(ISN test) (2010/02/03)
PVT	P49-PWR_CHARGER	Add	PC73,PC74,PC75 10U	For EMI solution(ISN test) (2010/02/03)
PVT	P49-PWR_CHARGER	Add	PC76 0.1U	For ESD solution (2010/02/03)
PVT	P38-PWR_3VALWP/5VALWP	Change	PQ27 from SSMK7002 to DTC115EUA	Use low Vth Transistor (2010/02/03)
PVT	P43-PWR_GM VGA_CORE	Change	PQ46 TPCA8030 to NTMFS4921NHT1G	For EMI solution (2010/02/03)
Pre MP	P52-PWR_1.05VSP/1.8VSP	Change	PR123 316k to 25.5k,PR124 402k to 51.1k	Adjust 1.8V voltage divided resistor (2010/03/07)
Pre MP	P52-PWR_1.05VSP/1.8VSP	Change	PU9 from MP2121 to SY8033	MP2121 ESD fail (2010/03/07)
Pre MP	P52-PWR_1.05VSP/1.8VSP	Delete	PR125 0 Ohm	Change for SY8033 solution(2010/03/07)
		Change	PC85 from 0.1U to 22U	
		Delete	PC87 10UF, PC84 0.1U	
Pre MP	P52-PWR_1.05VSP/1.8VSP	Change	PC86 10U to 68P	Improve 1.8V transient under shoot(2010/03/07)
Pre MP	P49-PWR_CHARGER	Change	PC24,PC25,PC26 10U to 4.7U	10U 0805 size price too high(2010/03/07)
Pre MP	P47-PWR_DCIN/DECTOR	Change	PC12 from SE033105Z80 to SE000001380	Change PN(2010/03/07)

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					Size	Document Number
					NWQAA LA6061P M/B	
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PIR (Product Improve Record)

NWQAA LA-6061P SCHEMATIC CHANGE LIST  
REVISION CHANGE: 0.1 TO 0.2  
GERBER-OUT DATE: 2009/12/30

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	12/7	25	Add +5VALW for JPIO pin5	For BACK_SENSE detect
2	12/7	13	Remove JLVDS pin10 and pin12 for +LCDVDD_R	3D Panel max. current is 1.5A
3	12/8	33	Combine JTOUCH and JLP to JTPL and remove C648	For ME cost down
4	12/17	33	Remove D19	Move D19 to LS-6061P
5	12/18	26	Reverse JBT pin definition	Due to pin reverse
6	12/18	30	Add RA43	For codec EC_MUTE# issue
7	12/21	29	Change JREAD to Push-push type (R015-211-LM-A)	For PRD update
8	12/21	13	Move LED_PWM and BKOFF#_R to JLVDS pin10 and pin12	For avoiding +LCD_INV short issue
9	12/22	32	Change H7 footprint to "DEBUG_PAD-MB-S"	For debug use
10	12/23	27	Add D24 and Q36 for BT_CTRL	For WLAN & BT combo module
11	12/23	21	Add R461	For CIR_EN#
12	12/24	25	Change JPIO footprint and reverse its pin definition	For ME request
13	12/24	15	Add R145	For U9 ESD damage issue
14	12/24	29	Add F3	For Card reader issue
15	12/29	25	Add R148 and R149	For Sleep & play music
16	12/29	13	Add C871 and C872	For RF request

NWQAA LA-6061P SCHEMATIC CHANGE LIST  
REVISION CHANGE: 0.2 TO 0.3  
GERBER-OUT DATE: 2010/02/08

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	1/15	30	Add RA43	For sleep & music on battery mode
2	1/21	31	Add R462	Avoid VR_ON floating
3	1/25	32	Change UG3 to SA000022I00	For LDO issue
4	1/25	33	Change SW2 to @	For ME interfere issue
5	2/1	15	Add R130	For AOC monitor issue
6	2/1	31	Change U19 to SA00001J5A0	For KB926 E0 version
7	2/1	29	Remove F3	For UC1 ES2 sample
8	2/1	16	Add D19 and R150	For RTC charge issue
9	2/2	31	Add CAP_RST# to EC	For ESD issue
10	2/3	29	Change RC7 to 33 ohm	For EMI request

NWQAA LA-6061P SCHEMATIC CHANGE LIST  
REVISION CHANGE: 0.3 TO 1.0  
GERBER-OUT DATE: 2010/03/15

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	3/6	29	Add QC2 and RC16	For O2 B0 workaround
2	3/7	16	Change D13.2 power to +CHGRTC	For RTC issue
3	3/12	33	Change H15-H19 to H_3P3	For ME request
4	3/15	33	Remove SW2	For ESD request
5	3/15	30	Change CA9 and CA10 to 1U	For cut-off frequency
6	3/16	30	Change MONO_IN to AGND	For high frequency noise issue

NWQAA LA-6061P SCHEMATIC CHANGE LIST  
REVISION CHANGE: 1.0 TO 2.0  
GERBER-OUT DATE: 2010/03/19

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	3/17	29	Change cardreader to JMB385/389	For customer request
2	3/18	31	Remove D86	For ESD request
3	3/18	22	Add R52	For CRT wave issue
4	3/19	22	Change L12 to 2.2 ohm	For CRT wave issue
5	3/22	15	Add D54	For HDMI CEC issue
6	3/24	13	Change C213 to 1U	For NALAA ESATA performance low issue

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Size	Document Number	NWQAA LA6061P M/B		Rev	2.0		
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