

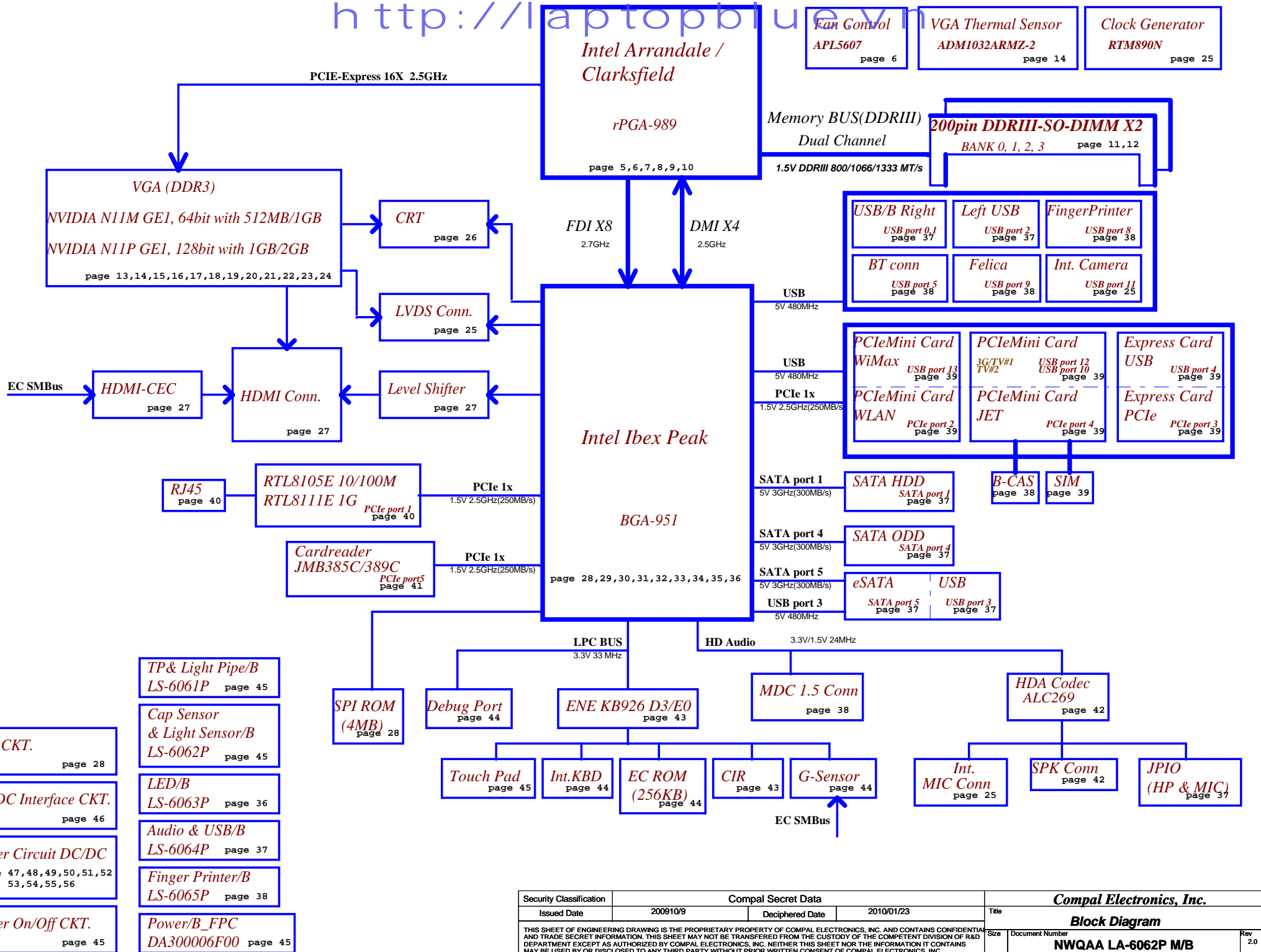
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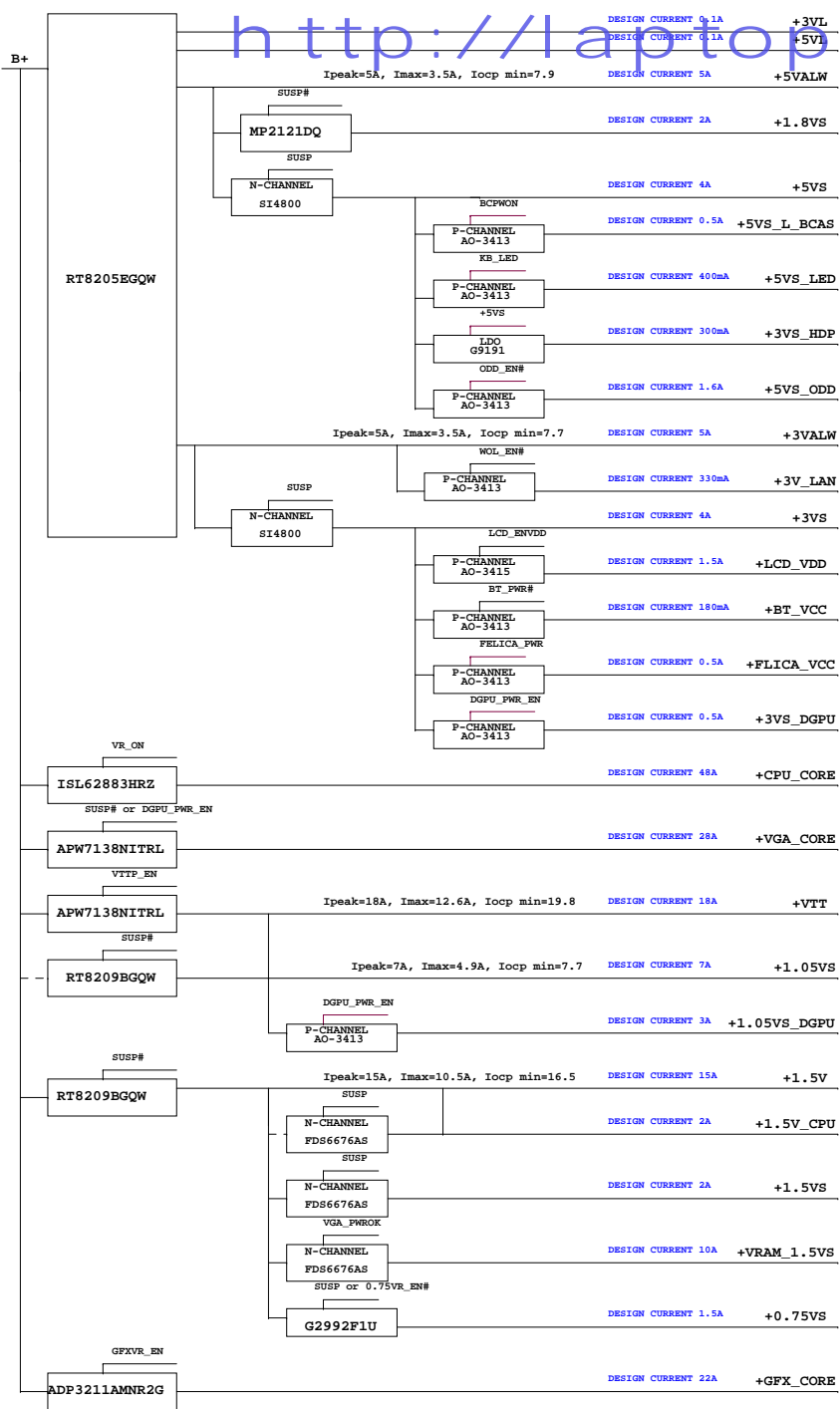
Marseille 10G

LA-6062P REV 2.0 Schematic

Intel Processor(CFD/ARD) / PCH(HM57/HM55/PM55)
2010-03-24 Rev 2.0

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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VTT +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	New Card		
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		
+3VS	3G		

EC SM Bus1 Address

EC SM Bus2 Address

Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b	+3VS	PCH	96 H	1001 0110 b
+3VL	HDMI-CEC	34 H	0011 0100 b	+3VS	NVIDIA GPU	9A H	1001 1010 b
				+3VS	G-Sensor	40 H	0100 0000 b
				+3VS	Light Sensor	52 H	0101 0010 b
Power	Device	HEX	Address				
+3VL	Cap. Sensor		Virtual I2C				

Platform	SKU	CPU	PCH	VGA
Calpella	UMA(OPT@)	Arrandale	HM55@/HM57@	N/A
	Discrete (DIS@)	Clarksfield/Arrandale	HM55@/HM57@/PM55@	N11P@/N11M@
	Optimus (OPT@)	Arrandale	HM55@/HM57@	N11P@/N11M@

BTO Option Table

Function	HDMI				CPU		
description	HDMI				Arrandale	Clarksfield	
explain	UMA	Discrete/Optimus	COMMON	CEC	Arrandale	Clarksfield	Clarksfield with S3 Power Saving
BTO	IHDMI@	DHDMI@	HDMI@	CEC@	M1@	M3@	PSM3@

Function	MINI PCI-E SLOT			LAN		Fingerprint	Modem	CIR	KB Light
description	SLOT2		SLOT1	LAN		Fingerprint	Modem	CIR	KB Light
explain	3G	TV Tuner	WIMAX	10/100M	Giga	Fingerprint	Modem	CIR	KB Light
BTO	3G@	TV@	WIMAX@	8105E@	8111E@	FP@	MDC@	CIR@	KBL@

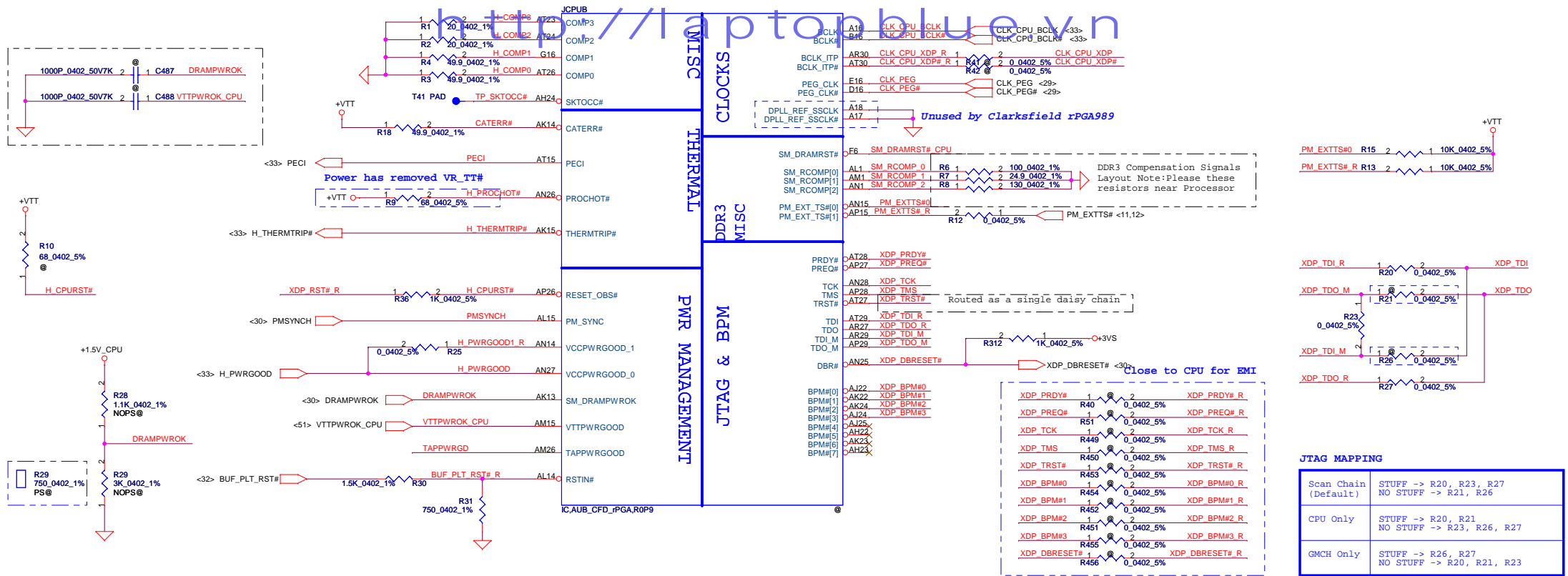
Function	Felica	BLUE TOOTH	G-SENSOR	SKU		LVDS		Camera & Mic	
description	Felica	BLUE TOOTH	G-SENSOR	SKU		3D Panel		Camera & Mic	
explain	Felica	BLUE TOOTH	G-SENSOR	Discrete	Optimus	Discrete		Optimus	Camera & Mic
BTO	FELICA@	BT@	GSSENSOR@	DIS@	OPT@	3D@	NO3D@	OPTFH@	CAM@

Function	S3 Power Saving		GPU					New Card
description	S3 Power Saving		N11P & N11E			N11M		New Card
explain	No Power Saving	Power Saving	VRAM	N11P	N11E	N11M-GE1	N11M-OP1	New Card
BTO	NOPS@	PS@	8PCS@	N11P@	N11E@	N11MGE@	N11MOP@	NEW@

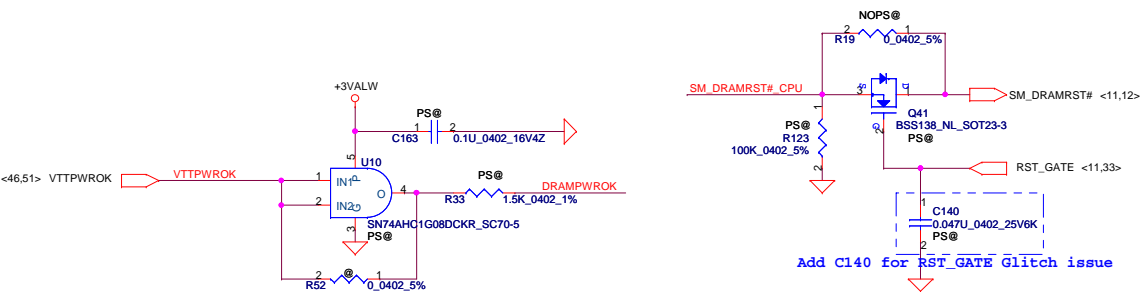
Function	Card reader	
description	JMB385C/389C	
explain	JMB385C	JMB389C
BTO	JMB385@	JMB389@

STATE	SIGNAL		
	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

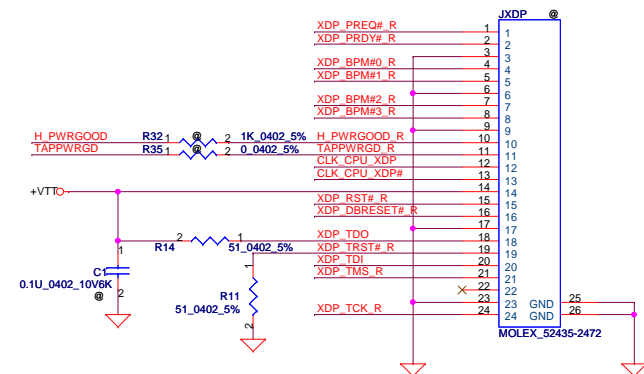
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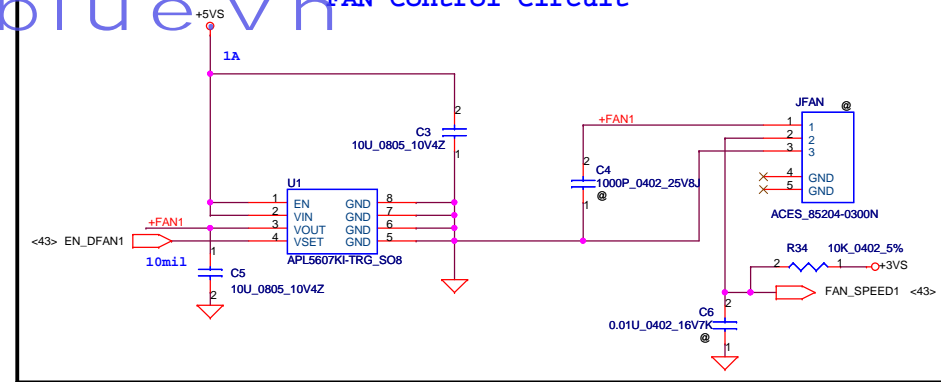
For S3 CPU Power Saving



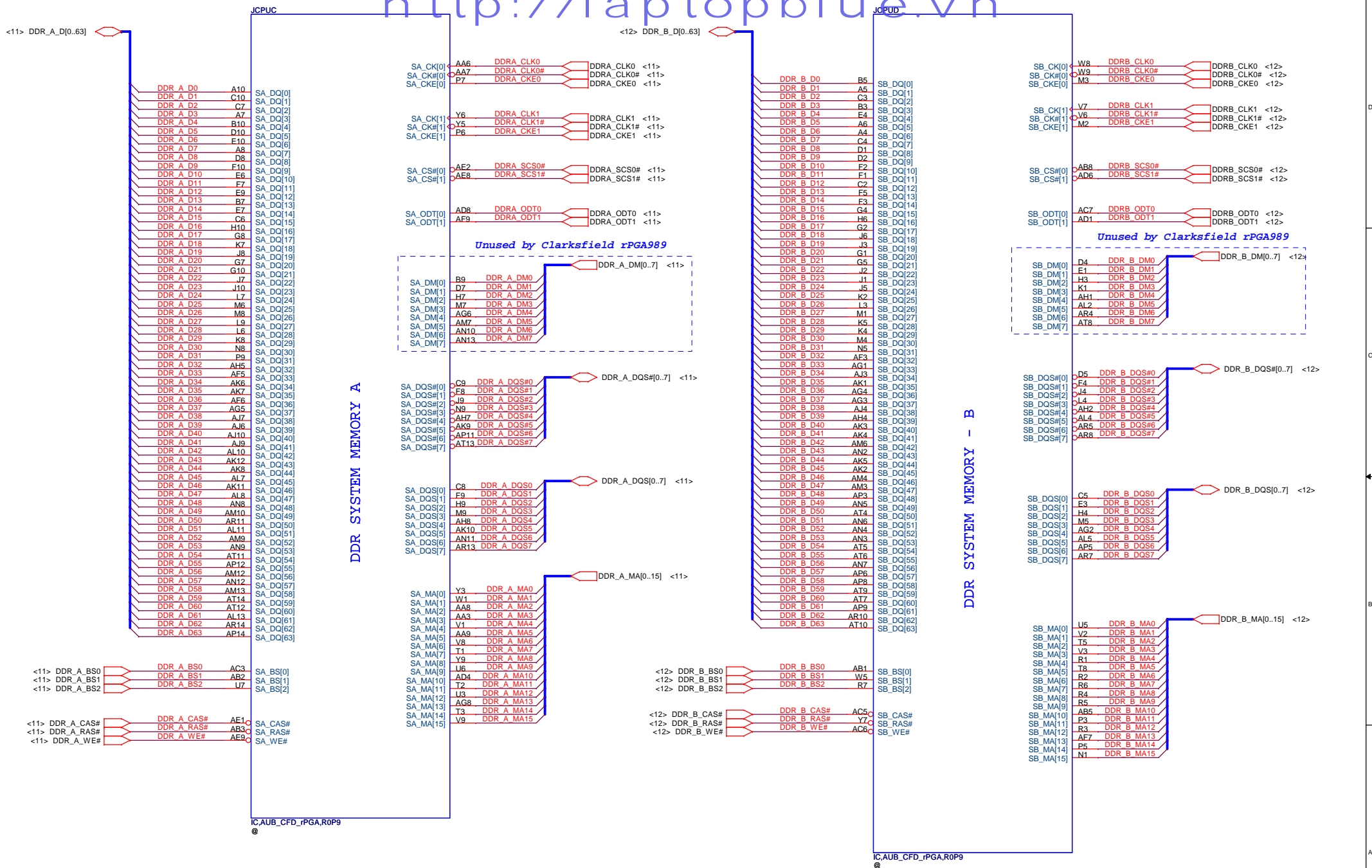
XDP Connector



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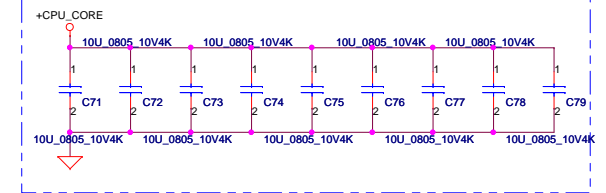


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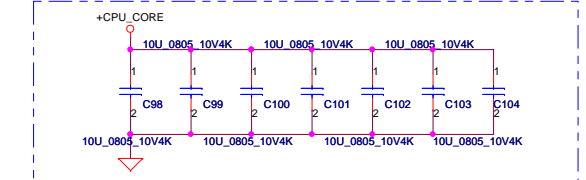
Material Note (+VTT):
390uF/ 10mohm, number are 3,
power x1, HW x2

(Place these capacitors under CPU socket Edge, top layer)

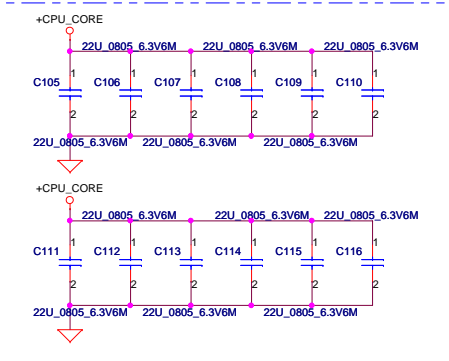
(Place these capacitors between inductor and socket on Bottom)



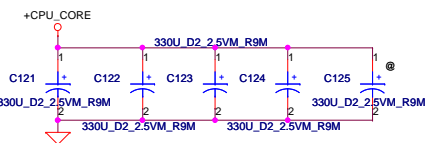
(Place these capacitors under CPU socket, top layer)



(Place these capacitors on CPU cavity, Bottom Layer)



TOP side (under inductor)



Check list:

+CPU_CORE: 6x 470uF, 12x 22uF, 17x 10uF
+VTT: 4x 330uF, 7x 22uF, 8x 10uF

JCPUF

Clarksfield: 65A
Auburndale:48A

Clarksfield: 21A
Auburndale:18A

1.1V RAIL POWER

CPU CORE SUPPLY

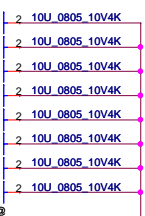
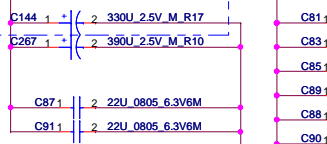
POWER

CPU VIDS

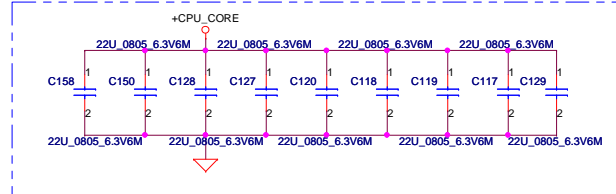
SENSE

IC_AUB_CFD_rPGA_R0P9

Change C144 to 4.5mm height at DVT



5/25: Add for power team request.

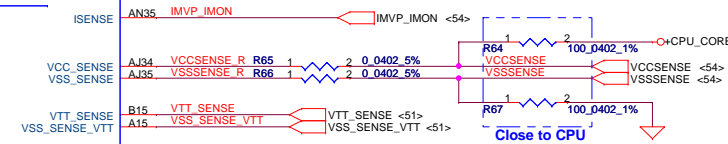
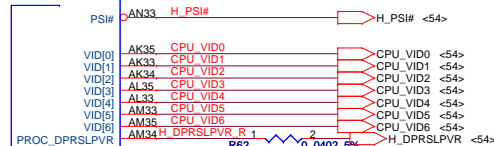


CRB default setting:
VID[6:0]=[0100111]

VTT Rail

Auburndale +1.1VS_VTT=1.05V
Clarksfield +1.1VS_VTT=1.1V

H_VTTSELECT = low, 1.1V
H_VTTSELECT = high, 1.05V



Close to CPU

http://laptopblue.vn

The diagram illustrates the pin connections for the CPU GND/RESERVED area, organized into three main sections: JCPUH, JCPUE, and JCPUF.

JCPUH Pins:

- VSS1-VSS80
- AE34-AE39
- AP25-AP30
- RSVD1-RSVD39
- RSVD40-RSVD43
- RSVD45-RSVD65
- RSVD_TP_59-RSVD_TP_75
- RSVD_TP_76-RSVD_TP_85
- RSVD_NCTF_23-RSVD_NCTF_24
- RSVD_NCTF_28-RSVD_NCTF_29
- RSVD_NCTF_30-RSVD_NCTF_31

JCPUE Pins:

- VSS1-VSS80
- AE34-AE39
- AP25-AP30
- RSVD1-RSVD39
- RSVD40-RSVD43
- RSVD45-RSVD65
- RSVD_TP_59-RSVD_TP_75
- RSVD_TP_76-RSVD_TP_85
- RSVD_NCTF_23-RSVD_NCTF_24
- RSVD_NCTF_28-RSVD_NCTF_29
- RSVD_NCTF_30-RSVD_NCTF_31

JCPUF Pins:

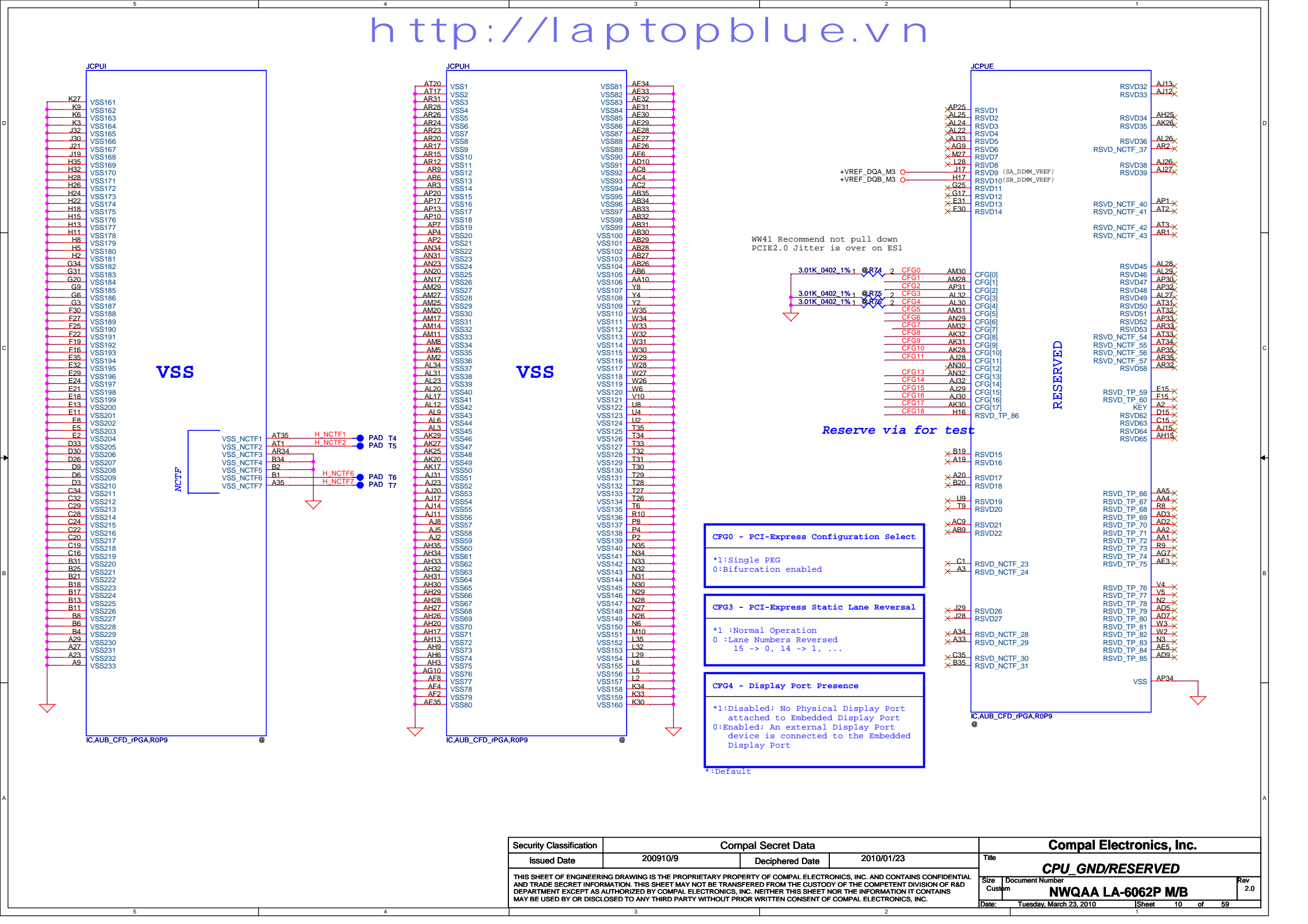
- VSS1-VSS80
- AE34-AE39
- AP25-AP30
- RSVD1-RSVD39
- RSVD40-RSVD43
- RSVD45-RSVD65
- RSVD_TP_59-RSVD_TP_75
- RSVD_TP_76-RSVD_TP_85
- RSVD_NCTF_23-RSVD_NCTF_24
- RSVD_NCTF_28-RSVD_NCTF_29
- RSVD_NCTF_30-RSVD_NCTF_31

Configuration Settings:

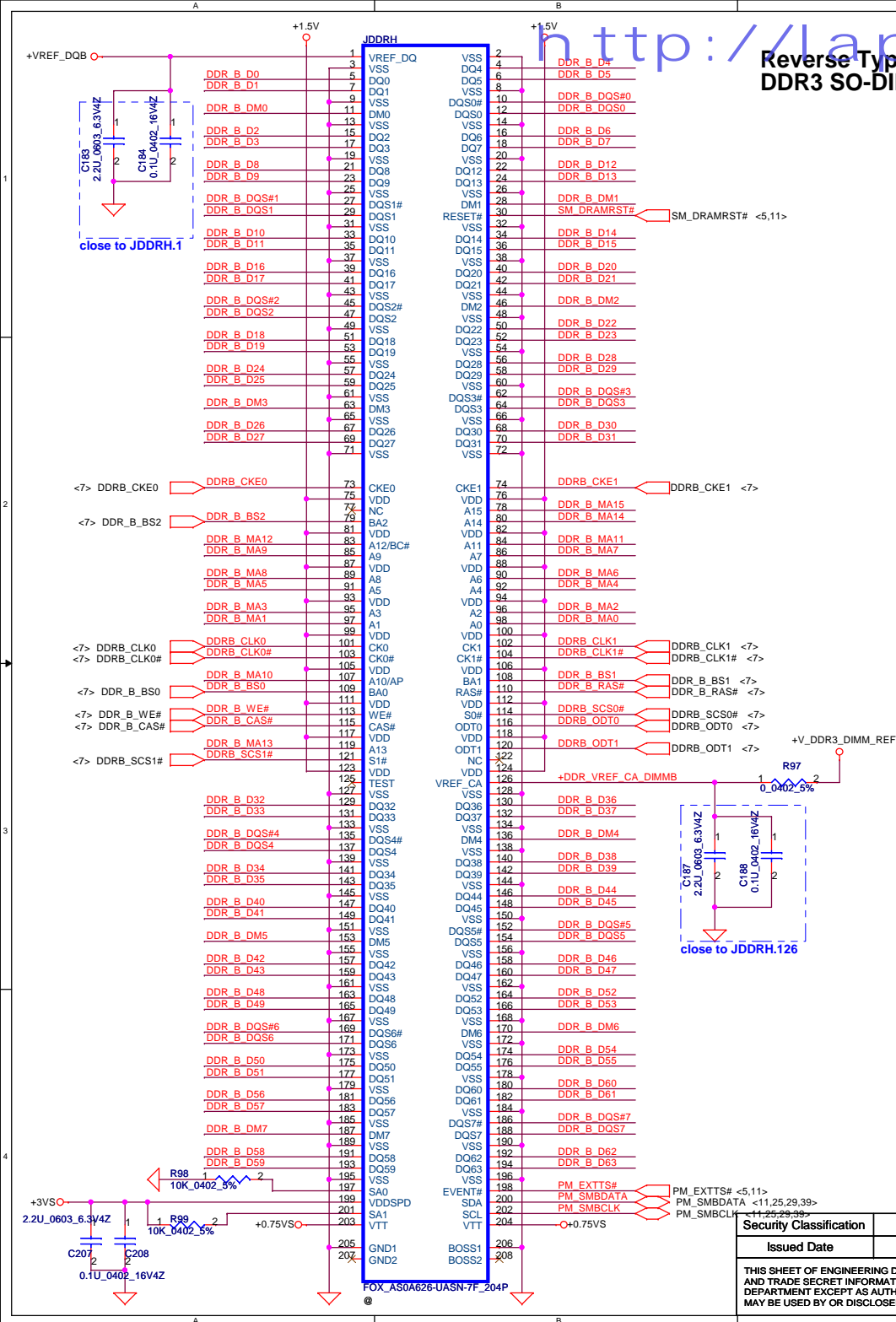
- CFG0 - PCI-Express Configuration Select**: *1:Single PEG, 0:Bifurcation enabled
- CFG3 - PCI-Express Static Lane Reversal**: *1 :Normal Operation, 0 :Lane Numbers Reversed (15 -> 0, 14 -> 1, ...)
- CFG4 - Display Port Presence**: *1:Disabled; No Physical Display Port attached to Embedded Display Port, 0:Enabled; An external Display Port device is connected to the Embedded Display Port

Title Block:

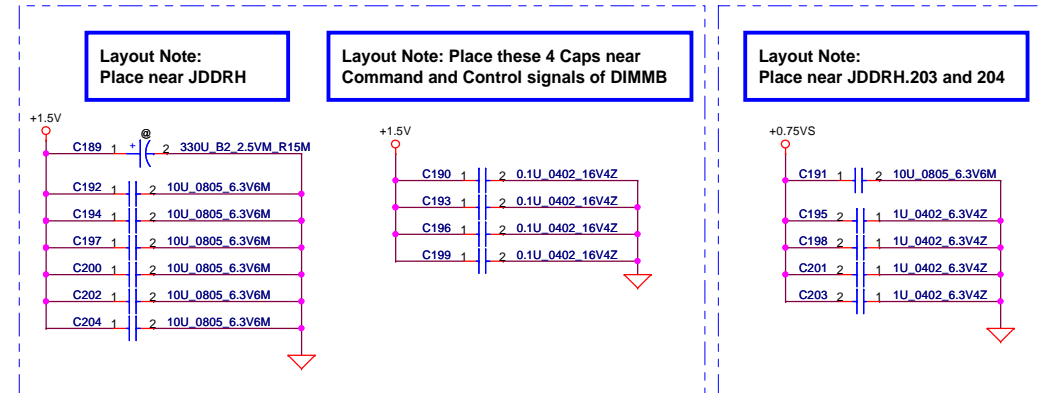
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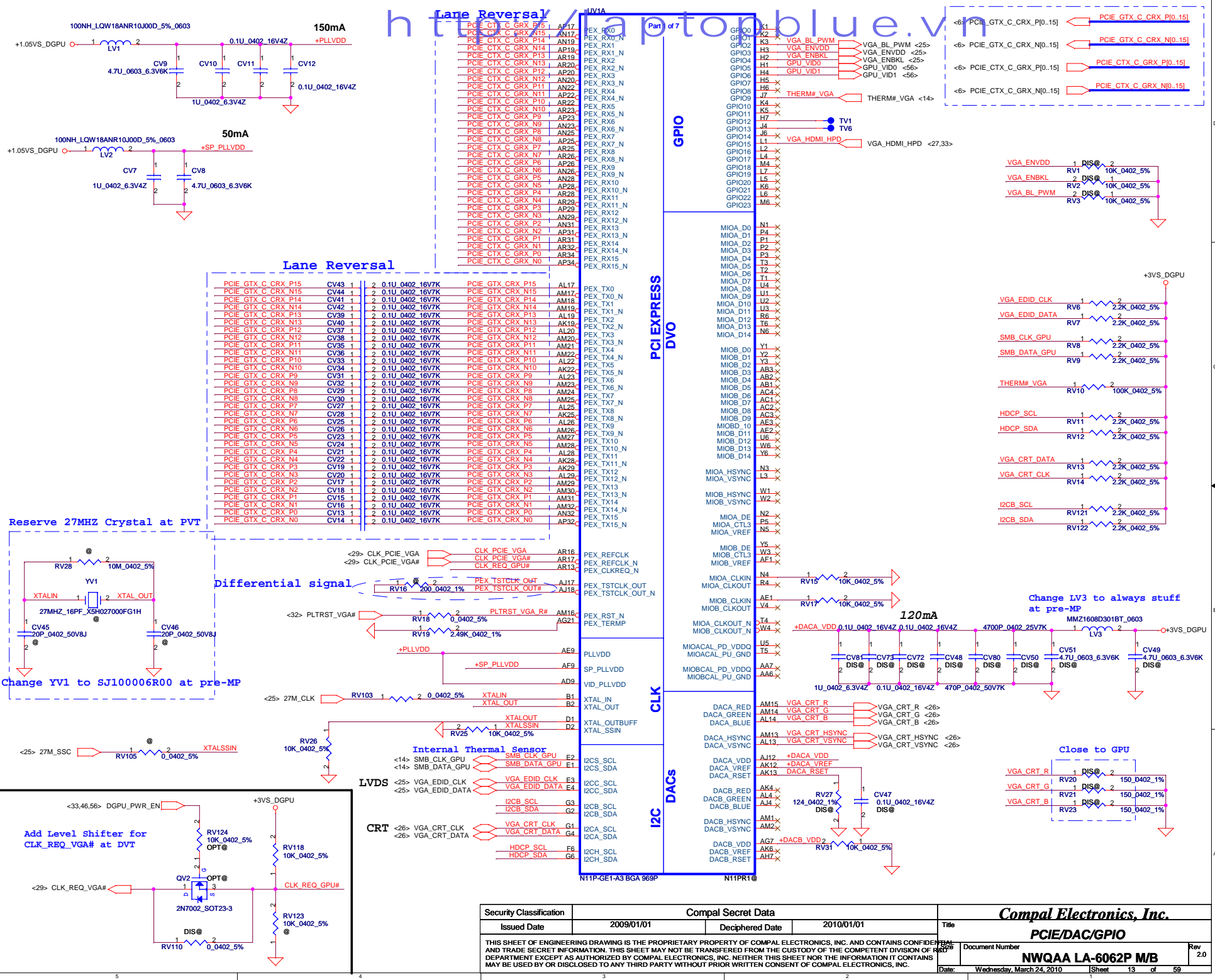
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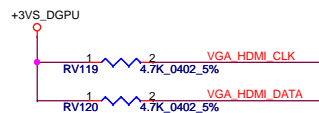
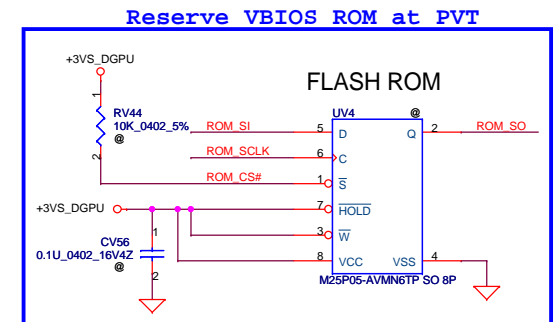
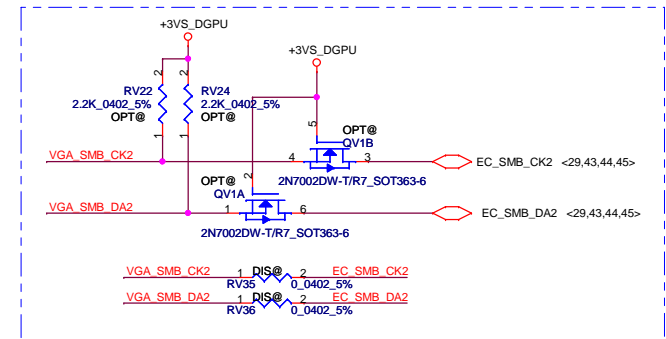
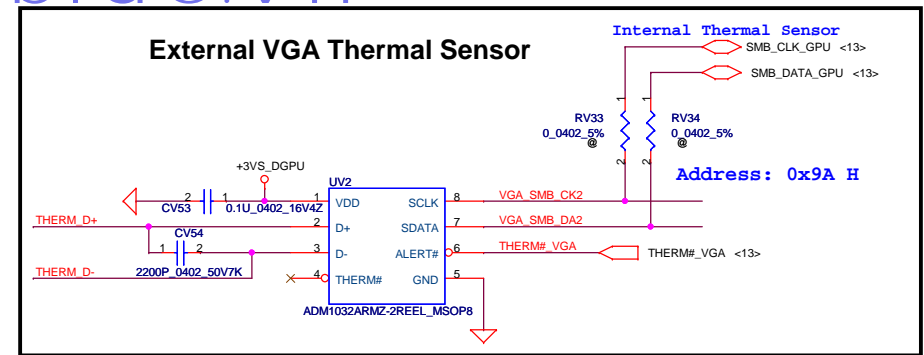
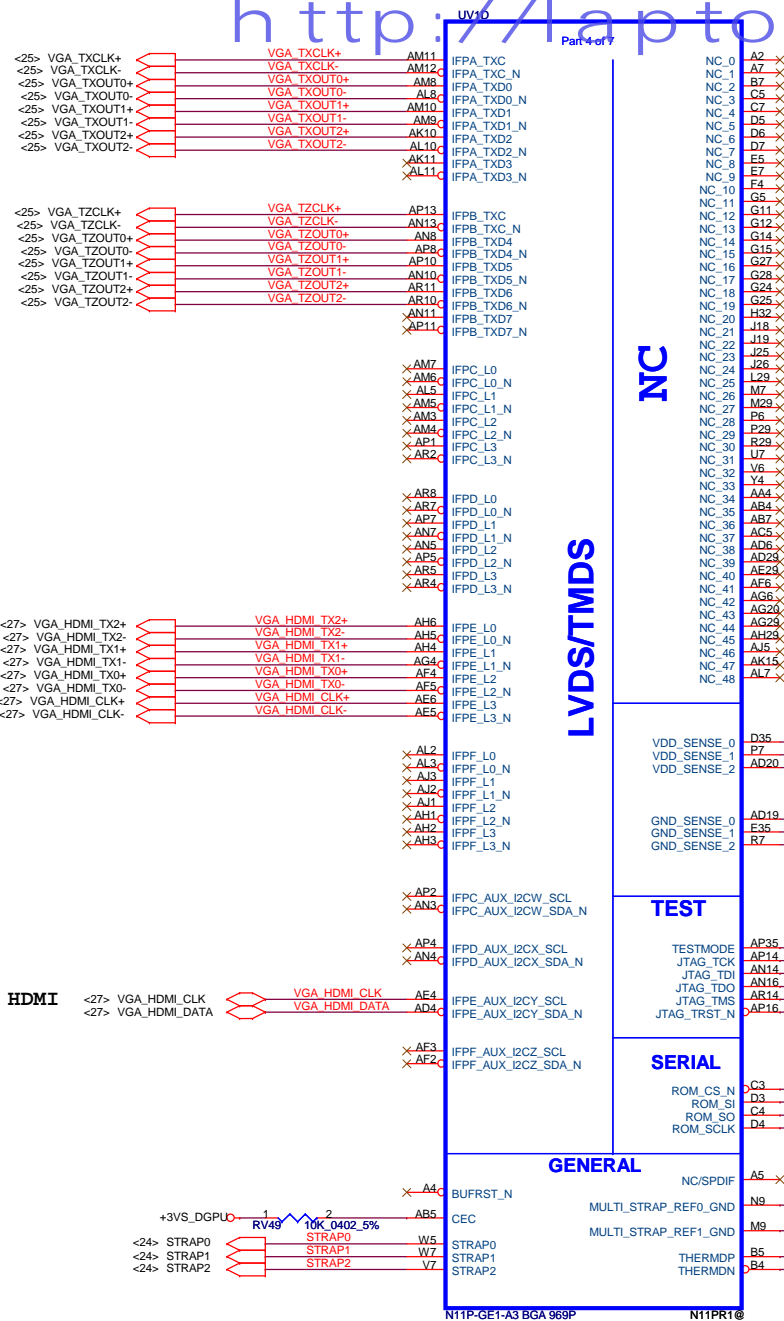
Reverse Type



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N11E-GE1-LP Performance Mode

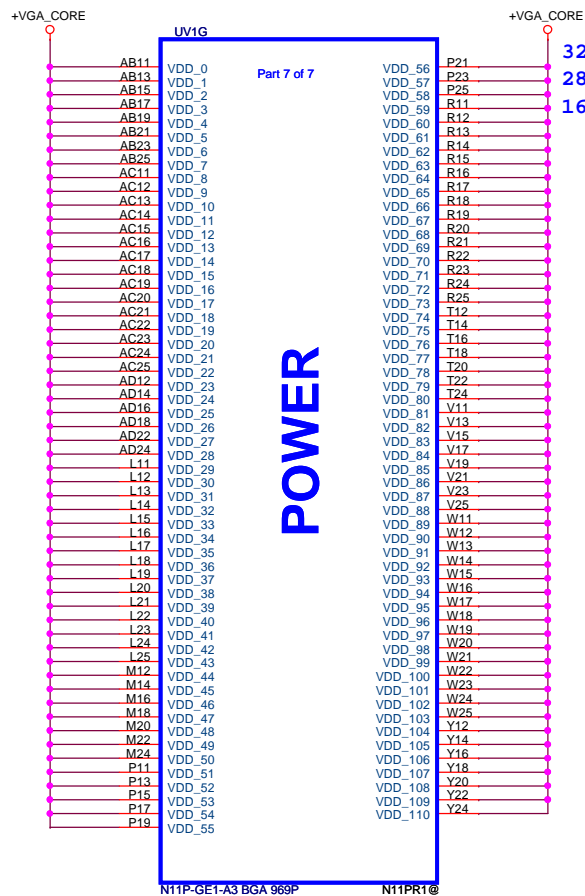
Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	450	790	0.90 V
P8	405	324	0.85 V
P12	135	135	0.80 V

N11P-GE1 Performance Mode

Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	575	790	0.95 V
P8	405	324	0.85 V
P12	135	135	0.80 V

N11M-GE1 & N11M-OP1 Performance Mode

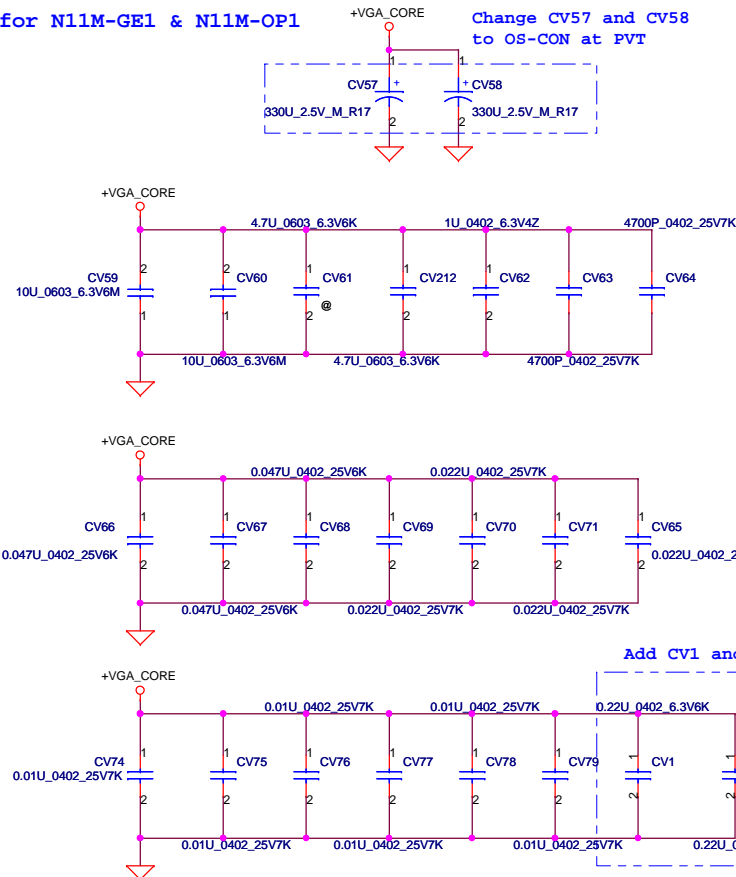
Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	625	790	1.03 V
P8	405	405	0.85 V
P12	135	135	0.85 V



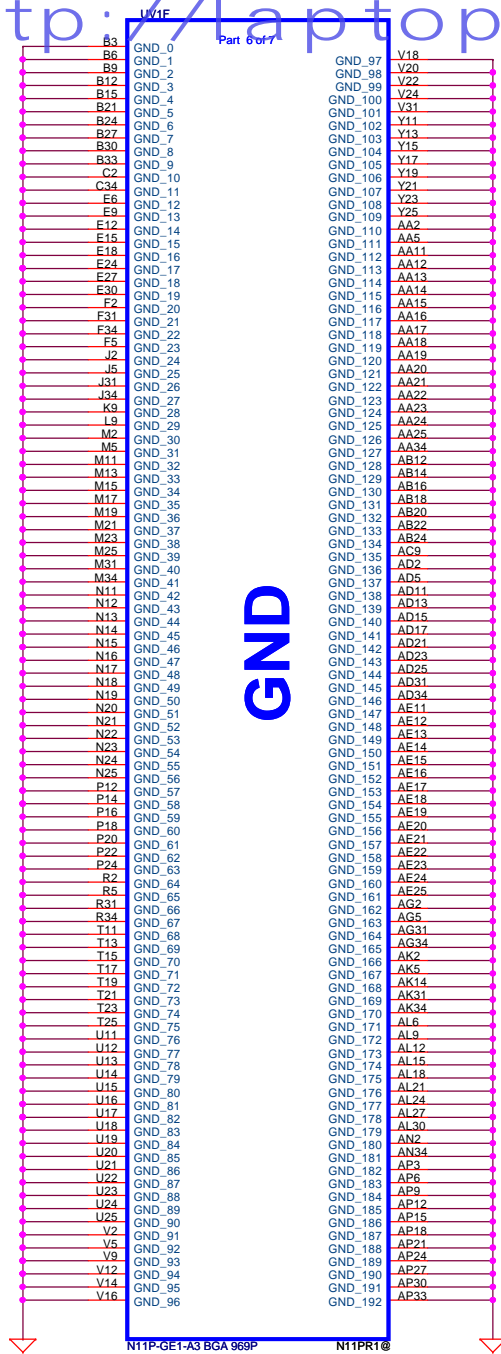
32A for N11E-GE1-LP

28A for N11P-GE1

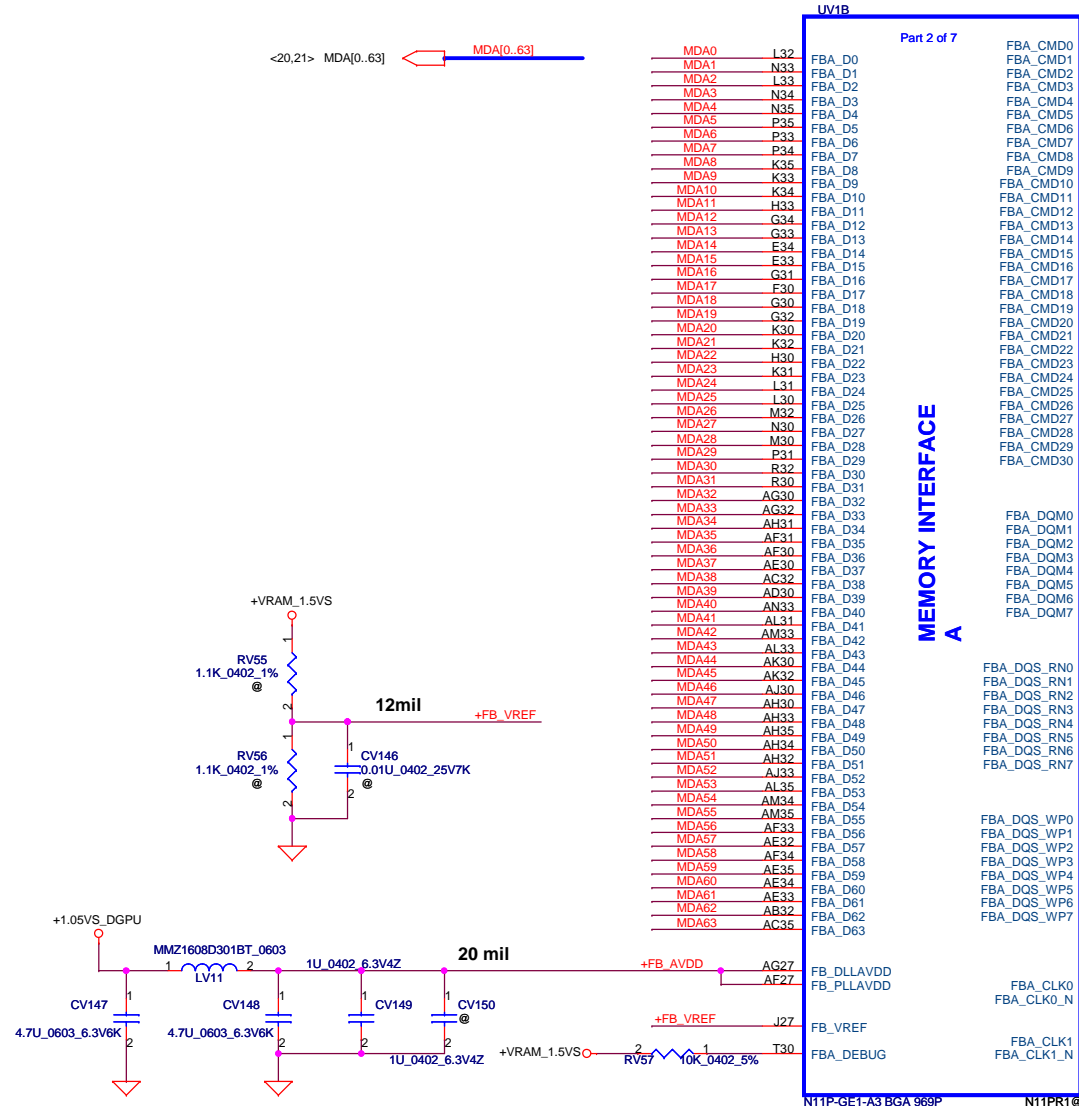
16A for N11M-GE1 & N11M-OP1



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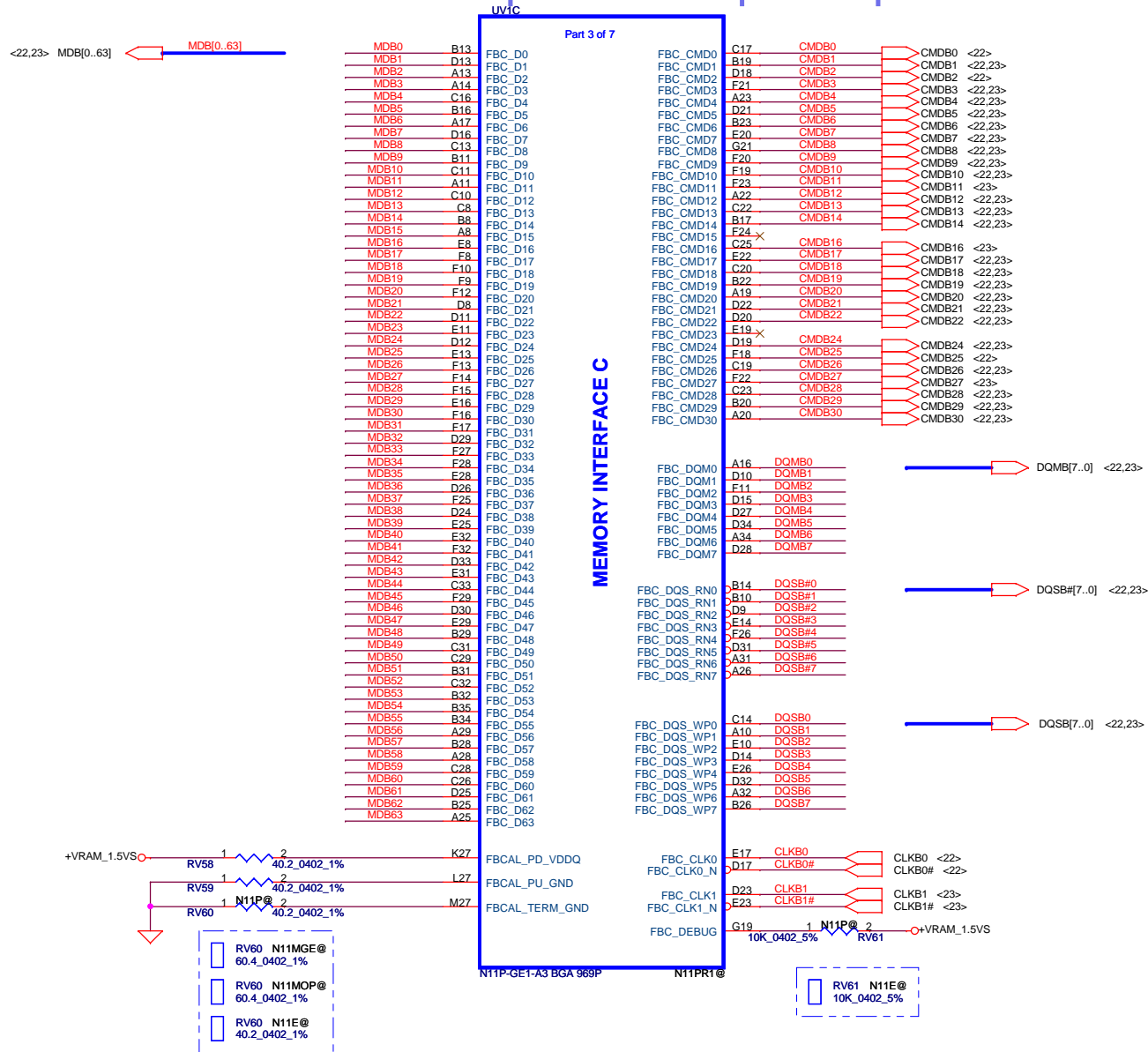


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Mode C - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

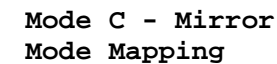


Mode C - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

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Document Number				Rev 2.0	
NWQAA LA-6062P M/B				Date: Wednesday, March 24, 2010	
Sheet 19 of 59				Sheet 19 of 59	

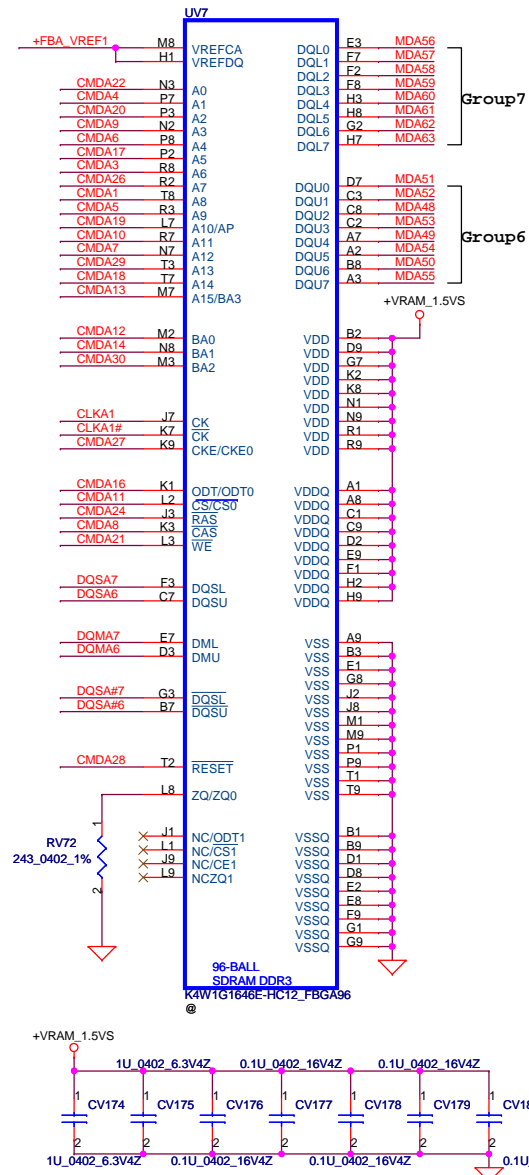
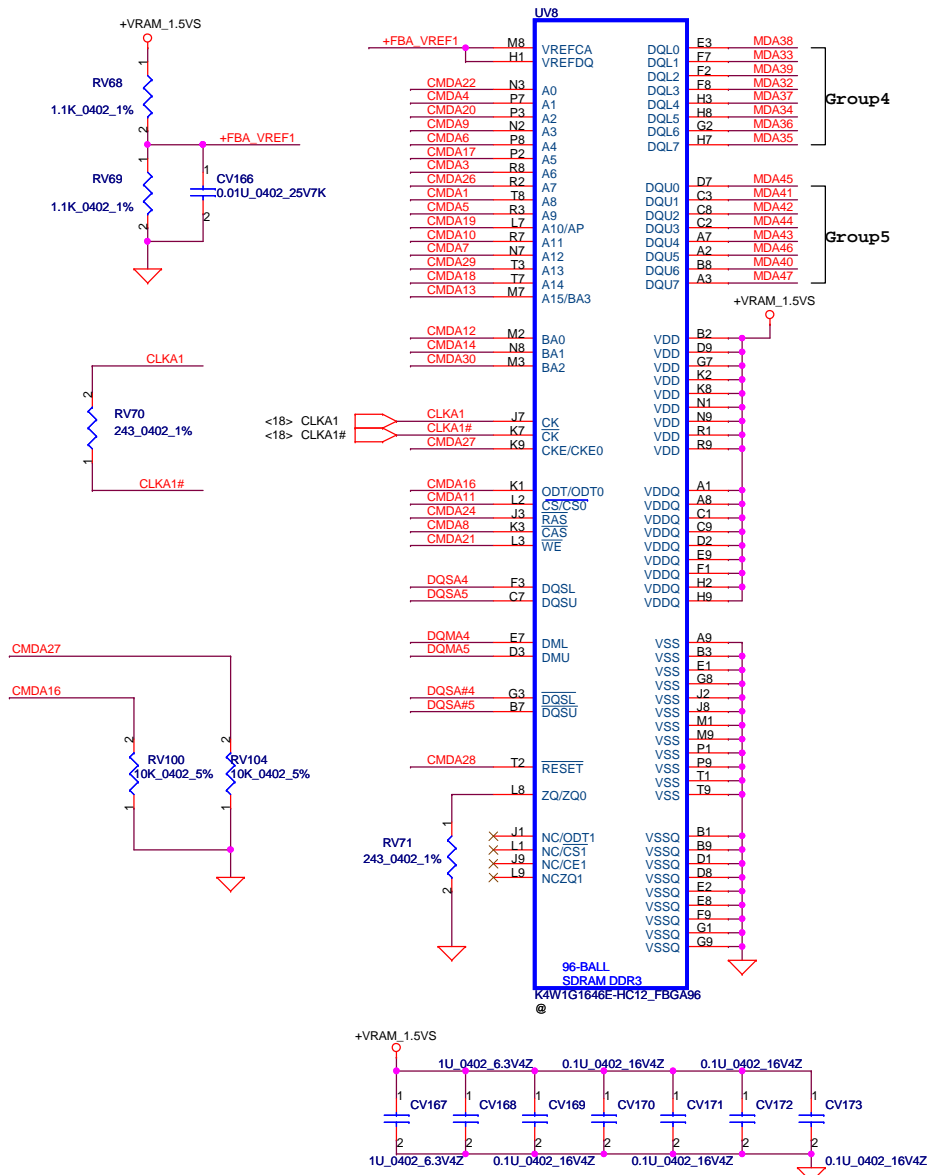
power 32 bits `http://laptopblue.vn`



CMD1
CMD1
CMD1

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Memory Partition A - Upper 32:bits

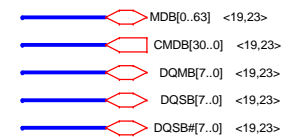
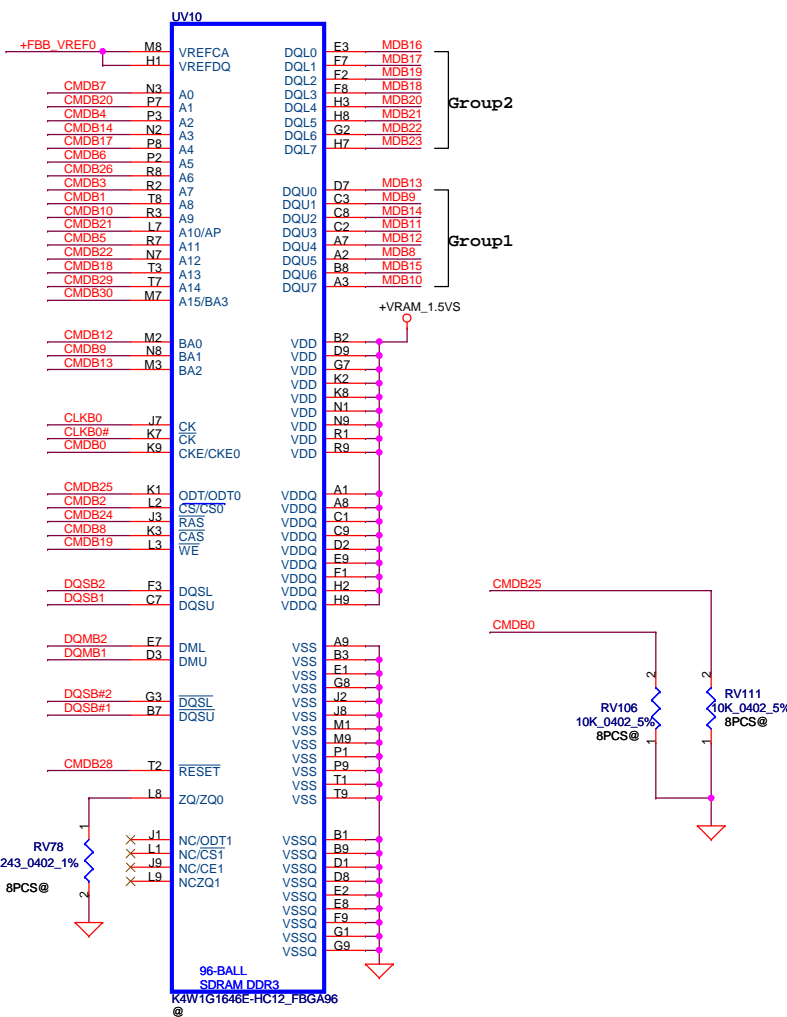
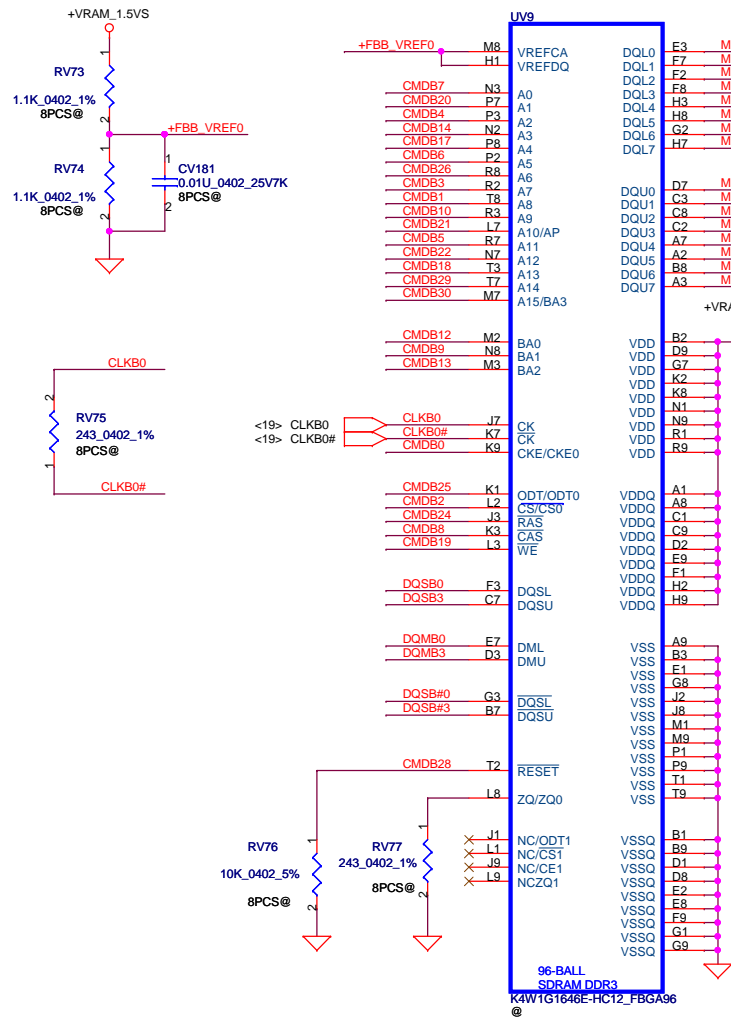


Mode C - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

Memory Partition C - Lower 32 bits

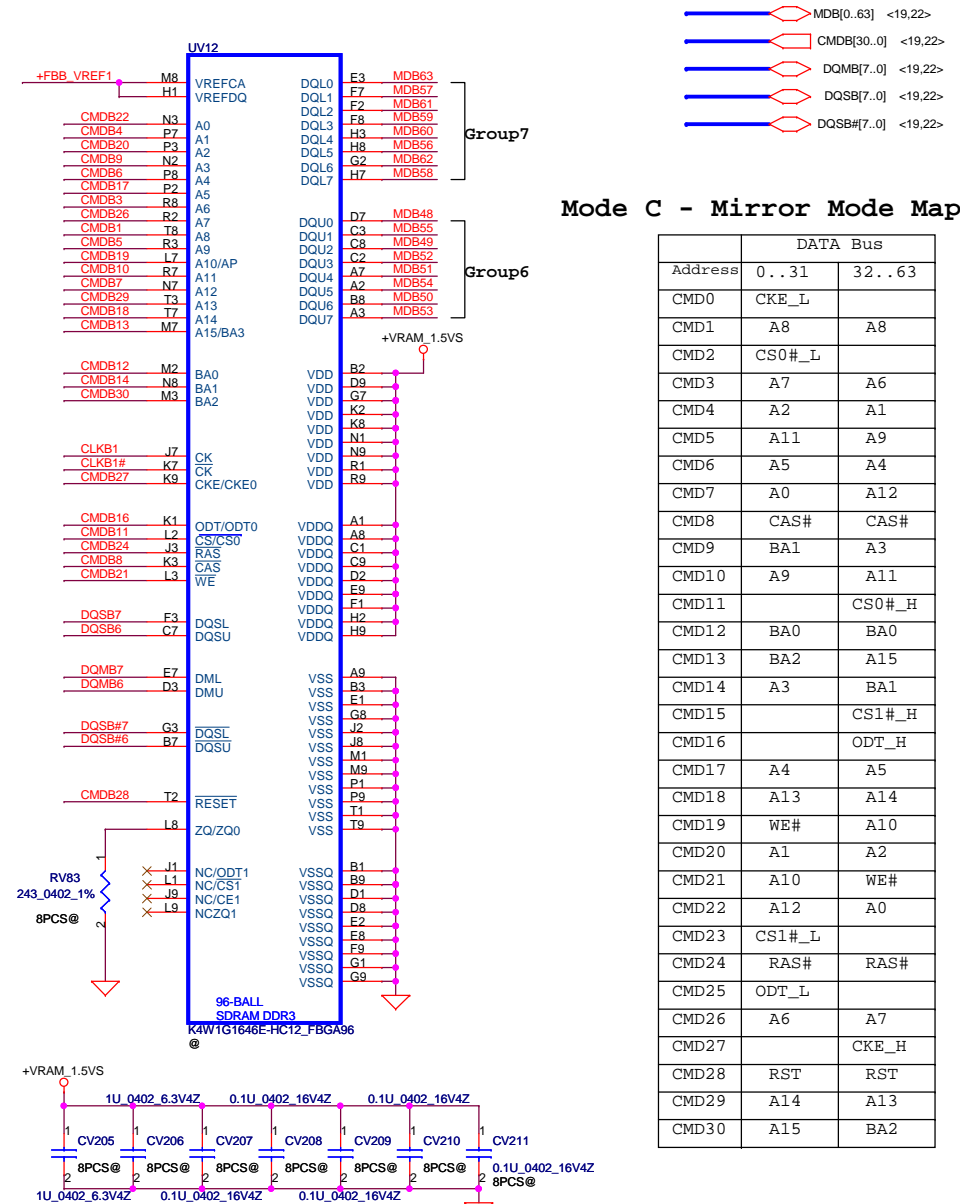
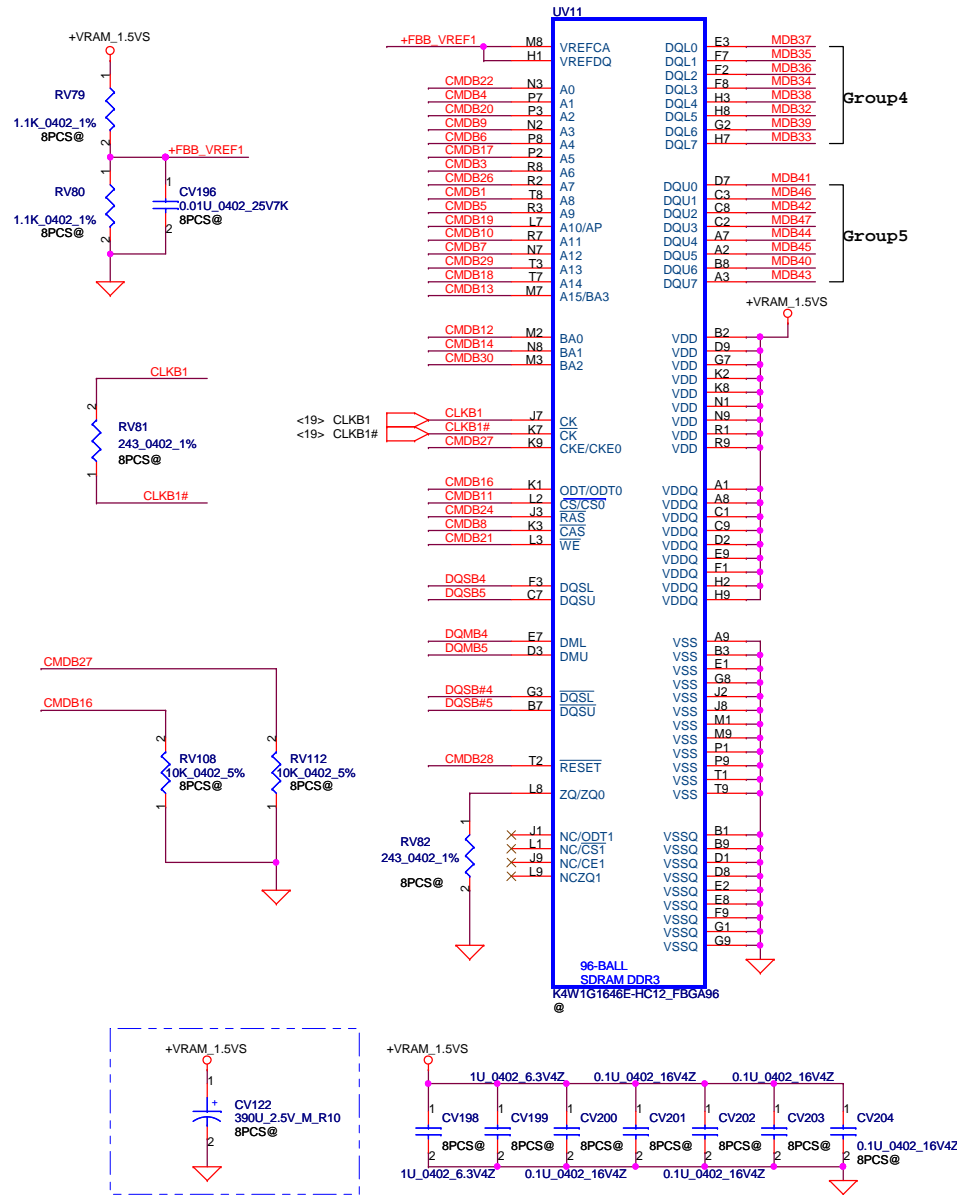
http://laptopblue.vn



Mode C - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

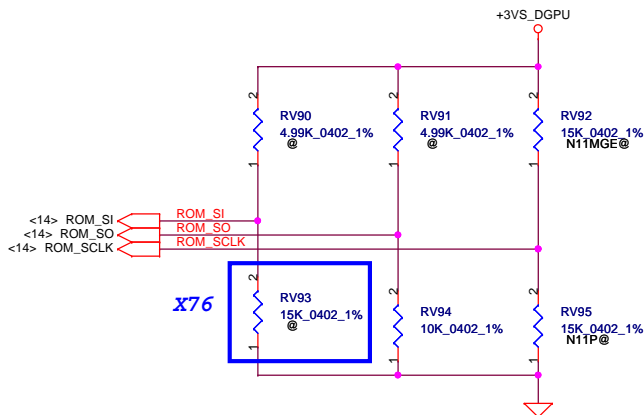
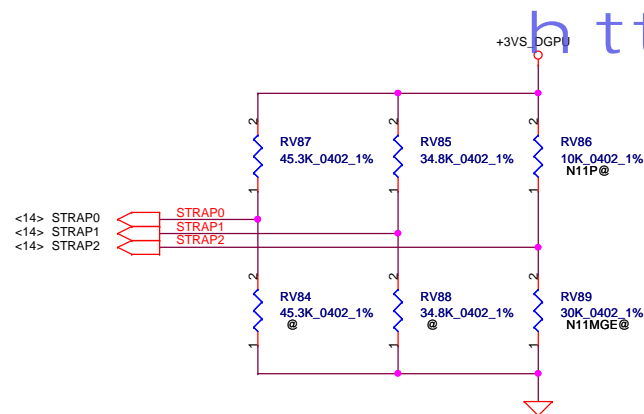
Memory Partition C - Upper 32 bits



Mode C - Mirror Mode Mapping

DATA Bus	
Address	0..31 32..63
CMD0	CKE_L
CMD1	A8
CMD2	CS0#_L
CMD3	A7
CMD4	A2
CMD5	A11
CMD6	A5
CMD7	A0
CMD8	CAS#
CMD9	BA1
CMD10	A9
CMD11	CS0#_H
CMD12	BA0
CMD13	BA2
CMD14	A3
CMD15	CS1#_H
CMD16	ODT_H
CMD17	A4
CMD18	A13
CMD19	WE#
CMD20	A1
CMD21	A10
CMD22	A12
CMD23	CS1#_L
CMD24	RAS#
CMD25	ODT_L
CMD26	A6
CMD27	CKE_H
CMD28	RST
CMD29	A14
CMD30	A15

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Issued Date	2009/01/01	Deciphered Date	2010/01/01	VRAM C Upper	
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	DeviceID	ROM_SCLK	STRAP2
N11M-GE1	0xA75	Pull up 15K	Pull down 30K
N11P-GE1	0xA29	Pull down 15K	Pull up 10K
N11M-OP1	0xA72	Pull up 15K	Pull down 15K
N11E-GE1(LP)	0xCB0	Pull up 15K	Pull down 5K

Hynix H5TQ1G63BFR-12C SA000032400	512M	0010	PD 15K
	1G	0010	PD 15K
Samsung K4W1G1646E-HC12 SA000035700	512M	0011	PD 20K
	1G	0011	PD 20K

SD034150280

SD034200280

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLEN_TERM
ROM_SI	+3VS_DGPU	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS_DGPU	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM (Default)
1	BIOS ROM is present

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
1110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

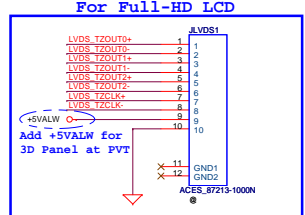
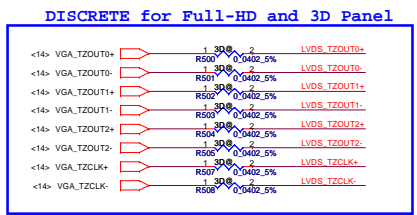
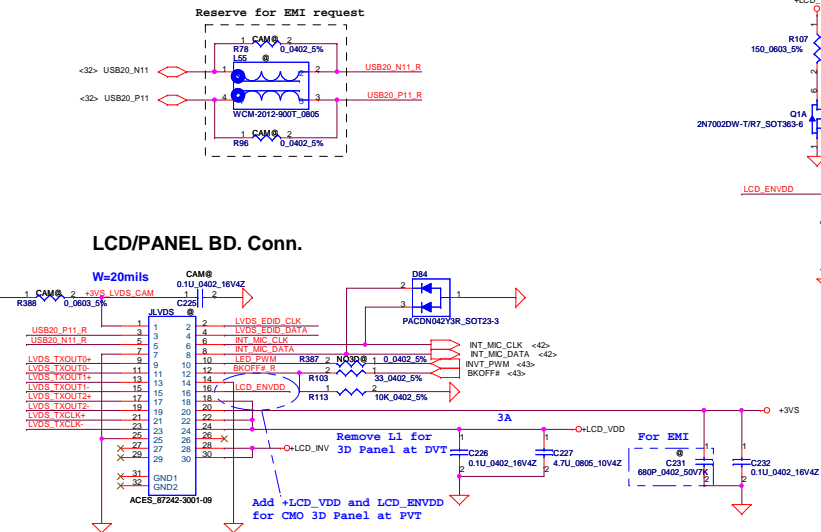
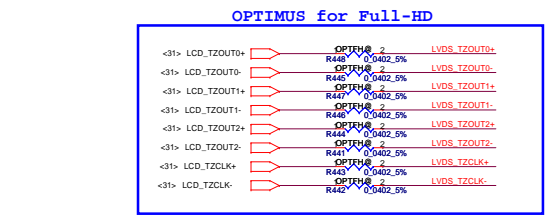
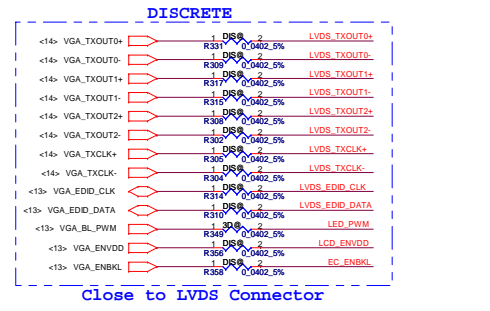
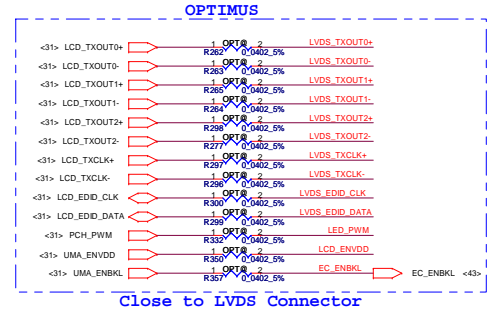
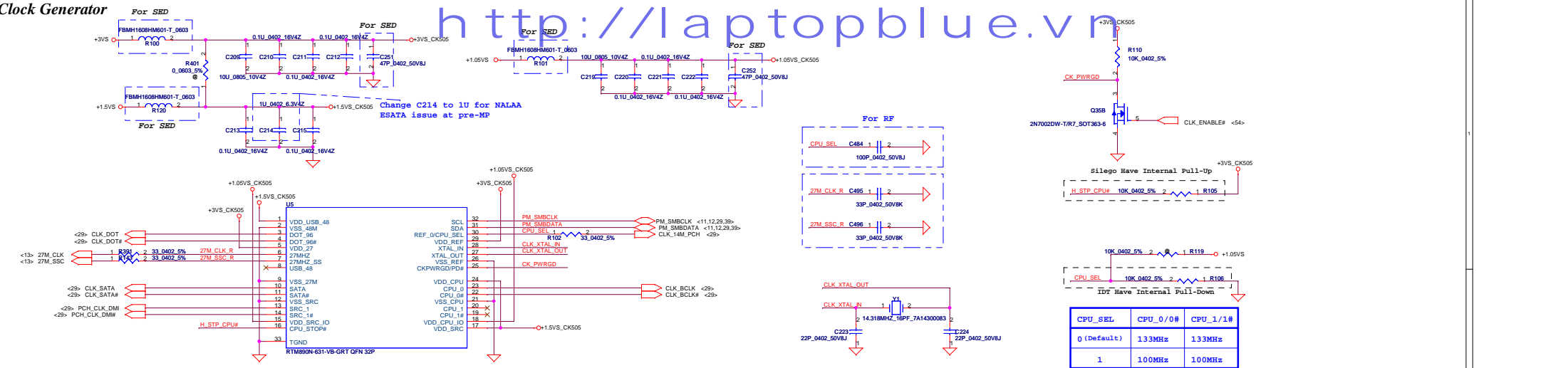
SLOT_CLOCK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

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Clock Generator



OPTIMUS

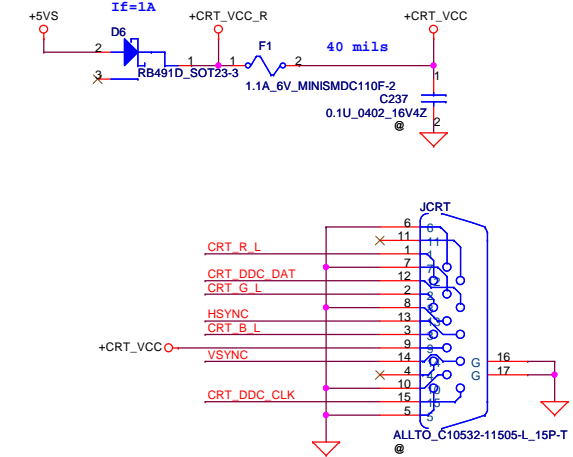
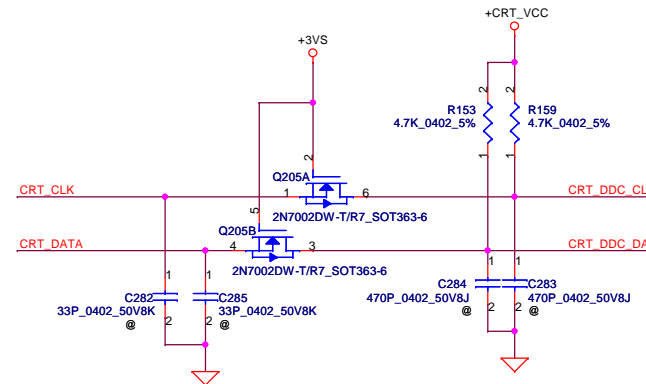
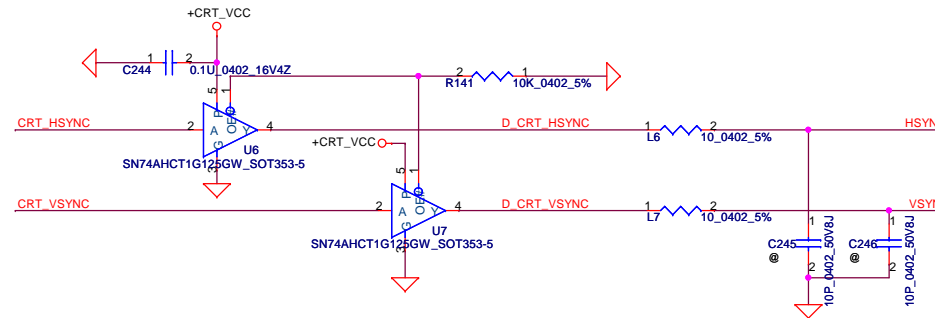
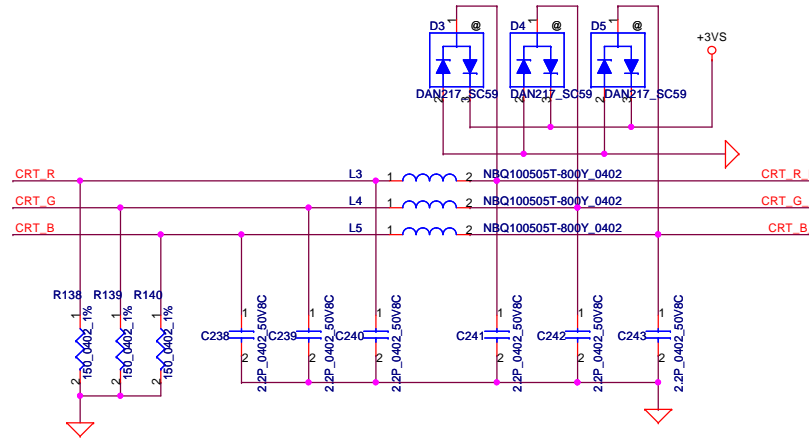
<31> UMA_CRT_R	1 OPT@ 2	CRT_R
<31> UMA_CRT_G	1 OPT@ 2	CRT_G
<31> UMA_CRT_B	1 OPT@ 2	CRT_B
<31> UMA_CRT_HSYNC	1 OPT@ 2	CRT_HSYNC
<31> UMA_CRT_VSYNC	1 OPT@ 2	CRT_VSYNC
<31> UMA_CRT_CLK	1 OPT@ 2	CRT_CLK
<31> UMA_CRT_DATA	1 OPT@ 2	CRT_DATA

Close to CRT Connector

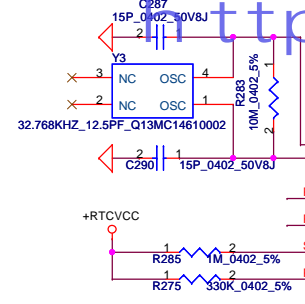
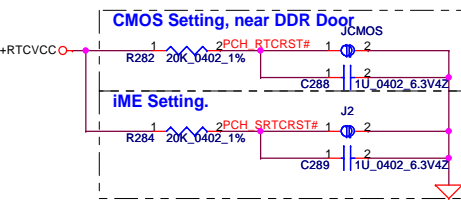
DISCRETE

<13> VGA_CRT_R	1 DIS@ 2	CRT_R
<13> VGA_CRT_G	1 DIS@ 2	CRT_G
<13> VGA_CRT_B	1 DIS@ 2	CRT_B
<13> VGA_CRT_HSYNC	1 DIS@ 2	CRT_HSYNC
<13> VGA_CRT_VSYNC	1 DIS@ 2	CRT_VSYNC
<13> VGA_CRT_CLK	1 DIS@ 2	CRT_CLK
<13> VGA_CRT_DATA	1 DIS@ 2	CRT_DATA

Close to CRT Connector



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Integrated SUS 1.05V VRM Enable

PCH_INTVRMEN High - Enable Internal VRs (must be always pulled high)

HDA_SYNC

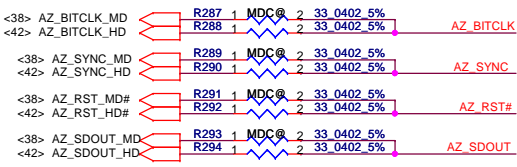
This signal has a weak internal pull down.
H=>On Die PLL is supplied by 1.5V
L=>On Die PLL is supplied by 1.8V

HDA_SDO

This signal has a weak internal pull down.
This signal can't PU

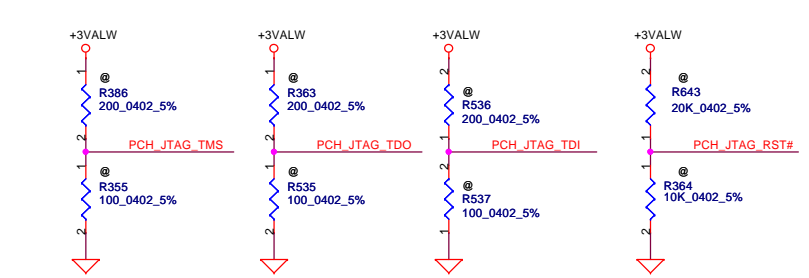
Flash Descriptor Security Override

HDA_DOCK_EN# Low = Enabled
High = Disabled *



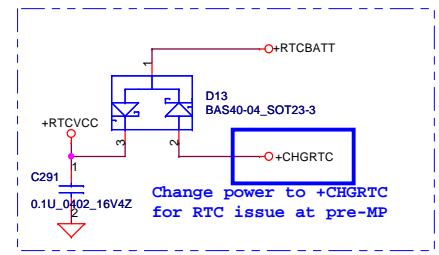
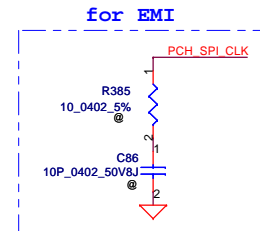
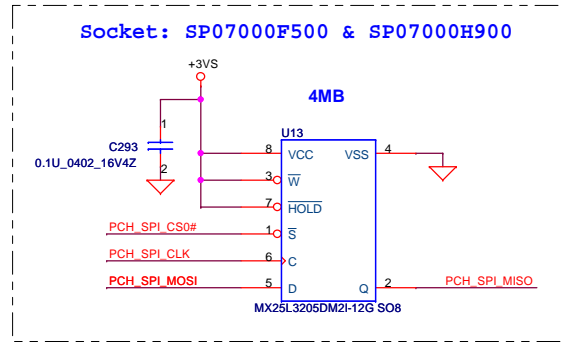
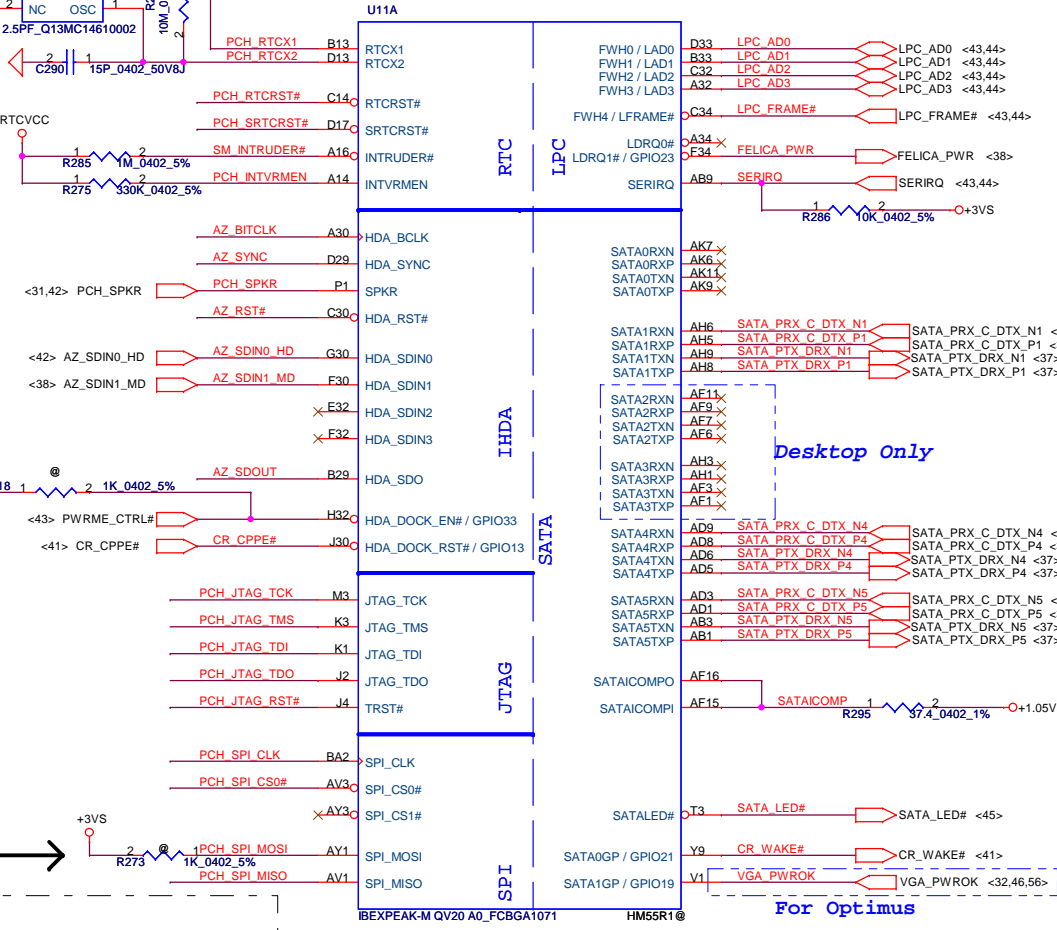
ITPM Enabled Internal: Pull down 20k

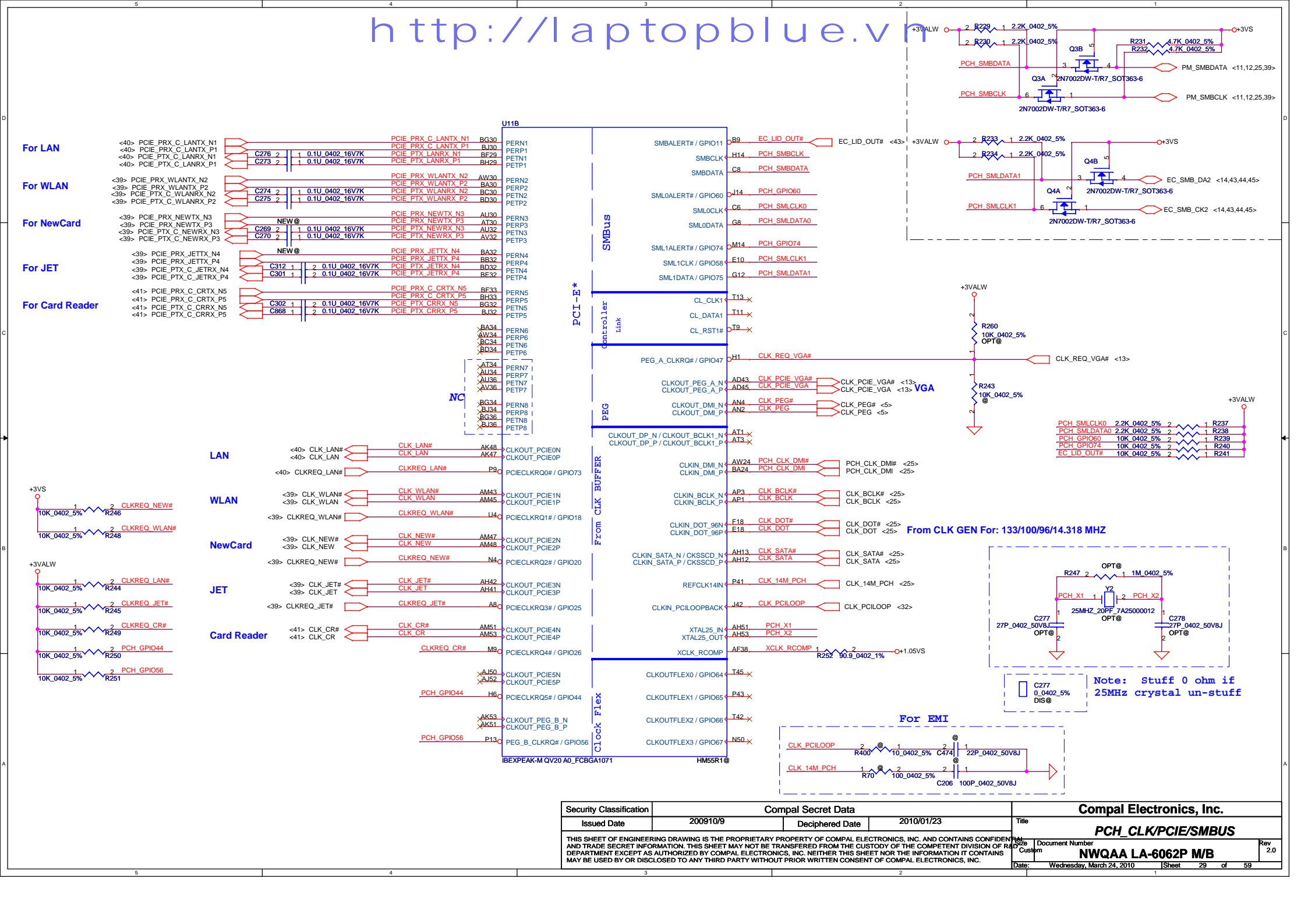
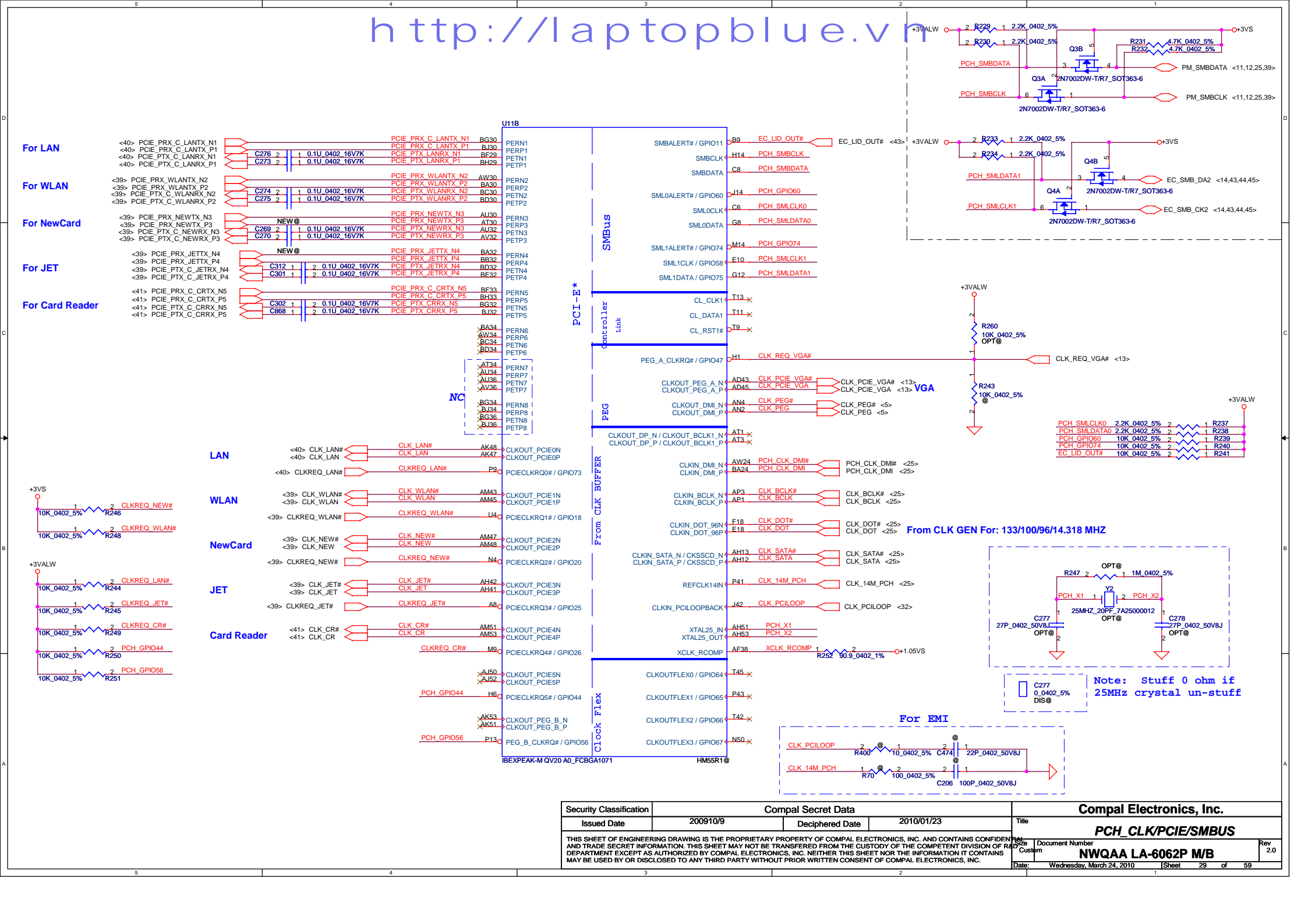
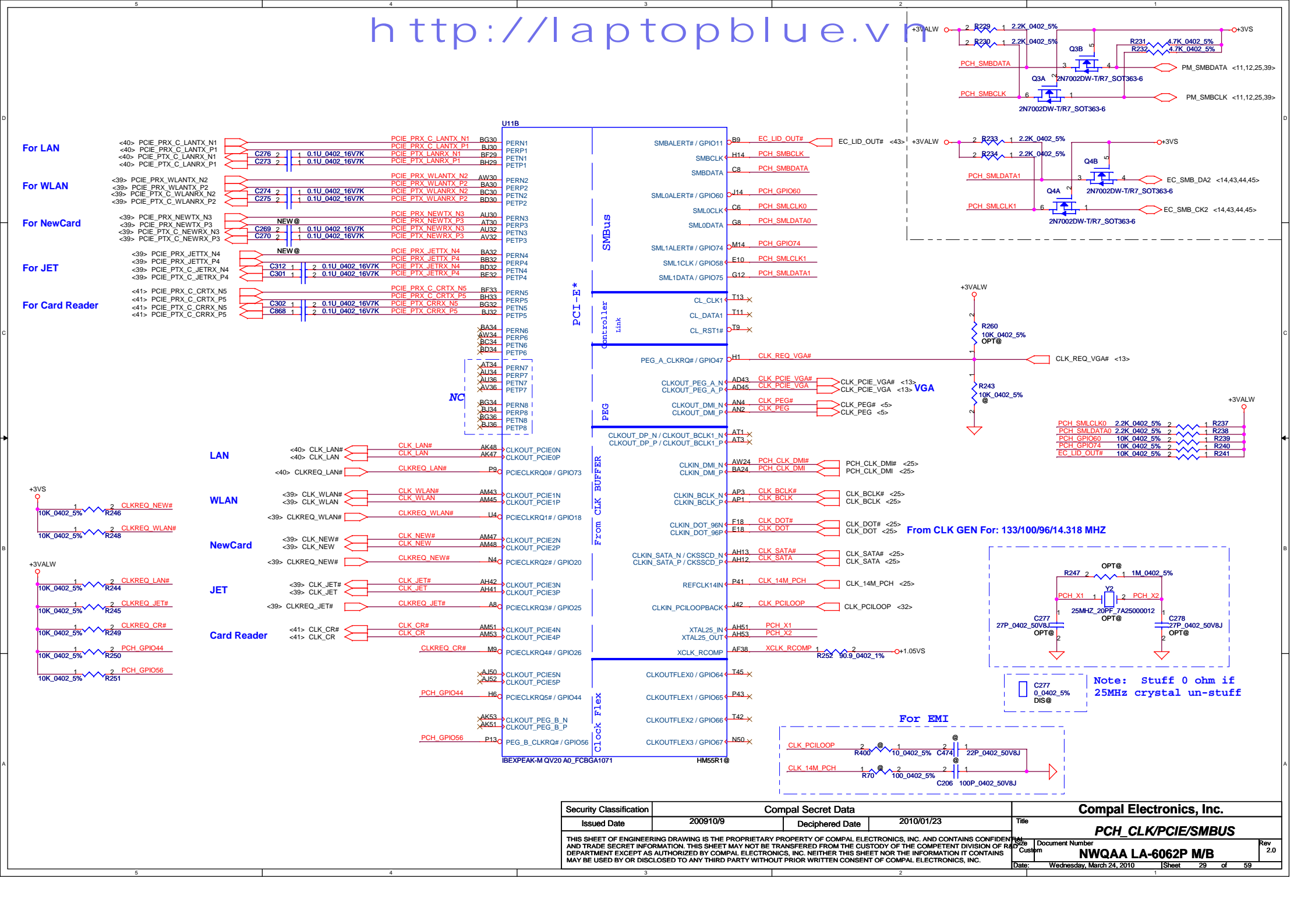
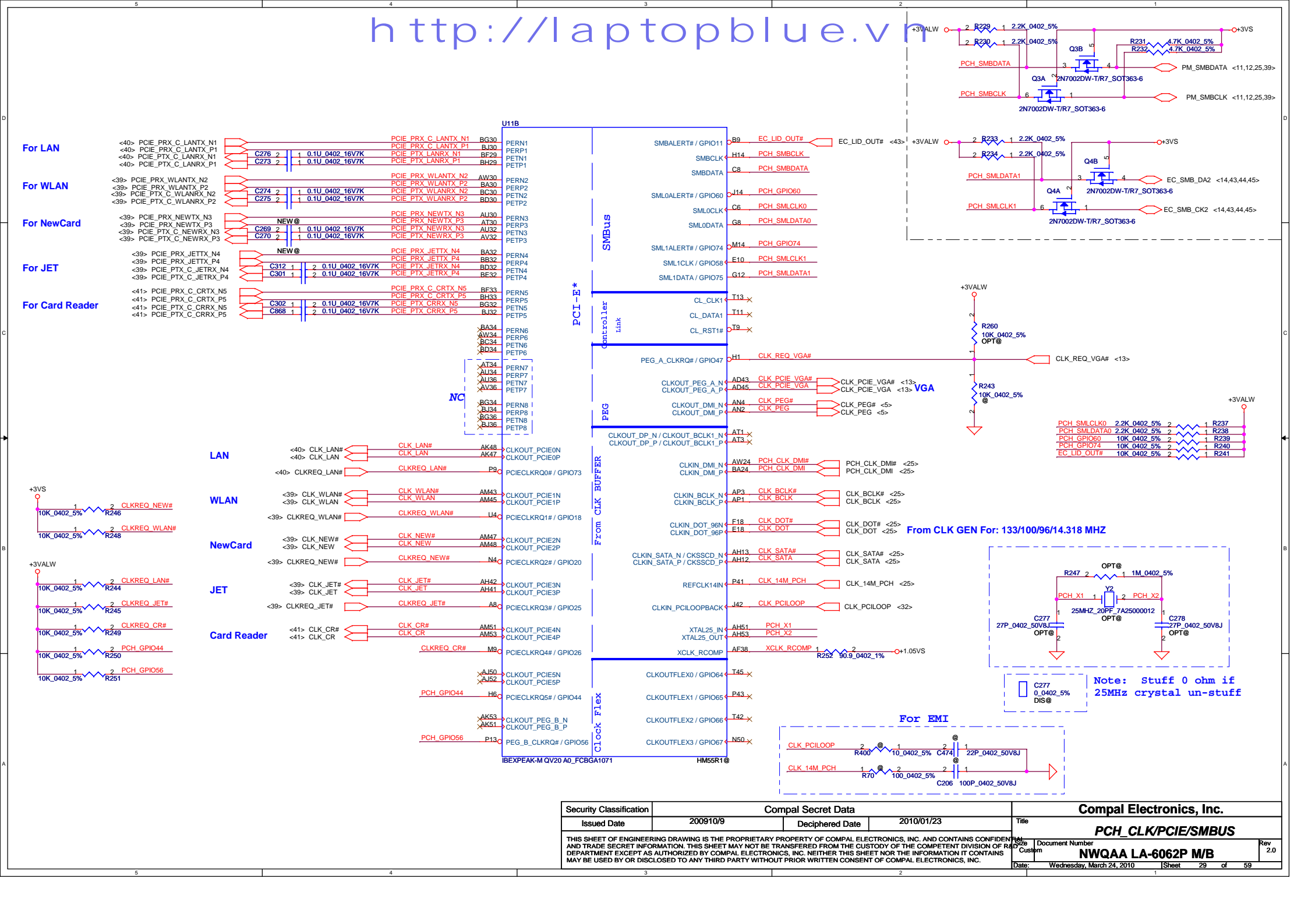
SPI_MOSI High = Enabled
Low = Disabled (Default)

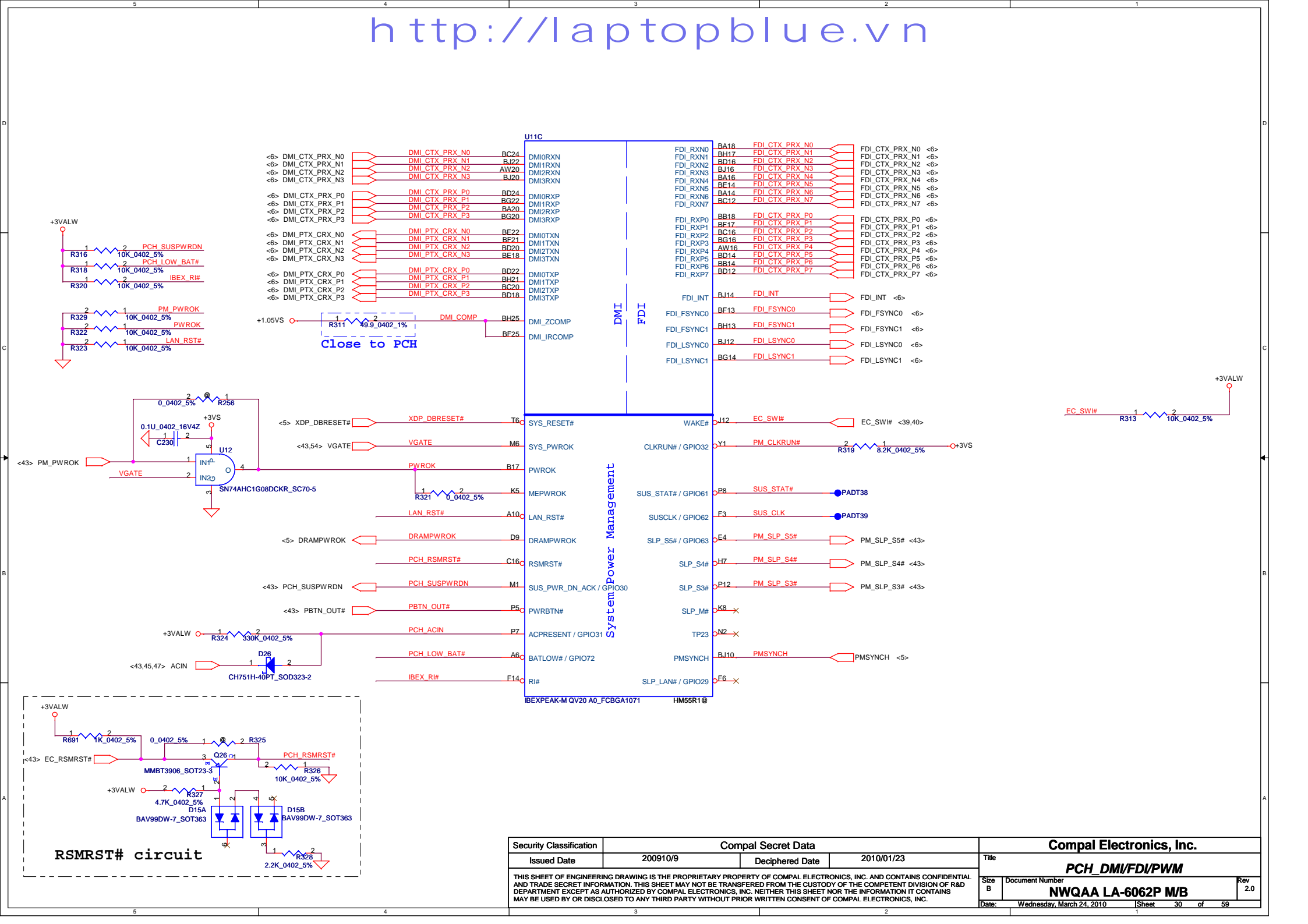


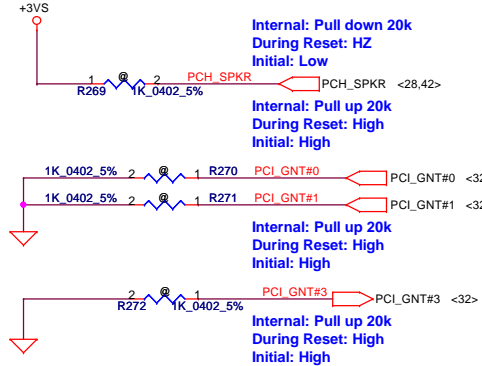
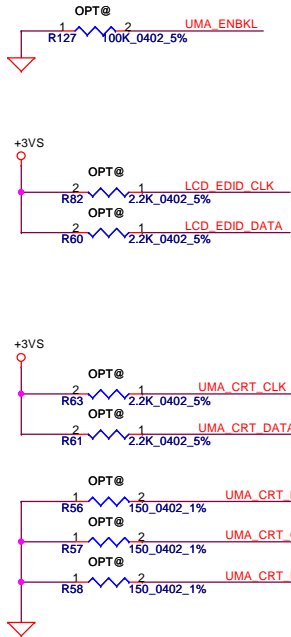
06/01 change R156 from 4.7K to 51 ohm

PCH Pin	RefDes	PCH JTAG Enable		PCH JTAG Disable (Default)	
		ES1	ES2	ES1	ES2
PCH_JTAG_TDO	R358	No Install	200ohm	No Install	No Install
PCH_JTAG_TMS	R355	No Install	100ohm	No Install	No Install
PCH_JTAG_TDI	R354	100ohm	100ohm	No Install	No Install
PCH_JTAG_RST#	R356	200ohm	200ohm	20Kohm	No Install
PCH_JTAG_TCK	R156	51ohm	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R643	20Kohm	20Kohm	No Install	No Install
PCH_JTAG_RST#	R353	10Kohm	10Kohm	No Install	No Install



[illegible]

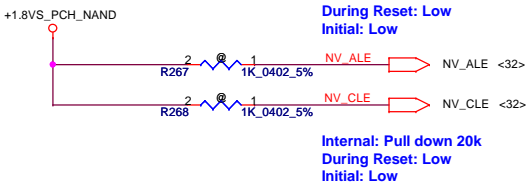




NO REBOOT Strap		
PCH_SPKR	Low= Disable High= Enable	

Boot BIOS Strap		
PCI_GNT#1	PCI_GNT#0	Boot BIOS Location
0	0	LPC (Default)
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

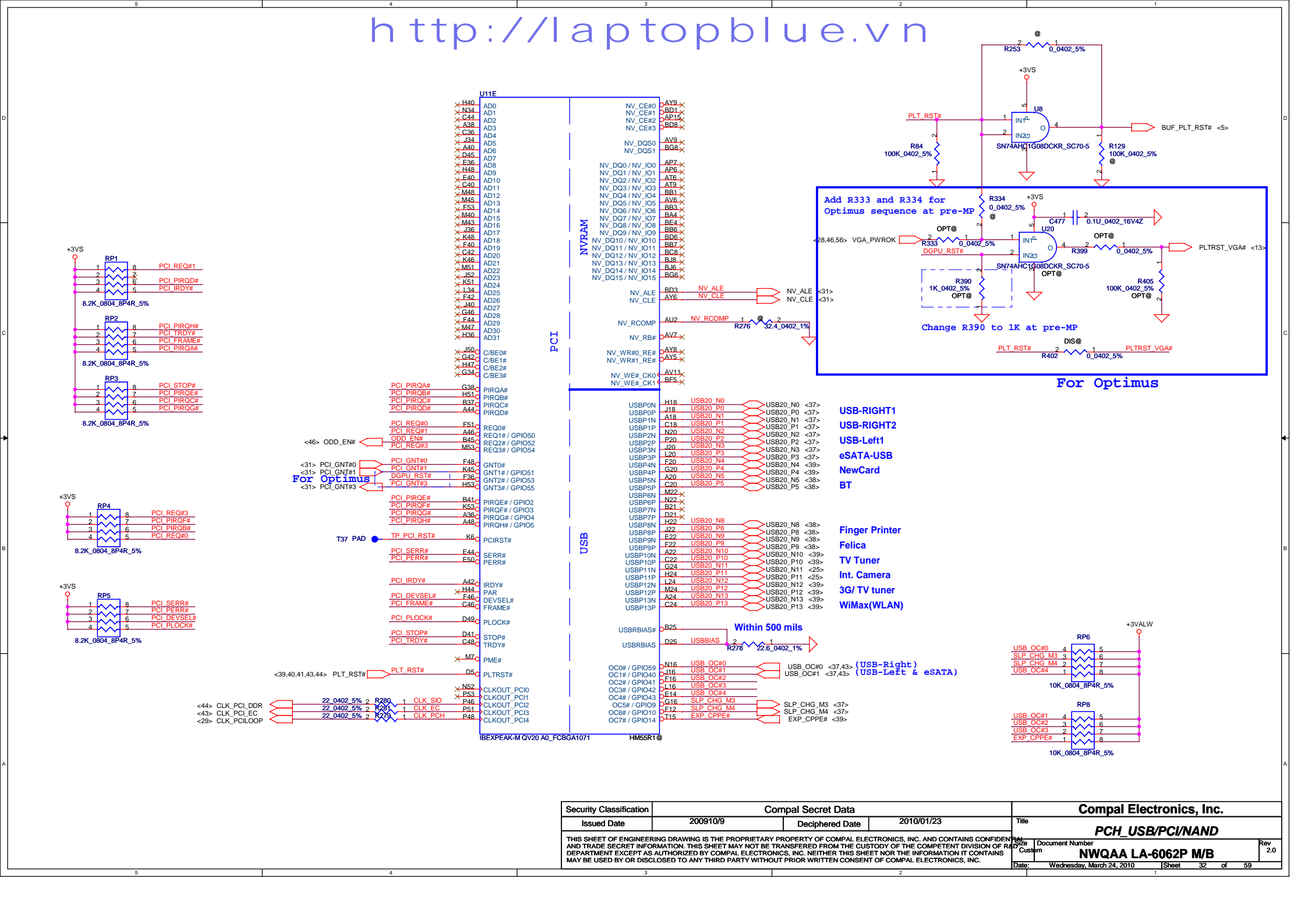
A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= A16 swap override Disable



Danbury Technology Enabled	
NV_ALE	High = Enabled Low = Disabled (Default)

DMI Termination Voltage	
NV_CLE	Low= Set to Vss (Default) High= Set to Vcc

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Issued Date	200910/9		Deciphered Date	2010/01/23		Title	PCH CRT/LVDS/HDMI/STRAP	
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The diagram illustrates the internal components of a laptop, specifically the USB, PCI, and NVRAM sections. It shows various connectors, resistors, capacitors, and integrated circuits. Key components include the USB controller (U11E), PCI controller (U11E), and NVRAM (U11E). The diagram is labeled with various signals and pin numbers, and includes a table of components and their values. A large blue box highlights the USB section, and a smaller blue box highlights the PCI section. The diagram is titled "PCH USB/PCI/NAND" and includes a security classification table at the bottom.

Security Classification

Security Classification	Compal Secret Data
Issued Date	200910/9
Deciphered Date	2010/01/23

Compal Electronics, Inc.

PCH USB/PCI/NAND

Document Number

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Rev

2.0

Date

Wednesday, March 24, 2010

Sheet

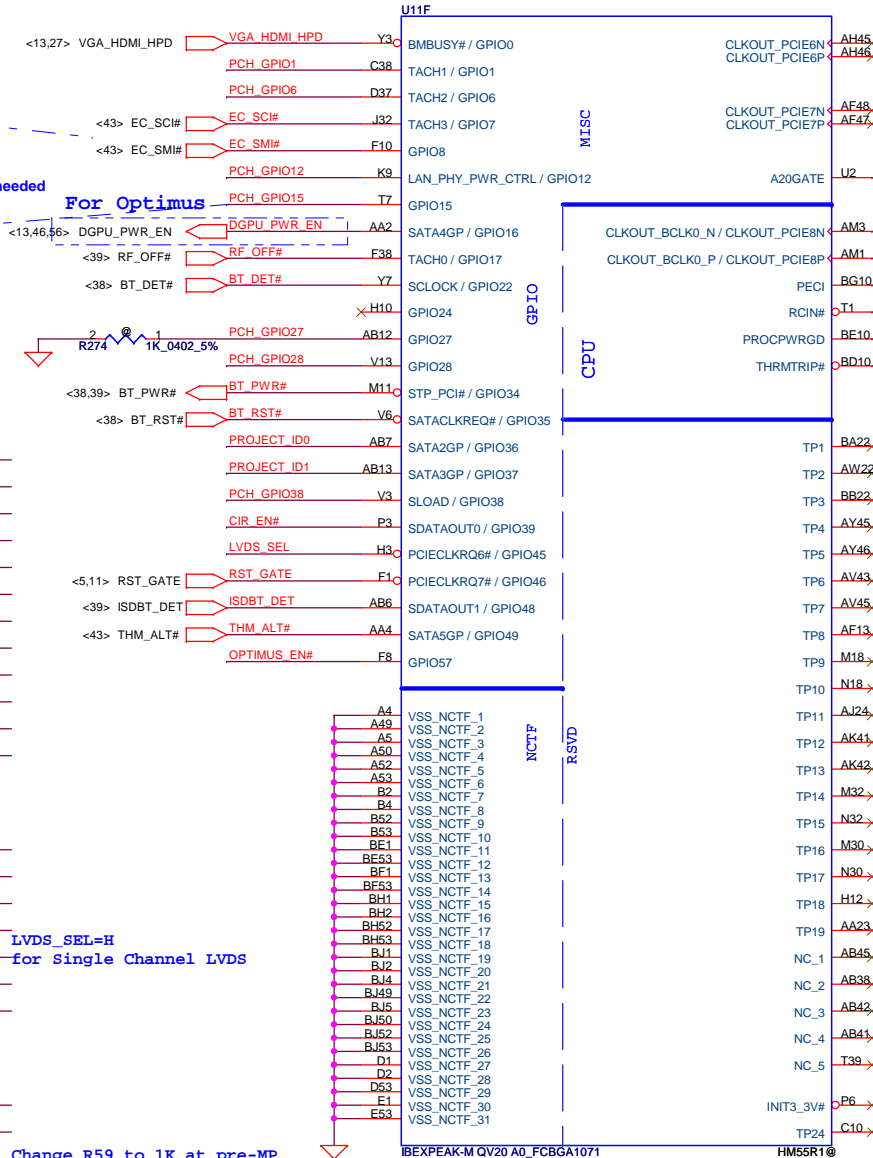
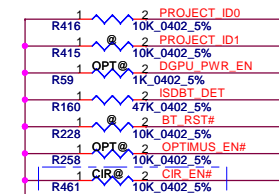
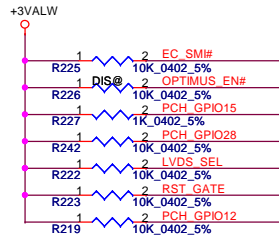
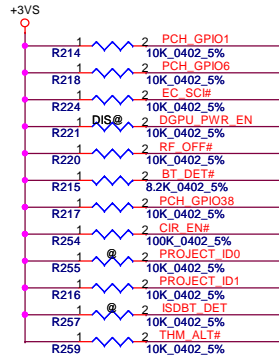
32 of 59

GPIO8
Not pull down
Internal: Pull up 20k
During Reset: High
Initial: High

GPIO15
a Strong pull up may be needed
for GPIO Functionality
Internal: Pull down 20k
During Reset: Low
Initial: Low

On-Die PLL VR

PCH_GPIO27 High = Enabled (Default)
Low = Disabled

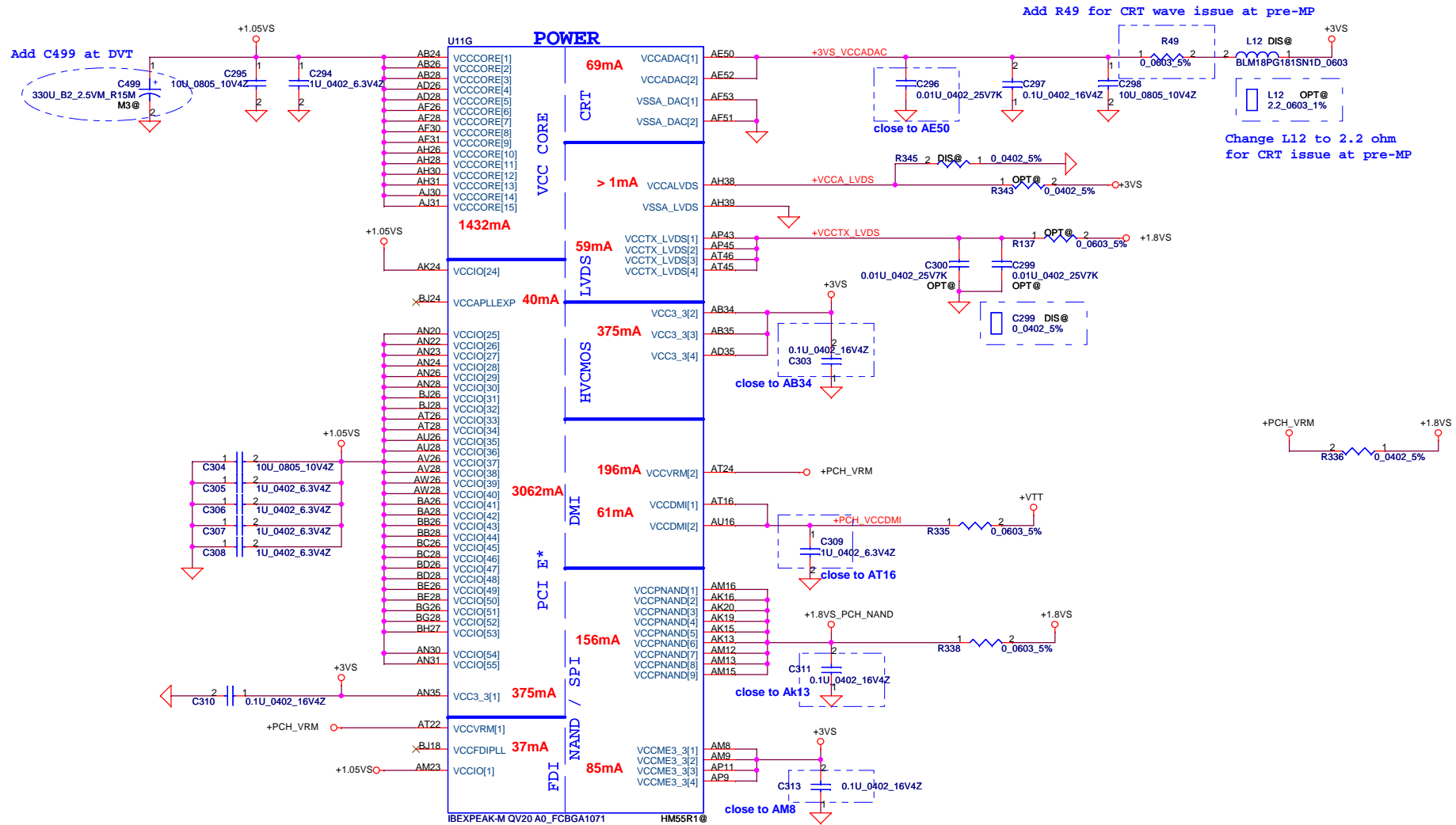


PROJECT_ID1	PROJECT_ID0	2010 Project ID setting
0	0	NDU00/10 (Streamline-M/-S 11.6/13.3")
0	1	NBQAA (Bordeaux 14")
1	0	NWQAA (Marseille 16")
1	1	NALAA (Hamburg 17.3")

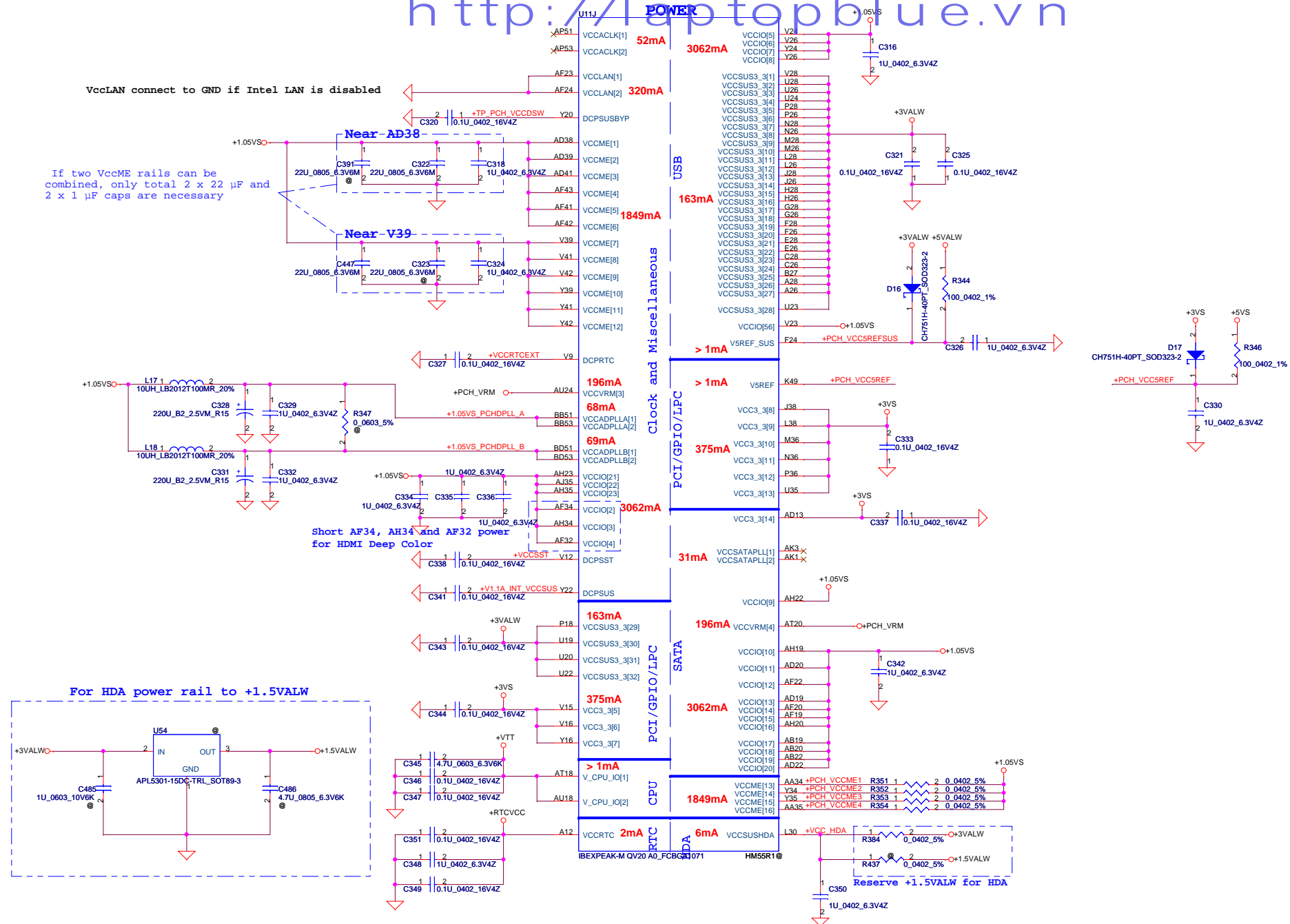
Not pull low
internal pull up
Internal: Pull up 20k
During Reset: High
Initial: High

Add OPTIMUS_EN# at DVT		
OPTIMUS_EN#	H	L
SKU	Discrete	Optimus

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Size B	Document Number	Rev 2.0		Date: Wednesday, March 24, 2010	
Sheet 33		of 59			



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				Customer	Rev 2		
				Date:	Tuesday, March 23, 2010	Sheet 35 of 59	

U11I			H49
AY7	VSS[159]	VSS[259]	H5
B11	VSS[160]	VSS[260]	J24
B15	VSS[161]	VSS[261]	K11
B19	VSS[162]	VSS[262]	K43
B23	VSS[163]	VSS[263]	K47
B31	VSS[164]	VSS[264]	K7
B35	VSS[165]	VSS[265]	L14
B39	VSS[166]	VSS[266]	L18
B43	VSS[167]	VSS[267]	L2
B47	VSS[168]	VSS[268]	L22
B7	VSS[169]	VSS[269]	L32
BC12	VSS[170]	VSS[270]	L36
BB12	VSS[171]	VSS[271]	L40
BB16	VSS[172]	VSS[272]	L52
BB20	VSS[173]	VSS[273]	M12
BB24	VSS[174]	VSS[274]	M16
BB30	VSS[175]	VSS[275]	M20
BB34	VSS[176]	VSS[276]	N38
BB38	VSS[177]	VSS[277]	M34
BB42	VSS[178]	VSS[278]	M38
BB46	VSS[179]	VSS[279]	M42
BB50	VSS[180]	VSS[280]	M46
BC10	VSS[181]	VSS[281]	M49
BC14	VSS[182]	VSS[282]	M5
BC18	VSS[183]	VSS[283]	M8
BC2	VSS[184]	VSS[284]	N24
BC22	VSS[185]	VSS[285]	P11
BC32	VSS[186]	VSS[286]	AD15
BC36	VSS[187]	VSS[287]	P22
BC40	VSS[188]	VSS[288]	P30
BC44	VSS[189]	VSS[289]	P32
BC52	VSS[190]	VSS[290]	P34
BH0	VSS[191]	VSS[291]	P42
BD48	VSS[192]	VSS[292]	P45
BD49	VSS[193]	VSS[293]	P47
BD5	VSS[194]	VSS[294]	R2
BE12	VSS[195]	VSS[295]	R52
BE16	VSS[196]	VSS[296]	T12
BE20	VSS[197]	VSS[297]	T41
BE24	VSS[198]	VSS[298]	T46
BE30	VSS[199]	VSS[299]	T49
BE34	VSS[200]	VSS[300]	T5
BE38	VSS[201]	VSS[301]	T8
BE42	VSS[202]	VSS[302]	U30
BE46	VSS[203]	VSS[303]	U31
BE48	VSS[204]	VSS[304]	U32
BE50	VSS[205]	VSS[305]	U34
BE6	VSS[206]	VSS[306]	P38
BE8	VSS[207]	VSS[307]	V11
BF3	VSS[208]	VSS[308]	V19
BF49	VSS[209]	VSS[309]	V20
BF51	VSS[210]	VSS[310]	V22
BG18	VSS[211]	VSS[311]	V30
BG24	VSS[212]	VSS[312]	V31
BG4	VSS[213]	VSS[313]	V32
BG50	VSS[214]	VSS[314]	V34
BH11	VSS[215]	VSS[315]	V35
BH15	VSS[216]	VSS[316]	V38
BH19	VSS[217]	VSS[317]	V43
BH23	VSS[218]	VSS[318]	V45
BH31	VSS[219]	VSS[319]	V46
BH35	VSS[220]	VSS[320]	V47
BH39	VSS[221]	VSS[321]	V49
BH43	VSS[222]	VSS[322]	V5
BH47	VSS[223]	VSS[323]	V7
BH7	VSS[224]	VSS[324]	V8
C12	VSS[225]	VSS[325]	W2
C50	VSS[226]	VSS[326]	W52
D61	VSS[227]	VSS[327]	Y11
E12	VSS[228]	VSS[328]	Y12
E16	VSS[229]	VSS[329]	Y15
E20	VSS[230]	VSS[330]	Y19
E24	VSS[231]	VSS[331]	Y23
E30	VSS[232]	VSS[332]	Y28
E34	VSS[233]	VSS[333]	Y30
E38	VSS[234]	VSS[334]	Y31
E42	VSS[235]	VSS[335]	Y32
E46	VSS[236]	VSS[336]	Y38
E48	VSS[237]	VSS[337]	Y43
E6	VSS[238]	VSS[338]	Y46
F8	VSS[239]	VSS[339]	P49
F49	VSS[240]	VSS[340]	Y5
F5	VSS[241]	VSS[341]	Y6
G10	VSS[242]	VSS[342]	Y8
G14	VSS[243]	VSS[343]	P24
G18	VSS[244]	VSS[344]	T43
G2	VSS[245]	VSS[345]	AD51
G22	VSS[246]	VSS[346]	AT8
G32	VSS[247]	VSS[347]	AD47
G36	VSS[248]	VSS[348]	Y47
G40	VSS[249]	VSS[349]	AT12
G44	VSS[250]	VSS[350]	AM6
G52	VSS[251]	VSS[351]	AT13
AF39	VSS[252]	VSS[352]	AM5
H16	VSS[253]	VSS[353]	AK45
H20	VSS[254]	VSS[354]	AK38
H30	VSS[255]	VSS[355]	AV14
H34	VSS[256]	VSS[356]	
H38	VSS[257]	VSS[357]	
H42	VSS[258]	VSS[358]	

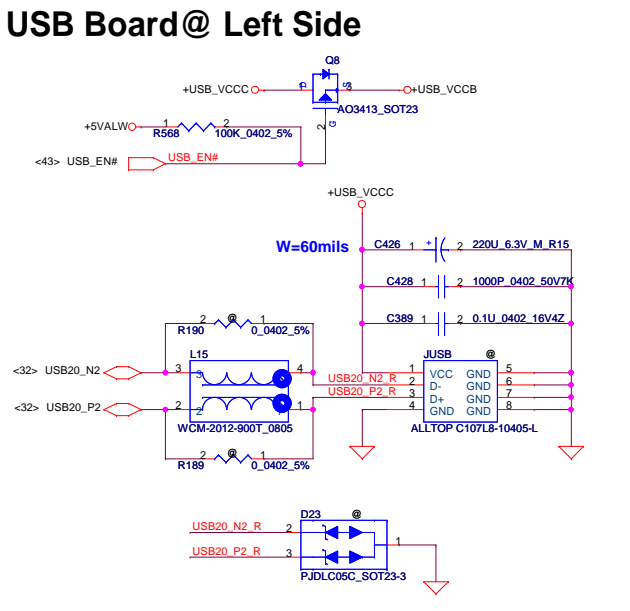
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AB16	VSS[0]		AK31
AA19	VSS[1]	VSS[80]	AK32
AA20	VSS[2]	VSS[81]	AK34
AA22	VSS[3]	VSS[82]	AK35
AM19	VSS[4]	VSS[83]	AK38
AA24	VSS[5]	VSS[84]	AK43
AA26	VSS[6]	VSS[85]	AK46
AA28	VSS[7]	VSS[86]	AK49
AA30	VSS[8]	VSS[87]	AK5
AA31	VSS[9]	VSS[88]	AK8
AB11	VSS[10]	VSS[89]	AL2
AB15	VSS[11]	VSS[90]	AL52
AB23	VSS[12]	VSS[91]	AM11
AB30	VSS[13]	VSS[92]	BB44
AB31	VSS[14]	VSS[93]	AD24
AB32	VSS[15]	VSS[94]	AM20
AB39	VSS[16]	VSS[95]	AM22
AB43	VSS[17]	VSS[96]	AM24
AB47	VSS[18]	VSS[97]	AM26
AB5	VSS[19]	VSS[98]	AM28
AB5	VSS[20]	VSS[99]	BA42
AC3	VSS[21]	VSS[100]	AM30
AC52	VSS[22]	VSS[101]	AM32
AD11	VSS[23]	VSS[102]	AM34
AD12	VSS[24]	VSS[103]	AM35
AD16	VSS[25]	VSS[104]	AM38
AD23	VSS[26]	VSS[105]	AM39
AD30	VSS[27]	VSS[106]	AM42
AD31	VSS[28]	VSS[107]	AM46
AD32	VSS[29]	VSS[108]	AV22
AD34	VSS[30]	VSS[109]	AM7
AD49	VSS[31]	VSS[110]	AA50
AU22	VSS[32]	VSS[111]	BB10
AD42	VSS[33]	VSS[112]	AN32
AD46	VSS[34]	VSS[113]	AN50
T12	VSS[35]	VSS[114]	AN52
AE2	VSS[36]	VSS[115]	AP12
AE4	VSS[37]	VSS[116]	AP46
AF12	VSS[38]	VSS[117]	AP49
Y13	VSS[39]	VSS[118]	AP5
AA49	VSS[40]	VSS[119]	AP8
AF35	VSS[41]	VSS[120]	AR2
AP13	VSS[42]	VSS[121]	AR52
AN34	VSS[43]	VSS[122]	AT11
AF45	VSS[44]	VSS[123]	AT32
AF46	VSS[45]	VSS[124]	AT36
AF49	VSS[46]	VSS[125]	AT41
AF5	VSS[47]	VSS[126]	AT47
AF8	VSS[48]	VSS[127]	AT7
AG2	VSS[49]	VSS[128]	AV12
AG52	VSS[50]	VSS[129]	AV16
AH11	VSS[51]	VSS[130]	AV20
AH15	VSS[52]	VSS[131]	AV24
AH24	VSS[53]	VSS[132]	AV30
AH32	VSS[54]	VSS[133]	AV34
AH34	VSS[55]	VSS[134]	AV38
AV18	VSS[56]	VSS[135]	AV42
AH43	VSS[57]	VSS[136]	AV46
AH47	VSS[58]	VSS[137]	AV49
AH7	VSS[59]	VSS[138]	AV5
AJ19	VSS[60]	VSS[139]	AV8
AJ2	VSS[61]	VSS[140]	AW14
AJ20	VSS[62]	VSS[141]	AW18
AJ28	VSS[63]	VSS[142]	AW2
AJ32	VSS[64]	VSS[143]	BF9
AJ34	VSS[65]	VSS[144]	AW32
AT5	VSS[66]	VSS[145]	AW36
AJ4	VSS[67]	VSS[146]	AW40
AK12	VSS[68]	VSS[147]	AW52
AM41	VSS[69]	VSS[148]	AY11
AN19	VSS[70]	VSS[149]	AY43
AK26	VSS[71]	VSS[150]	AY47
AK22	VSS[72]	VSS[151]	
AK23	VSS[73]	VSS[152]	
AK28	VSS[74]	VSS[153]	
	VSS[75]	VSS[154]	
	VSS[76]	VSS[155]	
	VSS[77]	VSS[156]	
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	VSS[79]	VSS[158]	

IBEXPEAK-M QV20 A0_FCBGA1071 HM55R1@

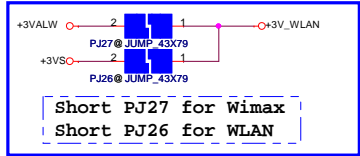
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						Size		Document Number		Rev	
						Custom		NWQAA LA-6062P M/B		2.0	
						Date:		Tuesday, March 23, 2010		Sheet 36 of 59	

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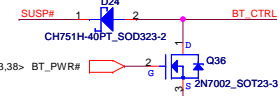
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				Date:	Wednesday, March 24, 2010	Sheet	37 of 59

Slot 1 Half PCIe Mini Card-WLAN/ WiMax



WLAN&BT Combo module circuits		
	BT on module	BT on module
	Enable	Disable
BT_CTRL	H	L
BT_PWR#	L	H

**If +3V_WLAN is +3VS, please remove D24



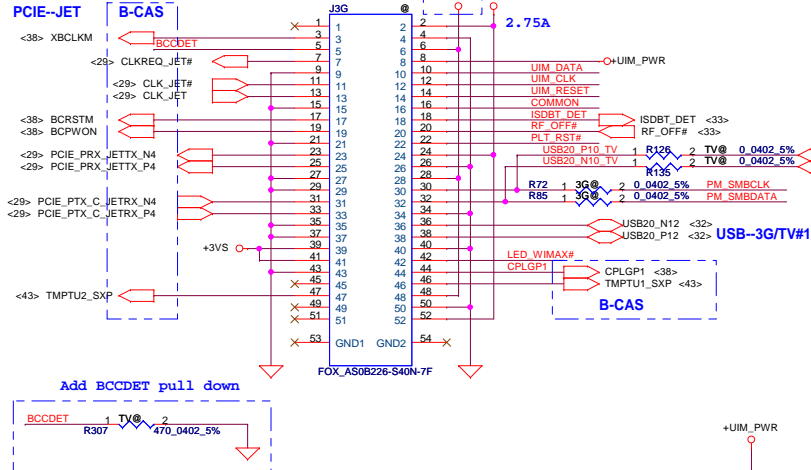
Add BT_CTRL for WLAN & BT Combo module at DVT

Slot 2 Full PCIe Mini Card- 3G/ TV Tuner

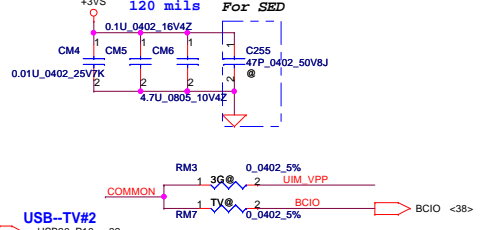
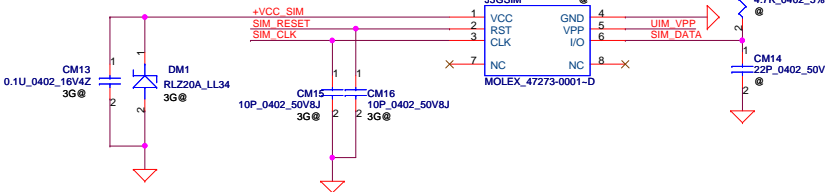
Half PCIe Mini Card- JET

Add +1.5VS for TV tuner

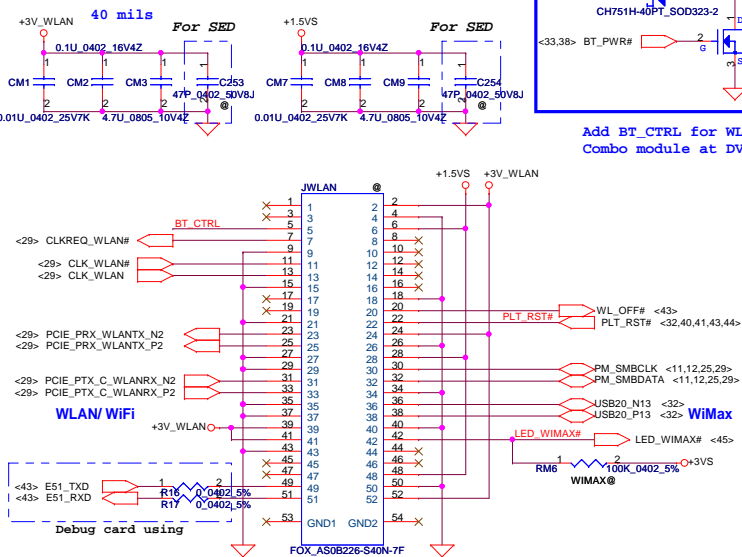
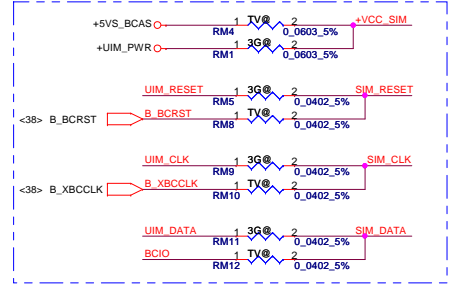
MC770A at PVT



Add BCCDET pull down

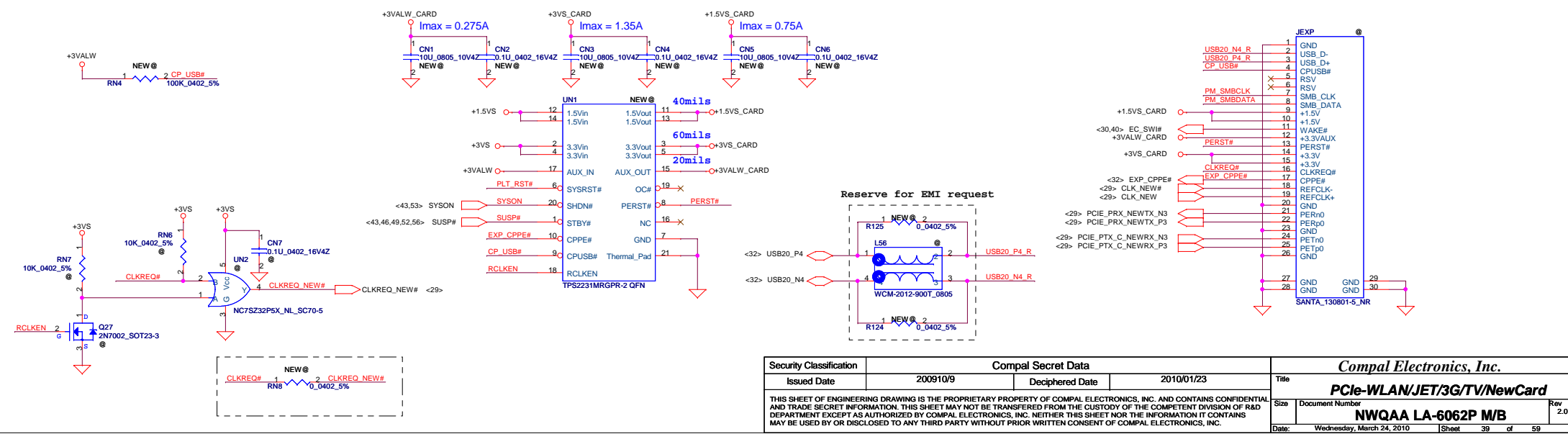


Close to J3G



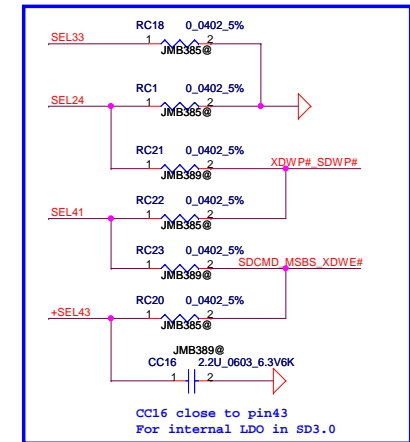
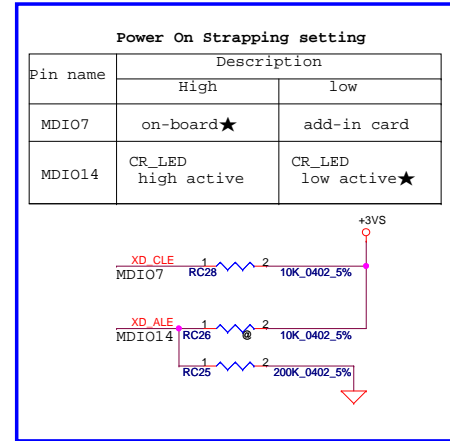
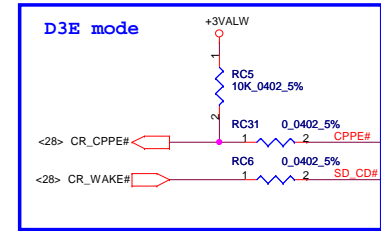
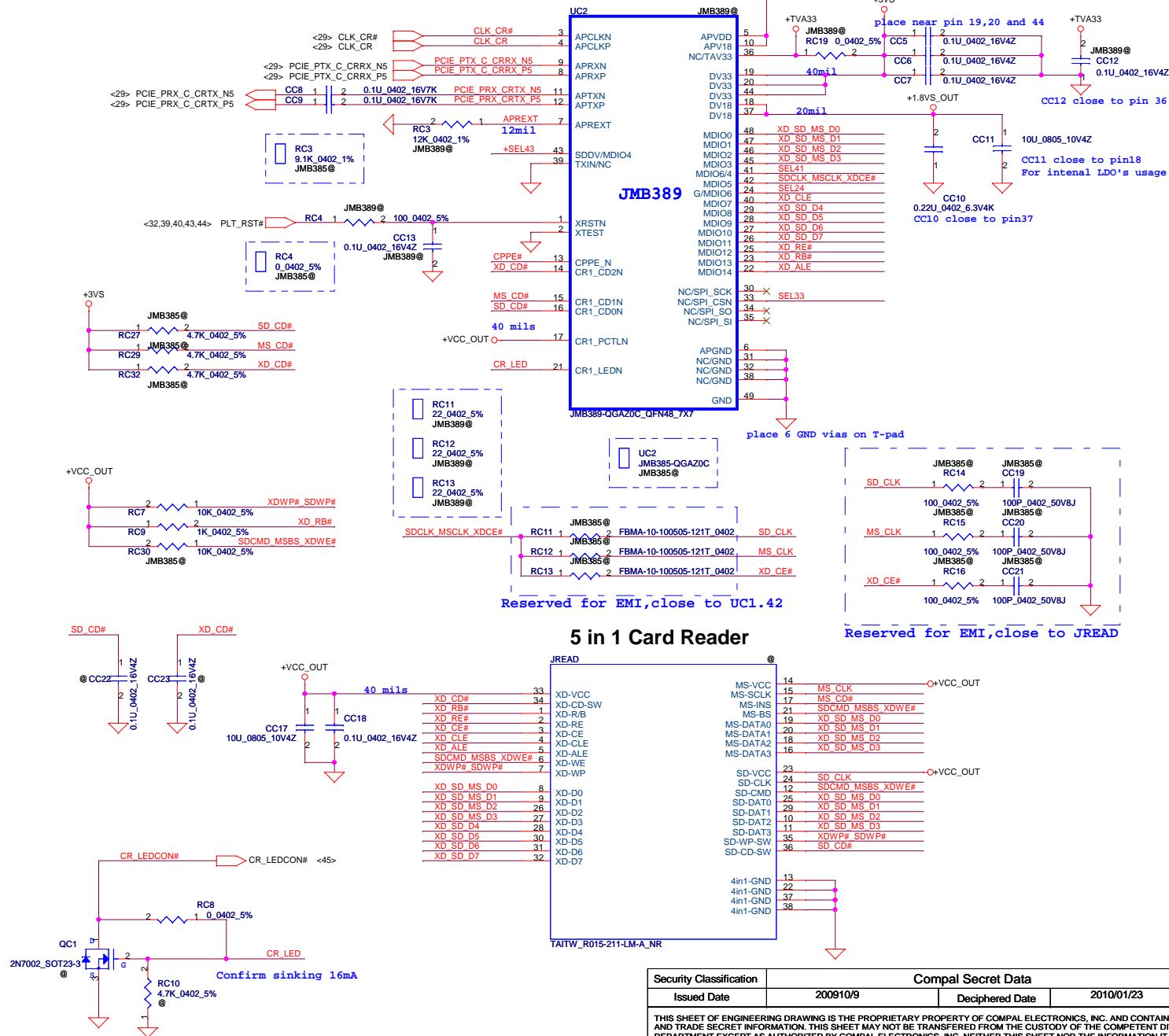
WLAN/ WiMax

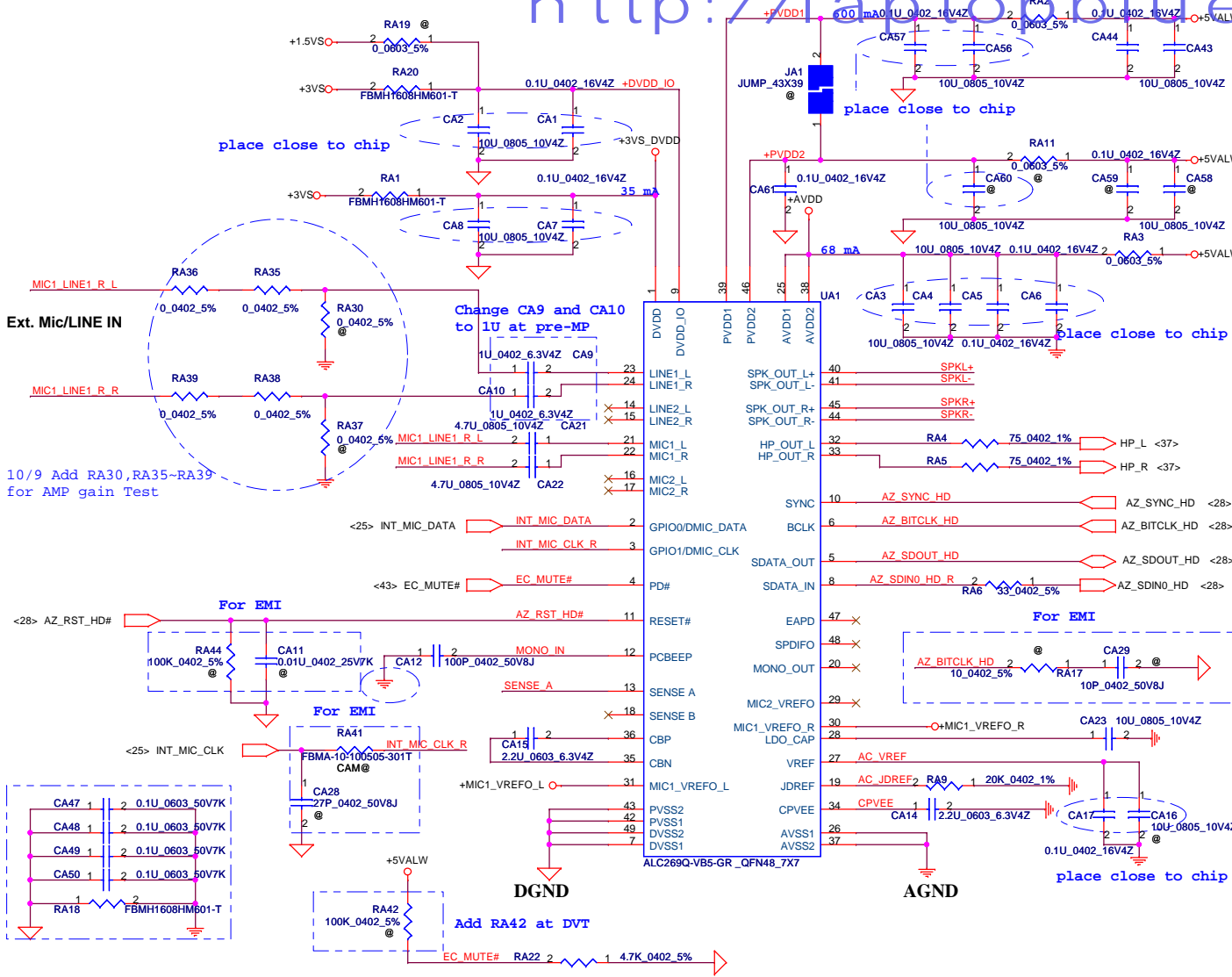
Debug card using



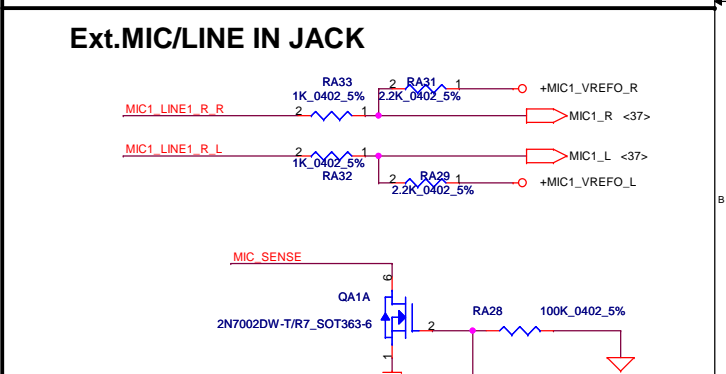
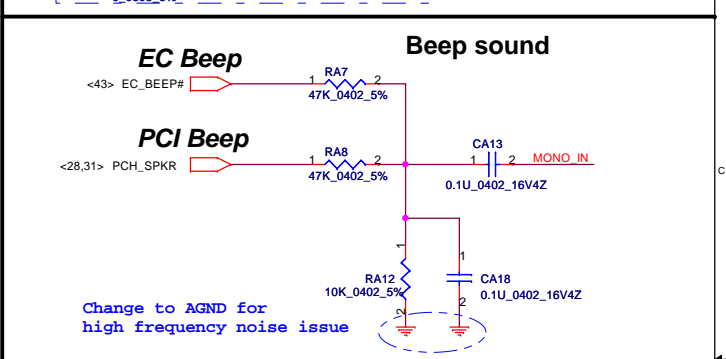
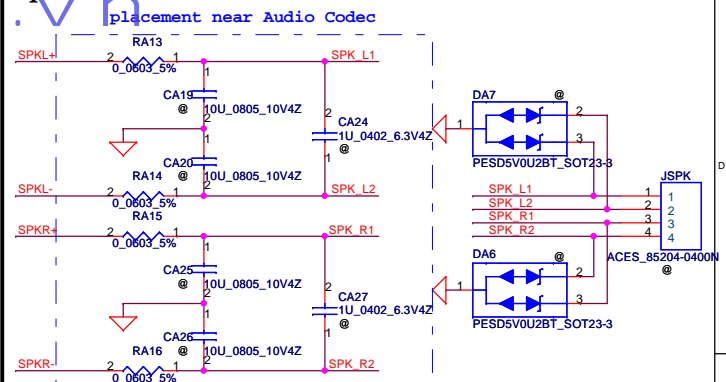
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						Date:	Wednesday, March 24, 2010	Sheet 39 of 59

JMB389C / JMB385C

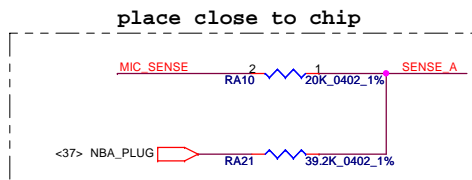




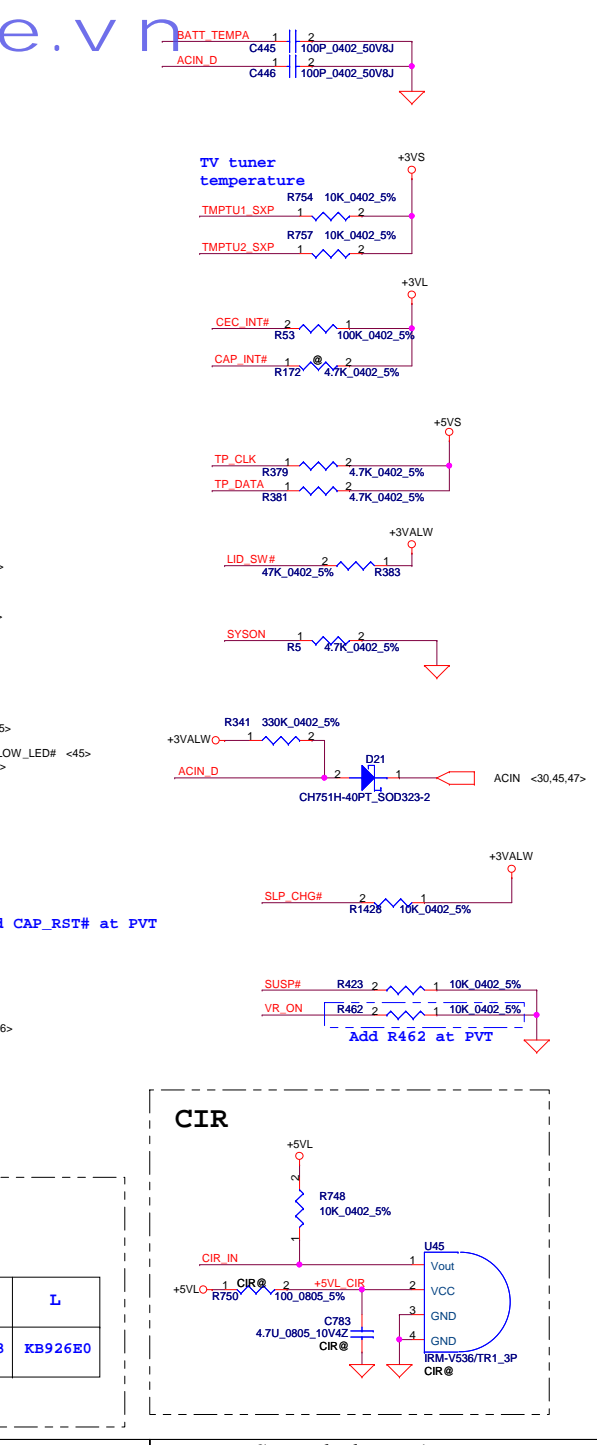
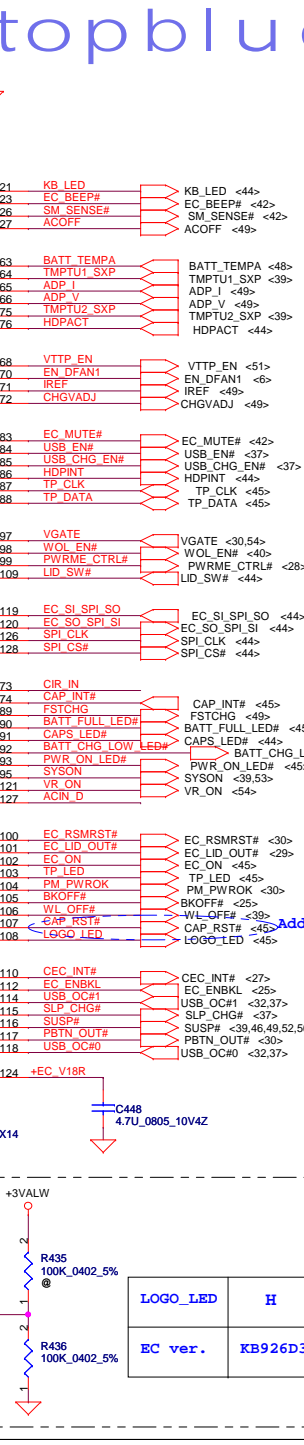
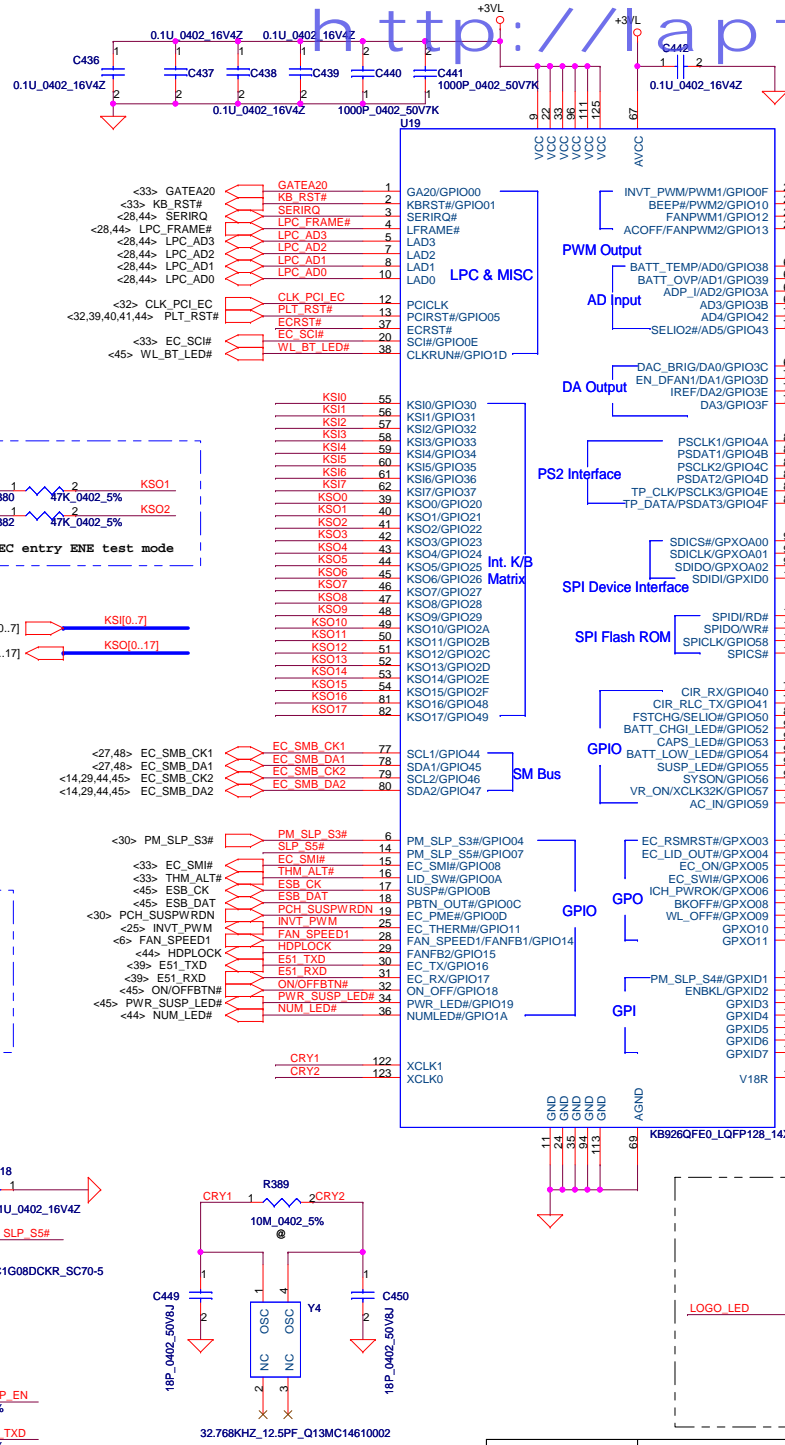
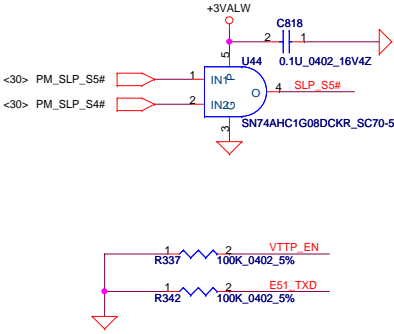
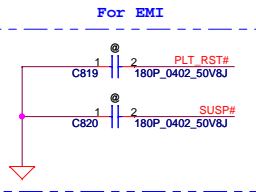
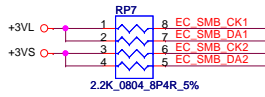
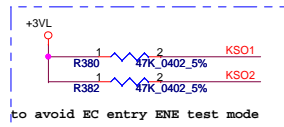
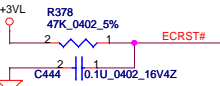
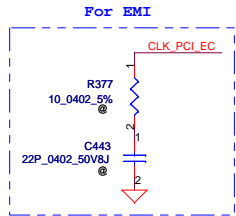
Speaker Connector



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

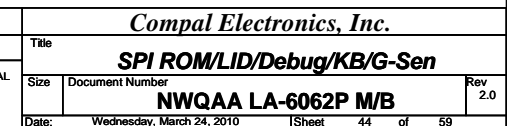
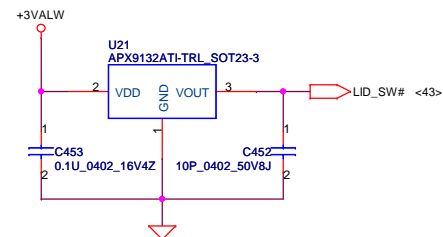


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				Date: Wednesday, March 24, 2010	
				Sheet 42 of 59	

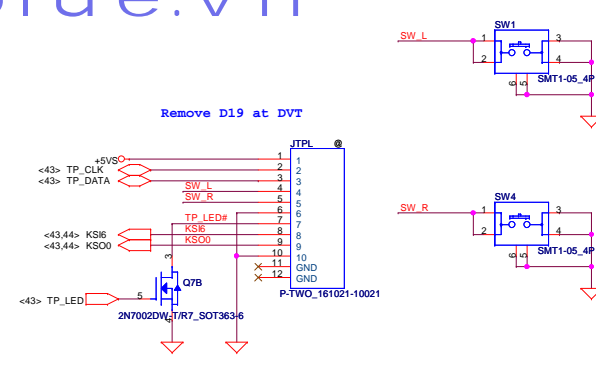


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Date: Wednesday, March 24, 2010				Sheet	43 of 59

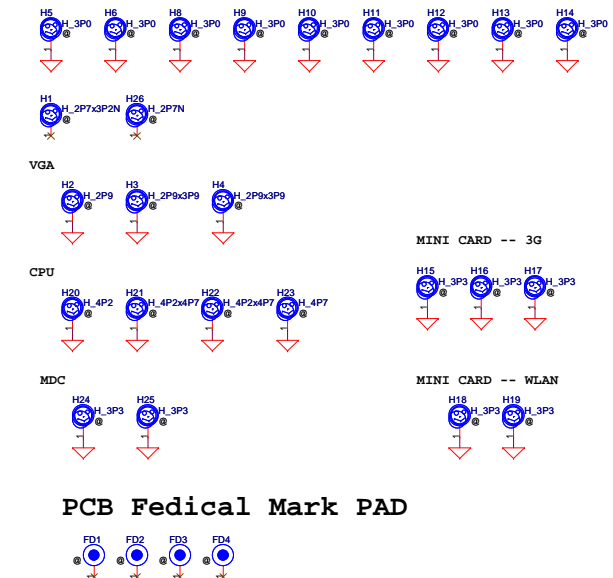
Id	SW	LPC Debug Port
1	h	http://laptopblue.v



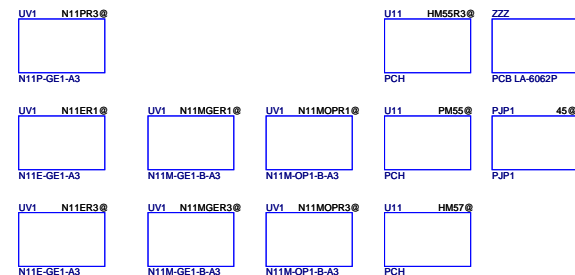
Touchpad & Light Pipe Connector



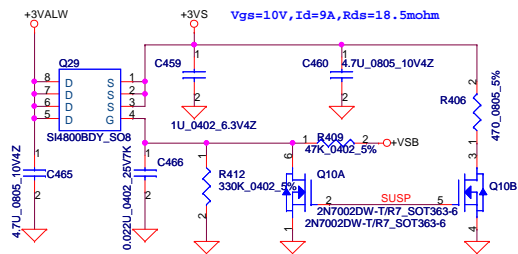
PCB Fedical Mark PAD



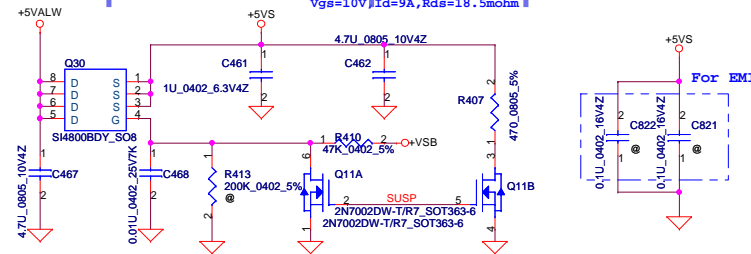
ISPD



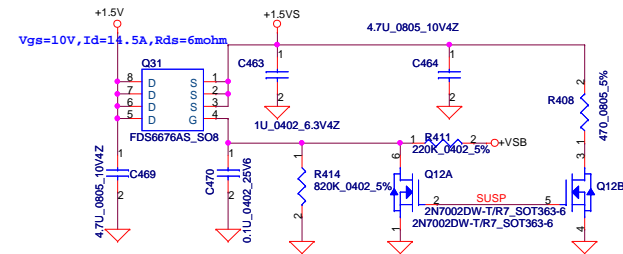
+3VALW TO +3VS



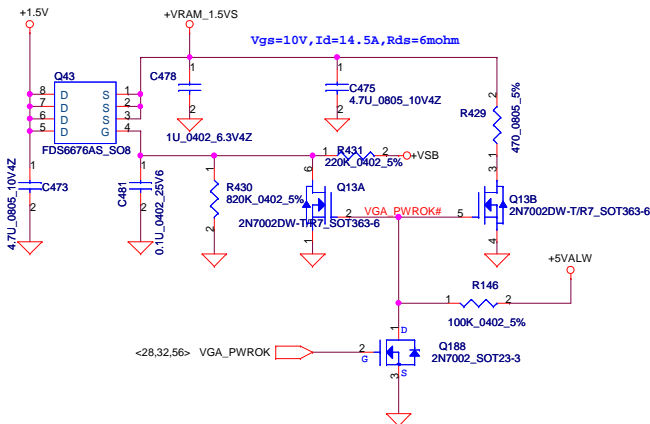
+5VALW TO +5VS



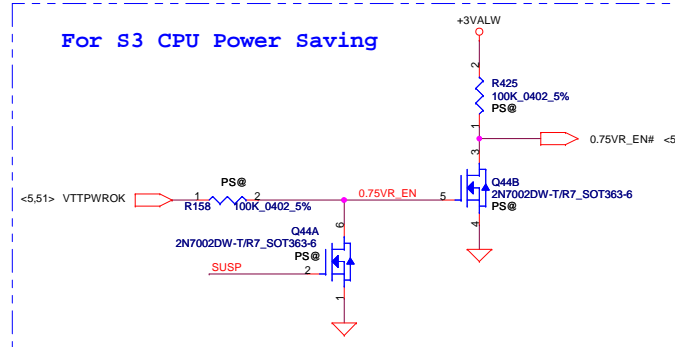
+1.5V to +1.5VS



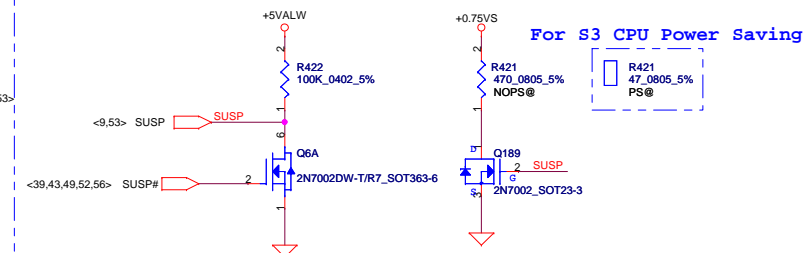
+1.5V to +VRAM_1.5VS



For S3 CPU Power Saving

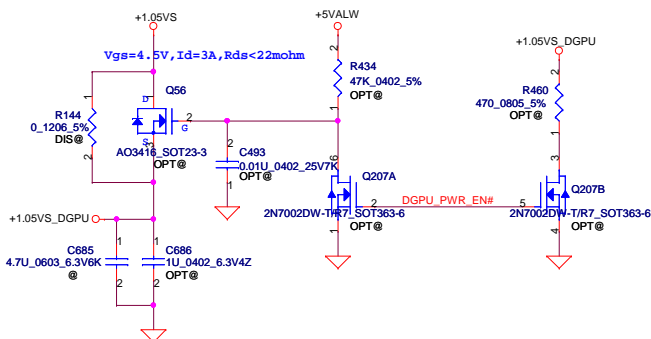


For S3 CPU Power Saving

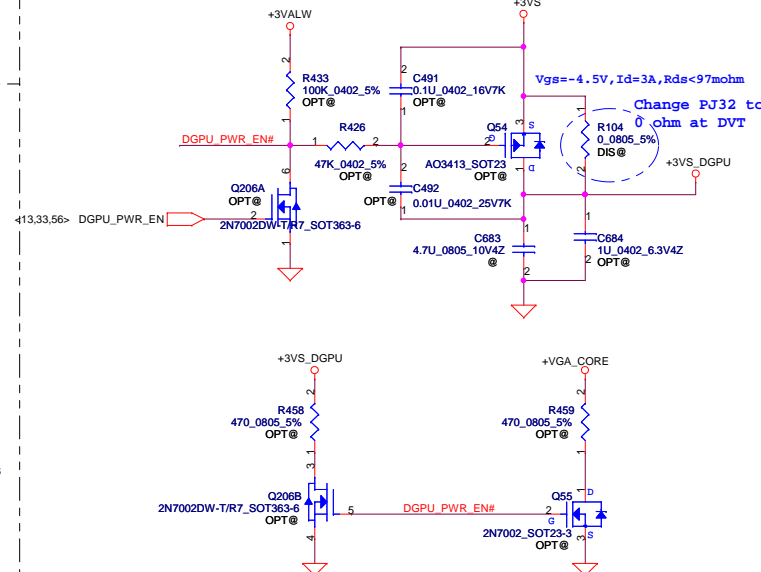


+1.05VS to +1.05VS_DGPU

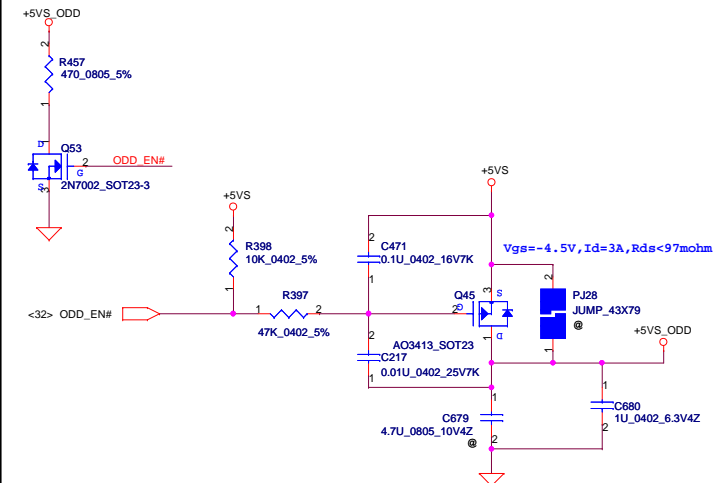
Change +1.05VS_DGPU circuit to N-channel MOS at PVT



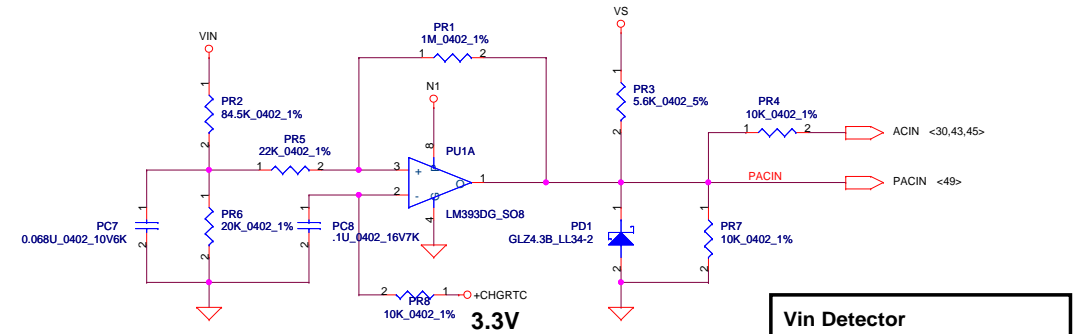
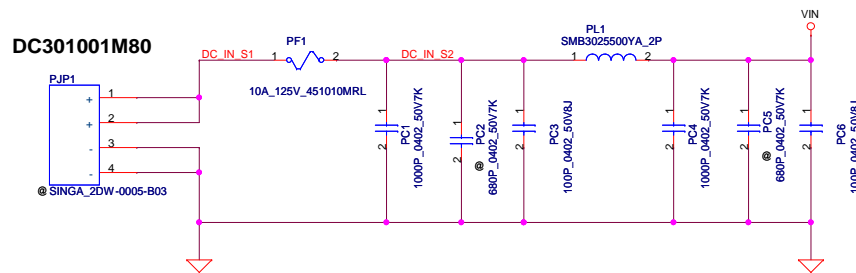
+3VS to +3VS_DGPU



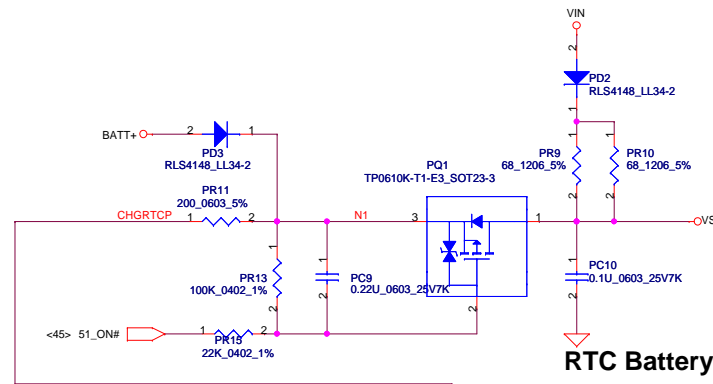
+5VS TO +5VS_ODD



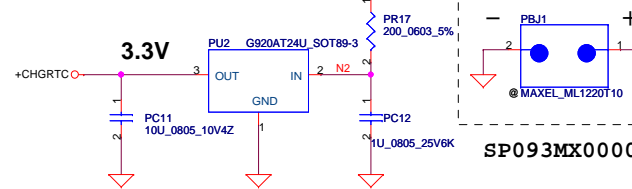
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Issued Date	200910/9	Deciphered Date	2010/01/23	Title	DC-DC INTERFACE
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				NWQAA LA-6062P M/B	2.0
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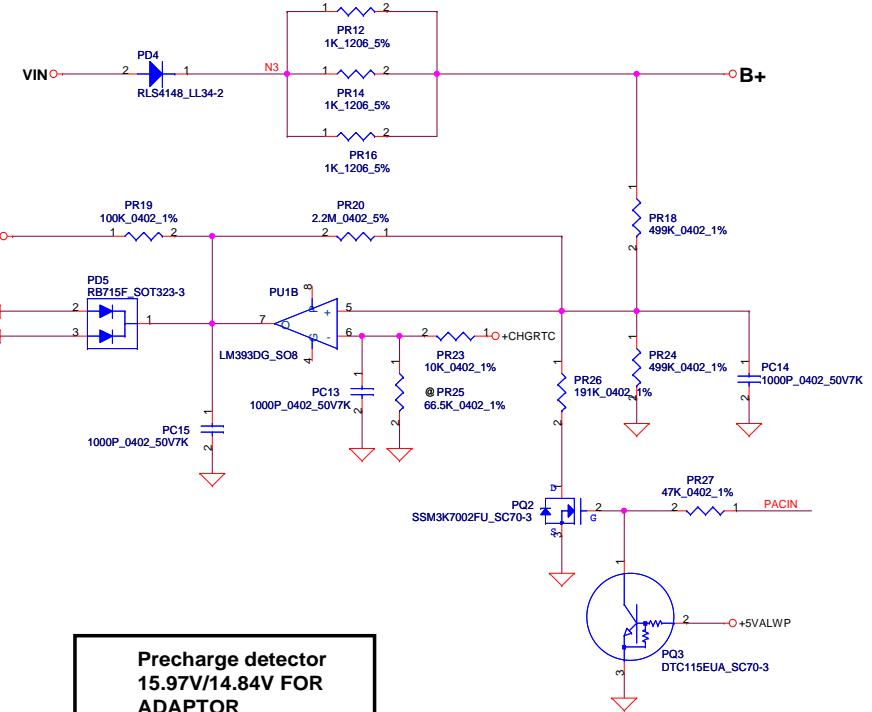
Vin Detector		
High	18.384	17.901 17.430
Low	17.728	17.257 16.976



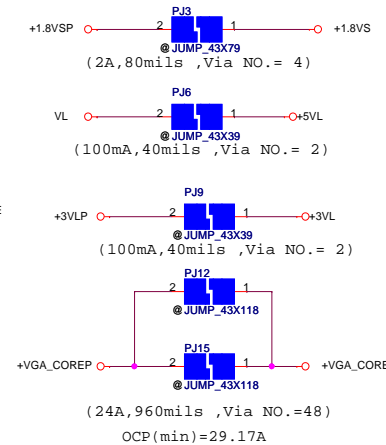
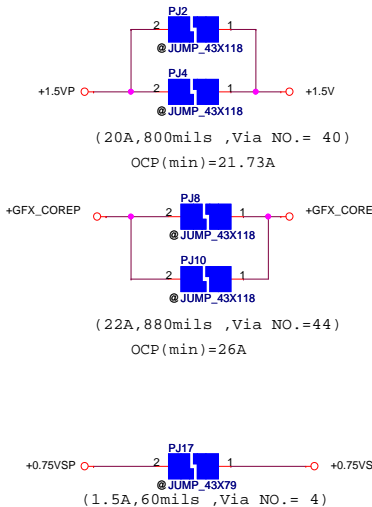
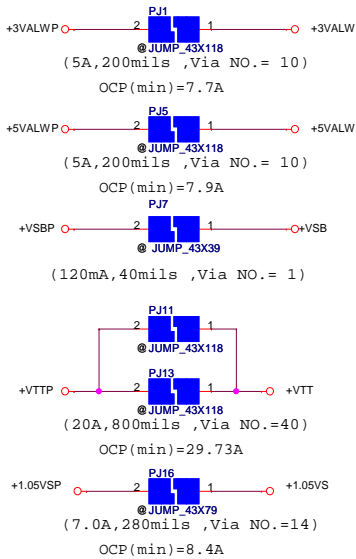
RTC Battery



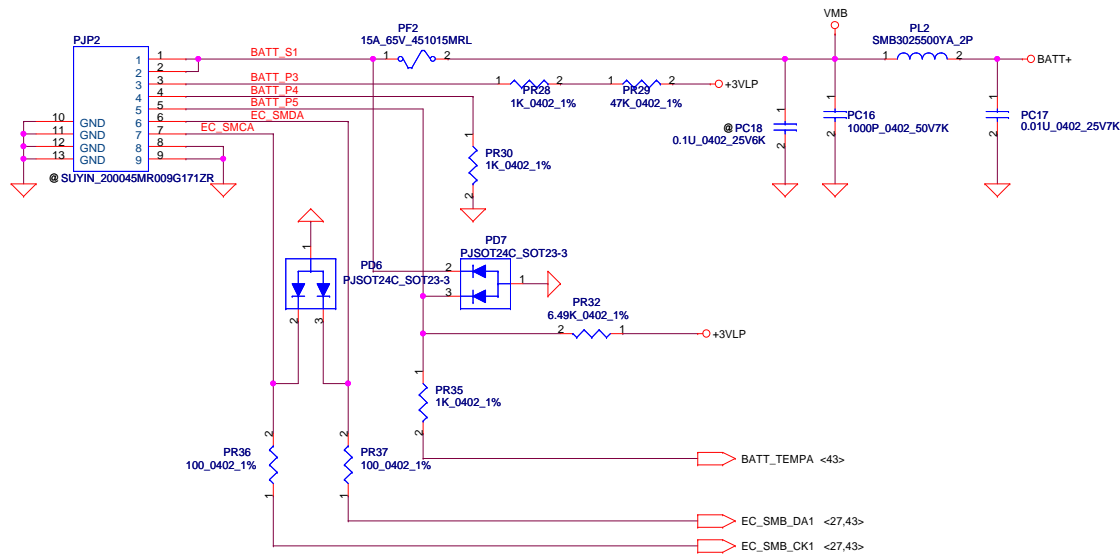
SP093MX0000



Precharge detector
15.97V/14.84V FOR
ADAPTOR



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				Document Number
				NWQAA LA-6062P M/B
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				2.0
				Date
				Wednesday, March 24, 2010
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				47 of 59

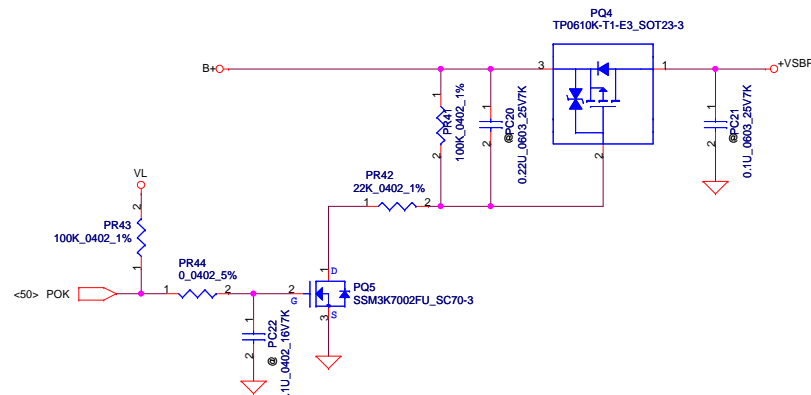
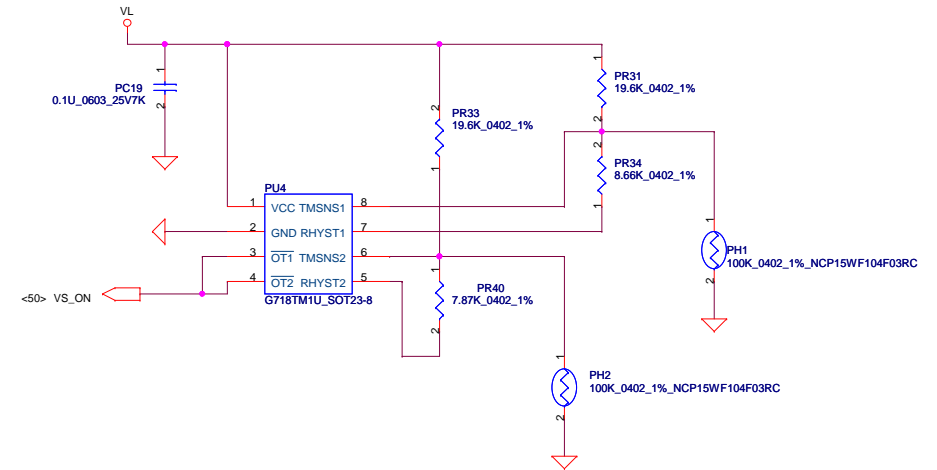


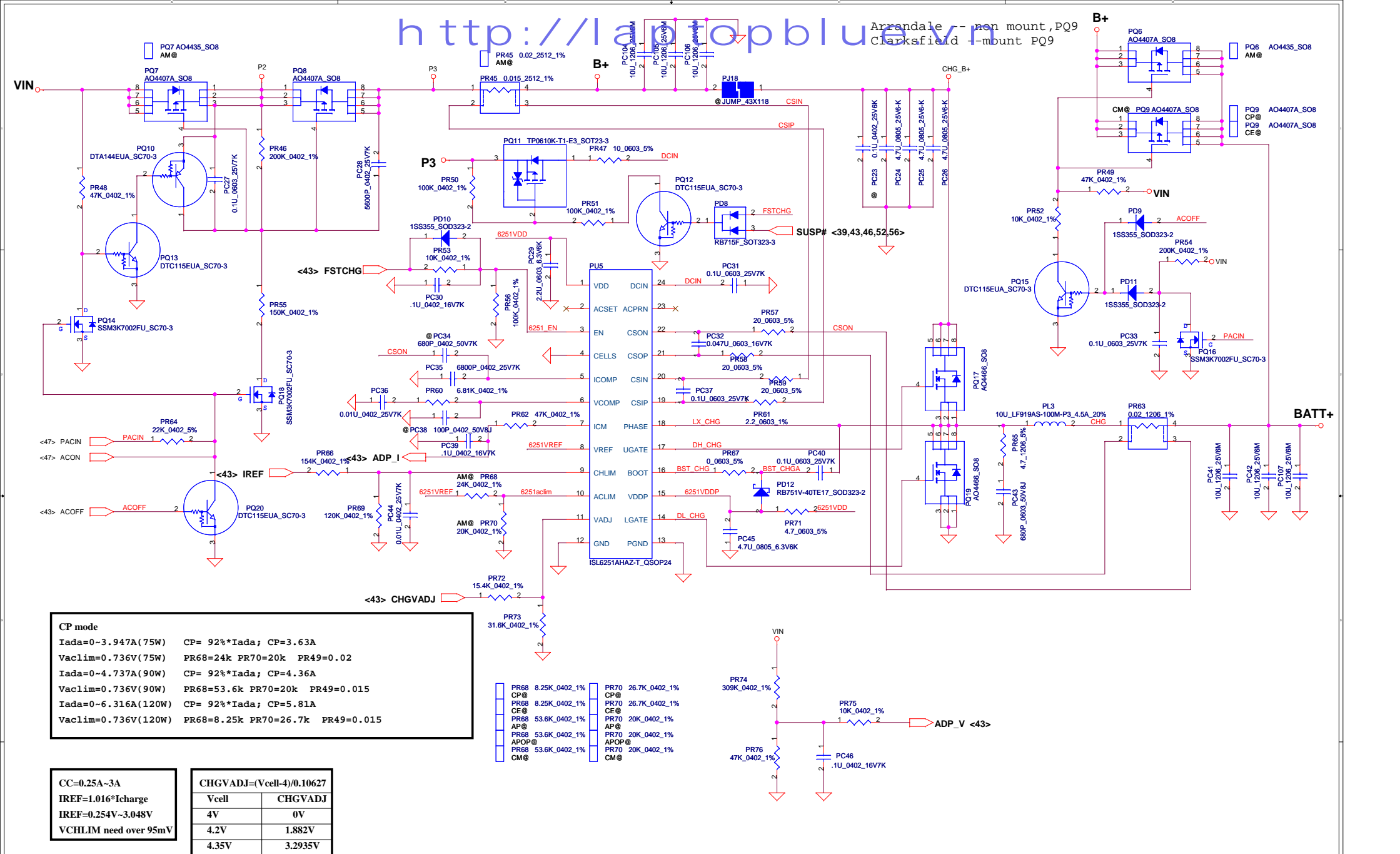
PH1 under CPU botten side :

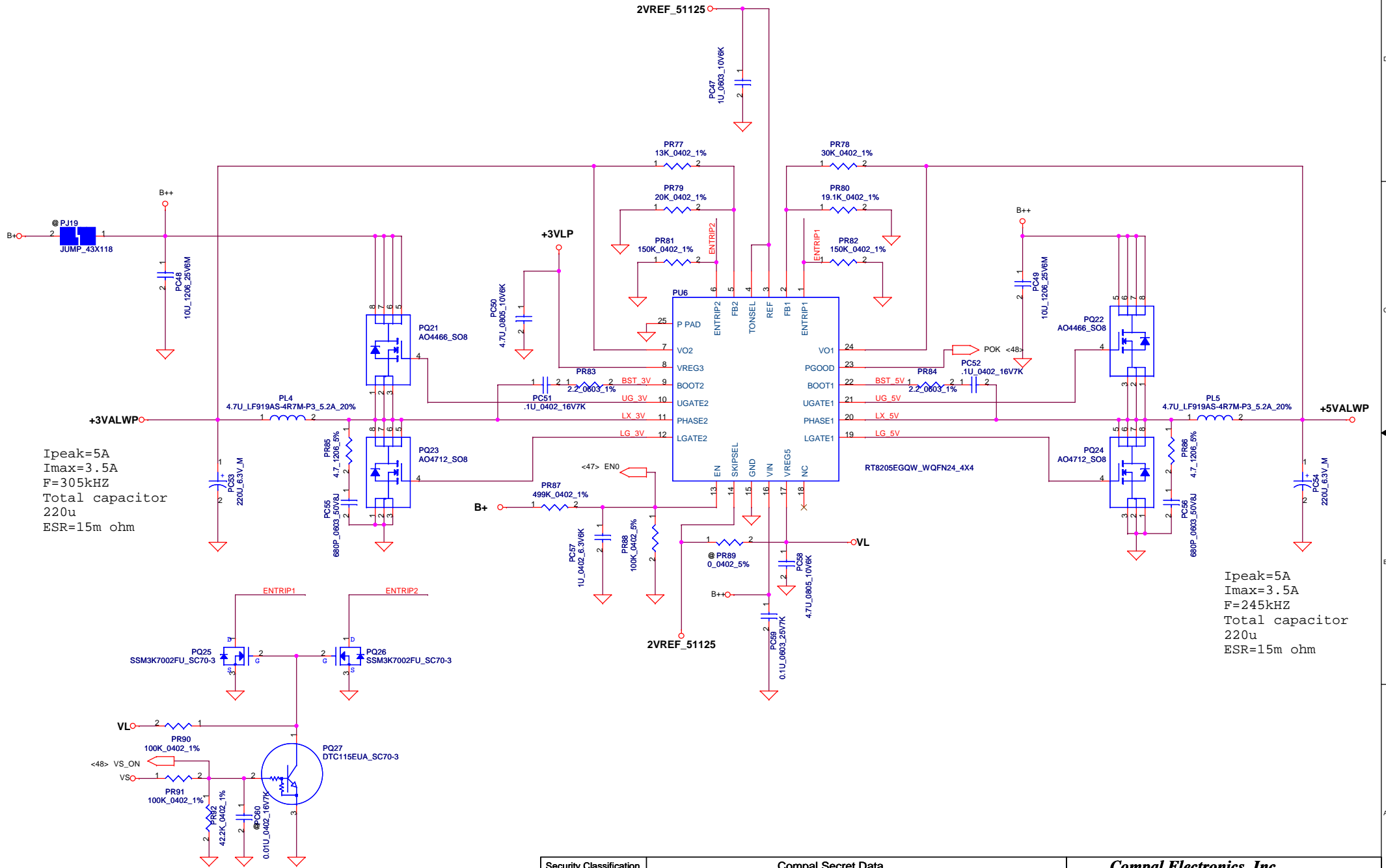
CPU thermal protection at 95 degree C
Recovery at 56 degree C

PH2 near main Battery CONN :

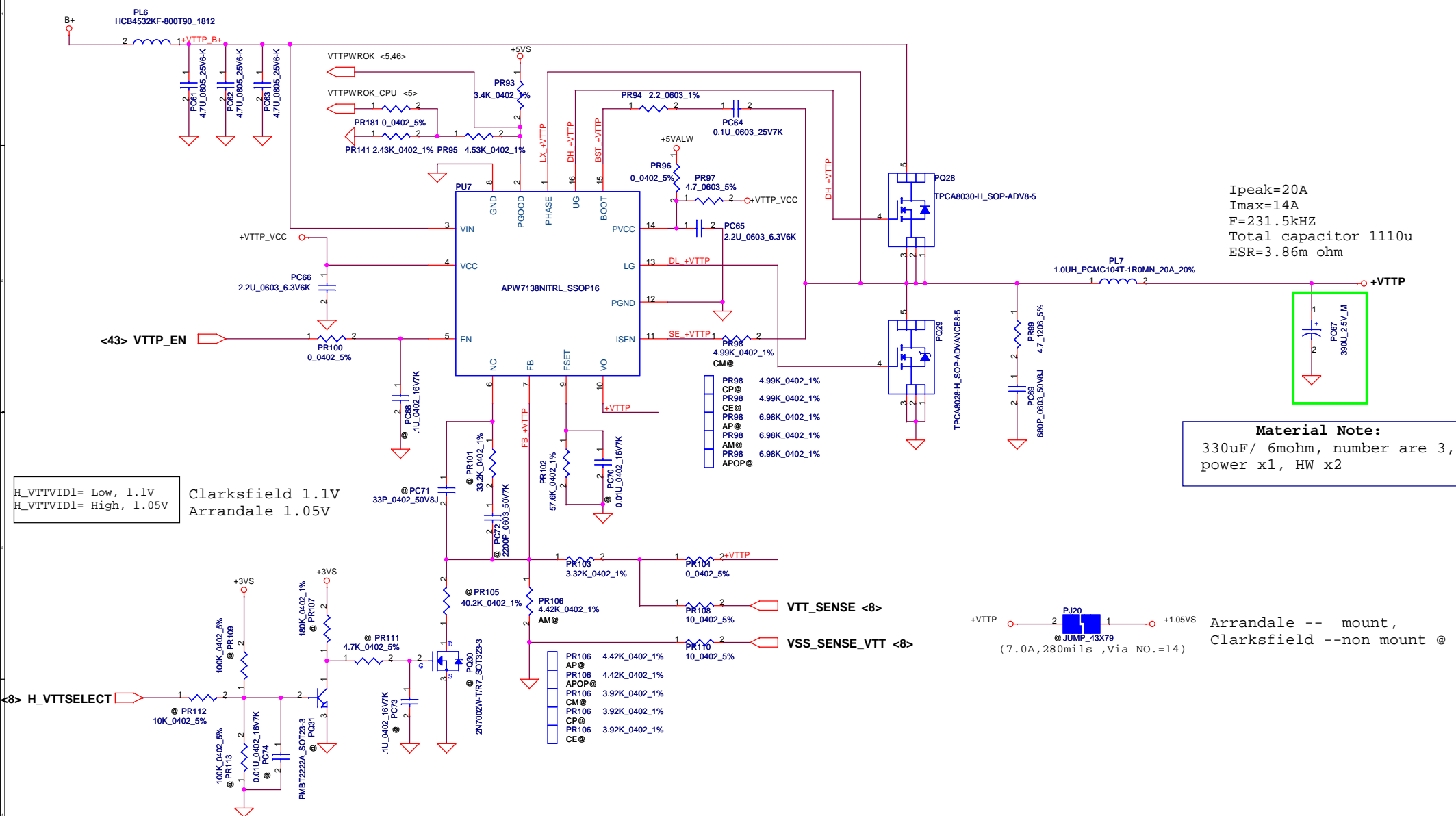
BAT. thermal protection at 95 degree C
Recovery at 48 degree C



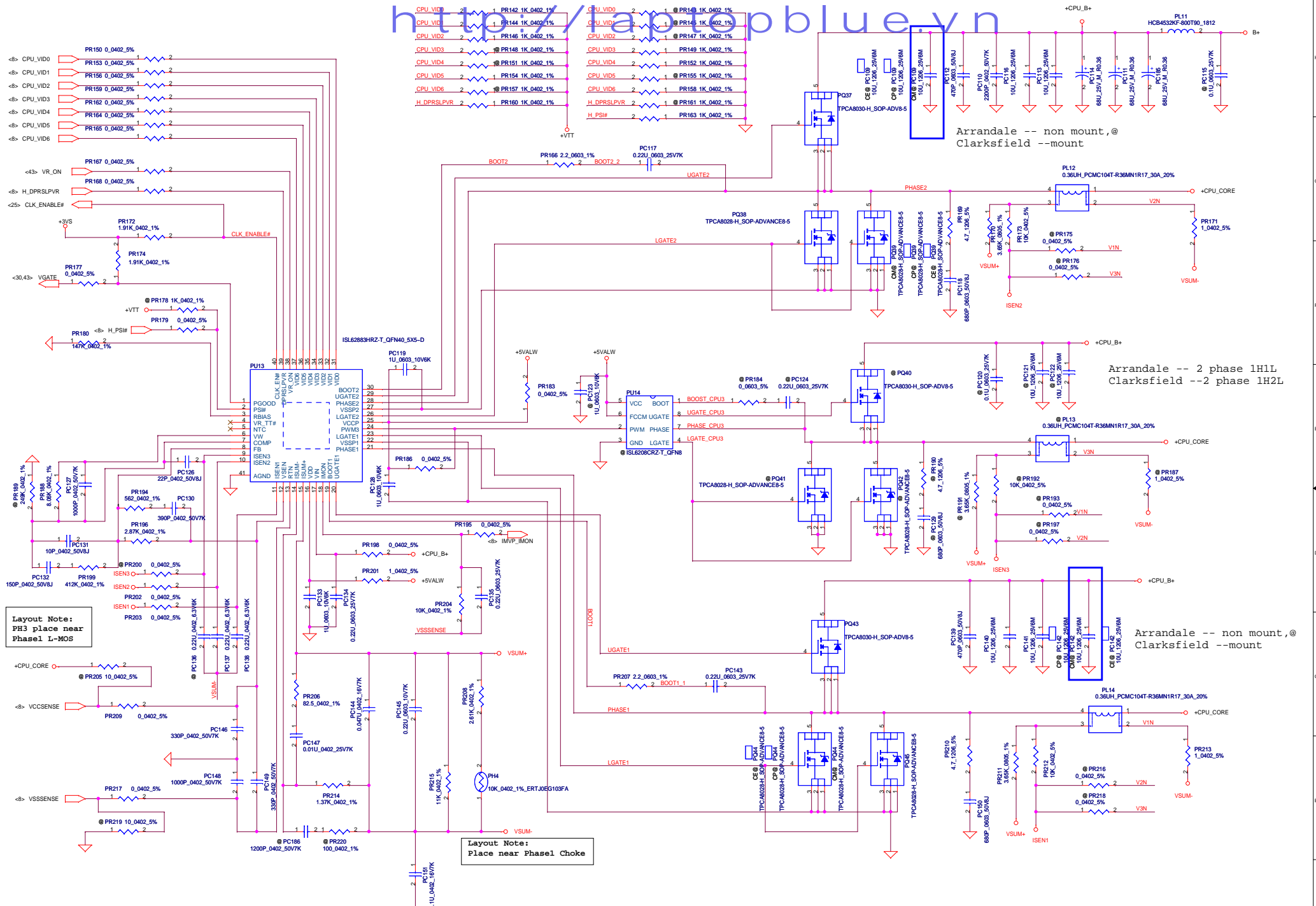


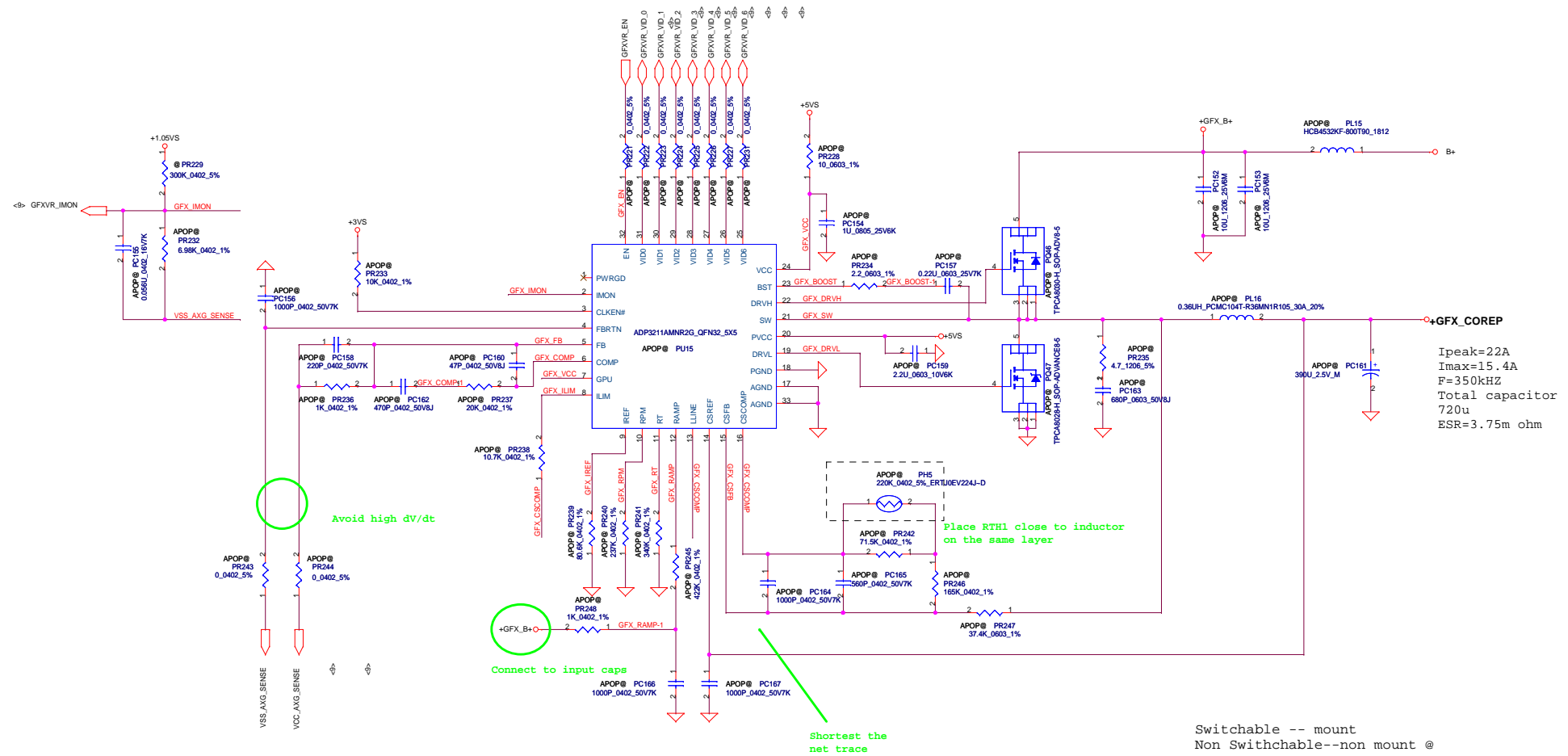


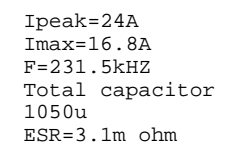
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Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title	
				3VALWP/5VALWP	
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				NWQAA LA-6062P M/B			
				Date:			

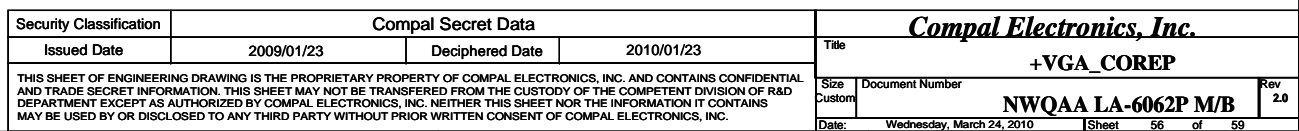






N11M-GE1/OP1	N11P-GE1	N11E-GE1_LP
Imax=16.09A Ipeak=18.19A Iocp=20.72A	Imax=16.8A Ipeak=24A Iocp=29.17A	Imax=16.8A Ipeak=24A Iocp=29.17A
PR255=5.36K PQ50=unpop	PR255=7.15K PQ50=unpop	PR255=7.15K

GPU_VID0	GPU_VID1	N11M-GE1/N11M-OP1	N11P-GE1	N11E-GE1-LP
0	0		0.80V	0.80V
1	0	0.85V	0.85V	0.85V
0	1			
1	1	1.03V	0.95V	0.9V
		PR260 = 4.75K PR262 =14K PR261 =56.2K PR263=16.2K	PR260 = 4.75K PR262 =14K PR261 =56.2K PR263=29.4K	PR260 = 4.75K PR262 =14K PR261 =56.2K PR263=63.4K



NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
EVT		P53-PWR_1.5VP/0.75VSP	Change PR132 18k to 6.19k	Modify 1.5V OCP to 18.09A (2009/11/25)
EVT		P56-PWR_VGA_COREP	Change PR270 0 to 100 Ohm	Adjust RC for Optimus sequence (2009/11/25)
			Change PC178 0.1U to 0.01U	
EVT		P39-PWR_+VTTTP	Change PR141 2.26k to 2.43k	Modify VTTTPWROK voltage (2009/11/25)
EVT		P39-PWR_+VTTTP	Remove PC71 33P, PC72 2200P, PR101 33.2k	APW7138 not use this function (2009/11/25)
EVT		P38-PWR_3VALWP/5VALWP	Change PR92 49.9k to 42.2k	Modify VS divider voltage to drive MOS (2009/11/25)
EVT		P56-PWR_VGA_COREP	Remove PC179 22P, PC181 2200P, PR258 49.9k	APW7138 not use this function (2009/11/25)
EVT		P56-PWR_VGA_COREP	Change PR255 7.15k to 9.09k	Modify VGA 11P OCP to 38.03A (2009/11/25)
EVT		P56-PWR_VGA_COREP	Remove PC177 10U	FAE suggest to remove 1 10U cap for IC on time control (2009/11/25)
EVT		P42-PWR_CPU_CORE	Change PL12,PL14 SH0000005680 to SH000000IK00	Use 5% DCR choke (2009/11/25)
EVT		P43-PWR_GM VGA_CORE	Change PH5 SL200000058L to SL2000000500	Use Compal PN (2009/11/25)
DVT		P56-PWR_VGA_COREP	Change PR255 9.09k to 7.15k	Modify VGA 11P OCP to 29.17A (2009/12/28)
DVT		P43-PWR_GM VGA_CORE	Change PL16 SH000000HK00 to SH000000IK00	Use same PN choke (2009/12/28)
DVT		P39-PWR_+VTTTP	Change PR106 4.42k to 3.92k	Modify VTT voltage to 1.1V for Clarkfield (2009/12/28)
DVT		P42-PWR_CPU_CORE	Change PC114, PC111, PC185 from SF000000F80 to SF000000W00	Cost down (2009/12/28)
DVT		P43-PWR_GM VGA_CORE	Change PC161 to SGA000002680	For DVT budding(thermal issue), it will change to original type for PVT (2009/12/28)
DVT		P56-PWR_VGA_COREP	Change PR253 0 to 20k	For VGA sequence(2009/12/28)
DVT		P56-PWR_VGA_COREP	Change PR270 0 to 20k	For VGA sequence(2009/12/28)
DVT		P52-PWR_1.05VSP/1.8VSP	Add PC83 0.1U and change PR122 0 to 68k	For VGA sequence(2009/12/28)
DVT		P48-PWR_BATTERY CONN / OTP	Add PD6, PD7 ESD diode	For ESD solution(2009/12/28)
DVT		P49-PWR_CHARGER	Add PC104,PC105,PC106 10U	Reserve for EMI solution(2009/12/28)
DVT		P50-PWR_3VALWP/5VALWP	Change PR83,PR84 0 to 2.2	Add boost resistor(For EMI solution)(2009/12/28)
			Add PR85,PR86 4.7 and PC55,PC56 680P	Add snubber(For EMI solution)(2009/12/28)
DVT		P42-PWR_CPU_CORE	Change PR166,PR207 0 to 2.2	Add boost resistor(For EMI solution)(2009/12/28)
			Add PR169,PR210 4.7 and PC118,PC150 680P	Add snubber(For EMI solution)(2009/12/28)
DVT		P55-PWR_GM VGA_CORE	Change PR234 0 to 2.2	Add boost resistor(For EMI solution)(2009/12/28)
			Add PR235 4.7 and PC163 680P	Add snubber(For EMI solution)(2009/12/28)
DVT		P56-PWR_VGA_COREP	Add PR254 4.7 and PC175 680P	Add snubber(For EMI solution)(2009/12/28)
DVT		P48-PWR_BATTERY CONN / OTP	Change PR33 10k,PR31 21k to 19.6k, PR34 9.53k to 8.66k, PR40 47k to 7.87k	Adjust OTP setting point(2009/12/28)
DVT		P42-PWR_CPU_CORE	Add PQ39,PQ44 TPCA8028-H	Use 1H 2L MOS solution for Clarksfield (2009/12/31)
DVT		P42-PWR_CPU_CORE	Add PC109,PC142 10U input cap	For Clarksfield solution (2009/12/31)
DVT		P42-PWR_CPU_CORE	Change PR214 1.2k to 1.37k	Adjust CPO_CORE OCP to 65A (2009/12/31)
DVT		P42-PWR_CPU_CORE	Change PR196 2.43k to 2.87k	Adjust CPU_CORE load line (2009/12/31)
DVT		P42-PWR_CPU_CORE	Change PR204 8.25k to 10k	Adjust resistor for Imon (2009/12/31)
DVT		P39-PWR_+VTTTP	Change PR98 4.99k to 6.98k	Adjust VTT_DIS_Arrandale OCP to 29.73A (2009/12/31)
DVT		P53-PWR_1.5VP/0.75VSP	Change PR132 6.19k to 7.5k	Adjust 1.5V OCP to 21.73A(2009/12/31)
DVT		P52-PWR_1.05VSP/1.8VSP	Change PQ33 from FDS6670 to AO4712	Change design rating(2009/12/31)
DVT		P39-PWR_+VTTTP	Change PR98 6.98k to 4.99k	Adjust VTT_DIS_Clarksfield OCP to 20.64A (2009/12/31)
DVT		P55-PWR_GM VGA_CORE	Change PR247 34.8k to 37.4k	Adjust GFX load line (2009/12/31)
DVT		P41-PWR_0.75VSP/1.8VSP	Change PC90 SE025681K80 to SE024681J80	Use same PN (2009/12/31)
DVT		P56-PWR_VGA_COREP	Change PR270 20k to 68k, PC178 0.01U to 0.1U	Adjust Optimus sequence (2010/01/06)
PVT		P41-PWR_0.75VSP/1.8VSP	Remove PR136, Add PR137 0 Ohm	For S3 power saving function (2010/02/03)
PVT		P43-PWR_GM VGA_CORE	Change PC161 to SF0000002000	Change to original type for PVT (2010/02/03)
PVT		P49-PWR_CHARGER	Change PC24,PC25,PC26 4.7U to 10U	For EMI solution(ISN test) (2010/02/03)
PVT		P49-PWR_CHARGER	Add PC107 10U	For EMI solution(ISN test) (2010/02/03)
PVT		P49-PWR_CHARGER	Add PC104,PC105,PC106 10U	For EMI solution(ISN test) (2010/02/03)
PVT		P38-PWR_3VALWP/5VALWP	Change PQ27 from SSMK7002 to DTC115EUA	Use low Vth Transistor (2010/02/03)
PVT		P52-PWR_1.05VSP/1.8VSP	Change PR119 10k to 15.8k	Adjust 1.05V OCP to 8.47A (2010/02/03)

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				Size	Document Number	Rev
					Calpella common	2.0
Date:		Tuesday, March 23, 2010		Sheet	57	of 59

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
Pre MP		P52-PWR_1.05VSP/1.8VSP	Change PR123 316k to 24.5k,PR124 402k to 51.1k	Adjus 1.8V voltage divided resistor (2010/03/07)
Pre MP		P52-PWR_1.05VSP/1.8VSP	Change PU9 from MP2121 to SY8033	MP2121 ESD fail (2010/03/07)
Pre MP		P52-PWR_1.05VSP/1.8VSP	Delete PR125 0 Ohm	Change for SY8033 solution(2010/03/07)
			Change PC85 from 0.1U to 22U	
			Delete PC87 10UF, PC84 0.1U	
Pre MP		P52-PWR_1.05VSP/1.8VSP	Change PC86 10U to 68P	Improve 1.8V transient under shoot(2010/03/07)
Pre MP		P49-PWR_CHARGER	Change PC24,PC25,PC26 10U to 4.7U	10U 0805 size price too high(2010/03/07)
Pre MP		P47-PWR_DCIN/DECTOR	Change PC12 from SE033105Z80 to SE000001380	Change PN(2010/03/07)
Pre MP		P49-PWR_CHARGER	Change PR68 from 53.6k to 24k, PR45 from 0.015 to 0.02 Ohm	Change CP from 90W to 75W(For cost down)(2010/03/07)
Pre MP		P49-PWR_CHARGER	Change PQ6,PQ7 from AO4407A to AO4435	Change MOS reting for 75W adapter(For cost down)(2010/03/07)
Pre MP		P56-PWR_VGA_COREP	Add PR264,PR267 100k	Use 100k resistor to pull high +3VS_DGPU(Set initial VID to P0 state)(2010/03/07)

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		Power PIR			
		Size	Document Number		
		Calpella common			Rev 2.0
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HW PIR (Product Improve Record)

NWQAA LA-6062P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 TO 0.2

GERBER-OUT DATE: 2009/12/30

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	12/7	37	Add +5VALW and +5VL for JPIO pin5	For BACK_SENSE detect
2	12/7	46	Change PJ32 to R104 and PJ33 to R144	For discrete BOM structure
3	12/7	25	Remove JLVDS pin10 and pin12 for +LCDVDD_R	3D Panel max. current is 1.5A
4	12/8	45	Combine JTOUCH and JLP to JTPL and remove C648	For ME cost down
5	12/8	13	Add QV2, RV110, RV123 and RV124	For CLK_REQ_VGA# level shifter
6	12/14	25	Add C495 and C496	For RF request
7	12/15	33	Add R258	For OPTIMUS_EN#
8	12/15	34	Add C499	For power team request
9	12/17	45	Remove D19	Move D19 to L8-6061P
10	12/18	38	Reverse JBT pin definition	Due to pin reverse
11	12/18	42	Add RA42	For codec EC_MUTE# issue
12	12/21	41	Change JREAD to Push-push type (R015-211-1M-A)	For PRD update
13	12/21	25	Move LED_PWM and BKOFF#_R to JLVDS pin10 and pin12	For avoiding +LCD_INV short issue
14	12/22	44	Change H7 footprint to "DEBUG_PAD-MB-S"	For debug use
15	12/23	39	Add D24 and Q36 for BT_CTRL	For WLAN & BT combo module
16	12/23	33	Add R461	For CIR_EN#
17	12/24	25	Mount C236 and C268	For ESD request
18	12/24	37	Change JPIO footprint and reverse its pin definition	For ME request
19	12/24	27	Add R145	For U9 ESD damage issue
20	12/24	41	Add F3	For connector short issue
21	12/28	42	Change RA41 to SM01000CY00 (FBMA-10-100505-301T)	For EMI request
22	12/28	25	Remove L1	For 3D panel
23	12/29	42	Change RA1, RA18 and RA20 to SM01000B200	For RF request
24	12/29	25	Change C484 to 100P	For RF request
25	1/6	37	Change C426 to SF000001500	For cost down
26	1/12	38	Change R132 BOM from FELICA@ to FELICA@	For Felica issue
27	1/12	11	Change C218 to SF0000002000	For cost down
28	1/12	8	Change C144 to SF0000002200	For thermal interfere issue

NWQAA LA-6062P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.2 TO 0.3

GERBER-OUT DATE: 2010/02/08

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	1/15	42	Add RA43	For sleep & music on battery mode
2	1/15	46	Change +1.05VS_DGPU to N-MOS	For +1.05VS_DGPU drop issue
3	1/21	43	Add R462	Avoid VR_ON floating
4	1/25	44	Change UG3 to SA000022I00	For LDO issue
5	1/25	45	Change SW2 to @	For ME interfere issue
6	1/27	9	Change CV57, CV58 abd C271 to OS-CON	For cost down
7	2/1	25	Add +LCD_VDD to JLVDS pin18	For CMO 3D Panel
8	2/1	27	Add R208	For AOC monitor issue
9	2/1	43	Change U19 to SA00001J5A0	For KB926 E0 version
10	2/1	39	Add +1.5VS for J3G	For TV tuner MC770A
11	2/1	41	Remove F3	For UCL ES2 sample
12	2/2	43	Add CAP_RST# to EC	For ESD issue
13	2/3	41	Change RC7 to 33 ohm	For EMI request
14	2/4	42	Remove RA40, add RA44 and RA22	For audio issue
15	2/4	14	Reserve VBIOS ROM	For SW request
16	2/5	32	Swap USB port4 and port8	For customer request
17	2/5	13	Reserve 27MHz crystal	For HDMI issue
18	2/9	40	Change L11 to 2.2U and C113 to 4.7U	For Realtek request
19	2/10	41	Change RC7-RC14 to 22 ohm	For O2 request
20	2/10	27	Remove HDMI common mode choke	For cost down

NWQAA LA-6062P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.3 TO 1.0

GERBER-OUT DATE: 2010/03/15

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	3/6	32	Change R390 to 1K	For Optimus sequence
2	3/6	33	Change R59 to 1K	For Optimus sequence
3	3/6	27	Change Q18 and Q19 power to +3VS_DGPU	For GPU power rail
4	3/6	41	Add QC2 and RC16	For O2 B0 workaround
5	3/7	28	Change D13.2 power to +CHGRTC	For RTC issue
6	3/8	32	Add R333 and R334	For Optimus sequence
7	3/8	25	Add BOM structure 3D@ and NO3D@	For 3D SKU PWM
8	3/8	13	Change YV1 to SJ100006R00	For cost down
9	3/11	46	Change C685 to 0603 size	For ME height limit
10	3/11	45	Change H15-H19 to H_3P3	For ME request
11	3/15	45	Remove SW2	For ESD request
12	3/15	42	Change CA9 and CA10 to 1U	For cut-off frequency
13	3/16	42	Change MONO_IN to AGND	For high frequency noise issue

NWQAA LA-6062P SCHEMATIC CHANGE LIST

REVISION CHANGE: 1.0 TO 2.0

GERBER-OUT DATE: 2010/03/19

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	3/17	41	Change cardreader to JMB385/389	For customer request
2	3/18	34	Add R49	For CRT wave issue
3	3/19	13	Change LV3 to always stuff	For NVIDIA request
4	3/19	34	Change L12 to 2.2 ohm for Optimus SKU	For CRT wave issue
5	3/22	27	Add D54	For HDMI CEC issue
6	3/24	25	Chane C214 to 1U	For NALAA ESATA performance low issue